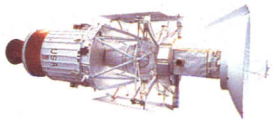
DATA CONVERTER REFERENCE MANUAL VOLUME I





D/A CONVERTERS • S/D CONVERTERS •
COMMUNICATIONS PRODUCTS •
DIGITAL PANEL METERS • DSP COMPONENTS •
BUS INTERFACE AND SERIAL I/O PRODUCTS •
ASICs • POWER SUPPLIES

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS IS VOLUME I OF THE DATA CONVERTER REFERENCE MANUAL

It and its companion volume contain Data Sheets, Selection Guides and a wealth of background information on signal conversion and a wide variety of components for mixed signal processing.

It is one member of a four-volume set of reference manuals describing and specifying Linear, Converter and Audio/Video products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of any data sheet in this volume or Volume II. You will find additional references for product categories not included in the *Data Converter Reference Manual*.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page, or in the listing for Volume II below. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guide (and the "Orientation" that usually accompanies it) will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents (of this volume) is provided for your convenience on pages 1–5 through 1–9.

IF YOU CAN'T FIND IT HERE OR IN VOLUME II . . . ASK!

If it's not a signal conversion product, it's probably in one of the two companion volumes, the *Linear Products Reference Manual* or the *Audio/Video Products Reference Manual*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

See the Worldwide Sales Directory on pages 11–12 and 11–13 at the back of this volume for our sales office phone numbers.

Contents of Other Reference Manuals

AUDIO/VIDEO PRODUCTS

- Operational Amplifiers
- Audio A/D Converters
- Video A/D Converters
- Audio D/A Converters
- Video D/A Converters
- Special Function Audio Products
- Special Function Video Products
- Digital Signal Processing Products
- Application Notes

DATA CONVERTER PRODUCTS (VOLUME II)

- A/D Converters
- V/F & F/V Converters
- Sample/Track-Hold Amplifiers
- Switches & Multiplexers
- Voltage References
- Data Acquisition Subsystems
- Analog I/O Ports
- Application Specific ICs
- Power Supplies

LINEAR PRODUCTS

- Operational Amplifiers
- Comparators
- Instrumentation Amplifiers
- Isolation Amplifiers
- Analog Multipliers/Dividers
- Log/Antilog Amplifiers
- RMS-to-DC Converters
- Mass Storage Components
- ATE Components
- Special Function Components
- Temperature Transducers
- Signal Conditioning Components & Subsystems
- Digital Panel Instruments
- Bus Interface & Serial I/O Products
- Automotive Components
- Application Specific ICs
- Power Supplies
- Component Test Systems

1992 DATA CONVERTER REFERENCE MANUAL

VOLUME I

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ANALOG DEVICES

1992
DATA CONVERTER REFERENCE MANUAL
Volume I

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Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the *1990 Databook Series*, more than 120 significant new products have been introduced by Analog Devices; they run the gamut from brand new product categories and technologies to new standard products (with improvements in price, performance or design) to augmented second-source products. In addition, the Analog Devices line of IC products now includes the products of Precision Monolithics, Inc., which was acquired by Analog Devices in 1990. The new products are all classified and summarized in these volumes, along with existing products that are desirable for use in new designs.

Examples of the variety and innovation content of outstanding new ICs to be found in these two volumes include:

- the ADV7141/46/48 Edsun CEG/DAC™ family of monolithic RAM-DACs, designed to eliminate "jaggies" and improve color resolution in VGA displays (Vol. I)
- the AD28msp02 16-bit codec, a complete analog front end for high-performance voiceband DSP applications (Vol. I)
- the DAC-8800 and -8840 TrimDACs™, which eliminate pots and permit automatic trimming of offsets and gains in electronic circuits and systems (Vol. I)
- the AD7710/11/12 family of 21-bit sigma-delta a/d converters with complete on-chip signal conditioning (Vol. II)
- the AD9100 wideband low-distortion monolithic track-hold amplifier with 13 ns acquisition time to 0.1% (Vol. II)
- the AD1674 12-bit sampling a/d converter, a "faster, better, cheaper" upgrade for AD574/674/774 a/d converter sockets (Vol. II)
- the AD9020/9060 10-bit TTL/ECL flash a/d converters with sampling rates to 75 MSPS (Vol. II)
- the AD671 12-bit, 500 ns a/d converter (Vol. II).

Many more could have been added to this list.

CDG/DAC, TrimDAC and DSPatch are trademarks of Analog Devices, Inc.

2-VOLUME DATA CONVERTER REFERENCE MANUAL

This two-volume set provides comprehensive technical data on Analog Devices data-conversion products, which are involved in spanning the interface between analog and digital worlds. It is a companion to the *Linear Products Databook*, which provides similar data for analog-to-analog products. Both volumes contain:

- comprehensive data sheets and package information on a total of more than 350 significant product families
- orientation material and selection guides for finding products rapidly
- a representative list of available Analog Devices technical publications on real-world analog and digital signal processing
- our Worldwide Sales Directory
- the complete Product Index to all data-conversion and DSP products listed in these two volumes and all products listed in the Linear Products Databook.

Division of Product Groups between the Two Books

Volume I contains information on

Digital-to-analog converters
Synchro/resolver-to-digital converters
Communications products
Digital panel meters
Digital signal processing products
Bus interface and serial I/O products
Application specific ICs
Power supplies.

Volume II contains information on:

Analog-to-digital converters
Voltage-to-frequency and frequency-to-voltage converters
Sample/track-hold amplifiers
Switches and multiplexers
Voltage references
Data acquisition subsystems
Analog I/O ports
Application-specific ICs
Power supplies.

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are listed in the Index, and data sheets may be available separately—but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its readers up-to-date applications information on

our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 11–8 to 11–11 at the back of the book.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 11–12 and 11–13 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S. and MIL-STD-1772 for hybrids. Many of our product —both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts. The 1990 issue consists of two volumes with data on 343 product families; the 120 entries in the second of those volumes describe qualified products manufactured by our PMI Division. A newsletter, *Analog Briefings*®, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 11–4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 11–5 you will find a guide to substitutions (where possible) for products no longer available.

ICs embodying combinations of functions that you need but cannot find among our standard offerings may be available to meet your specific requirements as custom designs. Consult the section in this book on Application Specific ICs—and/or get in touch with Analog Devices.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

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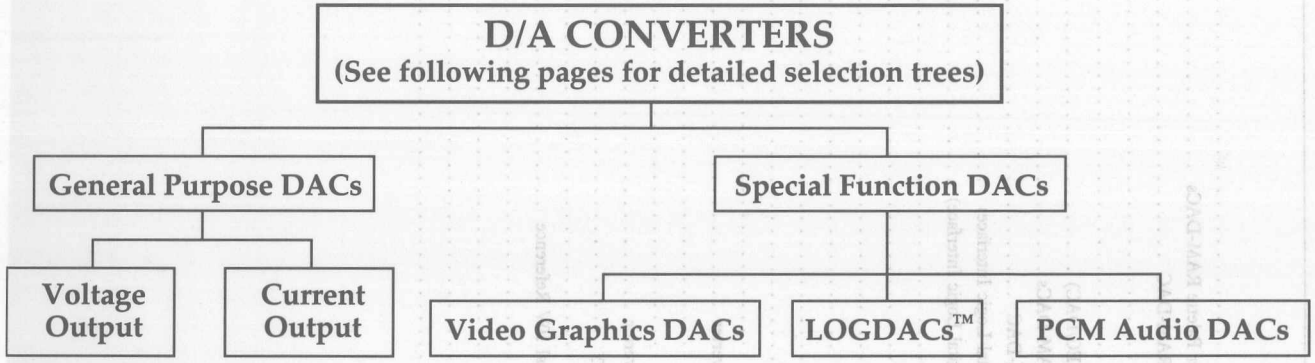
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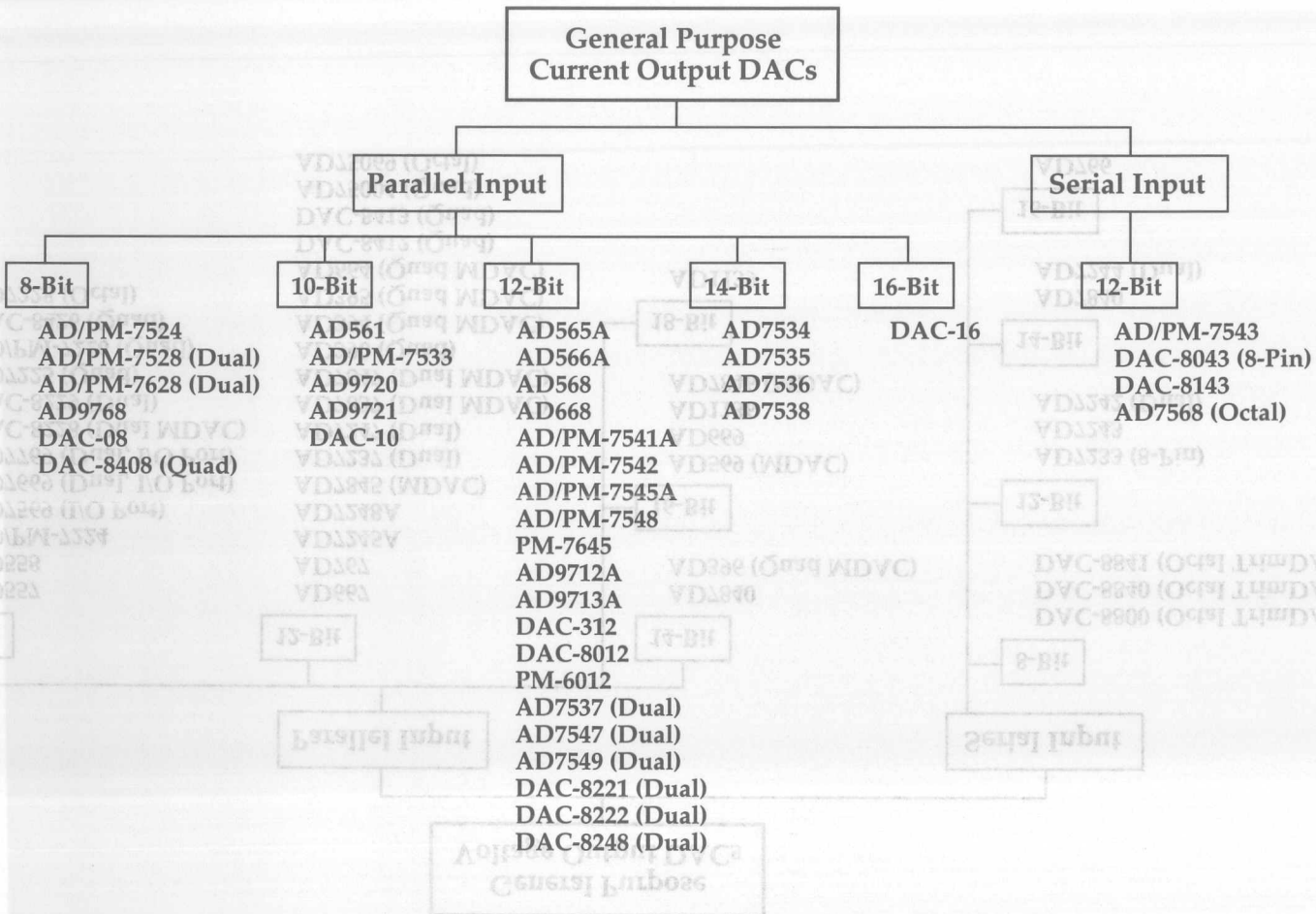
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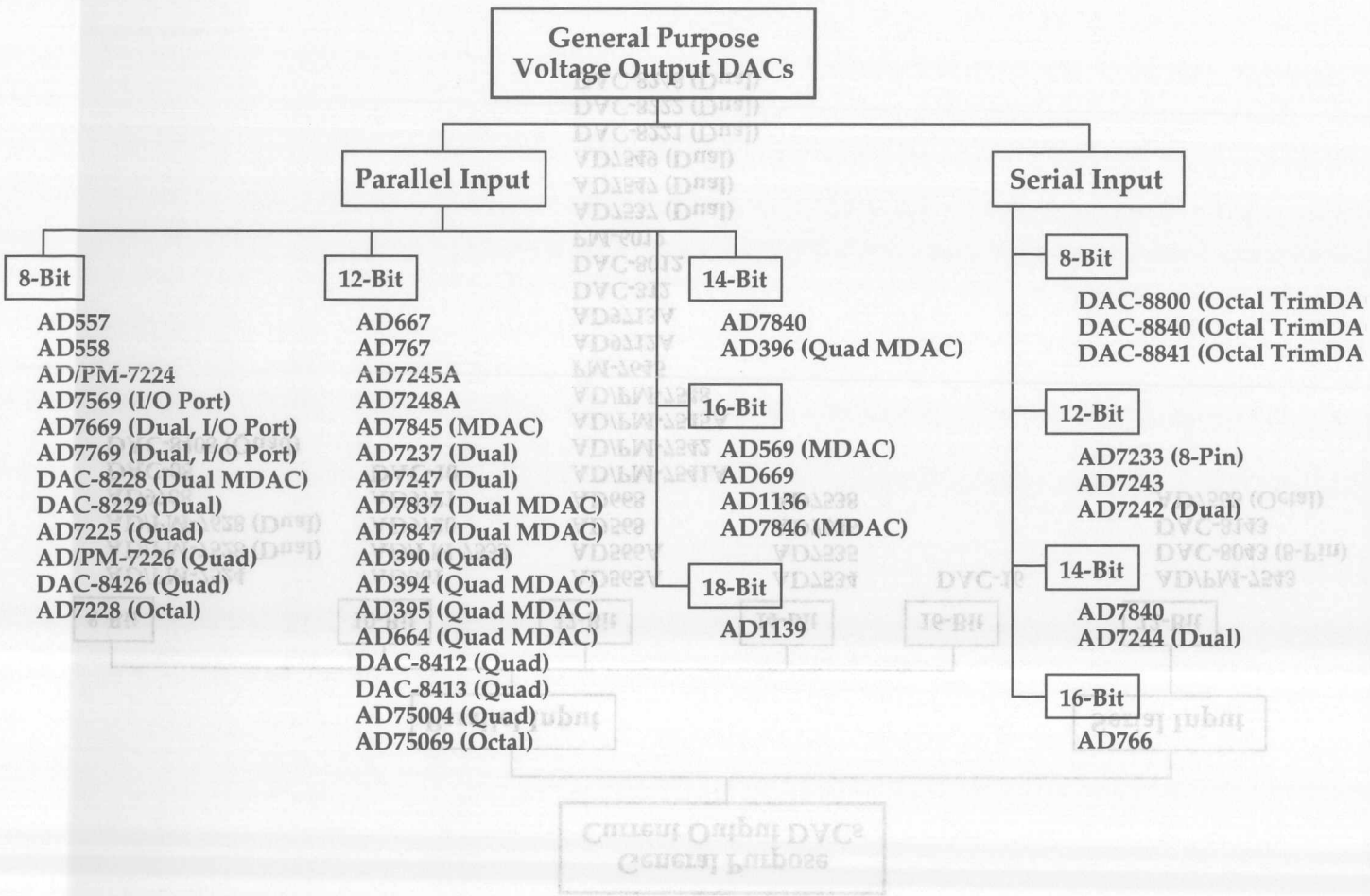
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PM-6012 – 12-Bit High Speed Multiplying D/A Converter 2–1141

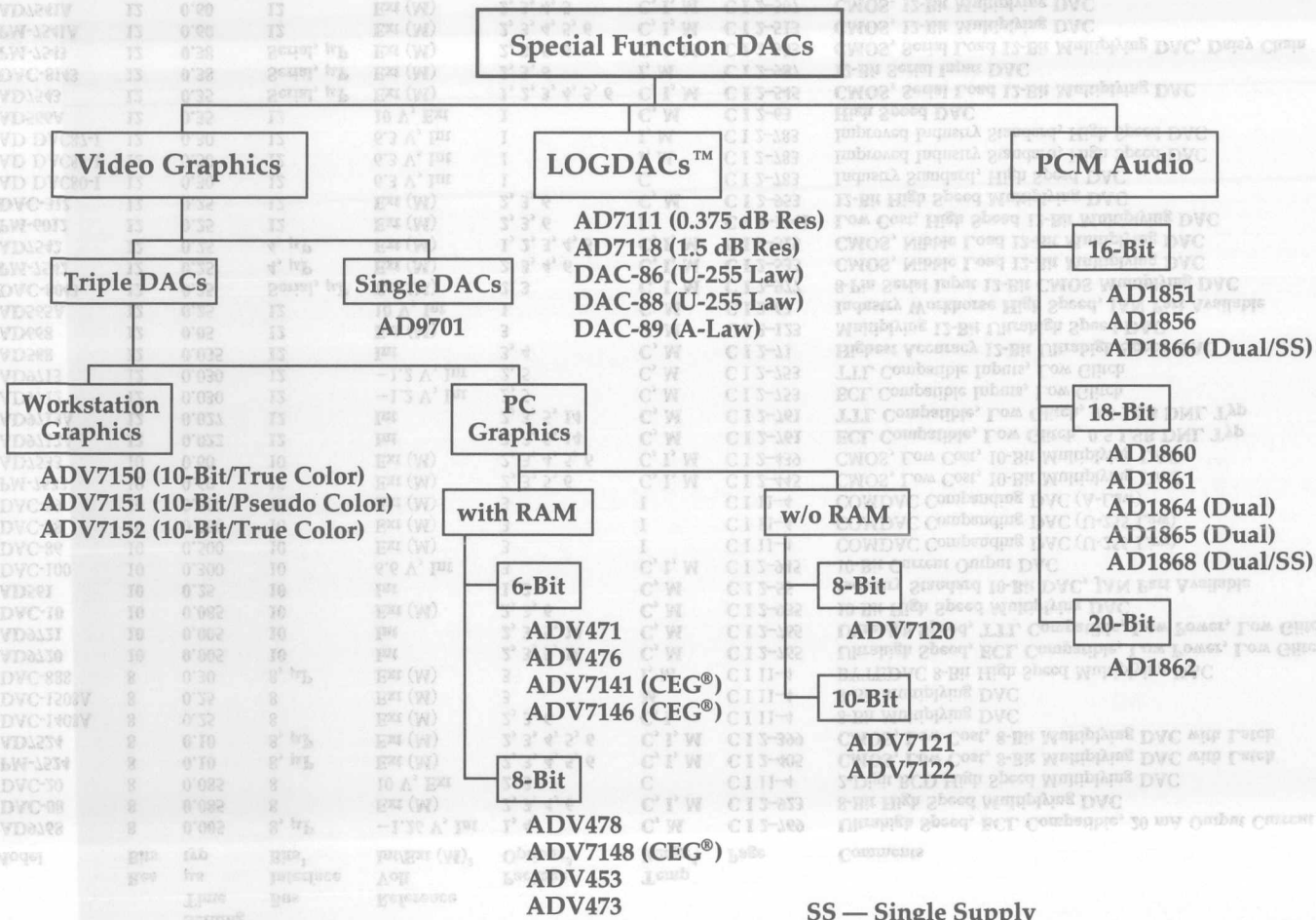
Selection Tree
D/A Converters




General Purpose
Current Output DACs
Parallel Input
Serial Input
8-Bit
10-Bit
12-Bit
14-Bit
16-Bit
12-Bit
AD/PM-7524
AD/PM-7528 (Dual)
AD/PM-7628 (Dual)
AD9768
DAC-08
DAC-8408 (Quad)
AD561
AD/PM-7533
AD9720
AD9721
DAC-10
AD565A
AD566A
AD568
AD668
AD/PM-7541A
AD/PM-7542
AD/PM-7545A
AD/PM-7548
PM-7645
AD9712A
AD9713A
DAC-312
DAC-8012
PM-6012
AD7537 (Dual)
AD7547 (Dual)
AD7549 (Dual)
DAC-8221 (Dual)
DAC-8222 (Dual)
DAC-8248 (Dual)
AD7534
AD7535
AD7536
AD7538
DAC-16
AD/PM-7543
DAC-8043 (8-Pin)
DAC-8143
AD7568 (Octal)

Selection Tree
D/A Converters





SS — Single Supply
CEG® — Continuous Edge Graphics smooths lines and increases color resolution in VGA* compatible systems.

*VGA is a trademark of International Business Machines Corp.

Selection Guide
Digital-to-Analog Converters

Single DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD9768	**8**	**0.005**	**8, µP**	**−1.26 V, Int**	**1, 4**	**C, M**	**C I 2–769**	**Ultrahigh Speed, ECL Compatible, 20 mA Output Current**
DAC-08	**8**	**0.085**	**8**	**Ext (M)**	**2, 3, 4, 6**	**C, I, M**	**C I 2–923**	**8-Bit High Speed Multiplying DAC**
DAC-20	8	0.085	8	10 V, Ext	2, 3	C	C I 11–4	2-Digit BCD High Speed Multiplying DAC
PM-7524	**8**	**0.10**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I 2–405**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
AD7524	**8**	**0.10**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I 2–399**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
DAC-1408A	8	0.25	8	Ext (M)	2, 3, 6	C, I	C I 11–4	8-Bit Multiplying DAC
DAC-1508A	8	0.25	8	Ext (M)	3	M	C I 11–4	8-Bit Multiplying DAC
DAC-888	8	0.30	8, µP	Ext (M)	3	I, M	C I 11–4	BYTEDAC 8-Bit High Speed Multiplying DAC
AD9720	**10**	**0.005**	**10**	**Int**	**2, 3, 5, 14**	**C, M**	**C I 2–765**	**Ultrahigh Speed, ECL Compatible, Low Power, Low Glitch**
AD9721	**10**	**0.005**	**10**	**Int**	**2, 3, 5, 14**	**C, M**	**C I 2–765**	**Ultrahigh Speed, TTL Compatible, Low Power, Low Glitch**
DAC-10	**10**	**0.085**	**10**	**Ext (M)**	**2, 3, 6**	**C, M**	**C I 2–935**	**10-Bit High Speed Multiplying DAC**
AD561	**10**	**0.25**	**10**	**Int**	**1, 2**	**C, M**	**C I 2–55**	**Industry Standard 10-Bit DAC, JAN Part Available**
DAC-100	10	0.300	10	6.6 V, Int	3	C, I, M	C I 2–945	10-Bit Current Output DAC
DAC-86	10	0.500	10	Ext (M)	3	I	C I 11–4	COMDAC Companding DAC (U-255 Law)
DAC-88	10	0.500	10	Ext (M)	3	I	C I 11–4	COMDAC Companding DAC (U-255 Law)
DAC-89	10	0.500	10	Ext (M)	3	I	C I 11–4	COMDAC Companding DAC (A-Law)
PM-7533	10	0.60	10	Ext (M)	2, 3, 5, 6	C, I, M	C I 2–445	CMOS, Low Cost, 10-Bit Multiplying DAC
AD7533	10	0.60	10	Ext (M)	2, 3, 4, 5, 6	C, I, M	C I 2–439	CMOS, Low Cost, 10-Bit Multiplying DAC
AD9712A	**12**	**0.022**	**12**	**Int**	**2, 3, 5, 14**	**C, M**	**C I 2–761**	**ECL Compatible, Low Glitch, 0.5 LSB DNL Typ**
AD9713A	**12**	**0.027**	**12**	**Int**	**2, 3, 5, 14**	**C, M**	**C I 2–761**	**TTL Compatible, Low Glitch, 0.5 LSB DNL Typ**
AD9712	12	0.030	12	−1.2 V, Int	2, 5	C, M	C I 2–753	ECL Compatible Inputs, Low Glitch
AD9713	12	0.030	12	−1.2 V, Int	2, 5	C, M	C I 2–753	TTL Compatible Inputs, Low Glitch
AD568	**12**	**0.035**	**12**	**Int**	**3, 4**	**C, M**	**C I 2–71**	**Highest Accuracy 12-Bit Ultrahigh Speed DAC**
AD668	**12**	**0.05**	**12**	**Ext (M)**	**3**	**C, M**	**C I 2–123**	**Multiplying 12-Bit Ultrahigh Speed DAC**
AD565A	**12**	**0.25**	**12**	**10 V, Int**	**1**	**C, M**	**C I 2–63**	**Industry Workhorse High Speed, JAN Part Available**
DAC-8043	**12**	**0.25**	**Serial, µP**	**Ext (M)**	**2, 3**	**C, I, M**	**C I 2–977**	**8-Pin Serial Input 12-Bit CMOS Multiplying DAC**
PM-7542	**12**	**0.25**	**4, µP**	**Ext (M)**	**2, 3, 4, 6**	**C, I, M**	**C I 2–533**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
AD7542	**12**	**0.25**	**4, µP**	**Ext (M)**	**1, 2, 3, 4, 5**	**C, I, M**	**C I 2–525**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
***PM-6012**	**12**	**0.25**	**12**	**Ext (M)**	**2, 3, 6**	**I**	**C I 2–1141**	**Low Cost, High Speed 12-Bit Multiplying DAC**
DAC-312	**12**	**0.25**	**12**	**Ext (M)**	**2, 3, 6**	**C, M**	**C I 2–953**	**12-Bit High Speed Multiplying DAC**
AD DAC80-I	12	0.30	12	6.3 V, Int	1	C	C I 2–783	Industry Standard, High Speed DAC
AD DAC85-I	12	0.30	12	6.3 V, Int	1	I, M	C I 2–783	Improved Industry Standard, High Speed DAC
AD DAC87-I	12	0.30	12	6.3 V, Int	1	I, M	C I 2–783	Improved Industry Standard, High Speed DAC
AD566A	**12**	**0.35**	**12**	**10 V, Ext**	**1**	**C, M**	**C I 2–63**	**High Speed DAC**
AD7543	**12**	**0.35**	**Serial, µP**	**Ext (M)**	**1, 2, 3, 4, 5, 6**	**C, I, M**	**C I 2–545**	**CMOS, Serial Load 12-Bit Multiplying DAC**
DAC-8143	**12**	**0.38**	**Serial, µP**	**Ext (M)**	**2, 3, 6**	**I, M**	**C I 2–987**	**12-Bit Serial Input DAC**
PM-7543	**12**	**0.38**	**Serial, µP**	**Ext (M)**	**2, 3, 5, 6**	**C, I, M**	**C I 2–553**	**CMOS, Serial Load 12-Bit Multiplying DAC, Daisy Chain**
PM-7541A	**12**	**0.60**	**12**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I 2–513**	**CMOS, 12-Bit Multiplying DAC**
AD7541A	**12**	**0.60**	**12**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I 2–507**	**CMOS, 12-Bit Multiplying DAC**

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
DAC-8012	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 5**	**C, I, M**	**C I 2–967**	**12-Bit CMOS DAC with Memory and Readback**
PM-7548	**12**	**1.0**	**8, µP**	**Ext (M)**	**2, 3, 5, 6**	**C, I, M**	**C I 2–613**	**CMOS, Byte Load 12-Bit DAC, Single or Dual Supply**
AD7548	**12**	**1.0**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I 2–601**	**CMOS, Byte Load 12-Bit DAC, Single or Dual Supply**
AD562	12	1.5	12	Ext	1	C, I, M	C I 2–59	Industry Standard, JAN Part Available
AD563	12	1.5	12	2.5 V, Int	1	C, M	C I 2–59	Industry Standard
AD7545A	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I 2–585**	**CMOS, Improved AD7545**
PM-7545	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I 2–573**	**CMOS, Parallel Load 12-Bit Multiplying DAC**
PM-7645	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4**	**C, I, M**	**C I 2–573**	**PM-7545 Specified for +15 V Operation**
AD7545	**12**	**2.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I 2–565**	**CMOS, Parallel Load 12-Bit Multiplying DAC**
AD7534	**14**	**1.5**	**8, µP**	**Ext (M)**	**2, 3, 5**	**C, I, M**	**C I 2–455**	**CMOS, Byte Load**
AD7535	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I 2–467**	**CMOS, Parallel or Byte Load**
AD7536	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I 2–479**	**CMOS, Parallel or Byte Load, Bipolar Output**
AD7538	**14**	**1.5**	**14, µP**	**Ext (M)**	**2, 3, 6**	**C, I, M**	**C I 2–499**	**CMOS, Parallel Load**
***AD1851**	**16**	**0.35**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–173**	**16-Bit 16 × F_S PCM Audio DAC**
AD1856	**16**	**0.35**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–183**	**16-Bit PCM Audio DAC**
***DAC-16**	**16**	**0.5**	**16**	**Ext (M)**	**1, 2**	**I, M**	**C I 2–943**	**16-Bit High Speed Multiplying DAC**
AD DAC71-I	16	1.0	16	6.3 V, Int	1, 7	C	C I 11–4	High Resolution 16-Bit DAC
AD DAC72-I	16	1.0	16	6.3 V, Int	1, 7	C, I	C I 11–4	High Resolution 16-Bit DAC
AD1860	**18**	**0.35**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–191**	**18-Bit PCM Audio DAC**
***AD1861**	**18**	**0.35**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–173**	**18-Bit 16 × F_S PCM Audio DAC**
***AD1862**	**20**	**0.35**	**Serial, µP**	**Int**	**2**	**C**	**C I 2–203**	**20-Bit Audio DAC**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parall (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given reference is pinned out.

[3]Package Options: 1-Side-Brazed Dual-In-Line Ceramic; 2-Plastic Molded Dual-In-Line; 3-Cerdip; 4-Leadless Chip Carrier; 5-Plastic Leaded Chip Carrier (PLCC); 6-Small Outline Package (SOIC); 7-Round metic Metal Can (Header); 14-J-Leaded Ceramic.

[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Digital-to-Analog Converters

Single DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD557	8	0.8	8, µP	Int	2, 5	C	C I 2–43	Lowest Cost 8-Bit DACPORT™; Single +5 V Supply
AD7569	8	1.0	8, µP	Int	2, 3, 4, 5, 6	C, I, M	C II 8–7	CMOS, Complete 8-Bit DAC/ADC/SHA/ Reference
AD558	8	3.0	8, µP	Int	1, 2, 4, 5	C, M	C I 2–47	10 V Out DACPORT, Single or Dual Supply
*PM7224	8	5.0	8, µP	2–12.5 V, Ext	2, 3, 4, 5, 6	C, I, M	C I 2–267	CMOS, Low Cost 8-Bit DAC
AD7224	8	5.0 (max)	8, µP	2–12.5 V, Ext	2, 3, 4, 5, 6	C, I, M	C I 2–259	CMOS, Low Cost 8-Bit DAC
DAC-06	10	1.5	10	6.7 V, Int	1	C, M	C I 11–4	Twos Complement Input Coding
DAC-210	10	1.5	10	7.6 V, Int	1	C, I	C I 11–4	Sign-Magnitude/Internal Reference
DAC-05	10	2.0	10	6.7 V, Int	1	C, M	C I 11–4	Sign-Magnitude for Unipolar Output
DAC-02	10	2.0	10	6.7 V, Int	1	C, M	C I 11–4	Sign-Magnitude/Bipolar Output
AD7848	12	2.5	12, µP	Int (+3 V), Ext	2, 3, 5	C, I	C I 2–735	CMOS, Complete 12-Bit DAC with 8-Word FIFO
AD7845	12	2.5	12, µP	Ext (M)	2, 3, 4, 5, 6	C, I, M	C I 2–709	CMOS, 12-Bit Multiplying DAC with Output Amplifier
AD DAC80-V	12	3.0	12	6.3 V, Int	1	C	C I 2–783	Improved Industry Standard
AD DAC85-V	12	3.0	12	6.3 V, Int	1	I, M	C I 2–783	Improved Industry Standard
AD DAC87-V	12	3.0	12	6.3 V, Int	1	I, M	C I 2–783	Improved Industry Standard
AD667	12	3.0	4/8/12, µP	10 V, Int	1, 2, 4, 5	C, I, M	C I 2–115	Highest Accuracy Complete 12-Bit DAC
AD767	12	3.0	12, µP	10 V, Int	1, 2	C, I, M	C I 2–159	Fastest Interface Complete 12-Bit DAC
AD7233	12	10 (max)	Serial, µP	Int	2	I	C I 2–339	Smallest 12-Bit Serial DACPORT (8-Pin) Bipolar ±5 V Output Range
*AD7243	12	10 (max)	Serial	Int (+5 V), Ext	2, 3, 6	I, M	C I 2–371	Low Cost 12-Bit Serial DACPORT in 16-Pin Package
AD7245A	12	10 (max)	12, µP	5 V, Int	2, 3, 4, 5, 6	C, I, M	C I 2–385	Faster Interface, 12 V and 15 V AD7245
AD7248A	12	10 (max)	8, µP	5 V, Int	2, 3, 5, 6	C, I, M	C I 2–385	Faster Interface, 12 V and 15 V AD7248
AD7245	12	10 (max)	12, µP	5 V, Int	2, 3, 4, 5	C, I, M	C I 2–383	CMOS, 12-Bit Complete DAC, Parallel Load
AD7248	12	10 (max)	8, µP	5 V, Int	2, 3, 4, 5	C, I, M	C I 2–383	CMOS, 12-Bit Complete DAC, Byte Load
AD7840	14	2.0	14/Serial, µP	Int (+3 V), Ext	2, 3, 5	C, I, M	C I 2–693	CMOS, 14-Bit Complete DAC, Parallel or Serial Load
*AD766	16	1.5	Serial, µP	Int	1, 2	C, I, M	C I 2–151	Zero-Chip Interface 16-Bit DSP DACPORT
*AD1851	16	1.5	Serial µP	Int	2, 6	C	C I 2–173	16-Bit, 16 × F_S PCM Audio DAC
AD1856	16	1.5	Serial, µP	Int	2, 6	C	C I 2–183	16-Bit PCM Audio DAC
AD569	16	3.0	8/16, µP	±5 V, Ext (M)	1, 2	I, M	C I 2–83	Monolithic, 16-Bit Monotonic DAC
AD DAC71-V	16	5.0	16	6.3 V, Int	1, 7	C	C I 11–4	High Resolution 16-Bit DAC
AD DAC72-V	16	5.0	16	6.3 V, Int	1, 7	C, I	C I 11–4	High Resolution 16-Bit DAC
AD7846	16	6	16, µP	Ext (M)	1, 2, 4, 5	C, I, M	C I 2–721	CMOS, 16-Bit Multiplying DAC with Readback Capability
*AD669	16	8	16, µP	10 V, Int	2, 3, 6	I, M	C I 2–139	Monolithic, Complete 16-Bit DAC
DAC1136	16	8	16	6 V, Int	Module	C	C I 11–4	High Resolution and Accuracy
AD1147	16	20	16, µP	10 V, Int	2	I	C I 11–4	Internal 8-Bit Latched Input DACs for Offset and Gain Adjust
AD1148	16	20	16, µP	10 V, Int	2	I	C I 11–4	Separate 8-Bit Bus for Internal Offset and Gain Adjust DACs

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD1860	**18**	**1.5**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–191**	**18-Bit PCM Audio DAC**
***AD1861**	**18**	**1.5**	**Serial, µP**	**Int**	**2, 6**	**C**	**C I 2–173**	**18-Bit, 16 × F_S PCM Audio DAC**
DAC1138	18	10	18	6 V, Int	Module	C	C I 11–4	High Resolution and Accuracy
AD1139	**18**	**40**	**18, µP**	**–10 V, Int**	**1**	**C**	**C I 2–167**	**True 18-Bit Accuracy**

Video Graphics DACs

Model	Res Bits	Rate Update Rate MHz min	Palette Size	Reference	Package Options[3]	Temp Range[4]	Page	Comments
ADV476	**6**	**66, 50, 35**	**256**	**I**	**2, 5**	**C**	**C I 2–817**	**CMOS, Triple 6-Bit Color Palette RAM-DAC**
***ADV7146**	**6/8**	**66, 50, 35**	**256**	**I**	**2, 5**	**C**	**C I 2–869**	**Pin Compatible to ADV476, INMOS 171/176 with CEG**
ADV471	**6**	**80, 66, 50, 35**	**256**	**V/I**	**5**	**C**	**C I 2–839**	**CMOS, Triple 6-Bit Color Palette RAM-DAC**
***ADV7141**	**6/8**	**80, 66, 50, 35**	**256**	**V/I**	**2, 5**	**C**	**C I 2–869**	**Pin Compatible to ADV471 with CEG**
***ADV477/ADV475**	**6/8**	**80, 66, 50, 35**	**256**	**V (Int.)**	**2, 5**	**C**	**C I 2–827**	**Low Power, Power Down RAM-DAC**
ADV476	**6**	**80, 66, 50, 35**	**256**	**V (Int.)**	**2, 5**	**C**	**C I 2–817**	**Low Power, Power Down RAM-DAC**
ADV478	**6/8**	**80, 66, 50, 35**	**256**	**V/I**	**5**	**C**	**C I 2–839**	**CMOS, Triple 8-Bit Color Palette RAM-DAC**
***ADV7148**	**6/8**	**80, 66, 50, 35**	**256**	**V/I**	**2, 5**	**C**	**C I 2–869**	**Pin Compatible to ADV478 with CEG**
ADV453	**8**	**66, 40**	**256**	**V**	**2, 5**	**C**	**C I 2–799**	**CMOS, Triple 8-Bit Color Palette RAM-DAC**
***ADV473**	**8**	**100, 80, 66, 50, 35**	**256**	**V/I (Int.)**	**5**	**C**	**C I 2–805**	**True-Color Video RAM-DAC (Triple 8-Bit)**
***ADV101**	**8**	**80, 50, 30**	**—**	**V**	**2, 5**	**C**	**C I 2–793**	**CMOS, Triple 8-Bit Video DAC**
ADV7120	**8**	**80, 50, 30**	**—**	**V**	**2, 5**	**C**	**C I 2–851**	**CMOS, Triple 8-Bit Video DAC**
AD9701	**8**	**225**	**—**	**—**	**1, 3, 4**	**I, M**	**C I 2–747**	**Single 8-Bit Video DAC**
ADV7121	**10**	**80, 50, 30**	**—**	**V**	**2, 5**	**C**	**C I 2–857**	**CMOS, Triple 10-Bit Video DAC**
ADV7122	**10**	**80, 50, 30**	**—**	**V**	**2, 5**	**C**	**C I 2–857**	**CMOS, Triple 10-Bit Video DAC**
***ADV7150**	**10**	**170, 135, 110, 85**	**256**	**V**	**10**	**C**	**C I 2–889**	**High Speed, True-Color Video RAM-DAC, (Triple 10-Bit) 4 × 1 Multiplexing**
***ADV7151**	**10**	**170, 135, 110, 85**	**256**	**V**	**10**	**C**	**C I 2–907**	**High Speed, Pseudo-Color Video RAM-DAC, (Triple 10-Bit)**
***ADV7152**	**10**	**170, 135, 110, 85**	**256**	**V**	**10**	**C**	**C I 2–889**	**High Speed, Pseudo-Color Video RAM-DAC, (Triple 10-Bit) 2 × 1 Multiplexing**

[1]This column lists the data format for the bus with "P" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]Package Options: 1-Side-Brazed Dual-In-Line Ceramic; 2-Plastic Molded Dual-In-Line; 3-Cerdip; 4-Leadless Chip Carrier; 5-Plastic Leaded Chip Carrier (PLCC); 6-Small Outline Package (SOIC); 7-Round Hermetic Metal Can (Header); 10-Plastic Quad Flatpack.

[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

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Digital-to-Analog Converters

Multiple DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page	Comments
AD7669	8	1.0	8, µP	Int	2	2, 5, 6	C, I, M	C II 8–7	CMOS, Complete 8-Bit Dual DAC/ADC/SHA/Reference
DAC-8228	8	2.0	8, µP	Ext (M)	2	2, 3, 6	I, M	C I 2–1029	CMOS, PM-7528 Pinout with Voltage Output
DAC-8229	8	2.0	8, µP	Ext (M)	2	2, 3, 6	I, M	C I 2–1041	CMOS, Single or Dual Supply Operation
AD7769	8	2.5	8, µP	Ext	2	2, 5	C, I	C II 8–27	CMOS, Complete 8-Bit Dual DAC/ 2-Channel ADC
DAC-8426	8	3.0	8, µP	10 V, Int	4	2, 3, 6	I, M	C I 2–1095	CMOS, Complete with 10 V Reference, Improved Timing
PM-7226A	8	3.0	8, µP	Ext (M)	4	2, 3, 6	I, M	C I 2–303	CMOS, Improved Timing, Specified for +5 V to +15 V Operation
AD7226	8	3.0	8, µP	2–12.5 V, Ext	8	2, 3, 4, 5, 6	C, I, M	C I 2–291	CMOS, No User Trims, Specified with Single or Dual Supplies
AD7225	8	5.0 (max)	8, µP	2–12.5 V, Ext	4	2, 3, 4, 5, 6	C, I, M	C I 2–279	CMOS, Separate References for Each DAC
DAC-8800	8	0.8	8, Serial	DC, Ext	8	2, 3, 6	C, I, M	C I 2–1107	Octal 8-Bit CMOS DAC (TrimDAC™)
DAC-8840	8	3.5	Serial	Ext (M)	8	2, 3, 6	I, M	C I 2–1121	CMOS, Four-Quadrant Multiplying with Op Amps
*DAC-8841	8	3.5	Serial	Ext (M)	8	2, 3, 6	I, M	C I 2–1131	Octal 8-Bit, Two Quadrant, Multiplying TrimDAC, +5 V Operation
AD7228	8	5.0 (max)	8, µP	2–10 V, Ext	8	2, 3, 4, 5, 6	C, I, M	C I 2–323	CMOS, Specified for Single or Dual Supply, Skinny 20-Pin DIP
*AD7228A	8	5.0 (max)	8, µP	2–10 V, Ext	8	2, 3, 5, 6	C, I, M	C I 2–331	CMOS, Specified for Single or Dual Supply, Skinny 20-Pin DIP
AD75004	12	2	12, µP	5 V, Int	4	2, 5	C	C I 2–773, C I 8–1	Fastest Quad 12-Bit Voltage Output DAC
*AD7242	12	2	Serial, µP	3 V, Int	2	2, 3, 6	C, I	C I 2–359	Complete ±5 V 12-Bit Dual DAC
AD392	12	4	12, µP	Int	4	8	C	C I 11–4	Fast Bus Access Time (<40 ns), Data Readback Capability
AD390	12	4	12, µP	10 V, Int	4	1	C, M	C I 2–23	Double Buffered, Simultaneous Update
*AD7837	12	5	8, µP	Ext (M)	2	2, 3, 6	C, I, M	C I 2–681	CMOS, MDAC, Byte Load, Double Buffered
*AD7847	12	5	12, µP	Ext (M)	2	2, 3, 6	C, I, M	C I 2–681	CMOS MDAC, Parallel Load
DAC-8412	12	6	12, µP	Ext	4	1, 2, 4, 5	I, M	C I 2–1083	Readback, Reset to Midscale, Low Power Quad DAC, +5 V to ±15 V Operation
*DAC-8413	12	6	12, µP	Ext	4	1, 2, 4, 5	I, M	C I 2–1083	Equivalent to DAC-8412 with Reset to Zero Scale

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page	Comments
***AD75069**	**12**	**8**	**12, µP**	**5 V, Int**	**8**	**5**	**C, I**	**C I 2–777**	**Monolithic Octal 12-Bit Voltage Output DAC**
AD7237	**12**	**10 (max)**	**8, µP**	**Int (+5 V), Ext**	**2**	**2, 3, 6**	**C, I, M**	**C I 2–347**	**CMOS, Complete 12-Bit Dual DAC, Byte Load**
AD7247	**12**	**10 (max)**	**12, µP**	**Int (+5 V), Ext**	**2**	**2, 3, 6**	**C, I, M**	**C I 2–347**	**CMOS, Complete 12-Bit Dual DAC, Parallel Load**
AD664	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1, 2, 4, 5**	**C, I, M**	**C I 2–95**	**Readback, Reset, Low Power Quad DAC**
AD394	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1**	**C, M**	**C I 2–31**	**Four Independent Reference Inputs, Bipolar Outputs**
AD395	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1**	**C, M**	**C I 2–31**	**Four Independent Reference Inputs, Unipolar Outputs**
***AD7244**	**14**	**2**	**Serial, µP**	**+3 V, Int**	**2**	**2, 3, 6**	**C, I, M**	**C I 2–359**	**Complete ±5 V 14-Bit Dual DAC**
AD396	14	10	8, µP	Ext (M)	4	1	C, M	C I 2–39	Four Independent Reference Inputs, Bipolar Output, Simultaneous Update
***AD1866**	**16**		**Serial**	**Int**	**2**	**2, 6**	**I**	**C I 2–235**	**Dual 16-Bit Audio DAC, +5 V Single Supply**
***AD1864**	**18**	**1.5**	**Serial, µP**	**Int**	**2**	**2, 5**	**C**	**C I 2–213**	**Dual 18-Bit Audio DAC**
***AD1865**	**18**	**1.5**	**Serial, µP**	**Int**	**2**	**2**	**C**	**C I 2–225**	**Dual 18-Bit, 16 × F_S PCM Audio DAC**
***AD1868**	**18**	**1.5**	**Serial, µP**	**Int**	**2**	**2, 6**	**C**	**C I 2–237**	**Dual 18-Bit Audio DAC, +5 V Single Supply**

[1]This column lists the data format for the bus with "P" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]Package Options: 1-Side-Brazed Dual-In-Line Ceramic; 2-Plastic Molded Dual-In-Line; 3-Cerdip; 4-Leadless Chip Carrier; 5-Plastic Leaded Chip Carrier (PLCC); 6-Small Outline Package (SOIC); 8-Metal Hermetic Dual-In-Line.

[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

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Digital-to-Analog Converters

Multiple DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page	Comments
PM7528	8	0.18	8, µP	Ext (M)	2	2, 3, 4, 5, 6	C, I, M	C I 2–423	CMOS, Single Supply Operation, TTL Compatible at V_{DD} = +5 V
AD7528	8	0.18	8, µP	Ext (M)	2	2, 3, 4, 5, 6	C, I, M	C I 2–415	CMOS, +5 V to +15 V Operation, TTL Compatible at V_{DD} = +5 V
DAC-8408	8	0.19	8, µP	Ext (M)	4	2, 3, 5, 6	C, I, M	C I 2–1069	CMOS, Data Readback Memory Function, Separate V_{REF}
PM-7628	8	0.20	8, µP	Ext (M)	2	2, 3, 4, 5, 6	I, M	C I 2–665	CMOS, +5 V or +15 V Operation, Improved Timing
AD7628	8	0.35	8, µP	Ext (M)	2	2, 3, 4, 5, 6	C, I, M	C I 2–657	CMOS, +12 V to +15 V Operation, TTL Compatible at V_{DD} = 12 V to 15 V
DAC-8221	12	0.45	12, µP	Ext (M)	2	2, 3, 4, 6	C, I, M	C I 2–1001	CMOS, Buffered Inputs, +5 V Operation
*AD7564	12	0.2	Serial, µP	Ext (M)	4	6	I	C I 2–637	Single +5 V Supply, Separate References, 28-Pin SOIC Package
*AD7568	12	0.2	Serial, µP	Ext (M)	8	10	I	C I 2–645	Single +5 V Supply, Separate References, 44-Pin PQFP
DAC-8212	12	1.0	12	Ext (M)	2	2, 3, 5	C, I, M	C I 11–4	CMOS, +5 V or +15 V Single Supply Operation
DAC-8222	12	1.0	12, µP	Ext (M)	2	2, 3, 4, 6	C, I, M	C I 2–1015	CMOS, Double Buffered Inputs, Parallel Load
DAC-8248	12	1.0	8, µP	Ext (M)	2	2, 3, 6	C, I, M	C I 2–1053	CMOS, Double Buffered Inputs, Byte Load
AD7537	12	1.5 (max)	8, µP	Ext (M)	2	2, 3, 4, 5	C, I, M	C I 2–491	CMOS, Byte Load, Double Buffered
AD7547	12	1.5 (max)	12, µP	Ext (M)	2	2, 3, 4, 5, 6	C, I, M	C I 2–593	CMOS, Parallel Load
AD7549	12	1.5 (max)	4, µP	Ext (M)	2	2, 3, 4, 5	C, I, M	C I 2–629	CMOS, Nibble Load, Double Buffered
*AD1864	18		Serial, µP	Int	2	2, 5	C	C I 2–213	Dual 18-Bit Audio DAC
*AD1865	18		Serial, µP	Int	2	2	C	C I 2–225	Dual 18-Bit, 16 × F_S PCM Audio DAC

LOGDAC™

Model	Res dB	Full-Scale Range dB	Accuracy dB	Package Options[3]	Temp Range[4]	Page	Comments
AD7111	**0.375**	**88.5**	**0.17**	**2, 3, 4, 6**	**C, I, M**	**C I 2–247**	**Low Distortion**
AD7118	1.5	88.5	0.35	2, 3, 4, 5, 6	C, I, M	C I 2–253	CMOS

[1]This column lists the data format for the bus with "μP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, μP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]Package Options: 2-Plastic Molded Dual-In-Line; 3-Cerdip; 4-Leadless Chip Carrier; 5-Plastic Leaded Chip Carrier (PLCC); 6-Small Outline Package (SOIC); 10-Plastic Quad Flatpack.
[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the most recent Databooks.
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Orientation
Digital-to-Analog Converters

INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary-weighted precision resistors, a set of electronic switches, and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are resolution, accuracy, and speed. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements, and power consumption.

In this catalog there are listed some 136 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be several times that number among which to choose. The reason for so many different types is the number of degrees of freedom in selection – technological, functional, performance and package. Complete information on converters may be found in the 700-page book, *Analog-Digital Conversion Handbook*, published by Prentice-Hall, Inc.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer registers (single- or dual-rank), configuration conditioning and even high-voltage isolation.

Basic DAC

This form which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed, for example, the 10ns HDM-1210. Basic current-output DACs, such as the AD565A, are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion. Some popular CMOS IC devices, such as the AD7543 and the AD7524, are quite simple (and correspondingly low in cost), but they usually require a buffering op amp.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7111 LOGDAC, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 0.375dB per bit; thus its gain at the input code 1000 0000 (binary 128) is −48dB (48 × 0.375), and the analog output swing for 10V p-p input is

$$0.04 \text{ p-p}V_{IN} \text{ to } \exp -\left(\frac{0.375N}{20}\right).$$

Similarly, companding DACs such as the DAC-86, DAC-88, and DAC-89 have a well-defined, nonlinear transfer function.

They are constructed such that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which increases the analog signal range. The effect of this is to compress more data into the more significant bits (see *Definitions-Companding DACS*).

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data may be a "gain" (multiplying DAC), a current and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is often provided by the DAC itself (whether monolithic, modular or hybrid), but many permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed and cost.

Many DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0 – 5V full-scale or 0 – 10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset resistor is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In order to avoid difficulties, the user must pay special attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the AD565A). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable and bipolar (e.g., AD7533, AD7541, AD7541A, etc.). The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data

There are a number of ways in which converters differ in regard to the input data: first, the *coding* must be appropriate (binary, offset-binary, twos complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range with sufficient accuracy. Analog Devices offers DACs with resolutions of 8, 10, 12, 14, 16, 18 and 20 bits. The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?)—misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the AD558 and AD7226 have a set of TTL buffers; the AD667 and AD7224 have two ranks of buffering).

Controls

If the DAC has external digital controls—for example, register strobes—their drive levels, digital sense (true or false), loading and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle or chip-select decoding, should be understood, and the appropriate ways of disabling them when not needed should be employed.

Many DACs are specifically designed to interface directly to the bus of the computer or microprocessor. These DACs provide the necessary control and handshake lines, as well as the data bit buffers, to minimize and often to eliminate the interface circuitry required. The bus timing should be studied with respect to the timing provided by the DAC interface, especially as the processor performs a data-write cycle to the DAC. Systems with higher speed clocks require either shorter DAC strobe times (such as the AD767) or the use of processor-wait states when the DAC is addressed. DACs for video applications, such as the AD9701, provide special control lines unique to CRT applications (e.g., blanking, sync and reference level display).

STATIC AND DYNAMIC PERFORMANCE SPECIFICATIONS

All DACs are specified using terms such as accuracy, linearity, offset, defined and explained below. These static, or "dc," parameters are necessary and sufficient for many applications; they may not be sufficient for others, such as those in digital signal processing, adaptive filtering, or waveform generation. Dynamic, ac specifications define how the DAC performs using parameters such as signal-to-noise ratio (SNR), intermodulation distortion (IMD) and total harmonic distortion (THD). These specifications characterize the performance of the DAC output in applications where the envelope of output changes and output timing errors are critical.

POWER SUPPLIES

Appropriate power supplies should be made available considering the logic levels and analog output signals to be employed into the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals while ensuring that a connection between the grounds can always exist at one point, even if this point is inadvertently unplugged from the system.

Specialty DACs and Features

Many DACs contain a single- or dual-rank of data buffers so data can be loaded into the DAC at any time, while minimizing undesired DAC output glitches. Additionally, DACs such as the AD7848 contain an integral FIFO (first-in, first-out) memory so that multiple digital values can be loaded as a single group from the processor bus. These preloaded values can then be clocked (at specific time intervals, if needed) into the DAC output, without intervention by the processor.

Video RAM-DACs

DACs (such as the ADV7XX series) for some industry-standard video displays contain large amounts of internal RAM. This RAM is organized for use as a color palette to store desired display color values, which are then called out as needed by the pixel data. These ICs usually contain triple DACs and RAM palettes, to support full-color operation with red, green, and blue outputs. While the output is normally linear, these DACs can also contain gamma-correction circuitry which carefully distorts the output to correct for nonlinearities in the output intensity of the CRT phosphors.

TrimDACs™

These DACs, such as the DAC-8800, are designed to replace manual trim potentiometers in circuitry. They combine a simple digital interface and an output structure to allow them to function as a variable resistor. They can be used for both static (dc) adjustment as well as multiplying applications where ac signal amplitude and phase are adjusted.

Audio DACs

These DACs are optimized for transforming data representing digitized audio signals (such as from compact disks, CDs) into conventional analog signals. They contain a serial bit interface, DAC core, and appropriate output amplifier, as well as nearly all auxiliary circuitry. They are available in 16-, 18-, and 20-bit versions.

Sigma-Delta DACs

These DACs use an architecture quite different from the DACs already discussed. In a sigma-delta DAC (sometimes called a "one-bit DAC"), a serial stream of digital bits representing the desired output value is fed to the DAC. The DAC (an anti-imaging filter) digitally filters this input stream, then feeds filtered output bits to a modulator circuit which develops the average value of the bits. A low-pass analog filter eliminates residual errors and glitches.

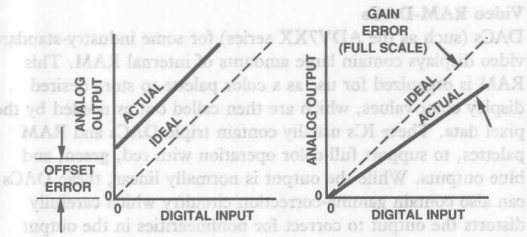
SPECIFICATIONS AND TERMS

Definitions of the performance specifications and related information are provided on the next few pages in alphabetical order.

Accuracy, Absolute

Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors and noise (*see figure*). Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "1/2LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.



Gain and Offset Error Defined

Accuracy, Relative
Relative accuracy error, expressed in %, ppm or fractions of 1LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range) after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

AC Feedthrough
The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

BCD
The abbreviation BCD stands for binary-coded decimal. It is a binary code used to represent decimal numbers in which the digits 0 through 9 are coded, using the 4-bit binary 8-4-2-1 code.

Binary
A positive-weighted code in which a number is represented by:

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + \ldots + a_n 2^n$$

where each coefficient "a_i" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots + a_n 2^{-n}$$

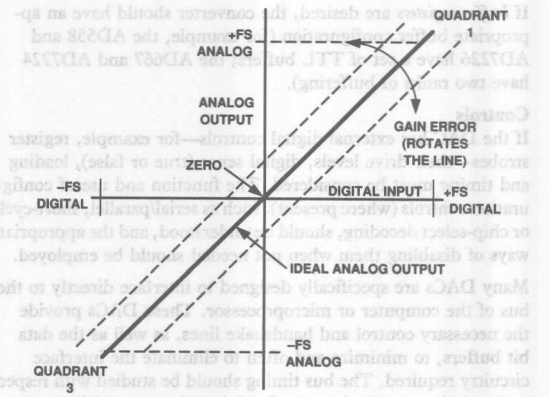
and N has a fractional value between zero and one.

Bit
The unit of binary information. It can have the value of zero or one.

Bipolar Output
When the analog signal range includes both positive and negative values, the output is said to be bipolar. The transfer characteristic of an ideal 2-quadrant bipolar-output DAC is shown in the following figure.

Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

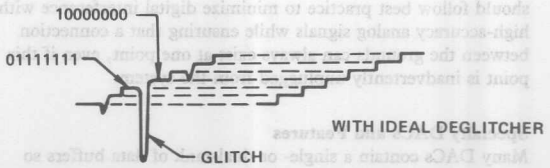
Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.



Bipolar Output Converter

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what are known as major and minor transitions. The most major transition is at half-scale when the DAC switches around the MSB and all switches change state, i.e., 0111 1111 to 1000 0000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that for a short time the D/A will give a zero (or full-scale) output and will then return to the required 1LSB above the previous reading. Such large transient spikes, which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches," hence, a deglitcher is a device that removes these glitches or reduces them to a set of small, uniform pulses. The deglitcher normally consists of a fast sample-hold circuit which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time skew between 0-1 and 1-0 transitions.



Digital Crosstalk (Q)
Digital crosstalk is a parameter that is used with multiple converters in a single package. It is the glitch impulse transferred from one converter that is being addressed to another converter that is not being addressed. It is specified in nV-secs and is measured with V_{REF} = 0V.

Digital Feedthrough (FT)
Digital feedthrough is the glitch-energy impulse transferred from the DAC's digital input to the analog output. It is specified in nV-secs and is measured with V_{REF} = 0V.

Dynamic Range (DR)
The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For linear DACs, this ratio is 2^n, where n = number of bits of resolution.

DR (in dB) = 20 $Log_{10}2^n \simeq$ 6n for linear DACs; (COMDACs® are 66 or 72dB).

Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1LSB or fractions of 1 volt with a given set of inputs at a specified frequency (see *AC Feedthrough, Digital Feedthrough*.

Four-Quadrant
In a multiplying DAC, "four-quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign (see *Multiplying DAC*).

Full-Scale (FS)
The full-scale output of a DAC is its maximum voltage or current. For a binary DAC, the full-scale output occurs when the digital inputs are all ones. The full-scale value is one LSB less than the reference value.

Full-Scale Gain Error (G_{FSE}) See Gain Error.

Full-Scale Range (FSR)
The difference between the maximum analog output and the minimum analog output of a DAC.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero*.

Gain Drift (TCG_{FS})
The variation of the full-scale value (voltage or current) measured over the operating temperature range is called gain drift. This parameter has units of %FS, ppmFS, or LSB. It may also be expressed % of FS/°C, ppm FS/°C, etc.

Gain Error (G_{FSE})
The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value (see prior figure). It is the deviation in slope of the DAC transfer characteristic from ideal.

Glitch
A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V × ns) or current (mA × ns) and time duration or charge transferred (in picocoulombs) (see *Deglitcher*).

Harmonic Distortion (and Total Harmonic Distortion)
The DAC is driven by the digitized representation of a sine wave. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second through fifth:

$$THD = 20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4 and V_5 are the rms amplitudes of the individual harmonics.

Integral Nonlinearity (INL) or Nonlinearity (NL)
This is the single most important DAC specification. For DACs, a specification of ± 1/2 LSB INL guarantees monotonicity and ± 1 LSB maximum differential nonlinearity (see *Linearity*).

Intermodulation Distortion
The DAC is driven by the digitized representation of two combined sine waves of frequencies f_a and f_b. As with any imperfectly linear device, distortion products (of order m + n) are produced at sum and difference frequencies of $mf_a \pm nf_b$ where m, n = 0, 1, 2, 3, ... Intermodulation terms are those for which m or n is not equal to zero. The second order terms include $(f_a + f_b)$ and $(f_a - f_b)$ and the third order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. IMD is defined as:

$$IMD = 20 \log \frac{\text{(rms sum of the sum and difference distortion products)}}{\text{rms amplitude of the fundamental}}$$

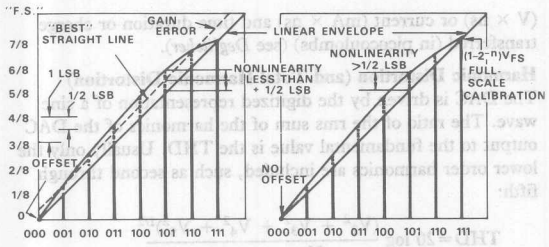
Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale is 2^{-n} where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

$$\text{LSB (Analog Value)} = \frac{FSR}{2^n}$$

where FSR = Full-Scale Range
n = number of bits

Linearity
Linearity error of a converter (also *integral nonlinearity*, see *Linearity, Differential*), expressed in %, ppm of full-scale range or (sub)multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the endpoints of the transfer characteristic after they have been calibrated (sometimes referred to as "endpoint" linearity). Endpoint linearity error is similar to *relative accuracy* error.

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a. 1/2LSB Nonlinearity Achieved by Arbitrary Location of "Best Straight Line."

b. Nonlinearity Reference Is Straight Line Through End-Points. Nonlinearity > 1/2LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points Is Easier to Measure, Gives More Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential

Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity* expressed in (sub)multiples of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to nonmonotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic

A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)

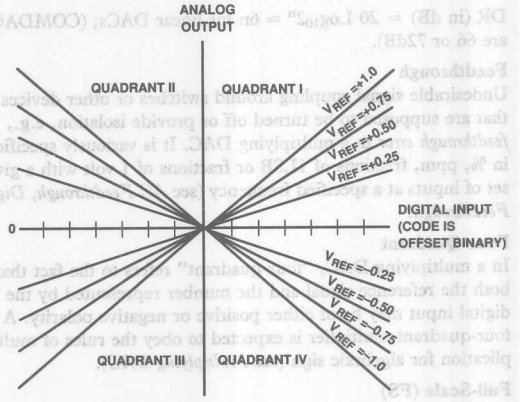
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB with a weight of 2^{n-1}, or 8LSBs. Its analog weight, relative to a DAC's full-scale span, is 1/2. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

$$\text{MSB (Analog Value)} = \frac{\text{FSR}}{2}$$

Multiplying DAC

A multiplying DAC differs from a fixed-reference DAC in its being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *Four-Quadrant*).

Some DACs can multiply only positive digital words by a positive reference. This is known as single quadrant operation (Quadrant I, see Figure). Two quadrant operation (Quadrants I and III) can be performed by a DAC that usually operates in Quadrant I by configuring the output for bipolar output operation. This is accomplished by offsetting the output by a negative MSB (1/2 of FSR), so that the MSB becomes the sign bit. DACs provide four quadrant operation by allowing the use of both positive and negative references (Quadrants I, II, III, IV).



DAC Transfer Curves

Noise, Peak and RMS

Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7111). Random noise is characterized by rms specifications for a given bandwidth or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7× the rms value is less than 0.1%.

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough and by glitch generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing and deglitching.

Offset

For almost all bipolar converters (e.g., ± 10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference because the 1/2 scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Offset Drift (TCV_{OS}, TCI_{OS})
The variation of the output offset (voltage or current) measured over the operating temperature range. The offset drift is divided by the temperature range over which it is measured and expressed in ppm per degree centigrade or percent of full-scale range. This parameter applies to DACs operating in the bipolar output mode. See zero-scale drift for DACs operating in the unipolar output mode.

Offset Error (V_{OSE}, I_{OSE})
The offset error is the error at analog zero for a data converter operating in the bipolar mode.

Output Resistance (R_O)
Output resistance is the equivalent internal resistance for a current output D/A converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV. It is a direct measure of the true compliance.

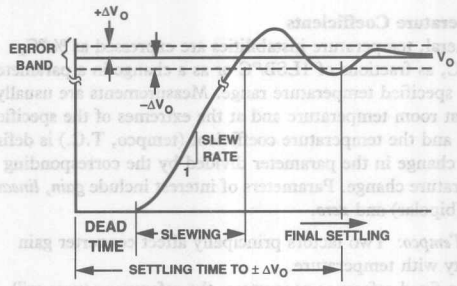
Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% dc change in the power supply (e.g., $0.05\%/1\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed $\pm 1/2$LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of $\pm 1/2$LSB due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Relative Accuracy
See Integral Nonlinearity.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7111 LOGDAC, has a logarithmic gain resolution of 0.375/88.5dB = 1:256dB which corresponds to a gain increment of 4.25%/step or 26,600:1.

Settling Time
The time required, following a prescribed data change from the 50% point of the logic input change, for the output of a DAC to reach and to remain within a given fraction (usually $\pm 1/2$LSB) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op amp circuit.



Settling Time Measurement

Signal-to-Noise Ratio
The measured ratio of signal to noise (SNR) at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by:

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 50dB.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see *Temperature Coefficient*).

Staircase
A voltage or current increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot) generated by applying a pulse train to a counter and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1LSB, the count is stopped and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10% – 90%) but does not include settling time, e.g., to <1/2LSB.

Temperature Coefficients
In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1LSB/°C or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar) and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C.
b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g., AD566K/T). High resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source
b) The voltage zero-stability of the output amplifier
c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC) and offset voltage and bias current of the output op amp (voltage-output DAC).

Three-State Outputs
A digital output circuit that can be programmed to output a logic low, logic high, or a high output impedance state. These outputs are generally connected to digital buses.

Total Unadjusted Error
Total unadjusted error is a comprehensive specification which includes internal voltage reference error, relative accuracy, gain and offset errors.

True Compliance
The true compliance of a DAC is the voltage range over which the current output can vary while the DAC maintains an absolute accuracy of ±1/2 LSB. The higher the DAC output impedance, the better the voltage compliance will be.

Unipolar Output
A DAC operates in the unipolar output mode when the analog output starts at a zero, stopping at a full-scale positive or negative value, while the digital inputs are changed from zero to all-ones code. The analog output occurs in one quadrant.

Zero-Scale Error (V_{ZSE}, I_{ZSE})
The zero-scale error is the error at analog zero for a data converter operating in the unipolar mode.

Zero-Scale Drift (TCV_{ZS}, TCI_{ZS})
The variation of zero scale measured over the operating temperature. It is expressed in ppmFS/°C, or %FS/°C, etc.

Zero-Scale Symmetry Error (V_{ZSS})
This definition applies only to sign-magnitude DACs. It is the change in the analog output produced by switching the sign bit with a zero-code input to the magnitude bits. It is expressed in units of voltage, current, or in fractions of an LSB.

Zero- and Gain-Adjustment Principles
The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for FS $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to $-$FS with all bits off, and the gain is set for $+$FS $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

DEFINITIONS—COMPANDING DACs

Chord
The mathematical formula describing the DAC transfer function is implemented by performing a piecewise linear approximation of the function. The straight line segments used in the approximation are called chords.

Chord Endpoints
The digital code corresponding to the maximum analog output for a given chord is called the chord endpoint.

Dynamic Range (DR)
The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For the COMDACs this would be output ($I_{7,15}$) divided by output ($I_{0,1}$). This is then converted to dB using the formula:

$$DR = 20 \log_{10} \frac{I_{7,15}}{I_{0,1}} \text{ (dB)}$$

Encode Current
The encode current is the difference between $I_{OE(+)}$ and $I_{OD(-)}$ or the difference between $I_{OE(-)}$ and $I_{OD(-)}$ at any code.

Full-Scale Symmetry Error
The full-scale symmetry error of a DAC is the difference between the maximum and the minimum analog output values. For the COMDAC this is the difference between $I_{OD(-)}$ and $I_{OD(+)}$ or $I_{OE(+)}$ and $I_{OE(-)}$.

Output-Level Notation
Each output current level may be designated by the digital input code as $I_{C,S}$, where c = chord number and s = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of the first chord (C_0); and $I_{7,15}$ = full-scale current.

Steps
Each chord is divided into equal increments called steps.

Step Nonlinearity
This is the deviation of the actual step size from the ideal step size within a chord. In a linear DAC, it corresponds to differential nonlinearity.

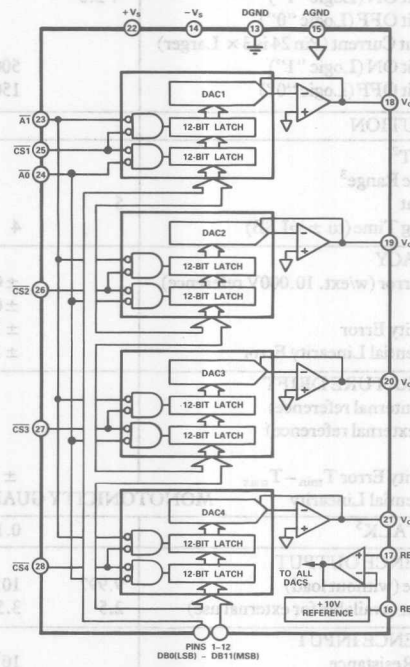
Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390*

FEATURES

- Four Complete 12-Bit DACs in One IC Package
- Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T)
- Factory-Trimmed Gain and Offset
- Buffered Voltage Output
- Monotonicity Guaranteed Over Full Temperature Range
- Double-Buffered Data Latches
- Includes Reference and Buffer
- Fast Settling: 8μs max to ±1/2LSB

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provides high reliability. The AD390 is ideal for systems requiring digital control of many analog voltages where board space is at a premium. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to ±1/2LSB max nonlinearity (AD390KD, TD) and absolute accuracy of ±0.05 percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried Zener voltage reference provides excellent temperature drift characteristics (20ppm/°C) and an initial tolerance of ±0.03% maximum. The internal reference buffer allows a single common reference to be used for multiple AD390 devices in large systems.

The individual DACs are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control inputs and the $\overline{A0}$ and $\overline{A1}$ lines. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD390 outputs are calibrated for a ±10V output range with positive-true offset binary input coding. A 0 to +10V version is available on special order.

The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD390 offers a dramatic reduction in printed circuit board space requirements in systems using multiple DACs.
2. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
3. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 8 microseconds maximum.
4. An internal 10 volt reference is available or an external reference can be used. With an external reference, the AD390 gain TC is ±5ppm/°C maximum.
5. The proprietary monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
6. The 28-pin double-width hybrid package provides extremely high functional density. No external components or adjustments are required to provide the complete function.
7. The AD390SD and AD390TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

***Protected by patent numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486 and other patents pending.**

	Min	Typ	Max	Min	Typ	Max	Units
DATA INPUTS (Pins 1-12 and 23-28)[1]							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
Bit OFF (Logic "0")			+0.8			+0.8	V
Input Current (Pin 24 is 3× Larger)							
Bit ON (Logic "1")		500	1200		500	1200	μA
Bit OFF (Logic "0")		150	400		150	400	μA
RESOLUTION			12			12	Bits
OUTPUT[2]							
Voltage Range[3]			±10			±10	V
Current	5			5			mA
Settling Time (to ±½LSB)		4	8		4	8	μs
ACCURACY							
Gain Error (w/ext. 10.000V reference)		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Linearity Error		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE DRIFT							
Gain (internal reference)			±40			±20	ppm/°C
(external reference)			±10			±5	ppm/°C
Zero			±10			±5	ppm/°C
Linearity Error $T_{min} - T_{max}$		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
CROSSTALK[5]		0.1			0.1		LSB
REFERENCE OUTPUT							
Voltage (without load)	9.997	10.000	10.003	9.997	10.000	10.003	V
Current (available for external use)	2.5	3.5		2.5	3.5		mA
REFERENCE INPUT							
Input Resistance		10^{10}			10^{10}		Ω
Voltage Range	5		11	5		11	V
POWER REQUIREMENTS							
Voltage[6]	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Current							
$+V_S$		20	35		20	35	mA
$-V_S$		−85	−100		−85	−100	mA
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]Timing specifications appear in Table 2.

[2]The AD390 outputs are guaranteed stable for load capacitances up to 300pF.

[3]±10V range is standard. A 0 to 10V version is also available. To order, use the following part numbers:

AD50207-1	J Grade
AD50207-2	K Grade
AD50207-3	S Grade
AD50207-4	T Grade
AD50207-7	S/883B Grade
AD50207-8	T/883B Grade

[4]*FSR means Full Scale Range and is equal to 20V for a ±10V range.*

[5]Crosstalk is defined as the change in any one output as a result of any other output being driven from −10V to +10V into a 2kΩ load.

[6]The AD390 can be used with supply voltage as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

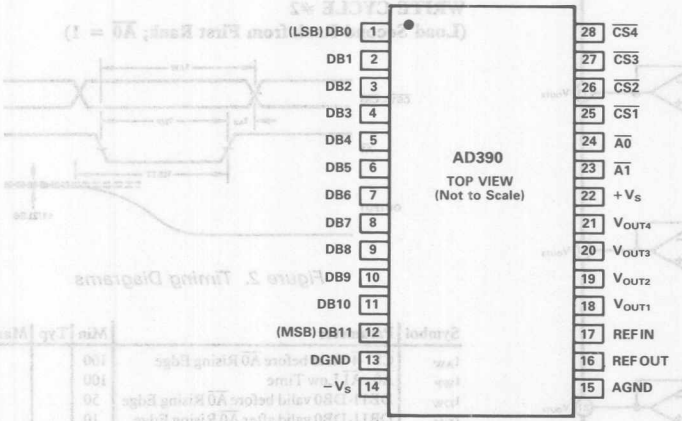
$+V_S$ to DGND . . . . . 0 to +18V
$-V_S$ to DGND . . . . . 0 to −18V
Digital Inputs (Pins 1-12, 23-28) to DGND . . . . −1 to +7V
Ref In to DGND . . . . . $\pm V_S$
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 16, 18-21)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

ORDERING GUIDE

Model	Temperature Range	Gain Error 25°C	Linearity Error $T_{min}-T_{max}$	Package Option*
AD390JD	0 to +70°C	±4LSB	±3/4LSB	DH-28
AD390KD	0 to +70°C	±2LSB	±1/2LSB	DH-28
AD390SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28
AD390TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28

*DH-28 = Side Brazed Ceramic DIP for Hybrid. For outline information see Package Information section.

PIN CONFIGURATION



AD390—Digital Circuit Details

DATA AND CONTROL SIGNAL FORMAT

The AD390 accepts 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$, $\overline{A0}$ and $\overline{A1}$ The input registers are double-buffered, allowing any register to be updated independently of the others. As detailed in Table I, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. The first rank register of a given DAC is loaded by bringing the appropriate chip select and $\overline{A0}$ both low. The second rank register of any DAC can then be loaded by bringing the appropriate chip select and $\overline{A1}$ both low. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident with $\overline{A1}$ low, all four DAC outputs will be updated to the value in the corresponding first rank registers. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

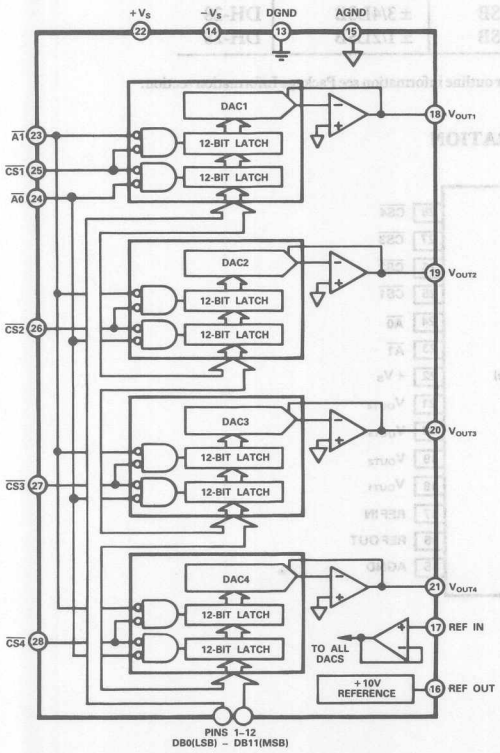


Figure 1. AD390 Functional Block Diagram

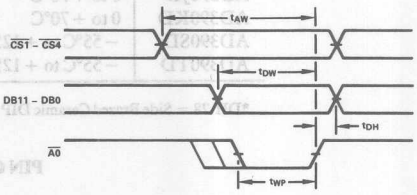
$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{A1}$	$\overline{A0}$	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table I. AD390 Truth Table

TIMING

The AD390 control signal timing is fairly straightforward. $\overline{A0}$, $\overline{A1}$ and $\overline{CS1}$-$\overline{CS4}$ must be concurrently valid for at least 100ns for a desired operation to occur. When loading data from a bus into the first rank register, the data inputs must be stable for at least 50ns before any control signal returns high. Data can change immediately after the control signals are inactive. When loading the second rank registers from the first rank, it is possible to exercise the chip select inputs at the same time as $\overline{A1}$. DAC settling time is measured from the falling edge of whichever control signal last becomes valid.

WRITE CYCLE #1
(Load First Rank from Data Bus; $\overline{A1}$ = 1)



WRITE CYCLE #2
(Load Second Rank from First Rank; $\overline{A0}$ = 1)

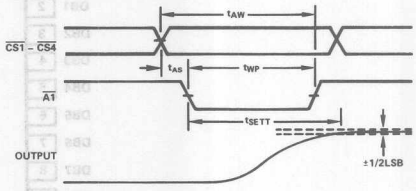


Figure 2. Timing Diagrams

Symbol	Parameter	Min	Typ	Max	Units
t_{AW}	$\overline{CS1-4}$ Valid before $\overline{A0}$ Rising Edge	100			ns
t_{WP}	$\overline{A0}$, $\overline{A1}$ Low Time	100			ns
t_{DW}	DB11-DB0 valid before $\overline{A0}$ Rising Edge	50			ns
t_{DH}	DB11-DB0 valid after $\overline{A0}$ Rising Edge	10			ns
t_{AS}	$\overline{CS1-4}$ valid before $\overline{A1}$ Low	0			ns
t_{SETT}	Output Voltage Settling Time		4	8	µs

Table II. AD390 Timing Specifications

INTERFACING THE AD390 TO MICROPROCESSORS

16-Bit Processors

The AD390 is a 12-bit resolution DAC system and is easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 3, the AD390 second rank registers are made transparent by hard-wiring $\overline{A1}$ low. A system $\overline{WR}$ signal is used to drive the $\overline{A0}$ control input and a 74LS139 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In this circuit, only one DAC at a time may be updated. If simultaneous update of all four DACs is required, a slightly different addressing scheme is used. The circuit shown in Figure 4 allows selection of either register of any DAC at the expense of larger memory space requirements. In this circuit, address lines A0 through A3 each select a single DAC of the four contained in the AD390. The use of a separate address line for each DAC allows several DACs to be accessed

simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address. Selection of first rank or second rank register for any DAC is done by using two additional address bits. The AD390 thus occupies a block of 64 memory word locations but offers considerable flexibility in DAC updating.

In this addressing scheme, the A5 and A4 lines divide the 64 locations into 4 blocks. When both A5 and A4 are high, no operation occurs. When A5 and A4 are both low, data written into any one of the DACs (selected by A3-A0) will immediately update that analog output. In the address block where A4 is low and A5 is high, data is written into the first rank register of the selected DAC (or DACs). When A5 is low and A4 is high, data previously written into the first rank register of the selected DAC is transferred to the second rank register, which updates the analog output. It is particularly useful to perform a $\overline{WR}$ operation with A5 low, A4 high, and A3 through A0 all low (base address plus 32) since this action will cause all four DAC outputs to be simultaneously updated to the values previously written into the first rank registers.

In both addressing schemes shown, A0 represents the least significant *word address* bit. In most 16-bit systems this will be the A1 address line. Data may reside in either the 12MSBs (left-justified) or the lower 12 bits (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

8-Bit Processors

Since the AD390 is designed to accept data in 12-bit words, an external latch is required in order to interface with 8-bit buses. Thus each DAC in the AD390 occupies 2 memory locations. The choice of data format is similar to the choice in the 16-bit bus interface. The data can either be right-justified (one byte contains the 8LSBs and another the 4MSBs in the bottom half of the byte) or left-justified (where one byte contains the 8MSBs and another the 4LSBs in the top half of the byte). The addressing scheme illustrated in Figure 6 allows 12-bit data to be sent to the first rank register of any DAC in a right-justified format. The first rank register of DAC occupies two memory locations–a write to the even (A0 low) address stores the 4MSBs of the DAC data in a 74LS173 quad latch. When the 8LSBs are written to the odd address (A0 = 1), the eight bits present on the data bus and the four bits held in the 74LS173 are strobed into the first rank register of the selected DAC. Address bits A1 through A4 select the DAC to be addressed, while A6 and A5 enable either the first or second rank register (or both) as in the 16-bit interface of Figure 4.

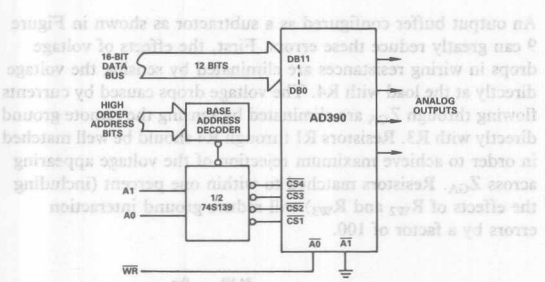


Figure 3. AD390–16-Bit Bus Interface

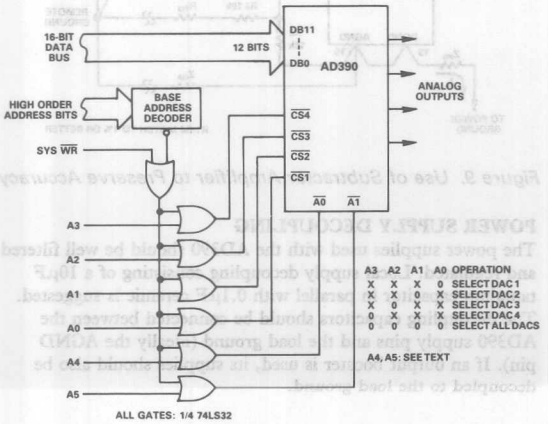
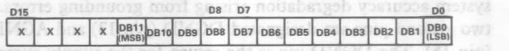
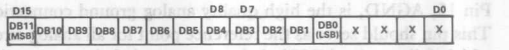


Figure 4. Alternate 16-Bit Bus Interface



a. Right-Justified Data ($0 \le D \le 4095$);

$V_{OUT} = -10V + (4.883mV \times D)$



b. Left-Justified Data $\left(0 \le D \le \frac{65520}{65536}\right)$;

$V_{OUT} = -10V + (20V \times D)$

Figure 5. 12-Bit Data Formats for 16-Bit Bus

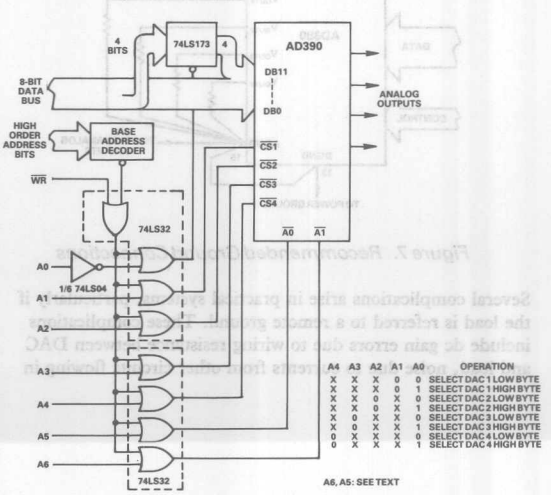


Figure 6. AD390–8-Bit Bus Interface Connections

REFERENCE CONNECTIONS

The AD390 is equipped with a precision internal reference voltage of 10.00 volts, trimmed to within ±3 millivolts. This reference is available for external use and can typically supply up to 3.5 milliamps of output current. In normal operation, this reference is connected to pin 17 (REF IN), which establishes the ±10 volt output scale. The internal reference is sufficiently accurate for most applications, however, if a master system reference is available, or if a range other than ±10V (±10.24V, for example) is desired, an external reference may be used. It is recommended that the reference used with the AD390 be at least 5 volts and at most 11 volts to preserve specified linearity.

Digital Input Code	Analog Output Voltage	
0000 0000 0000	−10.000V	−Full Scale
0100 0000 0000	−5.000V	−1/2 Scale
1000 0000 0000	0.000V	Zero
1000 0000 0001	+4.88mV	+1LSB
1100 0000 0000	+5.000V	+1/2 Scale
1111 1111 1111	+9.9951V	+Full Scale −1LSB

Table III. AD390 Analog Output vs. Digital Input (±10V Scale)

GROUNDING RULES

The AD390 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 13) and AGND (pin 15). The DGND pin is the return for the supply currents of the AD390, and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the digital circuitry which drives the AD390.

Pin 15, AGND, is the high quality analog ground connection. This pin should serve as the reference point for all analog circuitry which follows the AD390. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 15 as shown in Figure 7.

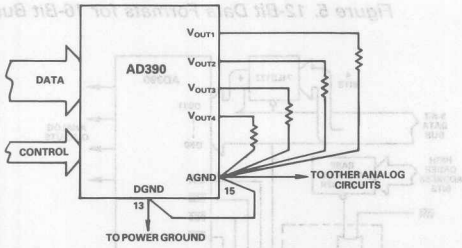


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the AD390 outputs are accurately developed between the output pin and pin 15 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD390 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

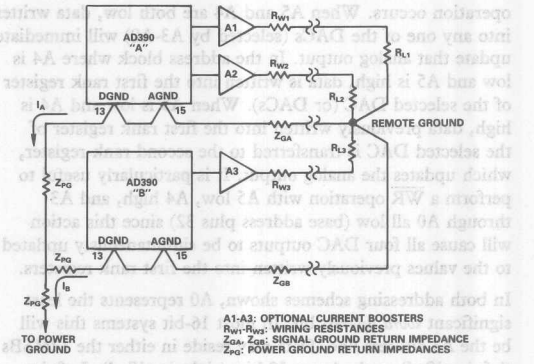


Figure 8. Grounding Errors in Multiple-AD390 Systems

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances are eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

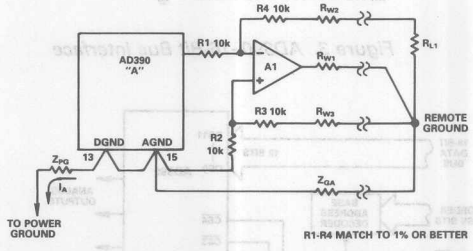


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

POWER SUPPLY DECOUPLING

The power supplies used with the AD390 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD390 supply pins and the load ground (ideally the AGND pin). If an output booster is used, its supplies should also be decoupled to the load ground.

OPERATION FROM ±12 VOLT SUPPLIES

The AD390 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB). The required 8.192V reference can be derived from a precision, low TC divider from the internal +10.000V reference. The only restriction is that the total load resistance presented to the +10.000V reference output must be at least 10kΩ for −55°C to +125°C temperature range 12 volt applications. Figure 10 shows a suggested circuit to set up a ±8.192V output range. Multiple AD390 units can share the same resistive divider-generated reference since the REF IN terminal is very high impedance.

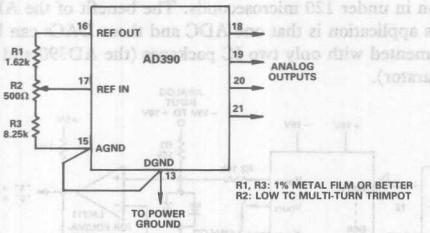


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

IMPROVING FULL-SCALE STABILITY

In large systems using multiple AD390s, it may be desirable for all devices to share a common reference. While it is possible to use the reference output for one device to provide a reference for all devices, use of an external precision reference can greatly improve system accuracy and temperature stability. The external reference should be at least +5V and at most +11V to preserve DAC linearity.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C, compared with the 10 to 20ppm/°C drift of the AD390 internal reference. The combination of the AD2710LN and AD390KD shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

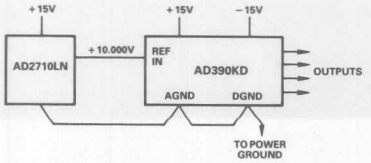
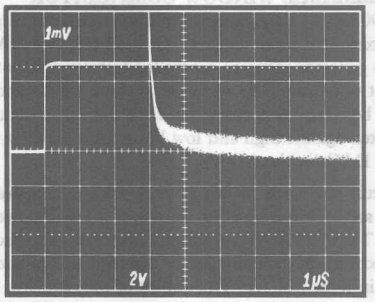


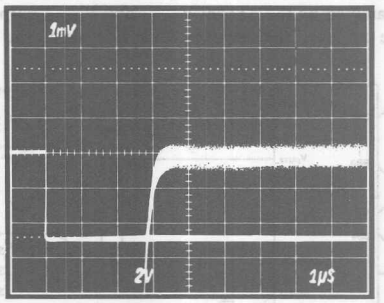
Figure 11. Low Drift AD390 Configuration

OUTPUT CURRENT BOOSTING

The output amplifiers used in the AD390 are capable of supplying a ±10 volt swing into a resistive load of 2kΩ or greater. Stability is guaranteed for load capacitance up to 300pF. Larger load capacitance may cause severe overshoot and possible oscillation. The settling characteristic of the AD390 output amplifier is shown in Figure 12.



a. All Bits OFF-to-ON



b. All Bits ON-to-OFF

Figure 12. AD390 Settling Characteristic

In many applications, including automatic test equipment, the load presented to the AD390 may be less than 2kΩ or include large capacitance. In such cases, it is advisable to use a buffer amplifier capable of delivering rated output to the most severe load anticipated. The AD382, for example, can supply ±10V into a 200Ω load and the AD3554 is suitable for load resistances down to 100Ω. In applications where errors due to output boosting must be minimized, the composite amplifier shown in Figure 13 provides excellent dc stability as well as 100mA output drive capability.

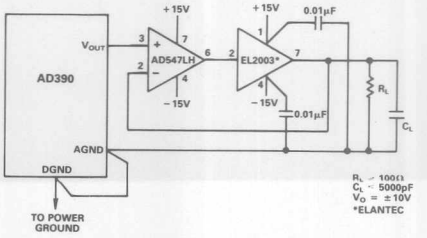


Figure 13. Composite Amplifier for Increased Output Drive

APPLICATIONS

The functional density of the AD390 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD390 in a fraction of the space which would be needed if separate DACs were used.

PROGRAMMABLE WINDOW COMPARATOR

The AD390 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD390.

In the circuit of Figure 14 two LM311 voltage comparators are used with an AD390 to test the output of a 5 volt power supply regulator. The AD390 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD390 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

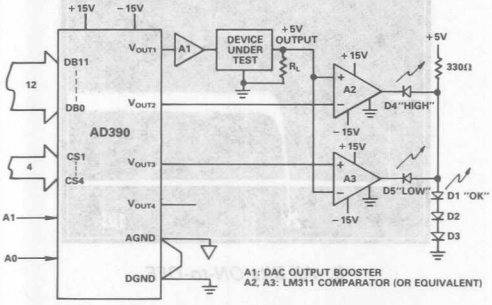


Figure 14. Programmable Window Comparator Used in Power Supply Testing

USING THE AD390 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD390 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD390 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 15. The LM311 comparator compares the unknown input voltage to one of the AD390 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 10 microseconds, resulting in 12-bit successive approximation conversion in under 120 microseconds. The benefit of the AD390 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD390 and the comparator).

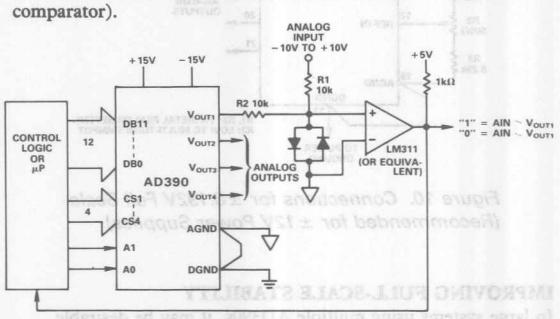


Figure 15. Using One AD390 Output for A/D Conversion

ANALOG DEVICES

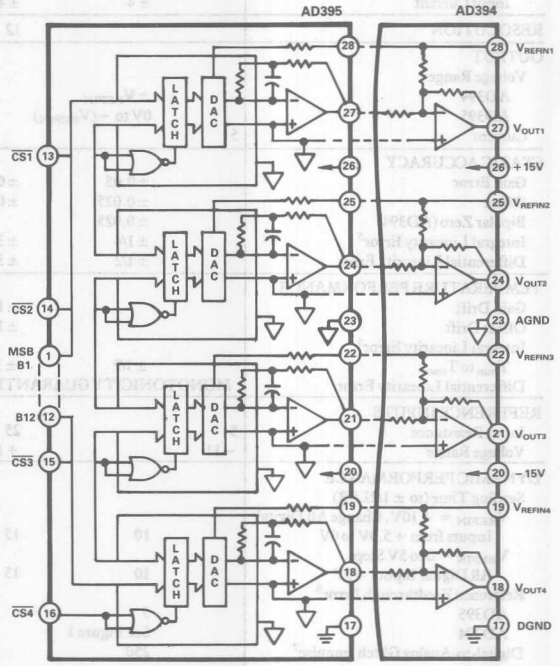
µP-Compatible Multiplying Quad 12-Bit D/A Converters

AD394/AD395

FEATURES

- Four Complete 12-Bit CMOS DACs with Buffer Registers
- Linearity Error ±1/2LSB T_{min}-T_{max} (AD394, AD395K,T)
- Factory-Trimmed Gain and Offset
- Precision Output Amplifiers for V_{OUT}
- Full Four Quadrant Multiplication per DAC
- Monotonicity Guaranteed Over Full Temperature Range
- Fast Settling: 15µs Max to ±1/2LSB
- Available to MIL-STD-883 (See ADI Military Catalog)

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD394 and AD395 contain four 12-bit, high-speed, low power, voltage output multiplying digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit CMOS DAC chip which reduces chip count and provides high reliability. The AD394 and AD395 both are ideal for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

Both the AD394 and the AD395 are laser-trimmed to ±1/2LSB max differential and integral linearity (AD394, AD395K,T) and full scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with a single 12-bit wide word. The 12-bit parallel digital input interfaces to most 12- and 16-bit bus systems.

The AD394 outputs (V_{REFIN} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding. The AD395 outputs (V_{REFIN} = −10V) provide a 0V to +10V unipolar output range with straight binary input coding.

Both the AD394 and the AD395 are packaged in a 28-lead ceramic package and are available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD394, AD395 offer a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by both the AD394 and the AD395.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Two or four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DAC's reference (V_{REFIN}).
9. Both the AD394S,TD and AD395S,TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

AD394/AD395—SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD394JD/SD[1] AD395JD/SD			AD394KD/TD[1] AD395KD/TD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[3]							
AD394		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
AD395		0V to $-(V_{REFIN})$			0V to $-(V_{REFIN})$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero (AD394)		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step, All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]							
AD395		5			5		mV p-p
AD394		See Figure 1			See Figure 1		
Digital-to-Analog Glitch Impulse[7]		250			250		nV·sec
Crosstalk							
Digital Input (Static)[8]		0.1			0.1		LSB
Reference[9]		2.0			2.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	28		20	28	mA
$-V_S$		18	22		18	22	mA
Power Dissipation		570	750		570	750	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]AD394 and AD395 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Catalog for proper part number and detail specification.

[2]Timing specifications appear in Table IV and Figure 5.

[3]Code tables and graphs appear on Theory of Operation page.

[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.

[6]For AD395 (unipolar), DAC register loaded with 0000 0000 0000, V_{REFIN} = 20V p-p, 10kHz sinewave. For AD394 (bipolar), V_{REFIN} = 20V p-p, 60 and 400Hz.

[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.

[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.

[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.

[10]The AD394 and the AD395 can be used with supply voltages as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND . . . . . −0.3V to +17V
$-V_S$ to DGND . . . . . +0.3V to −17V
Digital Inputs (Pins 1-16) to DGND . . . . . −0.3V to +7V
V_{REFIN} to DGND . . . . . ±25V
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 18, 21, 24, 27)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



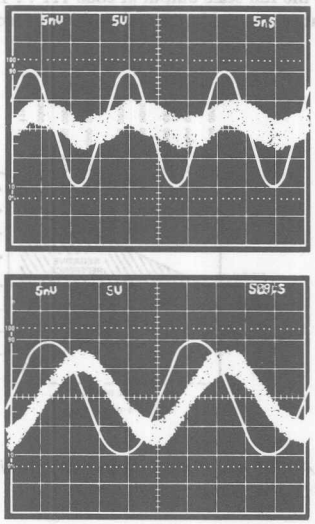


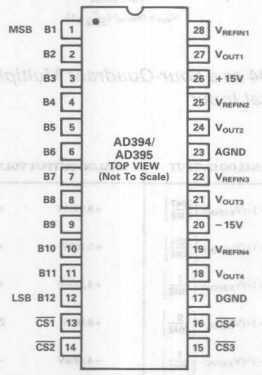
Figure 1. AD394 Feedthrough V_{REFIN} = 60Hz (top photo) and 400Hz (bottom photo) Sinewave. Digital code is set at 1000 000 0000.
SCALE: Reference Input 5V/DIV (Thin Trace)
Feedthrough Output 5mV/DIV
TIME: Top Photo 5ms/DIV
Bottom Photo 500µs/DIV

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD394, AD395, with the inherent reliability of integrated circuit construction, were designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliability, the AD394, AD395 are both fully compliant to MIL-STD-883 Class B, Method 5008.

Consult Analog Devices Military Catalog for proper ordering part number and detail specification.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD394JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD395JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD394KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD395KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD394SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD395SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD394TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A
AD395TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A

*DH-28A = Ceramic DIP. For outline information see Package Information section.

AD394/AD395—Theory of Operation

The AD394 quad DAC provides four-quadrant multiplication. It is a hybrid IC comprised of four monolithic 12-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or an ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has a 12-bit wide data latch to buffer the converter when connected to a microprocessor data bus.

The AD395 quad DAC provides two-quadrant multiplication and is comprised of four 12-bit CMOS multiplying DACs and four precision output amplifiers. The two-quadrant-multiplication function arises from a straight-binary digital input multiplied by a bipolar analog input which results in two-quadrant multiplication. The AD395 can also operate as a standard unipolar DAC when a fixed dc reference is applied to V_{REFIN}.

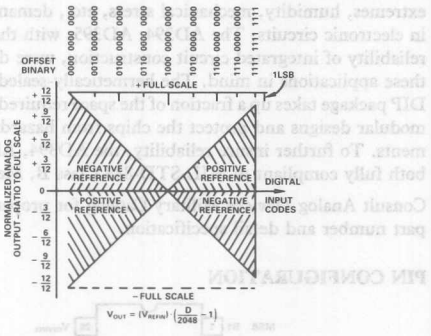


Figure 2. AD394 as a Four-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$+1 \cdot (V_{REFIN}) \left\{\frac{2047}{2048}\right\}$	+9.9951V	+FULL SCALE – 1LSB
1100	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0001	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{2048}\right\}$	+0.000V	ZERO
0111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	–4.88mV	–1LSB
0100	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	–5.000V	–1/2 SCALE
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{2048}\right\}$	–10.000V	–FULL SCALE

Table I. AD394 Bipolar Code Table

MULTIPLYING MODE

The figures below show the transfer function for each model. The diagrams indicate an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in each diagram indicates the transfer function if a fixed reference is at the input. The digital codes above each diagram indicate the mid and endpoints of each function. The relationship between the reference input (V_{REFIN}) the digital input code and the analog output is given in Tables I and II below. Note that the reference input signal sets the slope of the transfer function (and determines the full scale output at code 111 . . 111) while the digital input selects the horizontal position in each diagram.

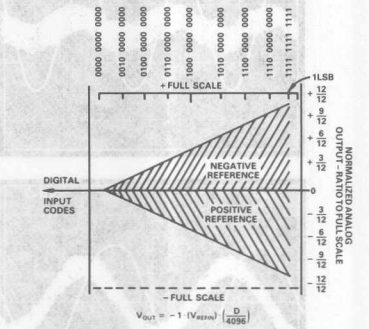


Figure 3. AD395 as a Two-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{4095}{4096}\right\}$	–9.9976V	–FULL SCALE – 1LSB
1000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{4096}\right\}$	–5.000V	–1/2 SCALE
0000	0000	0001	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{4096}\right\}$	–2.44mV	–1LSB
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{0}{4096}\right\}$	0.000V	ZERO

Table II. AD395 Unipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD394 and AD395 accept 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$. As detailed in Table III, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident, all four DAC outputs will be updated to the value located on the data bus. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

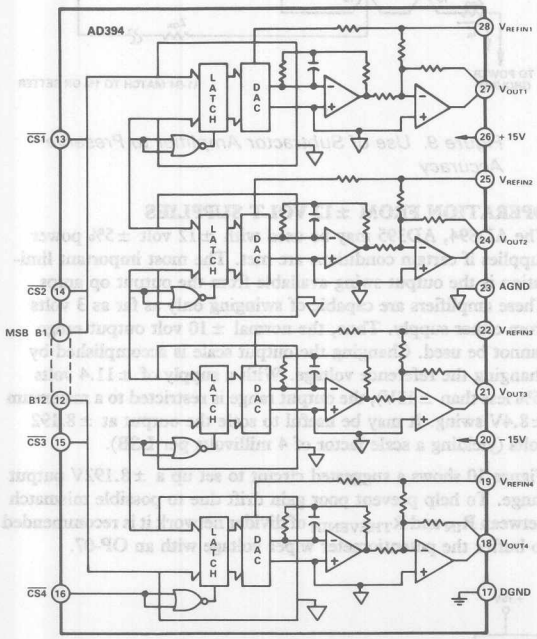


Figure 4. AD394 (Bipolar) Functional Block Diagram

TIMING

The AD394, AD395 control signal timing is very straightforward. $\overline{CS1}$-$\overline{CS4}$ must maintain a minimum pulsewidth of at least 170ns for a desired operation to occur. When loading data from a bus into a 12-bit wide data latch, the data must be stable for at least 150ns before returning CS to a high state. When the $\overline{CS}$ is low, the data latch is transparent allowing the data at the input to propagate through to the DAC. Data can change immediately *after the chip select returns high. DAC settling time is measured* from the falling edge of the active chip select.

Symbol	Parameter	t_{min} to t_{max}	Units
t_{CS}	Chip Select Pulse Width	170	ns min
t_{DA}	Data Access Time	0	ns min
t_{DS}	Data Set-Up Time	150	ns min
t_{DH}	Data Hold Time	5	ns min

Table IV. AD394, AD395 Timing Specifications

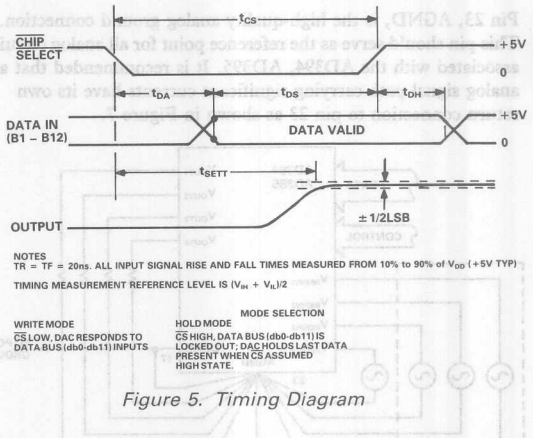


Figure 5. Timing Diagram

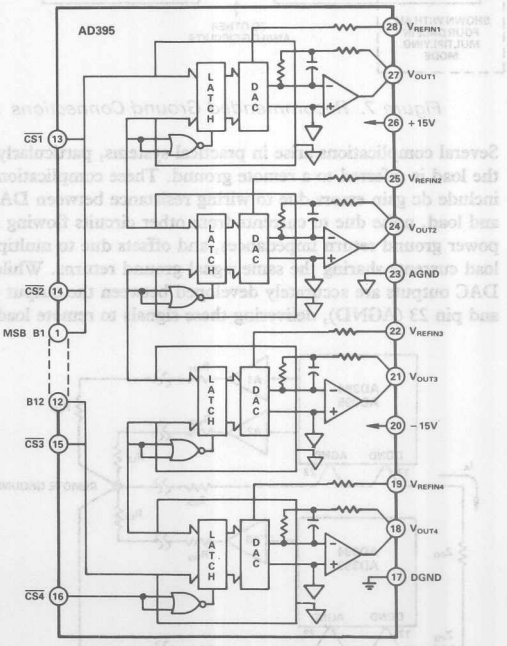


Figure 6. AD395 (Unipolar) Functional Block Diagram

AD394/AD395—Analog Circuit Details

GROUNDING RULES

The AD394 and AD395 include two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 17) and AGND (pin 23). The DGND pin is the return for the supply currents of the AD394, AD395 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD394, AD395. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 23 as shown in Figure 7.

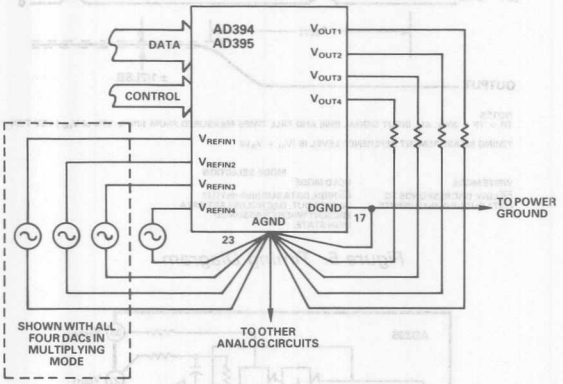


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and pin 23 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD394, AD395 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

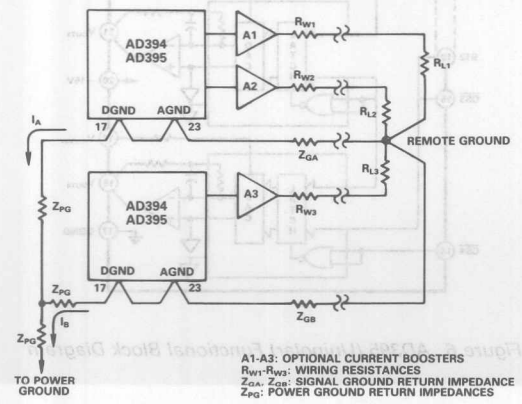


Figure 8. Grounding Errors in Multiple-AD394, AD395 Systems

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

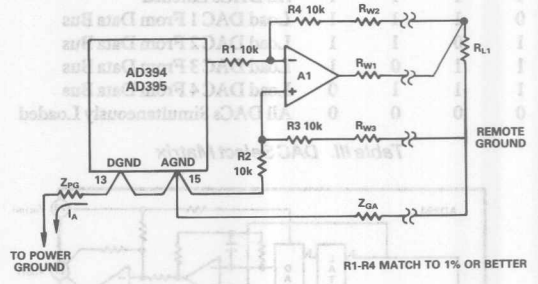


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12 VOLT SUPPLIES

The AD394, AD395 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB).

Figure 10 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

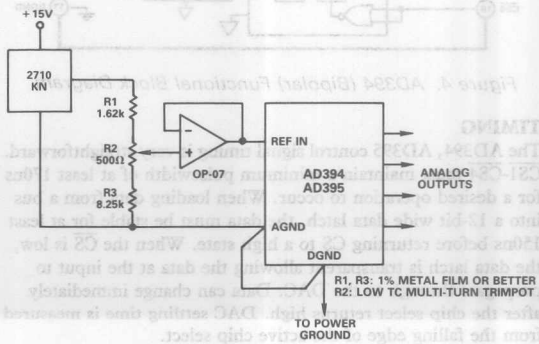


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD394, AD395 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD394 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C. The combination of the AD2710LN and AD394, AD395 shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

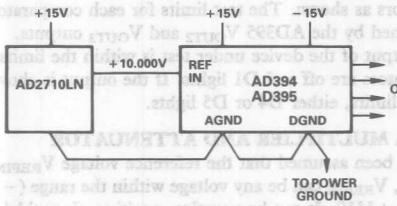


Figure 11. Low Drift AD394, AD395 Configuration

Applications

INTERFACING THE AD394, AD395 TO MICROPROCESSORS

The AD394, AD395 control logic provides simple interface to microprocessors. The individual latches allow for multi-DAC interfacing to a single data bus.

16-BIT PROCESSORS

The AD394, AD395 are 12-bit resolution DAC systems and are easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 12, a system write signal is used to control the decoded address lines and a 74LS139 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In the circuit of Figure 12, address lines A0 and A1 each select a single DAC of the four contained in the AD394 or AD395. The use of a separate address line for each DAC allows several DACs to be accessed simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address.

In the addressing scheme shown, A0 represents the least significant word address bit. Data may reside in either the 12MSBs (left-justified) or the 12LSBs (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

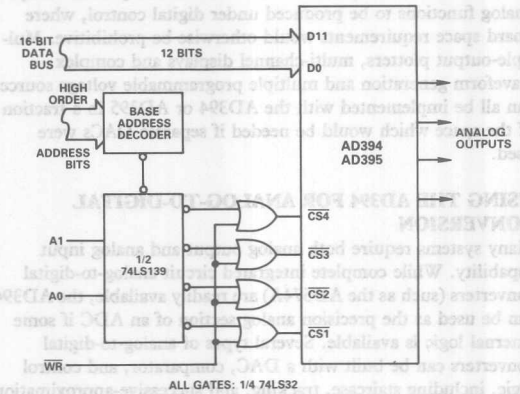


Figure 12. AD394, AD395 16-Bit Bus Interface

8-BIT PROCESSORS

The circuit of Figure 13 shows the general principles for connecting the AD394 or the AD395 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 12-bit word. The connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, and when active, the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer ensure that the inputs to the DAC do not float at an ill-defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when multiple DACs are utilized for 8-bit data bus applications.

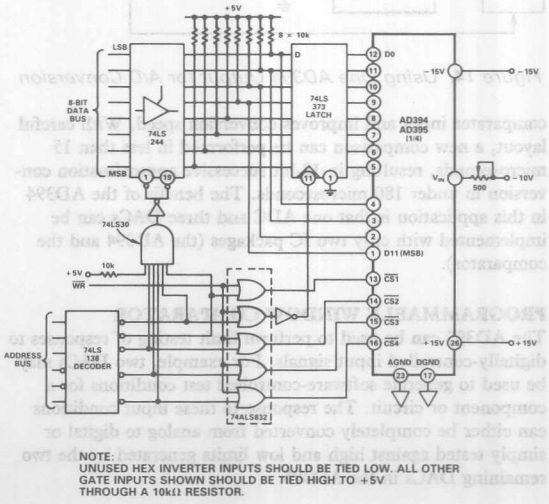


Figure 13. AD394, AD395 8-Bit Data Bus Interface

tiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD394 or AD395 in a fraction of the space which would be needed if separate DACs were used.

USING THE AD394 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD394 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD394 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 14. The AD311 comparator compares the unknown input voltage to one of the AD394 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the

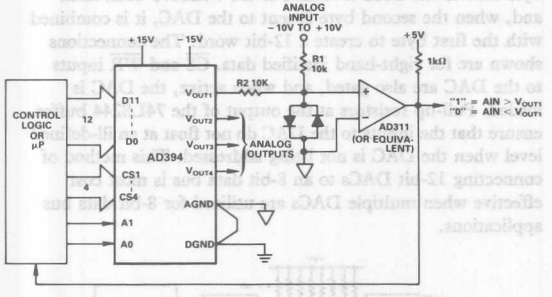


Figure 14. Using One AD394 Output for A/D Conversion

comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 15 microseconds, resulting in 12-bit successive approximation conversion in under 180 microseconds. The benefit of the AD394 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD394 and the comparator).

PROGRAMMABLE WINDOW COMPARATOR

The AD395 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD395.

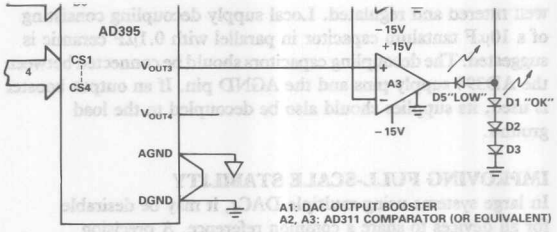


Figure 15. Programmable Window Comparator Used in Power-Supply Testing

In the circuit of Figure 15, two AD311 voltage comparators are used within AD395 to test the output of a 5 volt power-supply regulator. The AD395 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD395 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

AD395 AS A MULTIPLIER AND ATTENUATOR

So far, it has been assumed that the reference voltage V_{REFIN} is fixed. In fact, V_{REFIN} can be any voltage within the range ($-11V < V_{REFIN} < +11V$). It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converters" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REFIN} terminal.

$$V_{OUT} = -1 \cdot (V_{REFIN}) \cdot \frac{D}{(4096)} \qquad (0<D<4095)$$

D is the fractional binary value of the digital word applied to the converter. The AD395 multiplies the digital input value by the analog input voltage at V_{REFIN} for any value of V_{REFIN} up to 22V p-p. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion should consider the AD395 as a candidate. One popular use for AD395 is as a audio frequency attenuator. The audio signal is applied to the V_{REFIN} input and the attenuation code is applied to the DAC; the output voltage is the product of the two – an attenuated version of the input. The maximum attenuation range obtainable utilizing 12-bits is 4096:1 or 72db.

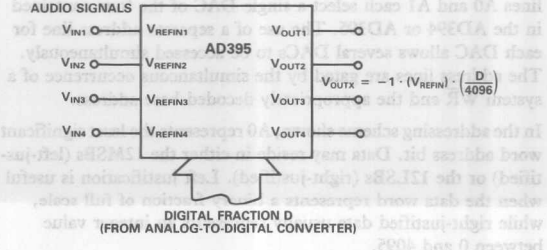
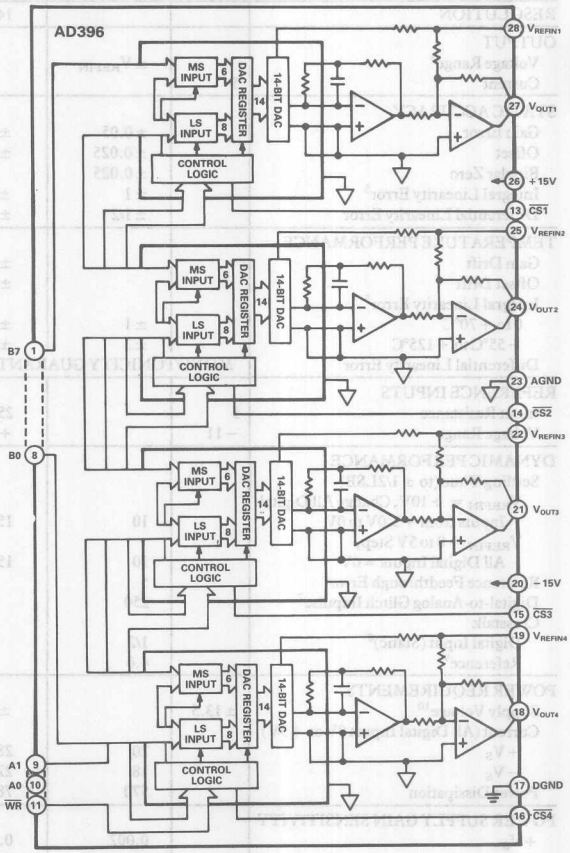


Figure 16. AD395 as a Multiplier or Attenuator

FEATURES

Four, Pre-Trimmed, 14-Bit CMOS DACs
Double Buffered for Simultaneous Update
Precision Output Amplifiers for Voltage Out
Full Four Quadrant Multiplication – Independently Pinned Out DAC Reference
Monotonicity Guaranteed Over Full MIL Temp. Range
Low Power – 780mW Max
Small 28 Lead, Hermetic Double DIP Package
MIL-STD-883 Processing Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD396 is a high-speed microprocessor compatible Quad 14-bit digital-to-analog converter. The AD396 contains four 14-bit, low power multiplying digital-to-analog converters followed by precision voltage output amplifiers all in a compact 28-pin hybrid package. The design is based on a proprietary latched 14-bit CMOS DAC chip which reduces chip count and provides high reliability.

The AD396 (K, T) is laser-trimmed to ±1LSB max differential and integral linearity, and to full-scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DACs. Address lines A0, and A1, control internal register loading and transfer.

The AD396 outputs (V_{REF} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding.

The AD396 is packaged in a 28-lead ceramic DIP package and is available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

The AD396 is for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

PRODUCT HIGHLIGHTS

1. The AD396 offers a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full-scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by the AD396.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DACs reference (V_{REFIN}).
9. The AD396S, T features guaranteed accuracy and linearity over the −55°C to +125°C temperature range.
10. MIL-STD-883 processing is available. See Analog Devices Military Data Sheet for further information.
11. Protection against power supply surges is included within the AD396.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD396 — SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD396JD/SD[1]			AD396KD/TD[1]			
	Min	Typ	Max	Min	Typ	Max	Units
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			14			14	Bits
OUTPUT							
Voltage Range[3]		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1	±2		±1/2	±1	LSB
Differential Linearity Error		±1/2	±1		±1/2	±1	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
0 to +70°C		±1	±2		±1/2	±1	LSB
−55°C to +125°C		±2	±4		±1	±2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital							
Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step,							
All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]		5			5		mV p-p
Digital-to-Analog Glitch Impulse[7]		250			250		nV·sec
Crosstalk							
Digital Input (Static)[8]		1/2			1/2		LSB
Reference[9]		4.0			4.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	28		20	28	mA
$-V_S$		18	22		18	22	mA
Power Dissipation		570	780		570	780	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]AD396S and T grades are available to MIL-STD-883, Method 5008, Class B.

[2]Timing specifications appear in Table IV and Figure 3.

[3]Code tables and graphs appear on Theory of Operation page.

[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range.

[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.

[6]For AD396 (bipolar), DAC register loaded with 10 0000 0000 0000, V_{REFIN} = 20V p-p, 60 and 400Hz.

[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.

[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.

[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.

[10]The AD396 can be used with supply voltages as low as ±11.4V. See Figure 7 of the full data sheet.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND . . . . . −0.3V to +17V
$-V_S$ to DGND . . . . . +0.3V to −17V
Digital Inputs (Pins 1-16) to DGND . . . . . −0.3V to +7V
V_{REFIN} to DGND . . . . . ±25V
AGND to DGND . . . . . +0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD396JD	0 to +70°C	±16LSB	±2LSB	DH-28A
AD396KD	0 to +70°C	±8LSB	±1LSB	DH-28A
AD396SD	−55°C to +125°C	±16LSB	±2LSB	DH-28A
AD396TD	−55°C to +125°C	±8LSB	±1LSB	DH-28A

*DH-28A = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

2

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATION



PIN	FUNCTION	DESCRIPTION
1	DB7	DATA BIT 7
2	DB6	DATA BIT 6
3	DB5	DATA BIT 5/DATA BIT 13 (DAC MSB)
4	DB4	DATA BIT 5/DATA BIT 12
5	DB3	DATA BIT 3/DATA BIT 11
6	DB2	DATA BIT 2/DATA BIT 10
7	DB1	DATA BIT 1/DATA BIT 9
8	DB0	DATA BIT 0/DATA BIT 8
9	A1	ADDRESS LINE 0
10	A0	ADDRESS LINE 1
11	$\overline{WR}$	WRITE INPUT. ACTIVE LOW
12	NC	NO CONNECTION
13	$\overline{CS1}$	CHIP SELECT DAC 1. ACTIVE LOW
14	$\overline{CS2}$	CHIP SELECT DAC 2. ACTIVE LOW
15	$\overline{CS3}$	CHIP SELECT DAC 3. ACTIVE LOW
16	$\overline{CS4}$	CHIP SELECT DAC 4. ACTIVE LOW
17	DGND	DIGITAL GROUND
18	V_{OUT4}	DAC 4 VOLTAGE OUTPUT
19	V_{REFIN4}	DAC 4 REFERENCE INPUT
20	−15V	−15V SUPPLY INPUT
21	V_{OUT3}	DAC 3 VOLTAGE OUTPUT
22	V_{REFIN3}	DAC 3 REFERENCE INPUT
23	AGND	ANALOG GROUND
24	V_{OUT2}	DAC 2 VOLTAGE OUTPUT
25	V_{REFIN2}	DAC 2 REFERENCE INPUT
26	+15V	+15V SUPPLY INPUT
27	V_{OUT1}	DAC 1 VOLTAGE OUTPUT
28	V_{REFIN1}	DAC 1 REFERENCE INPUT

Theory of Operation

The AD396 quad DAC provides four-quadrant multiplication. It is a hybrid comprised of four monolithic 14-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has data latches to buffer the converter when connected to a microprocessor data bus.

MULTIPLYING MODE

Figure 1 shows the transfer function for the AD396. The diagram indicates an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in the diagram indicates the transfer function for a fixed reference at the input.

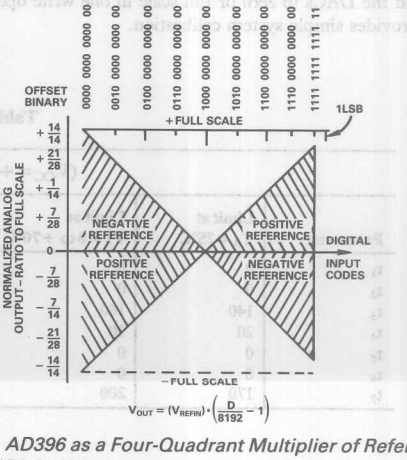


Figure 1. AD396 as a Four-Quadrant Multiplier of Reference Input and Digital Input

The digital codes above the diagram indicates the mid and end-points of the function. The relationship between the reference input (V_{REFIN}), the digital input code, and the analog output is given in Table I below. Note that the reference input signal sets the slope of the transfer function (and determines the full-scale output at code 111..111) while the digital input selects the horizontal position in each diagram.

Table I. AD396 Bipolar Code Table

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE (V_{REFIN} = +10 VOLTS)
1111	1111	1111 11	$+1 \cdot (V_{REFIN}) \left\{\frac{8191}{8192}\right\}$	+9.9988V
1100	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	+5.000V
1000	0000	0000 01	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	+1.22mV
1000	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{8192}\right\}$	+0.000V
0111	1111	1111 11	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	−1.22mV
0100	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	−5.000V
0000	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{8192}{8192}\right\}$	−10.000V

DATA AND CONTROL SIGNAL FORMAT

The AD396 accepts 14-bit data by loading two separate input registers off an 8-bit data bus, and then loading the internal DAC register. The LS (least significant) register is loaded with the bottom 8-bits of the 14-bit word by selecting the appropriate address lines (see Table II). The MS (most significant) register is loaded with the top 6-bits in a similar manner. The $\overline{CS}$ and $\overline{WR}$ line must also be asserted to load the registers. The internal DAC register can then be loaded with the 14-bit data word. The appropriate DAC or DACs are selected by asserting $\overline{CS1}$-$\overline{CS4}$ (see Table III). If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincidentally, all four DAC outputs will be updated to the value located in the DAC register. When $A_1 = 0$ and $A_0 = 0$ all DAC registers are transparent so by placing all 0s or 1s on the data inputs the user can load the DACs to zero or full scale in one write operation. This provides simple system calibration.

Table II. Truth Table

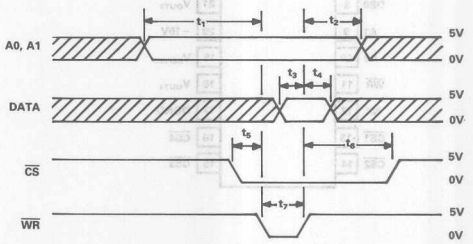
$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

Table III. DAC Select Matrix

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Register
1	0	1	1	Load DAC 2 From Data Register
1	1	0	1	Load DAC 3 From Data Register
1	1	1	0	Load DAC 4 From Data Register
0	0	0	0	All DACs Simultaneously Loaded

TIMING

The AD396 timing is shown in Figure 2, and has restrictions as stated in Table IV. $\overline{WR}$ must maintain a minimum pulse width of 240ns for desired operation to occur. When loading data in from the data bus, data must be stable for at least 180ns before returning $\overline{WR}$ to a high state. The Data must be held constant for at least 30ns after $\overline{WR}$ goes high to assure latching of valid data. DAC settling time is measured from the falling edge of the $\overline{WR}$ command.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 2. AD396 Timing Diagram

Table IV. Timing Characteristics

(V_{CC} = +15V, V_{EE} = −15V, V_{REF} = +10V)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	140	160	180	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

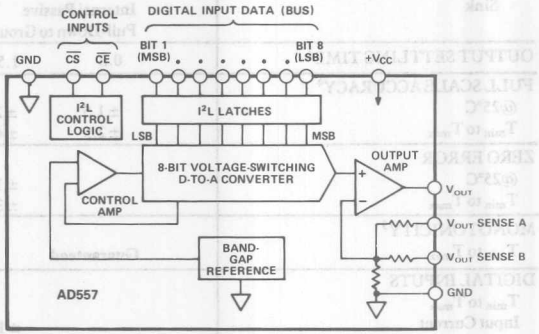
µP-Compatible 8-Bit DAC

AD557

FEATURES

Complete 8-Bit DAC
Voltage Output – 0 to 2.56V
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V (±10%)
Full Microprocessor Interface
Fast: 1µs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP or 20-Pin PLCC Package
Low Cost

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD557 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ±2.5LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD557 is available in two package configurations. The AD557JN is packaged in a 16-pin plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-pin JEDEC standard PLCC. Both versions are specified over the operating temperature range of 0 to +70°C.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The AD557 is designed and specified to operate from a single +4.5V to +5.5V power supply.
5. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.
6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

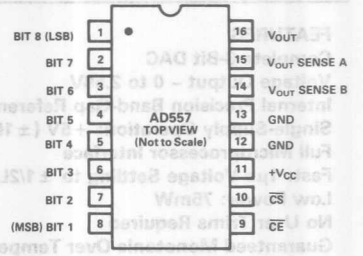
DACPORT is a trademark of Analog Devices, Inc.
Covered by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; other patents pending.

AD557—SPECIFICATIONS (@ T_A = +25C, V_{CC} = +5V unless otherwise specified)

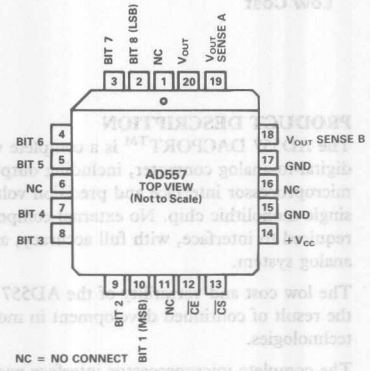
Model	AD557J Min	Typ	Max	Units
RESOLUTION			8	Bits
RELATIVE ACCURACY[1]				
0 to +70°C		±1/2	1	LSB
OUTPUT				
Ranges		0 to +2.56		V
Current Source		+5		mA
Sink		Internal Passive Pull-Down to Ground[2]		
OUTPUT SETTLING TIME[3]		0.8	1.5	µs
FULL SCALE ACCURACY[4]				
@25°C		±1.5	±2.5	LSB
T_{min} to T_{max}		±2.5	±4.0	LSB
ZERO ERROR				
@25°C			±1	LSB
T_{min} to T_{max}			±3	LSB
MONOTONICITY[5]				
T_{min} to T_{max}		**Guaranteed**		
DIGITAL INPUTS				
T_{min} to T_{max}				
Input Current			**±100**	µA
Data Inputs, Voltage				
Bit On – Logic "1"	2.0			V
Bit On – Logic "0"	0		0.8	V
Control Inputs, Voltage				
On – Logic "1"	2.0			V
On – Logic "0"	0		0.8	V
Input Capacitance		4		pF
TIMING[6]				
t_W Strobe Pulse Width	225			ns
T_{min} to T_{max}	**300**			ns
t_{DH} Data Hold Time	10			ns
T_{min} to T_{max}	**10**			ns
t_{DS} Data Setup Time	225			ns
T_{min} to T_{max}	**300**			ns
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	+4.5		+5.5	V
Current (I_{CC})		15	25	mA
Rejection Ratio			**0.03**	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125	mW
OPERATING TEMPERATURE RANGE	0		+70	°C

PIN CONFIGURATIONS

DIP



PLCC



ORDERING GUIDE

Model	Package Option*	Temperature
AD557JN	Plastic (N-16)	0 to +70°C
AD557JP	PLCC (P-20A)	0 to +70°C

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

NOTES

[1]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error" on AD558 data sheet.

[2]Passive pull-down resistance is 2kΩ.

[3]Settling time is specified for a positive-going full-scale step to ± 1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[4]The full-scale output voltage is 2.55V and is guaranteed with a + 5V supply.

[5]A monotonic converter has a maximum differential linearity error of ± 1LSB.

[6]See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
N/P (Plastic) Packages . . . . . 140/55°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CIRCUIT DESCRIPTION

The AD557 consists of four major functional blocks fabricated on a single monolithic chip (see Figure 1). The main D/A converter section uses eight equally weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

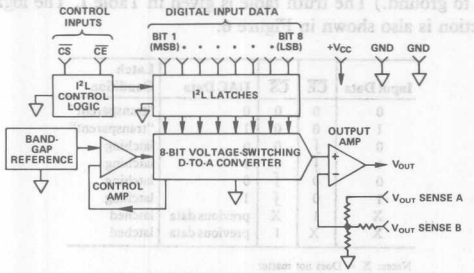


Figure 1. Functional Block Diagram

The high-speed output buffer amplifier is operated in the noninverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin film laser trimmed to match and track the DAC resistors and to assure precise initial calibration of the output range, 0V to 2.56V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2V and thus, unlike 6.3V temperature-compensated zeners, may be operated from a single, low-voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low power, small geometry and high speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a µP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

Digital Input Code			Output
Binary	Hexadecimal	Decimal	Voltage
0000 0000	00	0	0
0000 0001	01	1	0.010V
0000 0010	02	2	0.020V
0000 1111	0F	15	0.150V
0001 0000	10	16	0.160V
0111 1111	7F	127	1.270V
1000 0000	80	128	1.280V
1100 0000	C0	192	1.920V
1111 1111	FF	255	2.55V

CONNECTING THE AD557

The AD557 has been configured for low cost and ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision to be made by the user is whether the output range desired is unipolar or bipolar. Clean circuit board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

UNIPOLAR 0 TO +2.56V OUTPUT RANGE

Figure 2 shows the configuration for the 0 to +2.56V full-scale output range. Because of its precise factory calibration, the AD557 is intended to be operated without user trims for gain and offset; therefore, no provisions have been made for such user trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range. Note that decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.

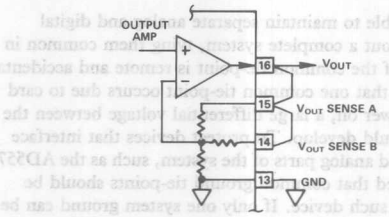


Figure 2. 0 to 2.56V Output Range

BIPOLAR −1.28V TO +1.28V OUTPUT RANGE

The AD557 was designed for operation from a single power supply and is thus capable of providing only a unipolar 0 to +2.56V output range. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 3 shows how a ±1.28V output range may be achieved when a −5V power supply is available. The offset is provided by the AD589 precision 1.2V reference which will operate from a +5V supply. The AD711 output amplifier can provide the necessary ±1.28V output swing from ±5V supplies. Coding is complementary offset binary.

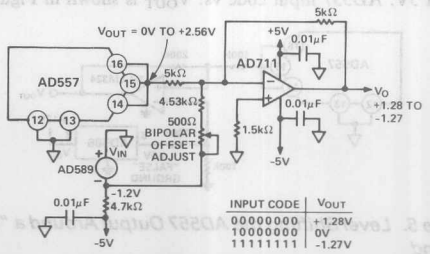


Figure 3. Bipolar Operation of AD557 from ±5V Supplies

GROUNDING AND BYPASSING

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD557 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD557 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 4 shows how the ground connections should be made.

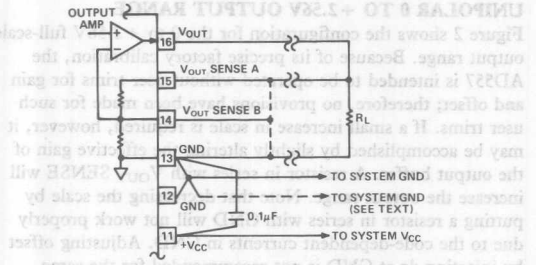


Figure 4. Recommended Grounding and Bypassing

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD557, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD557, it is recommended that analog common be selected.

USING A "FALSE" GROUND

Many applications, such as disk drives, require servo control voltages that swing on either side of a "false" ground. This ground is usually created by dividing the +12V supply equally and calling the midpoint voltage "ground."

Figure 5 shows an easy and inexpensive way to implement this. The AD586 is used to provide a stable 5V reference from the system's +12V supply. The op amp shown likewise operates from a single (+12V) supply available in the system. The resulting output at the V_{OUT} node is ±2.5V around the "false" ground point of 5V. AD557 input code vs. V_{OUT} is shown in Figure 6.

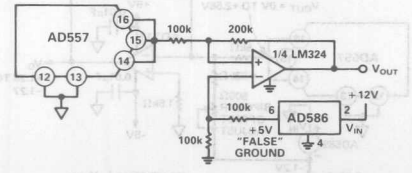


Figure 5. Level Shifting the AD557 Output Around a "False" Ground

TIMING AND CONTROL

The AD557 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1," the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0." (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	∫	0	0	latching
1	∫	0	1	latching
0	0	∫	0	latching
1	0	∫	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
∫ = Logic Threshold at Positive-Going Transition

Table I. AD557 Control Logic Truth Table

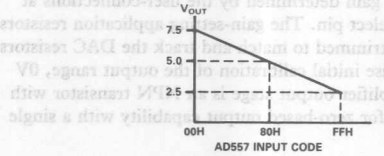


Figure 6. AD557 Input Code vs. Level Shifted Output in "False" Ground Configuration

In a level-triggered latch such as that used in the AD557, there is an interaction between the data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD557 is tested with $T_{DS} = T_W = 225ns$ at 25°C and 300ns at T_{min} and T_{max}, with $T_{DH} = 10ns$ at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals, $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

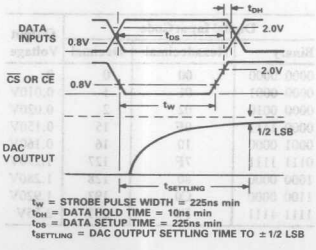


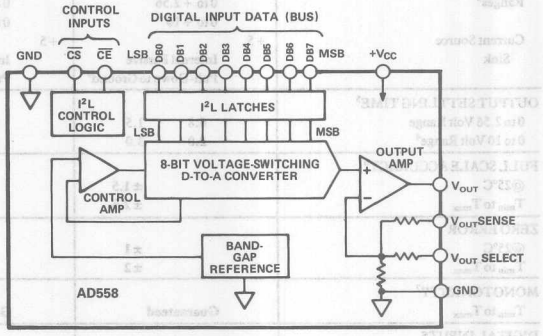
Figure 7. AD557 Timing

DACPORT
Low Cost, Complete μP-Compatible 8-Bit DAC
AD558

FEATURES

- Complete 8-Bit DAC
- Voltage Output — 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1μs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP and 20-Pin PLCC Packages
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD558 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for −55°C to +125°C operation. The "J" and "K" grades are available either in 16-pin plastic (N) or hermetic ceramic (D) DIPS. They are also available in 20-pin JEDEC standard PLCC packages. The "S" and "T" grades are available in the 16-pin hermetic ceramic DIP package.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100μA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.
7. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B visual inspection is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.
8. The AD558 is available in versions compliant with MIL-STD-883. Refer to Analog Devices Military Products Databook or current AD588/883B data sheet for detailed specifications.

*Protected by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; Patents Pending.

DACPORT is a trademark of Analog Devices, Inc.

	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION			8			8			8			8	Bits
RELATIVE ACCURACY[2]													
0 to +70°C			±1/2			±1/4			±1/2			±1/4	LSB
−55°C to +125°C									±3/4			±3/8	LSB
OUTPUT													
Ranges[3]		0 to +2.56 0 to +10			0 to +2.56 0 to +10			0 to +2.56 0 to +10			0 to +2.56 0 to +10		V V
Current Source	+5			+5			+5			+5			mA
Sink		Internal Passive Pull-Down to Ground[4]			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground		
OUTPUT SETTLING TIME[5]													
0 to 2.56 Volt Range		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	µs
0 to 10 Volt Range[4]		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	µs
FULL SCALE ACCURACY[6]													
@25°C			±1.5			±0.5			±1.5			±0.5	LSB
T_{min} to T_{max}			±2.5			±1			±2.5			±1	LSB
ZERO ERROR													
@25°C			±1			±1/2			±1			±1/2	LSB
T_{min} to T_{max}			±2			±1			±2			±1	LSB
MONOTONICITY[7]													
T_{min} to T_{max}		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
DIGITAL INPUTS													
T_{min} to T_{max}													
Input Current			±100			±100			±100			100	µA
Data Inputs, Voltage													
Bit On – Logic "1"	2.0			2.0			2.0			2.0			V
Bit On – Logic "0"	0		0.8	0			0			0			V
Control Inputs, Voltage													
On – Logic "1"	2.0			2.0			2.0			2.0			V
On – Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Input Capacitance		4			4			4			4		pF
TIMING[8]													
t_W Strobe Pulse Width	200			200			200			200			ns
T_{min} to T_{max}	270			270			270			270			ns
t_{DH} Data Hold Time	10			10			10			10			ns
T_{min} to T_{max}	10			10			10			10			ns
t_{DS} Data Set-Up Time	200			200			200			200			ns
T_{min} to T_{max}	270			270			270			270			ns
POWER SUPPLY													
Operating Voltage Range (V_{CC})													
2.56 Volt Range	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	V
10 Volt Range	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	V
Current (I_{CC})		15	25		15	25		15	25		15	25	mA
Rejection Ratio			0.03			0.03			0.03			0.03	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125		75	125		75	125		75	125	mW
V_{CC} = 15V		225	375		225	375		225	375		225	375	mW
OPERATING TEMPERATURE RANGE	0		+70	0		+70	−55		+125	−55		+125	°C

NOTES

[1]The AD558 S & T grades are available processed and screened to MIL-STD-883 Class B. Consult Analog Devices' Military Databook for details.

[2]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error".

[3]Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4]Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5]Settling time is specified for a positive-going full-scale step to ± 1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6]The full range output voltage for the 2.56 range is 2.55V and is guaranteed with a +5V supply, for the 10V range, it is 9.960V guaranteed with a +15V supply.

[7]A monotonic converter has a maximum differential linearity error of ±1LSB.

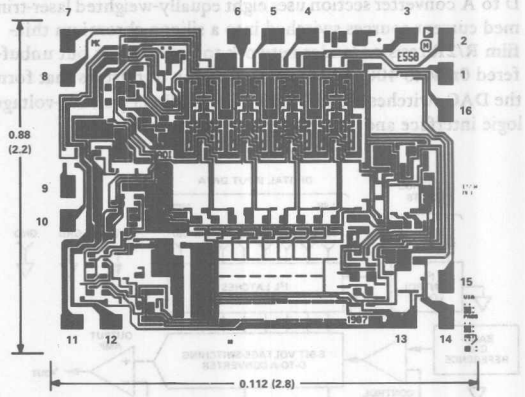
[8]See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0V to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
D (Ceramic) Package . . . . . −55°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
D (Ceramic) Package . . . . . 100/30°C/W
N/P (Plastic) Packages . . . . . 140/55°C/W

Dimensions shown in inches and (mm).



2

ORDERING GUIDE

Model[1]	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full Scale Error, Max T_{min} to T_{max}	Package Option[2]
AD558JN	0 to +70°C	±1/2LSB	±2.5LSB	Plastic (N-16)
AD558JP	0 to +70°C	±1/2LSB	±2.5LSB	PLCC (P-20A)
AD558JD	0 to +70°C	±1/2LSB	±2.5LSB	TO-116 (D-16)
AD558KN	0 to +70°C	±1/4LSB	±1LSB	Plastic (N-16)
AD558KP	0 to +70°C	±1/4LSB	±1LSB	PLCC (P-20A)
AD558KD	0 to +70°C	±1/4LSB	±1LSB	TO-116 (D-16)
AD558SD	−55°C to +125°C	±3/4LSB	±2.5LSB	TO-116 (D-16)
AD558TD	−55°C to +125°C	±3/8LSB	±1LSB	TO-116 (D-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices' Military Products Databook or current AD558/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

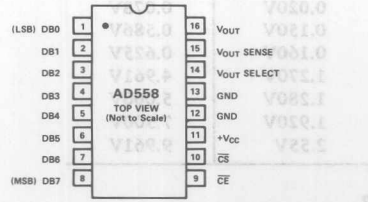


Figure 1a. AD558 Pin Configuration (DIP)

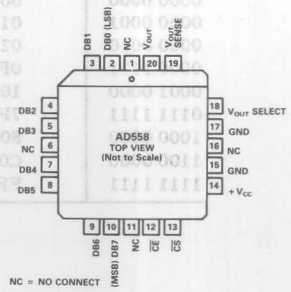


Figure 1b. AD558 Pin Configuration (PLCC)

CIRCUIT DESCRIPTION

The AD558 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 2). The main D to A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

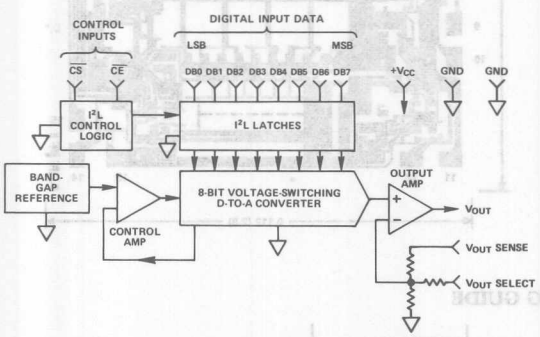


Figure 2. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD558, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, military-temperature range AD558 grades S and T are available screened to MIL-STD-883. For more complete data sheet information consult the Analog Devices' Military Databook.

CHIP AVAILABILITY

The AD558 is available in laser-trimmed, passivated chip form. AD558J and AD558T chips are available. Consult the factory for details.

Digital Input Code			Output Voltage	
Binary	Hexadecimal	Decimal	2.56V Range	10.00V Range
0000 0000	00	0	0	0
0000 0001	01	1	0.010V	0.039V
0000 0010	02	2	0.020V	0.078V
0000 1111	0F	15	0.150V	0.586V
0001 0000	10	16	0.160V	0.625V
0111 1111	7F	127	1.270V	4.961V
1000 0000	80	128	1.280V	5.000V
1100 0000	C0	192	1.920V	7.500V
1111 1111	FF	255	2.55V	9.961V

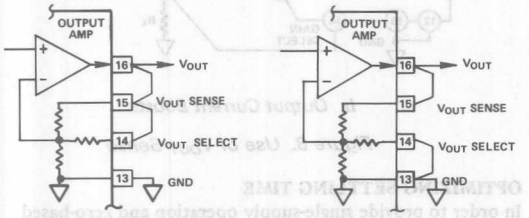
Input Logic Coding

CONNECTING THE AD558

The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit-board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 3 shows the two alternative output range connections. The 0V to 2.56V range may be selected for use with any power supply between +4.5V and +16.5V. The 0V to 10V range requires a power supply of +11.4V to +16.5V.

Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user-trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range.



a. 0V to 2.56V Output Range b. 0V to 10V Output Range

Figure 3. Connection Diagrams

For example if a 0V to 10.24V output range is desired (40mV = 1LSB), a nominal resistance of 850Ω is required. It must be remembered that, although the internal resistors all ratio-match and track, the *absolute* tolerance of these resistors is typically ±20% and the *absolute* TC is typically -50ppm/°C (0 to -100ppm/°C). That must be considered when re-scaling is performed. Figure 4 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.

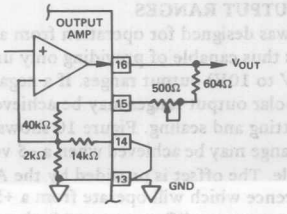


Figure 4. 10.24V Full-Scale Connection

GROUNDING AND BYPASSING*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 5 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

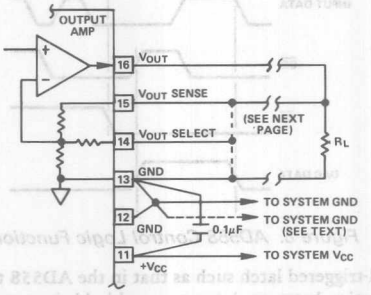


Figure 5. Recommended Grounding and Bypassing

POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5V and +16.5V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0V to 10V output range, the power supply voltage must be between +11.4V and +16.5V. If, however, the 0V to 2.56V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5V).

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers

*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A Change", is available at no charge from any Analog Devices Sales Office.

$\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↓	0	0	latching
1	↓	0	1	latching
0	0	↓	0	latching
1	0	↓	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
↓ = Logic Threshold at Positive-Going Transition

Table I. AD558 Control Logic Truth Table

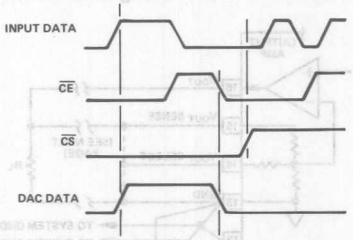


Figure 6. AD558 Control Logic Function

In a level-triggered latch such as that in the AD558 there is an interaction between data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD558 is tested with $t_{DS} = t_W = 200ns$ at 25°C and 270ns at T_{min} and T_{max}, with $t_{DH} = 10ns$ at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

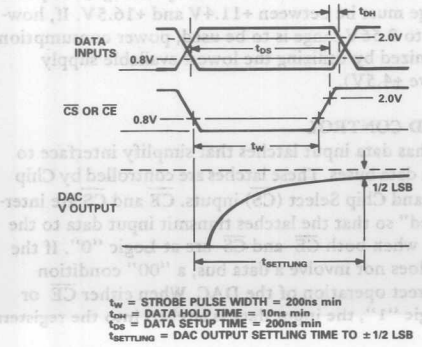
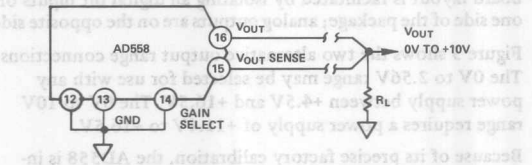


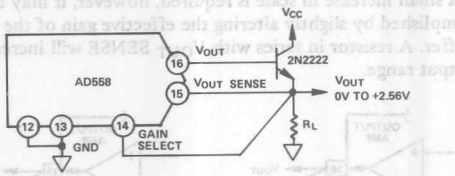
Figure 7. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 8a shows how I×R drops in long lines to remote loads may be cancelled by putting the drops "inside the loop." Figure 8b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for I x R Drops in Output Lines



b. Output Current Booster

Figure 8. Use of V_{OUT} Sense

OPTIMIZING SETTLING TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive "pull-down" to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 9. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5mA max.

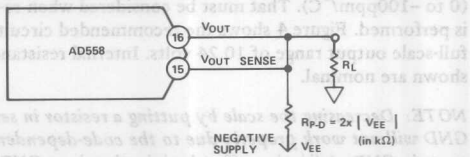


Figure 9. Improved Settling Time

BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0V to +2.56 and 0V to 10V) output ranges. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 10 shows how a ±1.28 volt output range may be achieved when a –5 volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a +5 volt supply. The AD544 output amplifier can provide the necessary ±1.28 volt output swing from ±5 volt supplies. Coding is complementary offset binary.

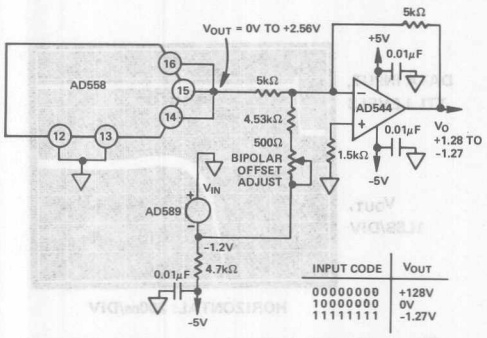


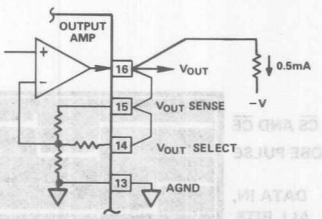
Figure 10. Bipolar Operation of AD558 from ±5V Supplies

MEASURING OFFSET ERROR

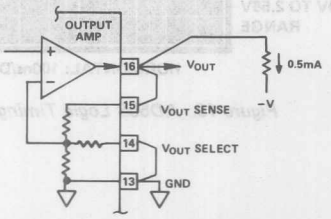
One of the most commonly specified end-point errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volts. There are some DACs, like the AD558 where offset errors may be present but not observable at the zero scale, because of other circuit limitations (such as zero coinciding with single-supply ground) so that a nonzero output at zero code cannot be read as the offset error. Factors like this make testing the AD558 a little more complicated.

By adding a pulldown resistor from the output to a negative supply as shown in Figure 11, we can now readoffset errors at zero code that may not have been observable due to circuit limitations. The value of the resistor should be such that, at zero voltage out, current through the resistor is 0.5mA max.



a. 0V to 2.56V Output Range

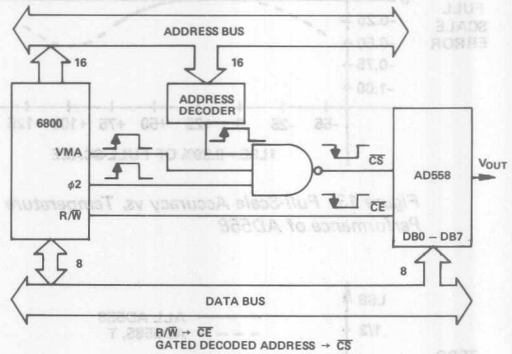


b. 0V to 10V Output Range

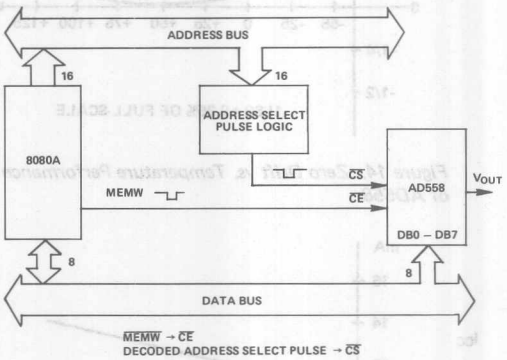
Figure 11. Offset Connection Diagrams

INTERFACING THE AD558 TO MICROPROCESSOR DATA BUSES

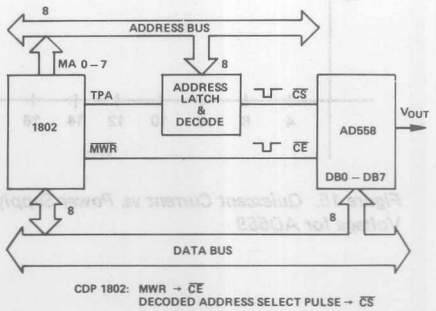
The AD558 is configured to act like a "write only" location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 12 shows interfaces for three popular microprocessor systems.



a. 6800/AD558 Interface



b. 8080A/AD558 Interface



c. 1802/AD558 Interface

Figure 12. Interfacing the AD558 to Microprocessors

AD558—Performance (typical @ +25°C, V_{CC} = +5V to +15V unless otherwise noted)

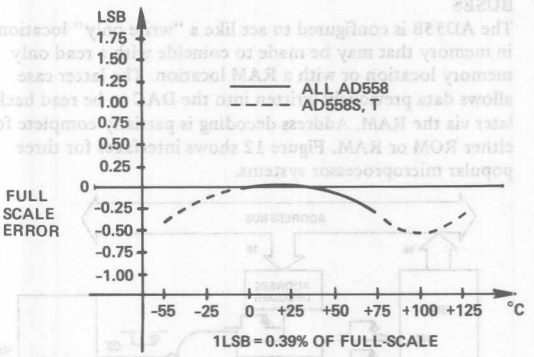


Figure 13. Full-Scale Accuracy vs. Temperature Performance of AD558

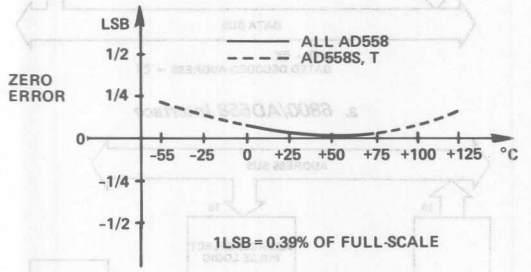


Figure 14. Zero Drift vs. Temperature Performance of AD558

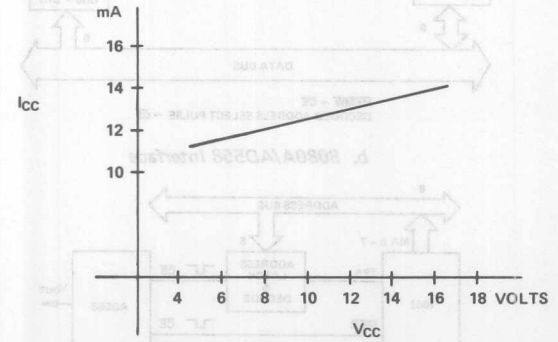


Figure 15. Quiescent Current vs. Power Supply Voltage for AD558

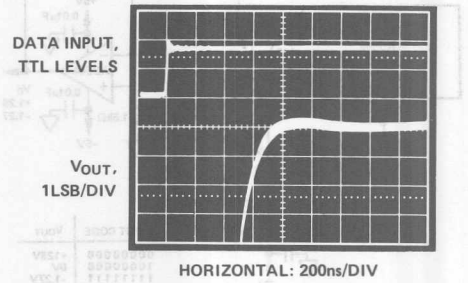


Figure 16. AD558 Settling Characteristic Detail 0V to 2.56V Output Range Full-Scale Step

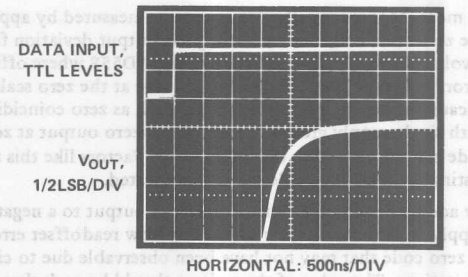


Figure 17. AD558 Settling Characteristic Detail 0V to 10V Output Range Full-Scale Step

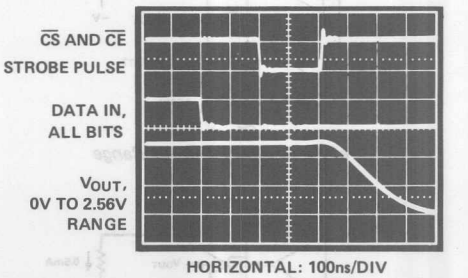


Figure 18. AD558 Logic Timing

Low Cost 10-Bit Monolithic D/A Converter

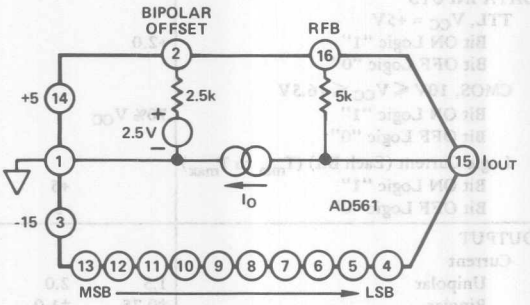
AD561*

FEATURES

- Complete Current Output Converter
- High Stability Buried Zener Reference
- Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
- Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
- Fast Settling – 250ns to 1/2LSB
- Guaranteed Monotonicity Over Full Operating Temperature Range
- TTL/DTL and CMOS Compatible (Positive True Logic)
- Single Chip Monolithic Construction
- Available in Chip Form
- MIL-STD-883-Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM

TO-116



PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

The AD561 is available in four performance grades. The AD561J and K are specified for use over the 0 to +70°C temperature range and are available in either a 16-pin hermetically-sealed ceramic DIP or a 16-pin molded plastic DIP. The AD561S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.
5. The AD561 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD561/883B data sheet for detailed specifications.

*Protected by Patent Nos.: 3,940,760; 3,747,088; RE 28,633; 3,803,590; RE 29,619; 3,961,326; 4,141,004; 4,213,806; 4,136,349.

MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage ("D" Package)		-65 to +150			*	*	°C
("N" Package)		-25 to +85			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES		0 to +10 -5 to +5			* *		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			*		% of F.S.

NOTES
*Specifications same as AD561J specs.
Specifications subject to change without notice.

RESOLUTION		10 Bits			10 Bits	
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES		0 to +10 -5 to +5			** **		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			**		% of F.S.

NOTES
**Specifications same as AD561S specs.
Specifications subject to change without notice.

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 1. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

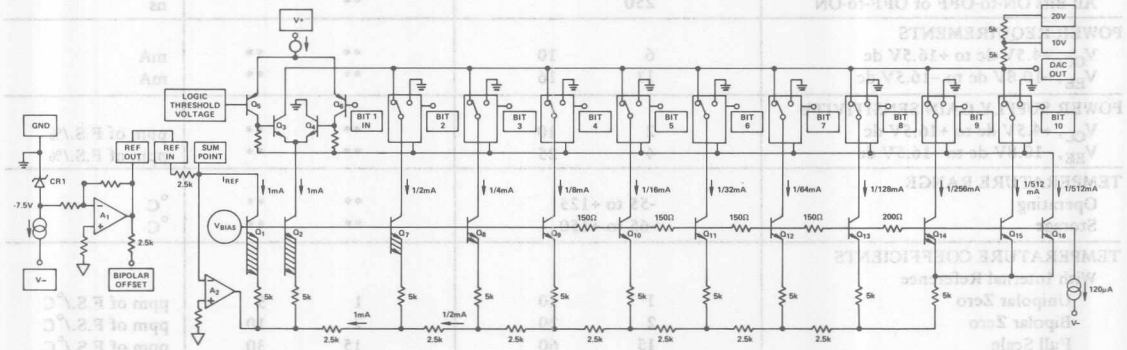


Figure 1. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PIN CONFIGURATION
TOP VIEW

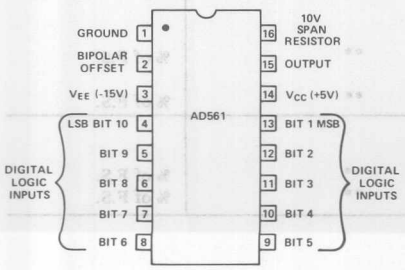


Figure 2.

ORDERING GUIDE

MODEL[1]	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTION[2]
AD561JD	0 to +70°C	±½LSB max	80ppm max	D-16
AD561JN	0 to +70°C	±½LSB max	80ppm max	N-16
AD561KD	0 to +70°C	±¼LSB max	30ppm max	D-16
AD561KN	0 to +70°C	±¼LSB max	30ppm max	N-16
AD561SD	-55 to +125°C	±½LSB max	60ppm max	D-16
AD561TD	-55 to +125°C	±¼LSB max	30ppm max	D-16
AD561/883B	-55 to +125°C	*	*	*

NOTES
[1] For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD561/883B data sheet.
[2] D = Ceramic DIP; N = Plastic DIP. For outline information see Package Information section.
*Refer to AD561/883B military data sheet.

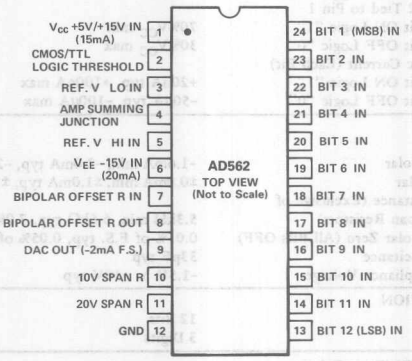
IC 12-Bit D/A Converters

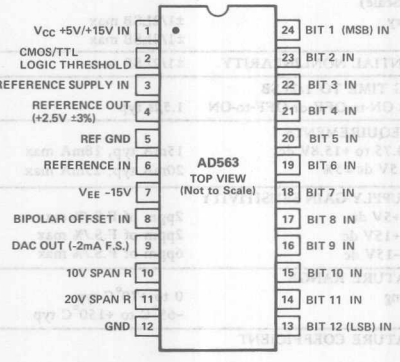
AD562/AD563*

FEATURES

True 12-Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24-Pin DIP
TTL/DTL and CMOS Compatibility
Positive True Logic
MIL-STD-883-Compliant Versions Available

PIN CONFIGURATIONS





PRODUCT DESCRIPTION

The AD562/AD563 are monolithic 12-bit digital-to-analog converters consisting of especially designed precision bipolar switches and control amplifiers and compatible high stability silicon chromium thin film resistors. The AD563 also includes its own internal voltage reference.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12-bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

The AD562 and AD563 are recommended for high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the extended temperature range, −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD562 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, the AD563 is recommended with its internal low drift voltage reference.
2. True 12-bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563s internally provided feedback resistors.
3. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.
4. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (< ±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.
5. TTL or CMOS inputs can be accommodated for supply voltages from +5V to +15V.
6. Positive true logic eliminates the need for additional inverter components.
7. The AD562 and AD563 are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

***Covered by Patent Nos. 3,961,326; 4,141,004; 3,747,088; RE 28,633; 3,803,590; 4,020,486; the AD563 is also covered by 4,213,806; 4,136,349.**

MODEL	AD562KD/BIN AD562KD/BCD	AD562AD/BIN AD562AD/BCD	AD562SD/BIN AD562SD/BCD
DATA INPUTS (positive True, Binary (BCD) and Offset Binary (BCD))			
TTL, V_{CC} = +5V, Pin 2 Open Circuit			
Bit ON Logic "1"	+2.0V	*	*
Bit OFF Logic "0"	+0.8V max	*	*
CMOS, 4.75 ≤ V_{CC} ≤ 15.8, Pin 2 Tied to Pin 1			
Bit ON Logic "1"	70%V_{CC} min	*	*
Bit OFF Logic "0"	30%V_{CC} max	*	*
Logic Current (Each Bit)			
Bit ON Logic "1"	+20nA typ, +100nA max	*	*
Bit OFF Logic "0"	−50μA typ, −100μA max	*	*
OUTPUT			
Current			
Unipolar	−1.6mA min, −2.0mA typ, −2.4mA max	*	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*	*
Resistance (Exclusive of Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*	*
Capacitance	33pF typ	*	*
Compliance Voltage	−1.5V to +10V typ	*	*
RESOLUTION			
Binary	12 Bits	*	*
BCD	3 Digits	*	*
ACCURACY (Error Relative to Full Scale)			
Binary	±1/2LSB max	*	±1/4LSB max
BCD	±1/2LSB max	*	±1/10LSB max
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*	*
SETTLING TIME TO 1/2LSB			
All Bits ON-to-OFF or OFF-to-ON	1.5μs typ	*	*
POWER REQUIREMENTS			
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*	*
V_{EE}, −15V dc ±5%	20mA typ, 25mA max	*	*
POWER SUPPLY GAIN SENSITIVITY			
V_{CC} @ +5V dc	2ppm of F.S./% max	*	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*	*
V_{EE} @ −15V dc	6ppm of F.S./% max	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C typ	−25°C to +85°C	−55°C to +125°C
Storage	−65°C to +150°C typ	*	*
TEMPERATURE COEFFICIENT			
Unipolar Zero	2ppm of F.S./°C max	*	*
Bipolar Zero	4ppm of F.S./°C max	*	*
Gain	5ppm of F.S./°C max	*	*
Differential Nonlinearity	2ppm of F.S./°C	*	1ppm of F.S./°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range	*	*
EXTERNAL ADJUSTMENTS[1]			
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*	*
Bipolar Zero Error with Fixed 50Ω Resistor	±0.1% of F.S. typ	*	*
Gain Adjustment Range	±0.25% of F.S. typ	*	*
Binary Bipolar Zero Adjustments Range	±0.25% of F.S. typ	*	*
BCD Bipolar Offset Adjustment Range	±0.17% of F.S. typ	*	*
PROGRAMMABLE OUTPUT RANGES	0 to +5V typ	*	*
	−2.5V to +2.5V typ	*	*
	0V to +10V typ	*	*
	−5V to +5V typ	*	*
	−10V to +10V typ	*	*
REFERENCE INPUT			
Input Impedance	20kΩ typ	*	*

*Specifications same as AD562KD. **Specifications same as AD563KD. ***Specifications same as AD563JD. [1]Device calibrated with internal reference.
Specifications subject to change without notice.

AD563JD/BIN AD563JD/BCD	AD563KD/BIN AD563KD/BCD	AD563SD/BIN AD563SD/BCD	AD563TD/BIN AD563TD/BCD
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	±1/4LSB	••	••
•	±1/4LSB	••	••
•	•	•	•
•	•	•	•
15mA typ, 20mA max	•••	•••	•••
•	•	•	•
3ppm of F.S./% typ, 10ppm of F.S./% max	•••	•••	•••
3ppm of F.S./% typ, 10ppm of F.S./% max	•••	•••	•••
14ppm of F.S./% typ, 25ppm of F.S./% max	•••	•••	•••
•	•	–55°C to +125°C	–55°C to +125°C
•	•	•	•
With Internal Reference			
1ppm of F.S./°C typ, 2ppm of F.S./°C max	•••	•••	•••
10ppm of F.S./°C max	•••	•••	•••
50ppm of F.S./°C max	20ppm of F.S./°C max	30ppm of F.S./°C max	10ppm of F.S./°C max
•	•	•	•
•	•	•	•
With Fixed 10Ω Resistor			
±0.2% of F.S. typ	•••	•••	•••
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
5kΩ typ	•••	•••	•••

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S. The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD563 are 100% tested to be monotonic over the full operating temperature range.

UNIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For +10V F.S., connect the external operational amplifier output to Pin 10 and leave Pin 11 unconnected. For +5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . ZERO ADJUST

Turn all bits OFF and adjust R_1 until op amp output is 0 volts.

STEP III . . . GAIN ADJUST

Turn all bits ON for binary DAC's (bits 1, 4, 5, 8, 9 and 12 ON for BCD DAC's). Adjust R_2 until op amp output is:

BINARY	BCD
4.9988V for +5V Range	4.9950 for +5V Range
9.9976 for +10V Range	9.9900 for +10V Range

BIPOLAR DAC's

Figure 1b is a typical connection scheme for the AD563 used in bipolar operation.

STEP I . . . OUTPUT RANGE

Determine the output range required. For ±10V F.S., connect the external op amp output to Pin 11 and leave Pin 10 unconnected. For ±5V F.S., connect the external op amp output to Pin 10 and leave Pin 11 unconnected. For ±2.5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . OFFSET ADJUST

Turn all bits OFF and adjust R_3 until op amp output is:

−2.5000V for ±2.5V Range
−5.0000V for ±5V Range
−10.0000V for ±10V Range

STEP III . . . GAIN ADJUST (Bipolar Zero)

Turn bit 1 ON for Binary DAC's (bits 2 and 4 ON for BCD DAC's). Adjust R_2 until op amp output is 0 volts.

ORDERING GUIDE

MODEL[1]	INPUT CODE	TEMP. RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTION[2]
AD562KD/BIN	Binary	0 to +70°C	±1/2LSB max	5ppm max	D-24A
AD562KD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	5ppm max	D-24A
AD562AD/BIN	Binary	−25°C to +85°C	±1/2LSBmax	5ppm max	D-24A
AD562AD/BCD	Binary Coded Decimal	−25°C to +85°C	±1/2LSB max	5ppm max	D-24A
AD562SD/BIN	Binary	−55°C to +125°C	±1/4LSB max	5ppm max	D-24A
AD562SD/BCD	Binary Coded Decimal	−55°C to +125°C	±1/10LSB max	5ppm max	D-24A
AD563JD/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	D-24A
AD563JD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	D-24A
AD563KD/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	D-24A
AD563KD/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	D-24A
AD563SD/BIN	Binary	−55°C to +125°C	±1/4LSB max	30ppm max	D-24A
AD563SD/BCD	Binary Coded Decimal	−55°C to +125°C	±1/4LSB max	30ppm max	D-24A
AD563TD/BIN	Binary	−55°C to +125°C	±1/4LSB max	10ppm max	D-24A
AD563TD/BCD	Binary Coded Decimal	−55°C to +125°C	±1/4LSB max	10ppm max	D-24A

NOTES
[1] For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current /883B data sheet.
[2] D = Ceramic DIP. For outline information see Package Information section.

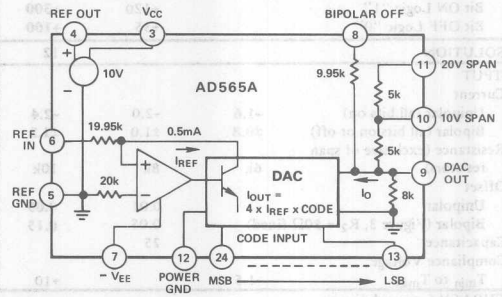
High Speed 12-Bit Monolithic D/A Converters

AD565A*/AD566A*

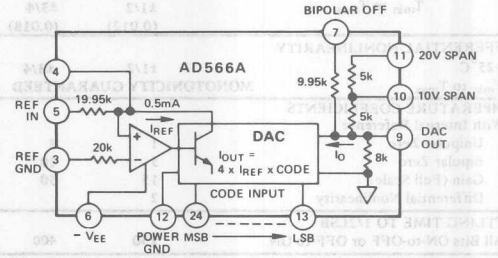
FEATURES

- Single Chip Construction
- Very High-Speed Settling to 1/2LSB
  - AD565A: 250ns max
  - AD566A: 350ns max
- Full-Scale Switching Time: 30ns
- Guaranteed for Operation with ±12V Supplies: AD565A with -12V Supply: AD566A
- Linearity Guaranteed Over Temperature: 1/2LSB max (K, T Grades)
- Monotonicity Guaranteed Over Temperature
- Low Power: AD566A = 180mW max; AD565A = 225mW max
- Use with On-Board High-Stability Reference (AD565A) or with External Reference (AD566A)
- Low Cost
- MIL-STD-883-Compliant Versions Available

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10-90% full-scale transition time less than 35ns and settle to within ±1/2LSB in 250ns max (350ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

***Covered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349; 4,020,486; 3,747,088.**

AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0 to +70°C temperature range while the S and T grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
4. The AD565A and AD566A are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

AD565A—SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = −15V, unless otherwise specified.)

MODEL	AD565AJ MIN	AD565AJ TYP	AD565AJ MAX	AD565AK MIN	AD565AK TYP	AD565AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

MODEL	AD565AS MIN	AD565AS TYP	AD565AS MAX	AD565AT MIN	AD565AT TYP	AD565AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGES (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω							
Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**		
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

NOTES

[1] The digital input levels are guaranteed but not tested over the temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{EE} of −15V dc.

Specifications subject to change without notice.

TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%-90%	5mA/μs
90%-10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

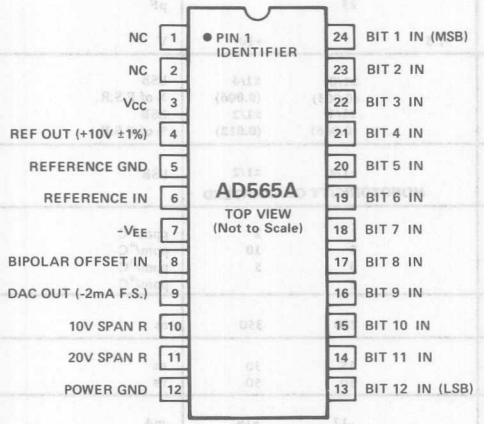
Specifications subject to change without notice.

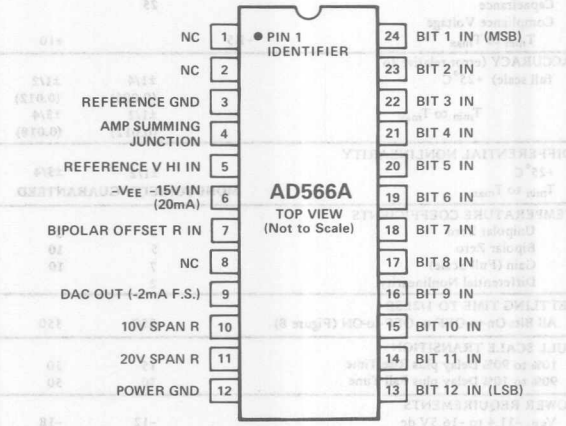
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground (AD565A) . . . . . 0V to −18V
Voltage on DAC Output (Pin 9) . . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to
Power Ground . . . . . −1.0V to +7.0V
Ref in to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref out (AD565A) . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

PIN DESIGNATIONS





AD565A ORDERING GUIDE

Model[1]	Max Gain T.C. (ppm of F.S./°C)	Temperature Range	Linearity Error Max @ +25°C	Package Option[2]
AD565AJD	50	0 to +70°C	± 1/2LSB	Ceramic (D-24)
AD565AKD	20	0 to +70°C	± 1/4LSB	Ceramic (D-24)
AD565ASD	30	−55°C to +125°C	± 1/2LSB	Ceramic (D-24)
AD565ATD	15	−55°C to +125°C	± 1/4LSB	Ceramic (D-24)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current /883B data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

AD566A ORDERING GUIDE

Model[1]	Max Gain T.C. (ppm or F.S./°C)	Temperature Range	Linearity Error Max @ +25°C	Package Option[2]
AD566AJD	10	0 to +70°C	± 1/2LSB	Ceramic (D-24)
AD566AKD	3	0 to +70°C	± 1/4LSB	Ceramic (D-24)
AD566ASD	10	−55°C to +125°C	± 1/2LSB	Ceramic (D-24)
AD566ATD	3	−55°C to +125°C	± 1/4LSB	Ceramic (D-24)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current /883B data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

GROUNDING RULES

The AD565A and AD566A bring out separate reference and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

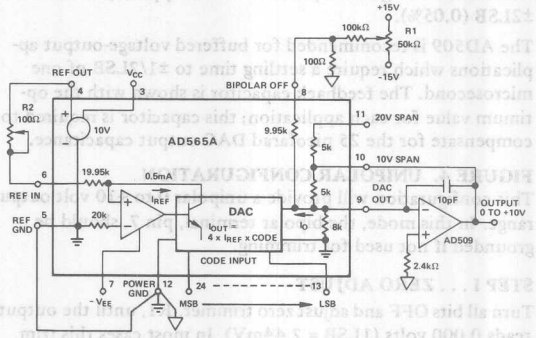


Figure 1. 0 to +10V Unipolar Voltage Output

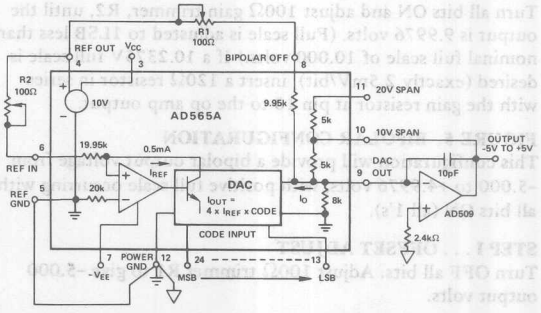


Figure 2. ±5V Bipolar Voltage Output

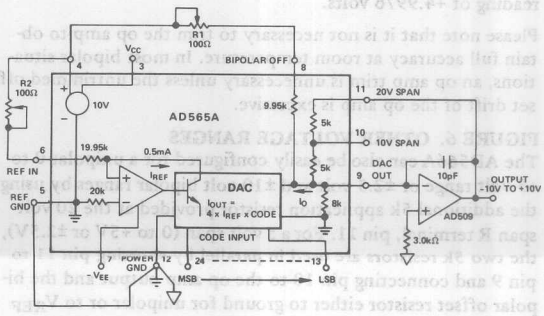


Figure 3. ±10V Voltage Output

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000		Zero	−Full Scale	Zero
011111111111		Mid Scale −1LSB	Zero −1LSB	+FS −1LSB
100000000000		+1/2 FS	Zero	−FS
111111111111		+FS −1LSB	+ Full Scale −1LSB	Zero −1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table I. Digital Input Codes

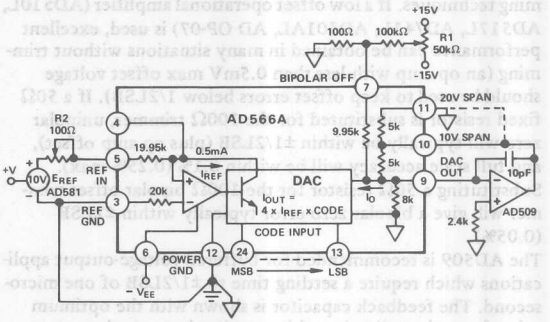


Figure 4. 0 to +10V Unipolar Voltage Output

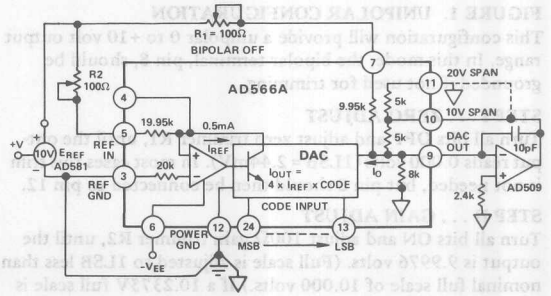
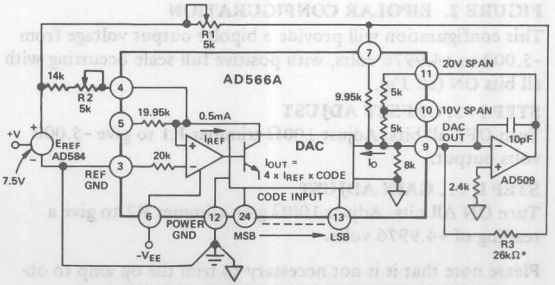


Figure 5. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 6. ±10V Voltage Output

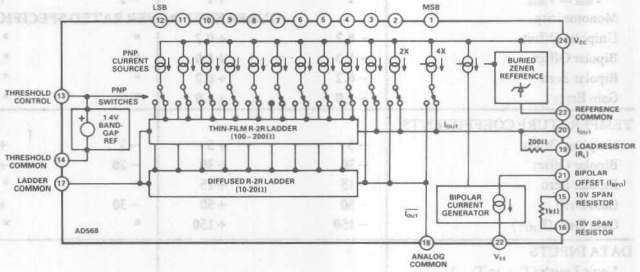
12-Bit Ultrahigh Speed Monolithic D/A Converter

AD568

FEATURES

- Ultrahigh Speed: Current Settling to 1LSB in 35ns
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- 10.24mA Full-Scale Output Suitable for Video Applications
- Integral and Differential Linearity Guaranteed Over Temperature
- 0.3" "Skinny DIP" Packaging
- Variable Threshold Allows TTL and CMOS Interface
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ± 1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.
6. The AD568 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD568/883B data sheet for detailed specifications.

AD568—SPECIFICATIONS (@ = +25°C, V_{CC}, V_{EE} = ±15V unless otherwise noted.)

Model	AD568J Min	AD568J Typ	AD568J Max	AD568K Min	AD568K Typ	AD568K Max	AD568S Min	AD568S Typ	AD568S Max	Units
RESOLUTION	12			12			12			Bits
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	−1/2		+1/2	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	−3/4		+3/4	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	−1		+1	LSB
T_{min} to T_{max}	−1		+1	−1		+1	−1		−1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	*		*	*		*	% of FSR
Bipolar Zero	−0.2		+0.2	*		*	*		*	% of FSR
Gain Error	−1.0		+1.0	*		*	*		*	% ofFSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−5		+5	−3		+3	−5		+5	ppm of FSR/°C
Bipolar Offset	−30		+30	−20		+20	−30		+30	ppm of FSR/°C
Bipolar Zero	−15		+15	*		*	*		*	ppm of FSR/°C
Gain Drift	−50		+50	−30		+30	−50		+50	ppm of FSR/°C
Gain Drift (I_{OUT})	−150		+150	*		*	*		*	ppm of FSR/°C
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10	0	+10	*	*	*	*	*	*	µA
I_{IL}	−0.5	−60	−100	*	*	*	*	−100	−200	µA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ±5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ±0.512									V
COMPLIANCE VOLTAGE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240		*			*		Ω
Inclusive of R_L	99	100	101		*			*		Ω
SETTLING TIME										
Current to										
±0.025%		35			*			*		ns to 0.025% of FSR
±0.1%		23			*			*		ns to 0.1% of FSR
Voltage										
50Ω Load[3], 0.512V p-p,										
to 0.025%		37			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		18			*			*		ns to 1% of FSR
75Ω Load[3], 0.768V p-p,										
to 0.025%		40			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		20			*			*		ns to 1% of FSR
100Ω (Internal R_L)[3], 1.024V p-p,										
to 0.025%		50			*			*		ns to 0.025% of FSR
to 0.1%		38			*			*		ns to 0.1% of FSR
to 1%		24			*			*		ns to 1% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		15			*			*		% of FSR
FULL-SCALE TRANSITION[5]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+13.5V to +16.5V		27	32		*	*		*	*	mA
−13.5V to −16.5V		−7	−8		*	*		*	*	mA
Power Dissipation		525	625		*	*		*	*	mW
PSRR			0.05			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2]	0		70	0		70	−55		+125	°C
Storage	−65		+150	*		*	*		*	°C

NOTES
*Same as AD568J.
[1]Measured in I_{OUT} mode.
[2]Measured in V_{OUT} mode, unless otherwise specified. See text for further information.
[3]Total Resistance. Refer to Figure 3.
[4]At the major carry, driven by HCMOS logic. See text for further explanation.
[5]Measured in V_{OUT} mode.
Specifications shown in boldface are tested on all production units at final electrical test.
Specifications subject to change without notice.

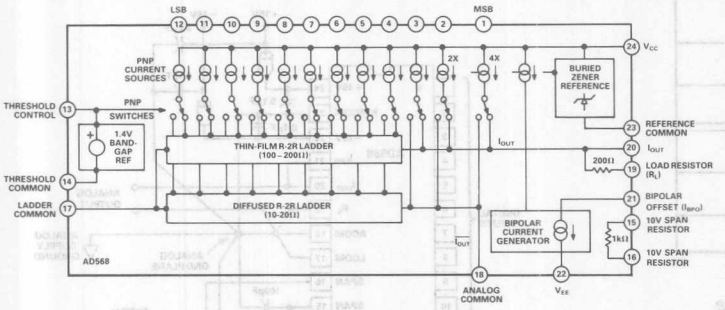
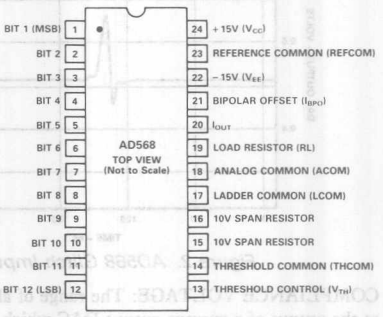


Figure 1. Functional Block Diagram

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM	0V to +18V
V_{EE} to REFCOM	0V to −18V
REFCOM to LCOM	+100mV to −10V
ACOM to LCOM	±100mV
THCOM to LCOM	±500mV
SPANs to LCOM	±12V
I_{BPO} to LCOM	±5V
I_{OUT} to LCOM	−5V to V_{TH}
Digital Inputs to THCOM	−500mV to +7.0V
Voltage Across Span Resistor	12V
V_{TH} to THCOM	−0.7V to +1.4V
Logic Threshold Control Input Current	5mA
Power Dissipation	1000mW
Storage Temperature Range	
Q (Cerdip) Package	−65°C to +150°C
Junction Temperature	175°C
Thermal Resistance	
θ_{ja}	75°C/W
θ_{jc}	25°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Package Option[2]	Temperature Range °C	Linearity Error Max. @ 25°C	Voltage Gain T.C. Max ppm/°C
AD568JQ	24-Lead Cerdip (Q-24)	0 to +70	±1/2	±50
AD568KQ	24-Lead Cerdip (Q-24)	0 to +70	±1/4	±30
AD568SQ	24-Lead Cerdip (Q-24)	−55 to +125	±1/2	±50

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD568/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

Definitions

LINEARITY ERROR (also called INTEGRAL NON-LINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples of 1LSB. The AD568 is laser trimmed to 1/4LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases.

UNIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the inputs are set to all 0s is called bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0V (or 0mA) for bipolar mode when only the MSB is on (100.....00) is called bipolar zero error.

GAIN ERROR: The difference between the ideal and actual output span of FS −1LSB, expressed in % of FS, or LSB, when all bits are on.

GLITCH IMPULSE: Asymmetrical switching times in a DAC give rise to undesired output transients which are quantified by their glitch impulse. It is specified as the net area of the glitch in nV-sec or pA-sec.

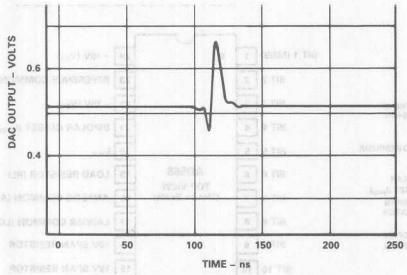


Figure 2. AD568 Glitch Impulse

COMPLIANCE VOLTAGE: The range of allowable voltage at the output of a current-output DAC which will not degrade the accuracy of the output current.

SETTLING TIME: The time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

Connecting the AD568

UNBUFFERED VOLTAGE OUTPUT

Unipolar Configuration

Figure 3 shows the AD568 configured to provide a unipolar 0 to +1.024V output range. In this mode, the bipolar offset terminal, Pin 21, should be grounded if not used for offset trimming.

The nominal output impedance of the AD568 with Pin 19 grounded has been trimmed to 100Ω, ±1%. Other output impedances can be generated with an external resistor, R_{EXT}, between Pins 19 and 20. An R_{EXT} equalling 300Ω will yield a total output resistance of 75Ω, while an R_{EXT} of 100Ω will provide 50Ω of output resistance. Note that since the full-scale output current of the DAC remains 10.24mA, changing the load impedance changes the unbuffered output voltage accordingly. Settling time and full-scale range characteristics for these load impedances are provided in the specifications table.

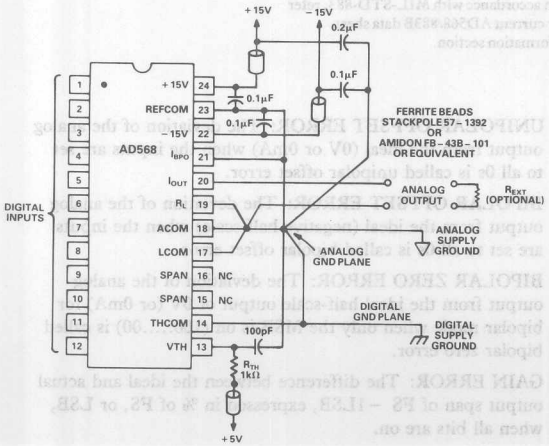


Figure 3. Unipolar Output Unbuffered 0 to +1.024V

Bipolar Configuration

Figure 4 shows the connection scheme used to provide a bipolar

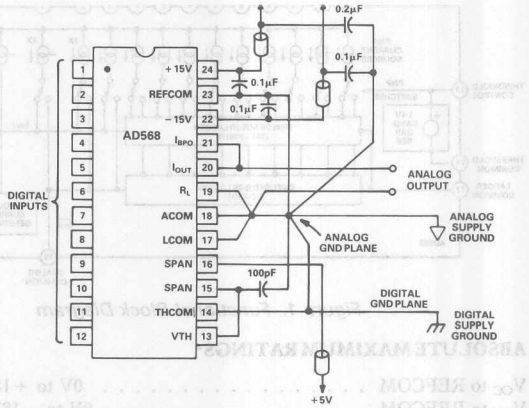


Figure 4. Bipolar Output Unbuffered ±0.512V

occurs when the MSB is ON with all other bits OFF (10 . . . 00), and full-scale minus 1LSB (0.51175V) is generated when all bits are ON (11 . . . 11). Figure 5 shows an optional bipolar mode with a 2.048V range. The scale factor in this mode will not be as accurate as the configuration shown in Figure 4, because the laser-trimmed resistor R_L is not used.

Figure 4 also demonstrates how the internal span resistor may be used to bias the V_{TH} pin (Pin 13) from a 5V supply. This eliminates the requirement for an external R_{TH} in applications that do not require the precision span resistor.

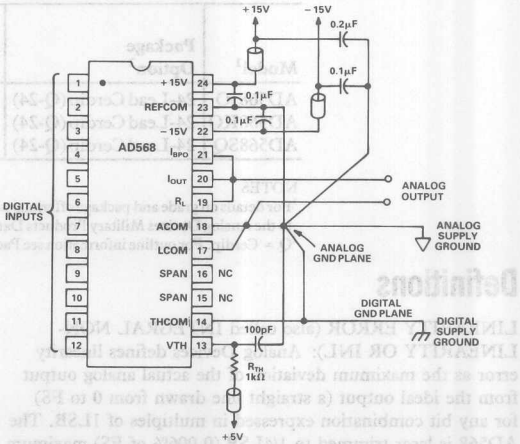


Figure 5. Bipolar Output Unbuffered ±1.024V

Optional Gain and Zero Adjustment

The gain and offset are laser trimmed to minimize their effects on circuit performance. However, in some applications, it may be desirable to externally reduce these errors further. In those cases, the following procedures are suggested.

UNIPOLAR MODE: (Refer to Figure 6)

Step 1 – Set all bits (BIT 1–BIT 12) to Logic "0" (OFF) – note the output voltage. This is the offset error.

Step 2 – Set all bits to Logic "1" (ON). Adjust the gain trim resistor so that the output voltage is equal to the desired full scale minus 1LSB plus the offset error measured in step 1.

trim resistor for 0V output.

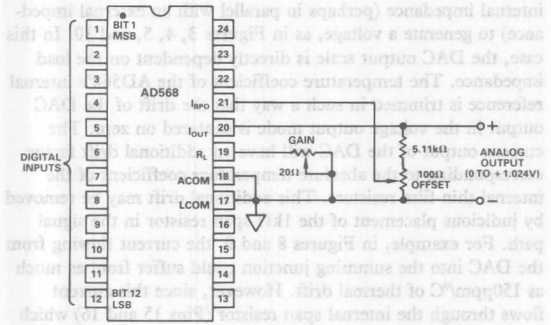


Figure 6. Unbuffered Unipolar Gain and Zero Adjust

BIPOLAR MODE (Refer to Figure 7)

Step 1 – Set bits to offset binary "zero" (10 . . . 00). Adjust the zero resistor to produce 0V at the DAC output. This removes the bipolar zero error.

Step 2 – Set all bits to Logic "1" (ON). Adjust gain trim resistor so the output voltage is equal to the desired full-scale minus 1LSB.

Step 3 – (Optional) If precise trimming of the bipolar offset is preferred to trimming of bipolar zero: set all bits to Logic "0" (OFF). Trim the zero resistor to produce the desired negative full scale at the DAC output.

Note: this may slightly compromise the bipolar zero trim.

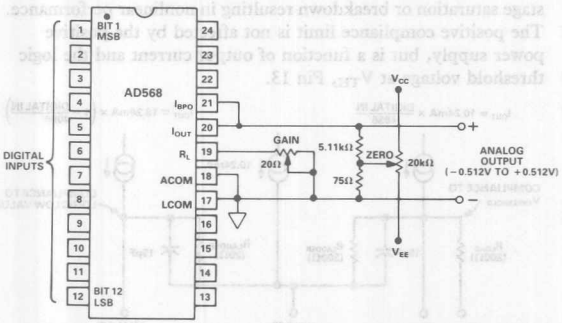


Figure 7. Bipolar Unbuffered Gain and Zero Adjust

BUFFERED VOLTAGE OUTPUT

For full-scale outputs of greater than 1V, some type of external buffer amplifier is required. The AD840 fills this requirement perfectly, settling to 0.025% from a 10V full-scale step in less than 100ns.

A 1kΩ span resistor has been provided on chip for use as a feedback resistor in buffered applications. Using R_{SPAN} (Pins 15, 16) introduces a 100mW code-dependent power source onto the chip which may generate a slight degradation in linearity. Maximum linearity performance can be realized by using an external span resistor.

Unipolar Inverting Configuration

Figure 8 shows the connections for producing a −10.24V full-scale swing. This configuration uses the AD568 in the current output mode into a summing junction at the inverting input terminal of DAC has an output impedance of 100Ω. This produces a noise gain of 11 from the noninverting terminal of the op amp, and hence, satisfies the stability criterion of the AD840 (stable at a gain of 10). The addition of a 5pF compensation capacitor across the 1kΩ feedback resistor produces optimal settling. Lower noise gain can be achieved by connecting R_L to I_{OUT}, increasing the DAC output impedance to approximately 200Ω, and reducing the noise gain to 6 (illustrated in Figure 9). While the output in this configuration will feature improved noise performance, it is somewhat less stable and may suffer from ringing. The compensation capacitance should be increased to 7pF to maintain stability at this reduced gain.

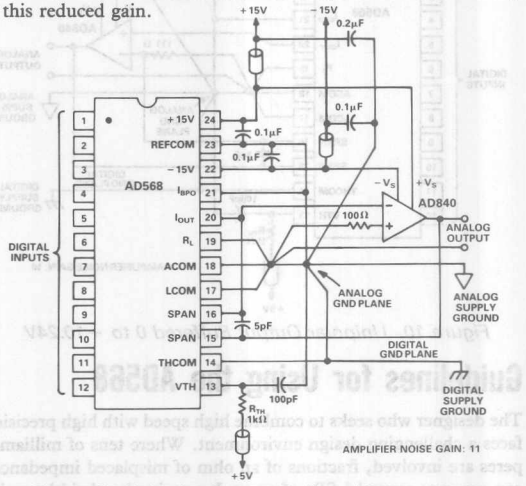


Figure 8. Unipolar Output Buffered 0 to −10.24V

Bipolar Inverting Configuration

Figure 9 illustrates the implementation of a +5.12V to −5.12V bipolar range, achieved by connecting the bipolar offset current, I_{BPO}, to the summing junction of the external amplifier. Note that since the amplifier is providing an inversion, the full-scale output voltage is −5.12V, while the bipolar offset voltage (all bits OFF) is +5.12V at the amplifier output.

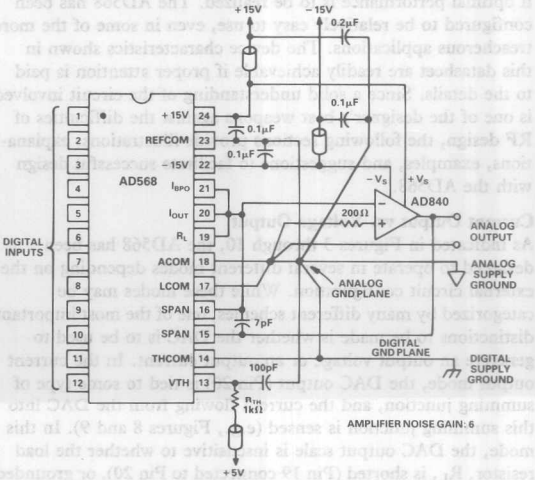


Figure 9. Bipolar Output Buffered ±5.12V

Noninverting Configuration

If a positive full-scale output voltage is required, it can be implemented using the AD568 in the unbuffered voltage output mode followed by the AD840 in a noninverting configuration (Figure 10). The noise gain of this topology is 10, requiring only 5pF across the feedback resistor to optimize settling.

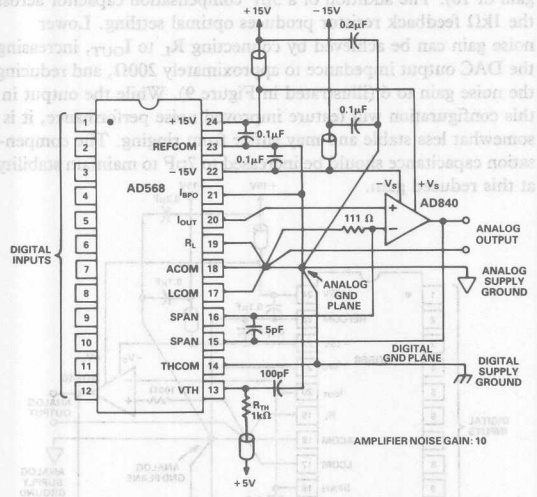


Figure 10. Unipolar Output Buffered 0 to +10.24V

Guidelines for Using the AD568

The designer who seeks to combine high speed with high precision faces a challenging design environment. Where tens of milliamperes are involved, fractions of an ohm of misplaced impedance can generate several LSBs of error. Increasing bandwidths make formerly negligible parasitic capacitances and inductances significant. As system performance reaches and exceeds that of the measurement equipment, time-honored test methods may no longer be trustworthy. The DAC's placement on the boundary between the analog and digital domains introduces additional concerns. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding, and measurement if optimal performance is to be realized. The AD568 has been configured to be relatively easy to use, even in some of the more treacherous applications. The device characteristics shown in this datasheet are readily achievable if proper attention is paid to the details. Since a solid understanding of the circuit involved is one of the designer's best weapons against the difficulties of RF design, the following sections provide illustrations, explanations, examples, and suggestions to facilitate successful design with the AD568.

Current Output vs. Voltage Output

As indicated in Figures 3 through 10, the AD568 has been designed to operate in several different modes depending on the external circuit configuration. While these modes may be categorized by many different schemes, one of the most important distinctions to be made is whether the DAC is to be used to generate an output voltage or an output current. In the current output mode, the DAC output (Pin 20) is tied to some type of summing junction, and the current flowing from the DAC into this summing junction is sensed (e.g., Figures 8 and 9). In this mode, the DAC output scale is insensitive to whether the load resistor, R_L, is shorted (Pin 19 connected to Pin 20), or grounded (Pin 19 connected to Pin 18). However, this does affect the output impedance of the DAC current and may have a significant impact on the noise gain of the external circuitry. In the voltage output mode, the DAC's output current flows through its own internal impedance (perhaps in parallel with an external impedance) to generate a voltage, as in Figures 3, 4, 5, and 10. In this case, the DAC output scale is directly dependent on the load impedance. The temperature coefficient of the AD568's internal reference is trimmed in such a way that the drift of the DAC output in the voltage output mode is centered on zero. The current output of the DAC will have an additional drift factor corresponding to the absolute temperature coefficient of the internal thin-film resistors. This additional drift may be removed by judicious placement of the 1kΩ span resistor in the signal path. For example, in Figures 8 and 9, the current flowing from the DAC into the summing junction could suffer from as much as 150ppm/°C of thermal drift. However, since this current flows through the internal span resistor (Pins 15 and 16) which has a temperature coefficient that matches the DAC ladder resistors, this drift factor is compensated and the buffered voltage at the amplifier output will be within specified limits for the voltage output mode.

Output Voltage Compliance

The AD568 has a typical output compliance range of +1.2V to −2.0V (with respect to the LCOM Pin). The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, as shown in Figure 11, there is an equivalent output impedance of 200Ω in parallel with 15pF at the output terminal which produces an equivalent error current if the voltage deviates from the ladder common. This is a linear effect which does not change with input code. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance. The positive compliance limit is not affected by the positive power supply, but is a function of output current and the logic threshold voltage at V_{TH}, Pin 13.

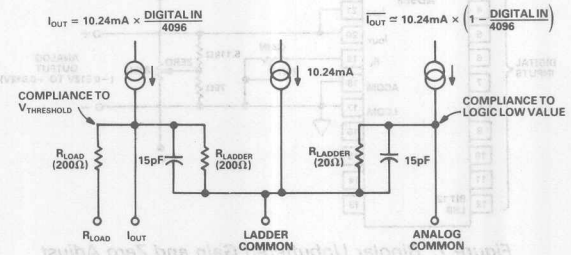


Figure 11. Equivalent Output

Digital Input Considerations

The AD568 uses a standard positive true straight binary code for unipolar outputs (all 1s full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full scale; with 111 . . . 11, the output will go to positive full scale less 1LSB; and with 100 . . 00 (only the MSB on), the output will go to zero.

The threshold of the digital inputs is set at 1.4V and does not vary with supply voltage. This is provided by a bandgap reference generator, which requires approximately 3mA of bias current achieved by tying R_{TH} to any $+V_L$ supply where

$$R_{TH} = \left(\frac{+V_L - 1.4V}{3mA}\right).$$

The input lines operate with small input currents to easily achieve interface with unbuffered CMOS logic. The digital input signals to the DAC should be isolated from the analog output as much as possible. To minimize undershoot, ringing, and possible digital feedthrough noise, the interconnect distances to the DAC inputs should be kept as short as possible. Termination resistors may improve performance if the digital lines become too long. The digital input should be free from large glitches and ringing and have maximum 10% to 90% rise and fall times of 5ns. Figure 12 shows the equivalent digital input circuit of the AD568.

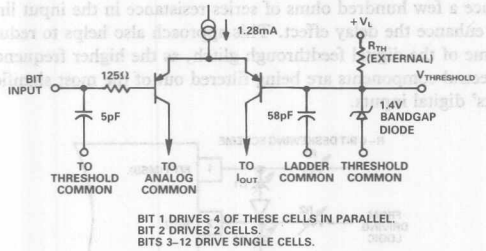


Figure 12. Equivalent Digital Input

Due to the high-speed nature of the AD568, it is recommended that high-speed logic families such as Schottky TTL, high-speed CMOS, or the new lines of FAST* TTL be used exclusively. Table I shows how DAC performance can vary depending on the driving logic used. As this table indicates, STTL, HCMOS, and FAST represent the most viable families for driving the AD568.

DAC PERFORMANCE VS. DRIVE LOGIC[1]

Logic Family	10-90% DAC Rise Time[2]	DAC SETTLING TIME[2,3] 1%	0.1%	0.025%	Glitch[4] Impulse	Maximum Glitch Excursion
TTL	11ns	18ns	34ns	50ns	2.5nV-s	240mV
LSTTL	11ns	28ns	46ns	80ns	950pV-s	160mV
STTL	9.5ns	16ns	33ns	50ns	850pV-s	150mV
HCMOS	11ns	24ns	38ns	50ns	350pV-s	115mV
FAST*	12ns	16ns	36ns	42ns	1.0nV-s	250mV

[1]All values typical, taken in test fixture diagrammed in Figure 13.
[2]Measurements are made for a 1V full-scale step into 100ΩDAC load resistance.
[3]Settling time is measured from the time the digital input crosses the threshold voltage (1.4V) to when the output is within the specified range of its final value.
[4]The worst case glitch impulse, measured on the major carry. DAC full scale is 1V.

Table I.

The variations in settling times can be attributed to differences in the rise time and current driving capabilities of the various families. Differences in the glitch impulse are predominantly dependent upon the variation in data skew. Variations in these specs occur not only between logic families, but also between different gates and latches within the same family. When selecting a gate to drive the AD568 logic input, pay particular attention to the propagation delay time specs: t_{PLH} and t_{PHL}. Selecting the smallest delays possible will help to minimize the settling time, while selection of gates where t_{PLH} and t_{PHL} are closely matched to one another will minimize the glitch impulse resulting from data skew. Of the common latches, the 74374 octal flip-flop provides the best performance in this area for many of the logic families mentioned above.

***FAST is a registered trademark of Fairchild Camera and Instrumentation Corporation.**

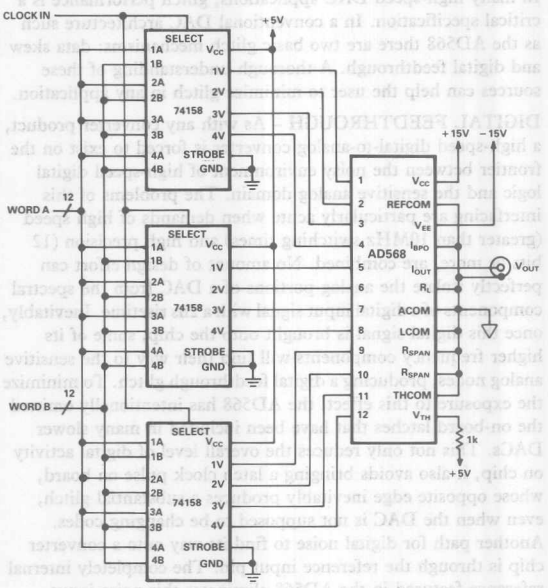


Figure 13. Test Setup for Glitch Impulse and Settling Time Measurements

Settling Time Considerations

As can be seen from Table I and the specifications page, the settling time of the AD568 is application dependent. The fastest settling is achieved in the current-output mode, since the voltage-output mode requires the output capacitance to be charged to the appropriate voltage. The DAC's relatively large output current helps to minimize this effect, but settling-time sensitive applications should avoid any unnecessary parasitic capacitance at the output node of voltage output configurations. Direct measurement of the fine scale DAC settling time, even in the voltage output mode, is extremely tricky: analog scope front ends are generally incapable of recovering from overdrive quickly enough to give an accurate settling representation. The plot shown in Figure 14 was obtained using Data Precision's 640 16-bit sampling head, which features the quick overdrive recovery characteristic of sampling approaches combined with high accuracy and relatively small thermal tail.

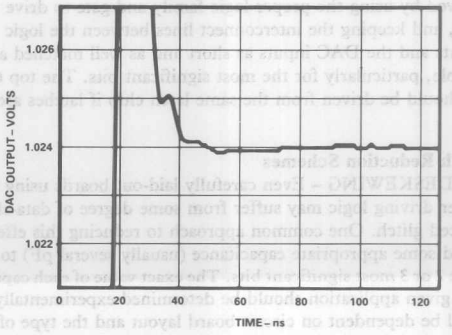


Figure 14. Zero to Full-Scale Settling

Glitch Considerations

In many high-speed DAC applications, glitch performance is a critical specification. In a conventional DAC architecture such as the AD568 there are two basic glitch mechanisms: data skew and digital feedthrough. A thorough understanding of these sources can help the user to minimize glitch in any application.

DIGITAL FEEDTHROUGH – As with any converter product, a high-speed digital-to-analog converter is forced to exist on the frontier between the noisy environment of high-speed digital logic and the sensitive analog domain. The problems of this interfacing are particularly acute when demands of high speed (greater than 10MHz switching times) and high precision (12 bits or more) are combined. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of a digital input signal with a 2ns risetime. Inevitably, once this digital signal is brought onto the chip, some of its higher frequency components will find their way to the sensitive analog nodes, producing a digital feedthrough glitch. To minimize the exposure to this effect, the AD568 has intentionally omitted the on-board latches that have been included in many slower DACs. This not only reduces the overall level of digital activity on chip, it also avoids bringing a latch clock pulse on board, whose opposite edge inevitably produces a substantial glitch, even when the DAC is not supposed to be changing codes. Another path for digital noise to find its way onto a converter chip is through the reference input pin. The completely internal reference featured in the AD568 eliminates this noise input, providing a greater degree of signal integrity in the analog portions of the chip.

DATA SKEW – The AD568, like many of its slower predecessors, essentially uses each digital input line to switch a separate, weighted current to either the output (I_{OUT}) or some other node (ANALOG COM). If the input bits are not changed simultaneously, or if the different DAC bits switch at different speeds, then the DAC output current will momentarily take on some incorrect value. This effect is particularly troublesome at the "carry points", where the DAC output is to change by only one LSB, but several of the larger current sources must be switched to realize this change. Data skew can allow the DAC output to move a substantial amount towards full scale or zero (depending upon the direction of the skew) when only a small transition is desired. Great care was taken in the design and layout of the AD568 to ensure that switching times of the DAC switches are symmetrical and that the length of the input data lines are short and well matched. The glitch-sensitive user should be equally diligent about minimizing the data skew at the AD568's inputs, particularly for the 4 or 5 most significant bits. This can be achieved by using the proper logic family and gate to drive the DAC, and keeping the interconnect lines between the logic outputs and the DAC inputs as short and as well matched as possible, particularly for the most significant bits. The top 6 bits should be driven from the same latch chip if latches are used.

Glitch Reduction Schemes

BIT-DESKEWING – Even carefully laid-out boards using the proper driving logic may suffer from some degree of data-skew induced glitch. One common approach to reducing this effect is to add some appropriate capacitance (usually several pF) to each of the 2 or 3 most significant bits. The exact value of each capacitor for a given application should be determined experimentally, as it will be dependent on circuit board layout and the type of driving logic used. Table II presents a few examples of how the glitch impulse may be reduced through passive deskewing.

BIT DELAY GLITCH REDUCTION EXAMPLES[1]

Logic Family	Gate	Uncompensated Glitch	Compensation Used	Compensated Glitch
HCMOS	74157	350pV-s	C2 = 5pF	250pV-s
STTL	74158	850pV-s	R1 = 50Ω, C1 = 7pF	600pV-s

NOTE
[1]Measurements were made using a modified version of the fixture shown in Figure 13, with resistors and capacitors placed as shown in Figure 15. Resistance and capacitance values were set to zero except as noted.

Table II.

As Figure 15 indicates, in some cases it may prove useful to place a few hundred ohms of series resistance in the input line to enhance the delay effect. This approach also helps to reduce some of the digital feedthrough glitch, as the higher frequency spectral components are being filtered out of the most significant bits' digital inputs.

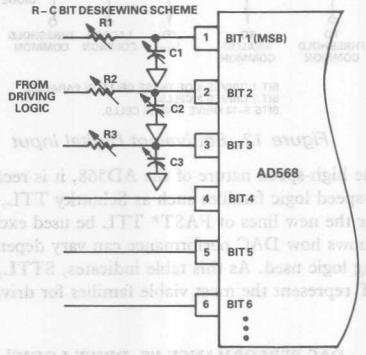


Figure 15. R–C Bit Deskewing Scheme

THRESHOLD SHIFT – It is also possible to reduce the data skew by shifting the level of logic voltage threshold, V_{TH} (Pin 13). This can be readily accomplished by inserting some resistance between the THRESHOLD COM pin (Pin 14) and ground, as in Figure 16. To generate threshold voltages below 1.4V, Pin 13 may be directly driven with a voltage source, leaving Pin 14 tied to the ground plane. As Note 2 in Table III indicates, lowering the threshold voltage may reduce output voltage compliance below the specified limits, which may be of concern in an unbuffered voltage output topology.

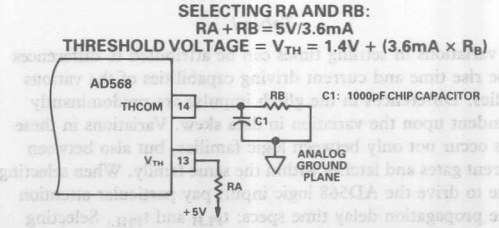


Figure 16. Positive Threshold Voltage Shift

Table III shows the glitch reduction achieved by shifting the threshold voltage for HCMOS, STTL, and FAST logic.

THRESHOLD SHIFT FOR GLITCH IMPROVEMENT[1]

Logic Family	Gate	Uncompensated Glitch	Modified Threshold[2]	Resulting Glitch
HCMOS	74HC158	350pV-s	1.7V	150pV-s
STTL	74S158	850pV-s	1.0V	200pV-s
FAST	74F158	1000pV-s	1.3V	480pV-s

NOTES
[1]Measurements made on a modified version of the circuit shown in Figure 13, with a 1V full scale.
[2]Use care in any scheme that lowers the threshold voltage since the output voltage compliance of the DAC is sensitive to this voltage. If the DAC is to be operated in the voltage output mode, it is strongly suggested that the threshold voltage be set at least 200mV above the output voltage full scale.

Table III.

Deglitching

Some applications may prove so sensitive to glitch impulse that reduction of glitch impulse by an order of magnitude or more is required. In order to realize glitch impulses this low, some sort of sample-and-hold amplifier (SHA)-based deglitching scheme must be used.

There are high-speed SHAs available with specifications sufficient to deglitch the AD568, however most are hybrid in design at costs which can be prohibitive. A high performance, low cost alternative shown in Figure 17 is a discrete SHA utilizing a high-speed monolithic op amp and high-speed DMOS FET switches.

This SHA circuit uses the inverting integrator architecture. The AD841 operational amplifier used (300MHz gain bandwidth product) is fabricated on the same high-speed process as the AD568. The time constant formed by the 200Ω resistor and the 100pF capacitor determines the acquisition time and also band limits the output signal to eliminate slew induced distortion.

A discrete drive circuit is used to achieve the best performance from the SD5000 quad DMOS switch. This switch driving cell is composed of MPS571 RF npn transistors and an MC10124 TTL to ECL translator. Using this technique provides both high speed and highly symmetrical drive signals for the SD5000 switches. The switches are arranged in a single-throw double-pole (SPDT) configuration. The 360pF "flyback" capacitor is switched to the op amp summing junction during the hold mode to keep switching transients from feeding to the output. This capacitor is grounded during sample mode to minimize its effect on acquisition time.

Circuit layout for a high speed SHA is almost as critical as the design itself. Figure 17 shows a recommended layout of the deglitching cell for a double sided printed circuit board. The layout is very compact with care taken that all critical signal paths are short.

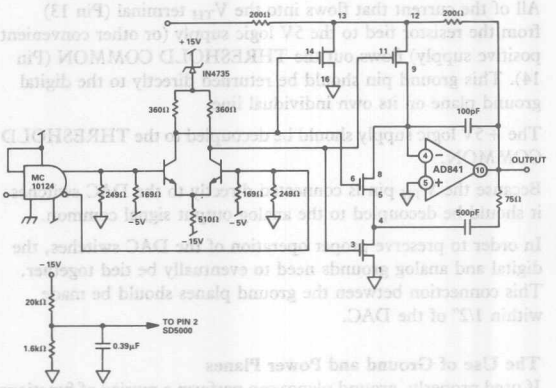


Figure 17. High Performance Deglitcher

Grounding Rules

The AD568 brings out separate reference, output, and digital power grounds. This allows for optimum management of signal ground currents for low noise and high-speed settling performance. The separate ground returns are provided to minimize changes in current flow in the analog signal paths. In this way, logic return currents are not summed into the same return path with the analog signals.

It is important to understand which supply and signal currents are flowing in which grounds so that they may be returned to the proper power supply in the best possible way.

The majority of the current that flows into the V_{CC} supply (Pin 24) flows out (depending on the DAC input code) either the ANALOG COMMON (Pin 18), the LADDER COMMON (Pin 17), and/or I_{OUT} (Pin 20).

The current in the LADDER COMMON is configured to be code independent when the output current is being summed into a virtual ground. If I_{OUT} is operated into its own output impedance (or in any unbuffered voltage output mode) the current in LADDER COMMON will become partially code dependent.

The current in the ANALOG COMMON (Pin 18) is an approximate complement of the current in I_{OUT}, i.e., zero when the DAC is at full scale and approximately 10mA at zero input code.

A relatively constant current (not code dependent) flows out the REFERENCE COMMON (Pin 23).

The current flowing out of the V_{EE} supply (Pin 22) comes from a combination of reference ground and BIPOLAR OFFSET (Pin 21). The plus and minus 15V supplies are decoupled to the REFERENCE COMMON.

The ground side of the load resistor R_L, ANALOG COMMON and LADDER COMMON should be tied together as close to the package pins as possible. The analog output voltage is then referred to this node and thus it becomes the "high quality" ground for the AD568. The REFERENCE COMMON (and Bipolar offset when not used), should also be connected to this node.

positive supply) flows out the THRESHOLD COMMON (Pin 14). This ground pin should be returned directly to the digital ground plane on its own individual line.

The +5V logic supply should be decoupled to the THRESHOLD COMMON.

Because the V_{TH} pin is connected directly to the DAC switches it should be decoupled to the analog output signal common.

In order to preserve proper operation of the DAC switches, the digital and analog grounds need to eventually be tied together. This connection between the ground planes should be made within 1/2" of the DAC.

The Use of Ground and Power Planes

If used properly, ground planes can perform a myriad of functions on high-speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from one another, with the analog ground plane covering analog signal traces and the digital ground plane confined to areas covering digital interconnect.

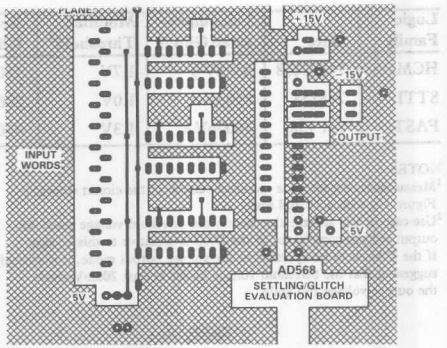
The two ground planes should be connected at or near the DAC. Care should be taken to insure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC and any clock lines. On the analog side, this includes the DAC output signal as well as the supply feeders. The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane. Figure 18 illustrates the PC board used for the circuit shown in Figure 13. This design was constructed on a simple two-layer board and illustrates many of the points discussed above. If more layers of interconnect are available, even better results are possible.

Using The Right Bypass Capacitors

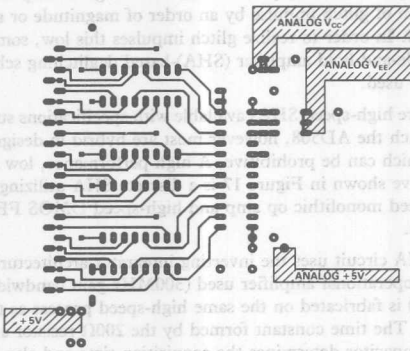
Probably the most important external components associated with any high-speed design are the capacitors used to bypass the power supplies. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configurations. The dominant consideration in selection of bypass capacitors for the AD568 is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20MHz and above, the very frequencies we are most interested in bypassing. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. A few general rules are of universal use when approaching the problem of bypassing:

Bypass capacitors should be installed on the printed circuit board with the shortest possible leads consistent with reliable construction. This helps to minimize series inductance in the leads. Chip capacitors are optimal in this respect.

Some series inductance between the DAC supply pins and the power supply plane often helps to filter out high-frequency power supply noise. This inductance can be generated using a small ferrite bead.



Component Side



Foil Side

Figure 18. Printed Circuit Board Layout

High-Speed Interconnect and Routing

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. It is suggested that all connections be short and direct, and as physically close to the package as possible, so that the length of any conduction path shared by external components will be minimized. When runs exceed an inch or so in length, some type of termination resistor may be required. The necessity and value of this resistor will be dependent upon the logic family used.

For maximum ac performance, the DAC should be mounted directly to the circuit board; sockets should not be used as they introduce unwanted capacitive coupling between adjacent pins of the device.

Applications

1μs, 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The AD568's unique combination of high speed and true 12-bit accuracy can be used to construct a 12-bit SAR-type A/D converter with a sub-μs conversion time. Figure 19 shows the configuration used for this application. A negative analog input voltage is converted into current and brought into a summing junction with the DAC current. This summing junction is bidirectionally clamped with two Shottky diodes to limit its voltage excursion from ground. This voltage is differentially amplified and passed to a high-speed comparator. The comparator output is latched and fed back to the successive approximation register, which is then clocked to generate the next set of codes for the DAC.

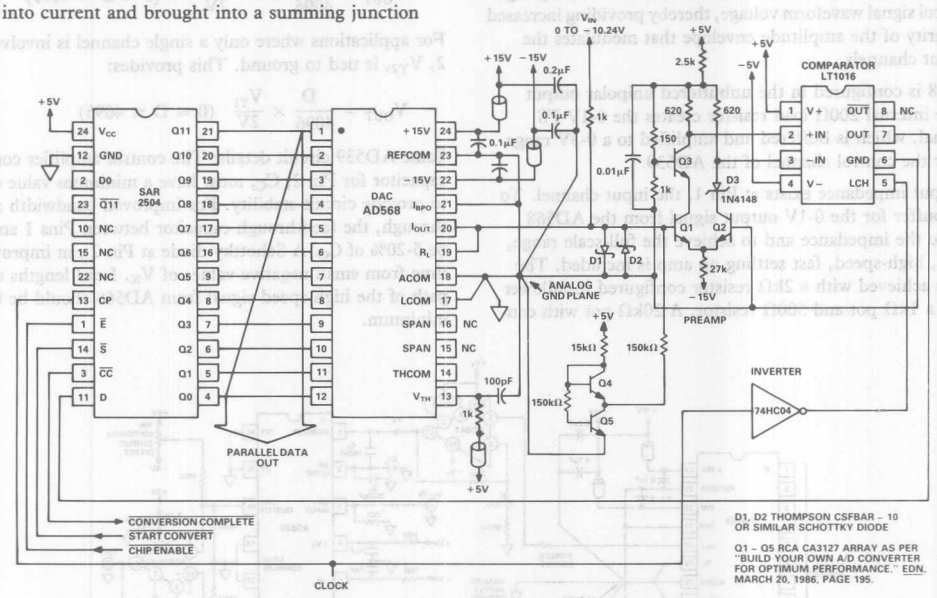


Figure 19. AD568 1μs Successive Approximation A/D Application

Circuit Details

Figure 20 shows an approximate timing budget for the A/D converter. If 12 cycles are to be completed in 1μs, approximately 80ns is allowed for each cycle. Since the Shottky diodes clamp the voltage of the summing junction, the DAC settling time approaches the current-settling value of 35ns, and hence uses up less than half the timing budget.

To maintain simplicity, a simple clock is used that runs at a constant rate throughout the conversion, with a duty cycle of approximately 90%. If absolute speed is worth the additional complexity, the clock frequency can be increased as the conversion progresses since the DAC must settle from increasingly smaller steps.

When seeking a cycle time of less than 100ns, the delays generated by the older generation SAR registers become problematic. Newer, higher speed SAR logic chips are becoming available in the classic 2504 pinout that cuts the logic overhead in half. One example of this is Zyrel's ZR2504.

Finding a comparator capable of keeping up with this DAC arrangement is fairly difficult: it must respond to an overdrive of 250μV (1LSB) in less than 25ns. Since no inexpensive comparator exists with these specs, special arrangements must be made. The LT1016 comparator provides relatively quick response, but requires at least 5mV of overdrive to maintain this speed. A discrete preamplifier may be used to amplify the summing junction voltage to sufficiently overdrive the comparator. Care must be exercised in the layout of the preamp/comparator block to avoid introducing comparator instability with the preamp's additional gain.

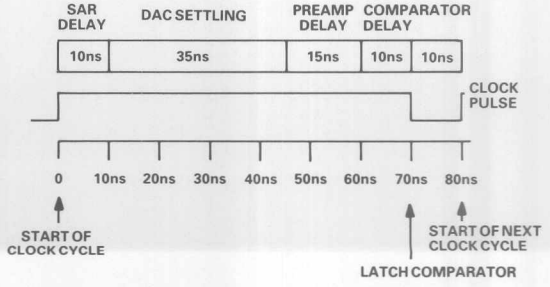


Figure 20. Typical Clock Cycle for a 1μs SAR A/D Converter

HIGH-SPEED MULTIPLYING DAC

A powerful use for the AD568 is found in multiplying applications, where the DAC controls the amplitude of a high-speed signal. Specifically, using the AD568 as the control voltage input signal for the AD539 60MHz analog multiplier and AD5539 wide-band op amp, a high-speed multiplying DAC can be built.

In the application shown in Figure 21, the AD568 is used in a buffered voltage output mode to generate the input to the AD539's control channel. The speed of the AD568 allows oversampling of the control signal waveform voltage, thereby providing increased spectral purity of the amplitude envelope that modulates the analog input channels.

The AD568 is configured in the unbuffered unipolar output mode. The internal 200Ω load resistor creates the 0-1V FS output signal, which is buffered and amplified to a 0-3V range suitable for the control channel of the AD539.

A 500Ω input impedance exists at Pin 1, the input channel. To provide a buffer for the 0-1V output signal from the AD568 looking into the impedance and to achieve the full-scale range, the AD841, high-speed, fast settling op amp is included. The gain of 3 is achieved with a 2kΩ resistor configured in follower mode with a 1kΩ pot and 500Ω resistor. A 20kΩ pot with connections to Pins 3, 4 and 12 is provided for offset trim.

The AD539 can accept two separate input signals, each with a nominal full-scale voltage range of ±2V. Each signal can then be simultaneously controlled by the AD568 signal at the common input channel, V_X. The current outputs from the two signal channels, Pins 11 and 14, applied to the AD5539 in a subtracting configuration, provide the voltage output signal:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1} - V_{Y2}}{2V} \quad (0 \leq D \leq 4095)$$

For applications where only a single channel is involved, channel 2, V_{Y2}, is tied to ground. This provides:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1}}{2V} \quad (0 \leq D \leq 4095)$$

Some AD539 circuit details: The control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000pF to provide circuit stability. For improved bandwidth and feedthrough, the feedthrough capacitor between Pins 1 and 2 should be 5-20% of C_C. A Schottky diode at Pin 2 can improve recovery time from small negative values of V_X. Lead lengths along the path of the high-speed signal from AD568 should be kept at a minimum.

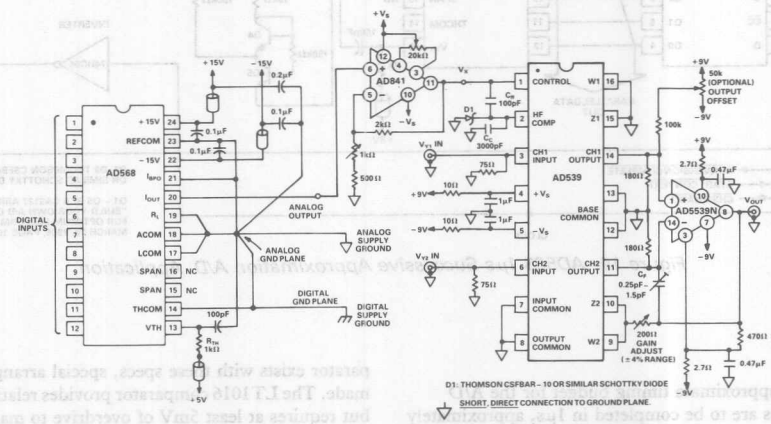


Figure 21. Wideband Digitally Controlled Multiplier

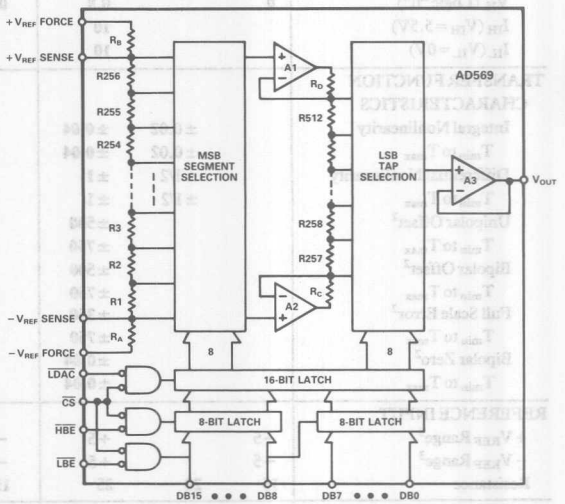
16-Bit Monotonic Voltage Output D/A Converter

AD569

FEATURES
- Guaranteed 16-Bit Monotonicity
- Monolithic BiMOS II Construction
- ±0.01% Typical Nonlinearity
- 8- and 16-Bit Bus Compatibility
- 3μs Settling to 16-Bits
- Low Drift
- Low Power
- Low Noise

APPLICATIONS
- Robotics
- Closed-Loop Positioning
- High-Resolution ADCs
- Microprocessor-Based Process Control
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit digital-to-analog converter (DAC) manufactured in Analog Devices' BiMOS II process. BiMOS II allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD569 chip includes two resistor strings, selector switches, decoding logic, buffer amplifiers, and double-buffered input latches.

The AD569's voltage-segmented architecture insures 16-bit monotonicity over time and temperature. Integral nonlinearity is maintained at ±0.01%, while differential nonlinearity is ±0.0004%. The on-chip, high-speed buffer amplifiers provide a voltage output settling time of 3μs to within ±0.001% for a full-scale step.

The reference input voltage which determines the output range can be either unipolar or bipolar. Nominal reference range is ±5V and separate reference force and sense connections are provided for high accuracy applications. The AD569 can operate with an ac reference in multiplying applications.

Data may be loaded into the AD569's input latches from 8- and 16-bit buses. The double-buffered structure simplifies 8-bit bus interfacing and allows multiple DACs to be loaded asynchronously and updated simultaneously. Four TTL/LSTTL/5V CMOS-compatible signals control the latches: $\overline{CS}$, $\overline{LBE}$, $\overline{HBE}$, and $\overline{LDAC}$.

The AD569 is available in five grades: J and K versions are specified from 0 to +70°C and are packaged in a 28-pin plastic DIP and 28-pin PLCC package; AD and BD versions are specified from −25°C to +85°C and are packaged in a 28-pin ceramic DIP. The SD version, also in a 28-pin ceramic DIP, is specified from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monotonicity to 16 bits is insured by the AD569's voltage-segmented architecture.
2. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift of the AD569 are negligible.
3. The AD569's versatile data input structure allows loading from 8- and 16-bit buses.
4. The on-chip output buffer amplifier can supply ±5V into a 1kΩ load, and can drive capacitive loads of up to 1000pF.
5. Kelvin connections to the reference inputs preserve the gain and offset accuracy of the transfer function in the presence of wiring resistances and ground currents.
6. The AD569 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD569/883B data sheet for detailed specifications.

Model	AD569JN/JP/AD			AD569KN/KP/BD			AD569SD			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION			16			16			16	Bits
LOGIC INPUTS										
V_{IH} (Logic "1")	**2.0**		**5.5**	**2.0**		**5.5**	**2.0**		**5.5**	Volts
V_{IL} (Logic "0")	**0**		**0.8**	**0**		**0.8**	**0**		**0.8**	Volts
I_{IH} (V_{IH} = 5.5V)			**10**			**10**			**10**	μA
I_{IL} (V_{IL} = 0V)			**10**			**10**			**10**	μA
TRANSFER FUNCTION CHARACTERISTICS										
Integral Nonlinearity		**±0.02**	**±0.04**		**±0.01**	**±0.024**			**±0.04**	% FSR[1]
T_{min} to T_{max}		**±0.02**	**±0.04**		**±0.020**	**±0.024**			**±0.04**	% FSR
Differential Nonlinearity		**±1/2**	**±1**		**±1/4**	**±1/2**			**±1**	LSB
T_{min} to T_{max}		**±1/2**	**±1**		**±1/2**	**±1**			**±1**	LSB
Unipolar Offset[2]			**±500**			**±350**			**±500**	μV
T_{min} to T_{max}			**±750**			**±450**			**±750**	μV
Bipolar Offset[2]			**±500**			**±350**			**±500**	μV
T_{min} to T_{max}			**±750**			**±450**			**±750**	μV
Full Scale Error[2]			**±350**			**±350**			**±350**	μV
T_{min} to T_{max}			**±750**			**±750**			**±750**	μV
Bipolar Zero[2]			**±0.04**			**±0.024**			**±0.04**	% FSR
T_{min} to T_{max}			**±0.04**			**±0.024**			**±0.04**	% FSR
REFERENCE INPUT										
$+V_{REF}$ Range[3]	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	Volts
$-V_{REF}$ Range[3]	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	Volts
Resistance	**15**	**20**	**25**	**15**	**20**	**25**	**15**	**20**	**25**	kΩ[4]
OUTPUT CHARACTERISTICS										
Voltage	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	Volts
Capacitive Load			**1000**			**1000**			**1000**	pF
Resistive Load	**1**			**1**			**1**			kΩ
Short Circuit Current		**10**			**10**			**10**		mA
POWER SUPPLIES										
Voltage										
$+V_S$	**+10.8**	**+12**	**+13.2**	**+10.8**	**+12**	**+13.2**	**+10.8**	**+12**	**+13.2**	Volts
$-V_S$	**−10.8**	**−12**	**−13.2**	**−10.8**	**−12**	**−13.2**	**−10.8**	**−12**	**−13.2**	Volts
Current										
$+I_S$		**+9**	**+13**		**+9**	**+13**		**+9**	**+13**	mA
$-I_S$		**−9**	**−13**		**−9**	**−13**		**−9**	**−13**	mA
Power Supply Sensitivity[5]										
$+10.8V \leq +V_S \leq +13.2V$		**±0.5**	**±2**		**±0.5**	**±2**		**±0.5**	**±2**	ppm/%
$-10.8V \geq -V_S \geq -13.2V$		**±1**	**±3**		**±1**	**±3**		**±1**	**±3**	ppm/%
TEMPERATURE RANGE										
Specified										
JN, KN, JP, KP	0		+70	0		+70				°C
AD, BD	−25		+85	−25		+85				°C
SD							−55		+125	°C
Storage										
JN, KN, JP, KP	−65		+150	−65		+150				°C
AD, BD, SD	−65		+150	−65		+150	−65		+150	°C

NOTES

[1]FSR stands for Full-Scale Range, and is 10V for a −5 to +5V span.

[2]Refer to Definitions section.

[3]For operation with supplies other than ±12V, refer to the Power Supply and Reference Voltage Range Section.

[4]Measured between $+V_{REF}$ Force and $-V_{REF}$ Force.

[5]Sensitivity of Full-Scale Error due to changes in $+V_S$ and sensitivity of Offset to changes in $-V_S$.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

These characteristics are included for Design Guidance Only and are not subject to test.
$+V_S = +12V; -V_S = -12V; +V_{REF} = +5V; -V_{REF} = -5V$ except where stated.

Parameter	Limit	Units	Test Conditions/Comments
Output Voltage Settling (Time to ±0.001% FS For FS Step)	5	µs max	No Load Applied (DAC output measured from falling edge of $\overline{LDAC}$.)
	3	µs typ	
	6	µs max	V_{OUT} Load = 1kΩ, C_{LOAD} = 1000pF. (DAC output measured from falling edge of $\overline{LDAC}$.)
	4	µs typ	
Digital-to-Analog Glitch Impulse	500	nV-sec typ	Measured with V_{REF} = 0V. DAC registers alternatively loaded with input codes of 8000_H and $0FFF_H$ (worst-case transition). Load = 1kΩ.
Multiplying Feedthrough	−100	dB max	$+V_{REF}$ = 1V rms 10kHz sine wave, $-V_{REF}$ = 0V
Output Noise Voltage Density (1kHz-1MHz)	40	nV/√Hz typ	Measured between V_{OUT} and $-V_{REF}$

TIMING CHARACTERISTICS ($+V_S = +12V, -V_S = -12V, V_{IH} = 2.4V, V_{IL} = 0.4V, T_{min}$ to T_{max})

Parameter	Limit	Units	Test Conditions/Comments
Case A[1]			150ns Pulse on $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ T_{HS} = 140ns min, T_{HH} = 10ns min
t_{WC}	120	ns min	$\overline{CS}$ Pulse Width
t_{SC}	60	ns min	$\overline{CS}$ Data Setup Time
t_{HC}	20	ns min	$\overline{CS}$ Data Hold Time
Case B[2]			None
t_{WB}	70	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time
t_{WD}	120	ns min	$\overline{LDAC}$ Pulse Width
Case C[3]			None
t_{WB}	120	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time

NOTES
[1]Write strobe applied to $\overline{CS}$ as shown in Figure 20a. Address decoding defines which register(s) data is strobed into (see Figure 1).
[2]Write strobe applied to $\overline{HBE}$ and/or $\overline{LBE}$ as in Figure 19 or applied to $\overline{LDAC}$ separately. DAC base address applied to $\overline{CS}$ (see Figure 2a).
[3]Write strobe applied to $\overline{LDAC}$ and either $\overline{HBE}$ or $\overline{LBE}$ for synchronous load of 16-bit DAC register with one of the 8-bit first-rank registers as shown in Figure 20b (see Figure 2b).

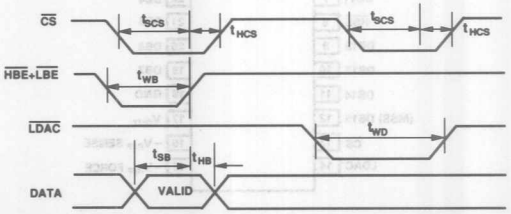


Figure 2a. AD569 Timing Diagram – Case B

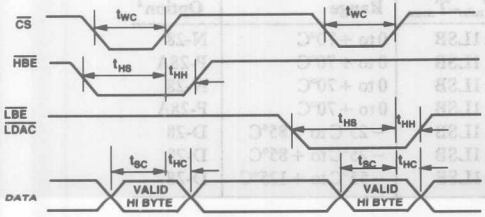


Figure 1. AD569 Timing Diagram – Case A

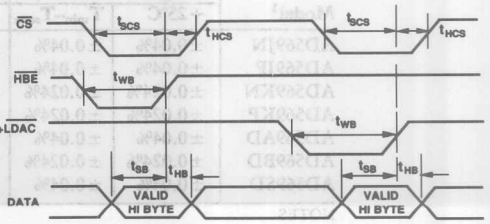


Figure 2b. AD569 Timing Diagram – Case C

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

$+V_S$ (Pin 1) to GND (Pin 18) . . . . . +18V, −0.3V
$-V_S$ (Pin 28) to GND (Pin 18) . . . . . −18V, +0.3V
$+V_S$ (Pin 1) to $-V_S$ (Pin 28) . . . . . +26.4V, −0.3V
Digital Inputs
(Pins 4–14, 19–27) to GND (Pin 18) . . . . . $+V_S$, −0.3V
$+V_{REF}$ Force (Pin 3) to $+V_{REF}$ Sense (Pin 2) . . . . ±16.5V
$-V_{REF}$ Force (Pin 15) to $-V_{REF}$ Sense (Pin 16) . . . ±16.5V
V_{REF} Force (Pins 3, 15) to GND (Pin 18) . . . . . ±V_S
V_{REF} Sense (Pins 2, 16) to GND (Pin 18) . . . . . ±V_S
V_{OUT} (Pin 17) . . . . . Indefinite Short to GND
Momentary Short to $+V_S$, $-V_S$
Power Dissipation (Any Package) 1000mW
Operating Temperature Range
Commercial Plastic (JN, KN, JP, KP Versions) . 0 to +70°C
Industrial Ceramic (AD, BD Versions) . . −25°C to +85°C
Extended Ceramic (SD Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

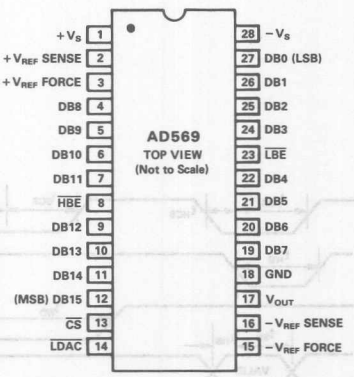
ESD SENSITIVITY

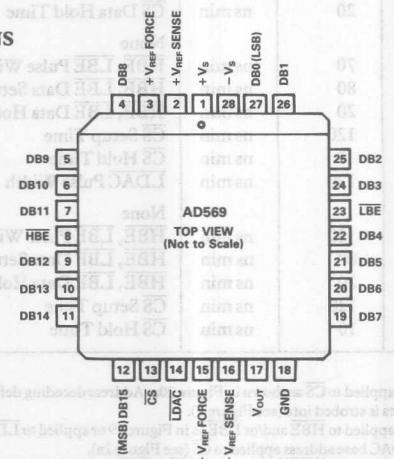
The AD569 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD569 has been classified as a Category A device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

PIN DESIGNATIONS





ORDERING GUIDE

Model[1]	Integral Nonlinearity +25°C	Integral Nonlinearity T_{min}–T_{max}	Differential Nonlinearity +25°C	Differential Nonlinearity T_{min}–T_{max}	Temperature Range	Package Option[2]
AD569JN	±0.04%	±0.04%	±1LSB	±1LSB	0 to +70°C	N-28
AD569JP	±0.04%	±0.04%	±1LSB	±1LSB	0 to +70°C	P-28A
AD569KN	±0.024%	±0.024%	±1/2LSB	±1LSB	0 to +70°C	N-28
AD569KP	±0.024%	±0.024%	±1/2LSB	±1LSB	0 to +70°C	P-28A
AD569AD	±0.04%	±0.04%	±1LSB	±1LSB	−25°C to +85°C	D-28
AD569BD	±0.024%	±0.024%	±1/2LSB	±1LSB	−25°C to +85°C	D-28
AD569SD	±0.04%	±0.04%	±1LSB	±1LSB	−55°C to +125°C	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD569/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

The AD569 consists of two resistor strings, each of which is divided into 256 equal segments (see Figure 3). The 8MSBs of the digital input word select one of the 256 segments on the first string. The taps at the top and bottom of the selected segment are connected to the inputs of the two buffer amplifiers A1 and A2. These amplifiers exhibit extremely high CMRR and low bias current, and thus accurately preserve the voltages at the top and bottom of the segment. The buffered voltages from the segment endpoints are applied across the second resistor string, where the 8LSBs of the digital input word select one of the 256 taps. Output amplifier A3 buffers this voltage and delivers it to the output.

Buffer amplifiers A1 and A2 leap-frog up the first string to preserve monotonicity at the segment boundaries. For example, when increasing the digital code from $00FF_H$ to 0100_H, (the first segment boundary), A1 remains connected to the same tap on the first resistor, while A2 jumps over it and is connected to the tap which becomes the top of the next segment. This design guarantees monotonicity even if the amplifiers have offset voltages. In fact, amplifier offset only contributes to integral linearity error.

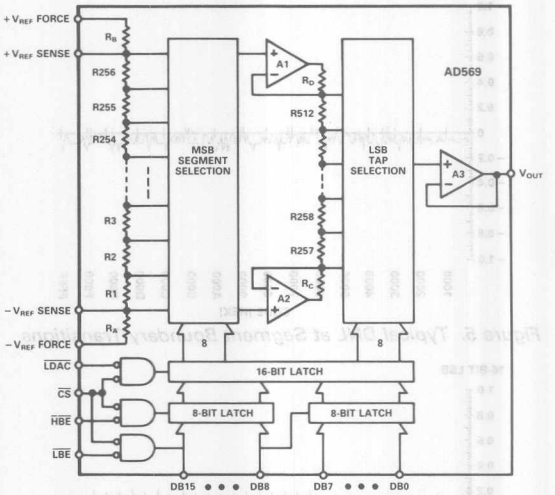


Figure 3. AD569 Block Diagram

CAUTION

It is generally considered good engineering practice to avoid inserting integrated circuits into powered-up sockets. This guideline is especially important with the AD569. An empty, powered-up socket configures external buffer amplifiers in an open-loop mode, forcing their outputs to be at the positive or negative rail. This condition may result in a large current surge between the reference force and sense terminals. This current surge may permanently damage the AD569.

ANALOG CIRCUIT DETAILS

Definitions

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal output (a straight line drawn from 0 to FS-1LSB) for any bit combination. The AD569's linearity is primarily limited by resistor uniformity in the first divider (upper byte of 16-bit input). The plot in Figure 4 shows the AD569's typical linearity error across the entire output range to be within ±0.01% of full scale. At 25°C the maximum linearity error for the AD569JN, AD and SD grades is specified to be ±0.04%, and ±0.024% for the KN and BD versions.

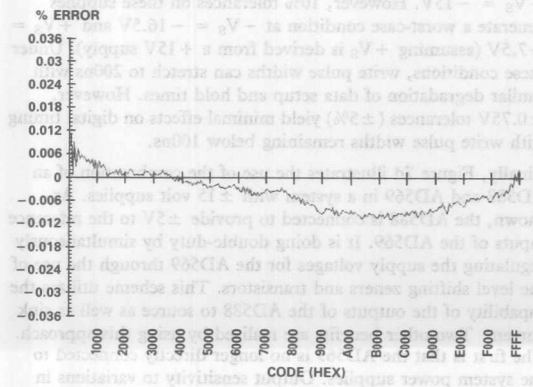


Figure 4. Typical Linearity

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs. All versions of the AD569 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: DNL is the measure of the change in the analog output, normalized to full scale, associated with a 1LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be less than 1LSB over the temperature range of interest. For example, for a ±5V output range, a change of 1LSB in digital input code should result in a 152μV change in the analog output (1LSB = 10V/65,536). If the change is actually 38μV, however, the differential linearity error would be −114μV, or −3/4LSB. By leapfrogging the buffer amplifier taps on the first divider, a typical AD569 keeps DNL within ±38μV (±1/4LSB) around each of the 256 segment boundaries defined by the upper byte of the input word (see Figure 5). Within the second divider, DNL also typically remains less than ±38μV as shown in Figure 6. Since the second divider is independent of absolute voltage, DNL is the same within the rest of the 256 segments.

OFFSET ERROR: The difference between the actual analog output and the ideal output ($-V_{REF}$), with the inputs loaded with all zeros is called the offset error. For the AD569, Unipolar Offset is specified with 0V applied to $-V_{REF}$ and Bipolar Offset is specified with −5V applied to $-V_{REF}$. Either offset is trimmed by adjusting the voltage applied to the $-V_{REF}$ terminals.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0.0000V when the inputs are loaded with 8000_H is called the Bipolar Zero Error. For the AD569, it is specified with ±5V applied to the reference terminals.

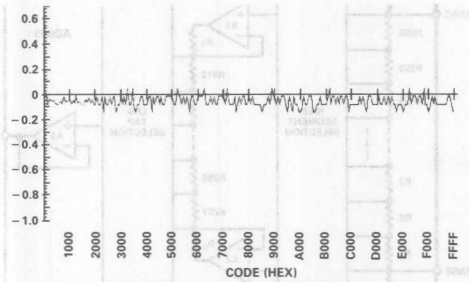
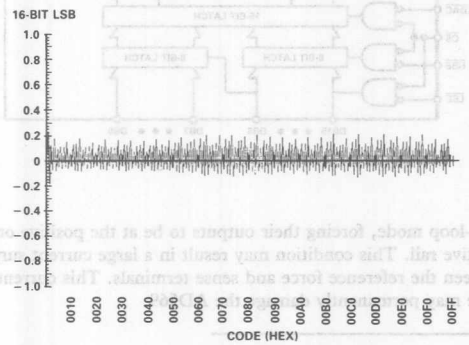
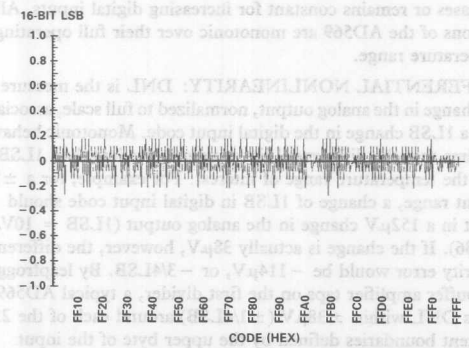


Figure 5. Typical DNL at Segment Boundary Transitions



a. Segment 1



b. Segment 256

Figure 6. Typical DNL Within Segments

MULTIPLYING FEEDTHROUGH ERROR: This is the error due to capacitive feedthrough from the reference to the output with the input registers loaded with all zeroes.

FULL-SCALE ERROR: The AD569's voltage dividing architecture gives rise to a fixed full-scale error which is independent of the reference voltage. This error is trimmed by adjusting the voltage applied to the $+V_{REF}$ terminals.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The charge injected into the analog output when a new input is latched into the DAC register gives rise to the Digital-to-Analog Glitch Impulse. with the reference connections tied to ground. It is specified as the area of the glitch in nV-secs.

TOTAL ERROR: The worst-case Total Error is the sum of the fixed full-scale and offset errors and the linearity error.

POWER SUPPLY AND REFERENCE VOLTAGE RANGES

The AD569 is specified for operation with ±12 volt power supplies. With ±10% power supply tolerances, the maximum reference voltage range is ±5 volts. Reference voltages up to ±6 volts can be used but linearity will degrade if the supplies approach their lower limits of ±10.8 volts (12 volts – 10%).

If ±12 volt power supplies are unavailable in the system, several alternative schemes may be used to obtain the needed supply voltages. For example, in a system with ±15V supplies, a single Zener diode can be used to reduce one of the supplies to 9 volts with the remaining one left at 15 volts. Figure 7a illustrates this scheme. A 1N753A or equivalent diode is an appropriate choice for the task. Asymmetrical power supplies can be used since the AD569's output is referenced to $-V_{REF}$ only and thus floats relative to logic ground (GND, Pin 18). Assuming a worst-case ±1.5 volt tolerance on both supplies (10% of 15 volts), the maximum reference voltage ranges would be +6 and −2 volts for $+V_S = +15V$ and $-V_S = -9V$, and +2 to −8 volts for $+V_S = 9V$ and $-V_S = -15V$.

Alternately, two 3V Zener diodes or voltage regulators can be used to drop each ±15 volt supply to ±12 volts, respectively. In Figure 7b, 1N746A diodes are a good choice for this task.

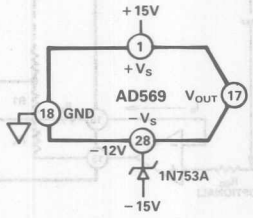
A third method may be used if both ±15 volt and ±5 volt supplies are available. Figure 7c shows this approach. A combination of $+V_S = +15V$ and $-V_S = -5V$ can support a reference range of 0 to 6 volts, while supplies of $+V_S = +5V$ and $-V_S = -15V$ can support a reference range of 0 to −8 volts. Again, 10% power supply tolerances are assumed.

NOTE: Operation with $+V_S = +5V$ alters the input latches' operating conditions causing minimum write pulse widths to extend to 1µs or more. Control signals $\overline{CS}$, $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ should, therefore, be tied low to render the latches transparent.

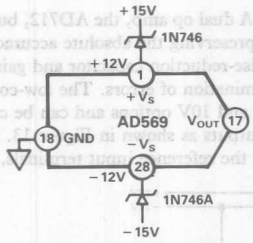
No timing problems exist with operation at $+V_S = 9V$ and $-V_S = -15V$. However, 10% tolerances on these supplies generate a worst-case condition at $-V_S = -16.5V$ and $+V_S = +7.5V$ (assuming $+V_S$ is derived from a +15V supply). Under these conditions, write pulse widths can stretch to 200ns with similar degradation of data setup and hold times. However, ±0.75V tolerances (±5%) yield minimal effects on digital timing with write pulse widths remaining below 100ns.

Finally, Figure 7d illustrates the use of the combination of an AD588 and AD569 in a system with ±15 volt supplies. As shown, the AD588 is connected to provide ±5V to the reference inputs of the AD569. It is doing double-duty by simultaneously regulating the supply voltages for the AD569 through the use of the level shifting zeners and transistors. This scheme utilizes the capability of the outputs of the AD588 to source as well as sink current. Two other benefits are realized by using this approach. The first is that the AD569 is no longer directly connected to the system power supplies. Output sensitivity to variations in those supplies is, therefore, eliminated. The second benefit is

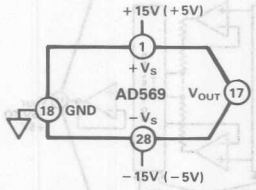
that, should a zener diode fail (a short circuit would be the most likely failure), the supply voltage decreases. This differs from the situation where the diode is used as a series regulator. In that case, a failure would place the unregulated supply voltage on the AD569 terminal.



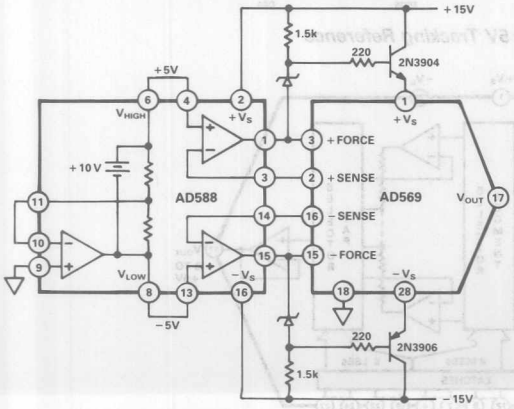
a. Zener Regulates Negative Supply



b. Diodes Regulate Both Supplies



c. Use of ±15V and ±5V Supplies



d. AD588 Produces References and Supply Voltages

Figure 7. Power Supply Options

ANALOG CIRCUIT CONNECTIONS

The AD569 is intended for use in applications where high resolution and stability are critical. Designed as a multiplying D/A converter, the AD569 may be used with a fixed dc reference or an ac reference. V_{REF} may be any voltage or combination of voltages at $+V_{FORCE}$ and $-V_{FORCE}$ that remain within the bounds set for reference voltages as discussed in the power supply range section. Since the AD569 is a multiplying D/A converter, its output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the reference terminal. The transfer function is $V_{OUT} = D \cdot V_{REF}$ where D is the fractional binary value of the digital word applied to the converter using offset-binary coding. Therefore, the output will range from $-V_{REF}$ for a digital input code of all zeros (0000_H) to $+V_{REF}$ for an input code of all ones ($FFFF_H$).

For applications where absolute accuracy is not critical, the simple reference connection in Figure 8 can be used. Using only the reference force inputs, this configuration maintains linearity and 16-bit monotonicity, but introduces small, fixed offset and gain errors. These errors are due to the voltage drops across resistors R_A and R_B shown in Figure 9. With a 10V reference voltage, the gain and offset errors will range from 80 to 100mV. Resistors R_A and R_B were included in the first resistor string to avoid degraded linearity due to uneven current densities at the string's endpoints. Similarly, linearity would degrade if the reference voltage were connected across the reference sense terminals. Note that the resistance between the force and sense terminals cannot be measured with an ohmmeter; the layout of the thin-film resistor string adds approximately 4kΩ of resistance (R_S) at the sense tap.

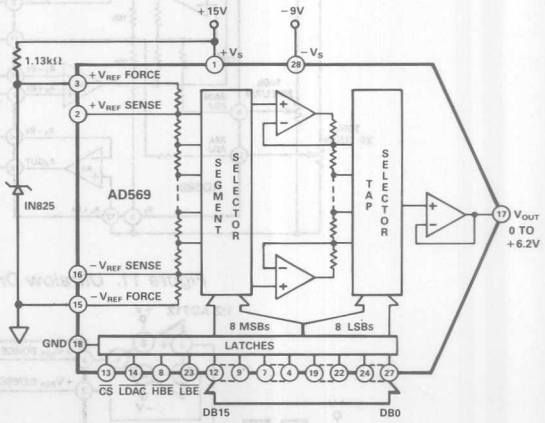


Figure 8. Simple Reference Connection

For those applications in which precision references and high accuracy are critical, buffer amplifiers are used at $+V_{REF}$ and $-V_{REF}$ as shown in Figure 10 to force the voltage across resistors R1 to R256. This insures that any errors induced by currents flowing through the resistances of the package pins, bond wires, aluminum interconnections, as well as R_A and R_B are minimized. Suitable amplifiers are the AD517, AD OP-07, AD OP-27, or the dual amplifier, the AD712. Errors will arise, however, as the buffer amplifiers' bias currents flow through R_S (4kΩ). If the bias currents produce such errors, resistance can be inserted at the noninverting terminal (R_{BC}) of the buffer amplifiers to compensate for the errors.

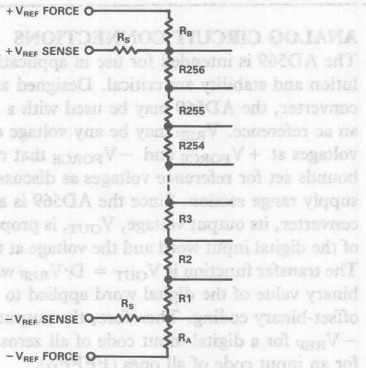


Figure 9. MSB Resistor Divider

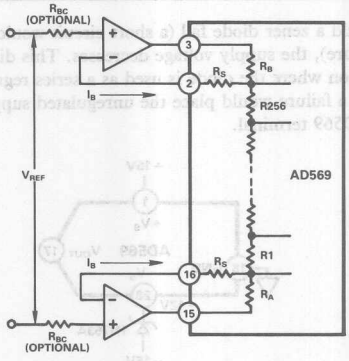


Figure 10. Reference Buffer Amplifier Connections

Figures 11, 12, and 13 show reference configurations for various output ranges. As shown in Figure 11, the pin-programmable AD588 can be connected to provides tracking ±5V outputs with 1-3ppm/°C temperature stability. Buffer amplifiers are included for direct connection to the AD569. The optional gain and balance adjust trimmers allow bipolar offset and full-scale errors to be nulled. In Figure 12, the low-cost AD586 provides +5V reference. A dual op amp, the AD712, buffers the reference input terminals preserving the absolute accuracy of the AD569. The optional noise-reduction capacitor and gain adjust trimmer allow further elimination of errors. The low-cost AD584 offers 2.5V, 5V, 7.5V, and 10V options and can be connected for ±5V tracking outputs as shown in Figure 13. Again, an AD712 is used to buffer the reference input terminals.

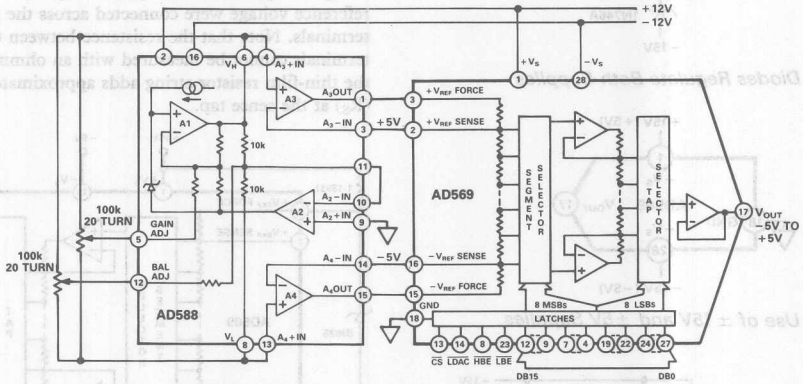


Figure 11. Ultralow Drift ±5V Tracking Reference

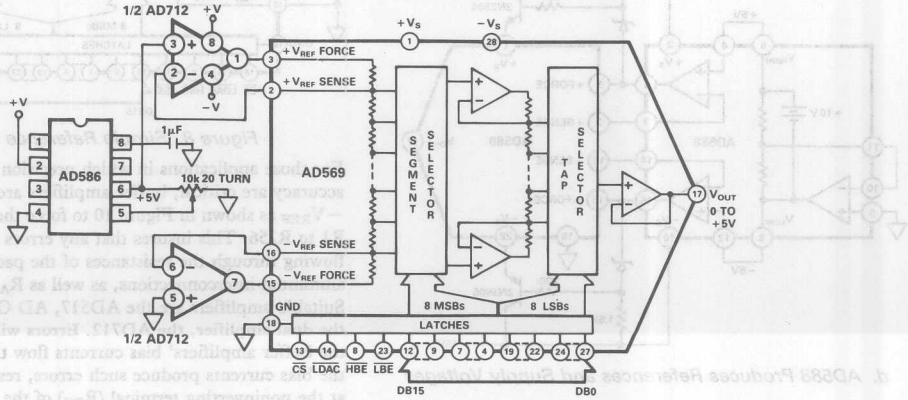


Figure 12. Low-Cost ±5V Reference

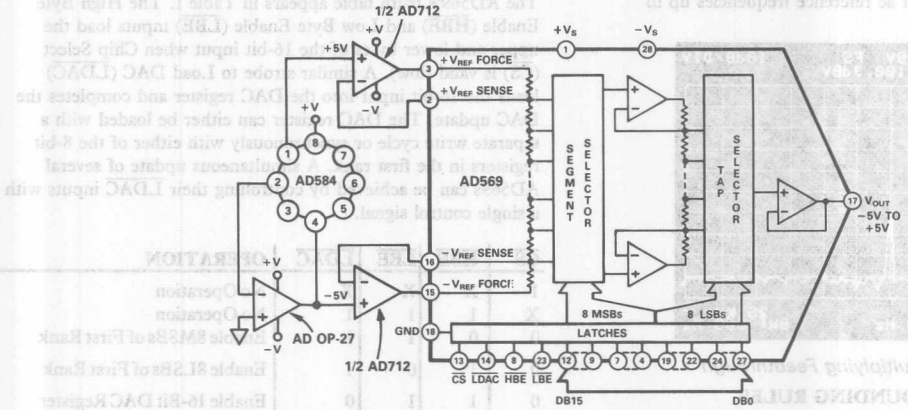
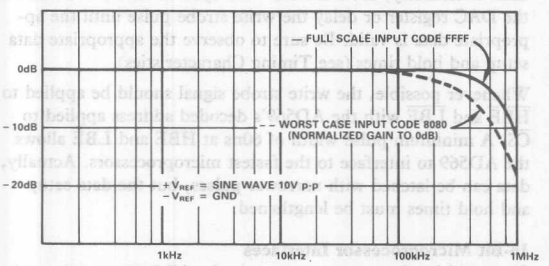


Figure 13. Low-Cost ±5V Tracking Reference

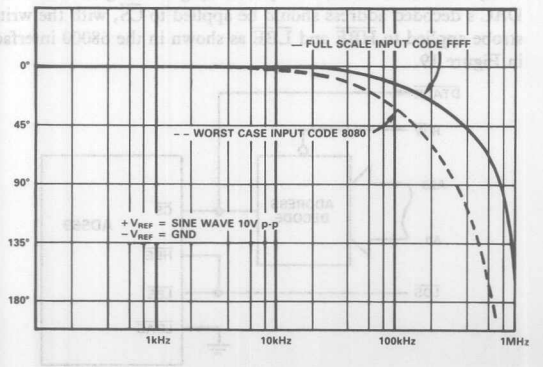
MULTIPLYING PERFORMANCE

Figure 14 illustrates the gain and phase characteristics of the AD569 when operated in the multiplying mode. Full-power bandwidth is shown in Figure 14a and the corresponding phase shift is shown in Figure 14b. Performance is plotted for both a full-scale input of $FFFF_H$ and an input of 8080_H. An input represents worst-case conditions because it places the buffer taps at the midpoints of both dividers. Figure 15 illustrates the AD569's ability to resolve 16-bits (where 1LSB is 96dB below full scale) while keeping the noise floor below −130dB with an ac reference of 1V rms at 200Hz.

Multiplying feedthrough is due to capacitive coupling between the reference inputs and the output. As shown in Figure 16,

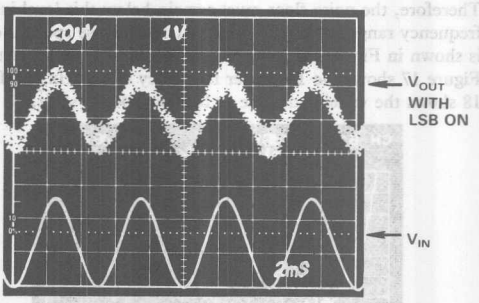


a. Bandwidth

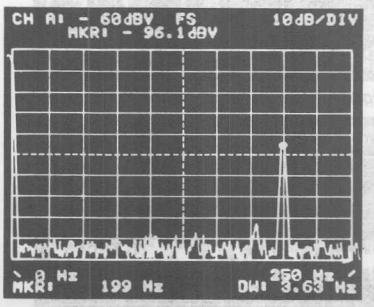


b. Phase Shift

Figure 14. Full Power Multiplying Performance



a. Time Domain



b. Frequency Domain

Figure 15. Multiplying Mode Performance (Input Code 0001_H)

remains below −100dB at ac reference frequencies up to 10kHz.

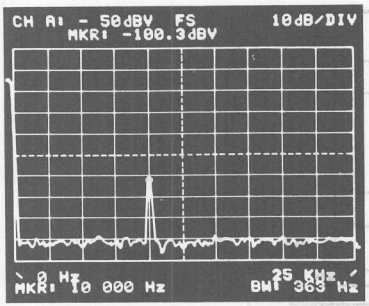


Figure 16. Multiplying Feedthrough

BYPASSING AND GROUNDING RULES

It is generally considered good engineering practice to use bypass capacitors on the device supply voltage pins and to insert small valued resistors in the supply lines to provide a measure of decoupling between various circuits in a system. For the AD569, bypass capacitors of at least 4.7μF and series resistors of 10Ω are recommended. The supply voltage pins should be decoupled to Pin 18.

NOISE

In high-resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 152μV (−96dB). Therefore, the noise floor must remain below this level in the frequency ranges of interest. The AD569's noise spectral density is shown in Figures 17 and 18. The lowband noise spectrum in Figure 17 shows the 1/f corner frequency at 1.2kHz and Figure 18 shows the wideband noise to be below 40nV/$\sqrt{\text{Hz}}$.

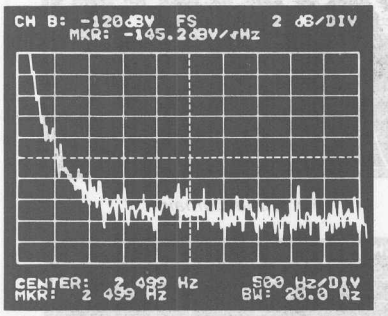


Figure 17. Lowband Noise Spectrum

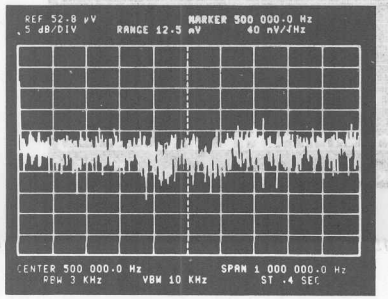


Figure 18. Wideband Noise Spectrum

The AD569's truth table appears in Table I. The High Byte Enable ($\overline{\text{HBE}}$) and Low Byte Enable ($\overline{\text{LBE}}$) inputs load the upper and lower bytes of the 16-bit input when Chip Select ($\overline{\text{CS}}$) is valid (low). A similar strobe to Load DAC ($\overline{\text{LDAC}}$) loads the 16-bit input into the DAC register and completes the DAC update. The DAC register can either be loaded with a separate write cycle or synchronously with either of the 8-bit registers in the first rank. A simultaneous update of several AD569s can be achieved by controlling their $\overline{\text{LDAC}}$ inputs with a single control signal.

$\overline{\text{CS}}$	$\overline{\text{HBE}}$	$\overline{\text{LBE}}$	$\overline{\text{LDAC}}$	OPERATION
1	X	X	X	No Operation
X	1	1	1	No Operation
0	0	1	1	Enable 8MSBs of First Rank
0	1	0	1	Enable 8LSBs of First Rank
0	1	1	0	Enable 16-Bit DAC Register
0	0	0	0	All Latches Transparent

Table I. AD569 Truth Table

All four control inputs latches are level-triggered and active low. When the DAC register is loaded directly from a bus, the data at the digital inputs will be reflected in the output any time $\overline{\text{CS}}$, $\overline{\text{LDAC}}$, $\overline{\text{LBE}}$ and $\overline{\text{HBE}}$ are low. Should this not be the desired case, bring $\overline{\text{LDAC}}$ (or $\overline{\text{HBE}}$ or $\overline{\text{LBE}}$) high before changing the data. Alternately, use a second write cycle to transfer the data to the DAC register or delay the write strobe pulse until the appropriate data is valid. Be sure to observe the appropriate data setup and hold times (see Timing Characteristics).

Whenever possible, the write strobe signal should be applied to $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ with the AD569's decoded address applied to $\overline{\text{CS}}$. A minimum pulse width of 60ns at $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ allows the AD569 to interface to the fastest microprocessors. Actually, data can be latched with narrower pulses, but the data setup and hold times must be lengthened.

16-Bit Microprocessor Interfaces

Since 16-bit microprocessors supply the AD569's complete 16-bit input in one write cycle, the DAC register is often unnecessary. If so, it should be made transparent by grounding $\overline{\text{LDAC}}$. The DAC's decoded address should be applied to $\overline{\text{CS}}$, with the write strobe applied to $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ as shown in the 68000 interface in Figure 19.

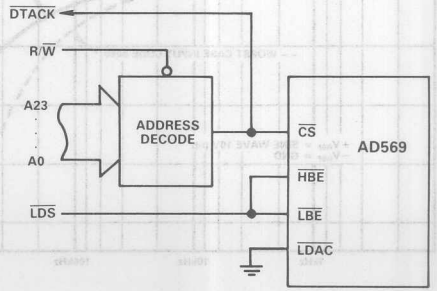


Figure 19. AD569/68000 Interface

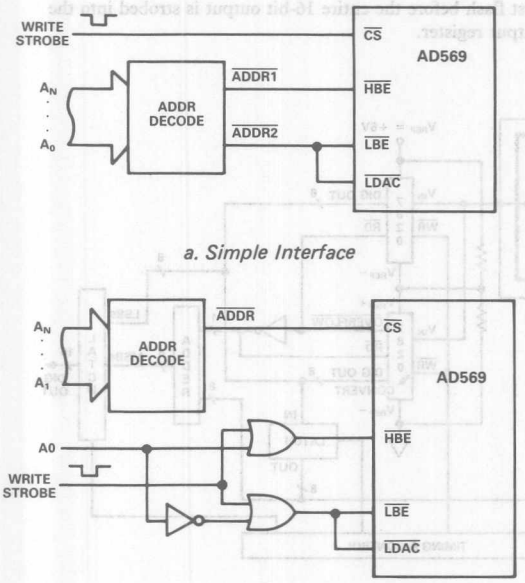


Figure 20. 8-Bit Microprocessor Interface

8-Bit Microprocessor Interfaces

Since 8-bit microprocessors require two write cycles to provide the AD569's 16-bit input, the DAC register must be utilized. It is most often loaded as the second byte enters the first rank of latches. This synchronous load method, shown in Figure 20, requires $\overline{\text{LDAC}}$ to be tied to either $\overline{\text{LBE}}$ or $\overline{\text{HBE}}$, depending upon the byte loading sequence. In either case, the propagation delay through the first rank gives rise to longer timing requirements as shown in Figure 2. If the DAC register ($\overline{\text{LDAC}}$) is controlled separately using a third write cycle, the minimum write pulse on $\overline{\text{LDAC}}$ is 70ns, as shown in Figure 1.

Two basic methods exist for interfacing the AD569 to an 8-bit microprocessor's address and control buses. In either case, at least one address line is needed to differentiate between the upper and lower bytes of the first rank ($\overline{\text{HBE}}$ and $\overline{\text{LBE}}$). The simplest method involves applying the two addresses directly to $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ and strobing the data using $\overline{\text{CS}}$ as shown in Figure 20a. However, the minimum pulse width on $\overline{\text{CS}}$ is 70ns with a minimum data setup time of 60ns. If operation with a shorter pulse width is required, the base address should be applied to $\overline{\text{CS}}$ with an address line gated with the strobe signal to supply the $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ inputs (see Figure 20b). However, since the write pulse sees a propagation delay, the data still must remain valid at least 20ns after the rising edge of the delayed write pulse.

2

OUTPUT SETTLING

The AD569's output buffer amplifier typically settles to within ±0.001% FS of its final value in 3μs for a 10V step. Figure 21 shows settling for negative and positive full-scale steps with no load applied. Capable of sourcing or sinking 5mA, the output buffer can also drive loads of 1kΩ and 1000pF without loss of stability. Typical settling to 0.001% under these worst-case conditions is 4μs, and is guaranteed to be a maximum of 6μs. The plots of Figure 21 were generated using the settling test procedure developed specifically for the AD569.

Subranging 16-Bit ADC

The subranging ADC shown in Figure 22 completes a conversion in less than 20μs, including the sample-hold amplifier's sample time. The sample-hold amplifier is allocated 5μs to settle to 16 bits.

Before the first flash, the analog input signal is routed through the AD630 at a gain of +1. The lower AD7820 quantizes the signal to the 8-bit level within 1.4μs, and the 8-bit result is routed to the AD569 via a digital latch which holds the 8-bit word for the AD569 and the output logic.

The AD569's reference polarity is reversed so that a full-scale output is −5V and zero scale is 0V, thereby subtracting an 8-bit approximation from the original sampled signal. The residue from the analog subtraction is then quantized by the second 8-bit flash conversion to recover the 8LSBs. Even though only the AD569's upper 8MSBs are used, the AD569's accuracy defines the A/D converter's overall accuracy. Any errors are directly reflected in the output.

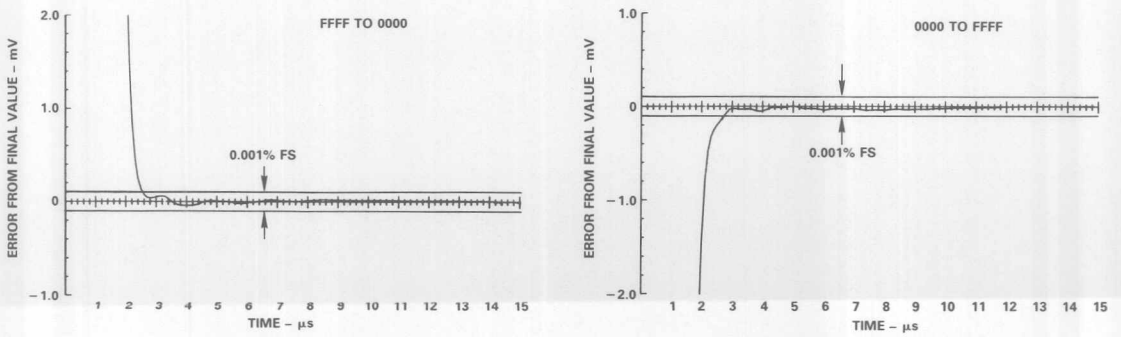


Figure 21. Full-Scale Output Settling

Preceding the second flash, the residue signal must be amplified by a factor of 256. The OP-37 provides a gain of 25.6 and the AD630 provides another gain of 10. In this case, the AD630 acts as a gain element as well as a channel control switch. The second flash conversion yields a 9-bit word. This provides one extra bit of overlap for digital correction of any errors that occurred in the first flash. The correction bit is digitally added to the first flash before the entire 16-bit output is strobed into the output register.

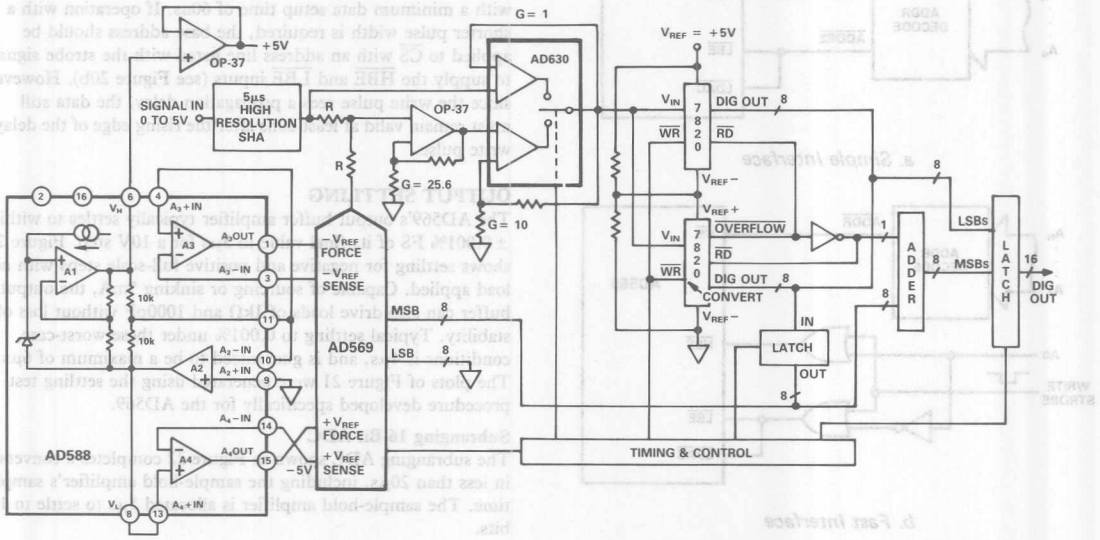


Figure 22. 16-Bit Subranging ADC

Monolithic 12-Bit Quad DAC

AD664

FEATURES

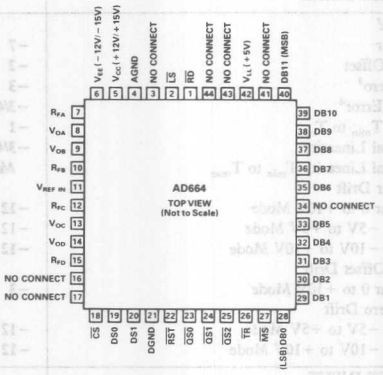
- Four Complete Voltage Output DACs
- Data Register Readback Feature
- "Reset to Zero" Override
- Multiplying Operation
- Double-Buffered Latches
- Surface Mount and DIP Packages
- MIL-STD-883 Compliant Versions Available

APPLICATIONS

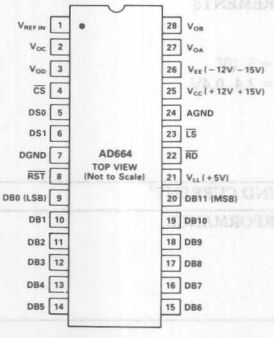
- Automatic Test Equipment
- Robotics
- Process Control
- Disk Drives
- Instrumentation
- Avionics

PIN CONFIGURATIONS

44-Pin Package



28-Pin DIP Package



PRODUCT DESCRIPTION

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

PRODUCT HIGHLIGHTS

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.
4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2LSB at room temperature and 3/4LSB maximum for the K, B and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have tristate outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.
10. The AD664 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD664/883B data sheet for detailed specifications.

AD664—SPECIFICATIONS (V_{LL} = +5V, V_{CC} = +15V, V_{REF} = −15V, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12	12		*	*	Bits
ANALOG OUTPUT							
Voltage Range[1]							
UNI Versions	0		V_{CC} − 2.0[2]	*		*	Volts
BIP Versions	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
Output Current	5			*			mA
Load Resistance		2			*		kΩ
Load Capacitance			500			*	pF
Short-Circuit Current		25	40		*	*	mA
ACCURACY							
Gain Error	−7	±3	7	−5	±2	5	LSB
Unipolar Offset	−2	±1/2	2	−1	±1/4	1	LSB
Bipolar Zero[3]	−3	±3/4	3	−2	±1/2	2	LSB
Linearity Error[4]	−3/4	±1/2	3/4	−1/2	±1/4	1/2	LSB
Linearity T_{min} to T_{max}	−1	±3/4	1	−3/4	±1/2	3/4	LSB
Differential Linearity	−3/4		3/4	−1/2		1/2	LSB
Differential Linearity T_{min} to T_{max}	Monotonic @ All Temperatures			Monotonic @ All Temperatures			
Gain Error Drift							
Unipolar 0 to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR[5]/°C
Bipolar −5V to +5V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Unipolar Offset Drift							
Unipolar 0 to +10V Mode	−3	±1.5	3	−2	±1	2	ppm of FSR/°C
Bipolar Zero Drift							
Bipolar −5V to +5V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2.6	*		*	kΩ
Voltage Range[6]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
POWER REQUIREMENTS							
V_{LL}	4.5	5.0	5.5	*	*	*	Volts
I_{LL}							
@ V_{IH}, V_{IL} = 5, 0V		0.1	1		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4V		3	6		*	*	mA
V_{CC}/V_{EE}	±11.4		±16.5	*		*	Volts
I_{CC}		12	15		*	*	mA
I_{EE}		15	19		*	*	mA
Total Power		400	525		*	*	mW
ANALOG GROUND CURRENT[7]	−600	±400	+600	*	*	*	μA
MATCHING PERFORMANCE							
Gain[8]	−6	±3	6	−4	±2	4	LSB
Offset[9]	−2	±1/2	2	−1	±1/4	1	LSB
Bipolar Zero[10]	−3	±1	3	−2	±1	2	LSB
Linearity[11]	−1.5	±1/2	1.5	−1	±1/2	1	LSB
CROSSTALK							
Analog			−90			*	dB
Digital			−60			*	dB
DYNAMIC PERFORMANCE (R_L = 2kΩ, C_L = 500pF)							
Settling Time to ±1/2LSB							
Off←Bits→On, GAIN = 1, V_{REF} = 10		8	10		*	*	μs
Settling Time to ±1/2LSB							
−10←V_{REF}→10V, GAIN = 1, Bits On		10			*		μs
Glitch Impulse			500			*	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough @ 1kHz		−75			*		dB
Reference −3dB Bandwidth		70			*		kHz
POWER SUPPLY GAIN SENSITIVITY							
11.4V←V_{CC}→16.5V		±2	±5		*	*	ppm/%
−16.5V←V_{EE}→−11.4V		±2	±5		*	*	ppm/%
4.5V←V_{LL}→5.5V		±2	±5		*	*	ppm/%

Model	JN/JP/AD/AJ/SD Min	Typ	Max	KN/KP/BD/BJ/BE/TD/TE Min	Typ	Max	Units
DIGITAL INPUTS							
V_{IH}	2.0			*			Volts
V_{IL}	0		0.8	*		*	Volts
Data Inputs							
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	*	*	*	µA
$\overline{CS}$/DS0/DS1/$\overline{RST}$/$\overline{RD}$/$\overline{LS}$							
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
$\overline{MS}$/$\overline{TR}$[12]							
I_{IH} @ $V_{IN} = V_{LL}$	−10	5	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	−5	0	*	*	*	µA
$\overline{QS0}$/$\overline{QS1}$/$\overline{QS2}$[12]							
I_{IH} @ $V_{IN} = V_{LL}$	−10	5	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	*	*	*	µA
DIGITAL OUTPUTS							
V_{OL} @ 1.6mA Sink			0.4			*	Volts
V_{OH} @ 0.5mA Source	2.4			*			Volts
TEMPERATURE RANGE							
JN/JP/KN/KP	0		+70	*		*	°C
AD/AJ/BD/BJ/BE	−40		+85	*		*	°C
SD/TD/TE	−55		+125	*		*	°C

NOTES

[1]A minimum power supply of ±12.0V is required for 0 to +10V and ±10V operation. A minimum power supply of ±11.4V is required for −5V to +5V operation.

[2]For V_{CC}<12V and V_{EE}>−12V. Voltage not to exceed 10V maximum.

[3]Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.

[4]Linearity error is defined as the maximum deviation of the actual DAC output from the ideal output (a straight line drawn from 0 to F.S. −1LSB).

[5]FSR means Full-Scale Range and is 20V for ±10V range and 10V for ±5V range.

[6]A minimum power supply of ±12.0V is required for a 10V reference voltage.

[7]Analog Ground Current is input code dependent.

[8]Gain error matching is the largest difference in gain error between any two DACs in one package.

[9]Offset error matching is the largest difference in offset error between any two DACs in one package.

[10]Bipolar zero error matching is the largest difference in bipolar zero error between any two DACs in one package.

[11]Linearity error matching is the difference in the worst case linearity error between any two DACs in one package.

[12]44-pin versions only.

*Specifications same as JN/JP/AD/AJ/SD.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those test are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades except where noted.)

V_{LL} to DGND	0 to +7V
V_{CC} to DGND	0 to +18V
V_{EE} to DGND	−18V to 0V
Soldering	+300°C, 10sec
Power Dissipation	1000mW
AGND to DGND	−1V to +1V
Reference Input	$V_{REF} \leq 10V$ and $V_{REF} \leq (V_{CC} - 2V, V_{EE} + 2V)$
V_{CC} to V_{EE}	0 to +36V
Digital Inputs	−0.3V to +7V
Analog Outputs	Indefinite Shorts to V_{CC}, V_{LL}, V_{EE} and GND

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



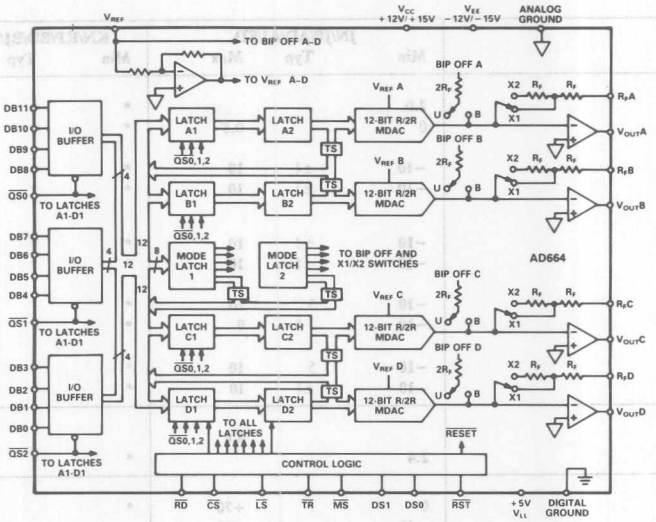


Figure 1a. 44-Pin Block Diagram

FUNCTIONAL DESCRIPTION

The AD664 combines four complete 12-bit voltage output D/A converters with a fast, flexible digital input/output port on one monolithic chip. It is available in two forms, a 44-pin version shown in Figure 1a and a 28-pin version shown in Figure 1b.

44-Pin Versions

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors which are laser-trimmed to achieve 1/2LSB linearity and guaranteed monotonicity. The output amplifier combines the best features of the bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10μs and each output can drive a 5mA, 500pF load. Short-circuit protection allows indefinite shorts to V_{LL}, V_{CC}, V_{EE} and GND. The output and span resistor pins are available separately. This feature allows a user to insert current-boosting elements to increase the drive capability of the system, as well as to overcome parasitics.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows the AD664 to be interfaced with most microprocessors. Through this interface, the wide variety of features on each chip may be accessed. For example, the input data for each DAC is programmed by way of 4-, 8-, 12- or 16-bit words. The double-buffered input structure of this latch allows all four DACs to be updated simultaneously. A readback feature allows the internal registers to be read back through the same digital port, as either 4-, 8- or 12-bit words. When disabled, the readback drivers are placed in a high impedance (tristate) mode. A TRANSPARENT mode allows the input data to pass straight through both ranks of input registers and appear at the DAC with a minimum of delay. One D/A may be placed in the transparent mode at a time, or all four may be made transparent at once. The MODE SELECT feature allows the output range and mode of the DACs to be selected via the data bus inputs. An internal mode select register stores the selections. This register may also be read back to check its contents. A RESET-TO-ZERO feature allows all DACs to be reset to 0 volts out by strobing a single pin.

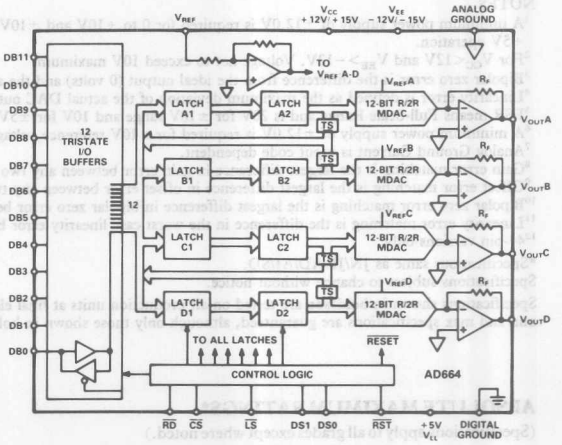


Figure 1b. 28-Pin Block Diagram

28-Pin Versions

The 28-pin versions are dedicated versions of the 44-pin AD664. Each offers a reduced set of features from those offered in the 44-pin version. This accommodates the reduced number of package pins available. Data is written and read with 12-bit words only. Output range and mode select functions are also not available in 28-pin versions. As an alternative, users specify either the UNI (unipolar, 0 to V_{REF}) models or the BIP (bipolar, $-V_{REF}$ to V_{REF}) models depending on the application requirements. Finally, the transparent mode is not available on the 28-pin versions.

	Mode = UNI	Mode = BIP
Gain = 1	000000000000 = 0V 100000000000 = $V_{REF}/2$ 111111111111 = V_{REF} – 1LSB	000000000000 = $-V_{REF}/2$ 100000000000 = 0V 111111111111 = $V_{REF}/2$ – 1LSB
Gain = 2	000000000000 = 0V 100000000000 = V_{REF} 111111111111 = $2 \times V_{REF}$ – 1LSB	000000000000 = $-V_{REF}$ 100000000000 = 0V 111111111111 = $+V_{REF}$ – 1LSB

Table I. Transfer Functions

2

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS – 1LSB) for any bit conbination. This is also referred to as relative accuracy. The AD664 is laser-trimmed to typically maintain linearity errors at less than ± 1/4LSB.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD664 are monotonic over their full operating temperature range.

DIFFERENTIAL LINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at 25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10V full-scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (V_{REF} = 10V, Gain = 1, 1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be – 1.83mV, or – 3/4LSB.

GAIN ERROR: DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

UNIPOLAR OFFSET ERROR: Unipolar offset error is the difference between the ideal output (0V) and the actual output of a DAC when the input is loaded with all "0s" and the MODE is unipolar.

BIPOLAR ZERO ERROR: Bipolar zero error is the difference between the ideal output (0V) and the actual output of a DAC when the input code is loaded with the MSB = "1" and the rest of the bits = "0" and the MODE is bipolar.

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

CROSSTALK: Crosstalk is the change in an output caused by a change in one or more of the other outputs. It is due to capacitive and thermal coupling between outputs.

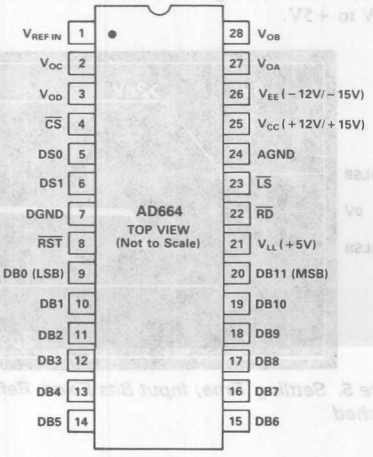
REFERENCE FEEDTHROUGH: The portion of an ac reference signal that appears at an output when all input bits are low. Feedthrough is due to capacitive coupling between the reference input and the output. It is specified in decibels at a particular frequency.

REFERENCE 3dB BANDWIDTH: The frequency of the ac reference input signal at which the amplitude of the full-scale output response falls 3dB from the ideal response.

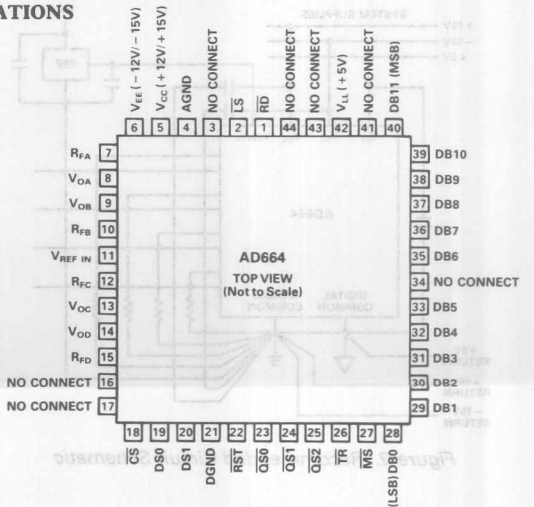
GLITCH IMPULSE: Glitch impulse is an undesired output voltage transient caused by asymmetrical switching times in the switches of a DAC. These transients are specified by their net area (in nV-sec) of the voltage vs. time characteristic.

PIN CONFIGURATIONS

28-Pin DIP Package



44-Pin Package



ANALOG CIRCUIT CONSIDERATIONS

Grounding Recommendations

The AD664 has two pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. A unique internal design has resulted in low analog ground current. This greatly simplifies management of ground current and the associated induced voltage drops. The analog ground pin should be connected to the analog ground point in the system. The external reference and any external loads should also be returned to analog ground.

The digital ground pin should be connected to the digital ground point in the circuit. This pin returns current from the logic portions of the AD664 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection be broken or otherwise disconnected, then two diodes should be connected between the analog and digital ground pins of the AD664 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD664 requires three power supplies for proper operation. V_{LL} powers the logic portions of the device and requires +5 volts. V_{CC} and V_{EE} power the remaining portions of the circuitry and require +12V to +15V and −12V to −15V, respectively. V_{CC} and V_{EE} must also be a minimum of two volts greater then the maximum reference and output voltages anticipated.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. V_{LL} should be bypassed to digital ground. V_{CC} and V_{EE} should be decoupled to analog ground.

Driving the Reference Input

The reference input of the AD664 can have an impedance as low as 1.3kΩ. Therefore, the external reference voltage must be able to source up to 7.7mA of load current. Suitable choices include the 5V AD586, the 10V AD587 and the 8.192V AD689.

The architecture of the AD664 derives an inverted version of the reference voltage for some portions of the internal circuitry. This means that the power supplies must be at least 2V greater than both the external reference and the inverted external reference.

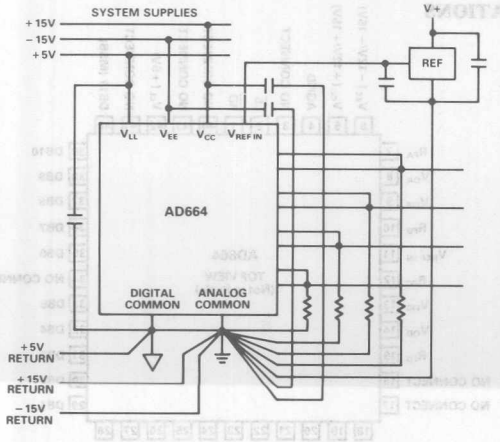


Figure 2. Recommended Circuit Schematic

Output Considerations

Each DAC output can source or sink 5mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40mA. Load capacitance of up to 500pF can be accomodated with no effect on stability. Should an application require additional output current, a current boosting element can be inserted into the output loop with no sacrifice in accuracy. Figure 3 details this method.

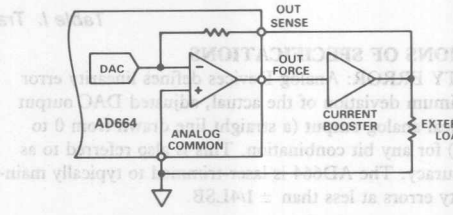


Figure 3. Current-Boosting Scheme

AD664 output voltage settling time is 10μs maximum. Figure 4 shows the output voltage settling time with a fixed 10V reference, gain = 1 and all bits switched from 1 to 0.

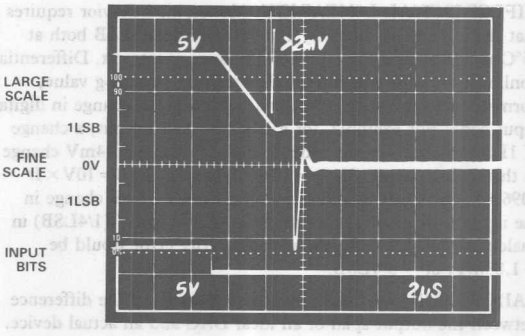


Figure 4. Settling Time; All Bits Switched from On to Off

Alternately, Figure 5 shows the settling characteristics when the reference is switched and the input bits remain fixed. In this case, all bits are "on", the gain is 1 and the reference is switched from −5V to +5V.

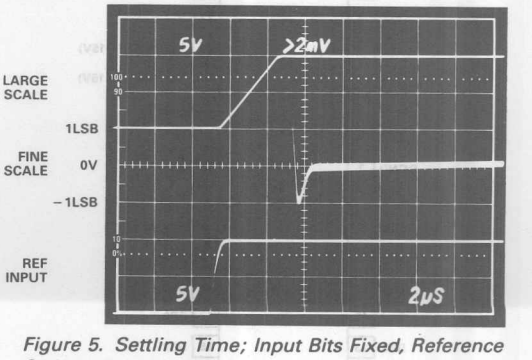


Figure 5. Settling Time; Input Bits Fixed, Reference Switched

Multiplying Mode Performance

Figure 6 illustrates the typical open-loop gain and phase performance of the output amplifiers of the AD664.

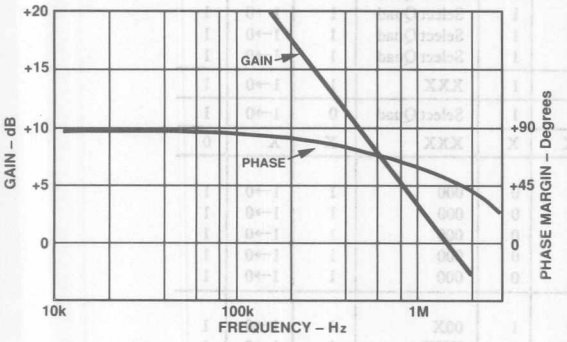


Figure 6. Gain and Phase Performance of AD664 Outputs

Crosstalk

Crosstalk is a spurious signal on one DAC output caused by a change in the output of one or more of the other DACs. Crosstalk can be induced by capacitive, thermal or load current induced feedthrough. Figure 7 shows typical crosstalk. DAC B is set to output 0 volts. The outputs of DAC A, C and D switch 2kΩ loads from 10V to 0V. The first disturbance in the output of DAC B is caused by digital feedthrough from the input data lows. The second disturbance is caused by analog feedthrough from the other DAC outputs.

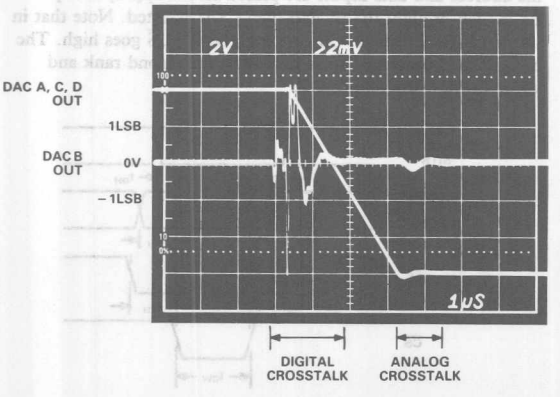


Figure 7. Output Crosstalk

Output Noise

Wideband output noise is shown in Figure 8. This measurement was made with a 7MHz noise bandwidth, gain = 1 and all bits on. The total rms noise is approximately one fifth the visual peak-to-peak noise.

DIGITAL INTERFACE

As Table II shows, the AD664 makes a wide variety of operating modes available to the user. These modes are accessed or programmed through the high-speed digital port of the quad DAC. On-board registers program and store the DAC input codes and

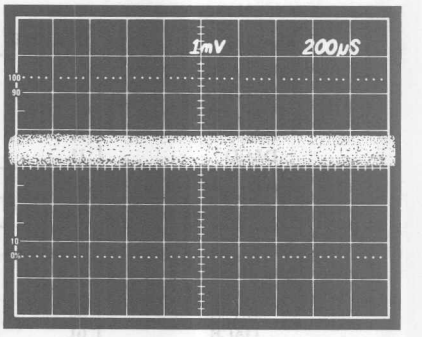


Figure 8. Typical Output Noise

the DAC operating mode data. All registers are double-buffered to allow for simultaneous updating of all outputs. Register data may be read back to verify the respective contents. The digital port also allows transparent operation. Data from the input pins can be sent directly through both ranks of latches to the DAC.

Partial address decoding is performed by the DS0, DS1, $\overline{QS0}$, $\overline{QS1}$ and $\overline{QS2}$ address bits. $\overline{QS0}$, $\overline{QS1}$ and $\overline{QS2}$ allow the 44-pin versions of the AD664 to be addressed in 4-bit nibble, 8-bit byte or 12-bit parallel words.

The $\overline{RST}$ pin provides a simple method to reset all output voltages to zero. Its advantages are speed and low software overhead.

INPUT DATA

In general, two types of data will be input to the registers of the AD664, input code data and mode select data. Input code data sets the DAC inputs while the mode select data sets the gain and range of each DAC.

The versatile I/O port of the AD664 allows many different types of data input schemes. For example, the input code for just one of the DACs may be loaded and the output may or may not be updated. Or, the input codes for all four DACs may be written, and the outputs may or may not be updated.

The same applies for MODE SELECTION. The mode of just one or many of the DACs may be rewritten and the user can choose to immediately update the outputs or wait until a later time to transfer the mode information to the outputs.

A user may also write both input code and mode information into their respective first ranks and then update all second ranks at once.

Finally, transparent operation allows data to be transferred from the inputs to the outputs using a single control line. This feature is useful, for example, in a situation where one of the DACs is used in an A/D converter. The SAR register could be connected directly to a DAC by using the transparent mode of operation. Another use for this feature would be during system calibration where the endpoints of the transfer function of each DAC would be measured. For example, if the full-scale voltages of each DAC were to be measured, then by making all four DACs transparent and putting all "1s" on the input port, all four DACs would be at full-scale. This requires far less software overhead than loading each register individually.

Table II. AD664 Digital Truth Table

Function	DS1, DS0	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}$, $\overline{1}$, $\overline{2^1}$	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load 1st Rank (data)								
DACA	00	0	1	1	Select Quad	1	1→0	1
DACB	01	0	1	1	Select Quad	1	1→0	1
DACC	10	0	1	1	Select Quad	1	1→0	1
DACD	11	0	1	1	Select Quad	1	1→0	1
Load 2nd Rank (data)	XX	1	1	1	XXX	1	1→0	1
Readback 2nd Rank (data)	Select D/A	X	1	1	Select Quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent[1]								
All DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
Mode Select[1,2]								
1st Rank	XX	0	0	1	00X	1	1→0	1
2nd Rank	XX	1	0	1	XXX	1	1→0	1
Readback Mode[1]	XX	X	0	1	00X	0	1→0	1

Notes: X = don't care.
[1]For 44-pin versions only. Allow the AD664 to be addressed in 4-bit nibble, 8-bit byte or 12-bit parallel words.
[2]For $\overline{MS}$, $\overline{TR}$, $\overline{LS}$ = 0, a $\overline{MS}$ 1st write occurs.

The following sections detail the timing requirements for various data loading schemes. All of the timing specifications shown assume V_{IH} = 2.4V, V_{IL} =0.4V, V_{CC} = +15V, V_{EE} = −15V and V_{LL} = +5V.

Load and Update One DAC Output

In this first example, the object is simply to change the output of one of the four DACs on the AD664 chip. The procedure is to select the address bits that indicate the DAC to be programmed, pull LATCH SELECT($\overline{LS}$) low, pull CHIP SELECT($\overline{CS}$) low, release $\overline{LS}$ and then release $\overline{CS}$. When $\overline{CS}$ goes low, data enters the first rank of the input latch. As soon as $\overline{LS}$ goes high, the data is transferred into the second rank and produces the new output voltage. During this transfer, $\overline{MS}$, $\overline{TR}$, $\overline{RD}$ and $\overline{RST}$ should be held high.

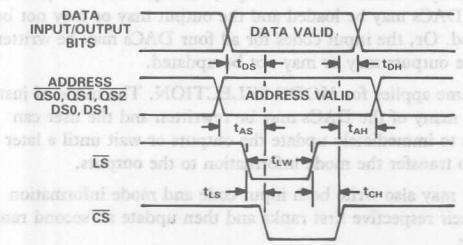


Figure 9a. Update Output of a Single DAC

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{LS}*	0	0
t_{DS}	0	0
t_{DH}	0	0
t_{LW}	50	60
t_{CH}	30	50
t_{AS}	0	0
t_{AH}	0	0

*FOR $t_{LS} > 0$, THE WIDTH OF $\overline{LS}$ MUST BE INCREASED BY THE SAME AMOUNT THAT t_{LS} IS GREATER THAN 0ns.

Figure 9b. Update Output of a Single DAC Timing

Preloading the First Rank of One DAC

In this case, the object is to load new data into the first rank of one of the DACs but *not* the output. As in the previous case, the address and data inputs are placed on the appropriate pins. $\overline{LS}$ is then brought to "0" and then $\overline{CS}$ is asserted. Note that in this situation, however, $\overline{CS}$ goes high before $\overline{LS}$ goes high. The input data is prevented from getting to the second rank and affecting the output voltage.

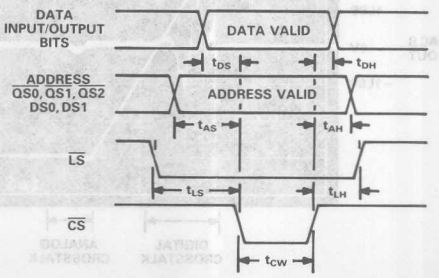


Figure 10a. Preload First Rank of a DAC

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{LS}	0	0
t_{LH}	10	15
t_{CW}	80	100
t_{DS}	0	0
t_{DH}	10	15
t_{AS}	0	0
t_{AH}	10	15

Figure 10b. Preload First Rank of a DAC Timing

This allows the user to "preload" the data to a DAC and strobe it into the output latch at some future time. The user could do this by reproducing the sequence of signals illustrated in the next section.

Update Second Rank of a DAC

Assuming that a new input code had previously been placed into the first rank of the input latches, the user can update the output of the DAC by simply pulling $\overline{CS}$ low while keeping $\overline{LS}$, $\overline{MS}$, $\overline{TR}$, $\overline{RD}$ and $\overline{RST}$ high. Address data is not needed in this case. In reality, all second ranks are being updated by this procedure, but only those which receive data different from that already there would manifest a change. Updating the second rank does not change the contents of the first rank.

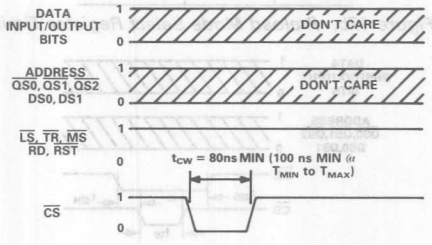


Figure 11. Update Second Rank of a DAC

The same options that exist for individual DAC input loading also exist for multiple DAC input loading. That is, the user can choose to update the first and second ranks of the registers *or* preload the first ranks and then update them at a future time.

Preload Multiple First Rank Registers

The first ranks of the DAC input registers may be preloaded with new input data without disturbing the second rank data. This is done by transferring the data into the first rank by bringing $\overline{CS}$ low while $\overline{LS}$ is low. But $\overline{CS}$ must return high before $\overline{LS}$. This prevents the data from the first rank from getting into the second rank. A simple second rank update cycle as shown in Figure 11 would move the "preloaded" information to the DACs.

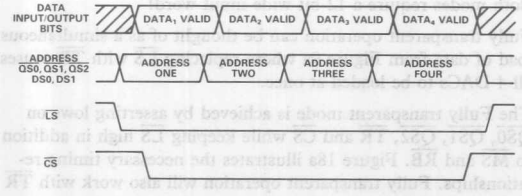


Figure 12. Preload First Rank Registers

Load and Update Multiple DAC Outputs

The following examples demonstrate two ways to update all DAC outputs. The first method involves doing all data transfers during one long $\overline{CS}$ low period. Note that in this case, shown in Figure 13, $\overline{LS}$ returns high before $\overline{CS}$ goes high. Data hold time, relative to an address change, is 70ns. This updates the outputs of all DACs simultaneously.

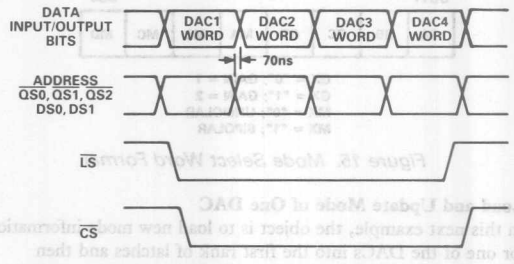


Figure 13. Update All DAC Outputs

The second method involves doing a $\overline{CS}$ assertion (low) and an $\overline{LS}$ toggle separately for each DAC. It is basically a series of preload operations (Figure 10). In this case, illustrated in Figure 14, two $\overline{LS}$ signals are shown. One, labeled $\overline{LS}$, goes high before $\overline{CS}$ returns high. This transfers the "new" input word to the DAC outputs sequentially. The second $\overline{LS}$ signal, labeled Alternate $\overline{LS}$, stays low until $\overline{CS}$ returns high. Using this sequence loads the first ranks with each "new" input word but doesn't update the DAC outputs. To then update all DAC outputs simultaneously would require the signals illustrated in Figure 11.

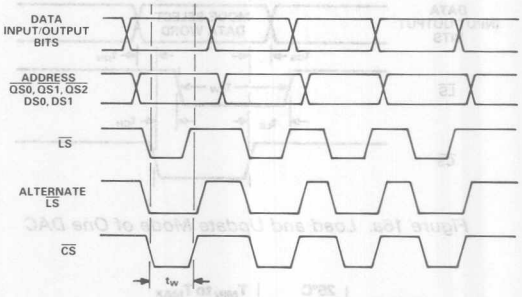


Figure 14. Load and Update Multiple DACs

SELECTING GAIN RANGE AND MODES (44-PIN VERSIONS)

The AD664's mode select feature allows a user to configure the gain ranges and output modes of each of the four DACs. On-board switches take the place of up to eight external relays that would normally be required to accomplish this task. The switches are programmed by the mode select word entered via the data I/O port. The mode select word is eight bits wide and occupies the topmost eight bits of the input word. The last four bits of the input word are "don't cares."

Figure 15 shows the format of the MODE SELECT word. The first four bits determine the gain range of the DAC. When set to be a gain of 1, the output of the DAC spans a voltage of 1 times the reference. When set to a gain of 2, the output of the DAC spans a voltage of 2 times the reference.

The next four bits determine the mode of the DAC. When set to UNIPOLAR, the output goes from 0 to REF or 0 to 2REF. When the BIPOLAR mode is selected, the output goes from −REF/2 to REF/2 or −REF to REF.

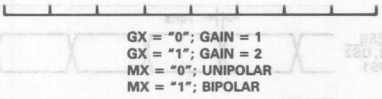


Figure 15. Mode Select Word Format

Load and Update Mode of One DAC

In this next example, the object is to load new mode information for one of the DACs into the first rank of latches and then immediately update the second rank. This is done by putting the new mode information (8-bit word length) onto the databus. Then $\overline{MS}$ and $\overline{LS}$ are pulled low. Following that, $\overline{CS}$ is pulled low. This loads the mode information into the first rank of latches. $\overline{LS}$ is then brought high. This action updates the second rank of latches (and, therefore, the DAC outputs). The load cycle ends when $\overline{CS}$ is brought high.

In reality, this load cycle really updates the modes of all the DACs, but the effect is to only change the modes of those DACs whose mode select information has actually changed.

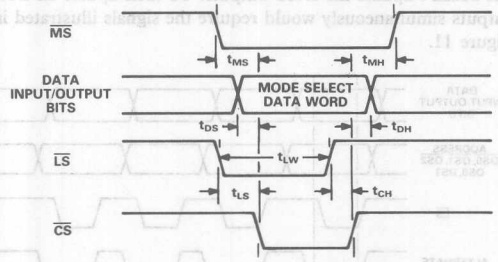


Figure 16a. Load and Update Mode of One DAC

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{MS}	0	0
t_{LS}*	0	0
t_{DS}	0	0
t_{LW}	50	60
t_{CH}	50	80
t_{DH}	0	0
t_{MH}	0	0

*FOR $t_{LS} > 0$, THE WIDTH OF $\overline{LS}$ MUST BE INCREASED BY THE SAME AMOUNT THAT t_{LS} IS GREATER THAN 0ns.

Figure 16b. Load and Update Mode of One DAC Timing

Preloading the Mode Select Register

Mode data can be written into the first rank of the mode select latch without changing the modes currently being used. This feature is useful when a user wants to preload new mode information in anticipation of strobing that in at a future time. Figure 17 illustrates the correct sequence and timing of control signals to accomplish this task.

This allows the user to "preload" the data to a DAC and strobe it into the output latch at some future time. The user could do this by reproducing the sequence of signals illustrated in Figures 17c and 17d.

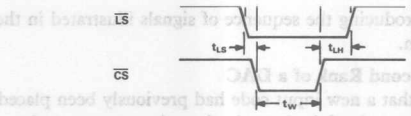


Figure 17a. Preload Mode Select Register

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{MH}	10	15
t_{MS}	0	0
t_{LS}	0	0
t_{DS}	0	0
t_W	80	100
t_{LH}	10	15
t_{DH}	10	15

Figure 17b. Preload Mode Select Register Timing

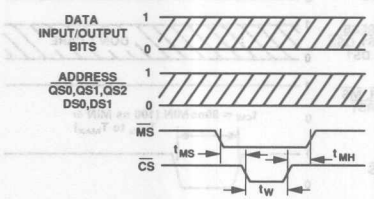


Figure 17c. Update Second Rank of Mode Select Latch

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{MS}	0	0
t_{MH}	0	0
t_W	80	100

Figure 17d. Update Second Rank of Mode Select Latch Timing

Transparent Operation (44-Pin Versions)

Transparent operation allows data from the inputs of the AD664 to be transferred into the DAC registers without the intervening step of being latched into the first rank of latches. Two modes of transparent operation exist, the "partially transparent" mode and a "fully transparent" mode. In the "partially transparent" mode, one of the DACs is transparent while the remaining three continue to use the data latched into their respective input registers. Both modes require a 12-bit wide input word!

Fully transparent operation can be thought of as a simultaneous load of data from Figure 9a where replacing $\overline{LS}$ with $\overline{TR}$ causes all 4 DACs to be loaded at once.

The Fully transparent mode is achieved by asserting lows on $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, $\overline{TR}$ and $\overline{CS}$ while keeping $\overline{LS}$ high in addition to $\overline{MS}$ and $\overline{RB}$. Figure 18a illustrates the necessary timing relationships. Fully transparent operation will also work with $\overline{TR}$ tied low (enabled).

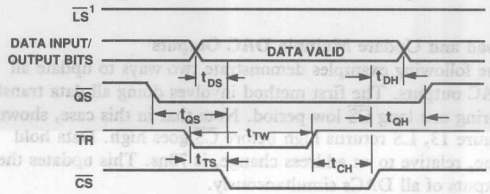


Figure 18a. Fully Transparent Mode

t_{QS}	0	0
t_{TS}*	0	0
t_{tW}	70	80
t_{CH}	80	90
t_{DH}	0	0
t_{QH}	0	0

*FOR $T_{TS} > 0$, THE WIDTH OF $\overline{TR}$ MUST BE INCREASED BY THE SAME AMOUNT THAT T_{TS} IS GREATER THAN 0ns.

Figure 18b. Fully Transparent Mode Timing

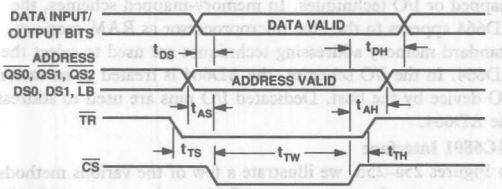


Figure 19a. Partially Transparent

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{DS}	0	0
t_{AS}	0	0
t_{TS}	0	0
t_W	80	90
t_{DH}	10	15
t_{AH}	10	15
t_{TH}	10	15

Figure 19b. Partially Transparent Mode Timing

Partially transparent operation can be thought of as preloading the first rank in Figure 10a without requiring the additional $\overline{CS}$ pulse from Figure 11.

The partially transparent mode is achieved by setting $\overline{CS}$, $\overline{QS0}$, $\overline{QS1}$, $\overline{LS}$, and $\overline{TR}$ low while keeping $\overline{RO}$ and $\overline{MS}$ high. The address of the transparent DAC is asserted on DS0 and DS1. Figure 19a ilustrates the necessary timing relationships. Partially transparent operation will also work with $\overline{TR}$ ties low (enabled).

OUTPUT DATA

Two types of outputs may be obtained from the internal data registers of the AD664 chip, mode select and DAC input code data. Readback data may be in the same forms in which it can be entered; 4-, 8-, and 12-bit wide words (12 bits only for 28-pin versions).

DAC Data Readback

DAC input code readback data is obtained by setting the address of the DAC (DS0, DS1) and Quads ($\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$) on the

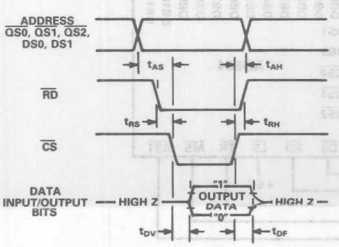


Figure 20a. DAC Input Code Readback

t_{AS}	0	0
t_{RS}	0	0
t_{DV}	130	160
t_{DF}	60	75
t_{AH}	0	0
t_{RH}	0	0

Figure 20b. DAC Input Code Readback Timing

address pins and bringing the $\overline{RD}$ and $\overline{CS}$ pins low. The timing diagram for a DAC code readback operation appears in Figure 20.

Mode Data Readback

Mode data is read back in a similar fashion. By setting $\overline{MS}$, $\overline{QS0}$, $\overline{QS1}$, $\overline{RD}$ and $\overline{CS}$ low while setting $\overline{TR}$ and $\overline{RST}$ high, the mode select word is presented to the I/O port pins. Figure 21 shows the timing diagram for a readback of the mode select data register.

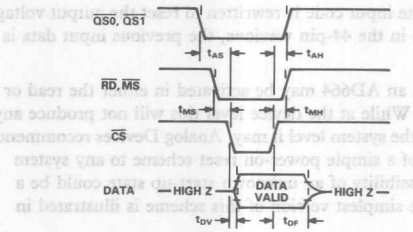


Figure 21a. Mode Data Readback

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_{AS}	0	0
t_{MS}	0	0
t_{DV}	130	160
t_{DF}	60	75
t_{AH}	0	0
t_{MH}	0	0

Figure 21b. DAC Mode Readback Timing

Output Loads

Readback timing is tested with the output loads shown in Figure 22.

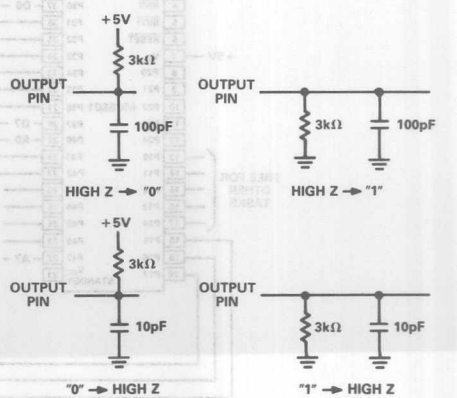


Figure 22. Output Loads

Asynchronous Reset Operation

The asynchronous reset signal shown in Figure 23 may be asserted at any time. A minimum pulse width (t_{RW}) of 90ns is required. The reset feature is designed to return all DAC outputs to 0 volts regardless of the mode or range selected. In the 44-pin versions, the modes are reset to unipolar 10V span (gain of 1), and the input codes are rewritten to be "0s." Previous DAC code and mode information is erased.

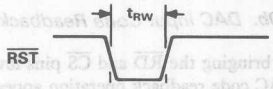


Figure 23a. Asynchronous Reset Operation

SYMBOL	25°C MIN (ns)	T_{MIN} to T_{MAX} MIN (ns)
t_W	70	90

Figure 23b. Asynchronous Reset Operation Timing

In the 28-pin versions of the AD664, the mode remains unchanged, the appropriate input code is rewritten to reset the output voltage to 0 volts. As in the 44-pin versions, the previous input data is erased.

At power-up, an AD664 may be activated in either the read or write modes. While at the device level this will not produce any problems, at the system level it may. Analog Devices recommends the addition of a simple power-on reset scheme to any system where the possibility of an unknown start-up state could be a problem. The simplest version of this scheme is illustrated in Figure 24.

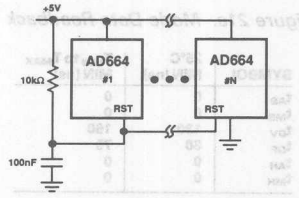


Figure 24. Power-On Reset

It is obvious from inspection that the scheme shown in Figure 24 is only appropriate for systems in which the $\overline{RST}$ is otherwise not used. Should the user wish to use the $\overline{RST}$ pin, an additional logic gate may be included to combine the power-on reset with the reset signal.

INTERFACING THE AD664 TO MICROPROCESSORS

The AD664 is easy to interface with a wide variety of popular microprocessors. Common architectures include processors with dedicated 8-bit data and address buses, an 8-bit bus over which data and address are multiplexed, an 8-bit data and 16-bit address partially muxed, and separate 16-bit data and address buses.

AD664 addressing can be accomplished through either memory-mapped or I/O techniques. In memory-mapped schemes, the AD664 appears to the host microprocessor as RAM memory. Standard memory addressing techniques are used to select the AD664. In the I/O schemes, the AD664 is treated as an external I/O device by the host. Dedicated I/O pins are used to address the AD664.

MC6801 Interface

In Figures 25a–25d, we illustrate a few of the various methods that can be used to connect an AD664 to the popular MC6801 microprocessor. In each of these cases, the MC6801 is intended to be configured in its expanded, nonmultiplexed mode of operation. In this mode, the MC6801 can address 256 bytes of external memory over 8-bit data (Port 3) and 8-bit address (Port 4) buses. Eight general-purpose I/O lines (Port 1) are also available. On-board RAM and ROM provide program and data storage space.

In Figure 25a, the three least significant address bits (P40, P41 and P42) are employed to select the appropriate on-chip addresses for the various input registers of the AD664. Three I/O lines (P17, P16 and P15) are used to select various operating features of the the AD664. IOS and E(nable) are combined to produce an appropriate $\overline{CS}$ signal. This addressing scheme leaves the five most significant address bits and five I/O lines free for other tasks in the system.

Figure 25b shows another way to interface an AD664 to the MC6801. Here we've used the six least significant address lines to select AD664 features and registers. This is a purely memory-mapped scheme while the one illustrated in Figure 25a uses some memory-mapping as well as some dedicated I/O pins. In

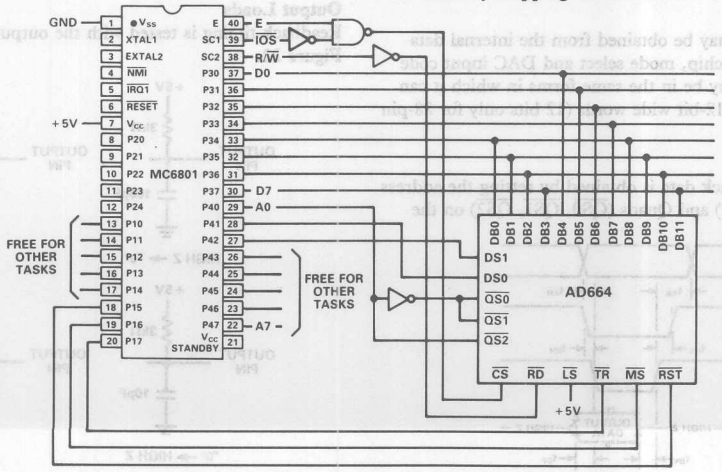


Figure 25a. Simple AD664 to MC6801 Interface

Figure 25b, two address lines and all eight I/O lines remain free for other system tasks.

Expansion of the scheme employed in Figure 25a results in that shown in Figure 25c. Here, two AD664s are connected to an MC6801, providing a total of eight 12-bit, software programmable DACs. Again, the three least significant bits of address are used to select the on-chip registers of the AD664. IOS and E, as well as a fourth address bit, are decoded to provide the appropriate $\overline{CS}$ signals. Four address and five I/O lines remain uncommitted.

A slightly more sophisticated approach to system expansion is illustrated in Figure 25d. Here, a 74LS138 (1-of-8 decoder) is used to address one of the eight AD664s connected to the MC6801. The three least significant address bits are used to select on-chip register and DAC. The next three address bits are used to select the appropriate AD664. IOS and E gate the 74LS138 output.

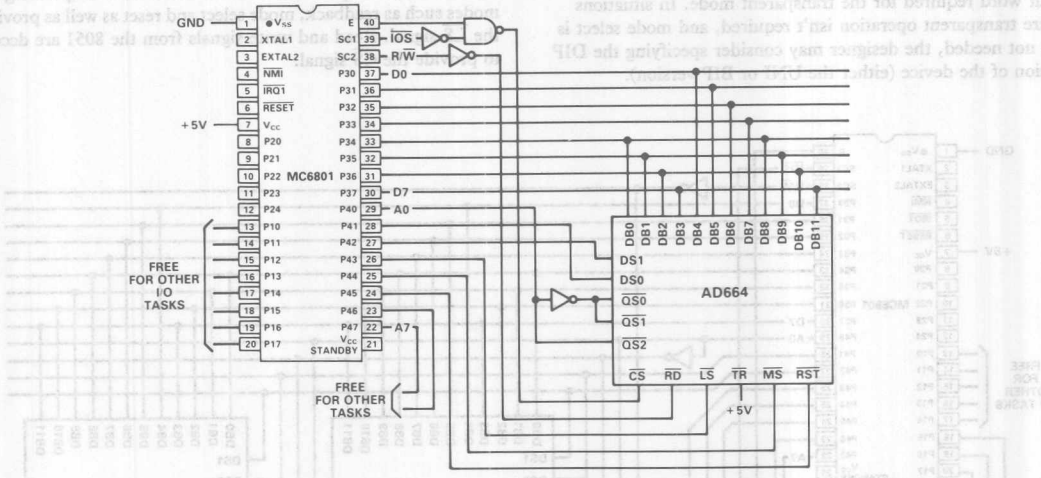


Figure 25b. Alternate AD664 to MC6801 Interface

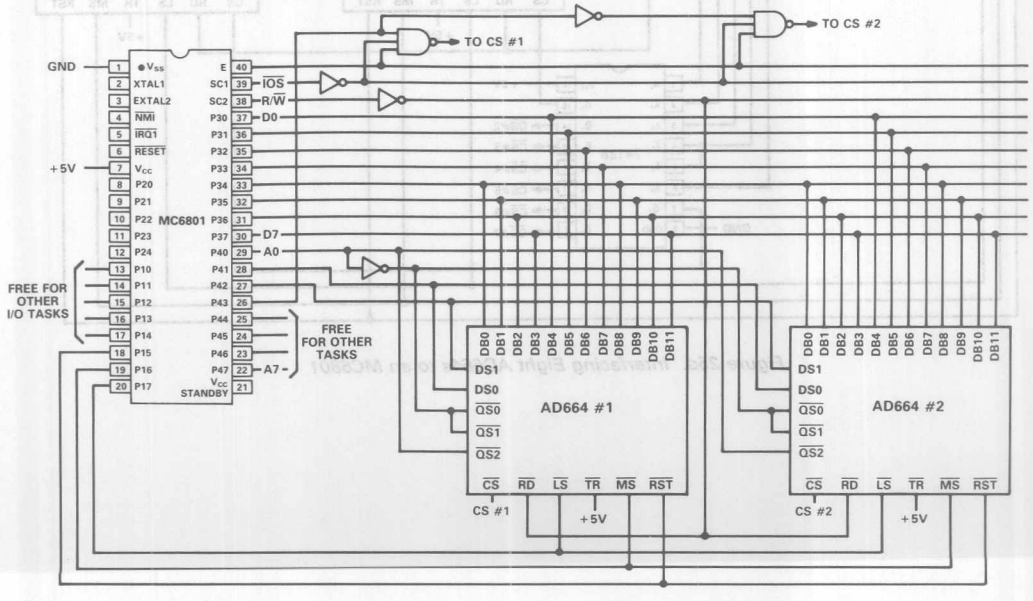


Figure 25c. Interfacing Two AD664s to an MC6801

The schemes in Figure 25 illustrate some of the trade-offs which a designer may make when configuring a system. For example, the designer may use I/O lines instead of address bits or vice versa. This decision may be influenced by other I/O tasks or system expansion requirements. He/she can also choose to implement only a subset of the features available. Perhaps the $\overline{RST}$ pin isn't really needed. Tying that input pin to V_{LOGIC} frees up another I/O or address bit. The same consideration applies to mode select. In all of these cases $\overline{TR}$ is shown tied to V_{LOGIC}, because the MC6801 cannot provide the 12-bit-wide input word required for the transparent mode. In situations where transparent operation isn't required, and mode select is also not needed, the designer may consider specifying the DIP version of the device (either the UNI or BIP version).

Each of the schemes illustrated in Figure 25 operates with an MC6801 at clock rates up to and including 1.5MHz. Similar schemes can be derived for other 8-bit microprocessors and microcontrollers such as the 8051/8086/8088/6502, etc. One such scheme developed for the 8051/AD664 is illustrated in Figure 26.

8051 Interface

Figure 26 shows the AD664 combined with an 8051 µcontroller chip. Three LSBs of address provide the quad and DAC select signals. Control signals from Port 1 select various operating modes such as readback, mode select and reset as well as providing the $\overline{LS}$ signal. Read and write signals from the 8051 are decoded to provide the $\overline{CS}$ signal.

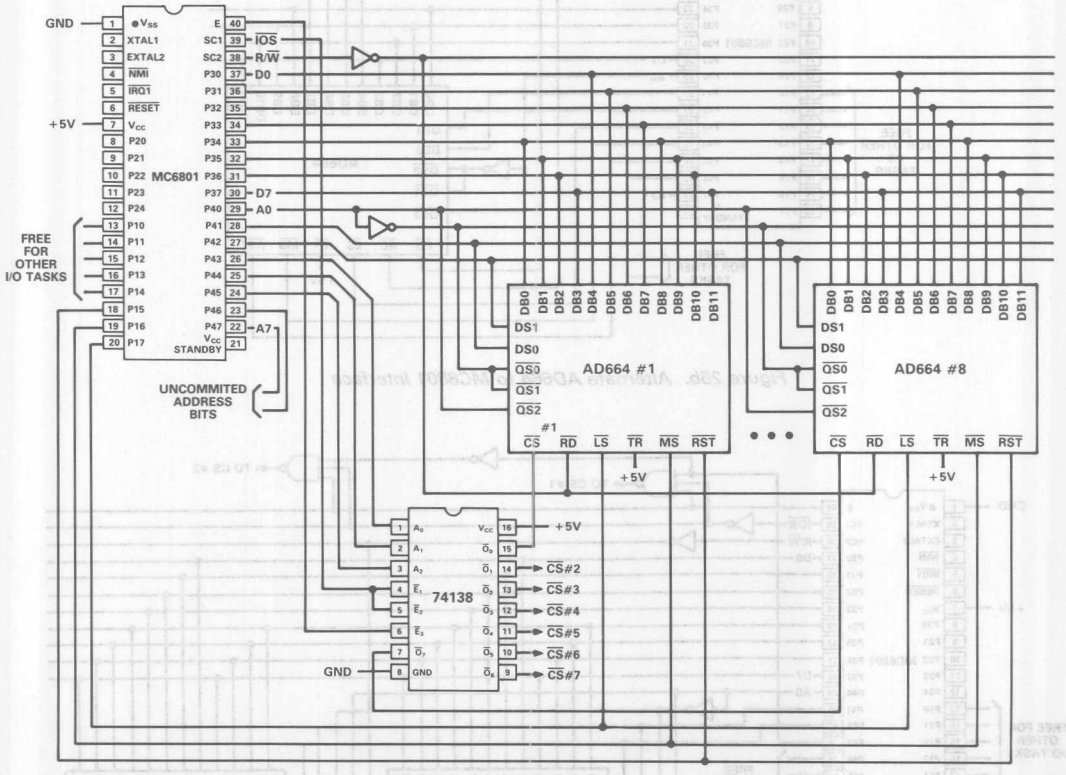


Figure 25d. Interfacing Eight AD664s to an MC6801

IBM PC* Interface

Figure 27 illustrates a simple interface between an IBM PC and an AD664. The three least significant address bits are used to select the Quad and DAC. The next two address bits are used for $\overline{LS}$ and $\overline{MS}$. In this scheme, a 12-bit input word requires two load cycles, an 8-bit word and a 4-bit word. Another write is required to transfer the word or words previously written to the second rank. A 12-bit-wide word again requires at least two read cycles; one for the 8MSBs and four for the LSBs. The page select signal produces a $\overline{CS}$ strobe for any address from 300H to 31FH.

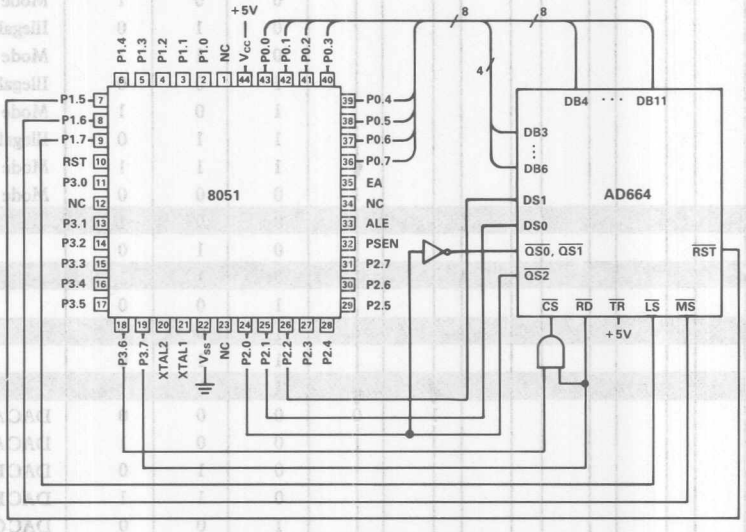


Figure 26. AD664 to 8051 Interface

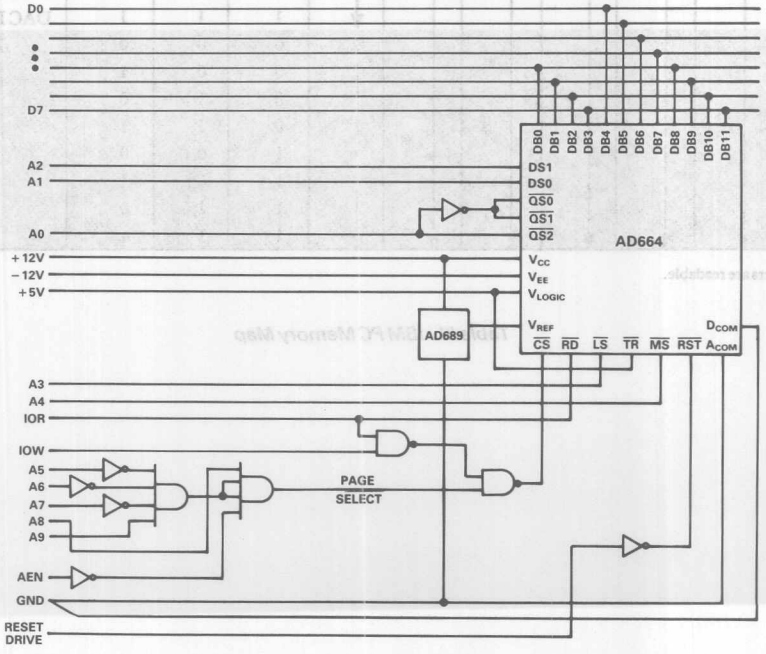


Figure 27. AD664 to IBM PC Interface

*IBM PC is a trademark of International Business Machines Corp.

Table III, shown below details the memory locations and addresses used by this interface.

HEX	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	REGISTER SELECTED
300	1	1	0	0	0	0	0	0	0	0	Illegal Address
301								0	0	1	Mode Select, 1st Rank
302								0	1	0	Illegal Address
303								0	1	1	Mode Select, 1st Rank
304								1	0	0	Illegal Address
305								1	0	1	Mode Select, 1st Rank
306								1	1	0	Illegal Address
307								1	1	1	Mode Select, 1st Rank
308							1	0	0	0	Mode Select, 2nd Rank
309								0	0	1	
30A								0	1	0	
30B								0	1	1	
30C								1	0	0	
30D								1	0	1	
30E								1	1	0	
30F								1	1	1	
310						1	0	0	0	0	DAC A, 4LSBs, 1st Rank
311								0	0	1	DAC A, 8MSBs, 1st Rank
312								0	1	0	DAC B, 4LSBs, 1st Rank
313								0	1	1	DAC B, 8MSBs, 1st Rank
314								1	0	0	DAC C, 4LSBs, 1st Rank
315								1	0	1	DAC C, 8MSBs, 1st Rank
316								1	1	0	DAC D, 4LSBs, 1st Rank
317								1	1	1	DAC D, 8MSBs, 1st Rank
318							1	0	0	0	2nd Rank
319								0	0	1	
31A								0	1	0	
31B								0	1	1	
31C								1	0	0	
31D								1	0	1	
31E								1	1	0	
31F								1	1	1	

Note: Shaded registers are readable.

Table III. IBM PC Memory Map

The following IBM PC Basic routine produces four output voltage ramps from one AD664. Line numbers 10 through 70 define the hardware addresses for the first and second ranks of DAC registers as well as the first and second ranks of the mode select register. Program variables are initialized in line numbers 110 through 130. Line number 170 writes "0s" out to the first rank and, then, the second rank of the mode select register.

Line numbers 200 through 320 calculate output voltages. Finally line numbers 410 through 450 update the first, then the second ranks of the DAC input registers. Hardware registers may be read with the "INP" instruction. For example, the contents of the DAC A register may be accessed with the following command: Line# A = INP(DACA).

```
  5  REM----AD664 LISSAJOUS PATTERNS----
 10  REM ---ASSIGN HARDWARE ADDRESSES---
 20  DACA = 785
 30  DACB = 787
 40  DACC = 789
 50  DACD = 791
 60  DAC2ND = 792
 70  MODE1 = 769 :MODE2 = 776
 80  REM
 90  REM
100  REM ---INITIALIZE VARIABLES---
110  X=0: Y1 = 128: Y2 = 64: Y3 = 32
120  CX = 1: CY1 = 1: CY2 = -1: CY3 = 1
130  FX = 9: FY1 = 5: FY2 = 13 : FY3 = 15
140  REM
150  REM
160  REM ---INITIALIZE MODES AND GAINS---
170  OUT MODE1,0: OUT MODE2,0
180  REM
190  REM
200  REM ---CALCULATE VARIABLES---
210   X  = X  + FX*CX
220   Y1 = Y1 + FY1*CY1
230   Y2 = Y2 + FY2*CY2
240   Y3 = Y3 + FY3*CY3
250  IF X > 255 THEN X = 255: CX = -1: GOTO 270
260  IF X < 0 THEN X = 0: CX = 1
270  IF Y1 > 255 THEN Y1 = 255: CY1 = -1: GOTO 290
280  IF Y1 < 0 THEN Y1 =0: CY1 = 1
290  IF Y2 > 255 THEN Y2 =255: CY2=-1: GOTO 310
300  IF Y2 < 0 THEN Y2 = 0: CY2=-1
310  IF Y3 > 255 THEN Y3 = 255: CY3=-1: GOTO 400
320  IF Y3 < 0 THEN Y3=0: CY3=1
330  REM
340  REM
400  REM ---SEND DAC DATA---
410  OUT DACA,X
420  OUT DACB,Y1
430  OUT DACC,Y2
440  OUT DACD,Y3
450  OUT DAC2ND,0
500  REM
510  REM
520  REM ---LOOP BACK---
530  GOTO 210
```

in one 12-bit input word. Four address bits are used to perform the on-chip D/A selection as well as the various operating features. The R/$\overline{W}$ signal controls the $\overline{RD}$ function and system reset controls $\overline{RST}$.

and Q32 pins with $\overline{UDS}$ and $\overline{LDS}$ to provide a way to write 8-bit input and read 8-bit output words.

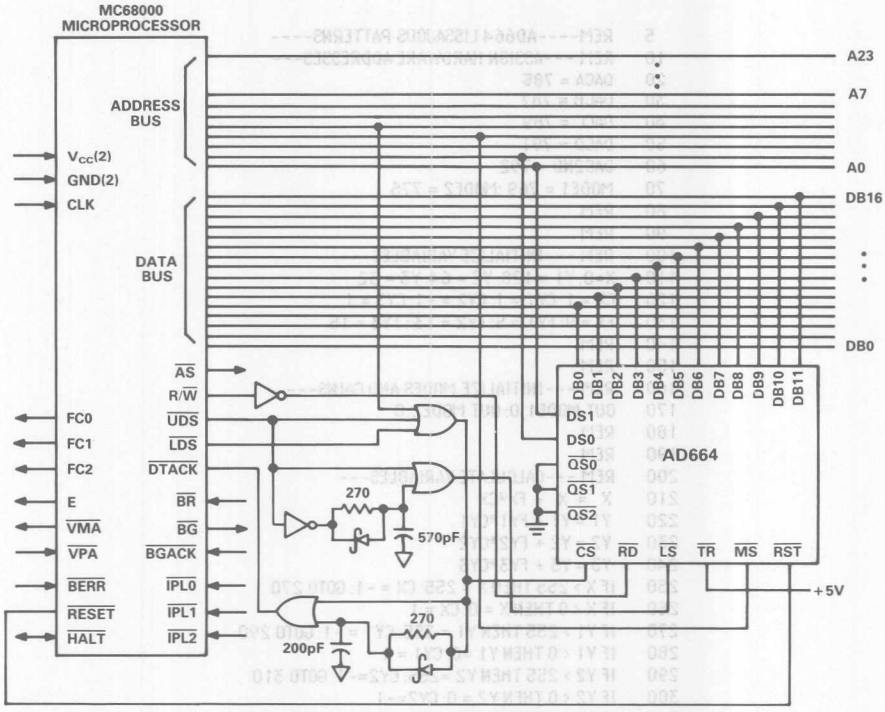


Figure 28. AD664 to MC68000 Interface

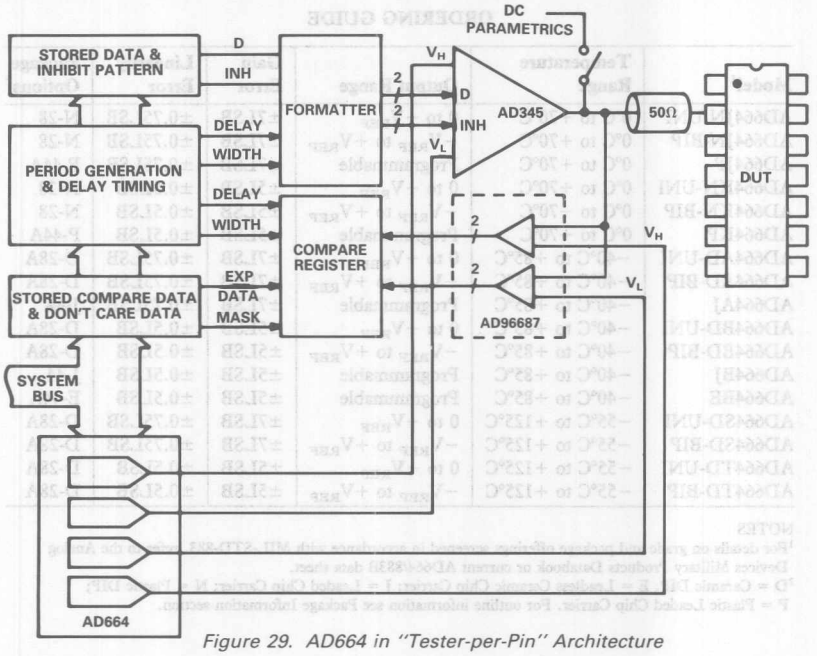


Figure 29. AD664 in "Tester-per-Pin" Architecture

APPLICATIONS OF THE AD664

"Tester-per-Pin" ATE Architecture

Figure 29 shows the AD664 used in a single channel of a digital test system. In this scheme, the AD664 supplies four individual output voltages. Two are provided to the V_{HIGH} and V_{LOW} inputs of the AD345 pin driver I.C. to set the digital output levels. Two others are routed to the inputs of the AD96687 dual comparator to supply reference levels of the readback features. This approach can be replicated to give as many channels of stimulus/readback as the tester has pins. The AD664 is a particularly appropriate choice for a large-scale system because the low power requirements (under 500mW) ease power supply and cooling requirements. Analog ground currents of 600μA or less make the ground current management task simpler. All DACs can be driven from the same system reference and will track over time and temperature. Finally, the small board area required by the AD664 (and AD345 and AD96687) allows a high functional density.

X-Y Plotters

Figure 30 is a block diagram of the control section of a microprocessor-controlled X-Y pen plotter. In this conceptual exercise, two of the DACs are used for the X-channel drive and two are used for the Y-channel drive. Each provides either the coarse or fine movement control for its respective channel. This approach offers increased resolution over some other approaches.

A designer can take advantage of the reset feature of the AD664 in the following manner. If the system is designed such that the "HOME" position of the pen (or galvanometer, beam, head or similar mechanism) results when the outputs of all of the DACs are at zero, then no system software is required to home the pen. A simple reset signal is sufficient.

Similarly, the transparent feature could be used to the same end. One code can be sent to all DACs at the same time to send the pen to the home position. Of course, this would require some software where the previous example would require only a single reset strobe signal!

Drawing scaling can be achieved by taking advantage of the AD664's software programmable gain settings. If, for example, an "A" size drawing is created with gain settings of 1, then a "C" size drawing can be created by simply resetting all DAC gains to 2 and redrawing the object. Conversely, a "C" size drawing created with gains of 2 can be reduced to "A" size simply by changing the gains to 1 and redrawing. The same principal applies for conversion from "B" size to "D" size or "D" size to "B" size. The multiplying capability of the AD664 provides another scaling option. Changing the reference voltage provides a proportional change in drawing size. Inverting the reference voltage would invert the drawing.

Swapping digital input data from the X channel to the Y channel would rotate the drawing 90 degrees.

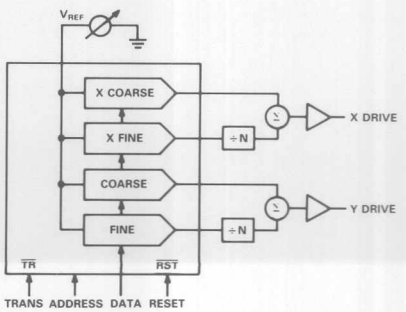


Figure 30. X-Y Plotter Block Diagram

ORDERING GUIDE

Model[1]	Temperature Range	Output Range	Gain Error	Linearity Error	Package Options[2]
AD664JN-UNI	0°C to +70°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	N-28
AD664JN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	N-28
AD664JP	0°C to +70°C	Programmable	±7LSB	±0.75LSB	P-44A
AD664KN-UNI	0°C to +70°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	N-28
AD664KN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	N-28
AD664KP	0°C to +70°C	Programmable	±5LSB	±0.5LSB	P-44A
AD664AD-UNI	−40°C to +85°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	D-28A
AD664AD-BIP	−40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	D-28A
AD664AJ	−40°C to +85°C	Programmable	±7LSB	±0.75LSB	J-44
AD664BD-UNI	−40°C to +85°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	D-28A
AD664BD-BIP	−40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	D-28A
AD664BJ	−40°C to +85°C	Programmable	±5LSB	±0.5LSB	J-44
AD664BE	−40°C to +85°C	Programmable	±5LSB	±0.5LSB	E-44A
AD664SD-UNI	−55°C to +125°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	D-28A
AD664SD-BIP	−55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	D-28A
AD664TD-UNI	−55°C to +125°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	D-28A
AD664TD-BIP	−55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	D-28A

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD664/883B data sheet.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Leaded Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

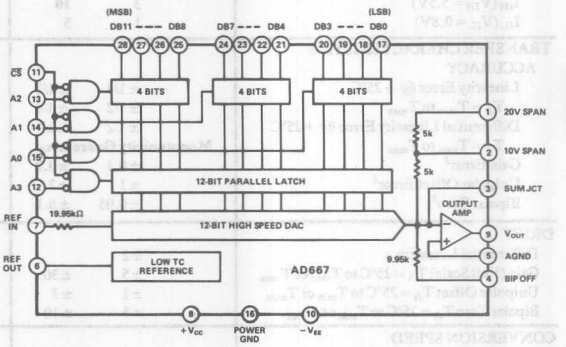
Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES

- Complete 12-Bit D/A Function
  - Double-Buffered Latch
  - On Chip Output Amplifier
  - High Stability Buried Zener Reference
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max
- Settling Time: 3μs max to 0.01%
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs
- Low Logic Input Currents
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K, B grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 5ppm/°C.

***Protected by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

The AD667 is available in five performance grades. The AD667J and K are specified for use over the 0 to +70°C temperature range and are available in a 28-pin molded plastic DIP (N) or PLCC (P) package. The AD667S grade is specified for the −55°C to +125°C range and is available in the ceramic DIP (D) or LCC (E) package. The AD667A and B are specified for use over the −25°C to +85°C temperature range and are available in a 28-pin hermetically sealed ceramic DIP (D) package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current steering switch and on-board high speed output amplifier settle within 1/2LSB for a 10V full scale transition in 2.0μs when properly compensated.
6. The AD667 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD667/883B data sheet for detailed specifications.

	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[1]							
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10	µA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{min}$ to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ‖500pF load)							
with 10kΩ Feedback		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3	µs
For LSB Change		1			1		µs
Slew Rate	10			10			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5V dc		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	V
Supply Current							
+11.4 to +16.5V dc		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	−65		+125	−65		+125	°C

NOTES
[1]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.
[2]Adjustable to zero.
[3]FSR means "Full Scale Range" and is 20V for ±10V range and 10V for the ±5V range.
[4]A minimum power supply of ±12.5V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

ABSOLUTE MAXIMUM RATINGS

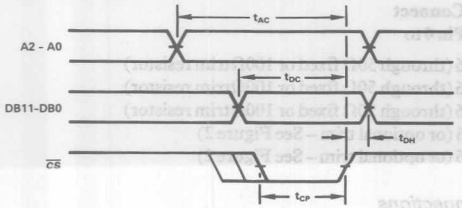
V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11–15, 17–28) to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

	AD667A			AD667B			AD667S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, $T_{min}-T_{max}$)[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/2	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2		±1/4	±3/4	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Differential Linearity		±2			±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±15	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+11.4 to +16.5V dc		8	12		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25		20	25	mA
TEMPERATURE RANGE										
Specification	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

TIMING DIAGRAMS

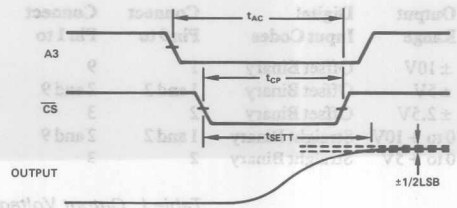
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)

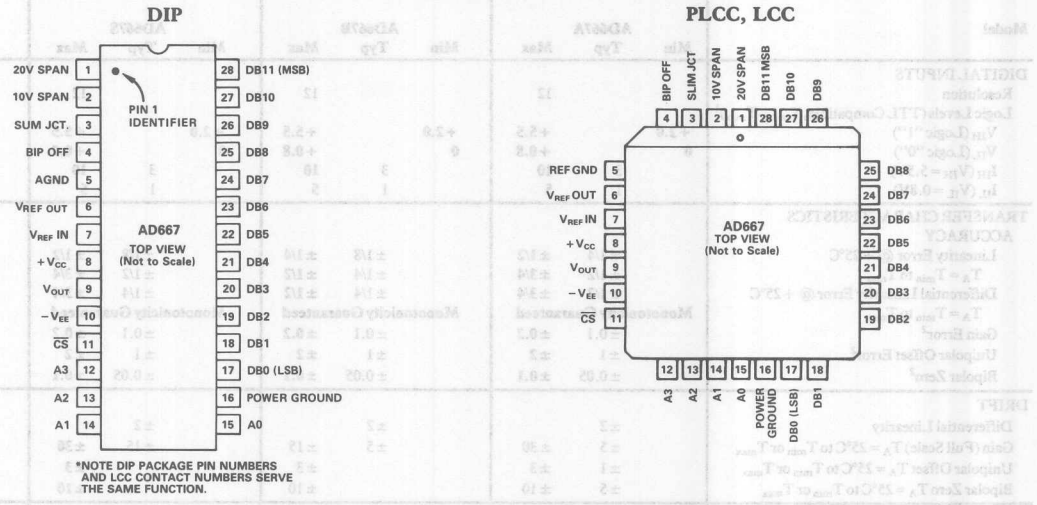


WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)



PIN CONNECTIONS



THE AD667 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD667 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and B versions and 1/2LSB for the J, A and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD667 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be −1.83mV, or −3/4LSB. The AD667K and B grades have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD667 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD667 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

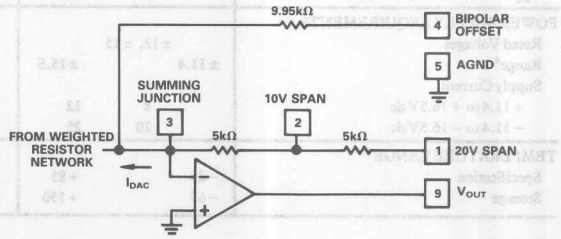


Figure 1. Output Amplifier Voltage Range Scaling Circuit

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ωtrim resistor)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ωtrim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ωtrim resistor)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

UNIPOLAR CONFIGURATION (Figure 2)
This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, pin 4, should be grounded if not used for trimming.

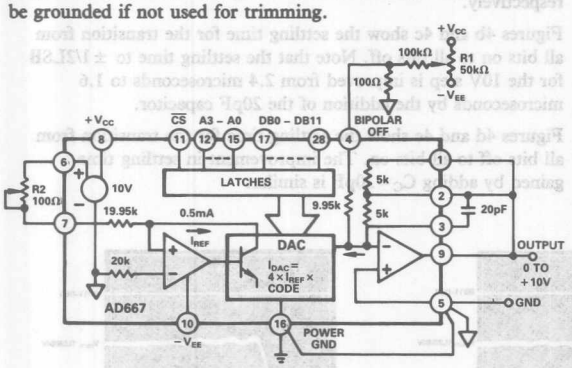


Figure 2. 0 to +10V Unipolar Voltage Output

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 4 should be connected to pin 5.

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

BIPOLAR CONFIGURATION (Figure 3)
This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST
Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

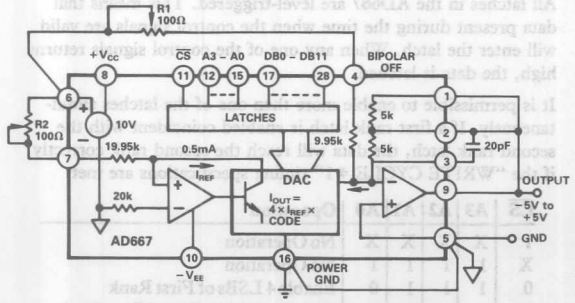


Figure 3. ±5V Bipolar Voltage Output

INTERNAL/EXTERNAL REFERENCE USE
The AD667 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD667 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD667 reference output should be buffered with an external op amp if it is required to supply more than 0.1mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD667 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD667 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +11 volts, which allows both 8.192V and 10.24V ranges to be used. The AD667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ±5% power supply requirement to be relaxed to ±12 volts ±10%.

It is not recommended that the AD667 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately −50ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24V full-scale is desired, a 140Ω 1% low-TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between pins 6 and 7) should be increased to 200Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200Ω.

GROUNDING RULES
The AD667 brings out separate analog and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths.

The analog ground at pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD667; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is pre-

ferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

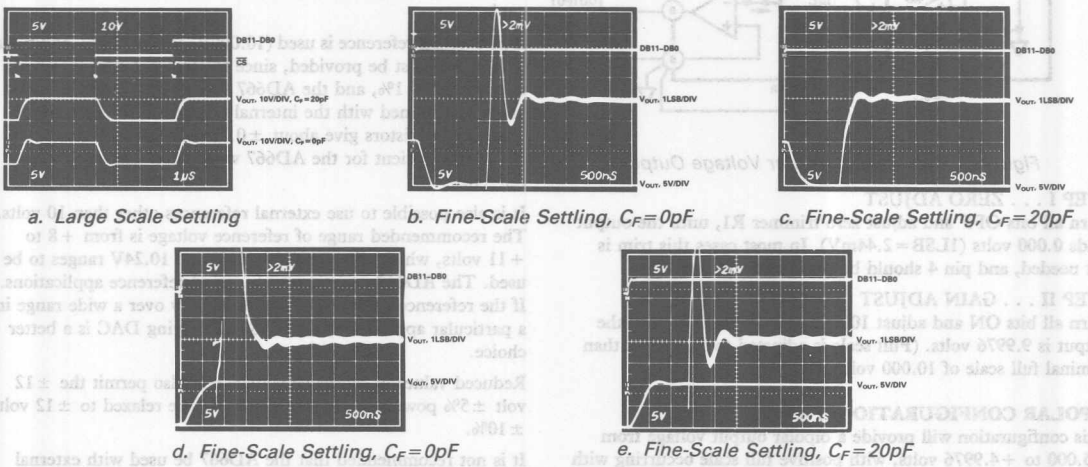
It is also important to apply decoupling capacitors properly on the power supplies for the AD667 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD667 to the analog ground pin of the AD667. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

The dynamic performance of the AD667's output amplifier can be optimized by adding a small (20pF) capacitor across the feedback resistor. Figure 4 shows the improvement in both large-signal and small-signal settling for the 10V range. In Figure 4a, the top trace shows the data inputs (DB11–DB0 tied together), the second trace shows the CS pulse (A3–A0 tied low), and the lower two traces show the analog outputs for C_F = 0 and 20pF respectively.

Figures 4b and 4c show the settling time for the transition from all bits on to all bits off. Note that the settling time to ±1/2LSB for the 10V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20pF capacitor.

Figures 4d and 4e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding C_C = 20pF is similar.



a. Large Scale Settling

b. Fine-Scale Settling, C_F = 0pF

c. Fine-Scale Settling, C_F = 20pF

d. Fine-Scale Settling, C_F = 0pF

e. Fine-Scale Settling, C_F = 20pF

Figure 4. Settling Time Performance

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD667 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD667 logic section.

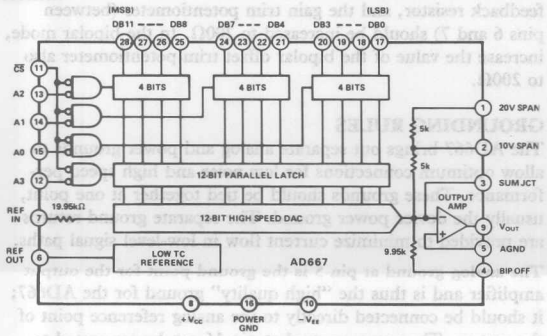


Figure 5. AD667 Block Diagram

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input. All control inputs are active low, consistent with general practice in microprocessor systems. The four address lines each enable one of the four latches, as indicated in Table II.

All latches in the AD667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the "WRITE CYCLE #1" timing specifications are met.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table II. AD667 Truth Table

INPUT CODING

The AD667 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0V and logic "0" is defined as an input voltage less than 0.8V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD667 can be used with two's complement input coding if an inverter is used on the MSB (DB11).

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 6.

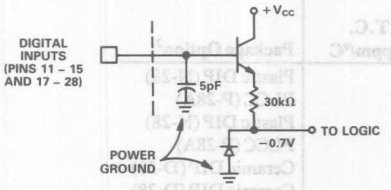


Figure 6. Equivalent Digital Input Circuit

The AD667 data and control inputs will float to a logic 0 if left open. It is recommended that any unused inputs be connected to power ground to improve noise immunity.

Fanout for the AD667 is 100 when used with a standard low power Schottky gate output device.

8-BIT MICROPROCESSOR INTERFACE

The AD667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

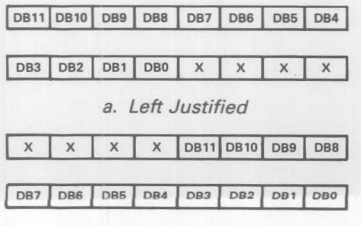


Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

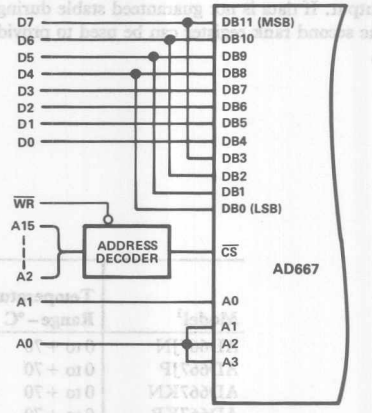


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD667 still occupies two adjacent locations in the processor's memory map. In the circuit of Figure 9, location X01 loads the 8LSBs and location X10 loads the 4MSBs and updates the output.

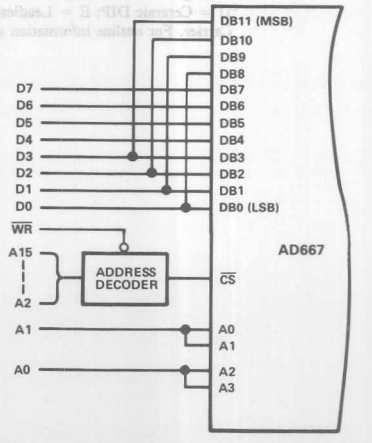


Figure 9. Right-Justified 8-Bit Bus Interface

USING THE AD667 WITH 12- AND 16-BIT BUSES

The AD667 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied low, and the latch is enabled by $\overline{CS}$ going low. The AD667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the AD667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

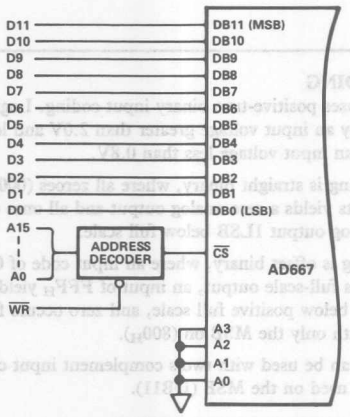


Figure 10. Connections for 12- and 16-Bit Bus Interface

ORDERING GUIDE

Model[1]	Temperature Range – °C	Linearity Error Max @ 25°C	Gain T.C. Max ppm/°C	Package Option[2]
AD667JN	0 to +70	±1/2LSB	30	Plastic DIP (N-28)
AD667JP	0 to +70	±1/2LSB	30	PLCC (P-28A)
AD667KN	0 to +70	±1/4LSB	15	Plastic DIP (N-28)
AD667KP	0 to +70	±1/4LSB	15	PLCC (P-28A)
AD667AD	−25 to +85	±1/2LSB	30	Ceramic DIP (D-28)
AD667BD	−25 to +85	±1/4LSB	15	Ceramic DIP (D-28)
AD667SD	−55 to +125	±1/2LSB	30	Ceramic DIP (D-28)
AD667SE	−55 to +125	±1/2LSB	30	LCC (E-28A)
AD667/883B	−55 to +125	*	*	*

NOTES

*Refer to AD667/883B military data sheet.

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD667/883B data sheet.

[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

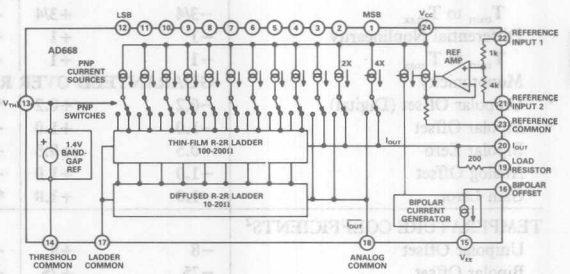
12-Bit Ultrahigh Speed Multiplying D/A Converter

AD668

FEATURES

- **Ultrahigh Speed: Current Settling to 1 LSB in 90 ns for a Full-Scale Change in Digital Input. Voltage Settling to 1 LSB in 120 ns for a Full-Scale Change in Analog Input**
- **15 MHz Reference Bandwidth**
- **Monotonicity Guaranteed over Temperature**
- **10.24 mA Current Output or 1.024 V Voltage Output**
- **Integral and Differential Linearity Guaranteed over Temperature**
- **0.3" "Skinny DIP" Packaging**
- **MIL-STD-883 Compliant Versions Available**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD668 is an ultrahigh speed, 12-bit, multiplying digital-to-analog converter, providing outstanding accuracy and speed performance in responding to both analog and digital inputs. The AD668 provides a level of performance and functionality in a monolithic device that exceeds that of many contemporary hybrid devices. The part is fabricated using Analog Devices' Complementary Bipolar (CB) Process, which features vertical NPN and PNP devices on the same chip without the use of dielectric isolation. The AD668's design capitalizes on this proprietary process in combination with standard low impedance circuit techniques to provide its unique combination of speed and accuracy in a monolithic part.

The wideband reference input is buffered by a high gain, closed loop reference amplifier. The reference input is essentially a 1 V, high impedance input, but trimmed resistive dividers are provided to readily accommodate 5 V and 1.25 V references. The reference amplifier features an effective small signal bandwidth of 15 MHz and an effective slew rate of 3% of full scale/ns.

Multiple matched current sources and thin film ladder techniques are combined to produce bit weighting. The output range can nominally be taken as a 10.24 mA current output or a 1.024 V voltage output. Varying the analog input can provide modulation of the DAC full scale from 10% to 120% of its nominal value. Bipolar outputs can be realized through pin-strapping to provide two-quadrant operation without additional external circuitry.

Laser wafer trimming insures full 12-bit linearity and excellent gain accuracy. All grades of the AD668 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100 Ω ± 1.0%.

The AD668 is available in four performance grades. The AD668JQ and KQ are specified for operation from 0°C to +70°C, the AD668AQ is specified for operation from −40°C to +85°C, and the AD668SQ specified for operation from −55°C to +125°C. All grades are available in a 24-pin cerdip (0.3" package.

PRODUCT HIGHLIGHTS

1. The fast settling time of the AD668 provides suitable performance for waveform generation, graphics display, and high-speed A/D conversion applications.
2. The high bandwidth reference channel allows high frequency modulation between analog and digital inputs.
3. The AD668's design is configured to allow wide variation of the analog input, from 10% to 120% of its nominal value.
4. The AD668's combination of high performance and tremendous flexibility makes it an ideal building block for a variety of high speed, high accuracy instrumentation applications.
5. The digital inputs are readily compatible with both TTL and 5V CMOS logic families.
6. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.
7. The AD668 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD668/883B data sheet for detailed specifications.

	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION	12			12			12			Bits
LSB WEIGHT (At Nominal FSR)										
Current		2.5			*			*		μA
Voltage (Current into R_L)		250			*			*		μV
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	*		*	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	*		*	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	*		*	LSB
T_{min} to T_{max}	−1		+1	−1/2		+1/2	*		*	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset (Digital)	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	−0.6		+0.6	*		*	% of FSR
Bipolar Zero	−0.5		+0.5	−0.2		+0.2	*		*	% of FSR
Analog Offset	−1.0		+1.0	−0.7		+0.7	*		*	% of V_{NOM}
Gain Error	−1.0		+1.0	*		*	*		*	% of FSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−8		+8	−5		+5	*		*	ppm of FSR/°C
Bipolar Offset	−25		+25	−15		+15	*		*	ppm of FSR/°C
Bipolar Zero	−20		+20	−15		+15	*		*	ppm of FSR/°C
Analog Offset	−20		+20	−10		+10	−20		+20	ppm of V_{NOM}/°C
Gain Drift	−30		+30	−15		+15	−40		+40	ppm of FSR/°C
Gain Drift (I_{OUT})		±150			±150			±150		ppm of FSR/°C
REFERENCE INPUT										
Input Resistance										
5.0 V Range		5			*			*		kΩ
1.25 V Range		5			*			*		kΩ
1.0 V Range		1			*			*		MΩ
Reference Range (T_{min} to T_{max})	10	100	120	*	*	*	*	*	*	% of V_{NOM}
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10		+10	*		*	*		*	μA
I_{IL}	0	60	100	*	*	*	0	100	200	−μA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ± 5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ± 0.512									V
OUTPUT COMPLIANCE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240	*	*	*	*	*	*	Ω
Inclusive of R_L	99	100	101	*	*	*	*	*	*	Ω
REFERENCE AMPLIFIER										
Input Bias Current		1.5			*			*		μA
Slew Rate		3			*			*		% of FS/ns
Large Signal Bandwidth		10			*			*		MHz
Small Signal Bandwidth		15			*			*		MHz
Undervoltage Recovery Time										
V_{REF}/V_{NOM} to 0%		35			*			*		ns

Parameter	AD668J/A Min	AD668J/A Typ	AD668J/A Max	AD668K Min	AD668K Typ	AD668K Max	AD668S Min	AD668S Typ	AD668S Max	Units
AC CHARACTERISTICS										
Analog Settling Time										
(10% to 120% Step)										
to ±1%		60			*			*		ns to 1% of FSR
to ±0.1%		90			*			*		ns to 0.1% of FSR
to ±0.025%		120			*			*		ns to 0.025% of FSR
Digital Settling Time										
Current										
to ±1%		30			*			*		ns to 1% of FSR
to ±0.025%		90			*			*		ns to 0.025% of FSR
Voltage (100 Ω, Internal R_L)[3]										
to 1%		50			*			*		ns to 1% of FSR
to 0.1%		75			*			*		ns to 0.1% of FSR
to 0.025%		110			*			*		ns to 0.025% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		20			*			*		% of FSR
Total Harmonic Distortion[5]		−75			*			*		dB
Multiplying Feedthrough Error[6]		−62			*			*		dB
FULL-SCALE TRANSITION[2]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+10.8 V to +16.5 V		27	**32**			*			*	mA
−10.8 V to −16.5 V		7	**9**			*			*	−mA
Power Dissipation		510	615			*			*	mW
PSRR[7]			**0.05**			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2] (J, K, S)	0		+70	*		*	−55		+125	°C
Rated Specification (A)	−40		+85							°C
Storage	−65		+150	*		*	*		*	°C

NOTES
*Same as AD668J/A.
[1]Measured in I_{OUT} mode. Specified at nominal 5 V full-scale reference.
[2]Measured in V_{OUT} mode, unless otherwise specified. Specified at nominal 5 V full-scale reference.
[3]Total resistance. Refer to Figure 4.
[4]At the major carry, driven by HCMOS logic.
[5]V_{OUT} = 1 V p-p, V_{IN} = 10% to 110%, 100 kHz. Digital Input All 1s.
[6]V_{IN} = 200 mV p-p, 1 MHz Sine Wave. Digital Input all 0s. See Figure 20.
[7]Measured at 15 V ± 10% and 12 V ± 10%.

Specifications shown in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM . . . . . 0 V to +18 V
V_{EE} to REFCOM . . . . . 0 V to −18 V
REFCOM to LCOM . . . . . +100 mV to −10 V
ACOM to LCOM . . . . . ±100 mV
THCOM to LCOM . . . . . ±500 mV
REFCOM to REFIN (1, 2) . . . . . 18 V
I_{BPO} to LCOM . . . . . ±5 V
I_{OUT} to LCOM . . . . . −5 V to V_{TH}
Digital Inputs to THCOM . . . . . −500 mV to +7.0 V
REFIN1 to REFIN2 . . . . . 36 V
V_{TH} to THCOM . . . . . −0.7 V to +1.4 V
Logic Threshold Control Input Current . . . . . 5 mA
Power Dissipation . . . . . 670 mW
Storage Temperature Range
Q (Cerdip) Package . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Thermal Resistance
θ_{JA} . . . . . +75°C/W
θ_{JC} . . . . . +25°C/W

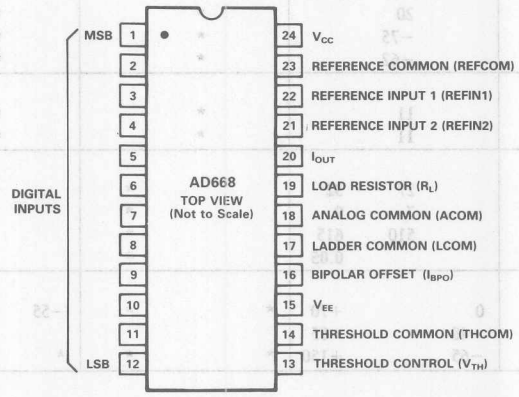
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max @ 25°C	Voltage Gain T.C. Max ppm/°C	Package Option[2]
AD668JQ	0°C to +70°C	±1/2	±30	Q-24
AD668KQ	0°C to +70°C	±1/4	±15	Q-24
AD668AQ	−40°C to +85°C	±1/2	±30	Q-24
AD668SQ	−55°C to +125°C	±1/2	±40	Q-24

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD668/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATION



DEFINITIONS

LINEARITY ERROR (also called INTEGRAL NONLINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples of 1 LSB. The AD668 is laser trimmed to 1/4 LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2 LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in the analog output, normalized to full scale, associated with a 1 LSB change in digital input code.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases. Monotonic behavior requires that the differential linearity error not exceed 1 LSB in the negative direction.

UNIPOLAR OFFSET ERROR (DAC OFFSET): The DAC offset is the portion of the DAC output that is independent of the digital input. The unipolar DAC offset error is measured as the deviation of the analog output from the ideal (0 V or 0 mA) when the analog input is set to 100% and the digital inputs are set to all 0s.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the DAC is connected in the bipolar mode (Pin 16 connected to Pin 20), the analog input is set to 100%, and the digital inputs are set to all 0s is called the bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal (0 V or 0 mA) for bipolar mode when only the MSB is on (100 . . . 00) is called bipolar zero error.

COMPLIANCE VOLTAGE: The allowable voltage excursion at the output node of a DAC which will not degrade the accuracy of the DAC output.

SETTLING TIME (DIGITAL CHANNEL): The time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

SETTLING TIME (ANALOG CHANNEL): The time required for the output to reach and remain within a specified error band about its final value, measured from the analog input's crossing of it's 50% value.

GAIN ERROR: The difference between the ideal and actual output span of FS−1 LSB, expressed either in % of FS or LSB, when all bits are on is called the gain error.

ANALOG OFFSET ERROR: The analog offset is defined as the offset of the analog amplifier channel, referred to the analog input. Ideally, this would be measured with the analog input at 0 V and the digital input at full scale. Since a 0 V analog input voltage constitutes an undervoltage condition, this specification is determined through linear extrapolation, as indicated in Figure 1.

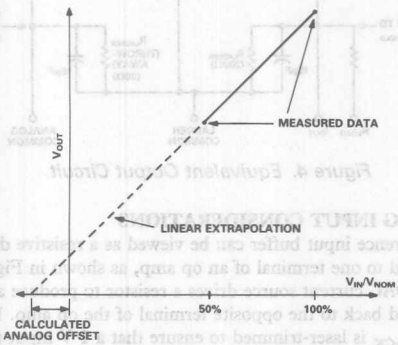


Figure 1. Derivation of Analog Offset Voltage

GLITCH IMPULSE: Asymmetrical switching times in a DAC may give rise to undesired output transients which are quantified by their glitch impulse. It is specified as the net area of the glitch in pV-sec.

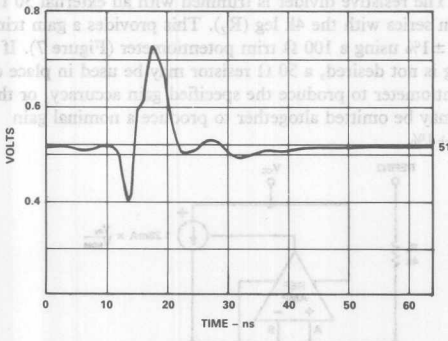


Figure 2. AD668 Major Carry Glitch

FUNCTIONAL DESCRIPTION

The AD668 is designed to combine excellent performance with maximum flexibility. The functional block diagram and the simple transfer functions provided below will provide the user with a basic grasp of the AD668's operation. Examples of typical circuit configurations are provided in the section APPLYING THE AD668. Subsequent sections contain more detailed information useful in optimizing DAC performance in high speed, high resolution applications.

DAC Transfer Function

The AD668 may be used either in a current-output mode (DAC output connected to a virtual ground) or a voltage-output mode (DAC output connected to a resistive load).

In current output mode:

Unipolar Mode

$$I_{OUT} = \frac{V_{IN}}{V_{NOM}} \times \frac{DAC\ code}{4096} \times 10.24\ mA$$

Bipolar Mode

$$I_{OUT} = \frac{V_{IN}}{V_{NOM}} \times \frac{DAC\ code}{4096} \times 10.24\ mA - \frac{V_{IN}}{V_{NOM}} \times 5.12\ mA$$

In voltage output mode:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

(for both unipolar and bipolar modes)

where:

V_{IN} – the analog input voltage.

V_{NOM} – the nominal full scale of the reference voltage: 1 V, 1.25 V, or 5 V, determined by the wiring configuration of Pins 21 and 22. (See APPLYING THE AD668.)

DAC code – the numerical representation of the DAC's digital inputs; a number between 0 and 4095.

R_{LOAD} – the resistance of the DAC output node; the maximum this can be is 200 Ω (the internal DAC ladder resistance). The on-board load resistor (Pin 19) has been trimmed so that its parallel combination with the DAC ladder resistance is 100 Ω (±1%).

Bipolar mode – produces a bipolar analog output from the digital input by offsetting the normal output current with a precision current source. This offset is achieved by connecting Pin 16 to the DAC output. In the unipolar mode, Pin 16 should be grounded.

If the dc errors are included, the transfer function becomes somewhat more complex:

$$I_{OUT} = \left(\frac{V_{IN}}{V_{NOM}} + OFFSET_{ANALOG}\right) \times \frac{DAC\ code}{4096} \times (1 + E) \times 10.24\ mA + OFFSET_{DIGITAL} \times \frac{V_{IN}}{V_{NOM}} \times 10.24\ mA - \left(\frac{V_{IN}}{V_{NOM}} + OFFSET_{ANALOG}\right) \times (5.12\ mA + [OFFSET_{BIPOLAR} \times 10.24\ mA])$$

(Last term is for use in bipolar mode; V_{OUT} is still just $I_{OUT} \times R_{LOAD}$.)

where:

$OFFSET_{ANALOG}$ = the analog offset error.
$OFFSET_{DIGITAL}$ = is the unipolar digital offset error.
$OFFSET_{BIPOLAR}$ = is the bipolar offset error.
E = the gain error, expressed fractionally.

Operating Limits:

$$0.1 < \frac{V_{IN}}{V_{NOM}} < 1.2$$

$0 < V_{IN}/V_{NOM} < 0.1$ constitutes an undervoltage condition and is subject to the specified recovery time.

$1.2 < V_{IN}/V_{NOM}$ constitutes an overvoltage condition. This can saturate the DAC transistors, resulting in decreased response

time and can, over extended time, damage the part through excessive power dissipation. Figure 3 indicates the specified regions of operation in both the unipolar and bipolar cases.

The small signal 3 dB bandwidth of the V_{IN} channel is 15 MHz. The large signal 3 dB bandwidth is approximately 10 MHz.

V_{OUT} is limited by the specified output compliance: −2 V to +1.2 V.

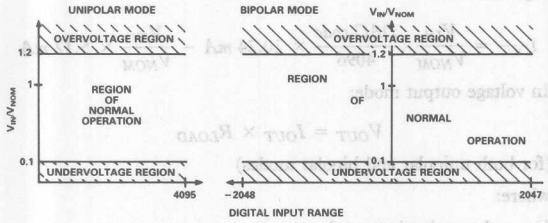


Figure 3. Quadrant Plots of the AD668

CIRCUIT DESCRIPTION OF THE AD668

Successful design of high speed, high resolution systems demands a designer's solid working knowledge of the components being used. The AD668 has been carefully configured to provide maximum functionality in a variety of applications. While it is beyond the scope of this data sheet to exhaustively cover each potential application topology, the detailed information that follows is intended to provide the designer with a sufficiently thorough understanding of the part's inner workings to allow selection of the circuit topology to best suit the application.

CURRENT OUTPUT VS. VOLTAGE OUTPUT

As indicated in the FUNCTIONAL DESCRIPTION, the AD668 output may be taken as either a voltage or a current, depending on external circuit connections. In the current output mode, the DAC output (Pin 20) is tied to a summing junction, and the current flowing from the DAC into this summing junction is sensed. In this mode, the DAC output scale is insensitive to whether the load resistor, R_{LOAD}, is shorted (Pin 19 connected to Pin 20), or grounded (Pin 19 connected to Pin 18). However, the connection of this resistor does affect the output impedance of the DAC and may have a significant impact on the noise gain and stability of the external circuitry. Grounding R_{LOAD} will reduce the output impedance, thereby increasing the noise gain and also enhancing the stability of a circuit using a non-unity-gain-stable op amp (see Figure 10).

In the voltage output mode, the DAC's output current flows through its own internal impedance (perhaps in parallel with an external impedance) to generate a voltage. In this case, the DAC output scale is directly dependent on the load impedance. The temperature coefficient of the AD668's transfer function will be lowest when used in the voltage output mode.

OUTPUT VOLTAGE COMPLIANCE

The AD668 has an output compliance range of −2.0 V to +1.2 V (with respect to the LCOM pin). The current steering output stages will be unaffected by changes in the output terminal voltage over this range. However, as shown in Figure 4, there is an equivalent output impedance of 200 Ω in parallel with 15 pF at the output terminal, producing an equivalent error current if the voltage deviates from the ladder common. This is a linear effect which does not change with input code. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance. The positive compliance limit is not affected by the positive power supply, but is a function of the output current and the logic threshold voltage at V_{TH}, Pin 13.

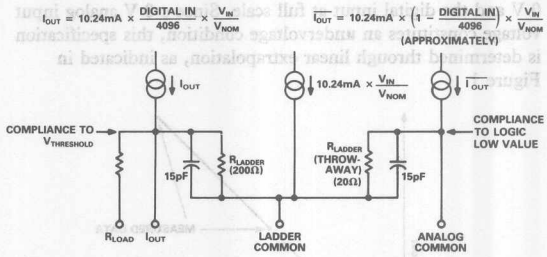


Figure 4. Equivalent Output Circuit

ANALOG INPUT CONSIDERATIONS

The reference input buffer can be viewed as a resistive divider connected to one terminal of an op amp, as shown in Figure 5. A unit DAC current source drives a resistor to produce a voltage that is fed back to the opposite terminal of the op amp. Resistor $R_{FEEDBACK}$ is laser-trimmed to ensure that a 1 V input to node A of the op amp will produce a 10.24 mA DAC output. REFIN1 and REFIN2 may be configured in any way the user chooses to provide a nominal input full scale of 1 V at node A. R1 and R2 are sized and trimmed to provide both a 5:1 voltage divider and a parallel impedance that matches the impedance at node B, thereby reducing the amplifier offset voltage due to bias current. The resistive divider is trimmed with an external 50 Ω resistor in series with the 4k leg (R_2). This provides a gain trim range of ±1% using a 100 Ω trim potentiometer (Figure 7). If trimming is not desired, a 50 Ω resistor may be used in place of the potentiometer to produce the specified gain accuracy, or the resistor may be omitted altogether to produce a nominal gain error of +1%.

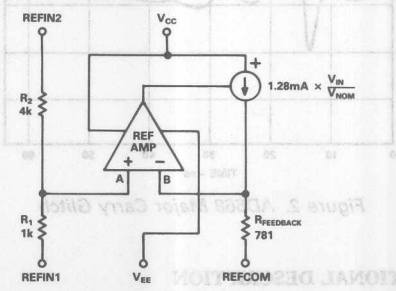


Figure 5. Equivalent Analog Input Circuitry

DIGITAL INPUT CONSIDERATIONS

The AD668 uses a standard positive true straight binary code for unipolar outputs (all 1s full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full scale; with 111 . . . 11, the output will go to positive full scale less 1 LSB; and with 100 . . . 00 (only the MSB on), the output will go to zero.

The threshold of the digital inputs is set at 1.4 V and does not vary with supply voltage. This reference is provided by a bandgap generator, which requires approximately 3 mA of bias

current achieved by tying R_{TH} to any $+V_{LOGIC}$ supply where:

$$R_{TH} = \left(\frac{+V_{LOGIC} - 1.4\ V}{3\ mA}\right)$$

(see Figure 6). The digital bit inputs operate with small input currents to easily interface to unbuffered CMOS logic. The digital input signals to the DAC should be isolated from the analog input and output as much as possible. To minimize undershoot, ringing, and digital feedthrough noise, the interconnect distance to the DAC inputs should be kept as short as possible. Termination resistors may improve performance if the digital lines become too long. The digital inputs should be free from large glitches and ringing and have 10% to 90% rise and fall times on the order of 5 ns.

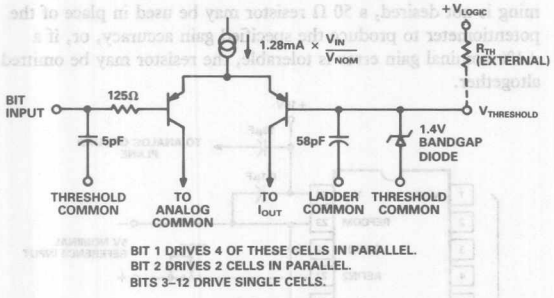


Figure 6. Equivalent Digital Input

To realize the AD668's specified ac performance, it is recommended that high speed logic families such as Schottky TTL, high speed CMOS, or the new lines of high speed TTL be used exclusively. Table I shows how DAC performance, particularly glitch, can vary depending on the driving logic used. As this table indicates, STTL, HCMOS, and FAST* represent the most viable families for driving the AD668.

Table I. DAC Performance vs. Drive Logic

Logic Family[1]	10-90%[2] DAC Rise Time	Settling Time[2, 3] 1%	0.1%	1 LSB (0.025%)	Glitch[4] Impulse	Maximum Glitch Excursion
TTL	10.5 ns	47 ns	77 ns	100 ns	2.5 nV-s	280 mV
LSTTL	11.25 ns	35 ns	60 ns	120 ns	1.2 nV-s	270 mV
STTL	11 ns	50 ns	75 ns	110 ns	500 pV-s	200 mV
HCMOS	12 ns	53 ns	78 ns	100 ns	350 pV-s	200 mV
FAST*	11.5 ns	49 ns	73 ns	100 ns	2 nV-s	250 mV

NOTES
[1]All values typical, taken in test fixture diagrammed in Figure 23.
[2]Measurements are made for a 1 V full-scale step into 100 Ω DAC load resistance.
[3]Settling time is measured from the time the digital input crosses the threshold voltage (1.4 V) to when the output is within the specified range of its final value.
[4]The worst case glitch impulse, measured on the major carry. DAC full scale is 1 V.
*FAST is a registered trademark of National Semiconductor Corporation.

The variations in DAC settling and rise times can be attributed to differences in rise time and current driving capabilities of the various families. Differences in the glitch impulse are predominantly dependent upon the variation in data skew. Variations in these specs occur not only between logic families, but also between different gates and latches within the same family. When selecting a gate to drive the AD668 logic input, pay particular attention to the propagation delay time specs: t_{PLH} and t_{PHL}. Selecting the smallest delays possible will help to minimize the settling time, while selection of gates where t_{PLH} and t_{PHL} are closely matched to one another will minimize the glitch impulse resulting from data skew. Of the common latches, the 74374 octal flip-flop provides the best performance in this area for many of the logic families mentioned above.

2

PIN BY PIN CURRENT ACCOUNTING

The internal wiring and pinout of the AD668 are dictated in large part by current management constraints. When using low impedance, high current, high accuracy parts such as the AD668, great care must be taken in the routing of not only signal lines, but ground and supply lines as well. The following accounting provides a detailed description of the magnitudes and signal dependencies of the currents associated with each of the part's pins. These descriptions are consistent with the functional block diagram as well as the equivalent circuits provided in Figures 4, 5, and 6.

V_{CC} – the current into this pin is drawn predominantly through the DAC current sources and generally runs about 2.2 times the DAC's nominal full scale. By design, this current is independent of the digital input code but is linearly dependent on analog input variations.

REFCOM – this node provides the reference ground for the reference amplifier's current feedback loop (as illustrated in Figure 5) as well as providing the negative supply voltage for most of the reference amplifier. The current consists of 1.2 mA of analog input dependent current and another 3 mA of input independent current. Analog input voltages should always be produced with respect to this voltage.

REFIN1 – has a 1k series resistance to the reference amplifier input and a 5k series resistance to REFIN2. REFIN1 may be used in conjunction with REFIN2 to provide a 5:1 voltage divider, or the two may be driven in parallel to provide a high impedance input node (see Figure 5).

REFIN2 – the 4k side of the input resistive divider. Note also that the combined impedance of these two resistors matches the effective impedance at the other input of the reference amplifier, thereby minimizing the offset due to bias currents. Circuits which alter this effective impedance may suffer increased analog offset and drift performance degradation as a result of the mismatch in these impedances.

I_{OUT} – the output current. In the current output mode with this node tied to a virtual ground, a 10.24 mA nominal full scale output current will flow from this pin. In the voltage output mode, with R_L grounded, half of the output current will flow out of R_L and the other half will flow out of LCOM. External resistive loading will cause current to be divided between LCOM, R_L, and I_{OUT} as Figure 4 suggests.

R_L – a 200 Ω resistor with one end internally wired to the output pin. If a 200 Ω ±20% DAC output impedance is desired, R_L should be shorted to I_{OUT}. Grounding R_L will provide a DAC output impedance of 100 Ω ±1%. As noted above, in voltage output configurations, a large portion of the DAC output current will flow through this pin.

output is not generally advised, since it is untrimmed and its positive output compliance is limited to the logic low voltage.

LCOM – the current in this node has been carefully configured to be independent of digital code when the output is into a virtual ground, thereby minimizing any detrimental effects of ladder ground resistance on linearity. However, the current in this node is proportional to the analog input voltage and the ground drop here is responsible for the dc analog feedthrough. The nominal value of this current is approximately equal to the DAC full scale.

IBPO – the bipolar offset current flows into this node, with voltage compliance to V_{EE} + 3 V. This is a high impedance current source, and should be grounded if the offset current is not used.

V_{EE} – this voltage may be set anywhere from −10.8 V to −16.5 V. The current in this node consists of 1.2 times the bipolar offset current plus 500 μA of bias current for the reference amplifier's front end. The negative supply current is independent of digital input but is linearly dependent on analog input.

THCOM – is the ground point for the bandgap diode that generates the threshold voltage. The current coming out of this node is the same as that flowing into V_{TH} plus a code-dependent number of base currents (see Figure 6). It is possible to introduce an offset between THCOM and the system common, thereby offsetting the effective logic threshold and positive output compliance voltage.

V_{TH} – as indicated earlier, if given sufficient positive bias current, this voltage will be 1.4 V above THCOM. The necessary bias current can readily be provided by a suitable resistor to any positive supply. As Figure 6 suggests, this node is directly coupled to the DAC output through several base to collector capacitances and hence, should be carefully decoupled to the analog ground.

DIGITAL INPUTS – when a bit is in the high state, the input current is the leakage current of a reverse biased diode. When the bit is driven low, it must sink a base current to ground, and this base current will be proportional to the analog input. Note that the input current for Bit 2 will be twice that for Bits 3–12, and Bit 1's current will be 4 times Bit 3's, but all the currents will be below the value specified.

APPLYING THE AD668

The following are some typical circuit configurations for the AD668. As Table II indicates, these represent only a sample of the possible implementations.

5 V REFIN, 1 V UNIPOLAR, UNBUFFERED VOLTAGE OUTPUT

Figure 7 shows a typical topology for generating an unbuffered voltage output. R_L (Pin 19) is grounded, producing a 100 Ω DAC output resistance that generates a 1.024 V output when the DAC current is at its full scale of 10.24 mA. The presence external100 Ω will reduce the total output resistance to 50 Ω and the full-scale voltage swing will drop to 0.512 V. Since the bipolar offset current is not used in this configuration, Pin 16 is connected to the analog ground plane.

The input divider has been connected to produce a 5 V full scale reference input by shorting REFIN1 to the analog ground plane and using REFIN2 as the reference input. With a 5 V nominal full scale, the 10% to 120% reference input range falls between 0.5 V and 6 V. The effective input resistance in this mode is 5 kΩ (±20%). The ratio of the input divider has been intentionally skewed by 50 Ω to provide an optional external fine trim for gain adjust. A trim range of ±1% is provided by the 100 Ω trimming potentiometer shown in Figure 7. If trimming is not desired, a 50 Ω resistor may be used in place of the potentiometer to produce the specified gain accuracy, or, if a +1% nominal gain error is tolerable, the resistor may be omitted altogether.

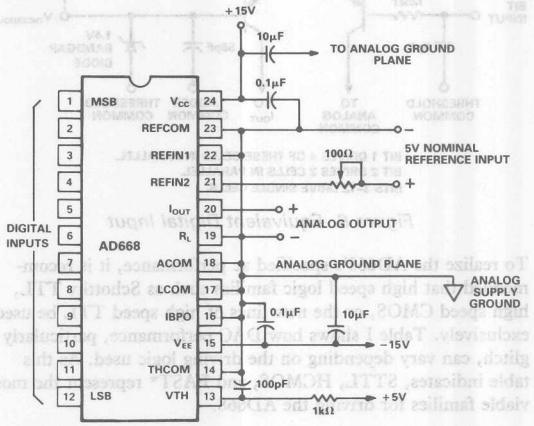


Figure 7. 5 V REFIN/1 V Unbuffered Unipolar Output

1.25 V REFIN, 1 V BIPOLAR, UNBUFFERED VOLTAGE OUTPUT

Figure 8 demonstrates another unbuffered voltage output topology, this time implementing a bipolar output and a 1.25 V reference input. The bipolar output is accomplished simply by tying Pin 16 to the output (Pin 20). Note that in this mode, when the digital inputs are all zeros and the analog input is at 1.25 V, −512 mV will be produced at the DAC output. Bipolar zero (0 V_{OUT}) will be produced when the MSB is ON with all other bits OFF (100 . . . 00), and the full-scale voltage minus 1 LSB (511.75 mV) will be generated when all bits are ON.

The input range of 1.25 V is generated by grounding REFIN2 (through an optional gain trim potentiometer or gain adjust 50 Ω resistor) and using REFIN1 as the reference input. The input resistance in this mode is also 5k.

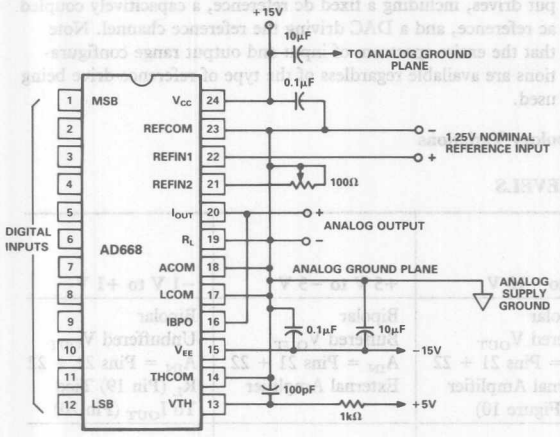


Figure 8. 1.25 V REFIN/± 500 mV Unbuffered Bipolar Output

5 V REFIN, 2 V BIPOLAR, UNBUFFERED VOLTAGE OUTPUT

Figure 9 demonstrates how a larger unbuffered voltage output swing can be realized. R_{LOAD} (Pin 19) is tied to the DAC output (Pin 20) to produce an output resistance of roughly 200 Ω.

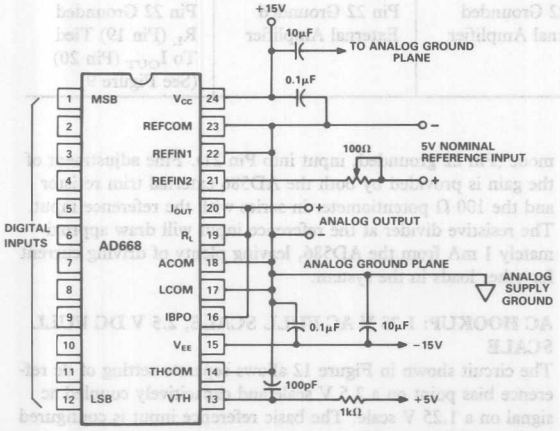


Figure 9. 5 V REFIN/± 1 V Unbuffered Bipolar Output

It should be noted that this impedance is not trimmed, and may vary by as much as 20%, but this can be compensated by adjusting the reference voltage. It is also important to note that limitations in the DAC output compliance would prohibit use of a 2 V unipolar output voltage swing.

1 V REFIN, –10 V UNIPOLAR, BUFFERED VOLTAGE OUTPUT

Figure 10 shows the implementation of the 1 V full scale for the reference input by tying REFIN1 and REFIN2 together and driving them both with the input voltage. This generates a high input impedance, and some care should be taken to insure that the driving impedance at this node is finite at all times to avoid saturating the reference amplifier. This is typically accomplished by a using a low impedance voltage source to drive the reference, but if the topology calls for this source to be switched out, a high impedance (10 kΩ) termination resistor should be used on the REFIN node.

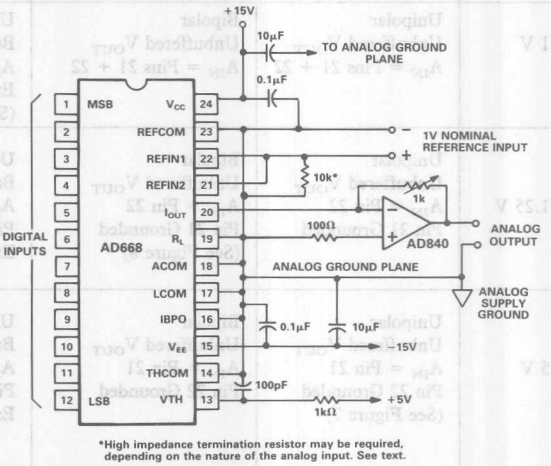


Figure 10. 1 V REFIN/–10 V Unipolar Buffered Output

For full-scale output ranges greater than 2 V, some type of external buffer amplifier is needed. The AD840 fills this requirement perfectly, settling to within 0.025% from a 10 V full-scale step in less than 100 ns. As shown in Figure 10, the amplifier establishes a summing node at ground for the DAC output. The output voltage is determined by the amplifier's feedback resistor (10.24 V for a 1k resistor). Note that since the DAC generates a positive current to ground, the voltage at the amplifier output will be negative. A series resistor between the noninverting amplifier input and ground minimizes the offset effects of op amp input bias currents.

The optimal DAC output impedance in buffered output applications depends on the buffer amplifier being used. The AD840 is stable at a gain of 10, so a lower DAC output impedance (higher noise gain) is desired for stability reasons, and R_{LOAD} should be grounded. The 100 Ω DAC output impedance produces a noise gain of 11 with the 1k feedback resistor. If the gain-of-two stable AD842 is used as a buffer, a 200 Ω DAC output impedance will produce a stable configuration with lower noise gain to the output; hence, R_{LOAD} should be connected to the DAC output.

As noted earlier, these four examples are part of an array of possible configurations available. Table II provides a quick reference chart for the more straightforward applications, but many other input and output signals are possible with some modifications.

The next three circuits provide examples of different analog input drives, including a fixed dc reference, a capacitively coupled ac reference, and a DAC driving the reference channel. Note that the entire spectrum of input and output range configurations are available regardless of the type of reference drive being used.

Table II. AD668 Topology Variations

	OUTPUT LEVELS				
Nominal Analog Input	**0 V to 1 V**	**−500 mV to +500 mV**	**0 V to −10 V**	**+5 V to −5 V**	**−1 V to +1 V**
1 V	Unipolar Unbuffered V_{OUT} A_{IN} = Pins 21 + 22	Bipolar Unbuffered V_{OUT} A_{IN} = Pins 21 + 22	Unipolar Buffered V_{OUT} A_{IN} = Pins 21 + 22 External Amplifier (See Figure 10)	Bipolar Buffered V_{OUT} A_{IN} = Pins 21 + 22 External Amplifier	Bipolar Unbuffered V_{OUT} A_{IN} = Pins 21 + 22 R_L (Pin 19) Tied To I_{OUT} (Pin 20)
1.25 V	Unipolar Unbuffered V_{OUT} A_{IN} = Pin 22 Pin 21 Grounded	Bipolar Unbuffered V_{OUT} A_{IN} = Pin 22 Pin 21 Grounded (See Figure 8)	Unipolar Buffered V_{OUT} A_{IN} = Pin 22 Pin 21 Grounded External Amplifier	Bipolar Buffered V_{OUT} A_{IN} = Pin 22 Pin 21 Grounded External Amplifier	Bipolar Unbuffered V_{OUT} A_{IN} = Pin 22 Pin 21 Grounded R_L (Pin 19) Tied To I_{OUT} (Pin 20)
5 V	Unipolar Unbuffered V_{OUT} A_{IN} = Pin 21 Pin 22 Grounded (See Figure 7)	Bipolar Unbuffered V_{OUT} A_{IN} = Pin 21 Pin 22 Grounded	Unipolar Buffered V_{OUT} A_{IN} = Pin 21 Pin 22 Grounded External Amplifier	Bipolar Buffered V_{OUT} A_{IN} = Pin 21 Pin 22 Grounded External Amplifier	Bipolar Unbuffered V_{OUT} A_{IN} = Pin 21 Pin 22 Grounded R_L (Pin 19) Tied To I_{OUT} (Pin 20) (See Figure 9)

DC REFERENCE: THE AD586 DRIVING THE AD668

Figure 11 illustrates one of the more obvious analog input sources: a fixed reference. The AD586 produces a temperature-stable 5 V analog output to drive the AD668 in the 5 V input mode (Pin 22 grounded, input into Pin 21). Fine adjustment of the gain is provided by both the AD586 external trim resistor and the 100 Ω potentiometer in series with the reference input. The resistive divider at the reference input will draw approximately 1 mA from the AD586, leaving plenty of driving current for other loads in the system.

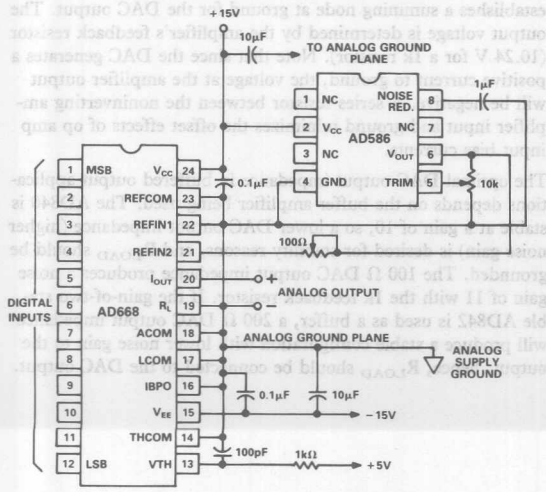


Figure 11. AD586 Driving the AD668

AC HOOKUP: 1.25 V AC FULL SCALE, 2.5 V DC FULL SCALE

The circuit shown in Figure 12 allows separate setting of dc reference bias point on a 2.5 V scale and capacitively coupled ac signal on a 1.25 V scale. The basic reference input is configured in the 1.25 V mode (Pin 21 grounded, Pin 22 used as the reference input.) The 2.5 V dc range is achieved by using an external 5k series resistor in the dc path. Note that because of the relatively wide tolerance (±20%) in the absolute value of the AD668's internal input divider resistors, substantial gain range adjustment should be provided in the external series resistance.

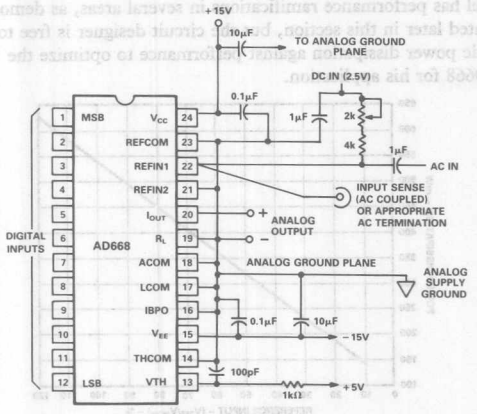


Figure 12. AC Hookup

DAC DRIVE: THE AD568 DRIVING THE AD668

The circuit shown in Figure 13 produces an analog output proportional to the product of two digital inputs. The AD568 has an on-board fixed reference and generates a full-scale output voltage of 1.024 V (just as the AD668 does in its unbuffered voltage output mode). This output voltage can be used to directly drive the AD668 in the 1 V reference input mode. Note that in this case, the lower 410 codes of the AD568 are out-of-bounds; they produce an undervoltage condition at the AD668 reference input. While the two DACs are similar in many ways, the optimal decoupling schemes differ between the two parts and care should be used to insure that each is implemented appropriately.

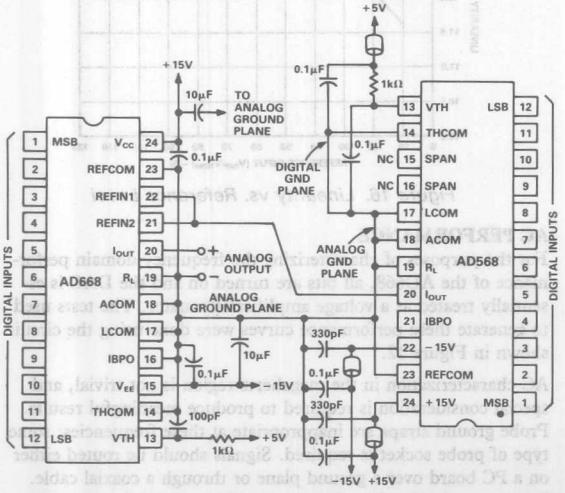
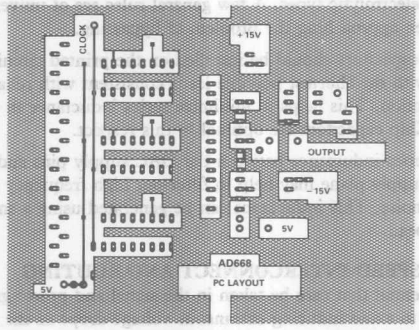


Figure 13. AD568 Driving the AD668

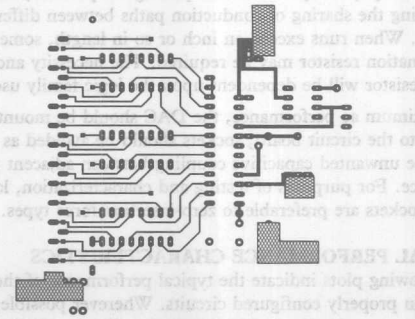
CONSTRUCTION GUIDELINES

HIGH FREQUENCY PRINTED CIRCUIT BOARD SUGGESTIONS

In systems seeking to simultaneously achieve high speed and high accuracy, the implementation and construction of the circuit is often as important as the circuit's design. Proper RF techniques must be used in device selection, placement and routing, and supply bypassing and grounding. In many areas, the performance of the AD668 may exceed the measurement capabilities of common lab instruments, making performance evaluation particularly difficult. The AD668 has been configured to be relatively easy to use in spite of these problems, and realization of the performance indicated in this datasheet should not be difficult if proper care is taken. Figure 14 provides an illustration of the printed circuit board layout used for much of the AD668's characterization. The board represents an implementation of the circuit shown in Figure 23, with the AD586 used to drive the reference channel (as in Figure 11).



Component Side



Foil Side

Figure 14. PC Board Layout

THE USE OF GROUND AND POWER PLANES

If properly implemented, ground planes can perform a myriad of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from one another, with the analog ground plane confined to areas covering analog signal traces and the digital ground plane confined to areas covering digital interconnect. The two ground planes should be connected by paths 1/4 inch to 1/2 inch wide on both sides of the DAC, as shown in Figure 14. Care should be taken to insure

On the digital side, this includes the digital input lines running to the DAC, as well as any clock signals. On the analog side, this includes the analog input signal, the DAC output signal, and the supply feeders. The use of wide runs or planes in the routing of the power supplies is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane.

USING THE RIGHT BYPASS CAPACITORS

The capacitors used to bypass the power supplies are probably the most important external components in any high speed design. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configuration. The dominant consideration in the selection of bypass capacitors for the AD668 is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and film type capacitors generally feature lower series inductance than tantalum or electrolytic types. A few general rules are of universal use when approaching the problem of bypassing.

Bypass capacitors should be installed on the printed circuit board with the shortest possible leads consistent with reliable construction. This helps to minimize series inductance in the leads. Chip capacitors are optimal in this respect.

Some series inductance between the DAC supply pins and the power supply plane may help to filter-out high frequency power supply noise. This inductance can be generated using a small ferrite bead.

HIGH SPEED INTERCONNECT AND ROUTING

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. It is suggested that all connections be short, direct, and as physically close to the package as possible, thereby minimizing the sharing of conduction paths between different currents. When runs exceed an inch or so in length, some type of termination resistor may be required. The necessity and value of this resistor will be dependent upon the logic family used.

For maximum ac performance, the DAC should be mounted directly to the circuit board; sockets should be avoided as they introduce unwanted capacitive coupling between adjacent pins of the device. For purposes of testing and characterization, low profile sockets are preferable to zero-insertion force types.

TYPICAL PERFORMANCE CHARACTERISTICS

The following plots indicate the typical performance of the AD668 in properly configured circuits. Wherever possible, suggestions are provided to assist the user in achieving the indicated performance levels.

DC PERFORMANCE

Power Consumption vs. V_{REF}/V_{NOM}

As suggested in previous sections, most portions of AD668's current budget are proportional to the analog input signal. As a result, operating the part at a reduced reference voltage offers substantial power savings. This may be particularly attractive in applications featuring a buffered output voltage, since the size of the feedback resistor may be increased to compensate for the reduced DAC current. For example, the DAC could be configured in the 5 V input mode, but driven with a 2.5 V reference, level has performance ramifications in several areas, as demonstrated later in this section, but the circuit designer is free to trade power dissipation against performance to optimize the AD668 for his application.

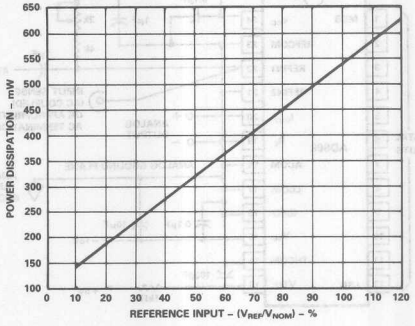


Figure 15. Power Consumption vs. Reference Level

Linearity vs. V_{REF}/V_{NOM}

At reduced current levels, the linearity of the PNP DAC used in the AD668 becomes more sensitive to the mismatch in transistor V_{BE}'s. As Figure 16 indicates, this effect starts to increase fairly dramatically for reference levels less than 25% of nominal. Increasing the current level above 100% does not appreciably improve the linearity performance since the DAC has been trimmed to perform optimally at the 100% reference level.

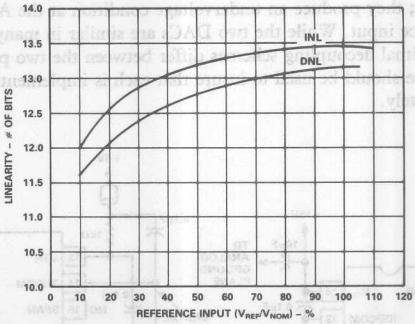


Figure 16. Linearity vs. Reference Level

AC PERFORMANCE

For the purposes of characterizing the frequency domain performance of the AD668, all bits are turned on and the DAC is essentially treated as a voltage amplifier/attenuator. The tests used to generate these performance curves were done using the circuit shown in Figure 12.

AC characterization in the megahertz region is not trivial, and special consideration is required to produce meaningful results. Probe ground straps are inappropriate at these frequencies; some type of probe socket is required. Signals should be routed either on a PC board over a ground plane or through a coaxial cable. Proper termination impedances should be used throughout the fixturing.

Large Signal Frequency Response

Figure 17 represents the gain and phase response of a signal swinging from 10% to 120% (peak to peak) of the nominal reference input. The DAC reference amplifier has an effective slew

rate or 30 V/μs at the DAC output, so there will be slew-induced distortion for full scale swings at greater than 10 MHz.

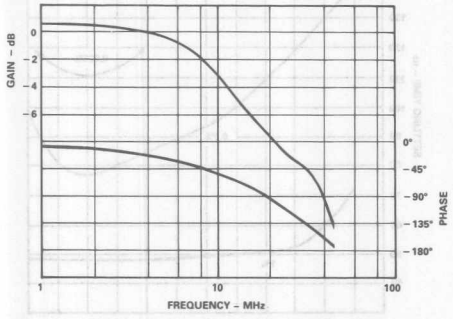


Figure 17. Large Signal Gain and Phase Response

Small Signal 3 dB Bandwidth vs. V_{REF}/V_{NOM}

Figure 18 demonstrates the small signal (20% of nominal reference) bandwidth sensitivity to the analog input's dc bias. The small signal 3 dB bandwidth at 100% reference levels is greater than 15 MHz, but the bandwidth remains greater than 10 MHz over the entire nominal reference range. The differential gain and phase for a 200 mV, 3 MHz signal are 0.5% and 2°, respectively.

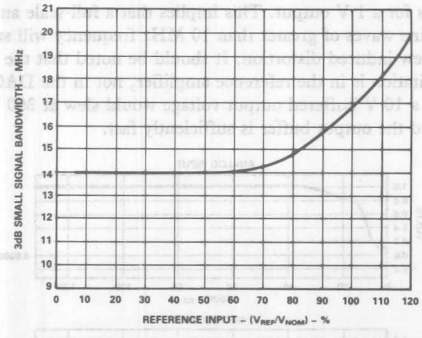


Figure 18. Small Signal Bandwidth vs. DC Reference Level

Noise Spectrum

Figure 19 shows the noise spectrum of the DAC with all bits on. The noise floor of −78 dB is just above the noise floor of the instrument being used, in part due to the relatively small (1 V) output signal of the DAC in voltage out mode.

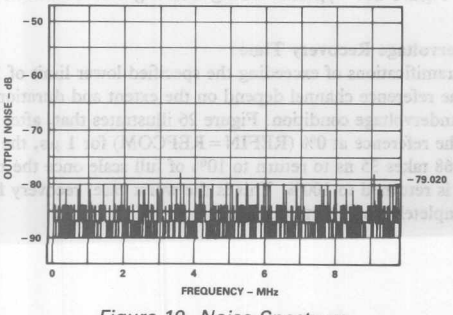


Figure 19. Noise Spectrum

Analog Feedthrough vs. Frequency

Analog feedthrough is a measure of the effective signal at the DAC output when all bits are off and a full-scale signal is placed at the analog input. At dc, the feedthrough is a result of analog input dependent ground drops, predominantly through the ladder ground. Good grounding practices will minimize this effect. At high frequencies, the signal may propagate to the output through a variety of capacitive paths. Proper shielding and routing should be implemented to eliminate external coupling between the analog input and the DAC output node.

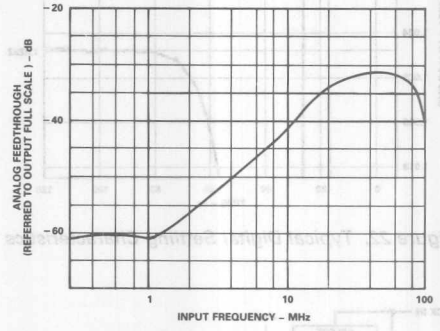


Figure 20. Analog Feedthrough vs. Frequency

Reference Channel THD

THD, or total harmonic distortion, is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental and is expressed in dBs. Figure 21 shows the typical THD of the AD668 reference channel for both large and small signals.

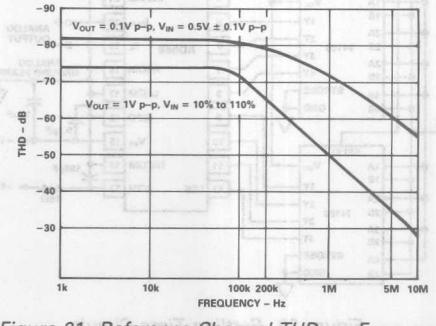


Figure 21. Reference Channel THD vs. Frequency

TRANSIENT PERFORMANCE

High accuracy settling time measurements of less than one hundred nanoseconds are extremely difficult to make. The conventional analog amplifiers used in oscilloscope front ends, typically, cannot recover from the overdrive resulting from a full-scale step in sufficient time. Sampling scopes can track much quicker rise times but often provide insufficient accuracy for 12-bit characterization. Data Precision's new 640 sampling scope provides a good combination of speed and resolution that provides just enough performance to measure the AD668's performance.

Digital Settling Time

Figure 22 illustrates the typical settling characteristic of the AD668 to a full-scale change in digital inputs with the analog input fixed at 100%. The digital driving circuity is shown in Figure 23. This circuit allows the DAC to be toggled between any two codes, and so provides an excellent means of characterizing both settling and glitch performance.

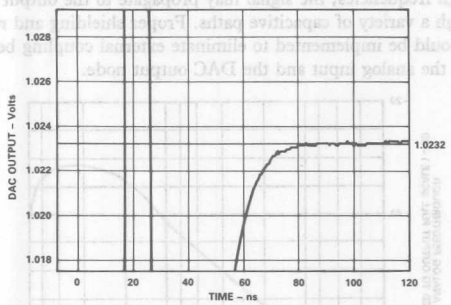


Figure 22. Typical Digital Settling Characteristics

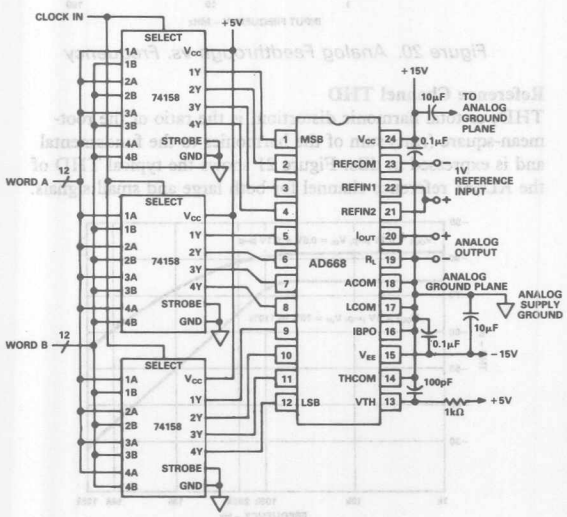


Figure 23. Settling Time Circuit

Digital Settling Time vs. V_{REF}

The reference amplifier loop has been compensated for optimal settling performance at $V_{REF}/V_{NOM} = 100\%$, but as Figure 24 indicates, there is relatively little degradation in settling performance for a wide range of reference levels. Consideration of Figures 15, 16, and 24 support that a 1/2 power solution would see very little degradation in speed or accuracy performance.

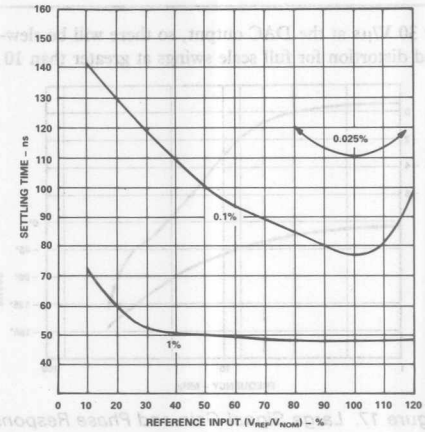


Figure 24. Digital Settling Time vs. Reference Level

Analog Settling Time

One of the biggest challenges in measuring the settling time of a high accuracy amplifier is producing a clean waveform with which to drive the input. In this case, an AD568 was used to drive the analog channel in the 1 V input mode (see Figure 13).

As indicated by Figure 25, the referred-to-output slew rate is 30 V/µs for a 1 V output. This implies that a full-scale analog input sine waves of greater than 10 MHz frequency will suffer some slew-induced distortion. It should be noted that the slewing limitation is in the reference amplifier, not in the DAC output, so a 10 V buffered output voltage would slew at 300 V/µs, provided the output buffer is sufficiently fast.

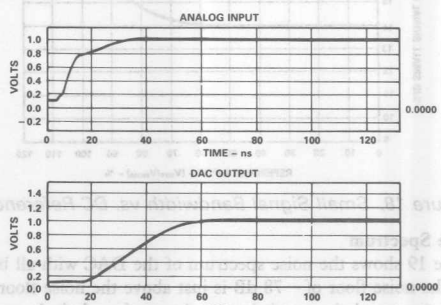


Figure 25. Typical Analog Settling Characteristic

Undervoltage Recovery Time

The ramifications of exceeding the specified lower limit of 10% on the reference channel depend on the extent and duration of the undervoltage condition. Figure 26 illustrates that, after holding the reference at 0% (REFIN = REFCOM) for 1 µs, the AD668 takes 35 ns to return to 10% of full scale once the reference is returned to 100%. This is the worst case: recovery from a completely "off" condition.

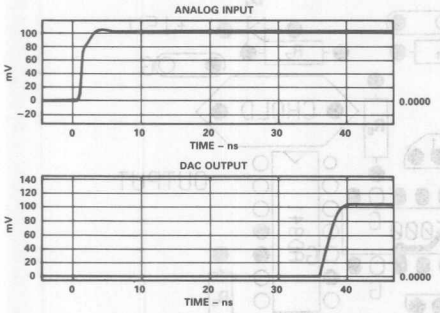


Figure 26. Undervoltage Recovery

Glitch Impulse

The AD668's glitch at the major carry is illustrated in Figure 2. The AD668 features a conventional DAC architecture that has two basic glitch mechanisms: digital feedthrough and data skew. Careful consideration of these mechanisms will help the glitch-conscious user minimize glitch in his application.

Digital Feedthrough

As with any converter product, a high speed digital-to-analog converter is forced to exist on the frontier between the noisy environment of high speed digital logic and the sensitive analog domain. The problems of this interfacing are particularly acute when demands of high speed (greater than 10MHz switching times) and high precision (12 bits or more) are combined. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of a digital input signal with a 2 ns rise time. Inevitably, once this digital signal is brought onto the chip, some of its higher frequency components will find their way to the sensitive analog nodes, producing a digital feedthrough glitch. To minimize the exposure to this effect, the AD668 has intentionally omitted the on-board latches that have been included in many slower DACs. This not only reduces the overall level of digital activity on chip, it also avoids bringing a latch clock pulse on board, whose opposite edge inevitably produces a substantial glitch, even when the DAC is not supposed to be changing codes.

Data Skew

The AD668, like many of its slower predecessors, essentially uses each digital input line to switch a separate, weighted current to either the output (I_{OUT}) or some other node (ANALOG COM). If the input bits are not changed simultaneously, or if the different DAC bits switch at different speeds, then the DAC output current will momentarily take on some incorrect value. This effect is particularly troublesome at the "carry points," where the DAC output is to change by only one LSB, but several of the larger current sources must be switched to realize this change. Data skew can allow the DAC output to move a substantial amount towards full scale or zero (depending upon the direction of the skew) when only a small transition is desired. Great care was taken in the design and layout of the AD668 to ensure that switching times of the DAC switches are symmetrical and that the length of the input data lines are short and well matched. The glitch-sensitive user should be equally diligent about minimizing the data skew at the AD668's inputs, particularly for the 4 or 5 most significant bits. This can be achieved by using the proper logic family and gate to drive the DAC, and keeping the interconnect lines between the log outputs and the DAC inputs as short and as well matched as possible, particularly for the most significant bits. The top 6 bits should be driven from the same latch chip if latches are used.

DEGLITCHING FOR PRECISION WAVEFORM GENERATION

There are high speed SHAs available with specifications sufficient to deglitch the AD668, however most are hybrid in design at costs which can be prohibitive. A high performance, low cost alternative shown in Figure 27 is a discrete SHA utilizing a high speed monolithic op amp and high speed DMOS FET switches.

This SHA circuit uses the inverting integrator architecture. The AD841 operational amplifier used (300 MHz gain bandwidth product) is fabricated on the same high speed process as the AD668. The time constant formed by the 100 Ω resistor and the 100 pF capacitor determines the acquisition time and also band limits the output signal to eliminate slew induced distortion.

A discrete drive circuit is used to achieve the best performance from the SD5000 quad DMOS switch. This switch driving cell is composed of MPS571 RF npn transistors and an MC10124 TTL to ECL translator. Using this technique provides both high speed and highly symmetrical drive signals for the SD5000 switches. The switches are arranged in a single-throw double-pole (SPDT) configuration. The 360 pF "flyback" capacitor is switched to the op amp summing junction during the hold mode to keep switching transients from feeding to the output. This capacitor is grounded during sample mode to minimize its effect on acquisition time.

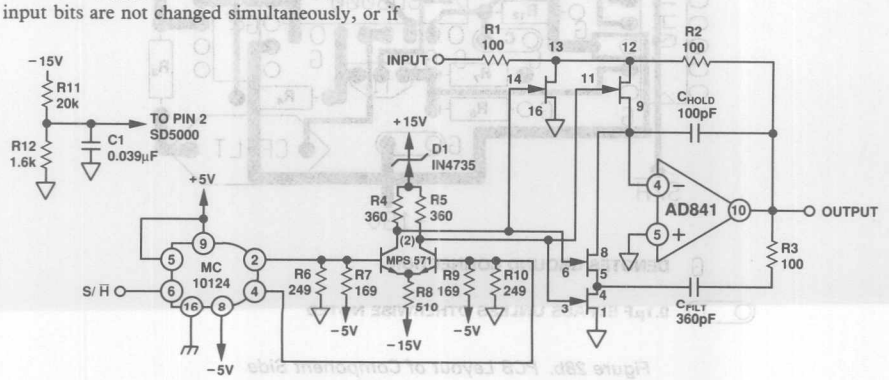


Figure 27. High Performance, Low Cost Deglitching Circuit

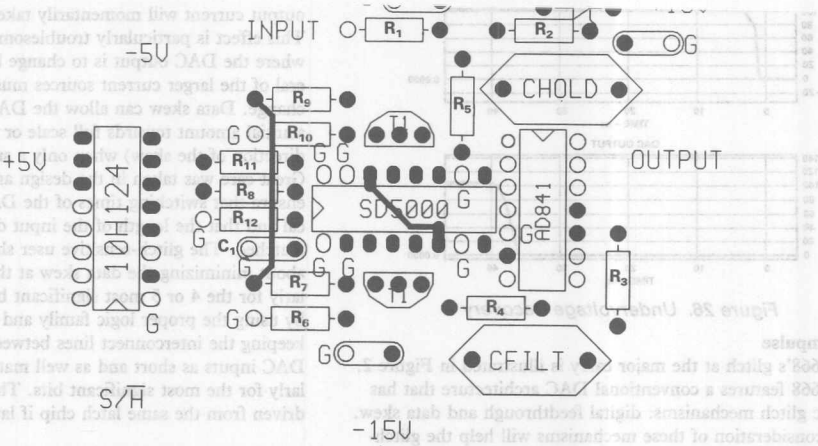


Figure 28a. PCB Layout of Foil Side

Circuit layout for a high speed deglitcher is almost as critical as the design itself. Figure 28 shows the recommended layout of the deglitching cell for a double-sided printed circuit board. The layout is very compact with care taken that all critical signal paths are short.

Performance of the AD668 in waveform generation applications is greatly improved with the use of this deglitching method. Peak harmonics and spurious free dynamic range are typically maintained at −70 dB to −75 dB with update rates up to 10 MHz.

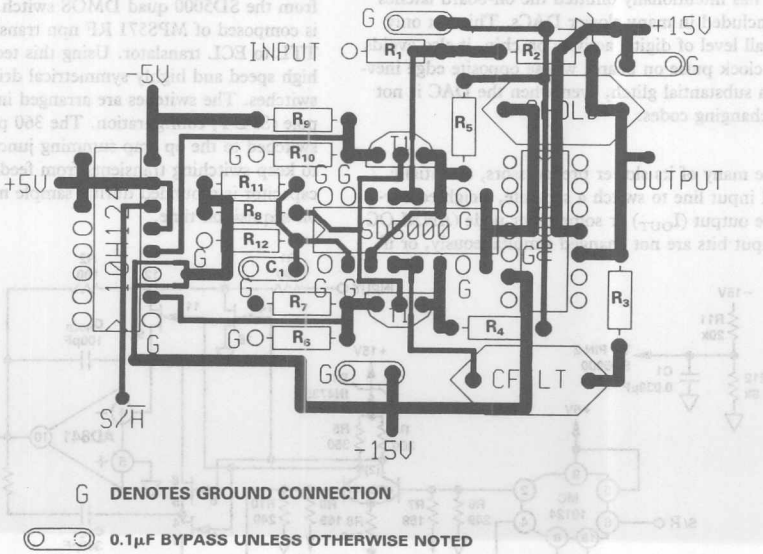


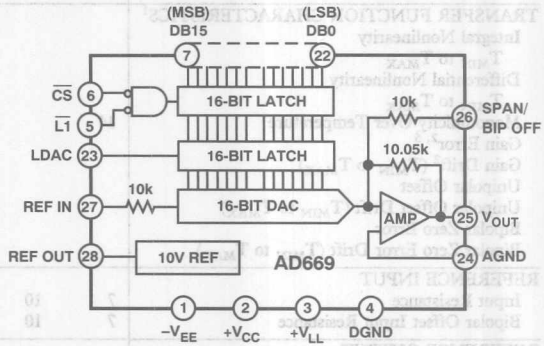
Figure 28b. PCB Layout of Component Side

AD669

FEATURES

- Complete 16-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Monolithic BiMOS II Construction
- ±1 LSB Integral Linearity Error
- 15-Bit Monotonic over Temperature
- Microprocessor Compatible
  - 16-Bit Parallel Input
  - Double-Buffered Latches
  - Fast 40 ns Write Pulse
- Unipolar or Bipolar Output
- Low Glitch: 15 nV-s
- Low THD+N: 0.009%
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD669 DACPORT™ is a complete 16-bit monolithic D/A converter with an on-board reference and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD669 chip includes current switches, decoding logic, an output amplifier, a buried Zener reference and double-buffered latches.

The AD669's architecture insures 15-bit monotonicity over temperature. Integral nonlinearity is maintained at ±0.003%, while differential nonlinearity is ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 μs to within 1/2 LSB for a full-scale step.

Data is loaded into the AD669 in a parallel 16-bit format. The double-buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system. Three TTL/LSTTL/5 V CMOS compatible signals control the latches: $\overline{CS}$, $\overline{LI}$ and LDAC.

The output range of the AD669 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V.

The AD669 is available in seven grades: AN and BN versions are specified from −40°C to +85°C and are packaged in a 28-pin plastic DIP. The AR and BR versions are specified for −40°C to +85°C operation and are packaged in a 28-pin SOIC. The AQ and BQ versions are also specified from −40°C to +85°C, while the SQ version is specified from −55°C to +125°C. The AQ, BQ and SQ versions are all packaged in a hermetic 28-pin cerdip package. The AD669 is also available compliant to MIL-STD-883. Refer to the AD669/883B data sheet for specifications and test conditions.

PRODUCT HIGHLIGHTS

1. The AD669 is a complete voltage output 16-bit DAC with voltage reference and digital latches on a single IC chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.2% maximum error. The reference voltage is also available for external applications.
3. The AD669 is both dc and ac specified. DC specs include ±1 LSB INL error and ±1 LSB DNL error. AC specs include 0.009% THD+N and 0.0063% SNR. The ac specifications make the AD669 suitable for signal generation applications.
4. The double-buffered latches on the AD669 eliminate data skew errors while allowing simultaneous updating of DACs in multi-DAC systems.
5. The output range is a pin-programmable unipolar 0 V to +10 V or bipolar −10 V to +10 V output. No external components are necessary to set the desired output range.
6. The AD669 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD669/883B data sheet for detailed specifications.

DACPORT is a trademark of Analog Devices, Inc.

AD669—SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V unless otherwise stated)

Model	AD669AN/AR Min	AD669AN/AR Typ	AD669AN/AR Max	AD669AQ/SQ Min	AD669AQ/SQ Typ	AD669AQ/SQ Max	AD669BN/BQ/BR Min	AD669BN/BQ/BR Typ	AD669BN/BQ/BR Max	Units
RESOLUTION	16			16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})										
V_{IH} (Logic "1")	2.0		5.5	*		*	*		*	Volts
V_{IL} (Logic "0")	0		0.8	*		*	*		*	Volts
I_{IH} (V_{IH} = 5.5 V)			±10			*			*	μA
I_{IL} (V_{IL} = 0 V)			±10			*			*	μA
TRANSFER FUNCTION CHARACTERISTICS[1]										
Integral Nonlinearity			±2			*			±1	LSB
T_{MIN} to T_{MAX}			±4			*			±2	LSB
Differential Nonlinearity			±2			*			±1	LSB
T_{MIN} to T_{MAX}			±4			*			±2	LSB
Monotonicity Over Temperature	14			14			15			Bits
Gain Error[2, 5]			±0.15			±0.10			±0.10	% of FSR
Gain Drift[2] (T_{MIN} to T_{MAX})			25			15			15	ppm/°C
Unipolar Offset			±5			±5			±2.5	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			5			3			3	ppm/°C
Bipolar Zero Error			±15			±15			±10	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			12			10			5	ppm/°C
REFERENCE INPUT										
Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
REFERENCE OUTPUT										
Voltage	9.98	10.00	10.02	*	*	*	*	*	*	Volts
Drift			25			15			15	ppm/°C
External Current[3]	2	4		*	*		*	*		mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
OUTPUT CHARACTERISTICS										
Output Voltage Range										
Unipolar Configuration	0		+10	*		*	*		*	Volts
Bipolar Configuration	−10		+10	*		*	*		*	Volts
Output Current	5			*			*			mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
POWER SUPPLIES										
Voltage										
V_{CC}[4]	+13.5		+16.5	*		*	*		*	Volts
V_{EE}[4]	−13.5		−16.5	*		*	*		*	Volts
V_{LL}	+4.5		+5.5	*		*	*		*	Volts
Current (No Load)										
I_{CC}		+12	+18		*	*		*	*	mA
I_{EE}		−12	−18		*	*		*	*	mA
I_{LL}										
@ V_{IH}, V_{IL} = 5, 0 V		0.3	2		*	*		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	7.5		*	*		*	*	mA
Power Supply Sensitivity		1	3		*	*		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*			*		mW
TEMPERATURE RANGE										
Specified Performance (A, B)	−40		+85	−40		+85	−40		+85	°C
Specified Performance (S)				−55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of FSR. For 14-bit resolution 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V for a 0 to +10 V span and 20 V for a −10 V to +10 V span.

[2]Gain error and gain drift measured using the internal reference. Gain drift is primarily reference related. See the Using the AD669 with the AD688 Reference section for further information.

[3]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD669.

[4]Operation on ±12 V supplies is possible using an external reference like the AD586 and reducing the output range. Refer to the Internal/External Reference Use section.

[5]Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode). Refer to the Analog Circuit Connections section.

*Same as AD669AN/AR specification.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

(With the exception of Total Harmonic Distortion + Noise and Signal-to-Noise Ratio, these characteristics are included for design guidance only and are not subject to test. THD+N and SNR are 100% tested. $T_{MIN} \le T_A \le T_{MAX}$, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V except where stated.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, T_A = +25°C
(Time to ±0.0008% FS	8	µs typ	20 V Step, T_A = +25°C
with 2 kΩ, 1000 pF Load)	10	µs typ	20 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	6	µs typ	10 V Step, T_A = +25°C
	8	µs typ	10 V Step $T_{MIN} \le T_A \le T_{MAX}$
	2.5	µs typ	1 LSB Step, $T_{MIN} \le T_A \le T_{MAX}$
Total Harmonic Distortion + Noise			
A, B, S Grade	**0.009**	% max	0 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
A, B, S Grade	**0.056**	% max	−20 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
A, B, S Grade	**5.6**	% max	−60 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
Signal-to-Noise Ratio	**0.0063**	% max	A-Weight Filter; T_A = +25°C
Digital-to-Analog Glitch Impulse	15	nV-s typ	DAC Alternately Loaded with 8000H and 7FFFH
Digital Feedthrough	2	nV-s typ	DAC Alternately Loaded with 0000H and FFFFH; $\overline{CS}$ High
Output Noise Voltage Density (1 kHz – 1 MHz)	120	nV/$\sqrt{Hz}$ typ	Measured at V_{OUT}, 20 V Span; Excludes Reference
Reference Noise	125	nV/$\sqrt{Hz}$ typ	Measured at REF OUT

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

TIMING CHARACTERISTICS

V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V

Parameter	Limit +25°C	Limit −40°C to +85°C	Limit −55°C to +125°C	Units
(Figure 1a)				
$t_{\overline{CS}}$	40	50	55	ns min
$t_{\overline{L1}}$	40	50	55	ns min
t_{DS}	30	35	40	ns min
t_{DH}	10	10	15	ns min
t_{LH}	90	110	120	ns min
t_{LW}	40	45	45	ns min
(Figure 1b)				
t_{LOW}	130	150	165	ns min
t_{HIGH}	40	45	45	ns min
t_{DS}	120	140	150	ns min
t_{DH}	10	10	15	ns min

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

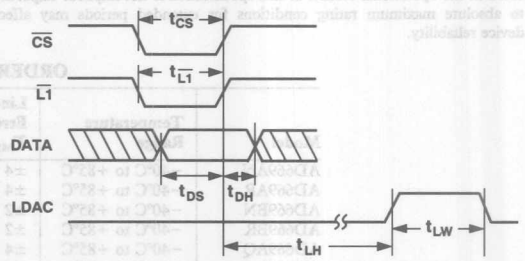
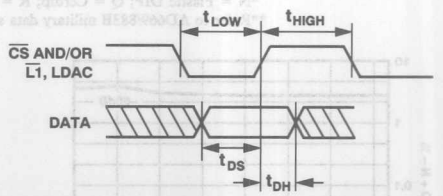


Figure 1a. AD669 Level Triggered Timing Diagram



TIE $\overline{CS}$ AND/OR $\overline{L1}$ TO GROUND OR TOGETHER WITH LDAC

Figure 1b. AD669 Edge Triggered Timing Diagram

ESD SENSITIVITY

The AD669 features input protection circuitry consisting of large transistors and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD669 has been classified as a Class 2 device.



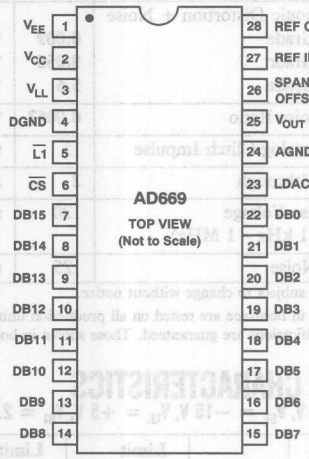
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND . . . . . −0.3 V to +17.0 V
V_{EE} to AGND . . . . . +0.3 V to −17.0 V
V_{LL} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . ±1 V
Digital Inputs (Pins 5 through 23) to DGND . . . . . −1.0 V to +7.0 V
REF IN to AGND . . . . . ±10.5 V
Span/Bipolar Offset to AGND . . . . . ±10.5 V
Ref Out, V_{OUT} . . . . . Indefinite Short To AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C . . . . . 1000 mW
Derates above +60°C . . . . . 8.7 mW/°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

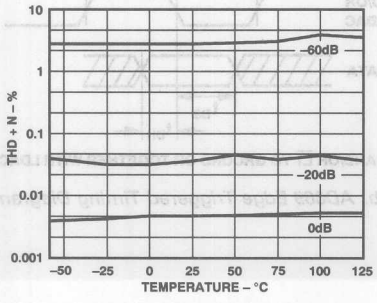
PIN CONFIGURATION



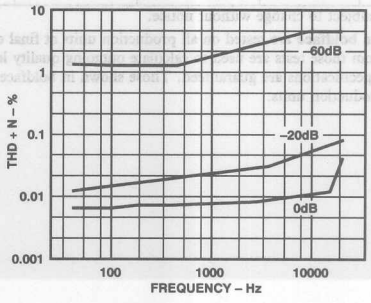
ORDERING GUIDE

Model	Temperature Range	Linearity Error Max T_{MIN} – T_{MAX}	Gain TC max ppm/°C	Package Description	Package Option*
AD669AN	−40°C to +85°C	±4 LSB	25	Plastic DIP	N-28
AD669AR	−40°C to +85°C	±4 LSB	25	SOIC	R-28
AD669BN	−40°C to +85°C	±2 LSB	15	Plastic DIP	N-28
AD669BR	−40°C to +85°C	±2 LSB	15	SOIC	R-28
AD669AQ	−40°C to +85°C	±4 LSB	15	Cerdip	Q-28
AD669BQ	−40°C to +85°C	±2 LSB	15	Cerdip	Q-28
AD669SQ	−55°C to +125°C	±4 LSB	15	Cerdip	Q-28
AD669/883B**	−55°C to +125°C	**	**	**	**

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
**Refer to AD669/883B military data sheet.



THD+N vs. Temperature



THD+N vs. Frequency

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS–1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be within ±1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured with all 0s loaded in the DAC.

BIPOLAR ZERO ERROR: When the AD669 is connected for bipolar output and 10 . . . 000 is loaded in the DAC, the deviation of the analog output from the ideal midscale value of 0 V is called the bipolar zero error.

DRIFT: Drift is the change in a parameter (such as gain, offset and bipolar zero) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

TOTAL HARMONIC DISTORTION + NOISE: Total harmonic distortion + noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending upon the amplitude of the output signal. Therefore, to be the most useful, THD+N should be specified for both large and small signal amplitudes.

SIGNAL-TO-NOISE RATIO: The signal-to-noise ratio is defined as the ratio of the output with no signal present to the amplitude of the output when a full-scale signal is present. This is measured with a standard A-weight filter.

DIGITAL-TO-ANALOG GLITCH IMPULSE: This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is measured at half scale when the DAC switches around the MSB and as many as possible switches change state, i.e., from 011 . . . 111 to 100 . . . 000.

DIGITAL FEEDTHROUGH: When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

THEORY OF OPERATION

The AD669 uses an array of bipolar current sources with MOS current steering switches to develop a current proportional to the applied digital word, ranging from 0 to 2 mA. A segmented architecture is used, where the most significant four data bits are thermometer decoded to drive 15 equal current sources. The lesser bits are scaled using a R–2R ladder, then applied together with the segmented sources to the summing node of the output amplifier. The internal span/bipolar offset resistor can be connected to the DAC output to provide a 0 V to +10 V span, or it can be connected to the reference input to provide a −10 V to +10 V span.

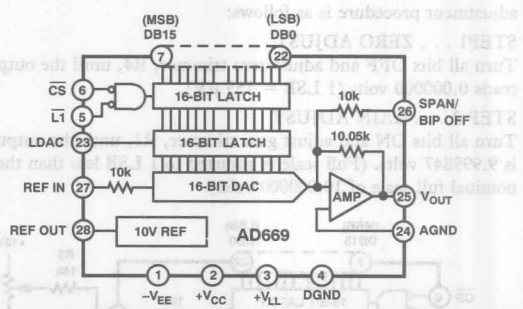


Figure 2. AD669 Functional Block Diagram

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD669 may be connected to produce a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. Gain and offset drift are minimized in the AD669 because of the thermal tracking of the scaling resistors with other device components.

UNIPOLAR CONFIGURATION

The configuration shown in Figure 3a will provide a unipolar 0 V to +10 V output range. In this mode, 50 Ω resistors are tied between the span/bipolar offset terminal (Pin 26) and V_{OUT} (Pin 25), and between REF OUT (Pin 28) and REF IN (Pin 27). It is possible to use the AD669 without any external components by tying Pin 28 directly to Pin 27 and Pin 26 directly to Pin 25. Eliminating these resistors will increase the gain error by 0.25% of FSR.

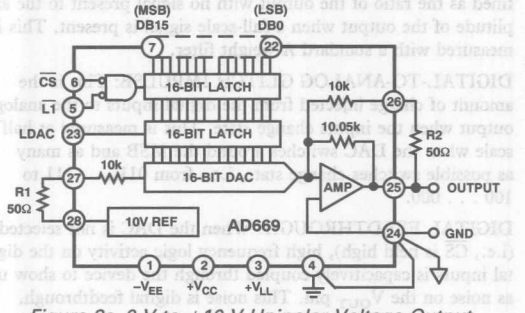


Figure 3a. 0 V to +10 V Unipolar Voltage Output

If it is desired to adjust the gain and offset errors to zero, this can be accomplished using the circuit shown in Figure 3b. The adjustment procedure is as follows:

STEP1 . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R4, until the output reads 0.000000 volts (1 LSB = 153 μV).

STEP 2 . . . GAIN ADJUST

Turn all bits ON and adjust gain trimmer, R1, until the output is 9.999847 volts. (Full scale is adjusted to 1 LSB less than the nominal full scale of 10.000000 volts).

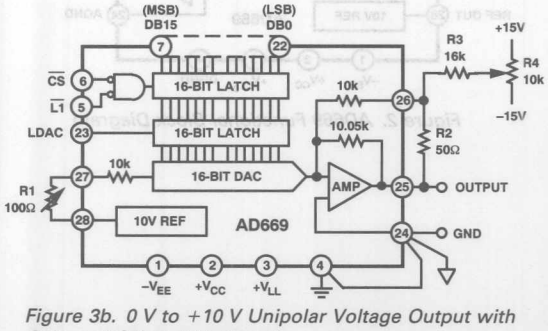


Figure 3b. 0 V to +10 V Unipolar Voltage Output with Gain and Offset Adjustment

BIPOLAR CONFIGURATION

The circuit shown in Figure 4a will provide a bipolar output voltage from −10.000000 V to +9.999694 V with positive full scale occurring with all bits ON. As in the unipolar mode, resistors R1 and R2 may be eliminated altogether to provide AD669 bipolar operation without any external components. Eliminating these resistors will increase the gain error by 0.50% of FSR in the bipolar mode.

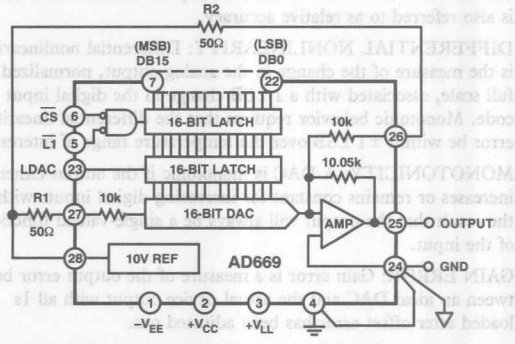


Figure 4a. ±10 V Bipolar Voltage Output

Gain offset and bipolar zero errors can be adjusted to zero using the circuit shown in Figure 4b as follows:

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust trimmer R2 to give −10.000000 volts output.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust R1 to give a reading of +9.999694 volts.

STEP III . . . BIPOLAR ZERO ADJUST (Optional)

In applications where an accurate zero output is required, set the MSB ON, all other bits OFF, and readjust R2 for zero volts output.

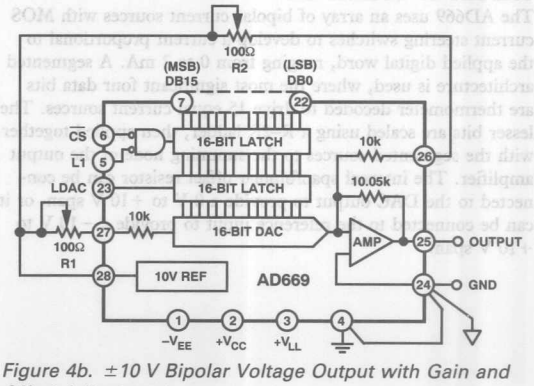


Figure 4b. ±10 V Bipolar Voltage Output with Gain and Offset Adjustment

It should be noted that using external resistors will introduce a small temperature drift component beyond that inherent in the AD669. The internal resistors are trimmed to ratio-match and temperature-track other resistors on chip, even though their absolute tolerances are ±20% and absolute temperature coefficients are approximately −50 ppm/°C. In the case that external resistors are used, the temperature coefficient mismatch between internal and external resistors, multiplied by the sensitivity of the circuit to variations in the external resistor value, will be the resultant additional temperature drift.

INTERNAL/EXTERNAL REFERENCE USE

The AD669 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener diode references. The performance of the AD669 is specified with the internal reference driving the DAC since all trimming and testing (especially for gain and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 1 mA to REF IN and 1 mA to BIPOLAR OFFSET). A minimum of 2 mA is available for driving external loads. The AD669 reference output should be buffered with an external op amp if it is required to supply more than 4 mA total current. The reference is tested and guaranteed to ±0.2% max error. The temperature coefficient is comparable to that of the gain TC for a particular grade.

If an external reference is used (10.000 V, for example), additional trim range should be provided, since the internal reference has a tolerance of ±20 mV, and the AD669 gain and bipolar offset are both trimmed with the internal reference. The optional gain and offset trim resistors in Figures 5 and 6 provide enough adjustment range to null these errors.

It is also possible to use external references other than 10 volts with slightly degraded linearity specifications. The recommended range of reference voltages is +5 V to +10.24 V, which allows 5 V, 8.192 V and 10.24 V ranges to be used. For example, by using the AD586 5 V reference, outputs of 0 V to +5 V unipolar or ±5 V bipolar can be realized. Using the AD586 voltage reference makes it possible to operate the AD669 off of ±12 V supplies with 10% tolerances.

Figure 5 shows the AD669 using the AD586 5 V reference in the bipolar configuration. This circuit includes two optional potentiometers and one optional resistor that can be used to adjust the gain, offset and bipolar zero errors in a manner similar to that described in the BIPOLAR CONFIGURATION section. Use −5.000000 V and +4.999847 as the output values.

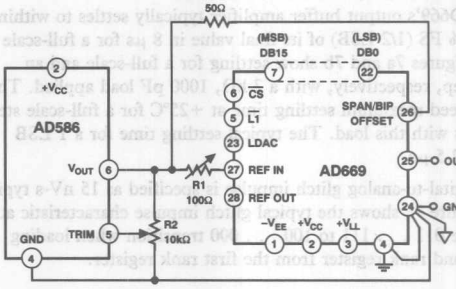


Figure 5. Using the AD669 with the AD586 5 V Reference

USING THE AD669 WITH THE AD688 HIGH PRECISION VOLTAGE REFERENCE

The AD669 is specified for gain drift from 15 ppm/°C to 25 ppm/°C (depending upon grade) using its internal 10 volt reference. Since the internal reference contributes the vast majority of this drift, an external high precision voltage reference will greatly improve performance over temperature. As shown in Figure 6, the +10 volt output from the AD688 is used as the AD669 reference. With a 3 ppm/°C drift over the industrial temperature range, the AD688 will improve the gain drift by a factor of 5 to a factor of 8 (depending upon the grade of the AD669 being used). Using this combination may result in apparent increases in initial gain error due to the differences between the internal reference by which the device is laser trimmed and the external reference with which the device is actually applied. The AD669 internal reference is specified to be 10 volts ±20 mV whereas the AD688 is specified as 10 volts ±5 mV. This may result in an additional 5 mV (33 LSBs) of apparent initial gain error beyond the specified AD669 gain error. The circuit shown in Figure 6 also makes use of the −10 V AD688 output to allow the unipolar offset and gain to be adjusted to zero in the manner described in the UNIPOLAR CONFIGURATION section.

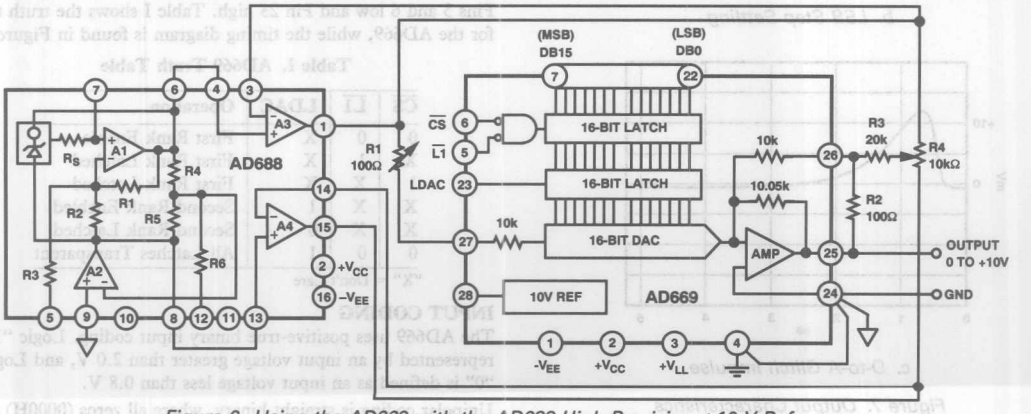
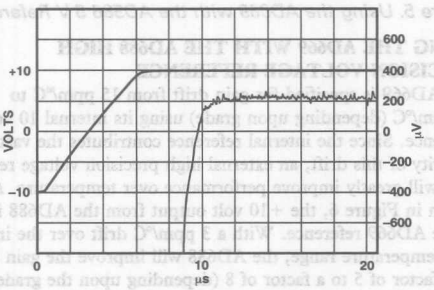


Figure 6. Using the AD669 with the AD688 High Precision ±10 V Reference

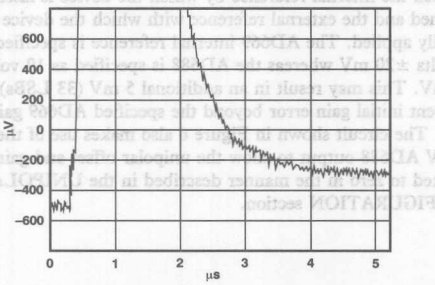
OUTPUT SETTLING AND GLITCH

The AD669's output buffer amplifier typically settles to within 0.0008% FS (1/2 LSB) of its final value in 8 μs for a full-scale step. Figures 7a and 7b show settling for a full-scale and an LSB step, respectively, with a 2 kΩ, 1000 pF load applied. The guaranteed maximum settling time at +25°C for a full-scale step is 13 μs with this load. The typical settling time for a 1 LSB step is 2.5 μs.

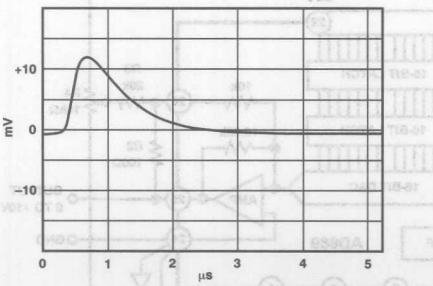
The digital-to-analog glitch impulse is specified as 15 nV-s typical. Figure 7c shows the typical glitch impulse characteristic at the code 011 . . . 111 to 100 . . . 000 transition when loading the second rank register from the first rank register.



a. –10 V to +10 V Full-Scale Step Settling



b. LSB Step Settling



c. D-to-A Glitch Impulse

Figure 7. Output Characteristics

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD669 consists of two independently addressable registers in two ranks. The first rank consists of a 16-bit register which is loaded directly from a 16-bit microprocessor bus. Once the 16-bit data word has been loaded in the first rank, it can be loaded into the 16-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values.

The first rank latch is controlled by $\overline{CS}$ and $\overline{LI}$. Both of these inputs are active low and are level-triggered. This means that data present during the time when both $\overline{CS}$ and $\overline{LI}$ are low will enter the latch. When either one of these signals returns high, the data is latched.

The second rank latch is controlled by LDAC. This input is active high and is also level-triggered. Data that is present when LDAC is high will enter the latch, and hence the DAC will change state. When this pin returns low, the data is latched in the DAC.

Note that LDAC is not gated with $\overline{CS}$ or any other control signal. This makes it possible to simultaneously update all of the AD669's present in a multi-DAC system by tying the LDAC pins together. After the first rank register of each DAC has been individually loaded and latched, the second rank registers are then brought high together, updating all of the DACs at the same time. To reduce bit skew, it is suggested to leave 100 ns between the first rank load and the second rank load.

The first rank latch and second rank latch can be used together in a master-slave or edge-triggered configuration. This mode of operation occurs when LDAC and $\overline{CS}$ are tied together with $\overline{LI}$ tied to ground. Rising edges on the LDAC-$\overline{CS}$ pair will update the DAC with the data presented preceding the edge. The timing diagram for operation in this mode can be seen in Figure 1b. Note, however, that the sum of t_{LOW} and t_{HIGH} must be long enough to allow the DAC output to settle to its new value.

It is possible to make the second rank register transparent by tying Pin 23 high. Any data appearing in the first rank register will then appear at the output of the DAC. It should be noted, however, that the deskewing provided by the second rank latch is then defeated, and glitch impulse may increase. If it is desired to make both registers transparent, this can be done by tying Pins 5 and 6 low and Pin 23 high. Table I shows the truth table for the AD669, while the timing diagram is found in Figure 1.

Table I. AD669 Truth Table

$\overline{CS}$	$\overline{LI}$	LDAC	Operation
0	0	X	First Rank Enable
X	1	X	First Rank Latched
1	X	X	First Rank Latched
X	X	1	Second Rank Enabled
X	X	0	Second Rank Latched
0	0	1	All Latches Transparent

"X" = Don't Care

INPUT CODING

The AD669 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0 V, and Logic "0" is defined as an input voltage less than 0.8 V.

Unipolar coding is straight binary, where all zeros (0000H) on the data inputs yields a zero analog output and all ones (FFFFH) yields an analog output 1 LSB below full scale.

Bipolar coding is offset binary, where an input code of 0000H yields a minus full-scale output, an input of FFFFH yields an output 1 LSB below positive full scale, and zero occurs for an input code with only the MSB on (8000H).

The AD669 can be used with twos complement input coding if an inverter is used on the MSB (DB15).

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts. The input lines can thus interface with any type of 5 volt logic.

The AD669 data and control inputs will float to indeterminate logic states if left open. It is important that $\overline{CS}$ and $\overline{L1}$ be connected to DGND and that LDAC be tied to V_{LL} if these pins are not used.

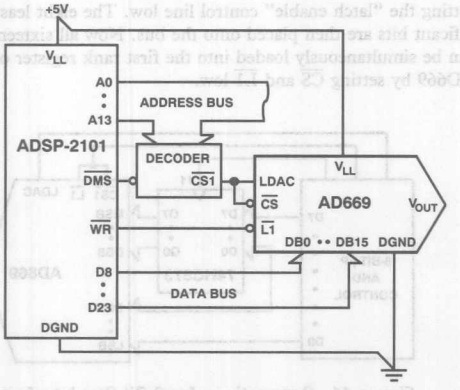
Fanout for the AD669 is 40 when used with a standard low power Schottky gate output device.

16-BIT MICROPROCESSOR INTERFACE

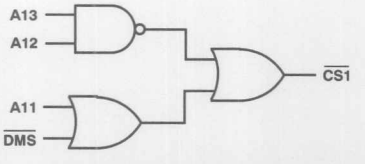
The 16-bit parallel registers of the AD669 allow direct interfacing to 16-bit general purpose and DSP microprocessor buses. The following examples illustrate typical AD669 interface configurations.

AD669 TO ADSP-2101 INTERFACE

The flexible interface of the AD669 minimizes the required "glue" logic when it is connected in configurations such as the one shown in Figure 8. The AD669 is mapped into the ADSP-2101's memory space and requires two wait states using a 12.5 MHz processor clock.



8a. ADSP-2101 to AD669 Interface



8b. Typical Address Decoder

Figure 8. ADSP-2101 to AD669 Interface

In this configuration, the ADSP-2101 is set up to use the internal timer to interrupt the processor at the desired sample rate. The $\overline{WR}$ pin and data lines D8–D23 from the ADSP-2101 are tied directly to the $\overline{L1}$ and DB0 through DB15 pins of the AD669, respectively. The decoded signal $\overline{CS1}$ is connected to both $\overline{CS}$ and LDAC. When a timer interrupt is detected, the ADSP-2101 automatically vectors to the appropriate service routine with minimal overhead. The interrupt routine then instructs the processor to execute a data memory write to the address of the AD669.

The $\overline{WR}$ pin and $\overline{CS1}$ both go low causing the first 16-bit latch inside the AD669 to be transparent. The data present in the first rank is then latched by the rising edge of $\overline{WR}$. The rising edge of $\overline{CS1}$ will cause the second rank 16-bit latch to become transparent updating the output of the DAC. The length of $\overline{WR}$ is extended by two wait states to comply with the timing requirements of t_{LOW} shown in Figure 1b. It is important to latch the data with the rising edge of $\overline{WR}$ rather than the decoded $\overline{CS1}$. This is necessary to comply with the t_{DH} specification of the AD669.

Figure 8b shows the circuitry a typical decoder might include. In this case, a data memory write to any address in the range 3000H to 3400H will result in the AD669 being updated. These decoders will vary greatly depending on the number of devices memory-mapped by the processor.

AD669 TO DSP56001 INTERFACE

Figure 9 shows the interface between the AD669 and the DSP56001. Like the ADSP-2101, the AD669 is mapped into the DSP56001's memory space. This application was tested with a processor clock of 20.48 MHz (t_{CYC} = 97.66 ns) although faster rates are possible.

An external clock connected to the $\overline{IRQA}$ pin of the DSP56001 interrupts the processor at the desired sample rate. If ac performance is important, this clock should be synchronous with the DSP56001 processor clock. Asynchronous clocks will cause jitter on the latch signal due to the uncertainty associated with the

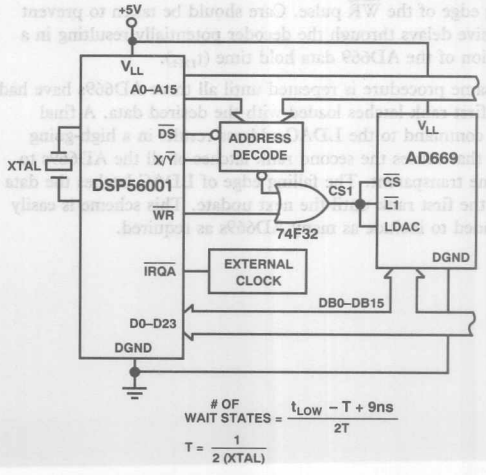


Figure 9. DSP560001 to AD669 Interface

acknowledgment of the interrupt. A synchronous clock is easily generated by dividing down the clock from the DSP crystal. If ac performance is not important, it is not necessary for $\overline{IRQA}$ to be synchronous.

After the interrupt is acknowledged, the interrupt routine initiates a memory write cycle. All of the AD669 control inputs are tied together which configures the input stage as an edge triggered 16-bit register. The rising edge of the decoded signal latches the data and updates the output of the DAC. It is necessary to insert wait states after the processor initiates the write cycle to comply with the timing requirements t_{LOW} shown in Figure 1b. The number of wait states that are required will vary depending on the processor cycle time. The equation given in Figure 9 can be used to determine the number of wait states given the frequency of the processor crystal.

As an example, the 20.48 MHz crystal used in this application results in T = 24.4 ns which means that the required number of wait states is about 2.76. This must be rounded to the next highest integer to assure that the minimum pulse widths comply with those required by the AD669. As the speed of the processor is increased, the data hold time relative to $\overline{CS1}$ decreases. As processor clocks increase beyond 20.48 MHz, a configuration such as the one shown for the ADSP-2101 is the better choice.

AD669 TO 8086 INTERFACE

Figure 10 shows the 8086 16-bit microprocessor connected to multiple AD669s. The double-buffered capability of the AD669 allows the microprocessor to write to each AD669 individually and then update all the outputs simultaneously. Processor speeds of 6, 8, and 10 MHz require no wait states to interface with the AD669.

The 8086 software routine begins by writing a data word to the $\overline{CS1}$ address. The decoder must latch the address using the ALE signal. The decoded $\overline{CS1}$ pulse goes low causing the first rank latch of the associated AD669 to become transparent.

Simultaneously, the 8086 places data on the multiplexed bus which is then latched into the first rank of the AD669 with the rising edge of the $\overline{WR}$ pulse. Care should be taken to prevent excessive delays through the decoder potentially resulting in a violation of the AD669 data hold time (t_{DH}).

The same procedure is repeated until all three AD669s have had their first rank latches loaded with the desired data. A final write command to the LDAC address results in a high-going pulse that causes the second rank latches of all the AD669s to become transparent. The falling edge of LDAC latches the data from the first rank until the next update. This scheme is easily expanded to include as many AD669s as required.

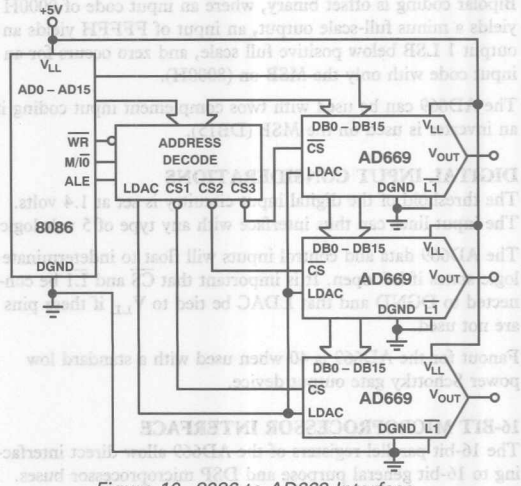


Figure 10. 8086-to-AD669 Interface

8-BIT MICROPROCESSOR INTERFACE

The AD669 can easily be operated with an 8-bit bus by the addition of an octal latch. The 16-bit first rank register is loaded from the 8-bit bus as two bytes. Figure 11 shows the configuration when using a 74HC573 octal latch.

The eight most significant bits are latched into the 74HC573 by setting the "latch enable" control line low. The eight least significant bits are then placed onto the bus. Now all sixteen bits can be simultaneously loaded into the first rank register of the AD669 by setting $\overline{CS}$ and $\overline{L1}$ low.

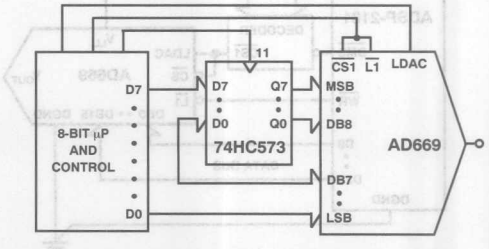


Figure 11. Connections for 8-Bit Bus Interface

NOISE

In high resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 153 μV (−96 dB). Therefore, the noise floor must remain below this level in the frequency range of interest. The AD669's noise spectral density is shown in Figures 12 and 13. Figure 12 shows the DAC output noise voltage spectral density for a 20 V span excluding the reference. This figure shows the 1/f corner frequency at 100 Hz and the wideband noise to be below 120 nV/$\sqrt{\text{Hz}}$. Figure 13 shows the reference noise voltage spectral density. This figure shows the reference wideband noise to be below 125 nV/$\sqrt{\text{Hz}}$.

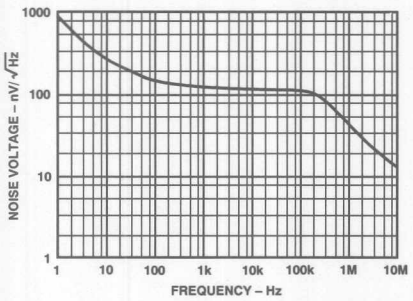


Figure 12. DAC Output Noise Voltage Spectral Density

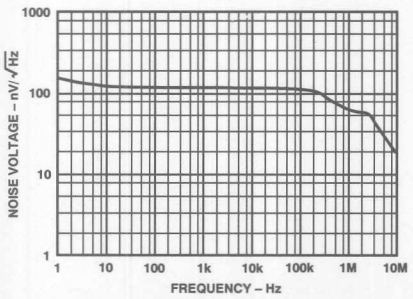


Figure 13. Reference Noise Voltage Spectral Density

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 306 μA current through a 0.5 Ω trace will develop a voltage drop of 153 μV, which is 1 LSB at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes should also be utilized, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

One feature that the AD669 incorporates to help the user layout is the analog pins (V_{CC}, V_{EE}, REF OUT, REF IN, SPAN/BIP OFFSET, V_{OUT} and AGND) are adjacent to help isolate analog signals from digital signals.

2

SUPPLY DECOUPLING

The AD669 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling. V_{CC} and V_{EE} should be bypassed to analog ground, while V_{LL} should be decoupled to digital ground.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD669, associated analog circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD669 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

The AD669 has two pins, designated analog ground (AGND) and digital ground (DGND.) The analog ground pin is the "high quality" ground reference point for the device. Any external loads on the output of the AD669 should be returned to analog ground. If an external reference is used, this should also be returned to the analog ground.

If a single AD669 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD669. If multiple AD669s are used or the AD669 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

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ANALOG DEVICES

16-Bit DSP DACPORT

AD766

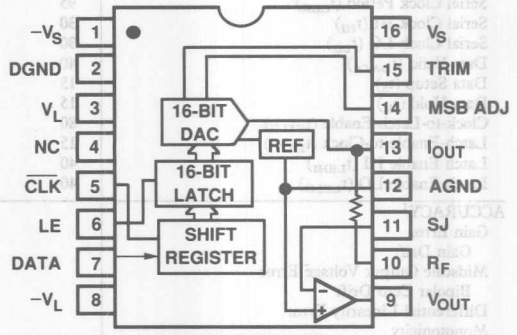
FEATURES

- Zero-Chip Interface to Digital Signal Processors
- Complete DACPORT™
  - On-Chip Voltage Reference
  - Voltage and Current Outputs
- Serial, Twos-Complement Input
- ±3 V Output
- Sample Rates to 390 kSPS
- 94 dB Minimum Signal-to-Noise Ratio
- –81 dB Maximum Total Harmonic Distortion
- 15-Bit Monotonicity
- ±5 V to ±12 V Operation
- 16-Pin Plastic and Ceramic Packages
- Available in Commercial, Industrial, and Military Temperature Ranges

APPLICATIONS

- Digital Signal Processing
- Noise Cancellation
- Radar Jamming
- Automatic Test Equipment
- Precision Industrial Equipment
- Waveform Generation

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD766 16-bit DSP DACPORT provides a direct, three-wire interface to the serial ports of popular DSP processors, including the ADSP-2101, TMS320CXX, and DSP56001. No additional "glue logic" is required. The AD766 is also complete, offering on-chip serial-to-parallel input format conversion, a 16-bit current-steering DAC, voltage reference, and a voltage output op amp. The AD766 is fabricated in Analog Devices' BiMOS II mixed-signal process which provides bipolar transistors, MOS transistors, and thin-film resistors for precision analog circuits in addition to CMOS devices for logic.

The design and layout of the AD766 have been optimized for ac performance and are responsible for its guaranteed and tested 94 dB signal-to-noise ratio to 20 kHz and 79 dB SNR to 250 kHz. Laser-trimming the AD766's silicon chromium thin-film resistors reduces total harmonic distortion below −81 dB (at 1 kHz), a specification also production tested. An optional linearity trim pin allows elimination of midscale differential linearity error for even lower THD with small signals.

The AD766's output amplifier provides a ±3 V signal with a high slew rate, small glitch, and fast settling. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

DACPORT is a trademark of Analog Devices, Inc.

The serial interface consists of bit clock, data, and latch enable inputs. The twos-complement data word is clocked MSB first on falling clock edges into the serial-to-parallel converter, consistent with the serial protocols of popular DSP processors. The input clock can support data transfers up to 12.5 MHz. The falling edge of latch enable updates the internal DAC input register at the sample rate with the sixteen bits most recently clocked into the serial input register.

The AD766 operates over a ±5 V to ±12 V power supply range. The digital supplies, $+V_L$ and $-V_L$, can be separated from the analog signal supplies, $+V_S$ and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. An internal bandgap reference provides a precision voltage source to the output amp that is stable over temperature and time.

Power dissipation is typically 120 mW with ±5 V supplies and 300 mW with ±12 V. The AD766 is available in commercial (0°C to 70°C), industrial (−40°C to 85°C), and military (−55°C to 125°C) grades. Commercial and industrial grade parts are available in a 16-pin plastic DIP; military parts processed to MIL-STD-883B are packaged in a 16-pin ceramic DIP. See Analog Devices' *Military Products Databook* or current military data sheet for specifications for the military version.

RESOLUTION						Bits
DIGITAL INPUTS						
V_{IH}	2.0		$+V_L$	2.0	$+V_L$	V
V_{IL}			0.8		0.8	V
I_{IH}, $V_{IH} = V_L$			**1.0**		**1.0**	μA
I_{IL}, $V_{IL} = 0.4$			**−10**		**−10**	μA
SERIAL PORT TIMING						
Serial Clock Period (t_{CLK})	95			115		ns
Serial Clock HI (t_{HI})	30			30		ns
Serial Clock LO (t_{LO})	30			70		ns
Data Valid (t_{DATA})	40			40		ns
Data Setup (t_S)	15			20		ns
Data Hold (t_H)	15			20		ns
Clock-to-Latch-Enable (t_{CTLE})	80			100		ns
Latch-Enable-to-Clock (t_{LETC})	15			15		ns
Latch Enable HI (t_{LEHI})	40			40		ns
Latch Enable LO (t_{LELO})	40			80		ns
ACCURACY[1]						
Gain Error		±2.0			±2.0	% of FSR
Gain Drift		±25			±25	ppm of FSR/°C
Midscale Output Voltage Error		±30			±30	mV
Bipolar Zero Drift		±4			±4	ppm of FSR/°C
Differential Linearity Error		±0.001			±0.001	% of FSR
Monotonicity		15			15	Bits
TOTAL HARMONIC DISTORTION						
F_{OUT} = 1037 Hz[1]						
0 dB		−88	**−81**		−88	**−81** dB
−20 dB		−75	**−65**		−75	**−65** dB
−60 dB		−37	**−27**		−37	**−27** dB
F_{OUT} = 49.07 kHz[2]						
0 dB		−77	**−72**		−77	**−72** dB
−20 dB		−69	**−66**		−69	**−66** dB
−60 dB		−25	**−21**		−25	**−21** dB
SIGNAL-TO-NOISE RATIO[3]						
20 Hz to 20 kHz (F_{OUT} = 1037 Hz)[1]	**94**	102		**94**	102	dB
20 kHz to 250 kHz (F_{OUT} = 49.07 kHz)[2]	**79**	83		**79**	83	dB
SETTLING TIME (to ±0.0015% of FSR)						
Voltage Output[1]						
6 V Step		1.5			1.5	μs
1 LSB Step		1.0			1.0	μs
Slew Rate		9			9	V/μs
Current Output						
1 mA Step 10 Ω to 100 Ω Load		350			350	ns
1 kΩ Load		350			350	ns
OUTPUT						
Voltage Output Configuration[1]						
Bipolar Range	±2.88	±3.0	±3.12	±2.88	±3.0	±3.12 V
Output Current		±8.0			±8.0	mA
Output Impedance		0.1			0.1	Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common	
Current Output Configuration						
Bipolar Range	±0.7	±1.0	±1.3	±0.7	±1.0	±1.3 mA
Output Impedance (±30%)		1.7			1.7	kΩ
POWER SUPPLY						
Voltage: $+V_L$ and $+V_S$	**4.75**		**13.2**	**4.75**		**13.2** V
$-V_L$ and $-V_S$	**−13.2**		**−4.75**	**−13.2**		**−4.75** V
Current Case 1[1]: V_S and V_L = +5 V +I		12.0	**15.0**		12.0	**15.0** mA
$-V_S$ and $-V_L$ = −5 V −I		−12.0	**−15.0**		−12.0	**−15.0** mA
Case 2: V_S and V_L = +12 V +I		10.5			10.5	mA
$-V_S$ and $-V_L$ = −12 V −I		−14			−14	mA
Case 3[4]: V_S and V_L = +5 V +I		12			12	mA
$-V_S$ and $-V_L$ = −12 V −I		−14			−14	mA
Power Dissipation: V_S and V_L = ±5 V[1]		120	**150**		120	**150** mW
V_S and V_L = ±12 V		300			300	mW
V_S and V_L = +5 V, $-V_S$ and $-V_L$ = −12 V[4]		225			225	mW

Parameter	AD766J Min	AD766J Typ	AD766J Max	AD766A Min	AD766A Typ	AD766A Max	Units
TEMPERATURE RANGE							
Specified	0		+70	−40		+85	°C
Storage	−60		+100	−60		+100	°C

NOTES

[1]For A grade only, voltage outputs are guaranteed only if $+V_S \geq 7$ V and $-V_S \leq -7$ V.

[2]Specified using external op amp, see Figure 3 for more details.

[3]Tested at full-scale input.

[4]For A grade only, power supplies must be symmetric, i.e., $V_S = |-V_S|$ and $+V_L = |-V_L|$. Each supply must independently meet this equality within ±5%.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2 V
V_S to AGND . . . . . 0 to 13.2 V
$-V_L$ to DGND . . . . . −13.2 V to 0 V
$-V_S$ to AGND . . . . . −13.2 V to 0 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
AGND to DGND . . . . . ±0.3 V
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

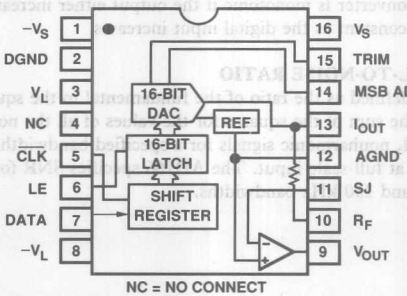
Model	Temperature Range	Package Option*
AD766JN	0°C to +70°C	N-16
AD766AN	−40°C to +85°C	N-16
AD766SD/883B	−55°C to +125°C	D-16

*N = Plastic DIP; D = Ceramic DIP. For outline information see Package Information section.

PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	$\overline{CLK}$	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

CONNECTION DIAGRAM



NC = NO CONNECT

ESD SENSITIVITY

The AD766 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD766 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.



AD766—Definition of Specifications

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of integral linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is the primary measure of dynamic performance.

BIPOLAR ZERO ERROR

Bipolar Zero Error or midscale error is the deviation of the actual analog output from the ideal output (0 V) when the 2s complement input code representing half scale (all 0s) is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1 LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

SIGNAL-TO-NOISE RATIO

SNR is defined as the ratio of the fundamental to the square root of the sum of the squares for the values of all the nonfundamental, nonharmonic signals for a specified bandwidth. SNR is tested at full-scale input. The AD766 specifies SNR for 20 kHz and 250 kHz bandwidths.

FUNCTIONAL DESCRIPTION

Serial input data is clocked into the AD766's shift register by the falling edge of $\overline{CLK}$. Data is presumed to be in twos-complement format with MSB (i.e., the sign bit) clocked in first. The shift register converts the most recently clocked-in 16 bits to a parallel word. The falling edge of the latch enable (LE) signal causes the most recent parallel word to be transferred to the internal DAC input latch. See Figure 2 for detailed serial port timing requirements.

The contents of the DAC input latch cause the 16-bit DAC to generate a corresponding current. This ±1 mA current is available directly on the I_{OUT} pin.

To use the internal op amp, connect I_{OUT} (Pin 13) directly to the summing junction pin, SJ (Pin 11) and connect the feedback resistor pin, R_F (Pin 10) to V_{OUT} (Pin 9). Note that the internal op amp is in the inverting configuration. Using the internal 3 kΩ feedback resistor, this op amp will produce ±3 V outputs.

One advantage of external pins at each end of the feedback resistor is that it allows the user to implement a single pole active low-pass filter simply by adding a capacitor across these pins (Pins 10 and 13). The circuit can best be understood redrawn as shown in Figure 1.

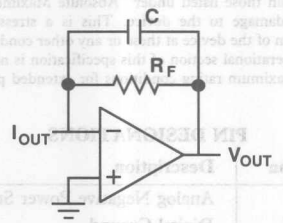


Figure 1. Low-Pass Filter Using External Capacitor

The frequency response from this filter will be

$$\frac{V_{OUT(s)}}{I_{OUT}} = \frac{-R_F}{R_F \cdot C \cdot s + 1}$$

where R_F is 3 kΩ (±20%).

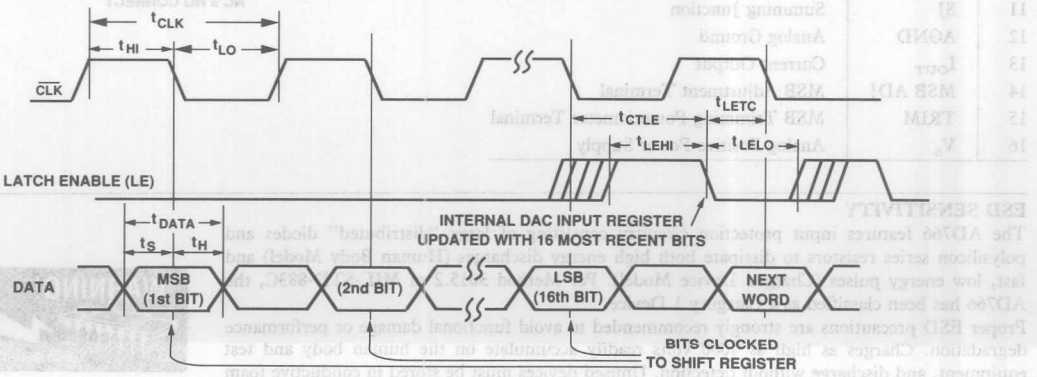


Figure 2. AD766 Serial Input Timing

For applications requiring broader bandwidths and/or even lower noise than that afforded by the AD766's internal op amp, an external op amp can easily by used in its place. I_{OUT} (Pin 13) drives the negative (inverting) input terminal of the external op amp, and its external voltage output is connected to the feedback resistor pin, R_F (Pin 10). To insure that the AD766's unused internal op amp remains in a closed-loop configuration, V_{OUT} (Pin 9) should be tied to the summing junction pin, SJ (Pin 11).

As an example, Figure 3 shows the AD766 using the AD744 op amp as an external current-to-voltage converter. In this inverting configuration, the AD744 will provide the same ±3 V output as the internal op amp would have. Other recommended amplifiers include the AD845 and AD846. Note that a single pole of low-pass filtering could also be attained with this circuit simply by adding a capacitor in parallel with the feedback resistor as just shown in Figure 1.

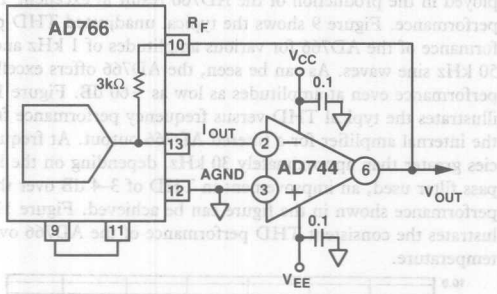


Figure 3. External Op Amp Connections

Residual DAC differential linearity error around midscale can be externally trimmed out, improving THD beyond the AD766's guaranteed tested specifications. This error is most significant with low-amplitude signals because the ratio of the midscale linearity error to the signal amplitude is greatest in this case, thereby increasing THD. The MSB adjust circuitry shown in Figure 4 can be used for improving THD with low-level signals. Otherwise, the AD766 will operate to its specifications with MSB ADJ (Pin 14) and TRIM (Pin 15) unconnected.

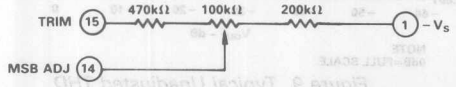


Figure 4. Optional MSB Adjustment Circuit

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD766 has two ground pins, designated AGND (analog ground) and DGND (digital ground). The analog ground pin is the "high-quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD766 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 5, the analog and digital grounds should be connected together at one point in the system.

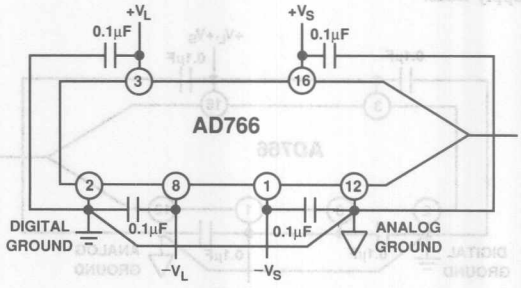


Figure 5. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD766 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5 V to ±12 V.

The $\pm V_L$ supplies operate the digital portions of the chip, including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to operate from ±5 V to ±12 V. To assure freedom from latch-up, $-V_L$ should never go more negative than $-V_S$.

Special restrictions on power supplies apply to extended-temperature range versions of the AD766 that do not apply to the commercial AD766J. First, supplies must be symmetric. That is, $+V_S = |-V_S|$ and $+V_L = |-V_L|$. Each supply must independently meet this equality within ±5%. Since we require that $-V_S \leq -V_L$ to guarantee latch-up immunity, this symmetry principle implies that the positive analog supply must be greater than or equal to the positive digital supply, i.e., $V_S \geq V_L$ for extended-temperature range parts. In other words, the digital supply range must be inside the analog supply range. Second, the internal op amp's performance in generating voltage outputs is only guaranteed if $+V_S \geq 7$ V (and $-V_S \leq -7$ V, by the symmetry principle). These constraints do not apply to the AD766J.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portions of the system, thus contributing to the performance as tested. However, four separate voltage supplies are not necessary for good circuit performance. For example, Figure 6 illustrates a

are available. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low-pass filters in the individual power supply leads.

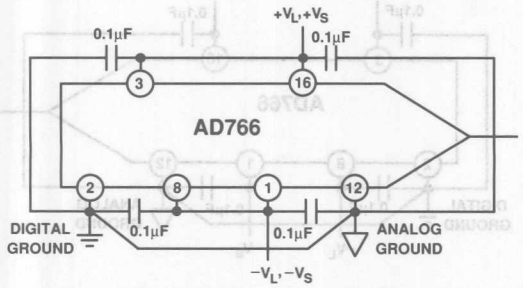


Figure 6. Alternate Recommended Schematic

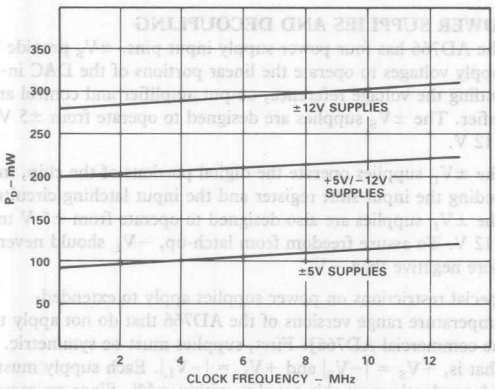


Figure 7. Power Dissipation vs. Clock Frequency

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

MEASUREMENT OF TOTAL HARMONIC DISTORTION

The THD specification of a DSP DAC represents the amount of undesirable signal produced during reconstruction of a digital signal processing applications, the DAC is tested at two output frequencies and at three signal levels over the full operating temperature ranges.

A block diagram of the test setup is shown in Figure 8. In this test setup, a digital data stream, representing a 0 dB, −20 dB or −60 dB sine wave is sent to the device under test. The frequencies used are 1037 Hz and 49.07 kHz. Input data is latched into the AD766 at 500 kSPS. The AD766 under test produces an analog output signal using the on-board op amp for 1 kHz and an external op amp for 50 kHz.

The automatic test equipment digitizes the output test waveform, and then an FFT to 250 kHz is performed on the results of the test. Based on the first 9 harmonics of the fundamental 1037 Hz and the first 3 harmonics of the 49.07 kHz output waves, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout and manufacturing techniques employed in the production of the AD766 result in excellent THD performance. Figure 9 shows the typical unadjusted THD performance of the AD766 for various amplitudes of 1 kHz and 50 kHz sine waves. As can be seen, the AD766 offers excellent performance even at amplitudes as low as −60 dB. Figure 10 illustrates the typical THD versus frequency performance from the internal amplifier for a filtered AD766 output. At frequencies greater than approximately 30 kHz, depending on the low-pass filter used, an improvement in THD of 3–4 dB over the performance shown in the figure can be achieved. Figure 11 illustrates the consistent THD performance of the AD766 over temperature.

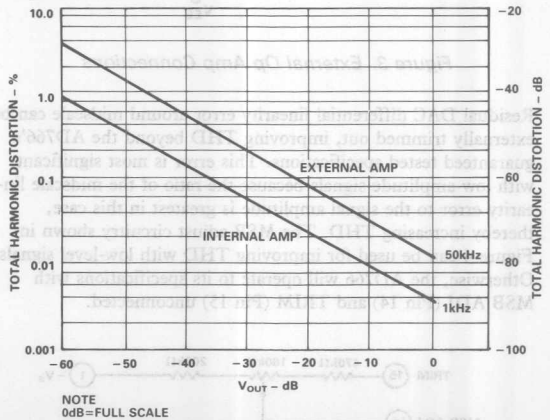


Figure 9. Typical Unadjusted THD

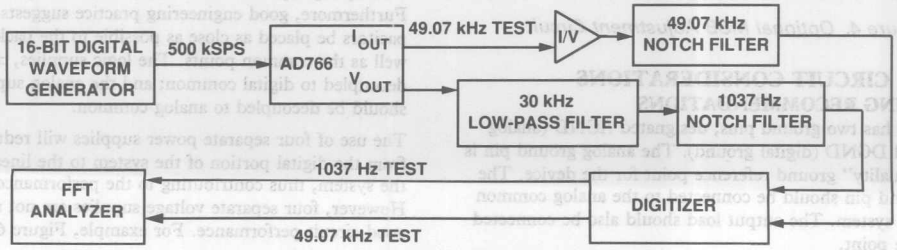


Figure 8. Distortion Test Circuit

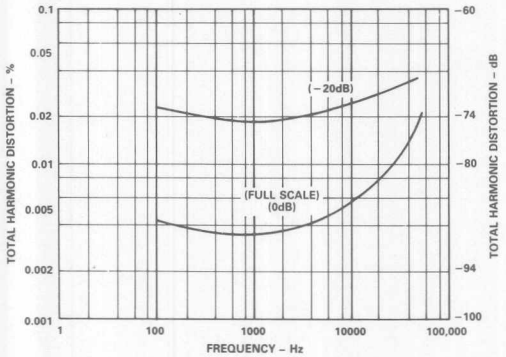


Figure 10. Typical THD vs. Frequency

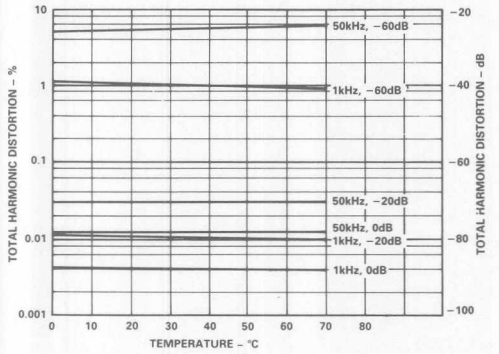


Figure 11. THD vs. Temperature

INTERFACING THE AD766 TO DIGITAL SIGNAL PROCESSORS

The AD766 is specifically designed to easily interface to several popular digital signal processors (DSP) without any additional logic. Such an interface reduces the possibility of interface problems and improves system reliability by minimizing component count.

AD766 TO ADSP-2101

The ADSP-2101 incorporates two complete serial ports which can be directly interfaced to the AD766 as shown in Figure 12. The SCLK, TFS and DT outputs of the ADSP-2101 are connected directly to the $\overline{CLK}$, LE and DATA inputs of the AD766, respectively. SCLK is internally generated and can be programmed to operate from 94 Hz to 6.25 MHz. Data (DT) is valid on the falling edge of SCLK. After 16 bits have been transmitted, the falling edge of TFS updates the AD766's data latch. Using both serial ports of the ADSP-2101, two AD766's can be directly interfaced with no additional hardware.

AD766 TO TMS320C25

Figure 13 shows the zero-chip interface to the TMS320C25. The *interface to other TMS320C2X processors is similar.* Note that the C25 should be run in continuous mode. The C25's frame synch signal (FSX) will be asserted at the beginning of each 16-bit word but will actually latch in the previous word.

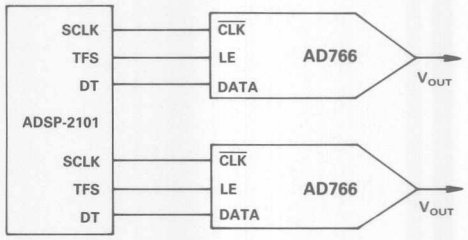


Figure 12. AD766 to ADSP-2101/ADSP-2102/ ADSP-2105/ADSP-2111

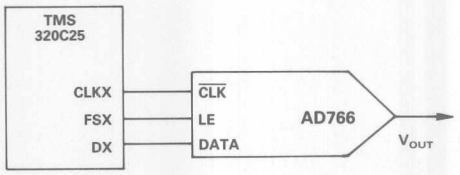


Figure 13. AD766 to TMS320C25

The CLKS, FSX and DX outputs of the TMS320C25 are connected to the $\overline{CLK}$, LE and DATA inputs of the AD766, respectively. Data (DX) is valid on the falling edge of CLKX. The maximum serial clock rate of the TMS320C25 is 5 MHz.

AD766 TO DSP56000/56001

Figure 14 shows the zero-chip interface to the DSP56000/56001. The SSI of the 56000/56001 allows serial clock rates up to fosc/4. SCK, SC2 and STD can be directly connected to the $\overline{CLK}$, LE and DATA inputs of the AD766. The CRA control register of the 56000 allows SCK to be internally generated and software configurable to various divisions of the master clock frequency. The data (STD) is valid on the falling edge of SCK.

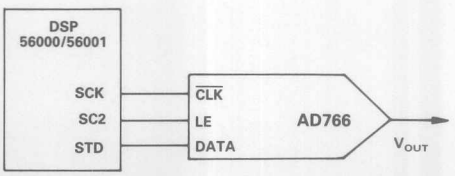


Figure 14. AD766 to DSP56000/DSP56001

Figure 12. AD766 to ADSP-2101/ADSP-2102/ ADSP-2105/ADSP-2111

Figure 13. AD766 to TMS32025

The CLKS, FSX and DX outputs of the TMS32025 are connected to the CLK, LE and DATA inputs of the AD766, respectively. Data (DX) is valid on the falling edge of CLKX. The maximum serial clock rate of the TMS32025 is 5 MHz.

AD766 TO DSP56000/56001

Figure 14 shows the zero-chip interface to the DSP56000/ 56001. The SSI of the 56000/56001 allows serial clock rates up to fosc/4. SCK, SC2 and STD can be directly connected to the CLK, LE and DATA inputs of the AD766. The CRA control register of the 56000 allows SCK to be internally generated and software configurable to various divisions of the master clock frequency. The data (STD) is valid on the falling edge of SCK.

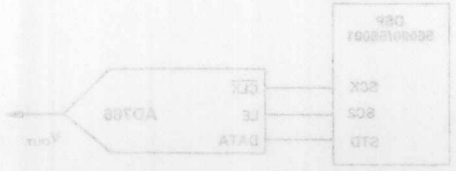


Figure 14. AD766 to DSP56000/DSP56001

Figure 10. Typical THD vs. Frequency

Figure 11. THD vs. Temperature

INTERFACING THE AD766 TO DIGITAL SIGNAL PROCESSORS

The AD766 is specifically designed to easily interface to several popular digital signal processors (DSP) without any additional logic. Such an interface reduces the possibility of interface problems and improves system reliability by minimizing component count.

AD766 TO ADSP-2101

The ADSP-2101 incorporates two complete serial ports which can be directly interfaced to the AD766 as shown in Figure 12. The SCLK, TFS and DT outputs of the ADSP-2101 are connected directly to the CLK, LE and DATA inputs of the AD766, respectively. SCLK is internally generated and can be programmed to operate from 94 Hz to 6.25 MHz. Data (DT) is valid on the falling edge of SCLK. After 16 bits have been transmitted, the falling edge of TFS updates the AD766's data latch. Using both serial ports of the ADSP-2101, two AD766's can be directly interfaced with no additional hardware.

AD766 TO TMS32025

Figure 13 shows the zero-chip interface to the TMS32025. The interface to other TMS32025 processors is similar. Note that the C25 should be run in continuous mode. The C25's frame synch signal (FSX) will be asserted at the beginning of each 16-bit word but will actually latch in the previous word.

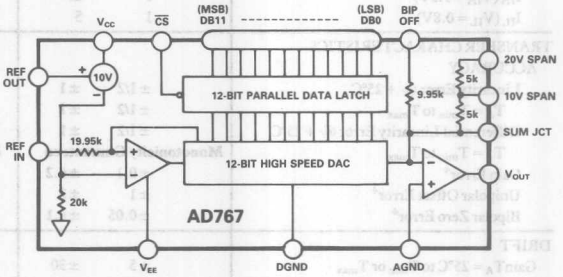
12-Bit D/A Converter

AD767*

FEATURES

- Complete 12-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Fast 40ns Write Pulse
- 0.3" Skinny DIP and PLCC Packages
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Settling Time: 3μs max to 1/2LSB
- Guaranteed for Operation with ±12V or ±15V Supplies
- TTL/5V CMOS Compatible Logic Inputs
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C.

PRODUCT HIGHLIGHTS

1. The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.
6. The AD767 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD767/883B data sheet for detailed specifications.

***Protected by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

DIGITAL INPUTS													
Resolution			12			12			12			Bits
Logic Levels (TTL Compatible, $T_{min}-T_{max}$)[3]													
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5			V
V_{IL} (Logic "0") J, K, A, B	0		+0.8	0		+0.8	0		+0.8			V
V_{IL} (Logic "0") S	0		+0.7									V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10			μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5			μA
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error @ +25°C		±1/2	±1		±1/8	±1/2		±1/2	±1			LSB
$T_A = T_{min}$ to T_{max}		±1/2	±1		±1/4	±1/2		±1/2	±1			LSB
Differential Linearity Error @ +25°C		±1/2	±1		±1/4	±1		±1/2	±1			LSB
$T_A = T_{min}$ to T_{max}	**Monotonicity Guaranteed**			**Monotonicity Guaranteed**			**Monotonicity Guaranteed**					LSB
Gain Error[4]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2			% of FSR[5]
Unipolar Offset Error[4]		±1	±2		±1	±2		±1	±2			LSB
Bipolar Zero Error[4]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1			% of FSR
DRIFT													
Gain T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±5	±30			ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3		±1	±3		±1	±3			ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10		±5	±10			ppm of FSR/°C
CONVERSION SPEED													
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)													
with 10kΩ Feedback		3	4		3	4		3	4			μs
with 5kΩ Feedback		2	3		2	3		2	3			μs
For LSB Change		1			1			1				μs
Slew Rate	10			10			10					V/μs
ANALOG OUTPUT													
Ranges[6]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10				V
Output Current	±5			±5			±5					mA
Output Impedance (dc)		0.05			0.05			0.05				Ω
Short-Circuit Current			40			40			40			mA
REFERENCE OUTPUT	**9.90**	10.00	**10.10**	**9.90**	10.00	**10.10**	**9.90**	10.00	**10.10**			V
External Current	0.1	1.0		0.1	1.0		0.1	1.0				mA
POWER SUPPLY SENSITIVITY													
V_{CC} = +11.4 to +16.5V dc		5	10		5	10		5	10			ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10		5	10			ppm of FS/%
POWER SUPPLY REQUIREMENTS													
Rated Voltages		±12, ±15			±12, ±15			±12, ±15				V
Range[6]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5			V
Supply Current													
+11.4 to +16.5V dc		9	13		9	13		9	13			mA
−11.4 to −16.5V dc		18	23		18	23		18	23			mA
Total Power Consumption		400	600		400	600		400	600			mW
TEMPERATURE RANGE													
J/K	0		+70	0		+70						°C
A/B	−25		+85	−25		+85	−25		+85			°C
S	−55		+125	−55		+125						°C
Operating	−55		+125	−55		+125						°C
Storage (All Grades)	−65		+125	−65		+125	−65		+125			°C

NOTES

[1]AD767 "S" specifications shown for information only. Consult Analog Devices Military Databook or contact factory for a controlled specification sheet.

[2]AD767A Chips specifications are tested at +25°C and, when in boldface, at +85°C. They are typical at −25°C.

[3]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[4]Adjustable to zero.

[5]FSR means "Full-Scale Range" and is 20V for ±10V range and 10V for the ±5V range.

[6]A minimum power supply of ±12.5V is required for a ±10V full-scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test (except per Notes 1 and 2). Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

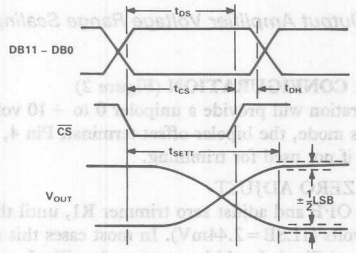
ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11, 13–24)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING SPECIFICATIONS

(All Models, $T_A = 25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$)

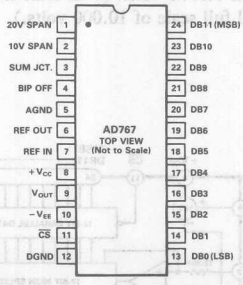


Symbol	Parameter	Min	Typ	Max	
t_{DS}	Data Valid to End of $\overline{CS}$	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{DH}	Data Hold Time	10	–	–	ns
	(−25°C to +85°C)	10	–	–	ns
	(−55°C to +125°C)	20	–	–	ns
t_{CS}	$\overline{CS}$ Pulse Width	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{SETT}	Output Voltage Settling Time*	–	2	4	μs

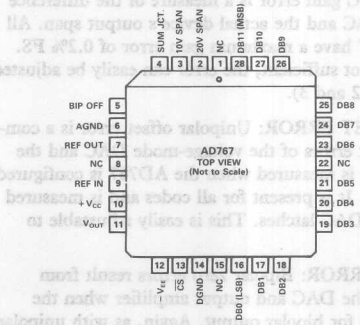
*t_{SETT} is measured referenced to the leading edge of t_{CS}. If $t_{CS} > t_{DS}$, then t_{SETT} is measured referenced to the beginning of Data Valid.

PIN CONFIGURATION

DIP



PLCC



ORDERING GUIDE

Model[1]	Package Option[2]	Temperature Range °C	Linearity Error Max $T_{min}-T_{max}$	Gain T.C. Max ppm/°C
AD767JN	Plastic DIP (N-24)	0 to +70	±1LSB	30
AD767JP	PLCC (P-28A)	0 to +70	±1LSB	30
AD767KN	Plastic DIP (N-24)	0 to +70	±1/2LSB	15
AD767KP	PLCC (P-28A)	0 to +70	±1/2LSB	15
AD767AD	Ceramic DIP (D-24A)	−25 to +85	±1LSB	30
AD767BD	Ceramic DIP (D-24A)	−25 to +85	±1/2LSB	15
AD767SD/883B	Ceramic DIP (D-24A)	−55 to +125	Note 2	Note 2
AD767A Chips	N/A	−25 to +85	±1LSB	30

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD767/883B data sheet.

AD767 — Analog Circuit Details

THE AD767 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. This is also referred to as relative accuracy. The AD767 is laser trimmed to typically maintain linearity errors at less than ±1/8LSB for the K and B versions and ±1/2LSB for the J, A and S versions. Linearity over temperature is also held to ±1/2LSB (K/B) or ±1LSB (J/A/S).

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD767 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full-scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be −1.83mV, or −3/4LSB.

GAIN ERROR: DAC gain error is a measure of the difference between an ideal DAC and the actual device's output span. All grades of the AD767 have a maximum gain error of 0.2% FS. However, if this is not sufficient, the error can easily be adjusted to zero (see Figures 2 and 3).

UNIPOLAR OFFSET ERROR: Unipolar offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured when the AD767 is configured for unipolar outputs. It is present for all codes and is measured with all "0s" in the DAC latches. This is easily adjustable to zero when required.

BIPOLAR ZERO ERROR: Bipolar zero errors result from errors produced by the DAC and output amplifier when the AD767 is configured for bipolar output. Again, as with unipolar offset and gain errors, this is easily adjusted to zero when required.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD767 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD767 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

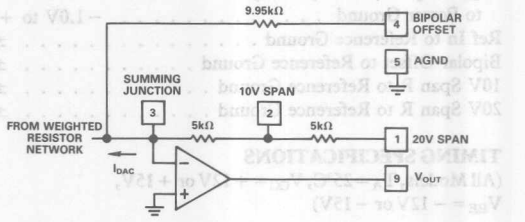


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, Pin 4, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and Pin 4 should be connected to Pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2 until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

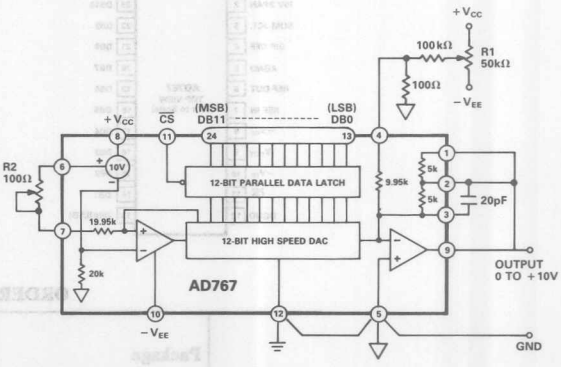


Figure 2. 0 to +10V Unipolar Voltage Output

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ωtrim resistor)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ωtrim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ωtrim resistor)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1s).

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST
Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

STEP III . . . BIPOLAR ZERO ADJUST (Optional)
In applications where an accurate zero output is required, set the MSB ON, all other bits OFF, and readjust R1 for zero volts output.

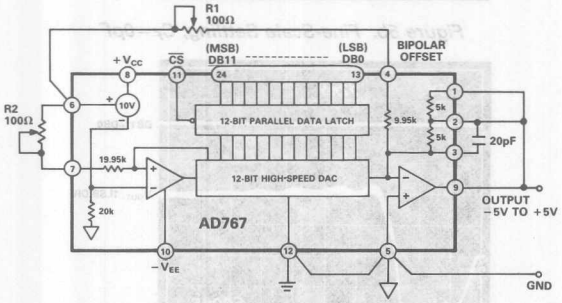


Figure 3. ±5V Bipolar Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD767 has an internal low-noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high-speed DAC and will give long-term stability equal or superior to the best discrete Zener reference diodes. The performance of the AD767 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads.

op amp if it is required to supply more than 0.1mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD767 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD767 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +10.5 volts, which allows both 8.192V and 10.24V ranges to be used. The AD767 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ±5% power supply requirement to be relaxed to ±12 volts ±10%.

It is not recommended that the AD767 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately −50ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24V full scale is desired, a 140Ω 1% low-TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between Pins 6 and 7) should be increased to 200Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200Ω.

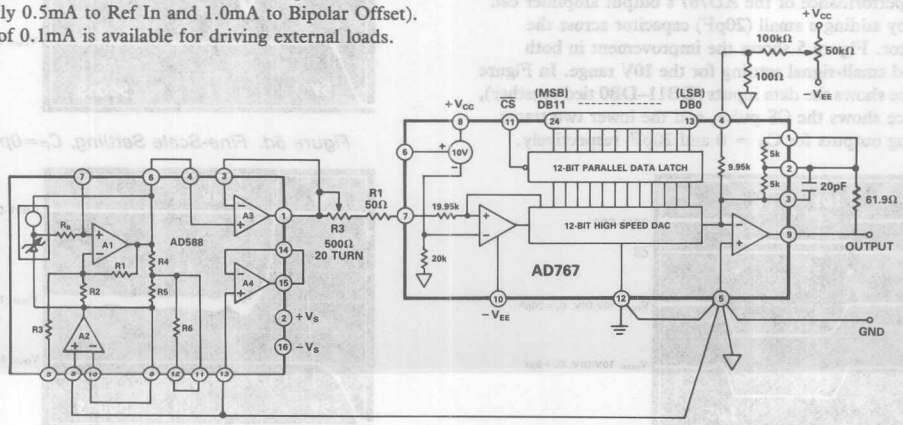


Figure 4. Using the AD767 with the AD588 High Precision Reference

VOLTAGE REFERENCE

The AD767 is specified for gain drift from 15ppm/°C to 30ppm/°C (depending on grade) using its internal 10 volt reference. Since the internal reference contributes the majority of this drift, an external high-precision voltage reference will greatly improve performance over temperature. As shown in Figure 4, the 10 volt output from the AD588 is used as the reference. With a 1.5ppm/°C output voltage drift the AD588 contributes less than 1/2LSB gain drift when used with the AD767 over the industrial temperature range. Using this combination may result in apparent increases in full-scale error due to the differences between the internal reference by which the device is laser trimmed and the external reference with which the device is actually applied. The AD767 internal reference is specified to be 10 volts ±100mV whereas the AD588 is specified as 10 volts ±1mV. This may result in up to 101mV of apparent full-scale error beyond the ±25mV specified AD767 gain error. The 500Ω potentiometer in series with the reference input allows adequate trim range to null this error.

GROUNDING RULES

The AD767 brings out separate analog and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths.

The analog ground at Pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD767; it should be connected directly to the analog reference point of the system. The power ground at Pin 12 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

It is also important to apply decoupling capacitors properly on the power supplies for the AD767. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD767 to the analog ground pin of the AD767. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

The dynamic performance of the AD767's output amplifier can be optimized by adding a small (20pF) capacitor across the feedback resistor. Figure 5 shows the improvement in both large-signal and small-signal settling for the 10V range. In Figure 5a, the top trace shows the data inputs (DB11–DB0 tied together), the second trace shows the CS pulse, and the lower two traces show the analog outputs for C_F = 0 and 20pF respectively.

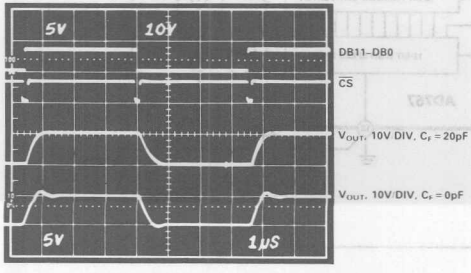


Figure 5a. Large Scale Settling

all bits on to all bits off. Note that the settling time to ±1/2LSB for the 10V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20pF capacitor.

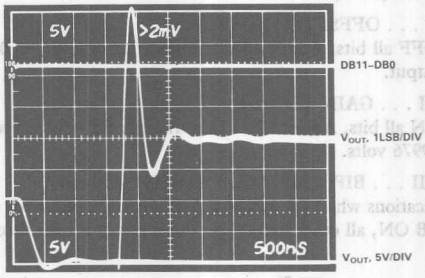


Figure 5b. Fine-Scale Settling, C_F = 0pF

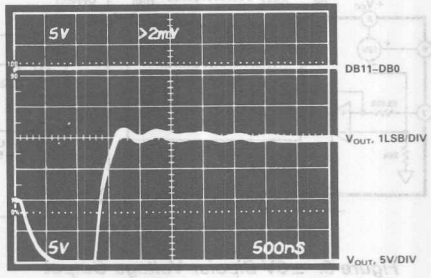


Figure 5c. Fine-Scale Settling, C_F = 20pF

Figures 5d and 5e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding C_C = 20pF is similar.

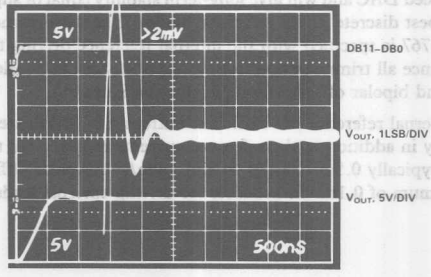


Figure 5d. Fine-Scale Settling, C_F = 0pF

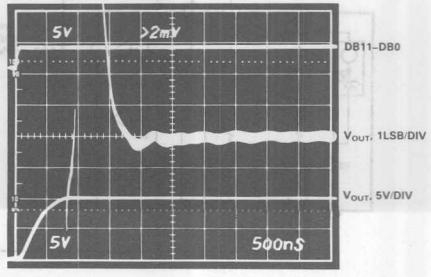


Figure 5e. Fine-Scale Settling, C_F = 20pF

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not change with supply voltage. Thus the AD767 digital interface may be driven with any of the popular types of 5 volt logic.

A good engineering practice is to connect unused inputs to power ground to improve noise immunity. Unconnected data and control inputs will float to logic 0 if left open.

The low digital input current of the AD767 eliminates the need for buffer/drivers required by many monolithic converters using bipolar technology. A single low-power Schottky gate, for example, will drive several AD767s when connected to a common bus.

INPUT CODING

The AD767 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0V, and logic "0" is defined as an input voltage less than 0.8V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD767 can be used with twos complement input coding if an inverter is used on the MSB (DB11).

MICROPROCESSOR INTERFACE

The AD767, with its 40ns minimum $\overline{CS}$ pulse width, may be easily interfaced to any of today's high-speed microprocessors. The 12-bit single buffered input register will accept 12-bit parallel data from processors such as the 68000, 8086, TMS320 series, and the Analog Devices ADSP-2100. Several illustrative examples follow.

68000 – AD767 INTERFACE

Figure 6 illustrates the AD767 interface to a 68000 microprocessor. An active low decoded address is OR'ed with the processor's R/$\overline{W}$ signal to provide $\overline{CS}$ and latch data into the AD767. Later in the bus cycle the processor issues the upper ($\overline{UDS}$) and lower ($\overline{LDS}$) data strobes which are gated with the decoded address to provide $\overline{DTACK}$ and terminate the bus cycle. As shown, this interface will support a 12.5MHz 68000 system.

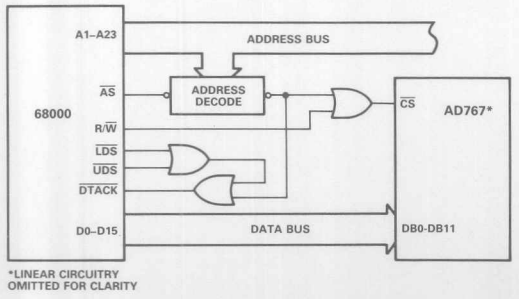


Figure 6. 68000 – AD767 Interface

8086 – AD767 INTERFACE

Interfacing the AD767 to the 8086 16-bit microprocessor requires a minimal amount of external components. A 10MHz 8086, for example, generates a 165ns low write pulse which may be gated with a decoded address to provide $\overline{CS}$ for the AD767. As $\overline{WR}$ returns high valid data is latched into the DAC. See Figure 7.

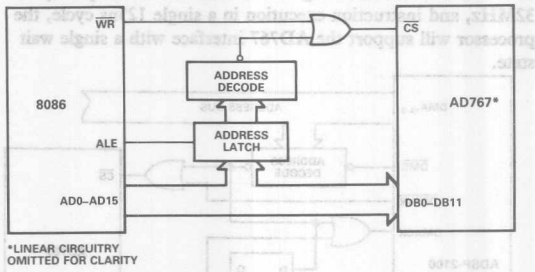


Figure 7. 8086 – AD767 Interface

TMS32010 – AD767 INTERFACE

The high-speed digital interface of the AD767 facilitates its use with the TMS32010 microprocessor at speeds up to 20MHz. In the three multiplexed LSBs of the address bus, PA2 – PA0 are decoded as a port address and OR'ed with the low write enable to generate $\overline{CS}$ for the DAC. A simple OUT xx,y instruction will output the data word stored in memory location xx to any one of eight port locations y.

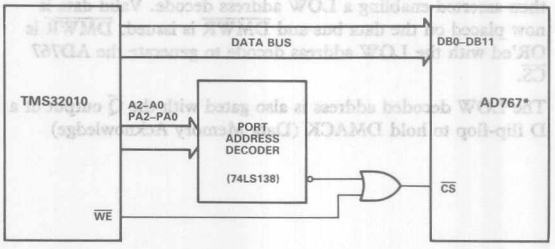


Figure 8. TMS32010 – AD767 Interface

TMS32020 – AD767 INTERFACE

Interfacing the AD767 to the TMS32020 microprocessor is easily achieved by using the TMS32020 I/O port capability. The $\overline{IS}$ signal distinguishes the I/O address space from the local program/data memory space and is used to enable a 74LS138 decoder. The decoded port address is then gated with the R/$\overline{W}$ and $\overline{STRB}$ signals to provide the AD767 $\overline{CS}$.

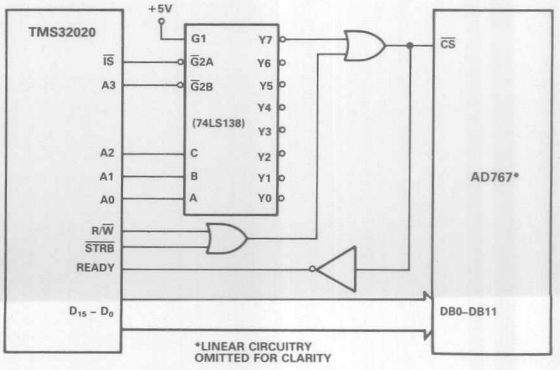


Figure 9. TMS32020 – AD767 Interface

ADSP-2100 – AD767 INTERFACE

The ADSP-2100 single chip DSP processor may be interfaced to the AD767 as shown in Figure 10. With a clock frequency of 32MHz, and instruction execution in a single 125ns cycle, the processor will support the AD767 interface with a single wait state.

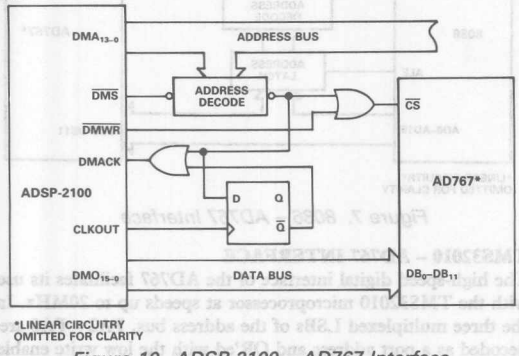


Figure 10. ADSP-2100 – AD767 Interface

At the beginning of the data memory access cycle the processor provides a 14-bit address on the DMA bus. The $\overline{DMS}$ signal is then asserted enabling a LOW address decode. Valid data is now placed on the data bus and $\overline{DMWR}$ is issued. $\overline{DMWR}$ is OR'ed with the LOW address decode to generate the AD767 $\overline{CS}$.

The LOW decoded address is also gated with the $\overline{Q}$ output of a D flip-flop to hold DMACK (Data Memory Acknowledge) LOW. This forces the processor into a wait state and extends the AD767 $\overline{CS}$ by 1 clock cycle. The rising edge of CLKOUT latches $\overline{Q}$ HIGH bringing DMACK HIGH. The cycle is now complete.

TMS320C25 – AD767 INTERFACE

Figure 11 illustrates the AD767 interface to a TMS320C25 digital signal processor. Due to the high-speed capability of the processor (40MHz), a single wait state is required and is easily generated using MSC. A 20MHz TMS320C25 however, does not require wait states and should be interfaced using the circuit shown in Figure 9.

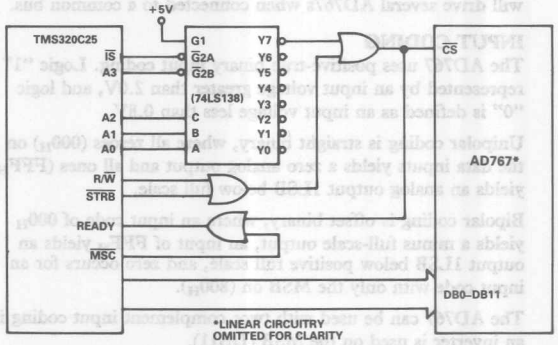


Figure 11. TMS320C25 – AD767 Interface

AD1139

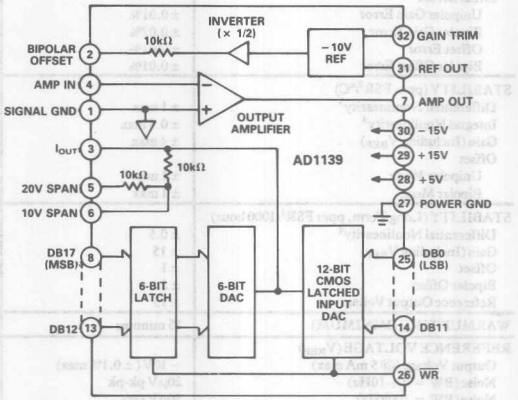
FEATURES

- 18-Bit Resolution
- Low Nonlinearity
  - Differential: ±1/2LSB max
  - Integral: ±1/2LSB max
- High Stability
  - Differential TC: ±1ppm/°C max
  - Integral TC: ±1/2ppm/°C max
  - Gain TC (with Reference): ±4ppm/°C max
- Fast Settling
  - Full Scale: 40µs to ±0.00019%
  - LSB: 6µs to ±0.00019%
- Small Hermetic 32-Lead Triple DIP Package
- Low Cost

APPLICATIONS

- Automatic Test Equipment
- Scientific Instrumentation
- Beam Positioners
- Digital Audio

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1139 is the first DAC offering 18-bit resolution (1 part in 262,144) and true 18-bit accuracy in a component size hybrid package. A proprietary bit switching technique provides high accuracy, speed and stability without compromising small size or low cost.

The AD1139 is a complete DAC with precision internal reference, latched data inputs and a quality output voltage amplifier. The analog output voltage ranges are pin programmable to +5V, +10V, ±5V and ±10V. Current output is also provided for use with external amplifiers. The internal precision −10V reference has a low ±3ppm/°C maximum temperature coefficient and is available for ratiometric applications.

The AD1139K is a true 18-bit accurate DAC with ±1/2LSB maximum differential and integral nonlinearity. The differential and integral nonlinearity temperature stability is guaranteed at ±1ppm/°C maximum and ±1/2ppm/°C maximum, respectively.

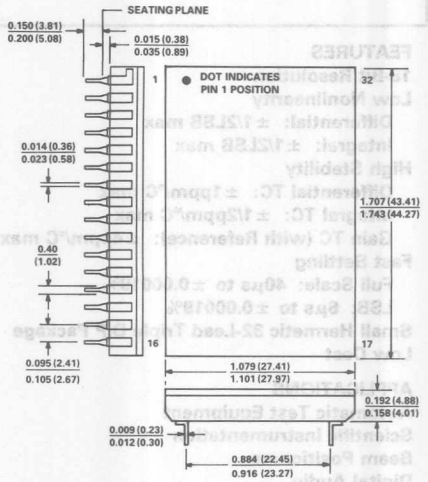
The AD1139 settles to within ±1/2LSB at 18 bits (±0.00019%) in 40µs for a full-scale step (10V). The glitch energy is a low 400mV × 500ns for a major carry, and wideband output noise is only 15µV.

The AD1139 operates from ±15V dc and +5V dc power supplies. Digital inputs are 5V CMOS compatible with binary input coding for unipolar output ranges and offset binary coding for bipolar ranges.

PRODUCT HIGHLIGHTS

1. Eighteen-bit resolution with ±1/2LSB maximum differential and integral nonlinearity in a hermetic 32-lead triple DIP package.
2. Complete DAC with internal reference, stable low-noise output amplifier, latched DAC inputs, reference output and internal application resistors for programmable output voltage ranges.
3. Temperature compensated internal precision reference with ±0.1% maximum initial accuracy and ±3ppm/°C maximum tempco.
4. Four pin programmable output voltage ranges (+5V, +10V, ±5V, ±10V) and current output available (−1mA, ±0.5mA).
5. The 18-bit parallel input latch assists in microprocessor interface.
6. Accurate measurements of the DAC's output are unusually simple since the AD1139 does *not* suffer from code dependent ground current errors.
7. True analog output remote sense capability.

ACCURACY		
Differential Nonlinearity	±1LSB max (= ±0.00038% max)	±1/2LSB max (= ±0.00019% max)
Integral Nonlinearity	±1LSB max (= ±0.00038%max)	±1/2LSB max (= ±0.00019% max)
Monotonicity (18 Bits)	Guaranteed	*
Initial Errors[1]		
Unipolar Gain Error	±0.01%	*
Bipolar Gain Error	±0.02%	*
Offset Error	±0.01%	*
Bipolar Offset Error	±0.01%	*
STABILITY (ppm FSR[2]/°C)		
Differential Nonlinearity[3]	±1 max	±0.5 typ, ±1 max
Integral Nonlinearity[3]	±0.5 max	*
Gain (Including V_{REF})	±4 max	*
Offset		
Unipolar Mode	±1 max	*
Bipolar Mode	±1 max	*
STABILITY (Long Term, ppm FSR[2]/1000 hour)		
Differential Nonlinearity[4]	±0.5	*
Gain (Including V_{REF})	±15	*
Offset	±1	*
Bipolar Offset	±2	*
Reference Output Voltage	±15	*
WARMUP TIME (MINIMUM)	15 minutes	*
REFERENCE VOLTAGE (V_{REF})		
Output Voltage (@ 5 mA max)	−10V (±0.1% max)	*
Noise (BW = 0.1-10Hz)	20μV pk-pk	10μV pk-pk
Noise (BW = 100kHz)	50μV rms	*
Tempco	3ppm/°C max	*
DYNAMIC PERFORMANCE		
Settling Time to 1/2LSB (@ 18 Bits)[5]		
Voltage		
Unipolar (10V Step)	40μs	*
Bipolar (20V Step)	60μs	*
Unipolar (LSB Step)	6μs	*
Bipolar (LSB Step)	8μs	*
Slew Rate	2V/μs	*
Current[6]		
Full-Scale Step	10μs	*
LSB Step	6μs	*
Glitch Energy (Major Carry @ 20MHz Bandwidth 0-to-10V Range)	400mV (500ns Duration)	*
DIGITAL INPUTS (5V CMOS Compatible)		
V_{IL}	≤0.8V	*
V_{IH}	≥3.5V	*
Unipolar Code	Binary (BIN)	*
Bipolar Code	Offset Binary (OBN)	*
ANALOG OUTPUT		
Current[4]	−1mA, ±0.5mA	*
Voltage (Pin Programmable)	+5V, +10V, ±5V, ±10V	*
Noise (Includes V_{REF})		
BW = 0.1-10Hz (μV pk-pk)	2×FSR	1×FSR
BW = 100kHz (Unipolar)	15μV rms	*
BW = 100kHz (Bipolar)	45μV rms	*
VOLTAGE COMPLIANCE	±10mV	*
Source Resistance		
Unipolar	3.3kΩ	*
Bipolar	2.85kΩ	*
Source Capacitance	10pF	*
POWER SUPPLY REQUIREMENTS		
+5V dc (±5%)	100μA	*
±15V dc (±5%)	+25mA, −30mA	*
POWER SUPPLY REJECTION		
(±15V dc)		
Gain	±2.5ppm/%	*
Offset	±0.3ppm/%	*
Reference Output	±2.5ppm/%	*
(+5V dc)		
Differential Nonlinearity	±0.15ppm/%	*
TEMPERATURE RANGE		
Operating (Rated Performance)	0 to +70°C	*
Storage	−40°C to +85°C	



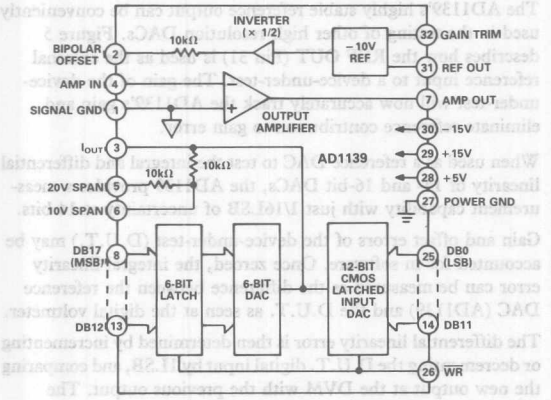


CAUTION: OBSERVE PROPER PLUG-IN POLARITY TO PREVENT DAMAGE TO CONVERTER

PIN DESIGNATIONS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SIGNAL GND	32	GAIN TRIM
2	BIPOLAR OFFSET	31	REF OUT
3	I_{OUT}	30	−15V
4	AMP IN	29	+15V
5	20V SPAN	28	+5V
6	10V SPAN	27	POWER GND
7	AMP OUT	26	$\overline{WR}$
8	DB17 (MSB)	25	DB0 (LSB)
9	DB16	24	DB1
10	DB15	23	DB2
11	DB14	22	DB3
12	DB13	21	DB4
13	DB12	20	DB5
14	DB11	19	DB6
15	DB10	18	DB7
16	DB9	17	DB8

NOTES
*Specifications same as AD1139J.
[1]Initial Errors are adjustable to zero via external potentiometers (see Figure 1).
[2]FSR means Full-Scale Range.
[3]Temperature stability of linearity is guaranteed to a 1% AQL, Level II sampling plan per MIL-STD-105.
[4]See Figure 7 for typical long-term linearity stability vs. temperature. Also, see the BURN-IN section on page 6 for caution against preconditioning by the user.
[5]Figure 9 provides typical LSB and full-scale settling time to within 1/2LSB at 12- to 18-bit resolutions.
[6]Current Output Operation is structured for input to the summing junction of an amplifier.
Specifications subject to change without notice.



AD1139 Functional Block Diagram

ANALOG OUTPUT RANGE

The AD1139 is pin programmable to provide a variety of analog outputs, either current or voltage. A unipolar output current of 0 to −1mA is available at Pin 3 and can be offset by 0.5mA (connect Pin 2 to Pin 3) for a biolar output of ±0.5mA. Output voltage ranges (+5V, +10V, ±5V and ±10V) are available at Pin 7 by connecting the current output (Pin 3) to the amplifier input (Pin 4) and the appropriate internal feedback resistors to the amplifier output (Pin 7) as shown in Figure 1.

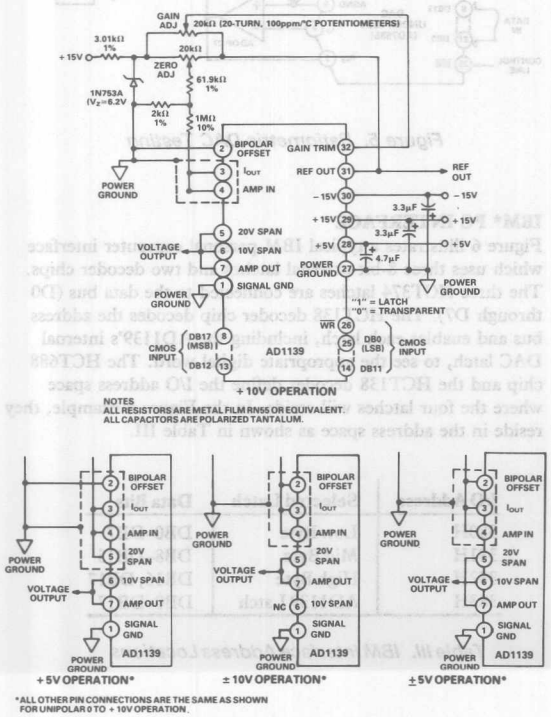


Figure 1. Output Voltage and Trim Configuration

OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 1. The offset adjust range is *plus 0.03% to minus 0.02% of full scale range* (wiper of potentiometer to REF OUT equals plus 0.03%). The gain adjust range is *plus 0.06% to minus 0.08% of full scale range* (wiper to REF OUT equals plus 0.06%). Measurement instruments used should be capable of resolving 1μV at plus full scale for the chosen output range and within 1μV of zero.

Procedure:

UNIPOLAR MODE

1. Apply a digital input of all "0s."
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1s."
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for exact value).

BIPOLAR MODE

1. Apply a digital input of 100 . . . . . 000.
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1s."
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for exact value).

	Code 000 00	Code 111 . . . 11	
Unipolar +5V	0.000000V	+4.999981V	
+10V	0.000000V	+9.999962V	
	Code 100 00	**Code 111 . . . .11**	**Code 000 . . . .00**
Bipolar ±5V	0.000000V	+4.999962V	−5.000000V
±10V	0.000000V	+9.999924V	−10.000000V

Table I. Full-Scale and Offset Calibration Voltages

Symbol	Parameter	Requirement
t_{DS}	Data Setup Time	160ns min
t_{DH}	Data Hold Time	120ns min
t_{WR}	Write Pulse Width	200ns min

Table II. Timing Requirements

TIMING DIAGRAM & LATCH CONTROL

Timing requirements for the AD1139 are shown in Table II. The timing diagram is shown in Figure 2. The WRite line controls an 18-bit wide data input latch. This latch is transparent when the WRite line is LOW, allowing all bits to be accessed directly. When the WRite line is activated HIGH, the data present at the inputs is held in the latch and the appropriate analog voltage is seen at the output.

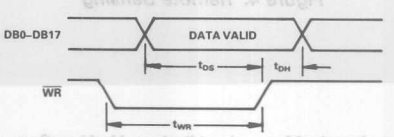


Figure 2. AD1139 Timing Diagram

GROUNDING & GUARDING

The current from measurement ground (Pin 1) is small and independent of the digital input code to the DAC. This greatly simplifies making error free analog measurements. Connect this high quality ground to the system's or application's high quality ground. Connect the DAC's power ground (Pin 27) to the system return, also connect the system's high quality ground to the system return. *It is most important that the measurement ground (Pin 1) and power ground (Pin 27) be connected externally for proper circuit operation.*

The current output pin (I_{OUT}, Pin 3) is sensitive to external noise sources, such as digital input lines. This pin and any components connected to this pin should be surrounded by a grounded guard as shown in Figure 3.

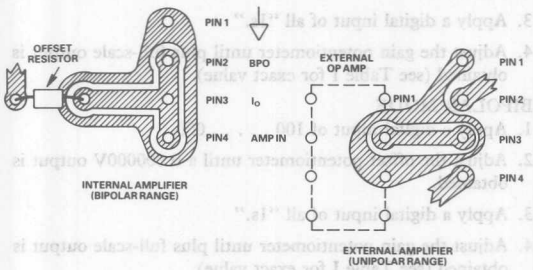


Figure 3. Guarding Recommendations

REMOTE SENSE APPLICATION

The AD1139's remote sense capability allows driving heavy loads or long cables without the usual, accompanying gain errors. By sensing at the load, as described in Figure 4, the load current will pass through the amplifier's output and the power ground, but not through the sense lines. The potential gain errors that would be induced by this load current are therefore minimized. The load should not exceed ± 10mA or 2 nanofarads to insure proper operation of the AD1139's internal output amplifier.

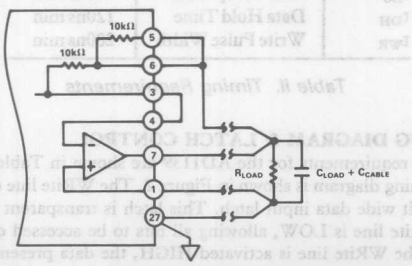


Figure 4. Remote Sensing

RATIOMETRIC DAC TESTING APPLICATION

The AD1139's highly stable reference output can be conveniently used in the testing of other high resolution DACs. Figure 5 describes how the REF OUT (Pin 31) is used as the external reference input to a device-under-test. The gain of the device-under-test will now accurately track the AD1139's gain and eliminate reference contribution to gain error.

When used as a reference DAC to test the integral and differential linearity of 14- and 16-bit DACs, the AD1139 provides a measurement capability with just 1/16LSB of uncertainty at 14 bits.

Gain and offset errors of the device-under-test (D.U.T.) may be accounted for in software. Once zeroed, the integral linearity error can be measured as the difference between the reference DAC (AD1139) and the D.U.T. as seen at the digital voltmeter.

The differential linearity error is then determined by incrementing or decrementing the D.U.T. digital input by 1LSB, and comparing the new output at the DVM with the previous output. The difference between these two measurements should be exactly one ideal LSB. The amount of disagreement from one ideal LSB is the differential linearity error.

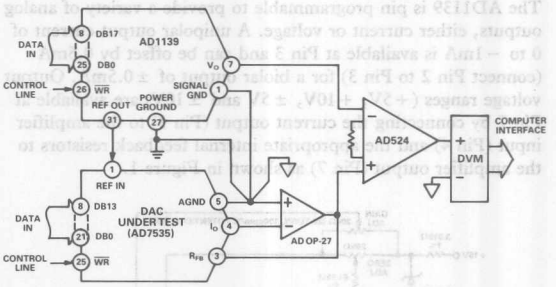


Figure 5. Ratiometric DAC Testing

IBM* PC INTERFACE

Figure 6 illustrates a typical IBM personal computer interface which uses three 8-bit external latches and two decoder chips. The three HCT374 latches are connected to the data bus (D0 through D7). The HCT138 decoder chip decodes the address bus and enables each latch, including the AD1139's internal DAC latch, to see the appropriate digital word. The HCT688 chip and the HCT138 decoder define the I/O address space where the four latches will reside. In the Figure 6 example, they reside in the address space as shown in Table III.

I/O Address	Selected Latch	Data Bits
380H	Low Byte	DB0–DB7
381H	Mid Byte	DB8–DB15
382H	High Byte	DB16, DB17
383H	AD1139 Latch	DB0–DB17

Table III. IBM Interface Address Locations

***IBM is a trademark of International Business Machines Corp.**

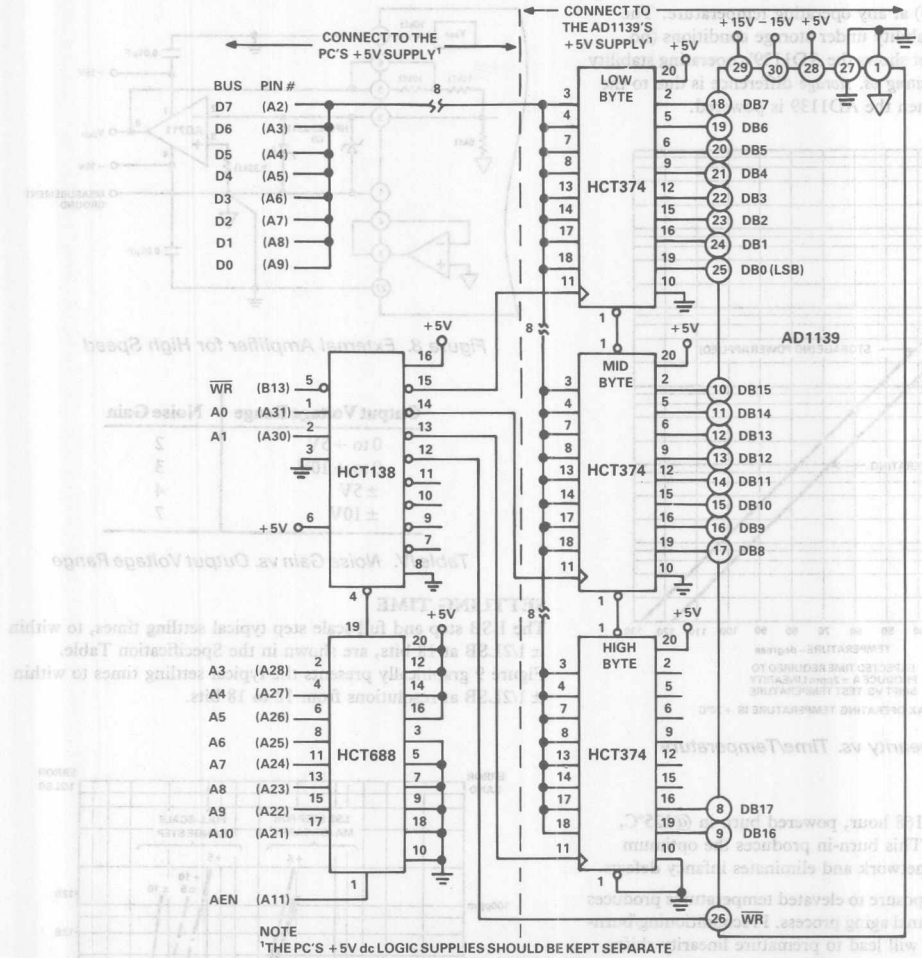


Figure 6. AD1139 to IBM PC Compatible Interface

LONG-TERM STABILITY VS. TEMPERATURE

Adjusting the linearity of any DAC after it is installed in the application is often difficult or impossible. It is preferable to maintain some specified accuracy over the useful working life of the product (commonly 5 to 10 years). Stable linearity performance over time can, therefore, be a very important parameter for the DAC.

Accelerated testing to determine the *expected linearity stability over time* can be accomplished by two different methods. Linearity is first measured at +25°C. The DAC is then operated at a fixed elevated temperature for an extended period of time. The DAC is then retested at +25°C, and the change in linearity error vs. time is calculated. The ARRHENIUS EQUATION (used in reliability calculations) can be used to determine what the acceleration factor is from +25°C to the elevated test temperature. Knowing the acceleration factor and the linearity error vs. time at the elevated temperature, one could calculate the expected long-term stability of linearity at nominal temperatures.

A second test method determines how long it will take for the linearity to shift by a specific error band (we chose ±2ppm for our example) at any specified temperature. The first step is to measure the linearity at a moderately elevated temperature (e.g., +85°C) and then monitor how long it takes at this temperature to reach the error band limit. The second step is to perform the same test at a much higher elevated temperature (e.g., +125°C). The two resulting time vs. temperature points are then plotted on semilog paper. A line drawn through the two points allows extrapolation to the length of time expected to reach the error band (±2ppm) at other temperatures, including +25°C.

Figure 7 shows how long it would take for the AD1139's linearity to drift ±2ppm (1/2LSB) at any operating temperature. The uppermost plot shows stability under storage conditions (no power), and the lower plot shows the AD1139's operating stability (under power). The *operating vs. storage* difference is due to the 10°C temperature rise when the AD1139 is powered.

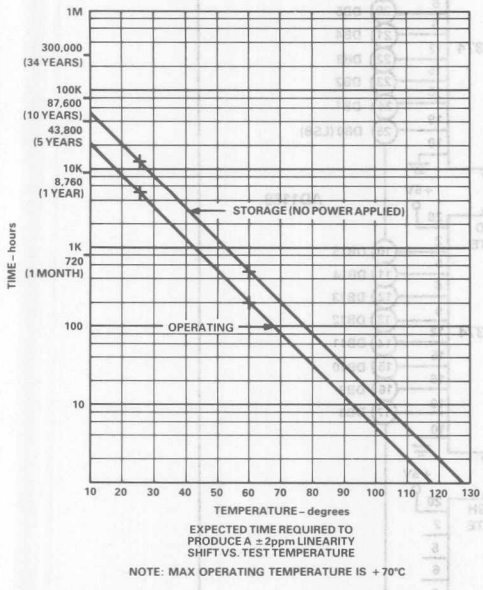


Figure 7. Nonlinearity vs. Time/Temperature

BURN-IN

All AD1139s undergo a 168 hour, powered burn-in @125°C, prior to laser trimming. This burn-in produces the optimum stability for the resistor network and eliminates infancy defects.

As shown in Figure 7, exposure to elevated temperatures produces an acceleration of the normal aging process. Preconditioning/burn-in employed by the user will lead to premature linearity shifts outside of the initial guaranteed specifications. The ADI warranty will not cover DACs that exhibit this type of *forced* premature specification degradation.

EXTERNAL AMPLIFIER FOR HIGH SPEED OR HIGH OUTPUT CURRENT

The AD1139's internal output amplifier is optimized for very low noise, dc stable applications with moderate settling time. Applications requiring higher speed or more output current can use an external amplifier, such as shown in Figure 8. The AD711 settles to within 16 bits in only 6µs for a unipolar full scale step. Other amplifiers may be chosen for differing tradeoffs. The noise gain seen by the output amplifier, depends on the output voltage range selected (see Table IV). The amplifier selected must be stable at the noise gain corresponding to the output range.

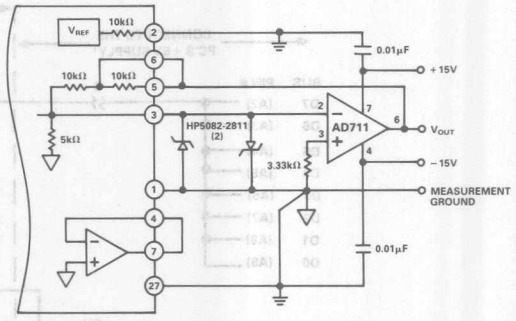


Figure 8. External Amplifier for High Speed

Output Voltage Range	Noise Gain
0 to +5V	2
0 to +10V	3
±5V	4
±10V	7

Table IV. Noise Gain vs. Output Voltage Range

SETTLING TIME

The LSB step and full-scale step typical settling times, to within ±1/2LSB at 18 bits, are shown in the Specification Table. Figure 9 graphically presents the typical settling times to within ±1/2LSB at resolutions from 12 to 18 bits.

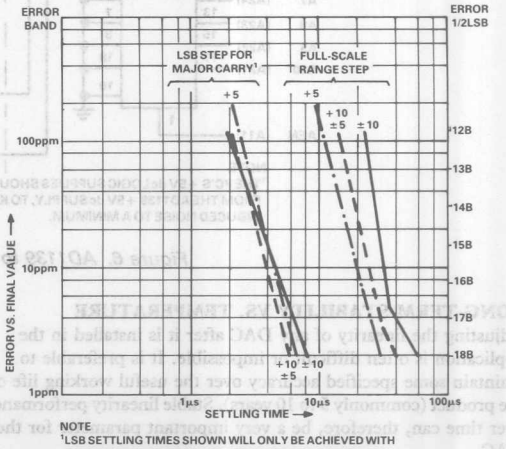
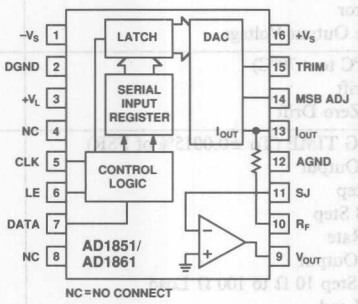


Figure 9. Settling Time vs. Resolution

FEATURES
110 dB SNR
Fast Settling Permits 16× Oversampling
±3 V Output
Optional Trim Allows Super-Linear Performance
±5 V Operation
16-Pin Plastic DIP and SOIC Packages
Pin-Compatible with AD1856 & AD1860 Audio DACs
2s Complement, Serial Input

APPLICATIONS
High-End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

FUNCTIONAL BLOCK DIAGRAM



NC=NO CONNECT

PRODUCT DESCRIPTION

The AD1851/AD1861 is a monolithic PCM audio DAC. The AD1851 is a 16-bit device, while the AD1861 is an 18-bit device. Each device provides a voltage output amplifier, DAC, serial-to-parallel register and voltage reference. The digital portion of the AD1851/AD1861 is fabricated with CMOS logic elements that are provided by Analog Devices' 2 μm ABCMOS process. The analog portion of the AD1851/AD1861 is fabricated with bipolar and MOS devices as well as thin-film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser-trimming of the linearity error affords low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small, contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3 V signal at load currents up to 8 mA. When used in current output mode, the AD1851/AD1861 provides a ±1 mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The AD1851 input clock can support a 12.5 MHz data rate, while the AD1861 input clock can support a 13.5 MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4×, 8× and 16× sampling frequencies.

The critical specifications of THD+N and signal-to-noise ratio are 100% tested for all devices.

The AD1851/AD1861 operates with ±5 V power supplies, making it suitable for home use markets. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. Power dissipation is 100 mW typical.

The AD1851/AD1861 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Both packages incorporate the industry standard pinout found on the AD1856 and AD1860 PCM audio DACs. As a result, the AD1851/AD1861 is a drop-in replacement for designs where ±5 V supplies have been used with the AD1856/AD1860. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

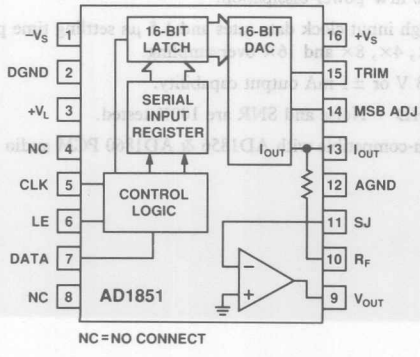
PRODUCT HIGHLIGHTS

1. AD1851 16-bit resolution provides 96 dB dynamic range. AD1861 18-bit resolution provides 108 dB dynamic range.
2. No external components are required.
3. Operates with ±5 V supplies.
4. Space saving 16-pin SOIC and plastic DIP packages.
5. 100 mW power dissipation.
6. High input clock data rates and 1.5 μs settling time permits 2×, 4×, 8× and 16× oversampling.
7. ±3 V or ±1 mA output capability.
8. THD + Noise and SNR are 100% tested.
9. Pin-compatible with AD1856 & AD1860 PCM audio DACs.

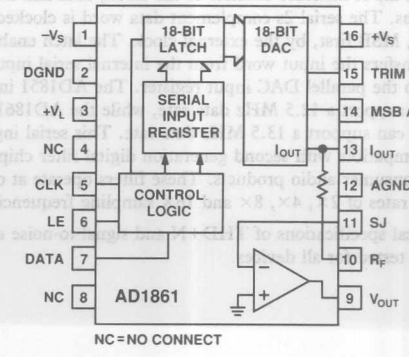
AD1851/AD1861—SPECIFICATIONS (T_A @ +25°C and ±5 V supplies, unless otherwise noted)

	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			1.0	μA
I_{IL}, $V_{IL} = 0.4$			−10	μA
ACCURACY				
Gain Error		±1		%
Midscale Output Voltage		±10		mV
DRIFT (0°C to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (To ±0.0015% of FSR)				
Voltage Output				
6 V Step		1.5		μs
1 LSB Step		1.0		μs
Slew Rate		9		V/μs
Current Output				
1 mA Step 10 Ω to 100 Ω Load		350		ns
1 kΩ Load		350		ns
OUTPUT				
Voltage Output Configuration				
Bipolar Range	±2.88	±3.0	±3.12	V
Output Current		±8		mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage				
$+V_L$ and $+V_S$	4.75		5.25	V
$-V_S$	−5.25		−4.75	V
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.



AD1851 Functional Block Diagram



AD1861 Functional Block Diagram

AD1851

	Min	Typ	Max	Units
RESOLUTION			16	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1851N-J, R-J		0.003	0.004	%
AD1851N, R		0.004	0.008	%
−20 dB, 990.5 Hz				
AD1851N-J, R-J		0.009	0.016	%
AD1851N, R		0.009	0.040	%
−60 dB, 990.5 Hz				
AD1851N-J, R-J		0.9	1.6	%
AD1851N, R		0.9	4.0	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1851N, R	88			dB
AD185IN-J, R-J	96			dB
SIGNAL-TO-NOISE RATIO	107	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	12.5			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		14		Bits
POWER SUPPLY				
Current				
+I		10.0	13.0	mA
−I		−10.0	−15.0	mA
Power Dissipation		100		mW

AD1861

	Min	Typ	Max	Units
RESOLUTION			18	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1861N-J, R-J		0.003	0.004	%
AD1861N, R		0.004	0.008	%
−20 dB, 990.5 Hz				
AD1861N-J, R-J		0.009	0.016	%
AD1861N, R		0.009	0.040	%
−60 dB, 990.5 Hz				
AD1861N-J, R-J		0.9	1.6	%
AD1861N, R		0.9	4.0	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1861N, R	88			dB
AD186IN-J, R-J	96			dB
SIGNAL-TO-NOISE RATIO	107	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	13.5			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		15		Bits
POWER SUPPLY				
Current				
+I		10.0	13.0	mA
−I		−10.0	−15.0	mA
Power Dissipation		100		mW

*Tested in accordance with EIAJ Test Standard CP-307.
Specifications subject to change without notice.

V_L to DGND . . . . . 0 V to 6.50 V
V_S to AGND . . . . . 0 V to 6.50 V
$-V_S$ to AGND . . . . . −6.50 V to 0 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
AGND to DGND . . . . . ±0.3 V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1	$-V_S$	ANALOG NEGATIVE POWER SUPPLY
2	DGND	LOGIC GROUND
3	V_L	LOGIC POSITIVE POWER SUPPLY
4	NC	NO CONNECTION
5	CLK	CLOCK INPUT
6	LE	LATCH ENABLE INPUT
7	DATA	SERIAL DATA INPUT
8	NC	NO INTERNAL CONNECTION*
9	V_{OUT}	VOLTAGE OUTPUT
10	R_F	FEEDBACK RESISTOR
11	SJ	SUMMING JUNCTION
12	AGND	ANALOG GROUND
13	I_{OUT}	CURRENT OUTPUT
14	MSB ADJ	MSB ADJUSTMENT TERMINAL
15	TRIM	MSB TRIMMING POTENTIOMETER TERMINAL
16	V_S	ANALOG POSITIVE POWER SUPPLY

*PIN 8 HAS NO INTERNAL CONNECTION; $-V_L$ FROM AD1856 OR AD1860 SOCKET CAN BE SAFELY APPLIED.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

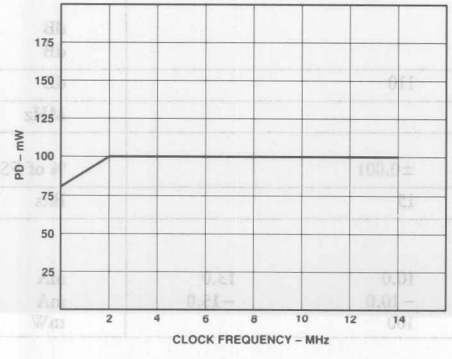


ORDERING GUIDE

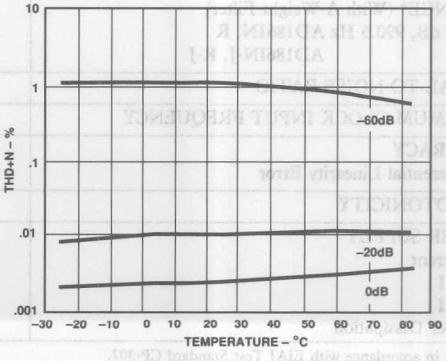
Model	Resolution	THD+N	Package Option*
AD1851N	16 Bits	0.008%	N-16
AD1851N-J	16 Bits	0.004%	N-16
AD1851R	16 Bits	0.008%	R-16A
AD1851R-J	16 Bits	0.004%	R-16A
AD1861N	18 Bits	0.008%	N-16
AD1861N-J	18 Bits	0.004%	N-16
AD1861R	18 Bits	0.008%	R-16A
AD1861R-J	18 Bits	0.004%	R-16A

*N = Plastic DIP Package; R = Small Outline (SOIC) Package.
For outline information see Package Information section.

Typical Performance



Power Dissipation vs. Clock Frequency



THD vs. Temperature

TOTAL HARMONIC DISTORTION

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the first 19 harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small signal amplitudes (−20 dB and −60 dB).

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. This specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

SETTLING TIME

Settling time is the time required for the output of the DAC to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

MIDSCALE ERROR

Midscale error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0 V) when the 2s complement input code representing half scale is loaded in the input register.

D-RANGE DISTORTION

D-range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of −60 dB below full scale is reproduced. D-range is tested with a 1 kHz input sine wave. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio (SNR) is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

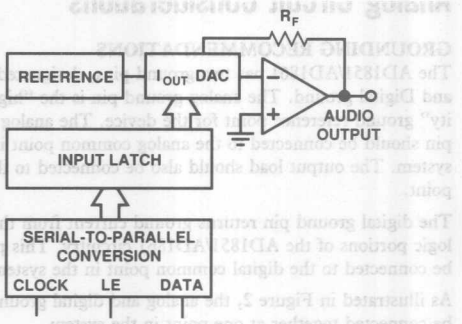


Figure 1. AD1851/AD1861 Functional Block Diagram

FUNCTIONAL DESCRIPTION

The AD1851/AD1861 is a complete monolithic PCM audio DAC. No additional external components are required for operation. As shown in Figure 1 above, each chip contains a voltage reference, an output amplifier, a DAC, an input latch and a parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on-chip feedback resistor, the output op amp converts the output current of the AD1851/AD1861 to a voltage output.

The DAC uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser-trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input register and serial-to-parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1851/AD1861.

Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1851/AD1861 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1851/AD1861 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 2, the analog and digital grounds should be connected together at one point in the system.

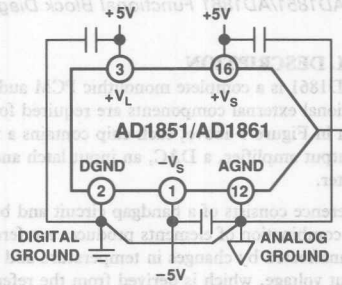


Figure 2. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1851/AD1861 has three power supply input pins. The $\pm V_S$ supplies provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate at ± 5 V.

The $+V_L$ supply operates the digital portions of the chip including the input shift register and the input latching circuitry. The $+V_L$ supply is designed to operate at $+5$ V.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as to the common points. The logic supply, $+V_L$, should be decoupled to digital common, while the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of three separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to improved performance.

However, three separate voltage supplies are not necessary for good circuit performance. For example, Figure 3 illustrates a system where only a single positive and a single negative supply are available.

In this example, the positive logic and positive analog supplies must both be connected to $+5$ V, while the negative analog supply will be connected to -5 V. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

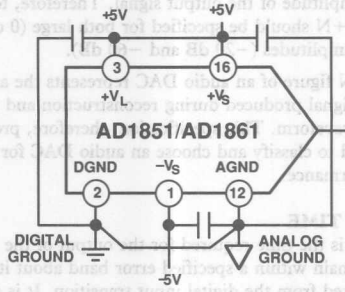


Figure 3. Alternate Recommended Schematic

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using the AD1851/AD1861.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 4 may be used to improve performance. The adjustment should be made with a small signal input (-20 dB or -60 dB).

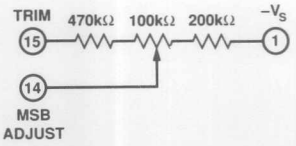


Figure 4. Optional THD Adjust Circuit

AD1851 DIGITAL CIRCUIT CONSIDERATIONS

AD1851 Input Data

Data is transmitted to the AD1851 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 5 illustrates the general signal requirements for data transfer to the AD1851.

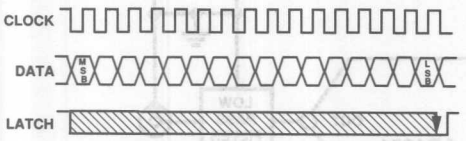


Figure 5. Signal Requirements for AD1851

Figure 6 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1851 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 5 and 6 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1851 input clock can run at a 12.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

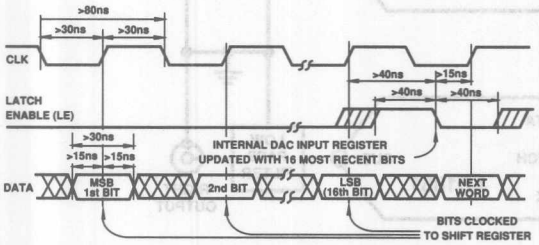


Figure 6. Timing Relationships of AD1851 Input Signals

AD1861 DIGITAL CIRCUIT CONSIDERATIONS

AD1861 Input Data

Data is transmitted to the AD1861 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer to the AD1861.

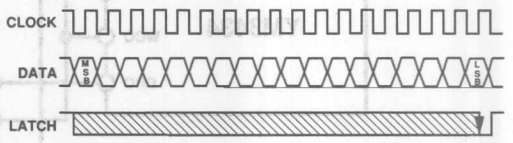


Figure 7. Signal Requirements for AD1861

Figure 8 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1861 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 7 and 8 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1861 input clock can run at a 13.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

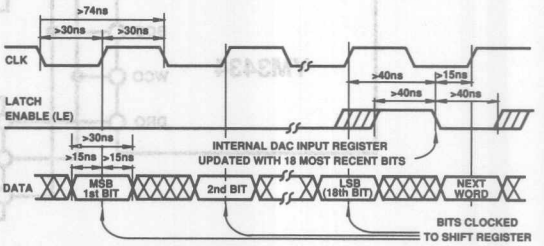


Figure 8. Timing Relationships of AD1861 Input Signals

APPLICATIONS

Figures 9 through 12 show connection diagrams for the AD1851 and AD1861 and the Yamaha YM3434 and the NPC SM5813AP/APT digital filter chips.

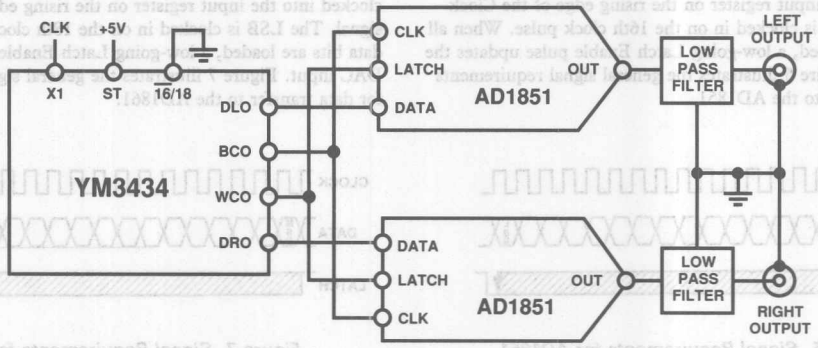


Figure 9. AD1851 with Yamaha YM3434 Digital Filter

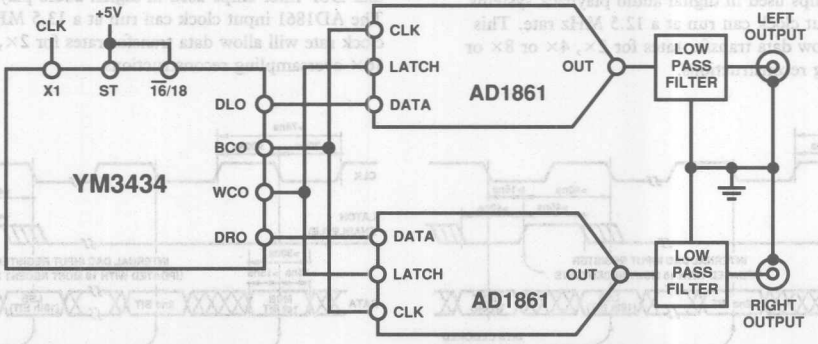


Figure 10. AD1861 with Yamaha YM3434 Digital Filter

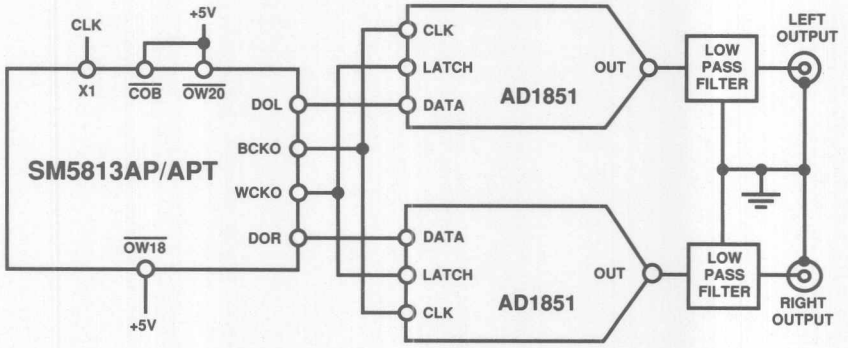


Figure 11. AD1851 with NPC SM5813AP/APT Digital Filter

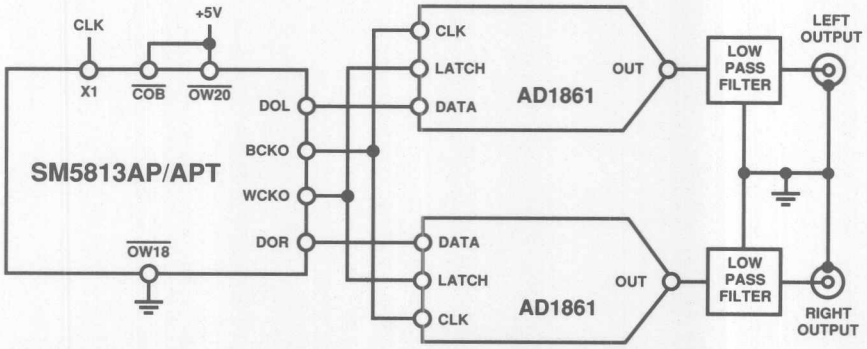


Figure 12. AD1861 with NPC SM5813AP/APT Digital Filter

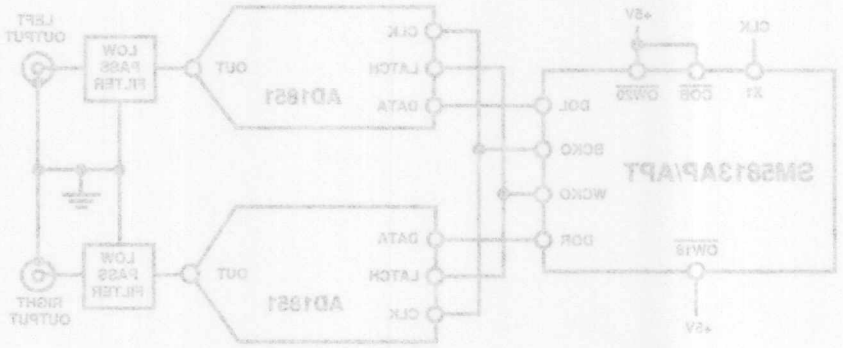


Figure 11. AD1851 with NPC SM5813AP/APT Digital Filter

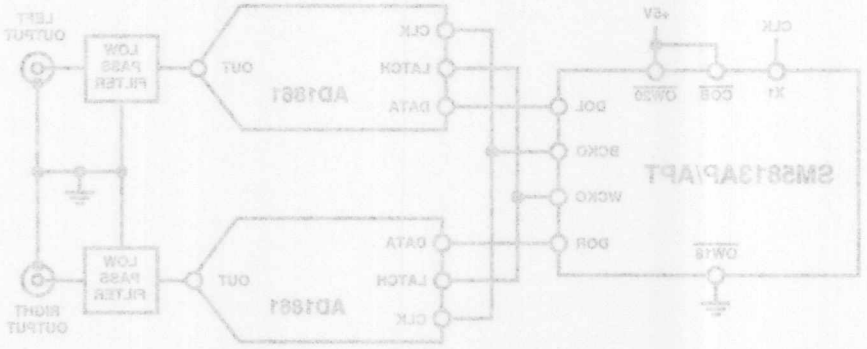


Figure 12. AD1861 with NPC SM5813AP/APT Digital Filter

ANALOG DEVICES

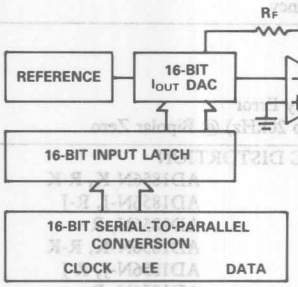
16-Bit PCM Audio DAC

AD1856

FEATURES
0.0025% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP or SOIC Package
Serial Input

APPLICATIONS
Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1856 is a monolithic 16-bit PCM Audio DAC. Each device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1856 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1856 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reconstructions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 10MHz clock rate. This serial input port is compatible with popular digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequency.

The AD1856 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home-use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is a typical 300mW when ±12V supplies are used.

The AD1856 is packaged in a 16-pin plastic DIP or SOIC package and incorporates the industry-standard pinout. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. Total harmonic distortion is 100% tested.
2. MSB trim feature allows superlinear operation.
3. The AD1856 operates with ±5V to ±12V supplies.
4. Serial interface is compatible with digital filter chips.
5. 1.5μs settling time permits 2×, 4× and 8× oversampling.
6. No external components are required.
7. 96dB dynamic range.
8. ±3V or ±1mA output capability.
9. 16-bit resolution.
10. 2s complement serial input words.
11. Low cost.
12. 16-pin plastic DIP or SOIC package.

RESOLUTION				**16**	Bits
DIGITAL INPUTS	V_{IH}		2.4	V_L	V
	V_{IL}		0	0.8	V
	I_{IH}, $V_{IH} = V_L$			**1.0**	µA
	I_{IL}, $V_{IL} = 0.4$			**−10**	µA
Clock Input Frequency			**10**		MHz
ACCURACY					
Gain Error				±2.0	%
Bipolar Zero Error				±30	mV
Differential Linearity Error				±0.001	% of FSR
Noise (rms, 20Hz to 20kHz) @ Bipolar Zero				6	µV
TOTAL HARMONIC DISTORTION					
0dB, 990.5Hz	AD1856N-K, R-K			0.002	**0.0025** %
	AD1856N-J, R-J			0.002	**0.004** %
	AD1856N, R			0.002	**0.008** %
−20dB, 990.5Hz	AD1856N-K, R-K			0.018	**0.020** %
	AD1856N-J, R-J			0.018	**0.040** %
	AD1856N, R			0.018	**0.040** %
−60dB, 990.5Hz	AD1856N-K, R-K			1.8	**2.0** %
	AD1856N-J, R-J			1.8	**4.0** %
	AD1856N, R			1.8	**4.0** %
MONOTONICITY				15	Bits
DRIFT (0 to +70°C)					
Total Drift				±25	ppm of FSR/°C
Bipolar Zero Drift				±4	ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)					
Voltage Output	6V Step			1.5	µs
	1LSB Step			1.0	µs
	Slew Rate			9	V/µs
Current Output	1mA Step 10Ω to 100Ω Load			350	ns
	1kΩ Load			350	ns
WARM-UP TIME			1		min
OUTPUT					
Voltage Output Configuration					
Bipolar Range				±3	V
Output Current			±8		mA
Output Impedance				0.1	Ω
Short Circuit Duration				Indefinite to Common	
Current Output Configuration					
Bipolar Range (±30%)				1.0	mA
Output Impedance (±30%)				1.7	kΩ
POWER SUPPLY					
Voltage, $+V_L$ and $+V_S$			4.75	5	13.2 V
Voltage, $-V_L$ and $-V_S$			−13.2	−5	−4.75 V
Current, +I, V_L and V_S = +5V, 10MHz Clock				10	**15** mA
Current, −I, $-V_L$ and $-V_S$ = −5V, 10MHz Clock				−12	**−15** mA
Current, +I, V_L and V_S = +12V, 10MHz Clock				12	mA
Current, −I, $-V_L$ and $-V_S$ = −12V, 10MHz Clock				−15	mA
POWER DISSIPATION					
V_S and V_L = ±5V, 10MHz Clock				110	**150** mW
V_S and V_L = ±12V, 10MHz Clock				135	mW
TEMPERATURE RANGE					
Specification			0		+70 °C
Operation			−25		+70 °C
Storage			−60		+100 °C

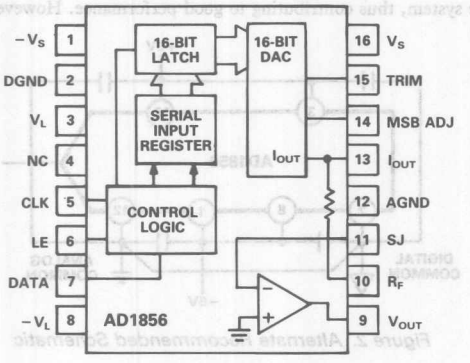
Specifications subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND. . . . . −13.2 to 0V
$-V_S$ to AGND . . . . . −13.2 to 0V
Digital Inputs to DGND . . . . . −0.3 to V_L
AGND to DGND . . . . . ±0.3V
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



Definition of Specifications

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is the primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dB). The theoretical dynamic range of an n-bit converter is approximately (6×n) dB. In the case of the 16-bit AD1856, that is 96dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and quantization and other errors.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the deviation in the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale (all 0s) is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

FUNCTIONAL DESCRIPTION

The AD1856 is a complete, monolithic 16-bit PCM audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, a 16-bit DAC, a 16-bit input latch and a 16-bit serial-to-parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This circuitry produces an output voltage that is stable over time and temperature changes.

The 16-bit D/A converter uses a combination of segmented decoder and R-2R architectures to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew-rate and optimum settling time. When combined with the on-board feedback resistor, the output op amp can convert the output current of the AD1856 to a voltage output.

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1856 has two ground pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1856 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

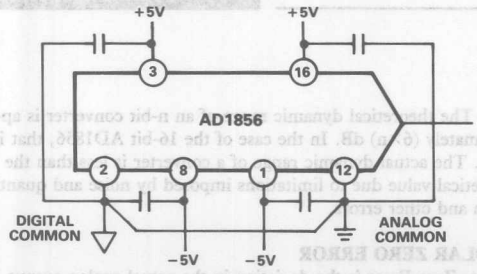


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1856 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to operate from ±5V to ±12V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portions of the system, thus contributing to good performance. However,

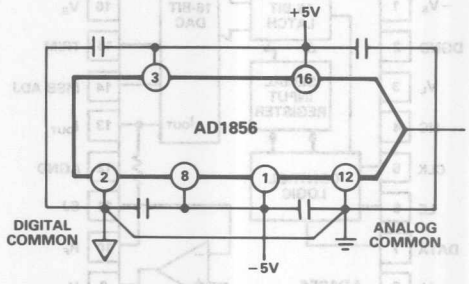


Figure 2. Alternate Recommended Schematic

four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available. Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1856. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low-pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

Analog Devices tests and grades all AD1856s on the basis of THD performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream, representing a 0db, −20dB or −60dB sine wave is sent to the device under test. The frequency of this waveform is 990.5Hz. Input data is sent to the AD1856 at a $4\times F_S$ rate (176.4kHz). The AD1856 under test produces an analog output signal with the on-board op amp.

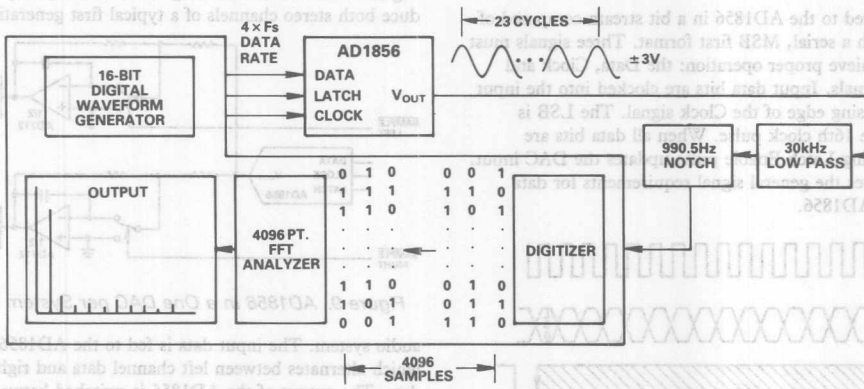


Figure 3. Block Diagram of Distortion Test Circuit

The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096 point FFT is performed on the results of the test. Based on the first 9 harmonics of the fundamental 990.5Hz output wave, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout and manufacturing techniques employed in the production of the AD1856 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1856 for various amplitudes of a 1kHz output signal. As can be seen, the AD1856 offers excellent performance, even at amplitudes as low as −60dB. Figure 5 illustrates the typical THD vs. frequency performance.

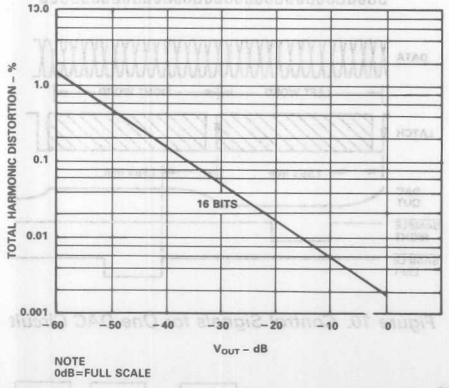


Figure 4. Typical Unadjusted THD vs. Amplitude

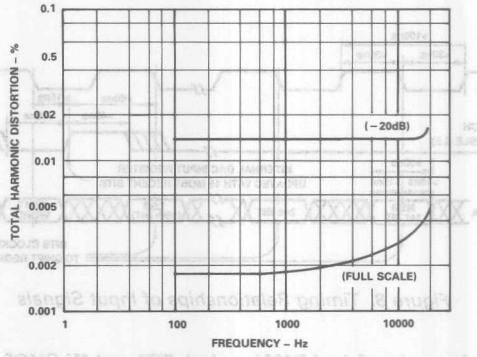


Figure 5. Typical THD vs. Frequency

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity errors around midscale to be eliminated. These errors are especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases and THD increases.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 6 may be used. This circuit allows the differential linearity error at midscale to be zeroed out. However, no adjustments are required to meet data sheet specifications.

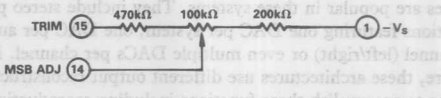


Figure 6. Optional THD Adjust Circuit

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1856 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation: the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer for the AD1856.

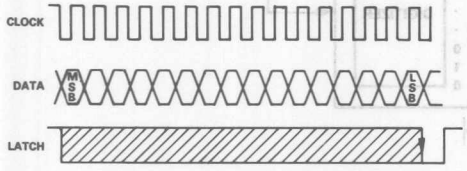


Figure 7. Signal Requirements of AD1856

Figure 8 provides the specific timing requirements that must be met in order for the data transfer to be accomplished properly.

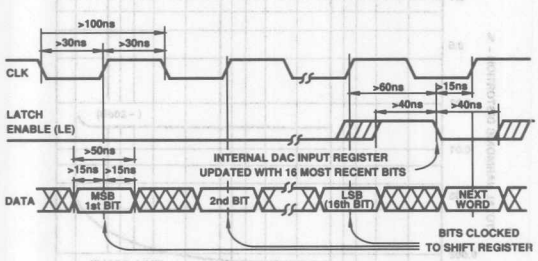


Figure 8. Timing Relationships of Input Signals

The input pins of the AD1856 are both TTL and 5V CMOS compatible, independent of power supply voltages used.

The input requirements illustrated in Figures 7 and 8 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1856 input clock can run at a 10MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this data sheet contains additional guides for using the AD1856 with various DSP filter chips available from Sony, NPC and Yamaha.

APPLICATIONS OF THE AD1856 PCM AUDIO DAC

The AD1856 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio-amplifier and DAT systems can all use the AD1856. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or even multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

One DAC per System

Figure 9 shows a circuit using one AD1856 per system to reproduce both stereo channels of a typical first generation digital

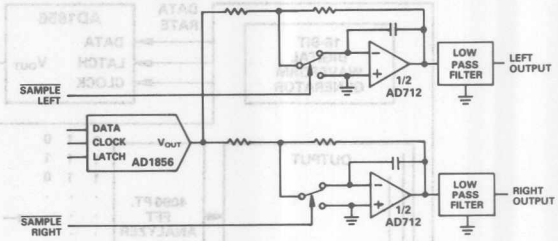


Figure 9. AD1856 in a One DAC per System Architecture

audio system. The input data is fed to the AD1856 in a format which alternates between left channel data and right channel data. The output of the AD1856 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1856. The timing diagram for the control signals for this circuit is shown in Figure 10.

The architecture illustrated in Figure 9 is suitable for low-end home or portable systems. However, its usefulness in mid- or high-end digital audio reproduction is limited by the phase delay which is introduced in the multiplexed output. This phase delay is due to the fact that the information contained in the input bit stream represents left and right channel audio sampled simultaneously but reconstructed alternately. One obvious solution to this problem may be arrived at by incorporating a third, noninverting SHA to delay the output of one channel to "catch up to" the other channel. This eliminates the phase shift by restoring simultaneous reproduction. This solution is illustrated in Figure 11.

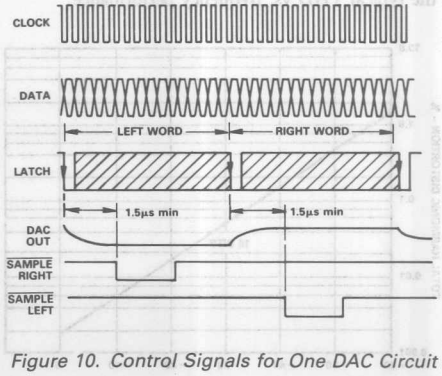


Figure 10. Control Signals for One DAC Circuit

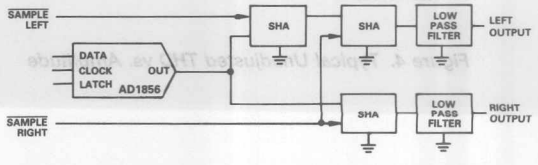


Figure 11. Third SHA Eliminates Phase Delay

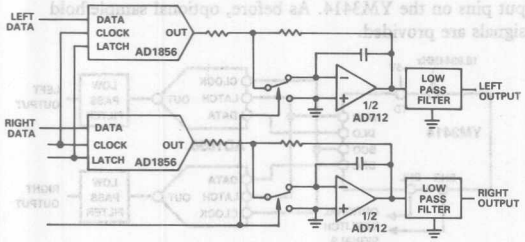


Figure 12. One DAC per Channel Architecture

One DAC per Channel

Another approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bit streams for the left channel and the right channel are simultaneously sent and latched into each DAC. This "second generation" approach, shown in Figure 12, is suitable for higher performance digital-audio playback units.

Two DACs per Channel (Four DAC System)

Another architecture uses two DACs per channel. In this scheme, shown in Figure 13, each DAC reproduces one half of the output waveform. The advantage obtained is that midscale differential linearity error no longer effects the zero-crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses ±3/4 full scale. The result is that THD performance for low amplitude signals is greatly improved. Not shown in Figure 13 is a VLSI circuit required to separate the incoming data into the appropriate form required by each DAC.

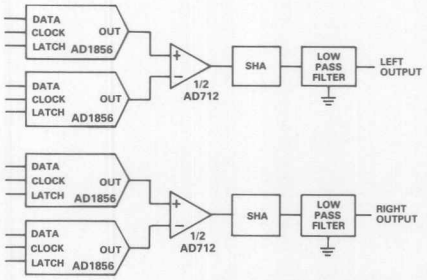


Figure 13. Two DACs per Channel Eliminate Midscale Distortion from the Zero-Crossing Points

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4× F_S yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low-pass filters which usually follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency.

When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz and from 44.1kHz to 64kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often use low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2× reconstruction frequency (88.2kHz) is used, the lowest unwanted frequency components now extend down to approximately 68kHz. A 4× rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require that the serial input data stream run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters."

The AD1856 is compatible with popular digital filter chips used in digital audio products such as the NPC SM5807, NPC SM5805, Yamaha YM3414, and Sony CXD1136.

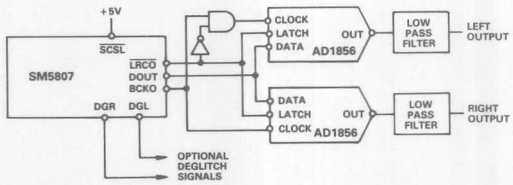


Figure 14. NPC SM5807 and AD1856 Interface

DUAL DAC, 4× F_S OVERSAMPLING ARCHITECTURE

Figure 14 illustrates the use of an NPC digital filter chip with two AD1856 audio DACs. This scheme achieves four times oversampling reconstruction with a dedicated DAC per channel. In this example of a typical compact disc player application, the digital filter chip accepts serial input words from the digital decoder/processor at a 44.1kHz sample rate. Through the use of oversampling, the SM5807 transmits data to the two DACs at a 176.4kHz rate. The serial DAC input data is sent out of the DOUT pin to the serial inputs of the DACs. Left channel and right channel data are sent alternately down the same wire. The Left/Right Channel Output signal, $\overline{\text{LRCO}}$ and two logic gates demultiplex the data clock signals from BCKO. In this example,

the BCKO rate is 192×F_S. However, a 196×F_S clock can be used if $\overline{SCSL}$ is wired to a logic zero. Finally, left and right channel deglitching signals are provided. At the user's option, these signals may be used to control external sample-hold amplifiers in order to obtain optimal performance.

ACHIEVING 8× F_S OVERSAMPLING WITH AD1856S AND YAMAHA YM3414

Figure 15 illustrates the combination of a Yamaha YM3414 digital filter chip and two AD1856 audio DACs. In this scheme, the use of a 16.9344MHz clock allows an 8 times oversampling rate for extremely high performance. In addition, a lower-order low-pass filter may be used without sacrificing performance. The DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3414. As before, optional sample/hold signals are provided.

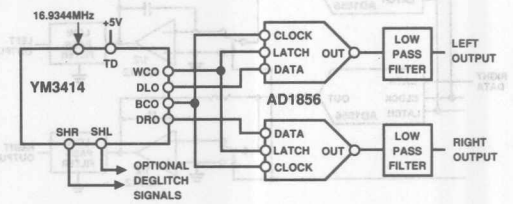


Figure 15. Yamaha YM3414 and AD1856 Interface

ORDERING GUIDE

Model	THD @ FS	Package Option*
AD1856N, R	0.008%	N-16, R-16A
AD1856N-J, R-J	0.004%	N-16, R-16A
AD1856N-K, R-K	0.0025%	N-16, R-16A

*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.

ANALOG DEVICES

18-Bit PCM Audio DAC

AD1860

FEATURES

- 0.002% THD + Noise
- Fast Settling Permits 8× Oversampling
- ±3V Output
- Optional Trim Allows Superlinear Performance
- ±5V to ±12V Operation
- 16-Pin Plastic DIP and SOIC Packages
- Industry Standard Pinout
- 2s Complement, Serial Input

APPLICATIONS

- High End Compact Disc Players
- Digital Audio Amplifiers
- DAT Recorders and Players
- Synthesizers and Keyboards

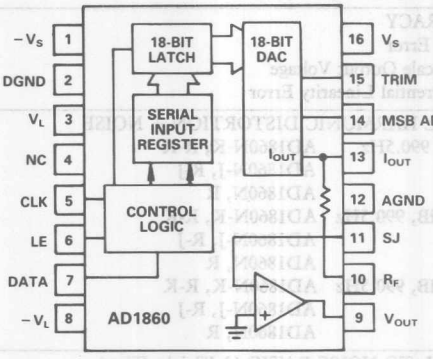
PRODUCT DESCRIPTION

The AD1860 is a monolithic 18-bit PCM Audio DAC. Each device provides a voltage output amplifier, 18-bit DAC, 18-bit serial to parallel input register and voltage reference. The digital portion of the AD1860 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1860 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. When used in current output mode, the AD1860 provides a ±1mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 12.5MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequencies.

FUNCTIONAL BLOCK DIAGRAM



The AD1860 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is 225mW typical when +5V/−12V supplies are used.

The AD1860 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC surface mount package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. 18-bit resolution provides 108dB dynamic range.
2. No external components are required.
3. Operates with ±5V to ±12V supplies.
4. 16-pin DIP or space saving SOIC package.
5. 110mW power dissipation.
6. 1.5μs settling time permits 2×, 4× and 8× oversampling.
7. ±3V or ±1mA output capability.
8. THD + Noise is 100% tested.

AD1860—SPECIFICATIONS (T_A at +25°C and ±5V supplies unless otherwise noted)

	Min	Typ	Max	Units
RESOLUTION			18	Bits
DIGITAL INPUTS V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			1.0	µA
I_{IL}, $V_{IL} = 0.4$			−10	µA
Clock Input Frequency	12.5			MHz
ACCURACY				
Gain Error		±2.0		%
Midscale Output Voltage		±30		mV
Differential Linearity Error		±0.001		% of FSR
TOTAL HARMONIC DISTORTION + NOISE				
0dB, 990.5Hz AD1860N-K, R-K		0.002	0.0025	%
AD1860N-J, R-J		0.002	0.004	%
AD1860N, R		0.004	0.008	%
−20dB, 990.5Hz AD1860N-K, R-K		0.006	0.020	%
AD1860N-J, R-J		0.010	0.020	%
AD1860N, R		0.010	0.040	%
−60dB, 990.5Hz AD1860N-K, R-K		0.9	2.0	%
AD1860N-J, R-J		0.9	2.0	%
AD1860N, R		0.9	4.0	%
SIGNAL TO NOISE RATIO (A-Weight Filter)	102	108		dB
DRIFT (0 to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.0015% of FSR)				
Voltage Output, 6V Step		1.5		µs
1LSB Step		1.0		µs
Slew Rate		9		V/µs
Current Output 1mA Step 10Ω to 100Ω Load		350		ns
1kΩ Load		350		ns
MONOTONICITY		15		Bits
OUTPUT				
Voltage Output Configuration				
Bipolar Range	±2.88	±3.0	±3.12	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage V_L and V_S	4.75		13.2	V
Voltage $-V_L$ and $-V_S$	−13.2		−4.75	V
Current +I, V_L and $V_S = 5V$, 10MHz Clock		10.0	13.0	mA
−I, $-V_L$ and $-V_S = -5V$, 10MHz Clock		12.0	−15.0	mA
Current +I, V_L and $V_S = 12V$, 10MHz Clock		10.5		mA
−I, $-V_L$ and $-V_S = -12V$, 10MHz Clock		13.5		mA
Current +I, V_L and $+V_S = +5V$, 10MHz Clock		10		mA
−I, $-V_L$ and $-V_S = -12V$, 10MHz Clock		14		mA
POWER DISSIPATION				
V_S and $V_L = \pm 5V$, 10MHz Clock		110		mW
V_S and $V_L = \pm 12V$, 10MHz Clock		288		mW
V_S and $V_L = +5V$, $-V_S$ and $-V_L = -12V$, 10MHz Clock		318		mW

	Min	Typ	Max	Units
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.

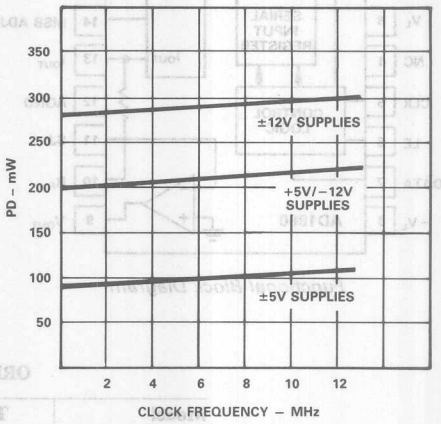
ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND . . . . . −13.2 to 0V
$-V_S$ to AGND . . . . . −13.2 to 0V
Digital Inputs to DGND . . . . . −0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

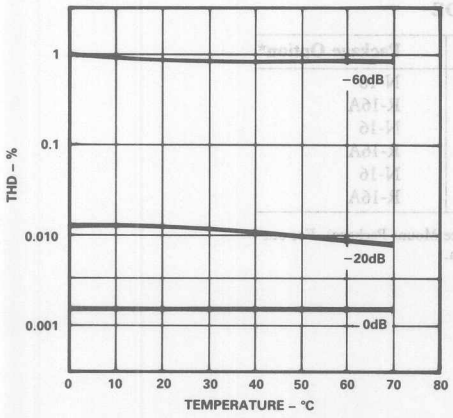
Note
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL PERFORMANCE

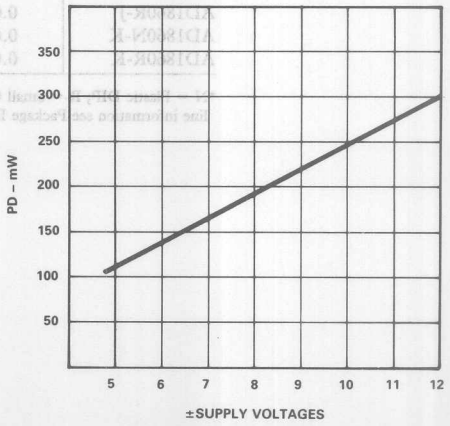
2



Power Dissipation vs. Clock Frequency



THD vs. Temperature

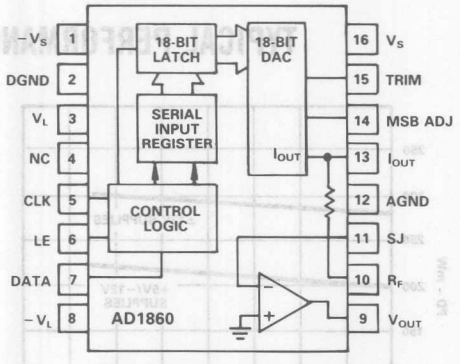


Power Dissipation vs. Supply Voltages

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.





Functional Block Diagram

PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Power Supply
2	DGND	Logic Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

ORDERING GUIDE

Model	THD @ FS	Package Option*
AD1860N	0.008%	N-16
AD1860R	0.008%	R-16A
AD1860N-J	0.004%	N-16
AD1860R-J	0.004%	R-16A
AD1860N-K	0.0025%	N-16
AD1860R-K	0.0025%	R-16A

*N = Plastic DIP; R = Small Outline IC (Surface Mount Package). For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dBs). The theoretical dynamic range of an n-bit converter is (6×n) dB. In the case of the 18-bit AD1860, that is 108dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and other errors.

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

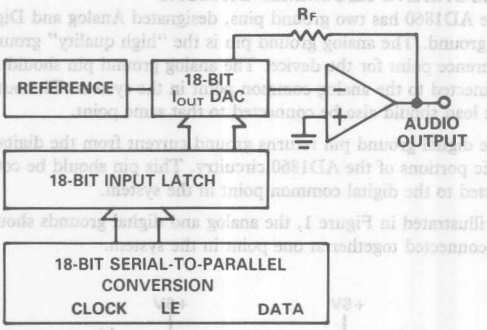
Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with a full-scale output present to the amplitude of the output when no signal is present. This is measured with a standard A-Weight filter.



AD1860 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1860 is a complete monolithic 18-bit PCM Audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, an 18-bit DAC, an 18-bit input latch and an 18-bit serial to parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on chip feedback resistor, the output op amp converts the output current of the AD1860 to a voltage output.

The 18-bit D/A converter uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The input register and serial to parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1860.

AD1860—Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1860 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1860 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

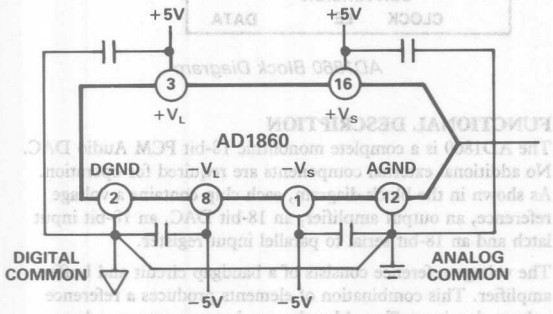


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1860 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to be operated from ±5V to ±12 V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to good performance. However, four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available.

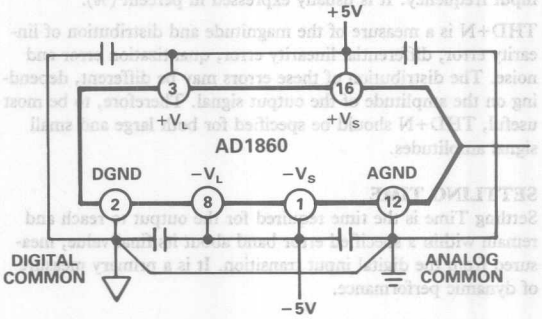


Figure 2. Typical Power Supply Sensitivity

Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1860. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with THD measurement, a THD+N specification is produced. This specification measures all undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests and grades all AD1860s on the basis of THD+N performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream representing a 0dB, −20dB or −60dB sinewave is sent to the device under test. The frequency of this waveform in 990.5 Hz.

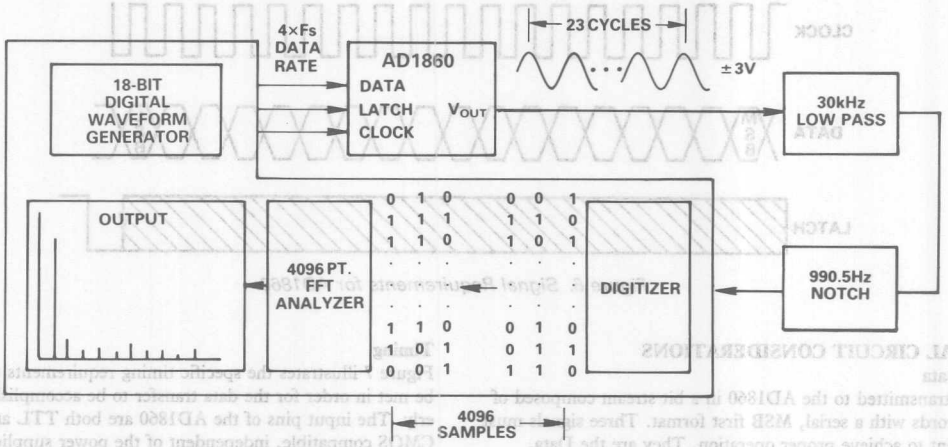


Figure 3. Block Diagram of DistortionTest Circuit

Input data is sent to the AD1860 at a $4\times F_S$ rate (176.4kHz). The AD1860 under test produces an output signal with its onboard op amp. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sinewave. A 4096 point FFT is performed on the results of the test. Based on the harmonics of the fundamental 990.5Hz test tone and the noise components, the total harmonic distortion + noise of the device is calculated. Neither a deglitcher nor an MSB trim is used during this test.

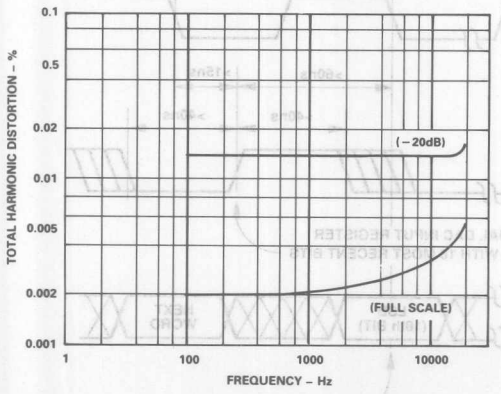


Figure 4. Typical THD vs Frequency

The circuit design, layout and manufacturing techniques employed in the production of the AD1860 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1860 for various amplitudes and frequencies of output signals. As can be seen, the AD1860 offers excellent performance, even at low amplitudes.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjust circuitry allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 5 may be used to improve performance.

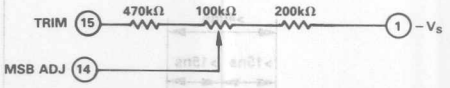


Figure 5. Optional THD Adjust Circuit

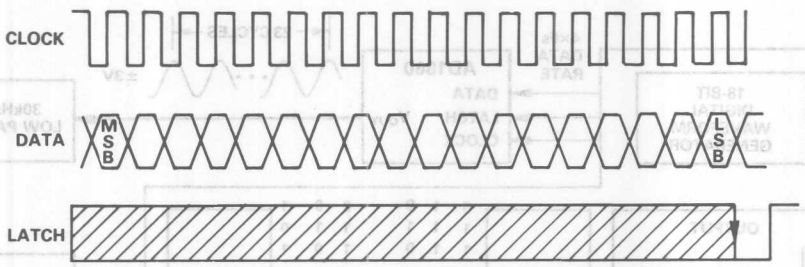


Figure 6. Signal Requirements for AD1860

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1860 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 6 illustrates the general signal requirements for data transfer for the AD1860.

Timing

Figure 7 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1860 are both TTL and 5V CMOS compatible, independent of the power supplies used. The input requirements illustrated in Figures 6 and 7 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1860 input clock can run at a 12.5MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this datasheet contains additional guides for using the AD1860 with various DSP filter chips available from Sony, NPC and Yamaha.

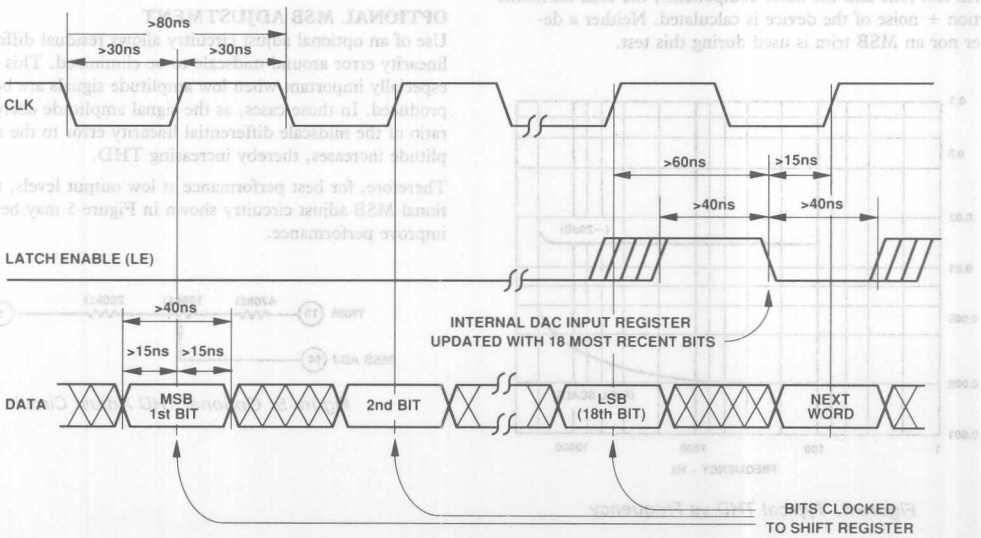


Figure 7. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1860 PCM AUDIO DAC

The AD1860 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio amplifier and DAT schemes can all use the AD1860. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

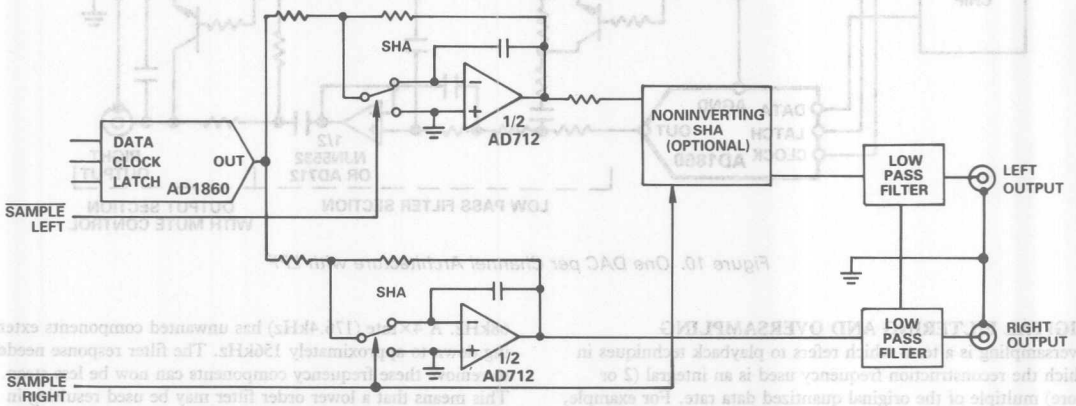


Figure 8. AD1860 in a One DAC per System Architecture

One DAC per System

Figure 8 shows a circuit using one AD1860 per system to reproduce both channels of a typical first generation stereo digital audio system. The input data is fed to the AD1860 in a format which alternates between left channel data and right channel data. The output of the AD1860 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1860. The timing diagram for the control signals for this circuit are shown in Figure 9.

However, when only two SHAs are used, the actual system performance is limited by the phase delay introduced by the demultiplexed format. This undesirable phase delay is caused by the fact that the data words presented to the inputs of the DAC represent samples taken at precisely the same point in time. But when reconstructed and demultiplexed by a single DAC, these same outputs occur at slightly different times.

By incorporating a noninverting SHA into the circuit, the phase delay can be eliminated. In Figure 8, the optional SHA ensures that the left channel output appears at the same time as the right channel output. This minor change to the circuit eliminates the artificially induced phase delay by restoring simultaneous outputs.

Following the outputs of the SHAs are low pass filters. These filters are required in any sampled data system to remove unwanted aliased components introduced by the sample and reconstruction operations.

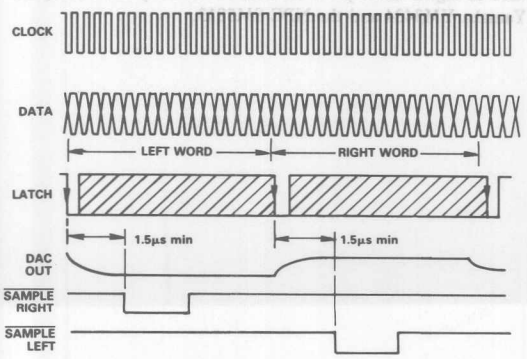


Figure 9. Control Signals for One DAC Circuit

One DAC per Channel

A second approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bitstream for each channel is transmitted and then latched into the input register of each DAC. This "second generation" approach is illustrated in Figure 10. A standard implementation of a low pass filter is shown at the output of each DAC. An optional sample/hold amplifier could be connected between the DACs and the LPFs to deglitch the outputs. This is not required, however, to achieve the specified performance.

Two DACs per Channel

Another architecture uses two DACs per channel. In this scheme each DAC reproduces one half of the output waveform. The advantage obtained with this structure is that midscale differential linearity error no longer affects the zero crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses 1/2 ± 1/4 full scale. The result is that THD performance for low amplitude signals is greatly improved.

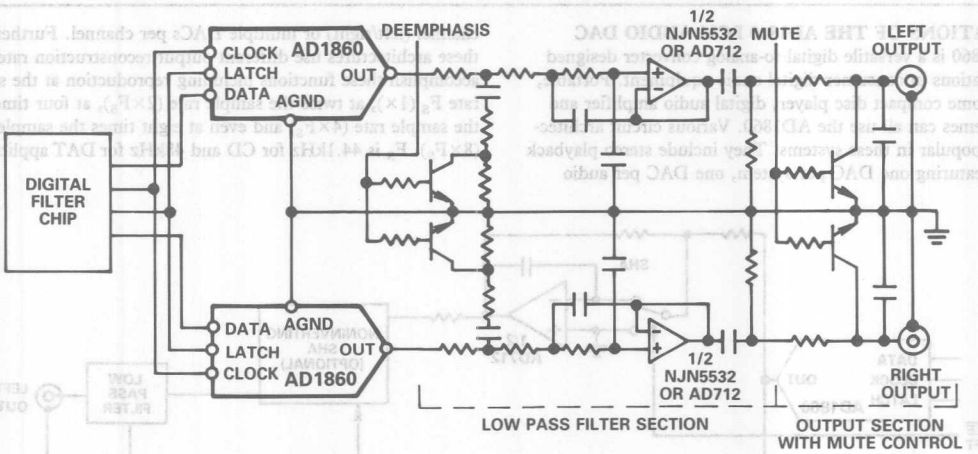


Figure 10. One DAC per Channel Architecture with LPF

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4×F_S, yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low pass filters which follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency. When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often used low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2×reconstruction frequency (88.2kHz) is used, the lowest frequency components now extend down to approximately 68kHz. A 4×rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles, as shown in Figure 10, are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require the serial input data stream to run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip (DSP) which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters".

The AD1860 is compatible with popular digital filter chips used in digital audio products such as the Sony CXD1088, the Yamaha YM3434 and the NPC SM5813.

Figure 11 illustrates the combination of a second generation digital filter chip, the Sony CXD1088, and the AD1860 audio DAC. The digital filter chip provides 18-bit data words to the DACs at $4\times F_S$. Very high performance can be achieved.

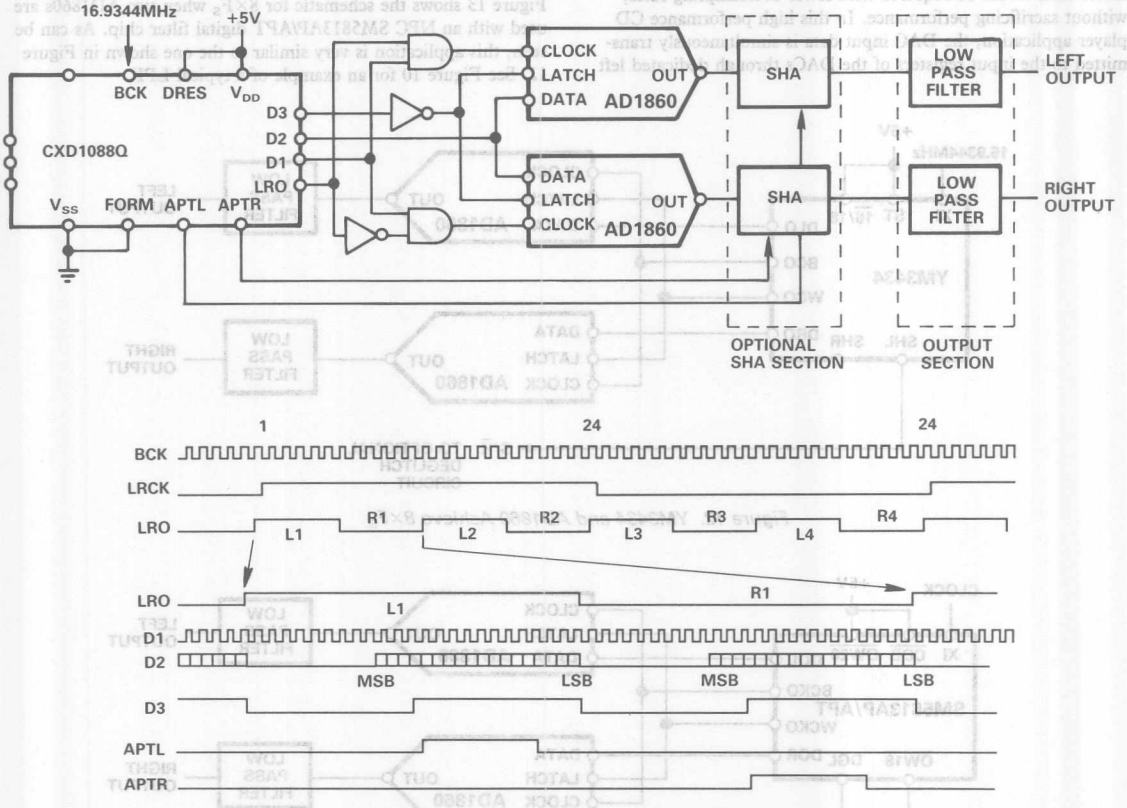


Figure 11. $4\times F_S$ with the CXD1088Q

tal filter chip and two AD1860 audio DACs. This combination of components results in $8\times F_S$ oversampling reconstruction rates. This rate allows the use of lower order output low pass filters than would be required with lower oversampling rates, without sacrificing performance. In this high performance CD player application, the DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left tation does not require any external components to achieve the full 108dB dynamic range afforded by the 18-bit AD1860 audio DAC. As before, optional sample/hold signals are provided.

Figure 13 shows the schematic for $8\times F_S$ when two AD1860s are used with an NPC SM5813AP/APT digital filter chip. As can be seen, this application is very similar to the one shown in Figure 12. See Figure 10 for an example of a typical LPF.

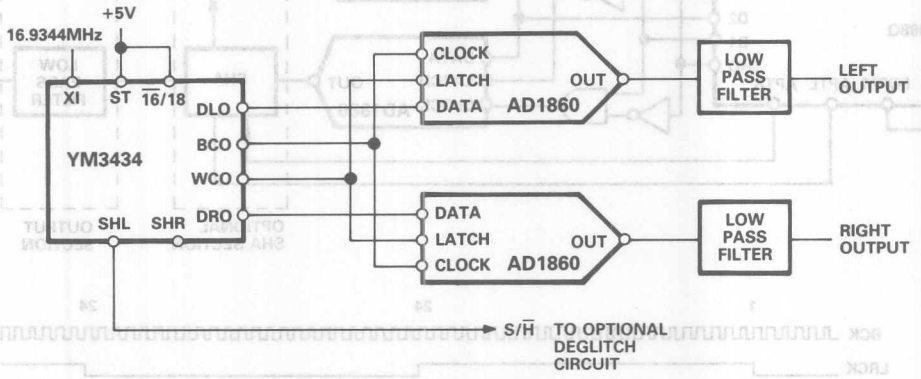


Figure 12. YM3434 and AD1860 Achieve $8\times F_S$

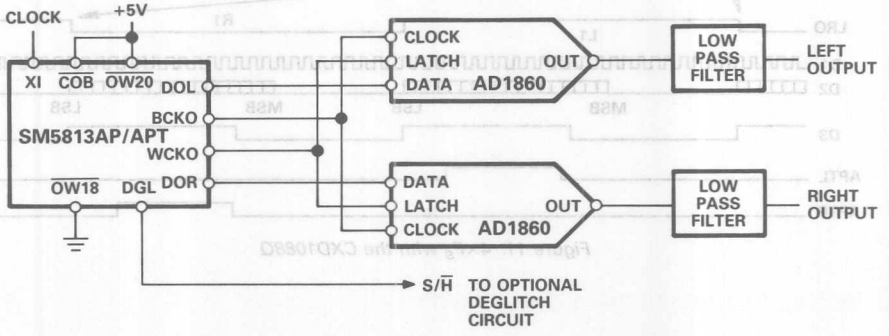


Figure 13. SM5813AP/APT and AD1860 Achieve $8\times F_S$

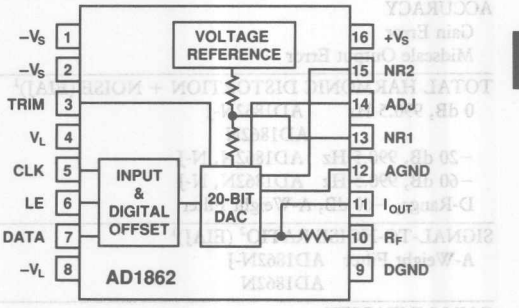
Ultralow Noise 20-Bit Audio DAC

AD1862*

FEATURES
- 119 dB Signal-to-Noise Ratio
- 102 dB D-Range Performance
- ±1 dB Gain Linearity
- ±1 mA Output Current
- 16-Pin DIP Package
- 0.0012% THD + N

APPLICATIONS
- High-Performance Compact Disc Players
- Digital Audio Amplifiers
- Synthesizer Keyboards
- Digital Mixing Consoles
- High-Resolution Signal Processing

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1862 is a monolithic 20-bit digital audio DAC. Each device provides a 20-bit DAC, 20-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1862 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1862 is fabricated with bipolar and MOS devices as well as thin-film resistors.

New design, layout and packaging techniques all combine to produce extremely high-performance audio playback. The design of the AD1862 incorporates a digital offset circuit which improves low-level distortion performance. Low-stress packaging techniques are used to minimize stress-induced parametric shifts. Stress-sensitive circuit elements are located in die areas which are least affected by packaging stress. Laser-trimming of initial linearity error affords extremely low total harmonic distortion. Output glitch is also small, contributing to the overall high level of performance.

The noise performance of the AD1862 is excellent. When used with the recommended two external noise-reduction capacitors, it achieves 119 dB signal-to-noise ratio.

The serial input port consists of the clock, data and latch enable pins. A serial 20-bit, 2s complement data word is clocked into the DAC, MSB first, by the external data clock. A latch-enable signal transfers the input word from the internal serial input register to the DAC input register. The data clock can function at 17 MHz, allowing 16 × F_S operation. The serial input port is compatible with second-generation digital filter chips for consumer audio products such as the NPC SM5813 and SM5818.

The AD1862 operates with ±5 V to ±12 V supplies for the digital power supplies and ±12 V supplies for the analog supplies. The digital and analog supplies can be separated for reduced digital crosstalk. Separate analog and digital common pins are also provided. The AD1862 typically dissipates less than 300 mW.

The AD1862 is packaged in a 16-pin plastic DIP. The operating range is guaranteed to be −25°C to +70°C.

PRODUCT HIGHLIGHTS

1. 119 dB signal-to-noise ratio (typical)
2. 102 dB D-Range performance (minimum)
3. ±1 dB gain linearity @ −90 dB amplitude
4. 20-bit resolution provides 120 dB of dynamic range
5. 16×F_S operation
6. 0.0012% THD+N @ 0 dB signal amplitude (typical)
7. Space saving 16-pin DIP package
8. ±1 mA output current

*Protected by U.S. Patents Numbers: 4,349,811; 4,857,862; 4,855,618; 3,961,326; 4,141,004; 4,902,959.

AD1862—SPECIFICATIONS (T_A at +25°C and ±12 V supplies, see Figure 10 for test circuit schematic)

	Min	Typ	Max	Units
RESOLUTION	20			Bits
DIGITAL INPUTS V_{IH}	2.0	**4.0**		V
V_{IL}		**0.4**	0.8	V
I_{IH} @ V_{IH} = 4.0 V			**1.0**	μA
I_{IL} @ V_{IL} = 0.4 V			**−10**	μA
Maximum Clock Input Frequency	**17**			MHz
ACCURACY				
Gain Error			**±2**	%
Midscale Output Error		±2	**±5**	μA
TOTAL HARMONIC DISTORTION + NOISE (EIAJ)[1]				
0 dB, 990.5 Hz AD1862N-J		−98 (0.0012)	**−96 (0.0016)**	dB (%)
AD1862N		−94 (0.0019)	**−92 (0.0025)**	dB (%)
−20 dB, 990.5 Hz AD1862N, N-J		−84 (0.0063)	**−80 (0.01)**	dB (%)
−60 dB, 990.5 Hz AD1862N, N-J		−45 (0.56)	**−42 (0.8)**	dB (%)
D-Range, −60 dB, A-Weight Filter	**102**			dB
SIGNAL-TO-NOISE RATIO[2] (EIAJ)[1]				
A-Weight Filter AD1862N-J	**113**	119		dB
AD1862N	**110**	119		dB
GAIN LINEARITY				
@ −90 dB AD1862N-J		±1		dB
AD1862N		±1		dB
OUTPUT CURRENT				
Bipolar Range		±1		mA
Tolerance		±1	**±2**	%
Output Impedance (±30%)		2.1		kΩ
Settling Time		350		ns
FEEDBACK RESISTOR				
Value		3		kΩ
Tolerance		±1	**±2**	%
POWER SUPPLY				
Voltage V_L and $-V_L$	4.75	**12.0**	13.2	±V
Voltage V_S and $-V_S$	10.8	**12.0**	13.2	±V
Current +I, V_L and V_S = 12 V, 17 MHz Clock		11	**15**	mA
−I, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		13	**16**	mA
POWER DISSIPATION				
V_L and V_S = 12 V, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		288	372	mW
TEMPERATURE RANGE				
Specification		**+25**		°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTE

[1]Test Method complies with EIAJ Standard CP-307.

[2]The signal-to-noise measurement includes noise contributed by the SE5534A op amp used in the test fixture but does not include the noise contributed by the low pass filter used in the test fixture.

Specifications in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

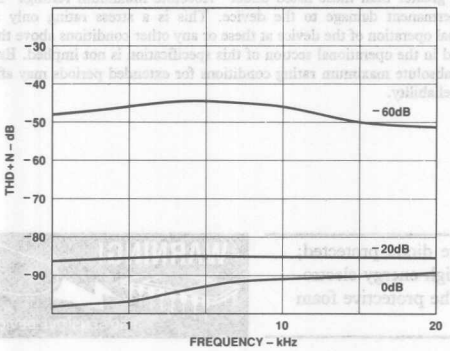


Figure 1. THD+N vs. Frequency

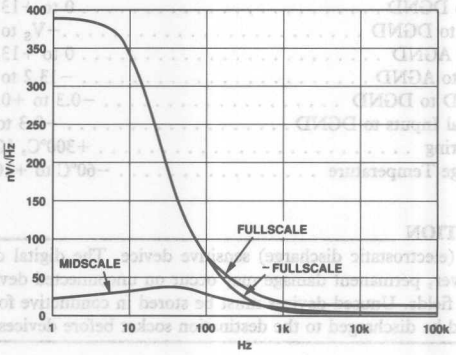


Figure 2. Noise Density

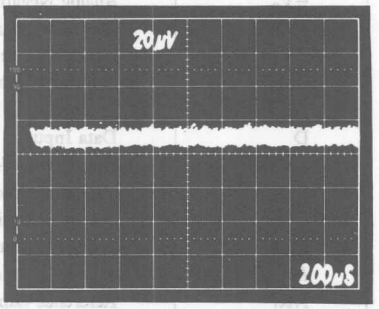


Figure 3. Broadband Noise (20 kHz Bandwidth, Midscale)

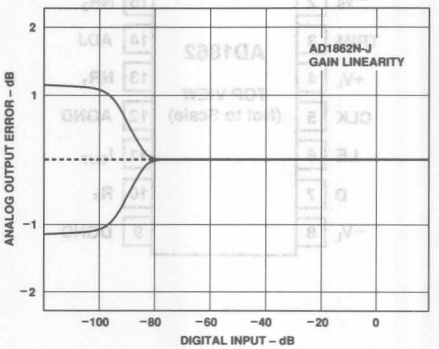


Figure 4. Gain Linearity

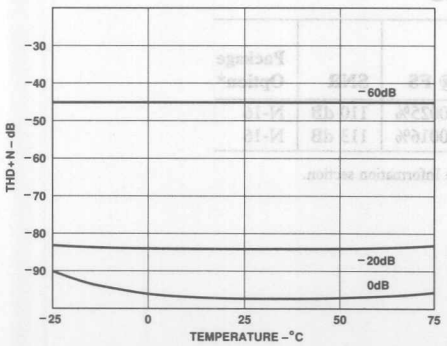


Figure 5. THD+N vs. Temperature (1 kHz)

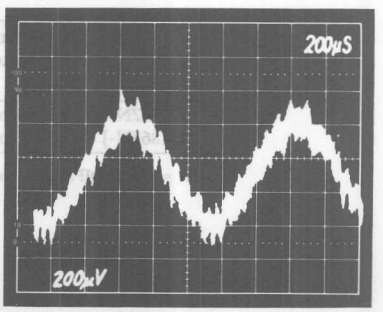


Figure 6. Midscale Differential Linearity

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND	0 to +13.2 V
$-V_L$ to DGND	$-V_S$ to 0 V
V_S to AGND	0 to +13.2 V
$-V_S$ to AGND	−13.2 to 0 V
AGND to DGND	−0.3 to +0.3 V
Digital Inputs to DGND	−0.3 to V_L
Soldering	+300°C, 10 sec
Storage Temperature	−60°C to +100°C

NOTE

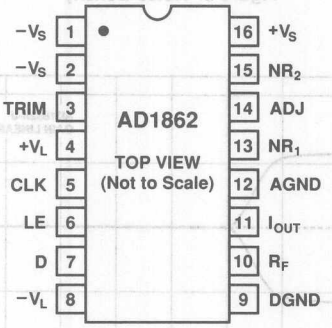
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATION



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Bias Capacitor
2	$-V_S$	Analog Negative Supply
3	TRIM	Trim Pot Connection
4	$+V_L$	Positive Logic Supply
5	CLK	External Clock Input
6	LE	Latch Enable Input
7	D	Data Input
8	$-V_L$	Negative Logic Supply
9	DGND	Digital Ground
10	R_F	Feedback Resistor
11	I_{OUT}	Output Current
12	AGND	Analog Ground
13	NR_1	Reference Capacitor
14	ADJ	Midscale Adjust
15	NR_2	Bias Capacitor
16	$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	Operating Temperature Range	THD+N @ FS	SNR	Package Option*
AD1862N	−25°C to +70°C	−92 dB, 0.0025%	110 dB	N-16
AD1862N-J	−25°C to +70°C	−96 dB, 0.0016%	113 dB	N-16

*N = Plastic DIP. For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-RANGE DISTORTION

D-Range Distortion is the ratio of the signal amplitude to the distortion plus noise at −60 dB. In this case, an A-Weight filter is used. The value specified for D-Range performance is the ratio measured plus 60 dB.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within ±1/2 LSB about its final value, measured from the digital input transition. It is a primary measure of dynamic performance and is usually expressed in nanoseconds (ns).

SIGNAL-TO-NOISE RATIO

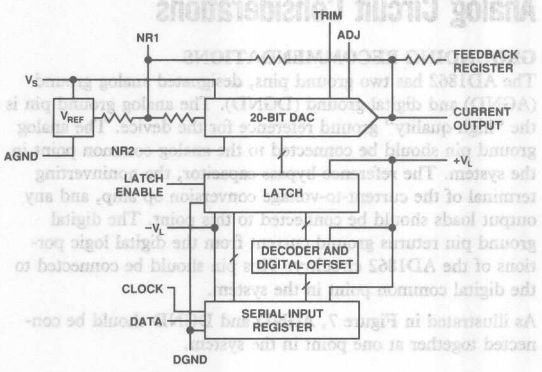
The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with full-scale present to the amplitude of the output when no signal is present. It is expressed in decibels (dB) and measured using an A-Weight filter.

GAIN LINEARITY

Gain Linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a low level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output when the 2s complement input code representing midscale is loaded in the input register. The AD1862 is a current output D/A converter. Therefore, this error is expressed in μA.



AD1862 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1862 is a high performance, monolithic 20-bit audio DAC. Each device includes a voltage reference, a 20-bit DAC, 20-bit input latch and a 20-bit serial-to-parallel input register. A special digital offset circuit, combined with segmentation circuitry, produces excellent THD+N and D-range performance.

Extensive noise-reduction features are utilized to make the noise performance of the AD1862 as high as possible. For example, the voltage reference circuit is a low-noise, 9 volt bandgap cell. This cell supplies the reference voltage to the bipolar offset circuit and the DAC. An external noise-reduction capacitor is connected to NR1 to form a low-pass filter network.

Additional noise-reduction techniques are used in the control amplifier of the DAC. By connecting an external noise-reduction capacitor to NR2 output noise contributions from the control portion of the DAC are similarly reduced. The noise-reduction efforts result in a signal-to-noise ratio of 119 dB.

The design of the AD1862 uses a combination of segmented decoder, R-2R topology and digital offset to produce low distortion at all signal amplitudes. The digital offset technique shifts the midscale output voltage (0 V) away from the MSB transition of the device. Therefore, small amplitude signals are not affected by an MSB change. An extra DAC cell is included to avoid clipping the output at full scale.

The DAC supplies a ±1 mA output current to an external I-to-V converter. An on-board 3 kΩ feedback resistor is also supplied. Both the output current and feedback resistor are laser-trimmed to ±2% tolerance, simplifying the selection of external filter and/or deemphasis network components. The input register and serial-to-parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. Internal TTL-to-CMOS converters are used to insure TTL and 5 V CMOS compatibility.

GROUNDING RECOMMENDATIONS

The AD1862 has two ground pins, designated analog ground (AGND) and digital ground (DGND). The analog ground pin is the "high-quality" ground reference for the device. The analog ground pin should be connected to the analog common point in the system. The reference bypass capacitor, the noninverting terminal of the current-to-voltage conversion op amp, and any output loads should be connected to this point. The digital ground pin returns ground current from the digital logic portions of the AD1862 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 7, AGND and DGND should be connected together at one point in the system.

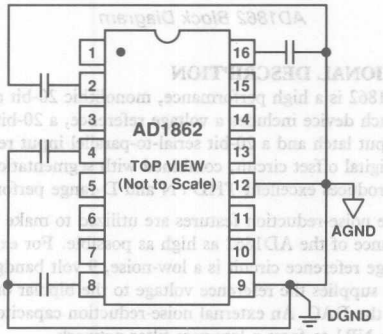


Figure 7. Grounding and Bypassing Recommendations

POWER SUPPLIES AND DECOUPLING

The AD1862 has four power supply input pins. $\pm V_S$ provide the supply voltages which operate the linear portions of the DAC including the voltage reference and control amplifier. The $\pm V_S$ supplies are designed to operate with ±12 volts.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register, the input latching circuitry and the TTL-to-CMOS level shifters. The $\pm V_L$ supplies are designed to be operated from ±5 V to ±12 V supplies subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply input pins. Good engineering practice suggests that these capacitors be placed as close as possible to the package pins and the common points. The logic supplies, $\pm V_L$, should be decoupled to DGND and the analog supplies, $\pm V_S$, should be decoupled to AGND.

EXTERNAL NOISE REDUCTION COMPONENTS

Two external capacitors are required to achieve low-noise operation. Their correct connection is illustrated in Figure 8. Capacitor C1 is connected between the pin labeled NR1 and analog common. C1 forms a low-pass filter element which reduces noise contributed by the voltage reference circuitry. The proper choice for this capacitor is a tantalum type with value of 10 μF or more. This capacitor should be connected to the package pins as closely as possible. This will minimize the effects of parasitic inductance of the leads and connections circuit connections.

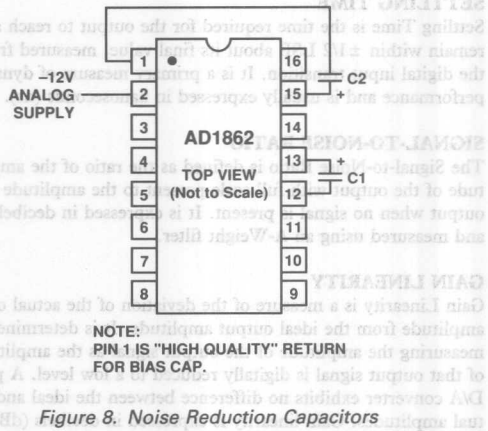


Figure 8. Noise Reduction Capacitors

Capacitor C2 is connected between the pin labeled NR2 and the negative analog supply, $-V_S$. This capacitor reduces the portion of output noise contributed by the control amplifier circuitry. C2 should be chosen to be a tantalum capacitor with a value of about 1 μF. Again, the connections between the AD1862 and C2 should be made as short as possible.

The recommended values for C1 and C2 are 10 μF and 1 μF, respectively. The ratio between C1 and C2 should be approximately 10. Additional noise reduction can be gained by choosing slightly higher values for C1 and C2 such as 22 μF and 2.2 μF. Figure 2 illustrates the noise performance of the AD1862 with 10 μF and 1 μF.

EXTERNAL AMPLIFIER CONNECTIONS

The AD1862 is a current-output D/A converter. Therefore, an external amplifier, in combination with the on-board feedback resistor, is required to derive an output voltage. Figure 9 illustrates the proper connections for an external operational amplifier. The output of the AD1862 is intended to drive the summing junction of an external current-to-voltage conversion op amp. Therefore, the voltage on the output current pin of the AD1862 should be approximately the same as that on the AGND pin of the device.

The on-board 3 kΩ feedback resistor and the ±1 mA output current typically have ±1% tolerance or less. This makes the choice of external components very simple and eliminates additional trimming. For example, if a user wishes to derive an output voltage higher than the ±3 V swing offered by the output current and feedback resistor combination, all that is required is to combine a standard value resistor with the feedback resistor to achieve the appropriate output voltage swing. This technique can be extended to include the choice of elements in the deemphasis network, etc.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with the THD measurement, a THD+N specification is realized. This specification indicates all of the undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests all AD1862s on the basis of THD+N performance. In this test procedure, a digital data stream representing a 0 dB, −20 dB or −60 dB sine wave is sent to the device under test. The frequency of the waveform is 990.5 Hz. Input data is sent to the AD1862 at an 8 × F_S rate (352.8 kHz). The AD1862 under test produces an output current which is converted to an output voltage by an external amplifier. Figure 10 illustrates the recommended test circuit. Deglitchers and trims are not used during this test procedure. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096 point FFT is performed on the test data.

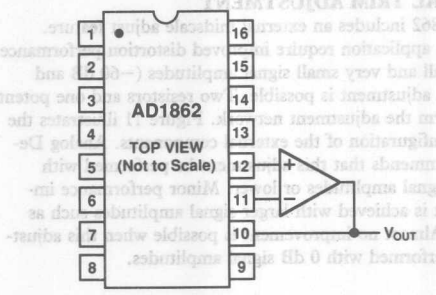


Figure 9. External Amplifier Connections

Based upon the harmonics of the fundamental 990.5 Hz test tone, and the noise components in the audio band, the total harmonic distortion + noise of the device is calculated. The AD1862 is available in two performance grades. The AD1862N produces a maximum of 0.0025% THD+N at 0 dB signal levels. The higher performance AD1862N-J produces a maximum of 0.0016% THD+N at 0 dB signal levels.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio (SNR) of the AD1862 is tested in the following manner. The amplitude of a 0 dB signal is measured. The device under test is then set to midscale output voltage (0 volts). The amplitude of all noise present to 30 kHz is measured. The SNR is the ratio of these two measurements. The SNR figure for the AD1862 includes the output noise contributed by the NE5534 op amp used in the test fixture but does not include the noise contributed by the low-pass filter used in the test fixture.

The AD1862N has a minimum SNR of 110 dB. The higher performance AD1862N-J has a minimum SNR of 113 dB.

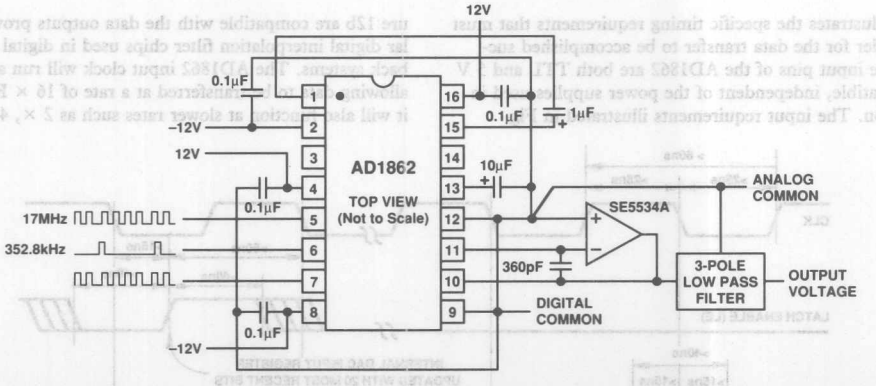


Figure 10. Recommended Test Circuit

OPTIONAL TRIM ADJUSTMENT

The AD1862 includes an external midscale adjust feature. Should an application require improved distortion performance under small and very small signal amplitudes (−60 dB and lower), an adjustment is possible. Two resistors and one potentiometer form the adjustment network. Figure 11 illustrates the correct configuration of the external components. Analog Devices recommends that this adjustment be performed with −60 dB signal amplitudes or lower. Minor performance improvement is achieved with larger signal amplitudes such as −20 dB. Almost no improvement is possible when this adjustment is performed with 0 dB signal amplitudes.

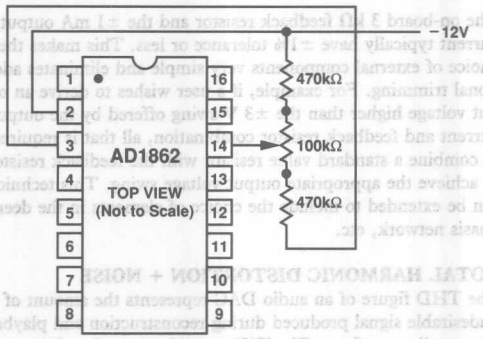


Figure 11. External Midscale Adjust

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

Data is transmitted to the AD1862 in a bit stream composed of 20-bit words with a serial, 2s complement, MSB first format. Three signals must be present to achieve proper operation. They are the data, clock and latch enable signals. Input data bits are clocked into the input register on the rising edge of the clock signal (CLK). The LSB is clocked in on the 20th clock pulse. When all data bits are loaded, a low going latch enable (LE) pulse updates the DAC input. Figure 12a illustrates the general signal requirements for data transfer for the AD1862.

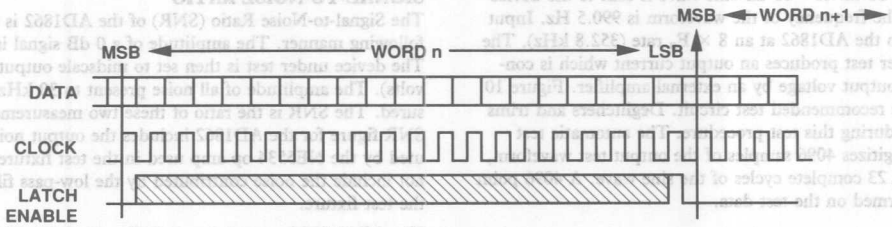


Figure 12a. Input Data

TIMING

Figure 12b illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished successfully. The input pins of the AD1862 are both TTL and 5 V CMOS compatible, independent of the power supplies used in the application. The input requirements illustrated in Figure 12b are compatible with the data outputs provided by popular digital interpolation filter chips used in digital audio playback systems. The AD1862 input clock will run at 17 MHz allowing data to be transferred at a rate of 16 × F_S. Of course, it will also function at slower rates such as 2 ×, 4 × or 8 × F_S.

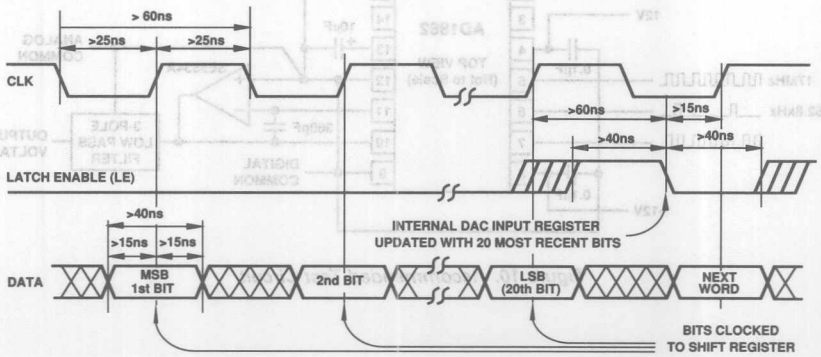


Figure 12b. Timing Requirements

The AD1862 is an extremely high performance DAC designed for high-end consumer and professional digital audio applications. Compact disc players, digital preamplifiers, digital musical instruments and sound processors benefit from the extended dynamic range, low THD+Noise and high signal-to-noise ratio. For the first time, the D/A converter is no longer the basic limitation in the performance of a CD player.

The performance of professional audio gear, such as mixing consoles, digital tape recorders and multivoice synthesizers can utilize the wide dynamic range and signal-to-noise ratio to achieve greater performance. And, the AD1862's space saving 16-pin package contributes to compact system design. This permits a system designer to incorporate more voices in multivoice synthesizers, more tracks in multitrack tape recorders and more channels in multichannel mixing consoles.

Furthermore, high-resolution signal processing and waveform generation applications are equally well served by the AD1862.

HIGH PERFORMANCE CD PLAYER

Figure 13 illustrates the application of AD1862s in a high performance CD player. Two AD1862s are used, one for the left channel and one for the right channel. The CXD11XX chip decodes the digital data coming from the read electronics and sends it to the SM5813. Input data is sent to each AD1862 by the SM5813 digital interpolating filter. This device operates at 8 times oversampling. The NE5534 op amps are chosen for current-to-voltage converters due to their low distortion and low noise. The output filters are 5-pole designs. For the purpose of clarity, all bypass capacitors have been omitted from the schematic.

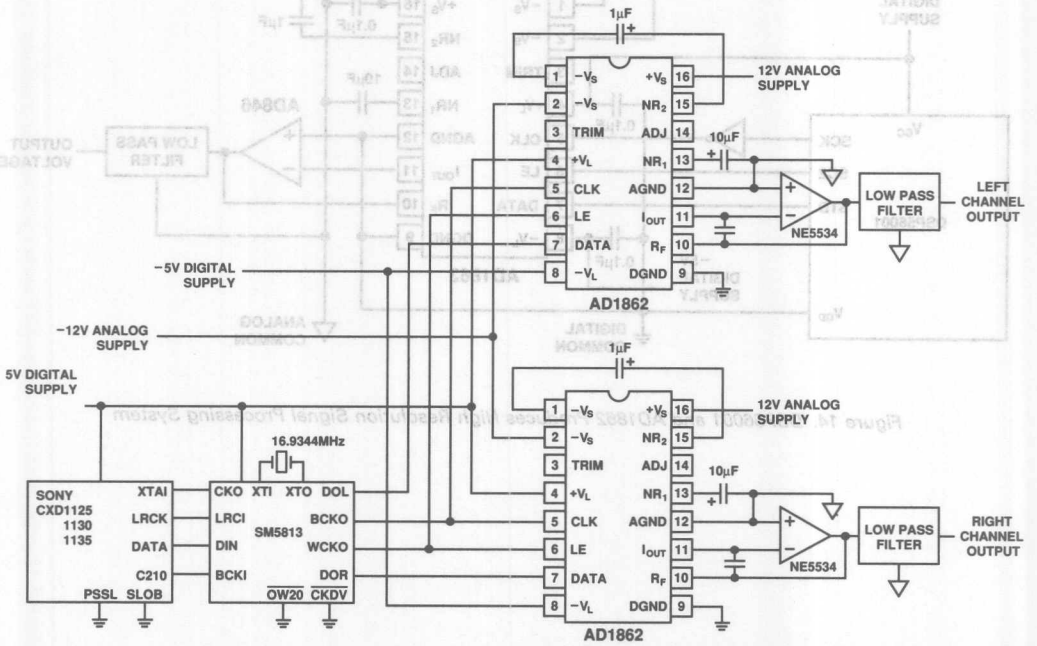


Figure 13. High Performance 20-Bit 8 × Oversampling CD Player Application

Figure 14 illustrates the AD1862 combined with the DSP56000. In high-resolution applications, the combination of the 24-bit architecture of the DSP56000 and the low noise and high resolution of the AD1862 can produce a high-resolution, low-noise system.

As shown in Figure 14, the clock signal supplied by the DSP processor must be inverted to be compatible with the input of the AD1862. The exact architecture of the output low-pass filter

higher the oversampling rate, the fewer number of filter poles are required to prevent aliasing.

The 20-bit resolution is particularly suitable for professional audio, mixing or equalization equipment. Its resolution allows 24 dB of equalization to be performed on 16-bit input words without signal truncation. Furthermore, up to sixteen 16-bit input words can be mixed and output directly to the AD1862. In this case, no loss of signal information would be encountered.

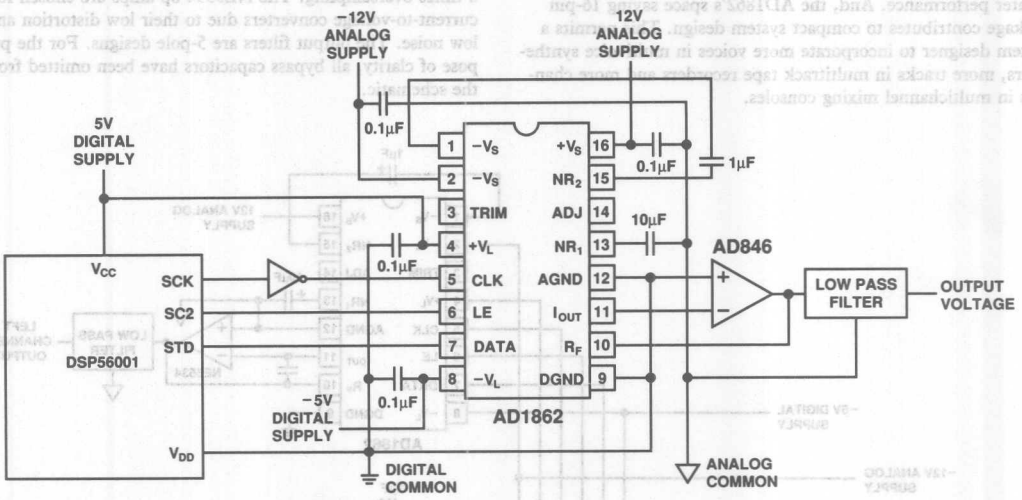


Figure 14. DSP56001 and AD1862 Produces High Resolution Signal Processing System

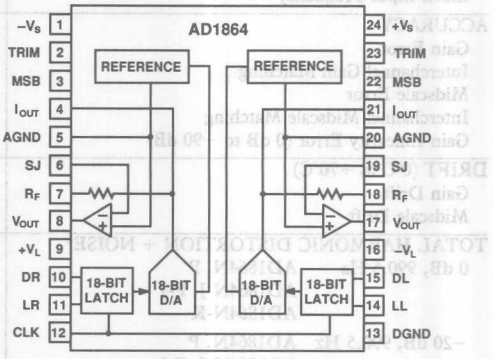
Complete Dual 18-Bit Audio DAC

AD1864*

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
Operates at 8 × Oversampling per Channel
±5 Volt to ±12 Volt Operation
Cophased Outputs
115 dB Channel Separation
±0.3% Interchannel Gain Matching
0.0017% THD+N

APPLICATIONS
Multichannel Audio Applications:
Compact Disc Players
Multi-Voice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

AD1864 DIP BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1864 is a complete dual 18-bit DAC offering excellent THD+N, while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1864 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices BiMOS II process.

The DACs on the AD1864 chip employ a partially-segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser-trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1864 provides two cophased ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1864 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout techniques. At the same time, both channels of the AD1864 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

A versatile digital interface allows the AD1864 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1864 operates from ±5 V to ±12 V power supplies. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1864 typically dissipates only 225 mW, with a maximum power dissipation of 265 mW.

The AD1864 is packaged in both a 24-pin plastic DIP and a 28-pin PLCC. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±13.2 V.

PRODUCT HIGHLIGHTS

1. The AD1864 is a complete dual 18-bit audio DAC.
2. 108 dB signal-to-noise ratio for low noise operation.
3. THD+N is typically 0.0017%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 8 × F_S.
8. Low Power — only 225 mW typ, 265 mW max.
9. 5-wire interface for individual DAC control.

*Covered by U.S. Patents Nos: RE 30,586; 3,961,326; 4,141,004; 4,349,811; 4,855,618; 4,857,862

AD1864—SPECIFICATIONS (T_A = +25°C, $\pm V_L = \pm V_S = \pm 5$ V, F_S = 352.8 kHz, without MSB adjustment)

		Min	Typ	Max	Units
RESOLUTION			18		Bits
DIGITAL INPUTS					
V_{IH}		2.0		$+V_L$	V
V_{IL}				0.8	V
I_{IH}, $V_{IH} = +V_L$				1.0	μA
I_{IL}, V_{IL} = 0.4 V				−10	μA
Clock Input Frequency		12.7			MHz
ACCURACY					
Gain Error			0.4	1.0	% of FSR
Interchannel Gain Matching			0.3	0.8	% of FSR
Midscale Error			4		mV
Interchannel Midscale Matching			5		mV
Gain Linearity Error (0 dB to −90 dB)			<2		dB
DRIFT (0°C to +70°C)					
Gain Drift			±25		ppm of FSR/°C
Midscale Drift			±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*					
0 dB, 990.5 Hz	AD1864N, P		0.004	0.006	%
	AD1864N-J, P-J		0.003	0.004	%
	AD1864N-K		0.0017	0.0025	%
−20 dB, 990.5 Hz	AD1864N, P		0.010	0.040	%
	AD1864N-J, P-J		0.010	0.020	%
	AD1864N-K		0.010	0.020	%
−60 dB, 990.5 Hz	AD1864N, P		1.0	4.0	%
	AD1864N-J, P-J		1.0	2.0	%
	AD1864N-K		1.0	2.0	%
CHANNEL SEPARATION*					
0 dB, 990.5 Hz		110	115		dB
SIGNAL-TO-NOISE RATIO*					
(20 Hz to 30 kHz)	N, N-J, N-K	102	108		dB
	P, P-J	95	108		
D-RANGE* (WITH A-WEIGHT FILTER)					
−60 dB, 990.5 Hz	AD1864N, P	88	100		dB
	AD1864N-J, P-J	94	100		dB
	AD1864N-K	94	100		dB
OUTPUT					
Voltage Output Configuration					
Output Range (±3%)		±2.88	±3.0	±3.12	V
Output Impedance			0.1		Ω
Load Current		±8			mA
Short-Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Output Range (±30%)			±1		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
$+V_L$ and $+V_S$		4.75	5.0	13.2	V
$-V_L$ and $-V_S$		−13.2	−5.0	−4.75	V
+I, ($+V_L$ and $+V_S$ = +5 V)			22	25	mA
−I, ($-V_L$ and $-V_S$ = −5 V)			−23	−28	mA
POWER DISSIPATION, $\pm V_L = \pm V_S = \pm 5$ V			225	265	mW
TEMPERATURE RANGE					
Specification		0	+25	+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C
WARMUP TIME		1			min

NOTE

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.

*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.

Specifications subject to change without notice.

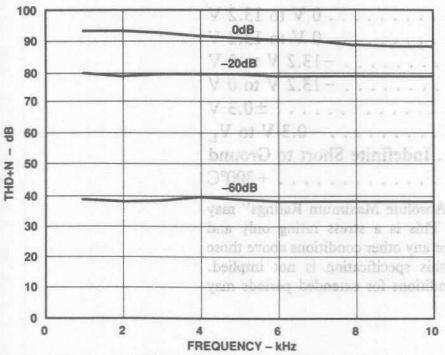


Figure 1. THD+N vs. Frequency

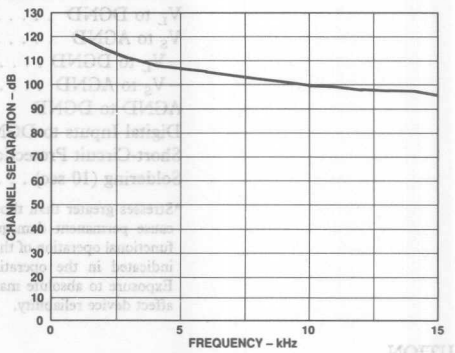


Figure 2. Channel Separation vs. Frequency

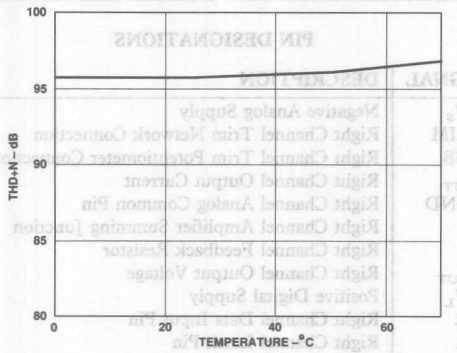


Figure 3. THD+N vs. Temperature

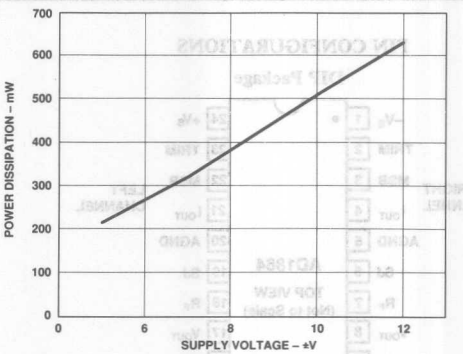


Figure 4. Power Dissipation vs. Supply Voltage

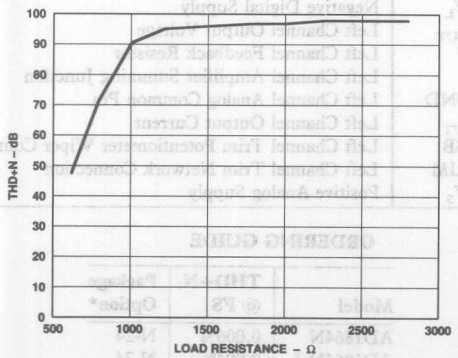


Figure 5. THD+N vs. Load Resistance

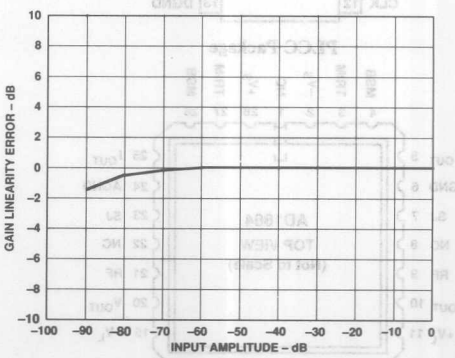


Figure 6. Gain Linearity Error vs. Input Amplitude

$-V_L$ to DGND	−13.2 V to 0 V
$-V_S$ to AGND	−13.2 V to 0 V
AGND to DGND	±0.3 V
Digital Inputs to DGND	−0.3 V to V_L
Short-Circuit Protection	Indefinite Short to Ground
Soldering (10 sec)	+300°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

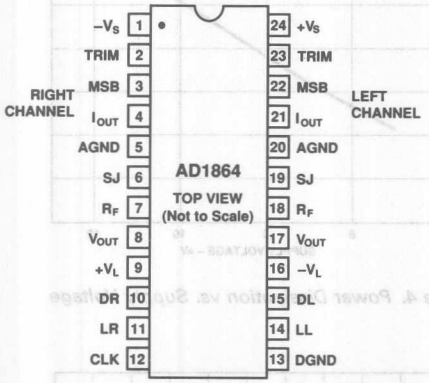
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

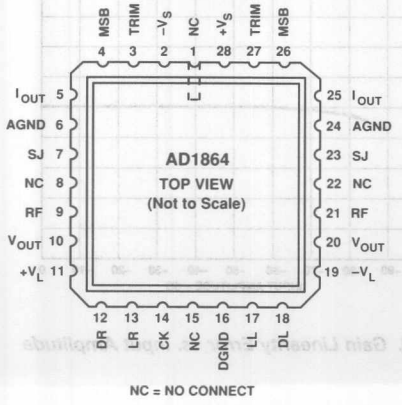


PIN CONFIGURATIONS

DIP Package



PLCC Package



NC = NO CONNECT

PIN DESIGNATIONS

SIGNAL	DESCRIPTION
$-V_S$	Negative Analog Supply
TRIM	Right Channel Trim Network Connection
MSB	Right Channel Trim Potentiometer Connection
I_{OUT}	Right Channel Output Current
AGND	Right Channel Analog Common Pin
SJ	Right Channel Amplifier Summing Junction
R_F	Right Channel Feedback Resistor
V_{OUT}	Right Channel Output Voltage
$+V_L$	Positive Digital Supply
DR	Right Channel Data Input Pin
LR	Right Channel Latch Pin
CLK	Clock Input Pin
DGND	Digital Common Pin
LL	Left Channel Latch Pin
DL	Left Channel Data Input Pin
$-V_L$	Negative Digital Supply
V_{OUT}	Left Channel Output Voltage
RF	Left Channel Feedback Resistor
SJ	Left Channel Amplifier Summing Junction
AGND	Left Channel Analog Common Pin
I_{OUT}	Left Channel Output Current
MSB	Left Channel Trim Potentiometer Wiper Connection
TRIM	Left Channel Trim Network Connection
$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	THD+N @ FS	Package Option*
AD1864N	0.006%	N-24
AD1864N-J	0.004%	N-24
AD1864N-K	0.0025%	N-24
AD1864P	0.006%	P-28A
AD1864P-J	0.004%	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (−20 dB, −60 dB) signal amplitudes. THD+N measurements for the AD1864 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output when cide midscale is entered to the amplitude of the output when a cide full scale is entered. It is measured using a standard A-Weight filter. SNR for the AD1864 is measured for noise components up to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1864 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of 60 dB below full-scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

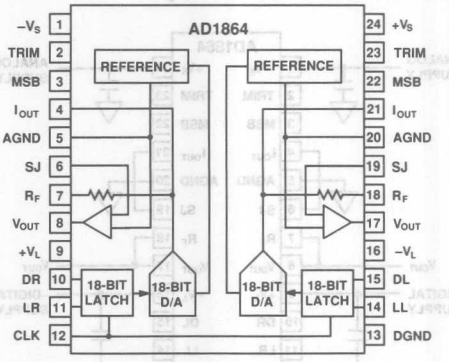
The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1864) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the 2s complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the 2s complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.



AD1864 DIP Block Diagram

FUNCTIONAL DESCRIPTION

The AD1864 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and time.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1864.

GROUNDING RECOMMENDATIONS

The AD1864 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 7, the AGND pins should *not* be connected at the chip.

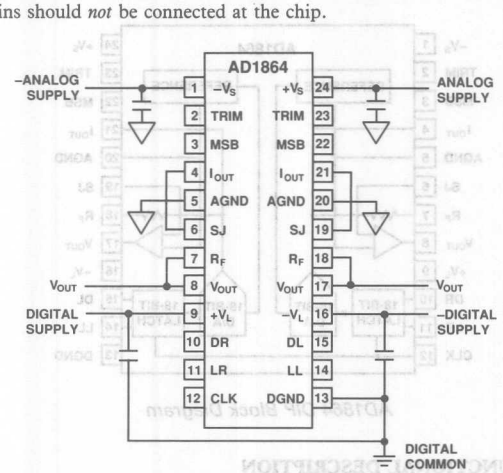


Figure 7. Recommended DIP Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1864 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1864 has four power supply pins. $\pm V_S$ provide the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ± 5 V to ± 12 V. These supplies should be decoupled to analog common using 0.1 μF capacitors. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift registers and the input latching circuitry. These supplies should be bypassed to digital common using 0.1 μF capacitors. $\pm V_L$ operates with ± 5 V to ± 12 V supplies. In order to assure proper operation of the AD1864, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive and negative power supply pins are provided for the analog and digital portions of the AD1864, it is also possible to use the AD1864 in systems featuring a single positive and a single negative power supply. In this case, the $+V_S$ and $+V_L$ input pins should be connected to the positive power supply. $-V_S$ and $-V_L$ should be connected to the single negative supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well-regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1864 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1864s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz (8 × Fs). The test waveform is a 990.5 kHz sine wave with 0 dB, −20 dB and −60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low-amplitude signals are being reproduced. The MSB-adjust circuitry is shown in Figure 8. The trim pot should be adjusted to produce the lowest distortion using an input signal with a −60 dB amplitude.

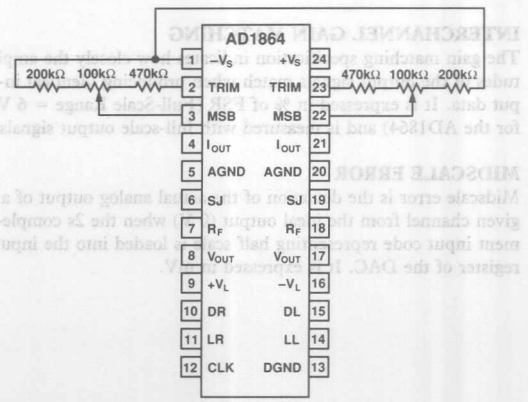


Figure 8. Optional DIP THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1864 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1864 can also be used in voltage output mode utilizing the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown in the AD1864 block diagram, each channel of the AD1864 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1864 channels. Figure 7 shows these connections. I_{OUT} is connected to the summing junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the performance shown on the specifications page while operating at $8 \times F_S$.

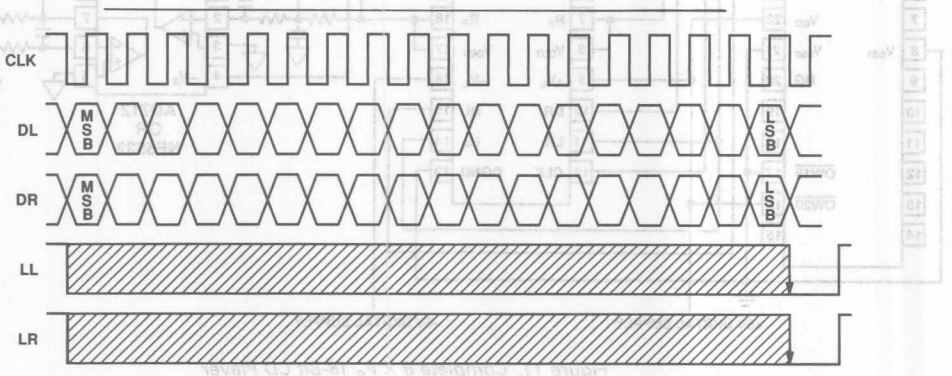


Figure 9. AD1864 Control Signals

INPUT DATA

Data is transmitted to the AD1864 in a bit stream composed of 18-bit words with a serial, 2s complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edges of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 9 illustrates the general signal requirements for data transfer for the AD1864.

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1864 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1864 is at least 12.7 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and $16 \times F_S$ (where F_S equals 44.1 kHz). The applications section of this datasheet contains additional guidelines for using the AD1864.

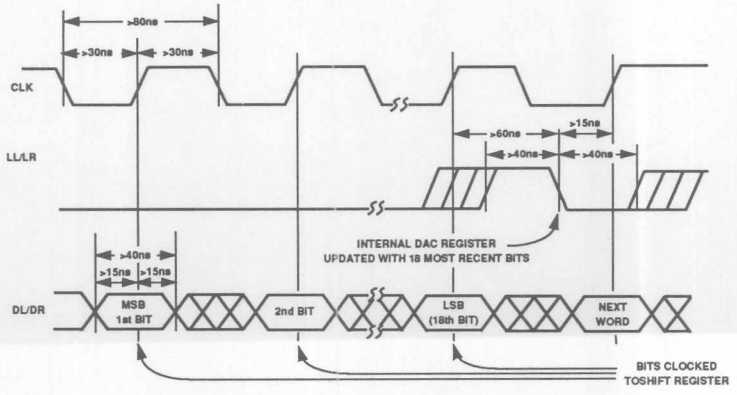


Figure 10. AD1864 Timing Diagram

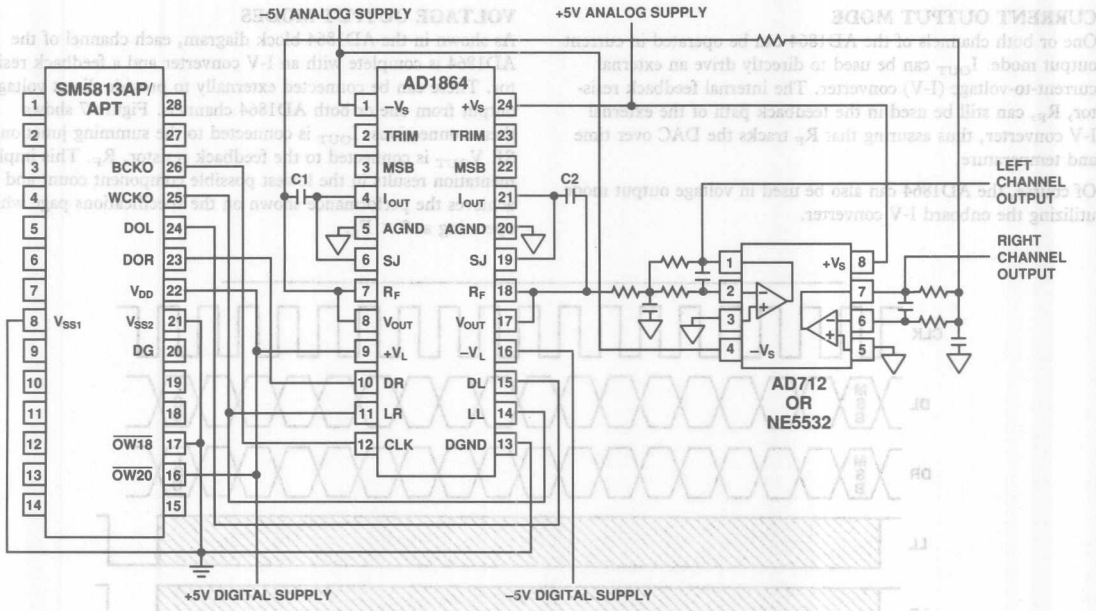


Figure 11. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

Figure 11 illustrates an 18-bit CD player design incorporating an AD1864 D/A converter, an AD712 or NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1864. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1864. Note that no external components are required by the AD1864. Also, no deglitching circuitry is required.

An AD712 or NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Close matching of the ac characteristics of the amplifiers on the AD712 as well as their low distortion make it an ideal choice for the task.

Low distortion, superior channel separation, low power consumption and a low component count are all realized by this simple design.

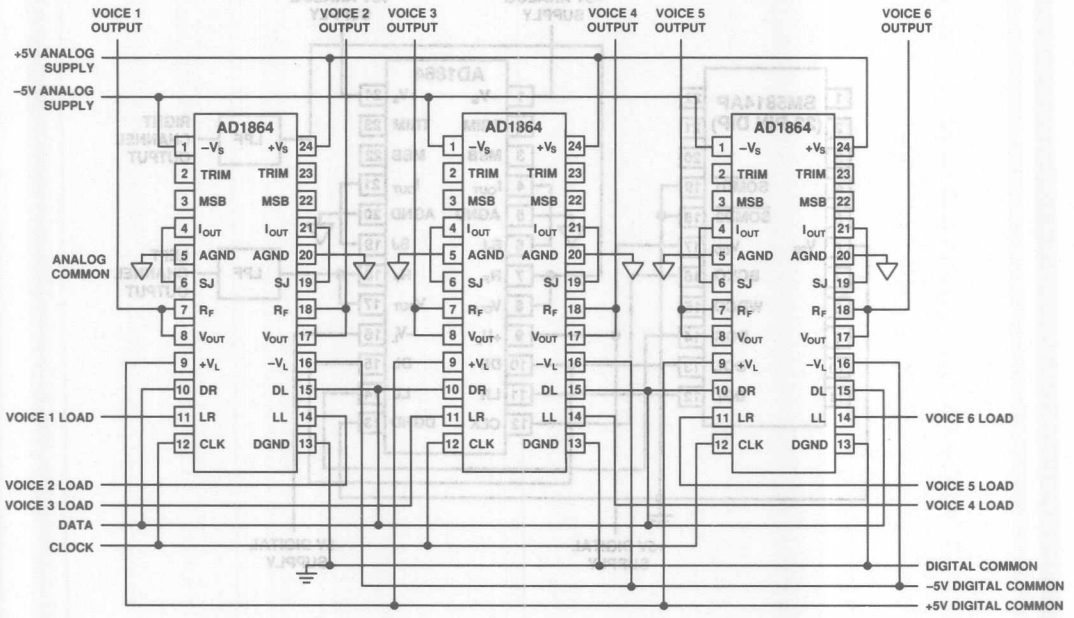


Figure 12. Cascaded AD1864s in a Multichannel Keyboard Instrument

MULTICHANNEL DIGITAL KEYBOARD DESIGN

Figure 12 illustrates how to cascade AD1864s to add multiple voices to an electronic musical instrument. In this example, the data and clock signals are shared between all six DACs. As the data representing an output for a specific voice is loaded, the appropriate DAC is updated. For example, after the 18 bits representing the next output value for Voice #4 is clocked out on the data line, then "Voice 4 Load" is pulled low. This produces a new output for Voice 4. Furthermore, all voices can be returned to the same output by pulling all six load signals low.

In this application, the advantages of choosing the AD1864 are clear. Its flexible digital interface allows the clock and data to be shared among all DACs. This reduces printed circuit board area requirements and also simplifies the actual layout of the board. The low power requirement of the AD1864 (typically 215 mW) is an advantage in a multiple DAC system where its power advantage is multiplied by the number of DACs used. The AD1864 requires no external components, simplifying the design, reducing the total number of components required and enhancing reliability.

ADDITIONAL APPLICATIONS

Figures 13 through 16 show connection diagrams for the AD1864 and a number of standard digital filter chips from Yamaha, NPC and Sony. Figure 13 shows the SM5814AP operating with pipelined data. Cophase operation is not available with the SM5814AP in 18-bit mode. Figures 14 through 16 are all examples of cophase operation. Each application operates at $8 \times F_S$ for each channel. The 2-pole Rauch low pass filters shown in Figure 11 can be used with all of the applications shown in this data sheet. The AD711 single op amp can also be used in these applications in order to ensure maximum channel separation.

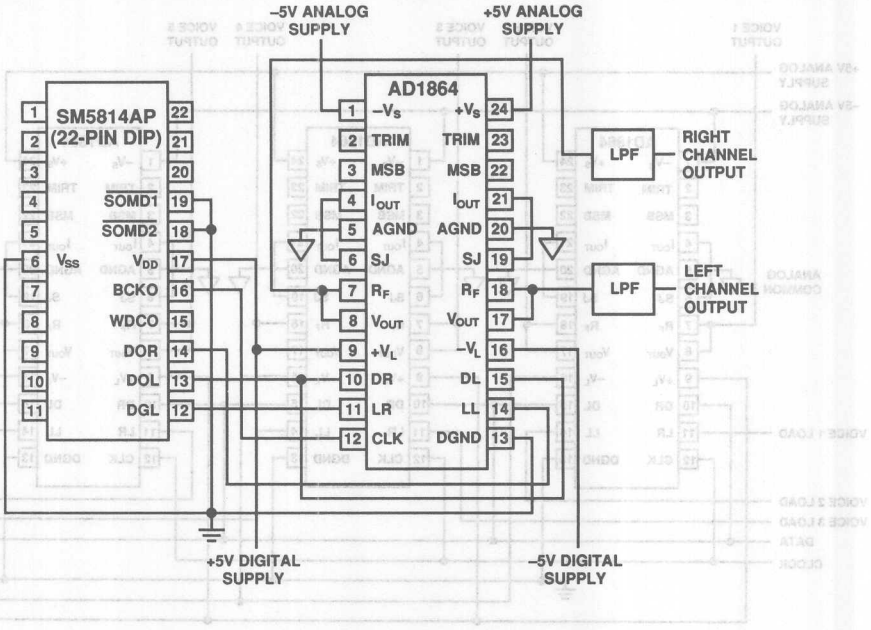


Figure 13. AD1864 with NPC SM5814AP Digital Filter

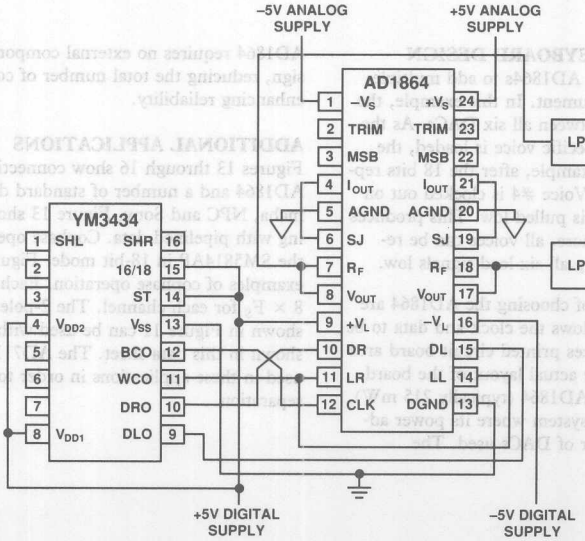


Figure 14. AD1864 with Yamaha YM3434 Digital Filter

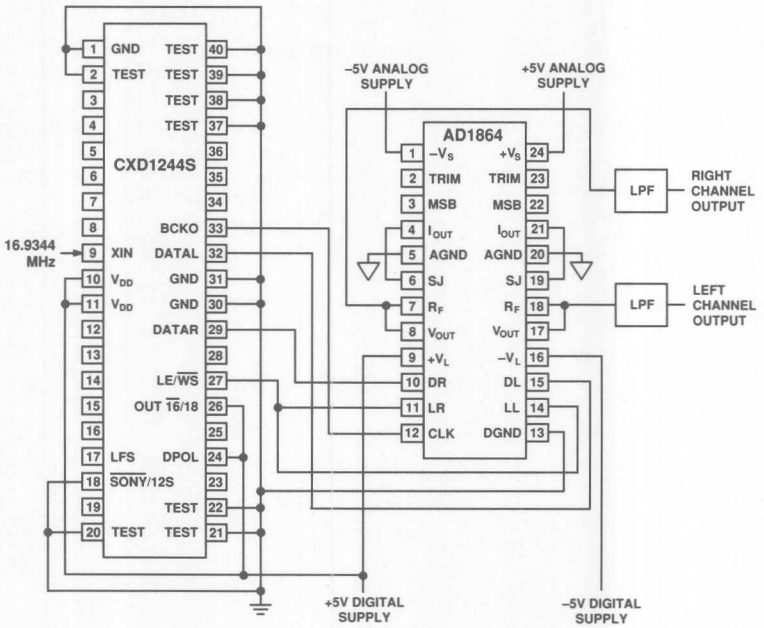


Figure 15. AD1864 with Sony CXD1244S Digital Filter

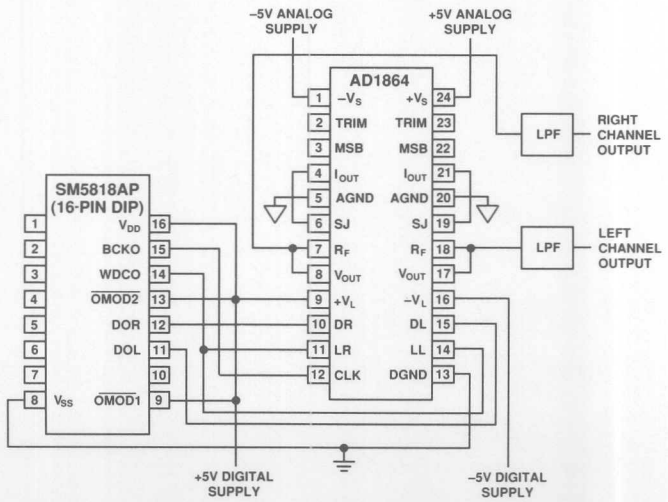


Figure 16. AD1864 with NPC SM5818AP Digital Filter

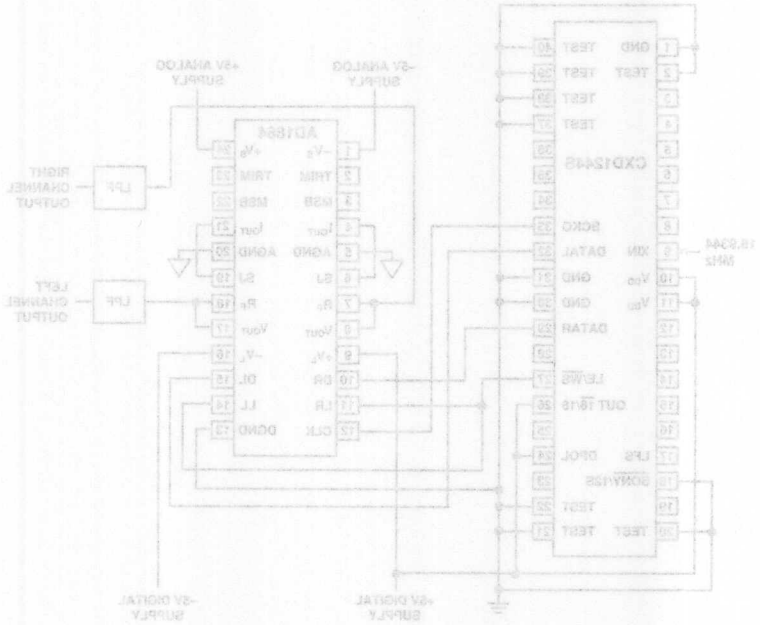


Figure 15. AD1864 with Sony CXD1244S Digital Filter

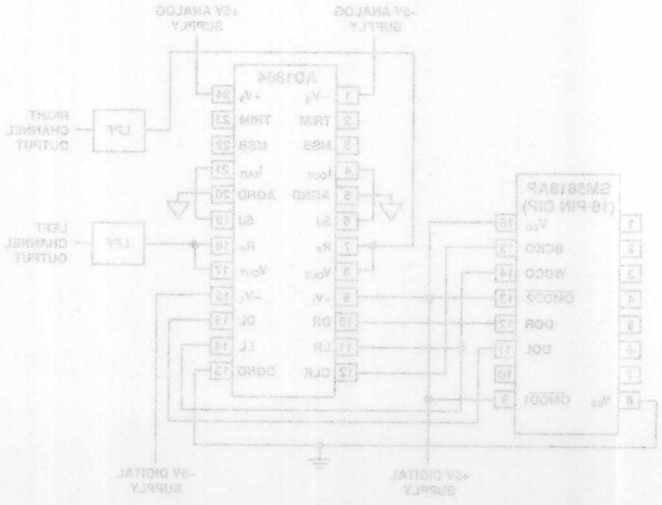


Figure 16. AD1864 with NPC SM5818AP Digital Filter

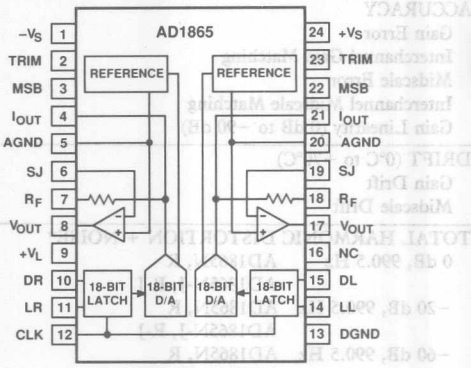
Complete Dual 18-Bit 16 × F_S Audio DAC

AD1865*

FEATURES
- Dual Serial Input, Voltage Output DACs
- No External Components Required
- 110 dB SNR
- 0.003% THD+N
- Operates at 16 × Oversampling per Channel
- ±5 Volt Operation
- Cophased Outputs
- 116 dB Channel Separation
- Pin Compatible with AD1864
- DIP or SOIC Packaging

APPLICATIONS
- Multichannel Audio Applications:
- Compact Disc Players
- Multivoice Keyboard Instruments
- DAT Players and Recorders
- Digital Mixing Consoles
- Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM
(DIP Package)



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. The AD1865 is a Complete Dual 18-Bit Audio DAC.
2. 110 dB Signal-To-Noise Ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × F_S.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.

*Protected by U.S. Patents Nos.: RE 30,586; 3,961,326; 4,141,004; 4,349,811; 4,855,618. 4,857,862.

REV. 0

AD1865—SPECIFICATIONS (T_A = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = −5 V, F_S = 705.6 kHz, no MSB adjustment or deglitcher)

Parameter		Min	Typ	Max	Unit
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.0		$+V_L$	V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = $+V_L$			**1.0**	μA
	I_{IL}, V_{IL} = 0.4 V			**−10**	μA
Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			0.2	**1.0**	% of FSR
Interchannel Gain Matching			0.3	**0.8**	% of FSR
Midscale Error			4		mV
Interchannel Midscale Matching			5		mV
Gain Linearity (0 dB to −90 dB)			<2		dB
DRIFT (0°C to +70°C)					
Gain Drift			±25		ppm of FSR/°C
Midscale Drift			±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*					
0 dB, 990.5 Hz	AD1865N, R		0.004	**0.006**	%
	AD1865N-J, R-J		0.003	**0.004**	%
−20 dB, 990.5 Hz	AD1865N, R		0.010	**0.040**	%
	AD1865N-J, R-J		0.010	**0.020**	%
−60 dB, 990.5 Hz	AD1865N, R		1.0	**4.0**	%
	AD1865N-J, R-J		1.0	**2.0**	%
CHANNEL SEPARATION*					
0 dB, 990.5 Hz		**110**	116		dB
SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz)		**107**	110		dB
D-RANGE* (with A-Weight Filter)					
−60 dB, 990.5 Hz	AD1865N, R	**88**	100		dB
	AD1865N-J, R-J	**94**	100		dB
OUTPUT					
Voltage Output Configuration					
Output Range (±1%)		**±2.94**	±3.0	**±3.06**	V
Output Impedance			0.1		Ω
Load Current		±8			mA
Short Circuit Duration		Indefinite to Common			
Current Output Configuration					
Bipolar Output Range (±30%)			±1		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
$+V_L$ and $+V_S$		4.75	**5.0**	5.25	V
$-V_S$		−5.25	**−5.0**	−4.75	V
+I, $+V_L$ and $+V_S$ = +5 V			22	**26**	mA
−I, $-V_S$ = −5 V			−23	**−26**	mA
POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = −5 V			225	**260**	mW
TEMPERATURE RANGE					
Specification		0	**+25**	+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C
WARMUP TIME		1			min

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6.0 V
V_S to AGND . . . . . 0 to 6.0 V
$-V_S$ to AGND . . . . . −6.0 to 0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



2

ORDERING GUIDE

Model	Temperature Range	THD+N @ FS	Package Option*
AD1865N	−25°C to +70°C	0.006%	N–24
AD1865N-J	−25°C to +70°C	0.004%	N–24
AD1865R	−25°C to +70°C	0.006%	R–28
AD1865R-J	−25°C to +70°C	0.004%	R–28

*N = Plastic DIP, R = Small Outline IC Package. For outline information see Package Information section.

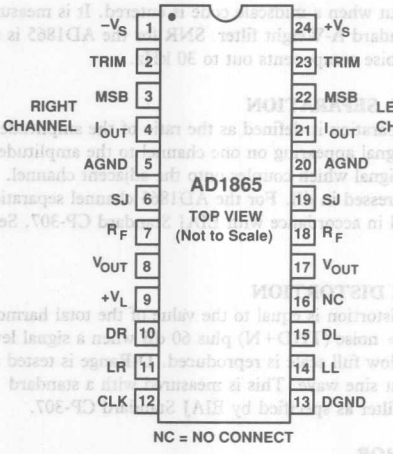
PIN DESIGNATIONS

DIP	SOIC		
1	22	$-V_S$	Negative Analog Supply
2	23	TRIM	Right Channel Trim Network Connection
3	24	MSB	Right Channel Trim Potentiometer Wiper Connection
4	26	I_{OUT}	Right Channel Output Current
5	28	AGND	Analog Common Pin
6	1	SJ	Right Channel Amplifier Summing Junction
7	2	R_F	Right Channel Feedback Resistor
8	3	V_{OUT}	Right Channel Output Voltage
9	4	$+V_L$	Positive Digital Supply
10	5	DR	Right Channel Data Input Pin
11	6	LR	Right Channel Latch Pin
12	7	CLK	Clock Input Pin
13	8	DGND	Digital Common Pin
14	9	LL	Left Channel Latch Pin
15	10	DL	Left Channel Data Input Pin
16	11, 16, 18, 25, 27	NC	No Internal Connection*
17	12	V_{OUT}	Left Channel Output Voltage
18	13	R_F	Left Channel Feedback Resistor
19	14	SJ	Left Channel Amplifier Summing Junction
20	15	AGND	Analog Common Pin
21	17	I_{OUT}	Left Channel Output Current
22	19	MSB	Left Channel Trim Potentiometer Wiper Connection
23	20	TRIM	Left Channel Trim Network Connection
24	21	$+V_S$	Positive Analog Supply

*Pin 16 has no internal connection; $-V_L$ from AD1864 DIP socket can be safely applied.

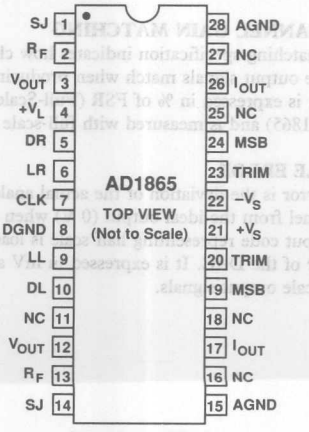
PINOUT

(24-Pin DIP Package)



NC = NO CONNECT

(28-Pin SOIC Package)



NC = NO CONNECT

AD1865—Definition of Specifications

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (−20 dB, −60 dB) signal amplitudes. THD+N measurements for the AD1865 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale code is entered to the amplitude of the output when a midscale code is entered. It is measured using a standard A-Weight filter. SNR for the AD1865 is measured for noise components out to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1865 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of −60 dB below full scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1865) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the twos complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV and is measured with half-scale output signals.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the twos complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.

FUNCTIONAL DESCRIPTION

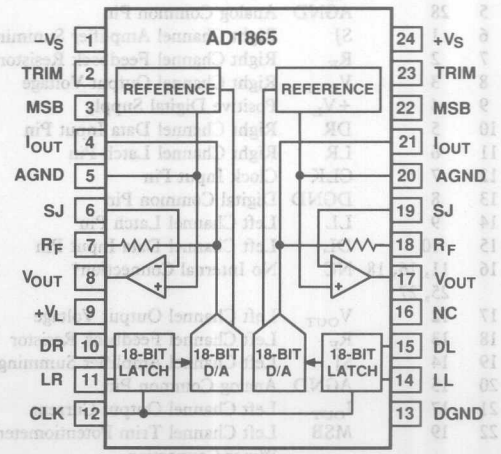
The AD1865 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and age.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R–2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1865.



AD1865 Block Diagram (DIP Package)

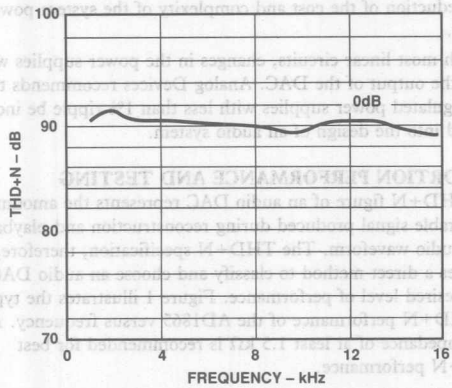


Figure 1. THD+N (dB) vs. Frequency (kHz)

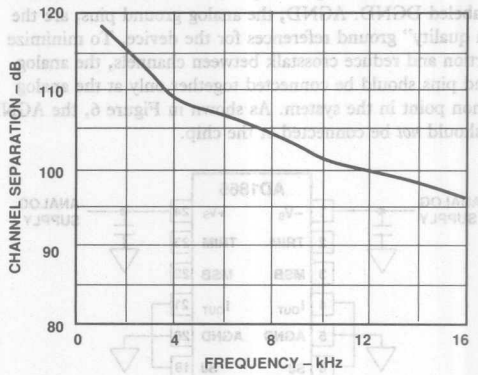


Figure 2. Channel Separation (dB) vs. Frequency (kHz)

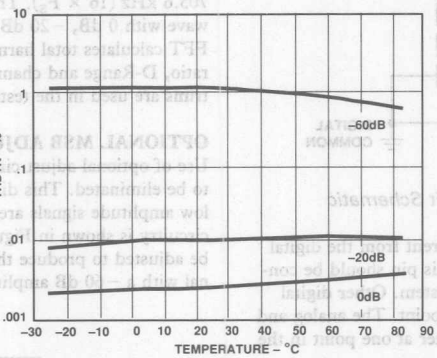


Figure 3. THD+N (%) vs. Temperature (°C)

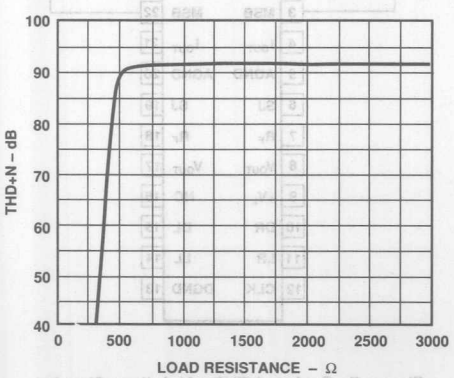


Figure 4. THD+N (dB) vs. Load Resistance (Ω)

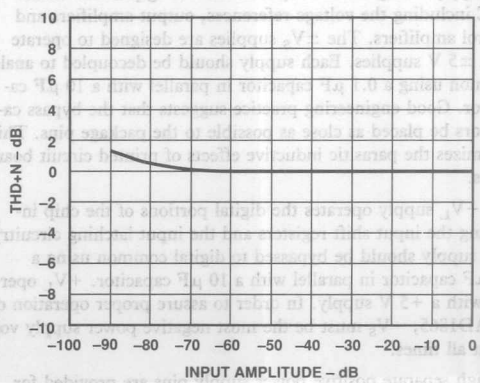


Figure 5. Gain Linearity (dB) vs. Input Amplitude (dB)

GROUNDING RECOMMENDATIONS

The AD1865 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 6, the AGND pins should *not* be connected at the chip.

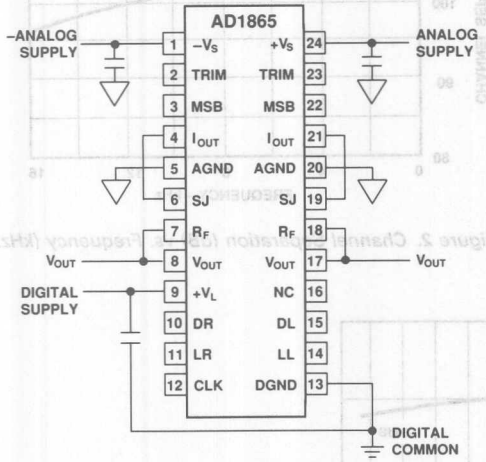


Figure 6. Recommended Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1865 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1865 has three power supply input pins. $\pm V_S$ provides the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ±5 V supplies. Each supply should be decoupled to analog common using a 0.1 μF capacitor in parallel with a 10 μF capacitor. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $+V_L$ supply operates the digital portions of the chip including the input shift registers and the input latching circuitry. This supply should be bypassed to digital common using a 0.1 μF capacitor in parallel with a 10 μF capacitor. $+V_L$ operates with a +5 V supply. In order to assure proper operation of the AD1865, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive power supply pins are provided for the analog and digital portions of the AD1865, it is also possible to use the AD1865 in systems featuring a single +5 V power supply. In this case, both the $+V_S$ and $+V_L$ input pins should be connected to the single +5 V power supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1865 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1865s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is transmitted at 705.6 kHz ($16 \times F_S$). The test waveform is a 990.5 Hz sine wave with 0 dB, −20 dB and −60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used in the testing of the AD1865.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low amplitude signals are being reproduced. The MSB adjust circuitry is shown in Figure 7. The trim potentiometer should be adjusted to produce the lowest distortion using an input signal with a −60 dB amplitude.

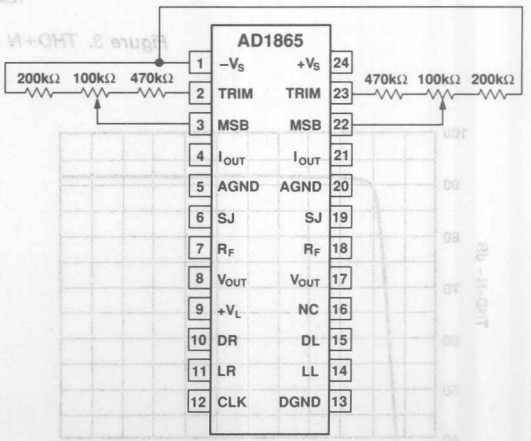


Figure 7. Optional THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1865 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1865 can also be used in voltage output mode in order to utilize the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown on the block diagram, each channel of the AD1865 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1865 channels. Figure 6 shows these connections. I_{OUT} is connected to the Summing Junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the specifications shown on the Specifications page while operating at 16 × F_S.

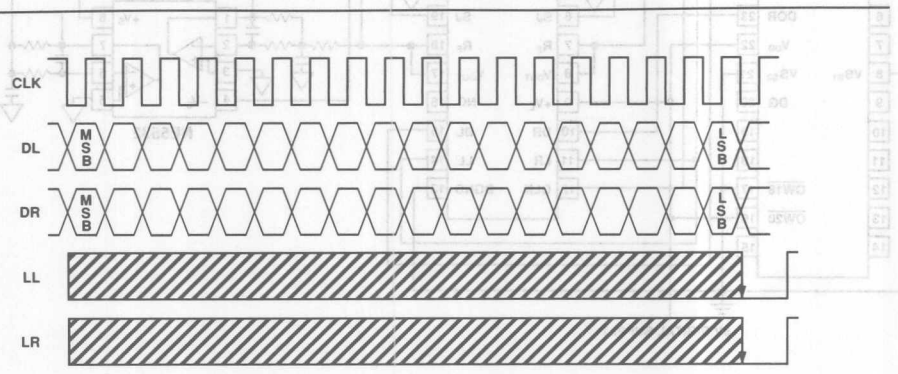


Figure 8. AD1865 Control Signals

INPUT DATA

Data is transmitted to the AD1865 in a bit stream composed of 18-bit words with a serial, twos complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edge of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 8 illustrates the general signal requirements for data transfer for the AD1865.

TIMING

Figure 9 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1865 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1865 is at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and 16 × F_S (where F_S equals 44.1 kHz).

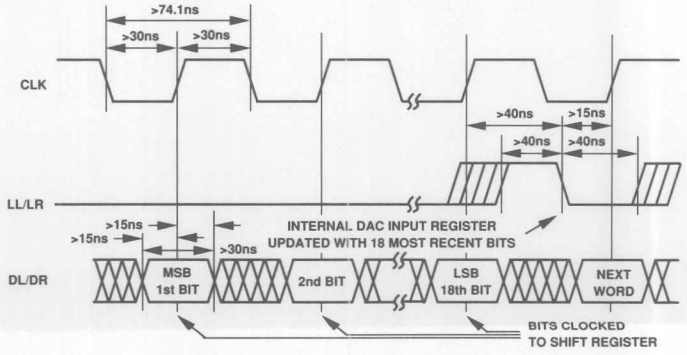


Figure 9. AD1865 Timing Diagram

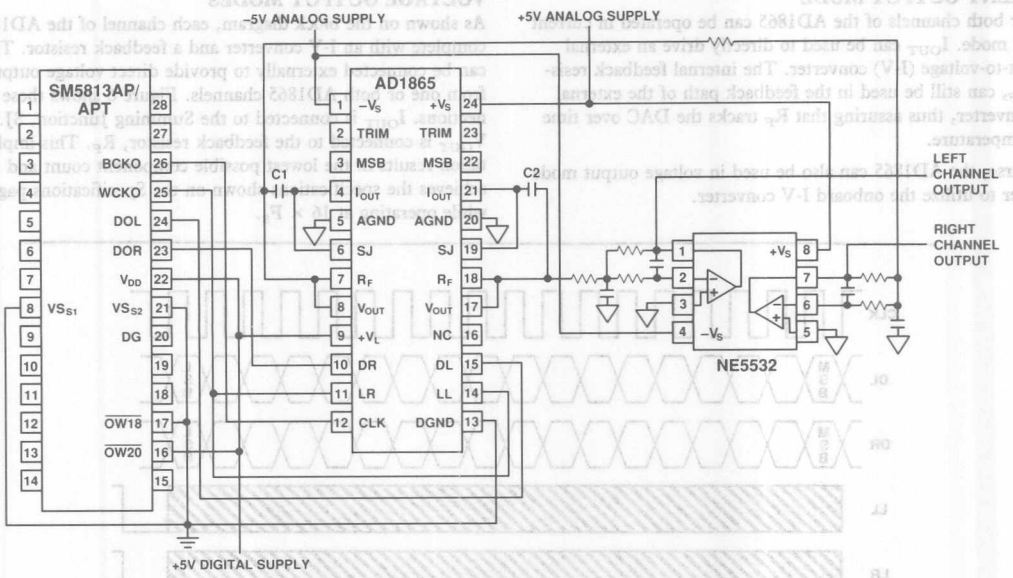


Figure 10. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

Figure 10 illustrates an 18-bit CD player design incorporating an AD1865 D/A converter, an NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1865. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1865. Note that no external components are required by the AD1865. Also, no deglitching circuitry is required.

An NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Low distortion, superior channel separation, low power consumption and a low parts count are all realized by this simple design.

MULTICHANNEL DIGITAL KEYBOARD DESIGN

Figure 11 illustrates how to cascade AD1865's to add multiple voices to an electronic musical instrument. In this example, the data and clock signals are shared between all six DACs. As the data representing an output for a specific voice is loaded, the appropriate DAC is updated. For example, after the 18-bits representing the next output value for Voice 4 is clocked out on the data line, then "Voice 4 Load" is pulled low. This produces a new output for Voice 4. Furthermore, all voices can be returned to the same output by pulling all six load signals low.

In this application, the advantages of choosing the AD1865 are clear. Its flexible digital interface allows the clock and data to be shared among all DACs. This reduces PC board area requirements and also simplifies the actual layout of the board. The low power requirements of the AD1865 (approximately 225 mW) is an advantage in a multiple DAC system where any power advantage is multiplied by the number of DACs used. The AD1865 requires no external components, simplifying the design, reducing the total number of components required and enhancing reliability.

2

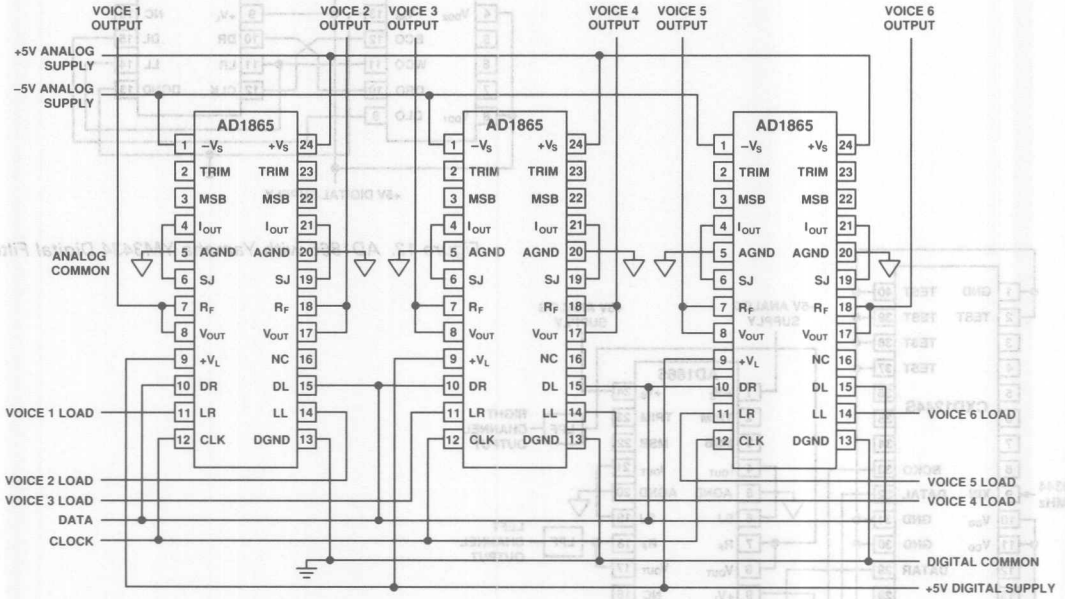


Figure 11. Cascaded AD1865s in a Multichannel Keyboard Instrument

ADDITIONAL APPLICATIONS

Figures 12 through 14 show connection diagrams for the AD1865 and standard digital filter chips from Yamaha, NPC and Sony. Each figure is an example of cophase operation operating at 8 × F_S for each channel. The 2-pole Rauch low pass filters shown in Figure 10 can be used with all of the applications shown in this data sheet.

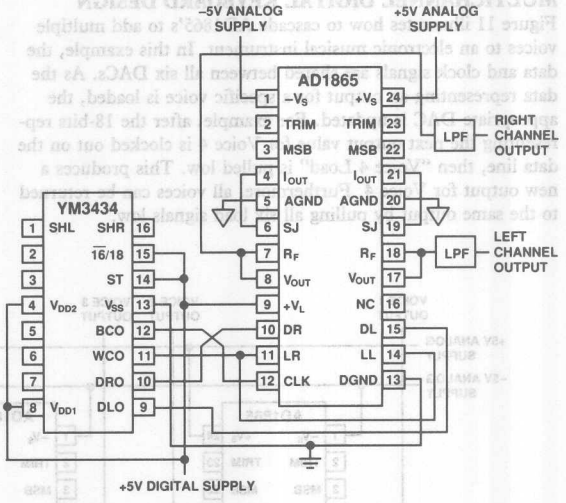


Figure 12. AD1865 with Yamaha YM3434 Digital Filter

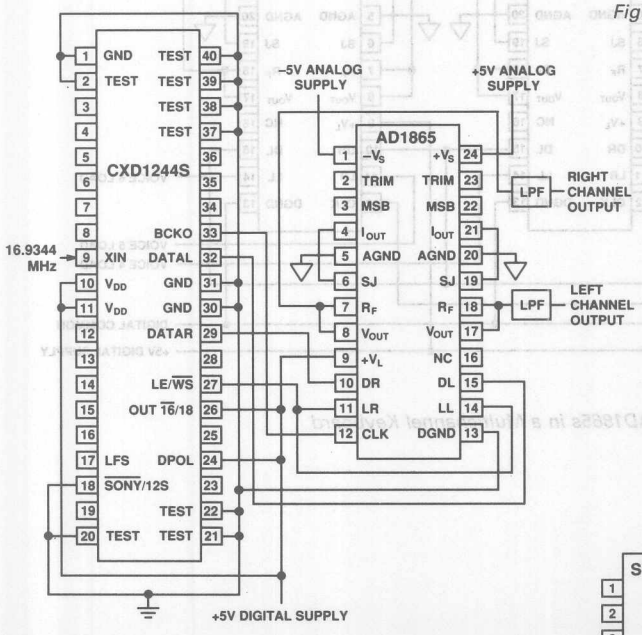


Figure 13. AD1865 with Sony CXD1244s Digital Filter

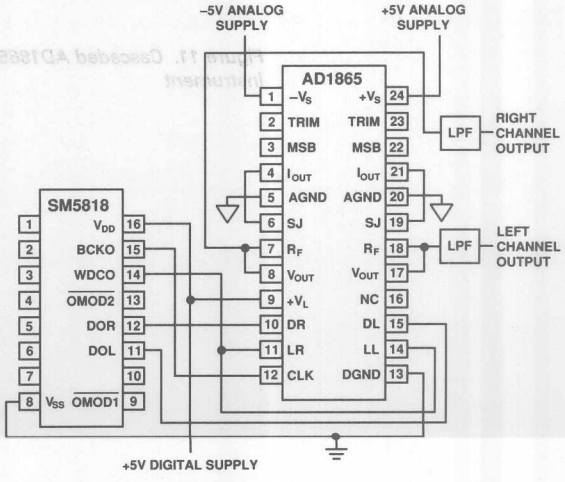


Figure 14. AD1865 with NPC SM5818AP Digital Filter

DEVICES

Dual 16-Bit Audio DAC

AD1866*

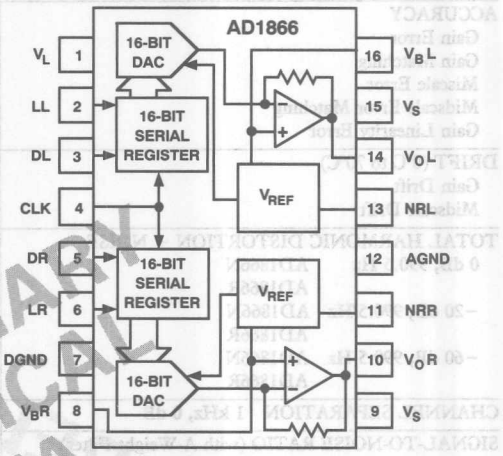
FEATURES

Dual Serial Input, Voltage Output DACs
Single +5 Volt Supply
0.005% THD+N
Low Power—45 mW
115 dB Channel Separation
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS

Multimedia Workstations
PC Audio Add-In Boards
Portable CD and DAT Players
Automotive CD and DAT Players
Noise Cancellation

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD1866 is a complete dual 16-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements and laser trimmed, thin film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation and low power dissipation.

The DACs on the AD1866 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into 7 elements. The 13 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1866 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. The 2.5 V reference voltages eliminate the need for "false ground" networks.

A versatile digital interface allows the AD1866 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 16 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S = 44.1 kHz) for each channel. The digital input pins of the AD1866 are TTL and +5 V CMOS compatible.

The AD1866 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1866 dissipates 45 mW.

The AD1866 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single supply operation @ +5 V.
2. 45 mW power dissipation.
3. THD+N is 0.005% (typical).
4. Signal-to-Noise Ratio is 95 dB (typical).
5. 115 dB channel separation (typical).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

***Protected by U.S. Patent Nos: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

RESOLUTION			16		Bits
DIGITAL INPUTS	V_{IH}	2.4			V
	V_{IL}			0.8	V
	I_{IH}, $V_{IH} = V_L$		1.0		μA
	I_{IL}, V_{IL} = DGND		−10.0		μA
Maximum Clock Input Frequency		13.5			MHz
ACCURACY					
Gain Error			±3		% of FSR
Gain Matching			±3		% of FSR
Miscale Error			±30		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to 70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			−130		μV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1866N		0.005	0.01	%
	AD1866R		0.005	0.01	%
−20 dB, 990.5/Hz	AD1866N		0.02		%
	AD1866R		0.02		%
−60 dB, 990.5 Hz	AD1866N		2.0		%
	AD1866R		2.0		%
CHANNEL SEPARATION	1 kHz, 0 dB	108	115		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)			95		dB
D-RANGE (with A-Weight Filter)			90		dB
OUTPUT					
Voltage Output Pins (V_{OL}, V_{OR})					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_{BL}, V_{BR})					
Output Range			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		4.75	5	5.25	V
Operation, V_L and V_S		3.5		5.25	V
+I, V_L and V_S = 5 V			9	13	mA
POWER DISSIPATION			45	65	mW
TEMPERATURE RANGE					
Operation		−35		85	°C
Storage		−60		100	°C

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Single Supply Dual 18-Bit Audio DAC

AD1868*

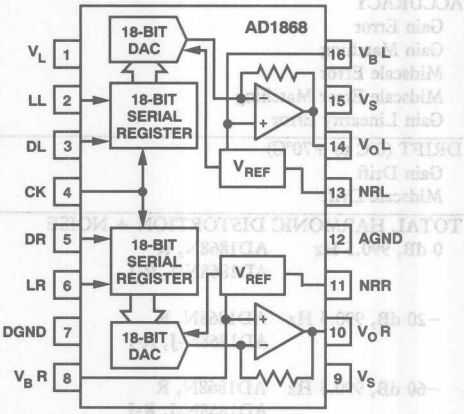
FEATURES

- Dual Serial Input, Voltage Output DACs
- Single +5 V Supply
- 0.004% THD+N (typical)
- Low Power: 50 mW (typical)
- >115 dB Channel Separation (typical)
- Operates at 8× Oversampling
- 16-Pin Plastic DIP or SOIC Package

APPLICATIONS

- Portable Compact Disc Players
- Portable DAT Players and Recorders
- Automotive Compact Disc Players
- Automotive DAT Players
- Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser-trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S equals 44.1 kHz) for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

The AD1868 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery-operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation @ +5 V
2. 50 mW power dissipation (typical)
3. THD+N is 0.004% (typical)
4. Signal-to-Noise Ratio is 97.5 dB (typical)
5. >115 dB channel separation (typical)
6. Compatible with all digital filter chips
7. 16-pin DIP and 16-pin SOIC packages
8. No deglitcher required
9. No external adjustments required

*Protected by U.S. Patents Numbers: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.

AD1868—SPECIFICATIONS (T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.4			V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = V_L		1.0		µA
	I_{IL}, V_{IL} = DGND		1.0		µA
Maximum Clock Input Frequency		13.5			MHz
ACCURACY					
Gain Error			±1		% of FSR
Gain Matching			±1		% of FSR
Midscale Error			±15		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			±100		µV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1868N, R		0.004	0.008	%
	AD1868N-J, R-J		0.004	0.006	%
−20 dB, 990.5 Hz	AD1868N, R		0.020	0.08	%
	AD1868N-J, R-J		0.020	0.08	%
−60 dB, 990.5 Hz	AD1868N, R		2.0	5.0	%
	AD1868N-J, R-J		2.0	5.0	%
CHANNEL SEPARATION 1 kHz, 0 dB		108	>115		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95	97.5		dB
D-RANGE (with A-Weight Filter)		86	92		dB
OUTPUT					
Voltage Output Pins (V_OL, V_OR)					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_BL, V_BR)					
Output Voltage			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		4.75	5	5.25	V
Operation, V_L and V_S		3.5		5.25	V
+I, V_L and V_S = 5 V			10	14	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Operation		−35		85	°C
Storage		−60		100	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6 V
V_S to AGND . . . . . 0 to 6 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



Typical Performance of the AD1868

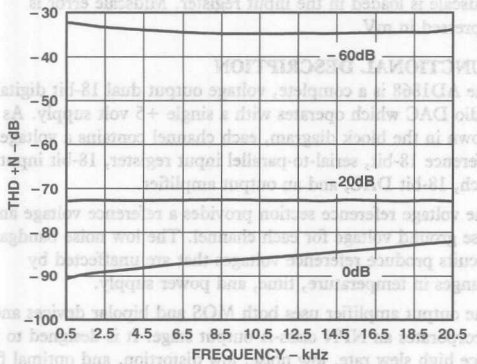


Figure 1. THD+N vs. Frequency

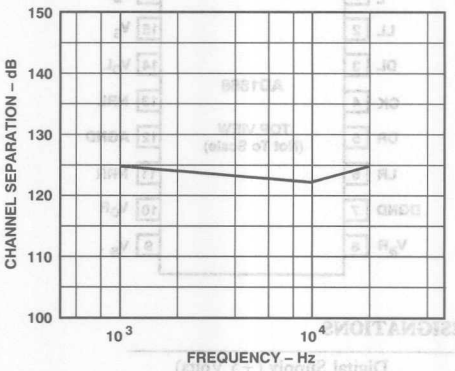


Figure 2. Channel Separation vs. Frequency

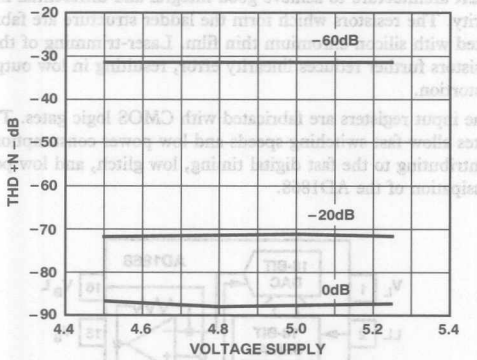


Figure 3. THD+N vs. Supply Voltage

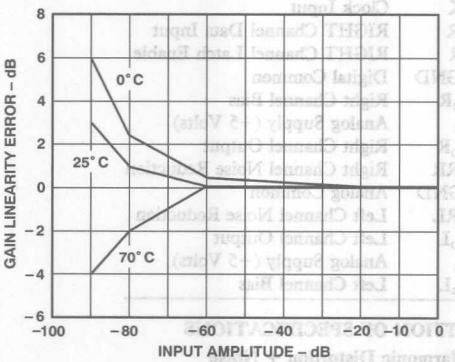


Figure 4. Gain Linearity Error vs. Input Amplitude

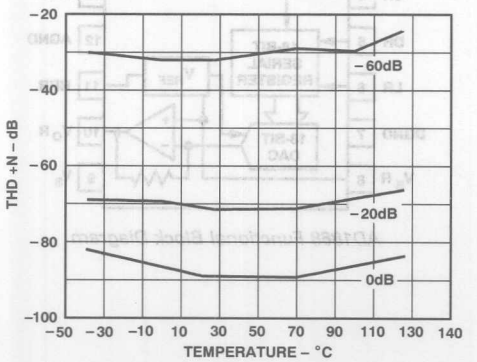


Figure 5. THD+N vs. Temperature

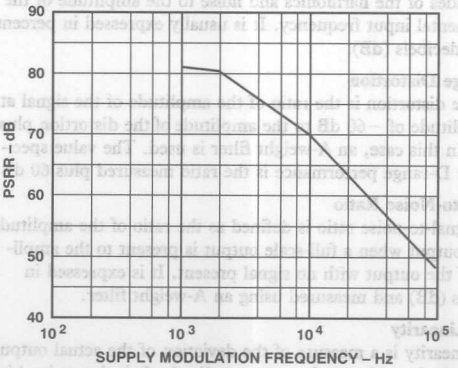
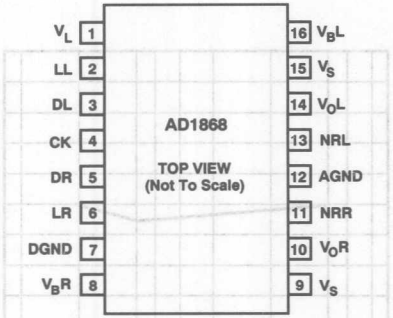


Figure 6. Power Supply Rejection Ratio vs. Frequency



PIN DESIGNATIONS

1	V_L	Digital Supply (+5 Volts)
2	LL	Left Channel Latch Enable
3	DL	Left Channel Data Input
4	CK	Clock Input
5	DR	RIGHT Channel Data Input
6	LR	RIGHT Channel Latch Enable
7	DGND	Digital Common
8	V_BR	Right Channel Bias
9	V_S	Analog Supply (+5 Volts)
10	V_OR	Right Channel Output
11	NRR	Right Channel Noise Reduction
12	AGND	Analog Common
13	NRL	Left Channel Noise Reduction
14	V_OL	Left Channel Output
15	V_S	Analog Supply (+5 Volts)
16	V_BL	Left Channel Bias

DEFINITION OF SPECIFICATIONS

Total Harmonic Distortion + Noise

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-Range Distortion

D-range distortion is the ratio of the amplitude of the signal at an amplitude of −60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

Signal-to-Noise Ratio

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

Gain Linearity

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

the bias when the twos complement input code representing midscale is loaded in the input register. Midscale error is expressed in mV.

FUNCTIONAL DESCRIPTION

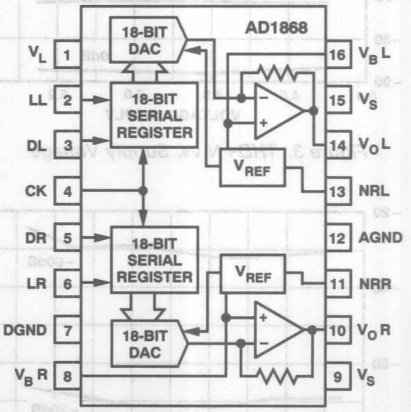
The AD1868 is a complete, voltage output dual 18-bit digital audio DAC which operates with a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference 18-bit, serial-to-parallel input register, 18-bit input-latch, 18-bit DAC, and an output amplifier.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class-A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

Each 18-bit DAC uses a combination of segmented decoder and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser-trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow fast switching speeds and low power consumption, contributing to the fast digital timing, low glitch, and low power dissipation of the AD1868.



AD1868 Functional Block Diagram

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1868 has two ground pins, designated as AGND (Pin 12) and DGND (Pin 7). The analog ground, AGND, serves as the "high quality" reference ground for analog signals and as a return path for the supply current from the analog portion of the device. The system analog common should be located as close as possible to Pin 12 to minimize any voltage drop which may develop between these two points, although the internal circuit is designed to minimize signal dependence of the analog return current.

The digital ground, DGND, returns ground current from the digital logic portion of the device. This pin should be connected to the digital common node in the system. As shown in Figure 7, the analog and digital grounds should be joined at one point in the system. When these two grounds are remotely connected such as at the power supply ground, care should be taken to minimize the voltage difference between the DGND and AGND pins in order to ensure the specified performance.

POWER SUPPLIES AND DECOUPLING

The AD1868 has three power supply input pins. V_S (Pins 9 and 15) provide the supply voltages which operate the analog portion of the device including the 18-bit DACs, the voltage references, and the output amplifiers. The V_S supplies are designed to operate with a +5 V supply. These pins should be decoupled to analog common using a 0.1 μF capacitor. Good engineeringpractice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the inherent inductive effects of printed circuit board traces.

V_L (Pin 1) operates the digital portions of the chip including the input shift registers and the input latching circuitry. V_L is also designed to operate with a +5 V supply. This pin should be bypassed to digital common using a 0.1 μF capacitor, again placed as close as possible to the package pin. Figure 7 illustrates the correct connection of the digital and analog supply bypass capacitors.

An important feature of the AD1868 audio DAC is its ability to operate at reduced power supply voltages. This feature is very important in portable battery-operated systems. As the batteries discharge, the supply voltage drops. Unlike any other audio DAC, the AD1868 can continue to function at supply voltages as low as 3.5 V. Because of its unique design, the power requirements of the AD1868 diminish as the battery voltage drops, further extending the operating time of the system.

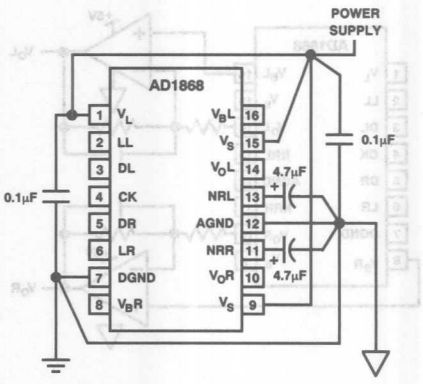


Figure 7. Recommended Circuit Schematic

NOISE REDUCTION CAPACITORS

The AD1868 has two noise-reduction pins designated as NRL (Pin 13) and NRR (Pin 11). It is recommended that external noise-reduction capacitors be connected from these pins to AGND to reduce the output noise contributed by the voltage reference circuitry. As shown in Figure 7, each of these pins should be bypassed to AGND with a 4.7 μF or larger capacitor. The connections between the capacitors, package pins and AGND should be as short as possible to achieve the lowest noise.

USING V_BL AND V_BR

The AD1868 has two bias voltage reference pins, designated as V_BR (Pin 8) and V_BL (Pin 16). These pins supply a dc reference voltage equal to the center of the output voltage swing. These bias voltages replace "False Ground" networks previously required in single-supply audio systems. At the same time, they allow dc-coupled systems, improving audio performance.

Figure 8a illustrates the traditional approach used to generate False Ground voltages in single-supply audio systems. This circuit requires additional power and circuit board space.

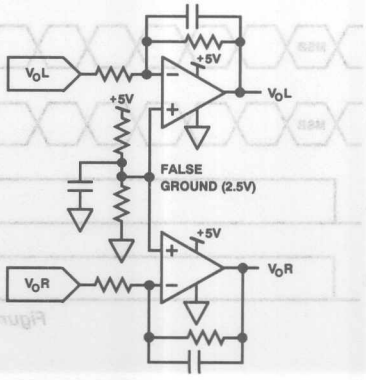


Figure 8a. Schematic Using False Ground

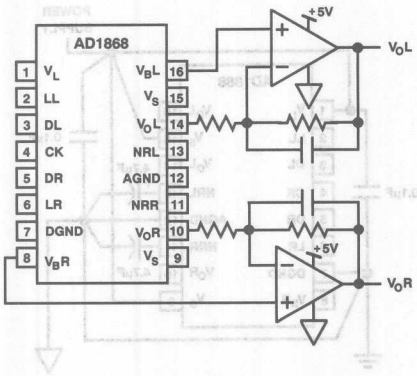


Figure 8b. Circuitry Using Voltage Biases

The AD1868 eliminates the need for "False Ground" circuitry. V_BR and V_BL generate the required bias voltages previously generated by the "False Ground." As shown in Figure 8b, V_BR and V_BL may be used as the reference point in each output channel. This permits a dc-coupled output signal path. This eliminates ac-coupling capacitors and improves low frequency performance. It should be noted that these bias outputs have relatively high output impedance and will not drive output currents larger than 100 μA without degrading the specified performance.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. Therefore, the THD+N specification provides a direct method to classify and choose an audio DAC for a desired level of performance.

Figure 1 illustrates the typical THD+N versus frequency performance of the AD1868. It is evident that the THD+N performance of the AD1868 remains stable at all three levels through a wide range of frequencies. A load impedance of at least 2 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1868s on the basis of THD+N performance. During the distortion test, a high speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz (8× F_S). The test waveform is a 990.5 Hz sine wave with 0 dB, −20 dB, and −60 dB amplitudes. A 4096-point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, and D-range. No deglitchers or external adjustments are used.

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

The AD1868 digital input port employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial inputs for the left and right DACs, respectively. Input data bits are clocked into the input register on the rising edge of CLK. The falling edges of LL and LR cause the last 18 bits which were clocked into the serial registers to be shifted into the DACs, thereby updating the respective DAC outputs. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together. Data is transmitted to the AD1868 in a bit stream composed of 18-bit words with a serial, twos complement, MSB first format. Left and right channels share the Clock (CLK) signal.

Figure 9 illustrates the general signal requirements for data transfer for the AD1868.

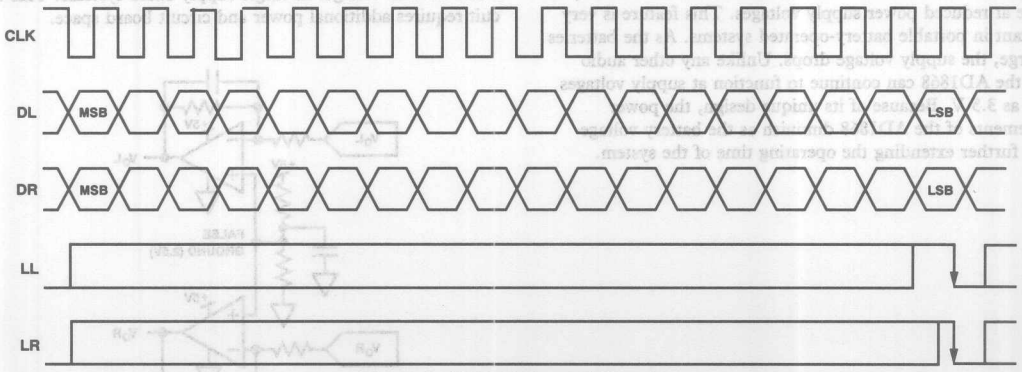


Figure 9. AD1868 Control Signals

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1868 are TTL and 5 V CMOS compatible.

The maximum clock rate of the AD1868 is specified to be at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8×, and 16× F_S (where F_S equals 44.1 kHz). The applications section of this data sheet contains additional guidelines for using the AD1868.

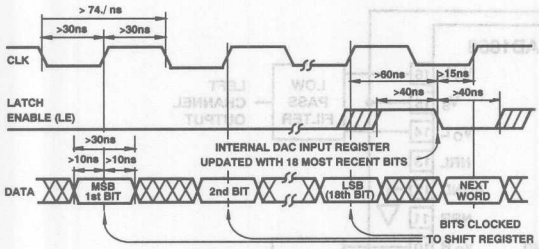


Figure 10. AD1868 Input Signal Timing

APPLICATIONS OF THE AD1868

The AD1868 is a high performance audio DAC specifically designed for portable and automotive digital audio applications. These market segments have technical requirements fundamentally different than those found in the high end or home-use market segments. Portable equipment must rely on components which require low amounts of power to offer reasonable playing times. Also, battery voltages drop as the end of the discharge cycle is approached. The AD1868's ability to operate from a single +5 V supply makes it a good choice for battery-operated gear. As the battery voltage drops, the power dissipation of the AD1868 drops. This extends the usable battery life. Finally, as the battery supply voltage drops, the bias voltages and signal swings also drop, preventing signal clipping and abrupt degradation of distortion. Figure 3 illustrates that THD+N performance of the AD1868 remains constant through a wide range of supply voltages.

Automotive equipment rely on components which are able to consistently perform in a wide range of temperatures. In addition, due to the limited space available in automotive applications, small size is essential. The AD1868 is able to satisfy both of these requirements. The device has guaranteed operation between −35°C and +85°C, and the 16-pin DIP or 16-pin SOIC package is particularly attractive where overall size is important.

Since the AD1868 provides dc bias voltages, the entire signal chain can be dc-coupled. This eliminate ac-coupling capacitors from the signal path, improving low frequency performance and lowering system cost and size.

In summary, the AD1868 is an excellent choice for battery-operated portable or automotive digital audio systems. In the following sections, some examples of high performance audio applications featuring the AD1868 are described.

AD1868 with Sony CXD2550P Digital Filter

Figure 11 illustrates an 18-bit CD player design incorporating an AD1868 DAC, a Sony CXD2550P digital filter and 2-pole antialias filters. This high performance, single-supply design operates at 8× F_S and is suitable for portable and automotive applications. In this design, the CXD2550P filter transmits left and right channel digital data to the AD1868. The left and right latch signals, LL and LR, are both provided by the word clock signal (LRCKO) of the digital filter. The digital data is converted to low distortion output voltages by the output amplifiers on the AD1868. Also, no deglitching circuitry or external adjustments are required. Bypass capacitors, noise-reduction capacitors and the antialias filter details are omitted for clarity.

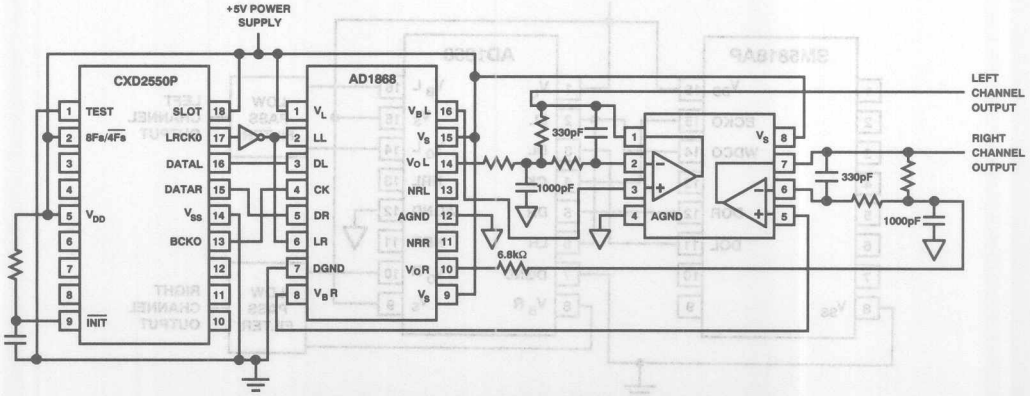


Figure 11. AD1868 with Sony CXD2550P Digital Filter

ADDITIONAL APPLICATIONS

In addition to CD player designs, the AD1868 is suitable for similar applications such as DAT, portable musical instruments, Laptop and Notebook personal computers, and PC audio I/O boards. The circuit techniques illustrated are directly applicable in those applications.

Figures 12, 13, and 14 show connection diagrams for the AD1868 with popular digital filter chips from NPC and Yamaha. Each application operates at 8× F_S operation. Please refer to the appropriate sections of this data sheet for additional information.

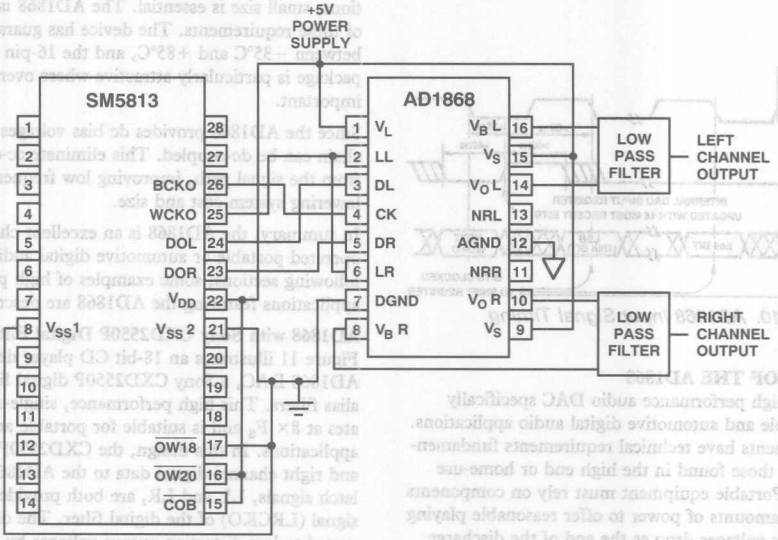


Figure 12. AD1868 with NPC SM5813 Digital Filter

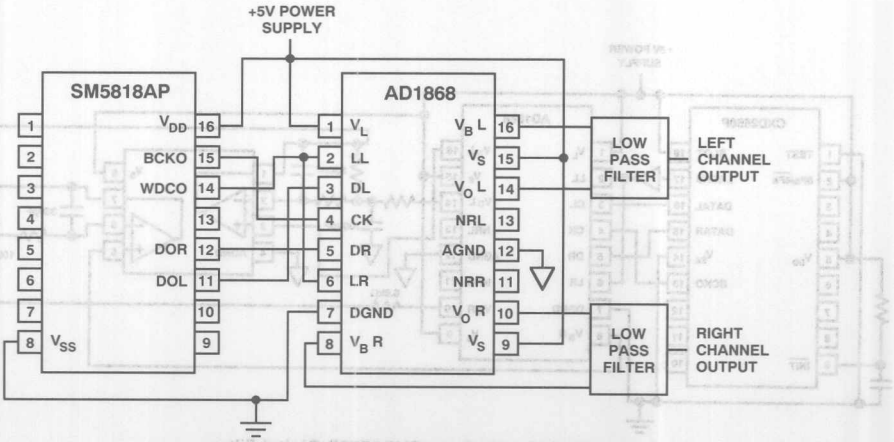


Figure 13. AD1868 with NPC SM5818AP Digital Filter

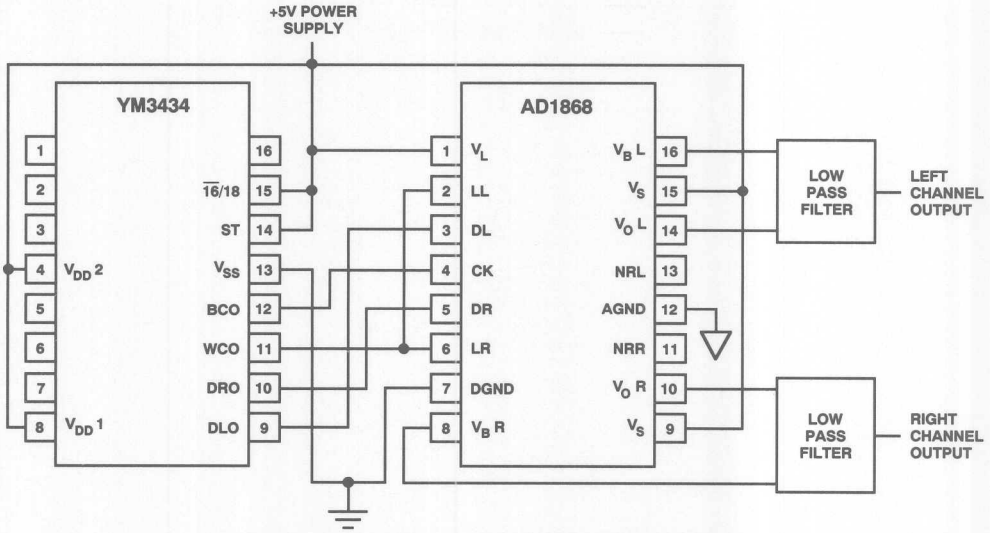


Figure 14. AD1868 with Yamaha YM3434 Digital Filter

2

ORDERING GUIDE

Model	THD+N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.006%	95 dB	N-16
AD1868R-J	0.006%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

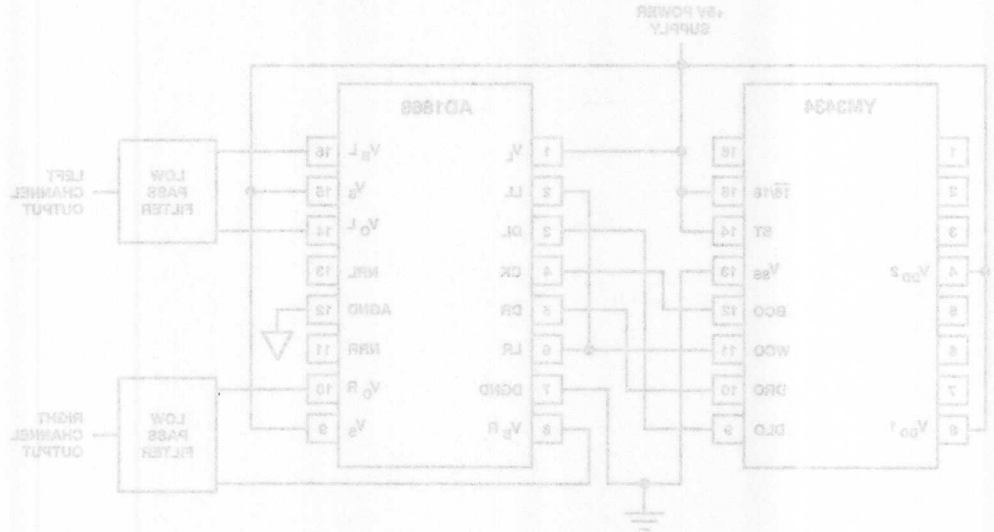


Figure 14. AD1868 with Yamaha YM3434 Digital Filter

ORDERING GUIDE

Model	THD+N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.008%	95 dB	N-16
AD1868R-J	0.008%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

ANALOG DEVICES

LOGDAC
CMOS Logarithmic D/A Converter

AD7111*

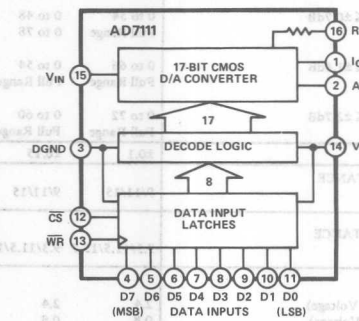
FEATURES

Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

APPLICATIONS

Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The LOGDAC™ AD7111 is a CMOS multiplying D/A converter which can attenuate an analog input signal over the range 0 to −88.5dB in 0.375dB steps.

The degree of attenuation is determined by an 8-bit data word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{CS}$ and $\overline{WR}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is available in a standard 16-pin DIP and in a 20-terminal surface mount package.

ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option*
AD7111KN	0°C to +70°C	0dB to 60dB	N-16
AD7111BQ	−25°C to +85°C	0dB to 60dB	Q-16
AD7111TQ	−55°C to +125°C	0dB to 60dB	Q-16
AD7111LN	0°C to +70°C	0dB to 72dB	N-16
AD7111CQ	−25°C to +85°C	0dB to 72dB	Q-16
AD7111UQ	−55°C to +125°C	0dB to 72dB	Q-16
AD7111TE/883B	−55°C to +125°C	0dB to 60dB	E-20A

*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip.
For outline information see Package Information section.

*U.S. Patent No. 4521764
LOGDAC is a trademark of Analog Devices Inc.

AD7111—SPECIFICATIONS (V_{DD} = +5V, V_{IN} = −10V dc, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated)

Parameter	AD7111L/C/U GRADES T_A = +25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0dB ATTENUATION						
0.375dB Steps:						
Accuracy ≤ ±0.17dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed attenuation ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for specified step sizes
0.75dB Steps:						
Accuracy ≤ ±0.35dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5dB Steps:						
Accuracy ≤ ±0.7dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range is from 0 to 88.5dB
3.0dB Steps:						
Accuracy ≤ ±1.4dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
6.0dB Steps:						
Accuracy ≤ ±2.7dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE (PIN 15)	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE (PIN 16)	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	μA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	μs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IH} or V_{IL}
	500	1000	500	1000	μA max	Digital Inputs = 0V or V_{DD}. See Figure 7.

NOTE
[1] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.
V_{DD} = +5V, V_{IN} = −10V dc except where stated, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated.

Parameter	AD7111L/C/U GRADES T_A = 25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ±10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	μs max	Full Scale Change Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.
Digital-to-Analog Glitch Impulse	100	–	100	–	nV secs typ	Measured with ADLH0032CG as Output Amplifier for Input Code Transition 10000000 to 00000000. C1 of Figure 1 is 0pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1kHz	–94	–72	–92	–68	dB max	Feedthrough is also determined by circuit
Total Harmonic Distortion	–91	–91	–91	–91	dB typ	layout (see Figure 4).
Output Noise Voltage Density	70	70	70	70	nV/$\sqrt{Hz}$ max	V_{IN} = 6V rms at 1kHz
Digital Input Capacitance	7	7	7	7	pF max	Includes AD544 Amplifier Noise

Specifications subject to change without notice.

V_{DD} (to DGND)	+7V
V_{IN} (to AGND)	+35V
Digital Input Voltage to DGND	$-0.3V$ to $V_{DD}+0.3V$
I_{OUT} to AGND	$-0.3V$ to V_{DD}
V_{IN} to AGND	±35V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Industrial (B, C Versions)	−25°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

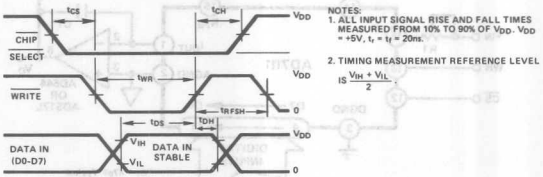
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

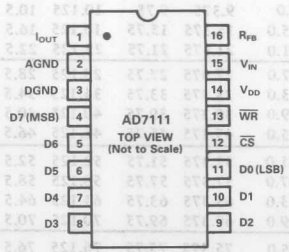
PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

WRITE CYCLE TIMING DIAGRAM

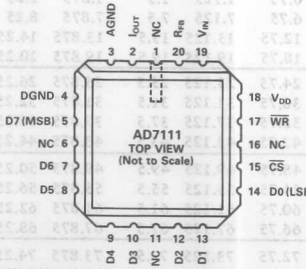


PIN CONFIGURATIONS

DIP



LCCC



CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7111 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. The rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \frac{0.375\ N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right| \text{ dB} = -0.375\ N$$

Where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leqslant N \leqslant 255$ the output is zero. Table I gives the output attenuation relative to 0dB for all possible input codes.

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For example, the AD7111L is guaranteed monotonic in 0.375dB steps from 0 to –54dB inclusive and in 0.75dB steps from 0 to –72dB inclusive. To achieve monotonic operation over the entire 88.5dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.

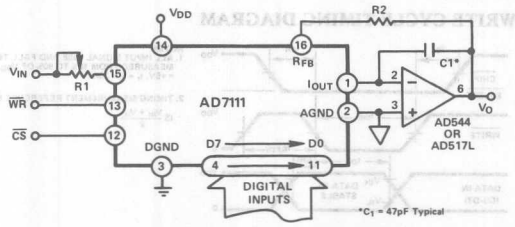


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C—see Figure 11. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 60pF to 185pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A converters" which is available from Analog Devices, Publication Number G479–15–8/78.

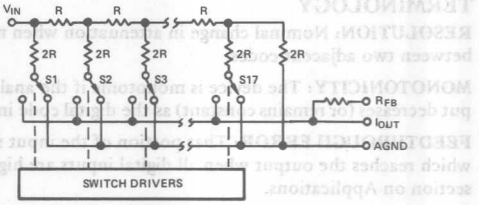


Figure 2. Simplified D/A Circuit of AD7111

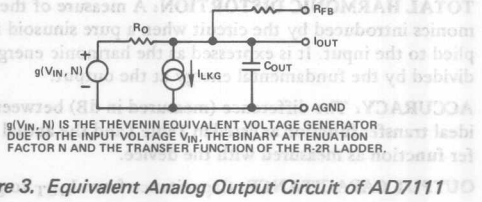


Figure 3. Equivalent Analog Output Circuit of AD7111

D7–D4 \ D3–D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Table I. Ideal Attenuation in dB vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7111 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7111 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

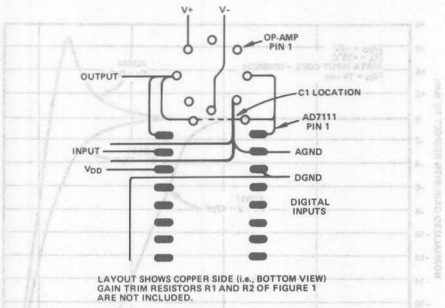


Figure 4. Suggested Layout for AD7111 and Op-Amp

It is recommended that when using the AD7111 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7111 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

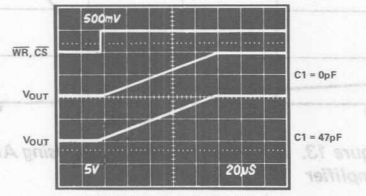


Figure 5. Response of AD7111 with AD517

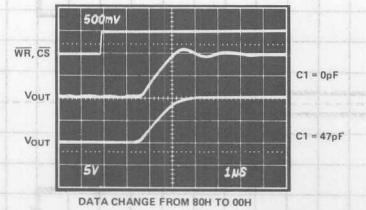


Figure 6. Response of AD7111 with AD544

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111 has been designed to minimize these glitches as much as possible.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 12. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7111 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7111 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7111 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7111 D/A converter circuit results in a constant attenuation error over the whole range. The AD7111 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors—R1 and R2 in Figure 1—can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00000000. The accuracy and monotonic range specifications of the AD7111 are not affected in any way by this gain trim procedure. For the AD7111L/C/U grades, suitable values for R1 and R2 of Figure 1 are R1 = 500Ω, R2 = 180Ω; for the K/B/T grades suitable values are R1 = 1000Ω, R2 = 270Ω. For additional information on gain error the reader is referred to Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices Inc., Publication Number E630–10–6/81.

AD7111 —Typical Performance Characteristics

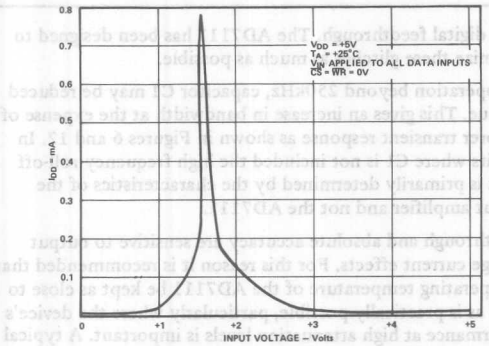


Figure 7. Typical Supply Current vs. Logic Input Level

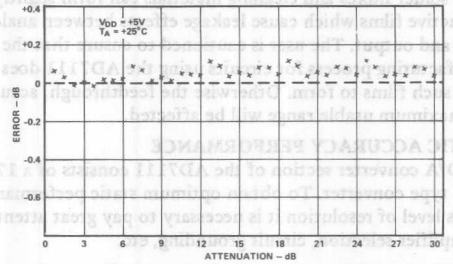


Figure 8. Typical Attenuation Error for 0.75dB Steps

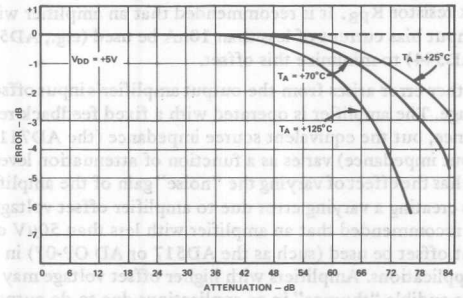


Figure 9. Typical Attenuation Error for 3dB Steps vs. Temperature

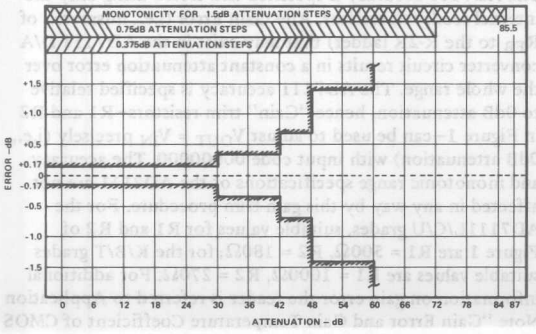


Figure 10. Accuracy Specification for K/B/T Grade Devices at T_A = +25°C

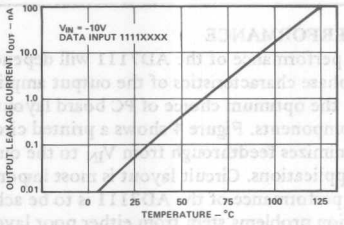


Figure 11. Output Leakage Current vs. Temperature

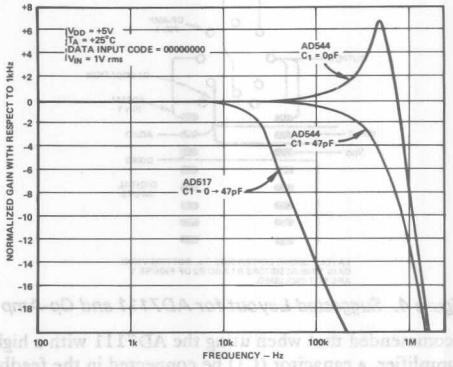


Figure 12. Frequency Response with AD544 and AD517 Amplifiers

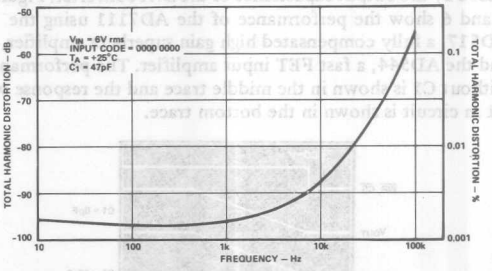


Figure 13. Distortion vs. Frequency Using AD544 Amplifier

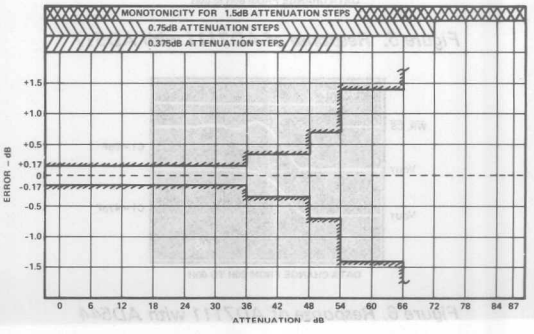


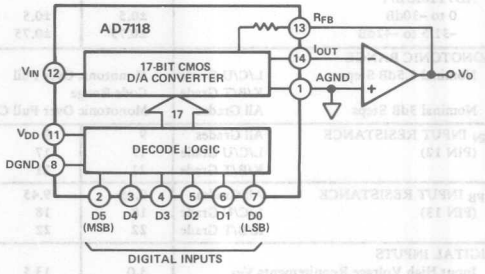
Figure 14. Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

LOGDAC
CMOS Logarithmic D/A Converter
AD7118*

FEATURES
- Dynamic Range 85.5dB
- Resolution 1.5dB
- Full ±25V Input Range Multiplying DAC
- Full Military Temperature Range –55°C to +125°C
- Low Distortion
- Low Power Consumption
- Latch Proof Operation (Schottky Diodes Not Required)
- Single 5V to 15V Supply

APPLICATIONS
- Digitally Controlled AGC Systems
- Audio Attenuators
- Wide Dynamic Range A/D Converters
- Sonar Systems
- Function Generators

FUNCTIONAL DIAGRAM

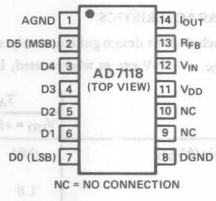


GENERAL DESCRIPTION

The LOGDAC™ AD7118 is a CMOS multiplying D/A converter which attenuates an analog input signal over the range 0 to −85.5dB in 1.5dB steps. The analog output is determined by a six-bit attenuation code applied to the digital inputs. Operating frequency range of the device is from dc to several hundred kHz.

The device is manufactured using an advanced monolithic silicon gate thin-film on CMOS process and is packaged in a 14-pin dual-in-line package.

PIN CONFIGURATION (Not to Scale)



NC = NO CONNECTION

ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option[1]
AD7118KN	0 to +70°C	0 to 42dB	N-16
AD7118LN	0 to +70°C	0 to 48dB	N-16
AD7118BQ	−25°C to +85°C	0 to 42dB	Q-16
AD7118CQ	−25°C to +85°C	0 to 48dB	Q-16
AD7118TQ[2]	−55°C to +125°C	0 to 42dB	Q-16
AD7118UQ[2]	−55°C to +125°C	0 to 48dB	Q-16

NOTES
[1]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number.

*Protected by U.S. Patent No. 4521,764.
LOGDAC is a trademark of Analog Devices, Inc.

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	TEST CONDITIONS/ COMMENTS
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
NOMINAL RESOLUTION		1.5	1.5	1.5	1.5	dB	
ACCURACY RELATIVE TO V_{IN}							
AD7118L/C/U							
0 to –30dB		±0.35	±0.35	±0.4	±0.4	dB max	Accuracy is measured using
–31.5 to –42dB		±0.7	±0.5	±0.8	±0.7	dB max	circuit of Figure 1 and includes
–43.5 to –48dB		±1.0	±0.7	±1.3	±1.0	dB max	any effects due to mismatch
AD7118K/B/T							between R_{FB} and the R-2R
0 to –30dB		±0.5	±0.5	±0.5	±0.5	dB max	ladder circuit.
–31.5 to –42dB		±0.75	±0.75	±1.0	±0.8	dB max	
MONOTONIC RANGE							
Nominal 1.5dB Steps	L/C/U Grade	Monotonic Over Full		0 to –72	0 to –72	dB	Digital Inputs 000000 to 110000
	K/B/T Grade	Code Range		0 to –66	0 to –66	dB	Digital Inputs 000000 to 101100
Nominal 3dB Steps	All Grades	Monotonic Over Full Code Range					
V_{IN} INPUT RESISTANCE	All Grades	9	9	9	9	kΩ min	
(PIN 12)	L/C/U Grade	17	17	17	17	kΩ max	
	K/B/T Grade	21	21	21	21	kΩ max	
R_{FB} INPUT RESISTANCE	All Grades	9.45	9.45	9.45	9.45	kΩ min	
(PIN 13)	L/C/U Grade	18	18	18	18	kΩ max	
	K/B/T Grade	22	22	22	22	kΩ max	
DIGITAL INPUTS							
Input High Voltage Requirements V_{IH}		3.0	13.5	3.0	13.5	V min	
Input Low Voltage Requirements V_{IL}		0.8	1.5	0.8	1.5	V max	
Input Leakage Current		±1	±1	±10	±10	μA max	Digital Inputs = V_{DD}
POWER SUPPLY							
V_{DD} for Specified Accuracy		5	–	5	–	V min	
		–	15	–	15	V max	
I_{DD}		0.5	1	1	2	mA max	Digital Inputs = 0V or V_{DD} (See Figure 7)

Specifications subject to change without notice.

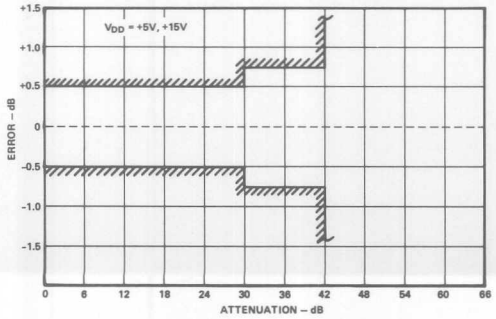
AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.

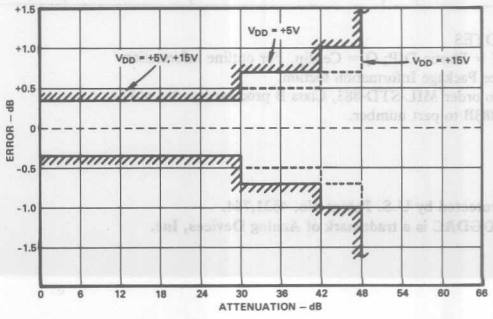
V_{DD} = +5V or +15V, V_{IN} = –10V except where stated, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated.

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$		0.01	0.005	0.01	0.005	dB per % max	ΔV_{DD} = ±10%, Input code = 100000
Propagation Delay		1.8	0.4	2.2	0.5	μs max	Full Scale Change
Digital to Analog Glitch Impulse		225	1200	–	–	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 100000 to 000000. C1 of Figure 1 is 0pF.
Output Capacitance (Pin 14)		100	100	100	100	pF max	
Input Capacitance Pin 12 and Pin 13		7	7	7	7	pF max	
Feedthrough at 1kHz	L/C/U Grade	–86	–86	–68	–68	dB max	Feedthrough is also deter-
	K/B/T Grade	–80	–80	–63	–63	dB max	mined by circuit layout
Total Harmonic Distortion		–85	–85	–85	–85	dB typ	V_{IN} = 6V rms
Intermodulation Distortion		–79	–79	–79	–79	dB typ	per DIN 45403 Blatt 4
Output Noise Voltage Density		70	70	70	70	$nV/\sqrt{Hz}$ max	Includes AD544 amplifier noise
Digital Input Capacitance		7	7	7	7	pF max	

Specifications subject to change without notice.



Accuracy Specification for K/B/T Grade Devices at T_A = +25°C



Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND) . . . . . +17V
V_{IN} (to AGND) . . . . . ±35V
Digital Input Voltage to DGND . . . . . −0.3V to V_{DD} +0.3V
I_{OUT} to AGND . . . . . −0.3V to V_{DD}
AGND to DGND . . . . . 0 to V_{DD}
DGND to AGND . . . . . 0 to V_{DD}
Power Dissipation (Any Package)
To +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 6mW/°C

Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periodsmay affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: Is a measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

ACCURACY: Is the difference (measured in dB) between the ideal transfer function as listed in Table 1 and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

INTERMODULATION DISTORTION: Is a measure of the interaction w hich takes place within the circuit between two sinusoids applied simultaneously to the input.

The reader is referred to Hewlett Packard Application Note 192 for further information.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7118 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital input logic. The logic translates the 6-bit binary input into a 17-bit word which is used to drive the D/A converter. Table I gives the nominal output voltages (and levels relative to 0dB = 10V) for all possible input codes. The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \left\{\frac{1.5N}{20}\right\}$$

$$\text{or } \left|\frac{V_O}{V_{IN}}\right|_{dB} = -1.5N$$

where N is the binary input for values 0 to 57. For $60 \leqslant N \leqslant 63$ the output is zero. See note 3 at bottom of Table 1.

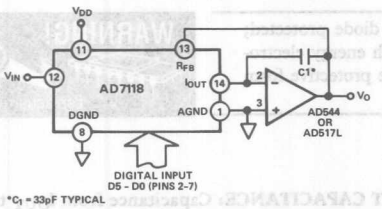


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7118 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, roughly doubles every 10°C—see Figure 10. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 12kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 50pF to 80pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Publication Number G479—15—8/78.

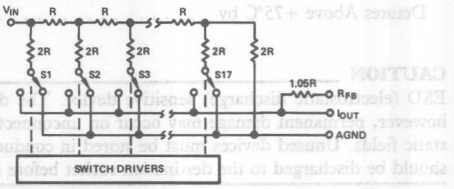


Figure 2. Simplified D/A Circuit of AD7118

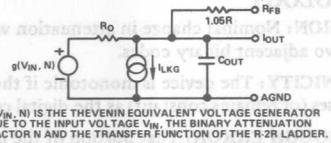


Figure 3. Equivalent Analog Output Circuit of AD7118

N	Digital Input D5 D0	Attenuation dB	V_{OUT}[1]	N	Digital Input	Attenuation	V_{OUT}[1]
0	00 00 00	0.0	10.00	31	01 11 11	46.5	0.0473
1	00 00 01	1.5	8.414	32	10 00 00	48.0	0.0398
2	00 00 10	3.0	7.079	33	10 00 01	49.5	0.0335
3	00 00 11	4.5	5.957	34	10 00 10	51.0	0.0282
4	00 01 00	6.0	5.012	35	10 00 11	52.5	0.0237
5	00 01 01	7.5	4.217	36	10 01 00	54.0	0.0200
6	00 01 10	9.0	3.548	37	10 01 01	55.5	0.0168
7	00 01 11	10.5	2.985	38	10 01 10	57.0	0.0141
8	00 10 00	12.0	2.512	39	10 01 11	58.5	0.0119
9	00 10 01	13.5	2.113	40	10 10 00	60.0	0.0100
10	00 10 10	15.0	1.778	41	10 10 01	61.5	0.00841
11	00 10 11	16.5	1.496	42	10 10 10	63.0	0.00708
12	00 11 00	18.0	1.259	43	10 10 11	64.5	0.00596
13	00 11 01	19.5	1.059	44	10 11 00	66.0	0.00501
14	00 11 10	21.0	0.891	45	10 11 01	67.5	0.00422
15	00 11 11	22.5	0.750	46	10 11 10	69.0	0.00355
16	01 00 00	24.0	0.631	47	10 11 11	70.5	0.00299
17	01 00 01	25.5	0.531	48	11 00 00	72.0	0.00251
18	01 00 10	27.0	0.447	49	11 00 01	73.5	0.00211
19	01 00 11	28.5	0.376	50	11 00 10	75.0	0.00178
20	01 01 00	30.0	0.316	51	11 00 11	76.5	0.00150
21	01 01 01	31.5	0.266	52	11 01 00	78.0	0.00126
22	01 01 10	33.0	0.224	53	11 01 01	79.5	0.00106
23	01 01 11	34.5	0.188	54	11 01 10	81.0	0.000891
24	01 10 00	36.0	0.158	55	11 01 11	82.5	0.000750
25	01 10 01	37.5	0.133	56	11 10 00	84.0	0.000631
26	01 10 10	39.0	0.112	57	11 10 01	85.5	0.000531
27	01 10 11	40.5	0.0944	58	11 10 10	87.0	0.000447
28	01 11 00	42.0	0.0794	59	11 10 11	88.5	0.000376
29	01 11 01	43.5	0.0668				
30	01 11 10	45.0	0.0562	60	11 11 XX[2]	∞	

NOTES
[1] V_{IN} = −10V dc
[2] X = 1 or 0. Output is fully muted for N>60
[3] Monotonic operation is not guaranteed for N = 58, 59

Table I. Ideal Attenuation vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7118 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7118 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

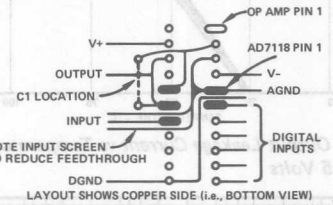


Figure 4. Suggested Layout for AD7118 and Op Amp

It is recommended that when using the AD7118 with a high speed amplifier, a capacitor C1 be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7118 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

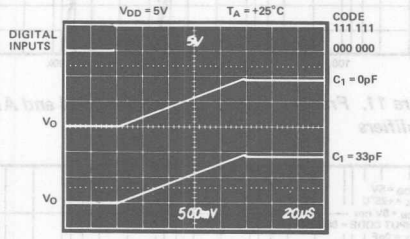


Figure 5. Response of AD7118 with AD517L

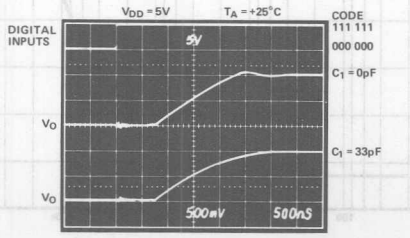


Figure 6. Response of AD7118 with AD544S

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7118 has been designed to minimize these glitches as much as possible. It is recommended that for minimum glitch energy the AD7118 be operated with V_{DD} = 5V. This will reduce the available energy for coupling across the parasitic capacitance. It should be noted that the accuracy of the AD7118 improves as V_{DD} is increased (see Figure 8) but the device maintains monotonic behavior to at least –66dB in the range $5 \leqslant V_{DD} \leqslant 15$ volts.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 11. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7118.

Feedthrough and absolute accuracy for attenuation levels beyond 42dB are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7118 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 10.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7118 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7118 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7118 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. To achieve an output offset error less than one half the smallest step size, it is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07).

If dc accuracy is not critical in the application, it should be noted that amplifiers with offset voltage up to approximately 2 millivolts can be used. Amplifiers with higher offset voltage may cause audible "thumps" due to dc output changes.

The AD7118 accuracy is specified and tested using only the internal feedback resistor. It is not recommended that "gain" trim resistors be used with the AD7118 because the internal logic of the circuit executes a proprietary algorithm which approximates a logarithmic curve with a binary D/A converter: as a result no single point on the attenuator transfer function can be guaranteed to lie exactly on the theoretical curve. Any "gain-error" (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7118 D/A converter circuit results in a constant attenuation error over the whole range. Since the gain-error of CMOS multiplying D/A converters is normally less than 1%, the accuracy error contribution due to "gain-error" effects is normally less than 0.09dB.

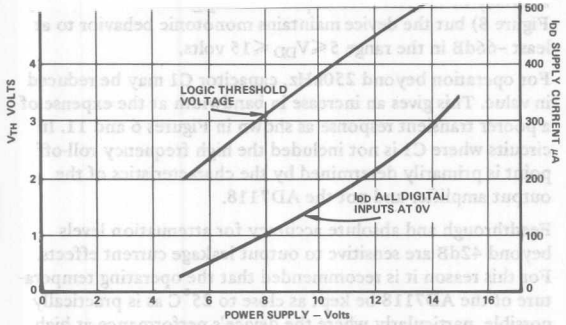


Figure 7. Digital Threshold & Power Supply Current vs Power Supply

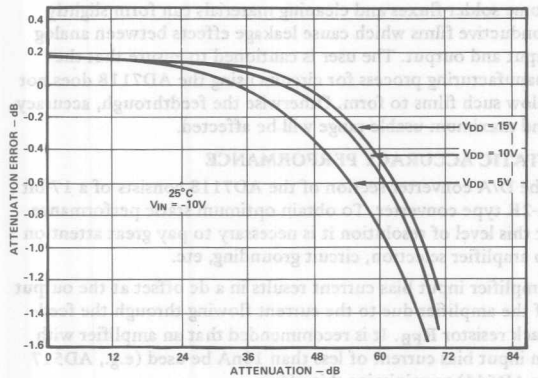


Figure 8. DC Attenuation Error vs. Attenuation & V_{DD}

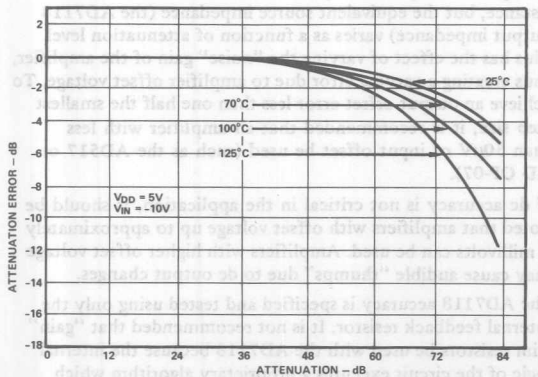


Figure 9. DC Attenuation Error vs. Attenuation & Temperature

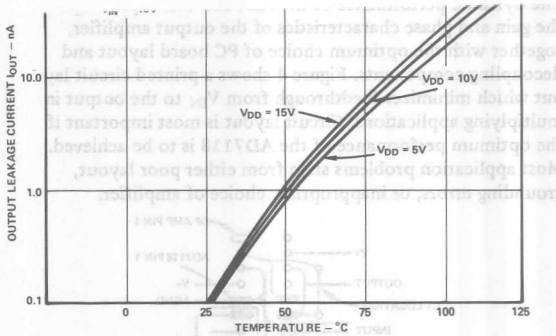


Figure 10. Output Leakage Current vs Temperature at V_{DD} = 5, 10 and 15 Volts

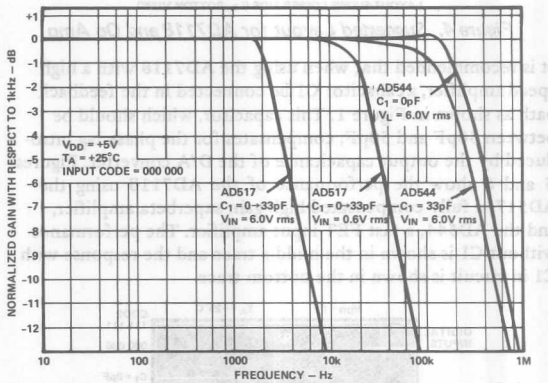


Figure 11. Frequency Response with AD544 and AD517 Amplifiers

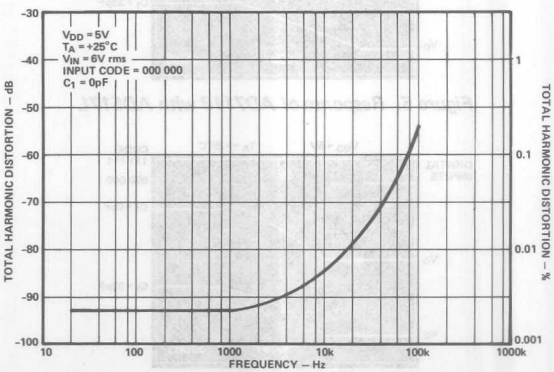


Figure 12. Distortion vs. Frequency Using AD544 Amplifier

ANALOG DEVICES

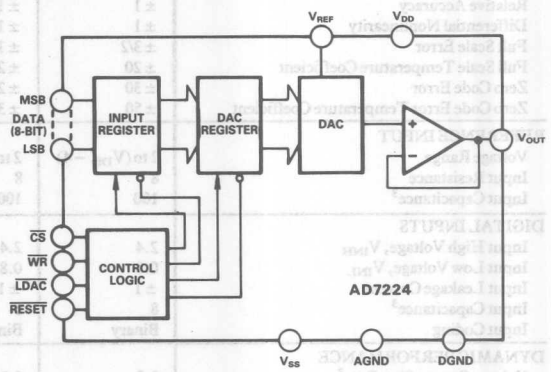
LC²MOS 8-Bit DAC With Output Amplifier

AD7224

FEATURES

8-Bit CMOS DAC with Output Amplifier
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less than 1 LSB Over Temperature
Extended Temperature Range Operation
µP-Compatible with Double Buffered Input
Standard 18-Pin DIPs and 20-Terminal Surface Mount Package and SOIC Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7224 is a precision 8-bit, voltage-output, digital-to-analog converter with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers– an input register and a DAC register. Only the data held in the DAC register determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224's. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35mW typical with single supply).
2. Low Total Unadjusted Error
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process, coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1LSB over the full operating temperature range.
3. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

AD7224—SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 11.4V to 16.5V, V_{SS} = −5V ± 10%; AGND = DGND = 0V; V_{REF} +2V to (V_{DD} −4V)[1] unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±3/2	±1	LSB max	
Full Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	μV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/μs min	
Voltage Output Settling Time[3]				
Positive Full Scale Change	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	7	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4]				
t_1				
@25°C	150	150	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_2				
@25°C	150	150	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	100	100	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error[3]	±2	±2	LSB max	
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[4]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2	2	V/μs min	
Voltage Output Settling Time[4]				
Positive Full Scale Change	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	20	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4]				
t_1				
@25°C	150	150	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_2				
@25°C	150	150	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	100	100	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +24V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commerical (K, L Versions) . . . . . −40°C to +85°C
Industrial (B, C Versions) . . . . . −40°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTES
[1]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7224KN	−40°C to +85°C	±2 max	N-18
AD7224LN	−40°C to +85°C	±1 max	N-18
AD7224KP	−40°C to +85°C	±2 max	P-20A
AD7224LP	−40°C to +85°C	±1 max	P-20A
AD7224KR-1	−40°C to +85°C	±2 max	R-20
AD7224LR-1	−40°C to +85°C	±1 max	R-20
AD7224BQ	−40°C to +85°C	±2 max	Q-18
AD7224CQ	−40°C to +85°C	±1 max	Q-18
AD7224TQ	−55°C to +125°C	±2 max	Q-18
AD7224UQ	−55°C to +125°C	±1 max	Q-18
AD7224TE	−55°C to +125°C	±2 max	E-20A
AD7224UE	−55°C to +125°C	±1 max	E-20A

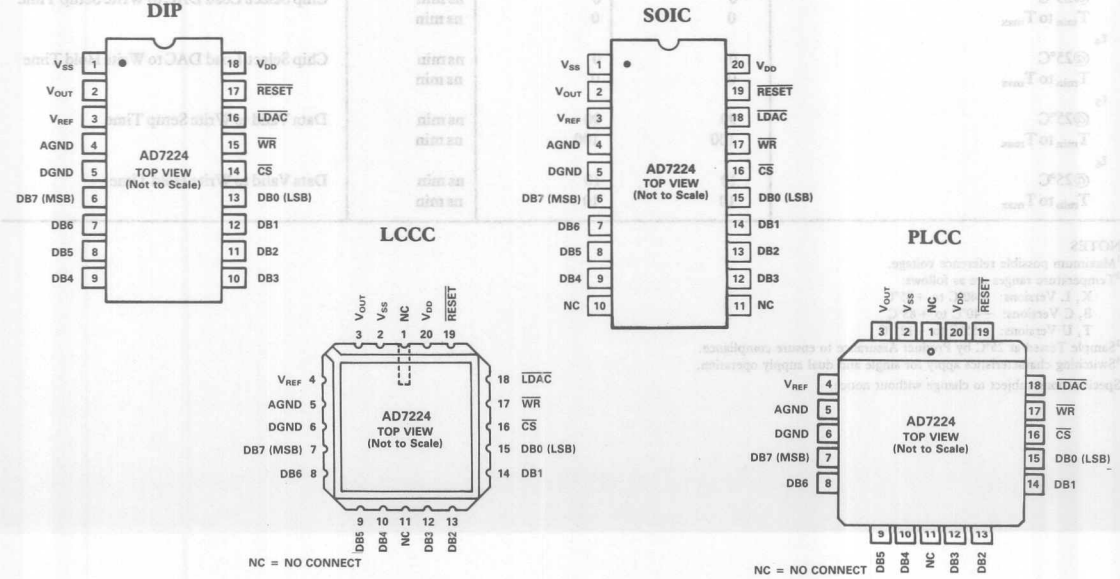
NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN CONFIGURATIONS



TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full scale error, relative accuracy and zero code error. Maximum output voltage is V_{REF} – 1LSB (ideal) where 1LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error, relative to LSB size, will increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero code error and full scale error and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output due to a change in the digital input code. It is specified in nV secs and is measured at V_{REF} = 0V.

FULL SCALE ERROR

Full Scale Error is defined as:
Measured Value – Zero Code Error – Ideal Value

CIRCUIT INFORMATION

D/A SECTION

The AD7224 contains an 8-bit voltage-mode digital-to-analog converter. The output voltage from the converter has the same polarity as the reference voltage allowing single supply operation. A novel DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2V to +12.5V.

The DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS single pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

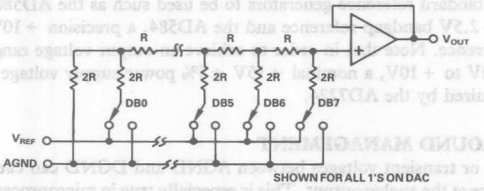


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and can vary from 8kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminal is also code dependent and typically varies from 25pF to 50pF.

The V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUT} = D \cdot V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

OP-AMP SECTION

The voltage-mode D/A converter output is buffered by a unity gain non-inverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF.

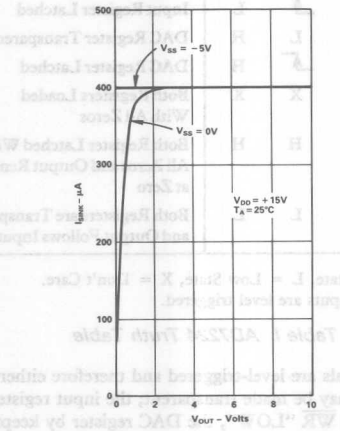


Figure 2. Variation of I_{SINK} with V_{OUT}

The AD7224 can be operated single or dual supply resulting in different performance in some parameters from the output amplifier. In single supply operation (V_{SS} = 0V = AGND) the sink capability of the amplifier, which is normally 400µA, is reduced as the output voltage nears AGND. The full sink capability of 400µA is maintained over the full output voltage range by tying V_{SS} to –5V. This is indicated in Figure 2.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

Additionally, the negative V_{SS} gives more head-room to the output amplifier which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7224 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode

between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

Table I shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input register to the DAC register. Only the data held in the DAC register will determine the analog output of the converter.

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
↓	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care.
All control inputs are level triggered.

Table I. AD7224 Truth Table

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW". Input data is latched on the rising edge of $\overline{WR}$.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line functions like a zero override with the output brought to 0V for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on $\overline{RESET}$ will latch all 0's into the registers and the output remains at 0V after the $\overline{RESET}$ line has returned "HIGH". The $\overline{RESET}$ line can be used to ensure power-up to 0V on the AD7224 output and is also useful, when used as a zero override, in system calibration cycles. Figure 3 shows the input control logic for the AD7224.

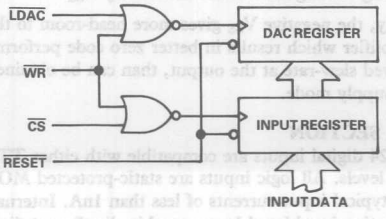
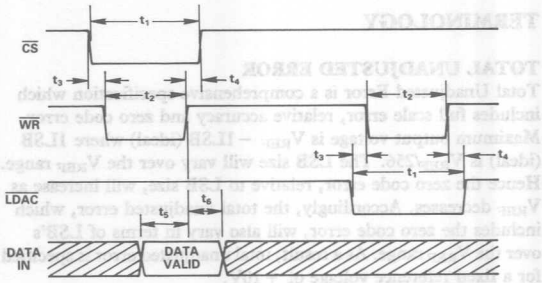


Figure 3. Input Control Logic



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}. $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$

Figure 4. Write Cycle Timing Diagram

SPECIFICATION RANGES

For the DAC to maintain specified accuracy, the reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

With dual supply operation, the AD7224 has an extended V_{DD} range from +12V ±5% to +15V ±10% (i.e., from +11.4V to +16.5V). Operation is also specified for a single V_{DD} power supply of +15V ±5%.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} −4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that in order to achieve an output voltage range of 0V to +10V, a nominal +15V ±5% power supply voltage is required by the AD7224.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7224. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7224 AGND and DGND pins (IN914 or equivalent).

Applying the 7224

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7224, with the output voltage having the same positive polarity as V_{REF}. The AD7224 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 5. The voltage at V_{REF} must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

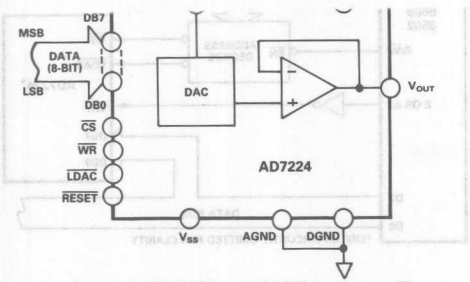


Figure 5. Unipolar Output Circuit

DAC Register Contents MSB LSB	Analog Output, V_{OUT}
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

The AD7224 can be configured to provide bipolar output operation using one external amplifier and two resistors. Figure 6 shows a circuit used to implement offset binary coding. In this case

$$V_O = \left(1 + \frac{R2}{R1}\right) \cdot (D\ V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_O = (2D - 1) \cdot V_{REF}$$

where D is a fractional representation of the digital word in the DAC register.

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature. Once again, the AD7224 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 6 with R1 = R2.

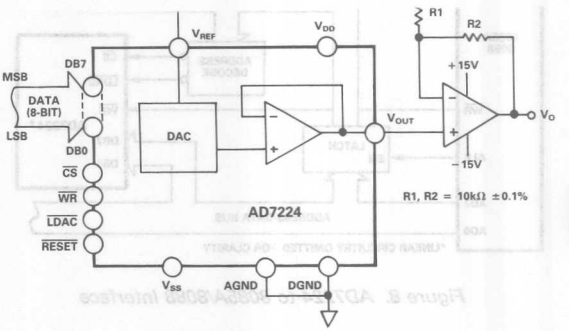


Figure 6. Bipolar Output Circuit

DAC Register Contents MSB LSB	Analog Output, V_O
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7224 AGND pin can be biased above system GND (AD7224 DGND) to provide an offset "zero" analog output voltage level. Figure 7 shows a circuit configuration to achieve this. The output voltage, V_{OUT}, is expressed as:

$$V_{OUT} = V_{BIAS} + D \cdot (V_{IN})$$

where D is a fractional representation of the digital word in the DAC register and can vary from 0 to 255/256.

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

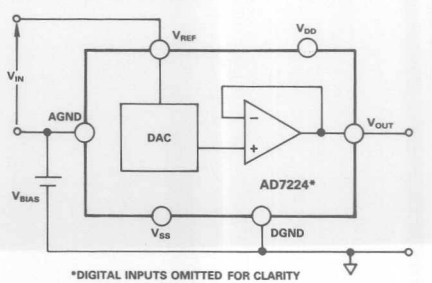


Figure 7. AGND Bias Circuit

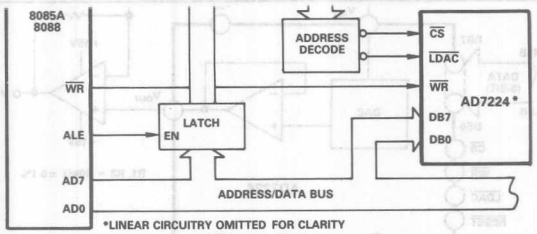


Figure 8. AD7224 to 8085A/8088 Interface

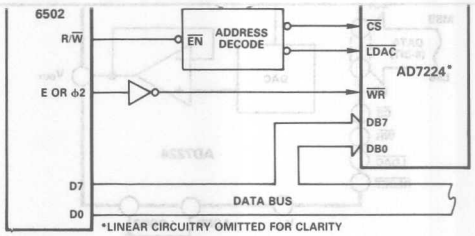


Figure 9. AD7224 to 6809/6502 Interface

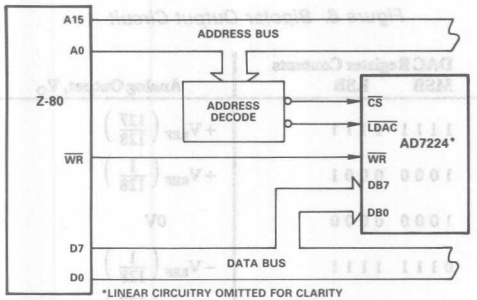


Figure 10. AD7224 to Z-80 Interface

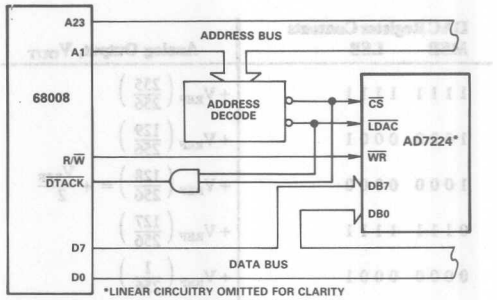


Figure 11. AD7224 to 68008 Interface

8-Bit CMOS D/A Converter with Voltage Output

PM-7224

FEATURES

- Internal Output Amplifier
- Double-Buffered Data Inputs
- Microprocessor Compatible
- Adjustment Free (±1/2 LSB Total Error)
- Guaranteed Monotonicity
- Single or Dual Supply Operation
- Space Saving 0.3" Wide 18-Pin DIP
- TTL/5V CMOS Compatible
- Fast Data Load, t_{WR} = 90ns (All Temperatures)
- Single Specification Table for Both Dual and Single Power Supply Operation
- Available in Die Form

APPLICATIONS

- Process/Industrial Controls
- Automatic Test Equipment
- Op Amp Offset Adjust
- Gain Adjust
- Attenuation
- Medical Equipment

ORDERING INFORMATION †

TOTAL UNADJUSTED ERROR	PACKAGE: MILITARY* TEMPERATURE	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE	PACKAGE: COMMERCIAL TEMPERATURE
±1/2 LSB	PM7224AX	PM7224EX	PM7224GP
±1 LSB	PM7224BX	PM7224FX	–
±1 LSB	PM7224BRC/883	PM7224FS	–
±1 LSB	–	PM7224FPC	–
±1 LSB	–	PM7224FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

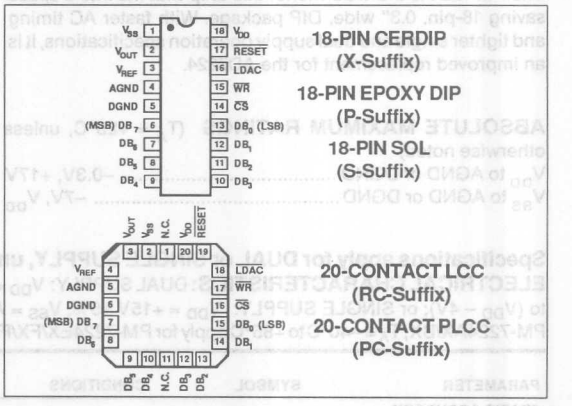
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7224AX	AD7224UQ	MIL
PM7224BX	AD7224TQ	
PM7224EX	AD7224CQ	IND
PM7224FX	AD7224BQ	
PM7224GP	AD7224LN	COM
PM7224FPC	AD7224KP	
PM7224FP	AD7224KN	

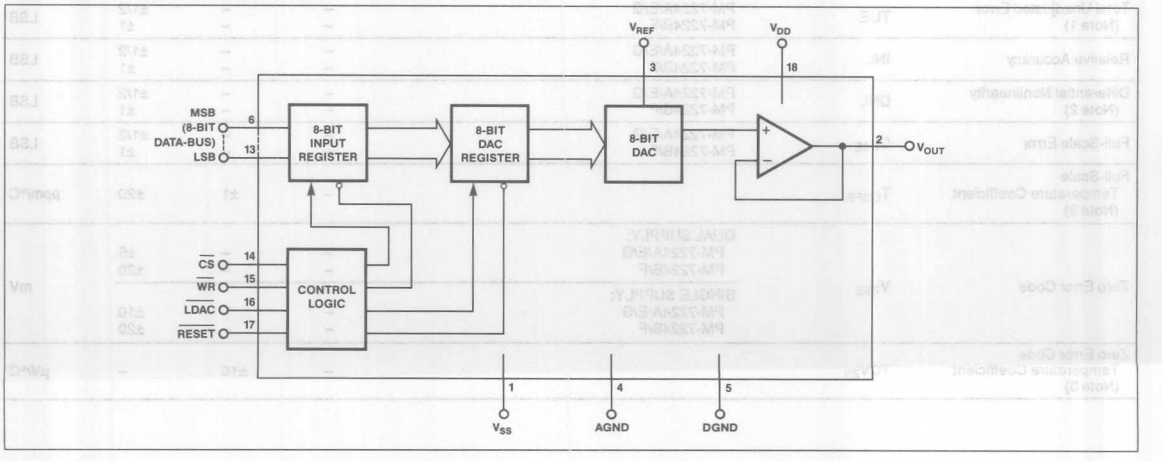
GENERAL DESCRIPTION

The PM-7224 is an improved version of the AD7224, which is an 8-bit, double-buffered, voltage output, CMOS digital-to-analog converter. It consists of a CMOS output amplifier, two 8-bit registers, interface control logic, and an R-2R resistor ladder network on a single monolithic chip.

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM



PC board-space and costs are greatly reduced by eliminating the need for an external amplifier and associated trim circuitry.

Excellent zero code error is achieved for both single and dual supply operation by laser trimming the offset during manufacturing. The internal amplifier can deliver up to 5mA into a 2kΩ load and can drive a 3300pF capacitive load.

A reset pin simplifies system power-up and/or calibration cycles. It allows the DAC to momentarily be reset to 0V and function like a zero-override when both registers are transparent; however, the DAC output will remain at 0V when both registers are latched.

The PM-7224 can be operated with either a single or dual supply; however, zero code error can be improved using dual supplies.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7224's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly-stable thin-film R-2R resistor ladder, aids in the PM-7224's excellent full-scale and zero-code error temperature coefficients. It also results in an inherently reliable DAC and output amplifier.

The PM-7224 is a CMOS monolithic chip that fits into a space saving 18-pin, 0.3" wide, DIP package. With faster AC timing and tighter single and dual supply operation specifications, it is an improved replacement for the AD7224.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to AGND or DGND ..... –0.3V, +17V
V_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3, V_{DD}
Digital Input Voltage to DGND ..... –0.3V, V_{DD}
V_{REF} to AGND ..... –0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature
  Military, AX/BX ..... –55°C to +125°C
  Extended Industrial, EX/FX/FP/FPC/FS ..... –40°C to +85°C
  Commercial, GP ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 5)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	84	15	°C/W
18-Pin Plastic DIP (P)	75	33	°C/W
20-Contact LCC (RC)	98	38	°C/W
18-Pin SOL (S)	89	27	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTES:
1. Outputs may be shorted to AGND provided the package power dissipation is not exceeded. Typical output short circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum ratings conditions for extended periods may affect device reliability.
5. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} – 4V); or SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; T_A = –55°C to +125°C apply for PM-7224AX/BX; T_A = –40°C to +85°C apply for PM-7224EX/FX/FP/FPC/FS; T_A = 0°C to +70°C for PM-7224GP, unless otherwise noted.

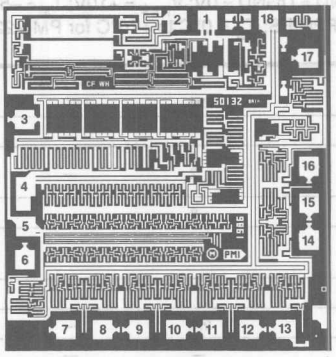
PARAMETER	SYMBOL	CONDITIONS	PM-7224 MIN	PM-7224 TYP	PM-7224 MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Relative Accuracy	INL	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Full-Scale Error	G_{FSE}	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Full-Scale Temperature Coefficient (Note 3)	T_{CGFS}		–	±1	±20	ppm/°C
Zero Error Code	V_{ZSE}	DUAL SUPPLY:				mV
		PM-7224A/E/G	–	–	±5	
		PM-7224B/F	–	–	±20	
		SINGLE SUPPLY:				
		PM-7224A/E/G	–	–	±10	
		PM-7224B/F	–	–	±20	
Zero Error Code Temperature Coefficient (Note 3)	TCV_{ZS}		–	±10	–	µV/°C

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.
ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} – 4V); or SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; T_A = –55°C to +125°C apply for PM-7224AX/BX; T_A = –40°C to +85°C apply for PM-7224EX/FX/FP/FPC/FS; T_A = 0°C to +70°C for PM-7224GP, unless otherwise noted. *Continued*

			PM-7224			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
REFERENCE INPUT						
Voltage Range (Note 4)		DUAL SUPPLY ONLY	2	—	(V_{DD} – 4)	V
Input Resistance	R_{IN}		8	—	—	kΩ
Input Capacitance (Note 3)	C_{IN}	Digital Inputs = all 1's	—	—	100	pF
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	—	—	V
Digital Input Low	V_{INL}		—	—	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	—	—	±1	μA
Input Capacitance (Note 3)	C_{IN}		—	—	8	pF
Input Coding				BINARY		
POWER SUPPLIES						
Power Supply Rejection Ratio	PSRR		—	—	0.005%	%/%
Positive Supply Current (Note 5)	I_{DD}	T_A = +25°C T_A = Full Temp Range	— —	— —	4 6	mA
Negative Supply Current (Note 5)	I_{SS}	DUAL SUPPLY ONLY T_A = +25°C T_A = Full Temp Range	— —	— —	3 5	mA
DYNAMIC PERFORMANCE						
V_{OUT} Slew Rate (Note 3)	SR		2.5	—	—	V/μS
V_{OUT} Settling Time Positive or Negative (Note 3, 6)	t_S		—	—	5	μS
Digital Feedthrough (Note 3)	Q		—	10	—	nVs
Minimum Load Resistance	$R_{L(MIN)}$	V_{OUT} = +10V	2	—	—	kΩ
SWITCHING CHARACTERISTICS (Note 3)						
Chip Select/Load DAC Pulse-Width	t_1		90	—	—	ns
Write/Reset Pulse-Width	t_2		90	—	—	ns
Chip Select/Load DAC to Write Setup Time	t_3		0	—	—	ns
Chip Select/Load DAC to Write Hold Time	t_4		0	—	—	ns
Data Valid to Write Setup Time	t_5		90	—	—	ns
Data Valid to Write Hold Time	t_6		10	—	—	ns

NOTES:
1. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
2. All devices guaranteed monotonic over the full operating temperature range.
3. Guaranteed by design and not subject to production test.
4. V_{DD} – 4 volts is the maximum reference voltage for the above specifications.
5. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
6. V_{REF} = +10V; to where output settles to 1/2 LSB.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.099 inch, 9306 sq. mils
(2.39 × 2.52 mm, 6.0 sq. mm)

1. V_{SS}
2. V_{OUT}
3. V_{REF}
4. AGND
5. DGND
6. DB7(MSB)
7. DB6
8. DB5
9. DB4
10. DB3
11. DB2
12. DB1
13. DB0(LSB)
14. $\overline{CS}$
15. $\overline{WR}$
16. $\overline{LDAC}$
17. $\overline{RESET}$
18. V_{DD}

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

WAFER TEST LIMITS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} − 4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise noted.

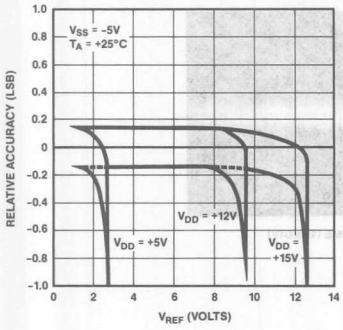
PARAMETER	SYMBOL	CONDITIONS	PM-7224GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits
Total Unadjusted Error (Note 1)	TUE		±1	LSB MAX
Relative Accuracy	INL		±1	LSB MAX
Differential Nonlinearity (Note 2)	DNL		±1	LSB MAX
Full Scale Error	G_{FSE}		±1	LSB MAX
Zero Code Error	V_{ZSE}		±20	mV MAX
REFERENCE INPUT				
Voltage Range (Note 3)	V_{REF}	DUAL SUPPLY ONLY	2 to (V_{DD} − 4V)	V
Reference Input Resistance	R_{IN}		8	kΩ MIN
DIGITAL INPUTS				
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Input Coding			BINARY	
POWER SUPPLIES				
Positive Supply Current (Note 4)	I_{DD}		4	mA MAX
Negative Supply Current (Note 4)	I_{SS}	DUAL SUPPLY ONLY	3	mA MAX

NOTES:
1. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
2. All dice guaranteed monotonic over the full operating temperature range.
3. V_{DD} − 4 volts is the maximum reference voltage for the above specifications.
4. V_{IN} = V_{INL} or V_{INH}; output unloaded.

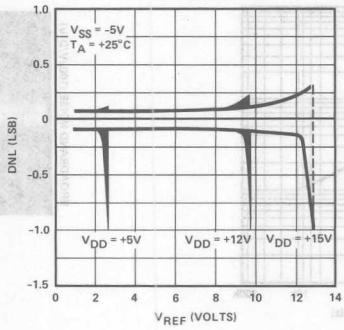
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

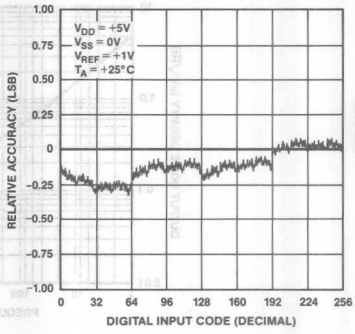
RELATIVE ACCURACY vs V_{REF}



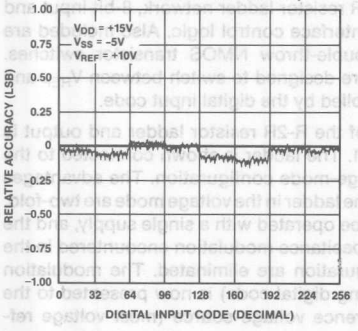
DIFFERENTIAL NONLINEARITY vs V_{REF}



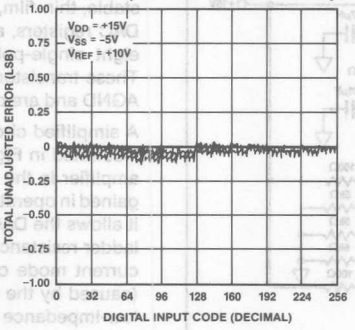
RELATIVE ACCURACY WITH SINGLE +5V SUPPLY



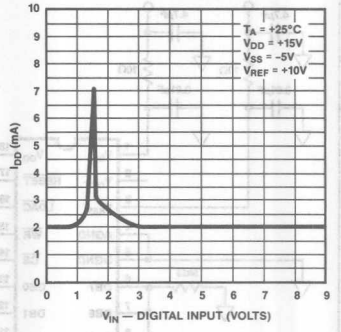
RELATIVE ACCURACY vs CODE AT T_A = -55°C, +25°C, +125°C (ALL SUPERIMPOSED)



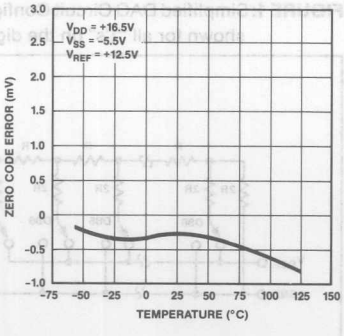
TOTAL UNADJUSTED ERROR vs CODE AT T_A = -55°C, +25°C, +125°C (ALL SUPERIMPOSED)



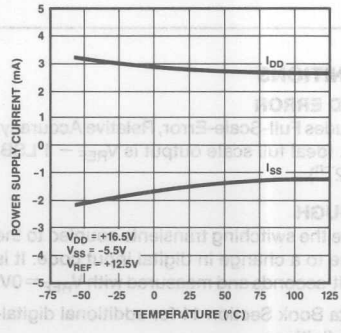
POSITIVE SUPPLY CURRENT (I_{DD}) vs LOGIC LEVEL



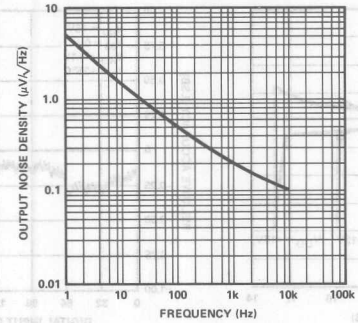
ZERO CODE ERROR vs TEMPERATURE



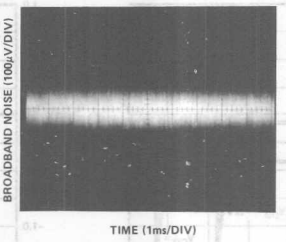
POWER SUPPLY CURRENT vs TEMPERATURE



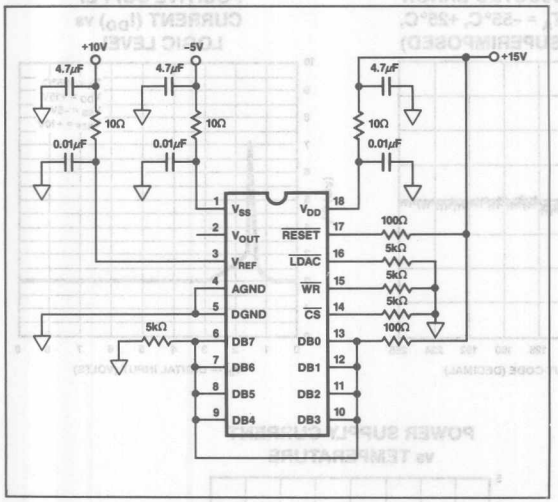
OUTPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



BROADBAND NOISE



BURN-IN CIRCUIT



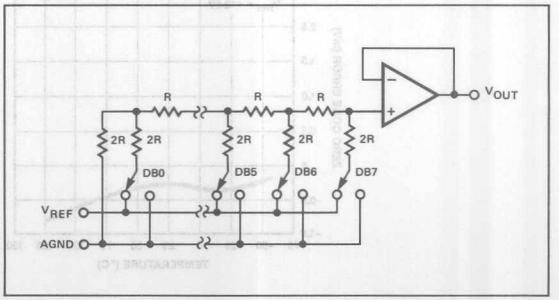
GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7224 contains an output buffer amplifier, a highly-stable, thin-film, R-2R resistor ladder network, 8-bit input and DAC registers, and interface control logic. Also included are eight single-pole double-throw NMOS transistor switches. These transistors were designed to switch between V_{REF} and AGND and are controlled by the digital input code.

A simplified circuit of the R-2R resistor ladder and output is illustrated in Figure 1. The ladder is shown connected to the amplifier in the voltage-mode configuration. The advantages gained in operating the ladder in the voltage mode are two-fold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low-impedance reference voltage source (most voltage reference output-impedances are low enough so that its output voltage will not be affected by the varying digital code). The

FIGURE 1: Simplified DAC Circuit Configuration. (Switches are shown for all "1's" on the digital inputs.)



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes Full-Scale-Error, Relative Accuracy, and Zero-Code-Error. Ideal full scale output is $V_{REF} - 1$ LSB, and 1 LSB is $V_{REF} \times (2^{-n})$.

DIGITAL FEEDTHROUGH

Digital feedthrough are the switching transients coupled to the output of the DAC due to a change in digital input code. It is expressed in nano-Volt-seconds and measured with $V_{REF} = 0V$.

Refer to PMI 1986 Data Book Section 11 for additional digital-to-analog converter definitions.

eliminated. Also, digital glitches fed through the switch capacitance to the output will be greatly reduced; it will be absorbed by the low output-impedance of the external reference resulting in a "cleaner" output voltage.

Figure 1 also shows the amplifier configured to operate as a buffer amplifier resulting in no signal inversion from input to output (V_{REF} to V_{OUT}). Also, note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section under AGND biasing.

For proper operation, maximum V_{REF} should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The voltage output equation is given by:

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

The R-2R resistor ladder network has a typical resistance of 10kΩ; a 100kΩ load would cause a 23 LSB gain error. Therefore, in order to drive a 2kΩ load, the R-2R ladder was terminated with a stable CMOS buffer amplifier. The amplifier can drive 10 volts across a 2kΩ load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7224's output can also withstand an indefinite short-circuit to AGND to typically 50mA. The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

The amplifier's output stage is an intrinsic NPN bipolar transistor. It is derived from the P^- well and the substrate. This transistor provides a low-impedance high-output current capability using only a small part of the chip area. The emitter of this NPN transistor is loaded with a 400μA NMOS current-source referenced to V_{SS}. This current is sunk into the negative supply allowing the amplifier's output to go directly to ground.

A simplified schematic of the output amplifier is shown in Figure 2. It shows the current-source connection between the NPN output transistor's emitter and V_{SS}. Figure 3 depicts a typical plot for the dual and single supply current sink capability of the DAC versus output voltage. Let's take a closer look at what happens to its behavior by referring to Figures 2 and 3.

It can be seen that with dual supplies the current-source is still in its high impedance (saturation) state when the output reaches 0 volts. This is due to the 5 volts (V_{SS}) across the current-source that is sinking the 400μamps. When $V_{SS} = 0$ volts, however, the current sink capability is reduced as the output voltage approaches 0 volts; the current-source is coming out of its saturation region and starts appearing resistive.

The amplifier's current-limiting and buffering abilities are achieved with an NMOS transistor and a series resistor, see the resistor and output transistor.

The amplifier's internal gain stages were designed so that they maintain sufficient gain over its common mode range; this results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The amplifier's offset is included in the data sheet under "total unadjusted error" specification.

2

FIGURE 2: Amplifier Output Stage

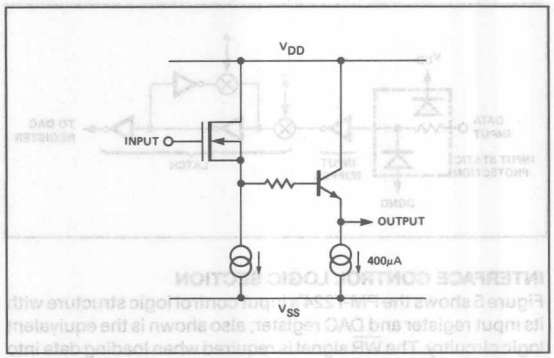
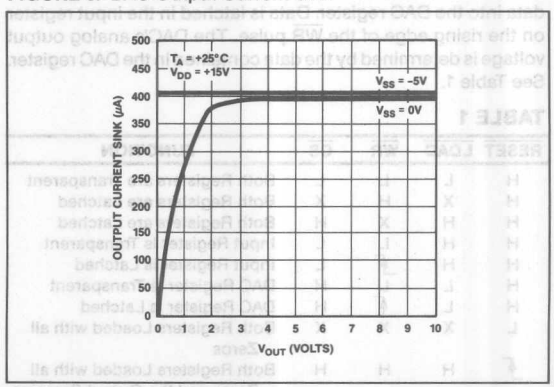


FIGURE 3: DAC Output Current Sink



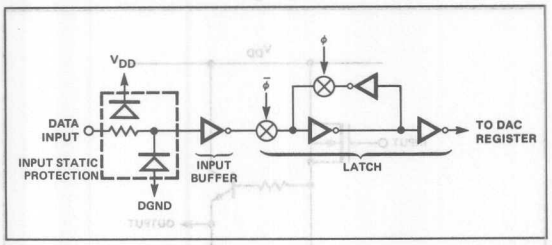
DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed to convert TTL and 5V CMOS input logic levels into CMOS levels to drive the internal circuitry. A simple internal 5V regulator is used to ensure the high speed timing requirements.

The PM-7224's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. As shown in Figure 4, these inputs are protected from electrostatic-discharge and build-up with two internal distributed-diodes; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

Figure 4 also shows the equivalent logic circuit for the digital data input register structure. This circuit drives the DAC register. The digital controls ϕ and $\bar{\phi}$ shown are controlled by the external $\overline{WR}$, and $\overline{CS}$ signals.

FIGURE 4: Input Register Structure



INTERFACE CONTROL LOGIC SECTION

Figure 5 shows the PM-7224's input control logic structure with its input register and DAC register; also shown is the equivalent logic circuitry. The $\overline{WR}$ signal is required when loading data into either register and is used in conjunction with either $\overline{CS}$ or $\overline{LDAC}$. $\overline{CS}$ loads data into the input register, and $\overline{LDAC}$ loads data into the DAC register. Data is latched in the input register on the rising edge of the $\overline{WR}$ pulse. The DAC's analog output voltage is determined by the data contained in the DAC register. See Table 1.

TABLE 1

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register is Transparent
H	H	↓	L	Input Register is Latched
H	L	L	H	DAC Register is Transparent
H	L	↓	H	DAC Register is Latched
L	X	X	X	Both Registers Loaded with all Zeros
↓	H	H	H	Both Registers Loaded with all Zeros and the Output Remains at Zero
↓	L	L	L	Both Registers are Transparent (output follows the input)

H = High State; L = Low State; X = Don't Care

Table 1 shows that the DAC is transparent when $\overline{WR}$, $\overline{CS}$, and $\overline{LDAC}$ are low, and the input register is transparent when $\overline{WR}$ and $\overline{CS}$ only are low. Also shown is the data being latched into the input register on the rising edge of the $\overline{WR}$ signal.

Also provided with the PM-7224 is a $\overline{RESET}$ pin as shown in Figure 5. A low $\overline{RESET}$ signal will reset both registers to zero. If the DAC is in the transparent mode, the DAC output will go to 0V for as long as the reset line remains low. If the DAC is in the latched mode, the output will go to 0V (and remain there) on the rising edge of the reset signal.

Figure 6 shows the PM-7224 write timing diagram.

FIGURE 5: Input Control Logic

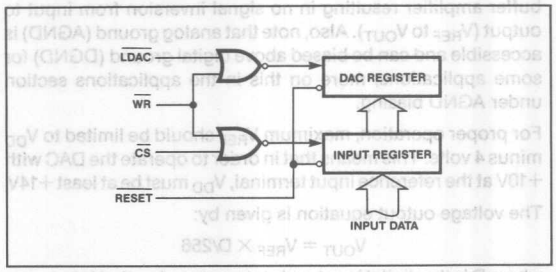
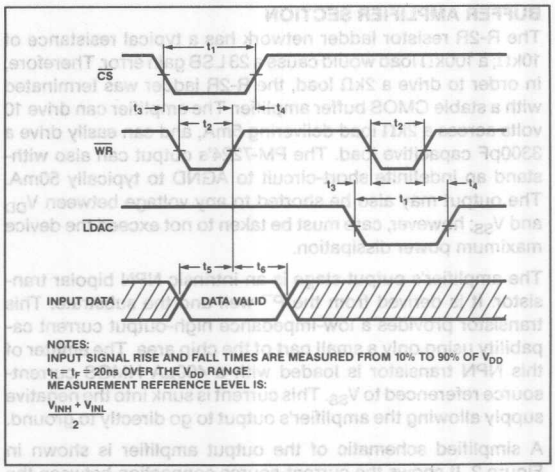


FIGURE 6: Write Timing Diagram



APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7224 data sheet is specified with a dual or single power supply condition. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V and a negative supply (V_{SS}) of −5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to V_{DD} − 4V. For those applications requiring +10 volts at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits.

The specified V_{REF} for the single supply specifications is +10V. V_{REF} voltage limitation of V_{DD} − 4V for dual or single power supply applications must be observed. This will ensure that the PM-7224's multiplying capabilities are preserved.

Although the PM-7224 can operate well with either a single or dual power supply, improved zero-code error can be achieved by using dual supplies.

DYNAMIC PERFORMANCE

The PM-7224's settling time is limited by the internal amplifier's slew rate; however, it sports an impressive settling time of 5μs using a dual or single power supply. Settling time is not affected by the DAC's output voltage polarity, positive or negative. The PM-7224 also has minimum signal overshoot or ringing.

AGND BIASING

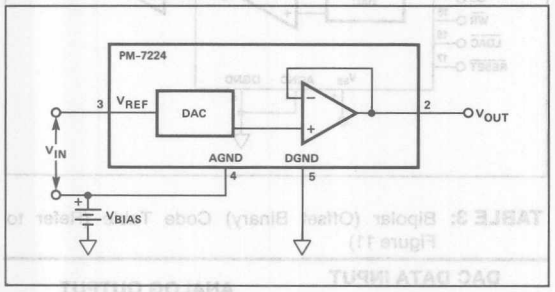
Some applications may require a DC offset voltage level at the DAC's output. This may be easily accomplished with the PM-7224; the desired DC offset voltage can be applied to the AGND pin as shown in Figure 7. The DAC's TTL/CMOS compatibility is not affected. Note that V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:

$$V_{OUT} = \text{AGND bias} + V_{IN} \times D/256$$

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

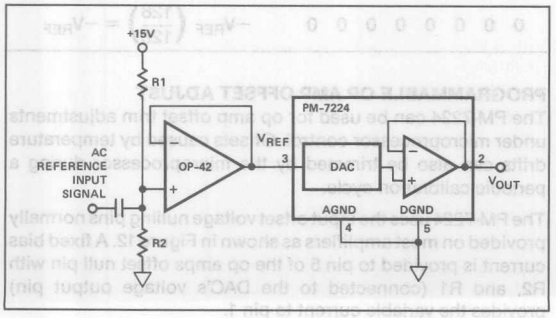
FIGURE 7: AGND Biasing Scheme



MULTIPLYING OPERATION

The PM-7224 has good multiplying capabilities if the reference input signal level is kept within +2V and V_{DD} − 4V, with V_{DD} of +16.5 V, the maximum input signal level is +12.5V; however, it is recommended that V_{DD} = +15V ±5% and the AC voltage swing between +2V and V_{DD} − 4V. The signal must be AC coupled and biased up with a voltage divider as shown in Figure 8. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance does not load the resistor divider, R1 and R2.

FIGURE 8: AC Signal Input Scheme

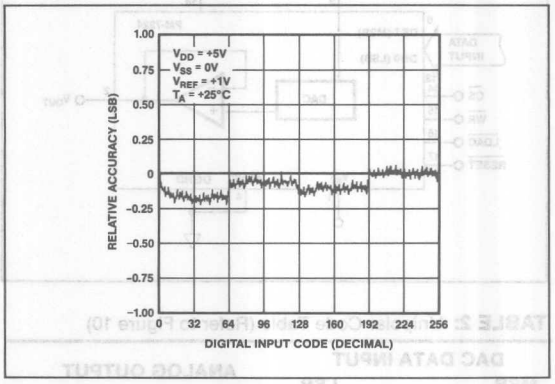


The V_{REF} small-signal frequency response (−3dB bandwidth) for the PM-7224 is typically 1.5MHz. Its small-signal harmonic distortion is less than −57dB at 1kHz and −55dB at 100kHz.

+5V SINGLE SUPPLY OPERATION

Although a +5V performance specification table is not listed, the PM-7224 can operate well with only a single +5V supply (see Figure 9). This will then limit the reference input voltage level to a maximum of +1V; the V_{DD} − 4V limitation must still be observed.

FIGURE 9: Relative Accuracy With Single +5V Operation



GENERAL GROUND MANAGEMENT

Digital transient voltages between AGND and DGND can appear as noise at the PM-7224's output. It is, therefore, recommended that AGND and DGND be tied together at the device socket; each ground is then brought out separately to their respective common ground points. A word of caution is worth mentioning here: ground loops can be created if both grounds are tied together at more than one location, i.e., at the device socket and back at the power supplies, or at any other location. These ground loops can cause noisy digital ground currents to flow through the analog ground paths and destroy its integrity. Analog ground should be maintained as a high quality ground.

If system requirements dictate the use of one common return line for each ground, then the DAC should be placed as close to the power supplies as possible. Also, for those systems that require both grounds be separated, two Schottky diodes should be tied in inverse parallel between AGND and DGND at the device socket.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system and causing system errors. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance.

High and low frequency decoupling capacitors at the device socket is strongly recommended; a 0.01μF ceramic in parallel with a 1 to 10μF tantalum decoupling capacitors should be used.

UNIPOLAR OPERATION

Figure 10 shows the PM-7224 configured to operate in the unipolar mode; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation.

FIGURE 10: Unipolar Operation

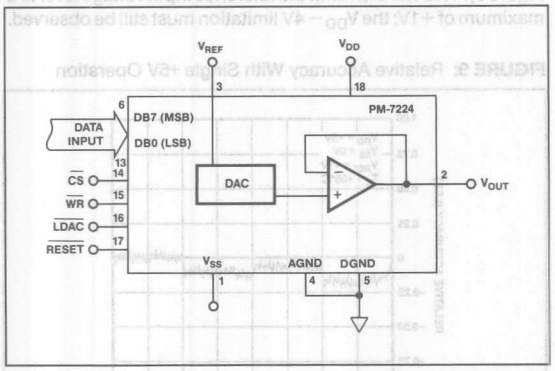


TABLE 2: Unipolar Code Table (Refer to Figure 10)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{225}{256}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right)=\frac{+V_{REF}}{2}$
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

It shows no signal inversion between $+V_{REF}$ and V_{OUT}. Also note that the analog output voltage is equal to V_{REF} multiplied by the digital input code, hence, multiplying DAC.

The expression for 1 LSB and V_{OUT} is:

$$1\ \text{LSB} = V_{REF} \times 2^{-8}, \text{ or } V_{REF} \times 1/256$$

and

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input integer between 0 and 255.

BIPOLAR OPERATION

Figure 11 illustrates the bipolar mode of operation for the PM-7224. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; see Table 3 for R1 = R2. This configuration requires an external amplifier and two resistors.

where D is the digital input code integer between 0 and 255. If R1 = R2, then V_{OUT} becomes:

$$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$$

To keep gain and offset errors at a minimum, R1 and R2 should be matched to ±0.1% and track over the operating temperature range of interest.

FIGURE 11: Bipolar Operation

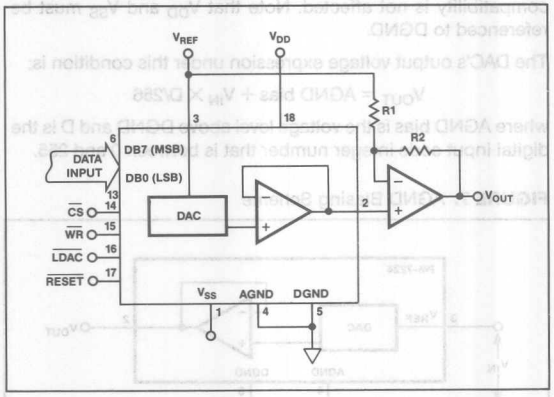


TABLE 3: Bipolar (Offset Binary) Code Table (Refer to Figure 11)

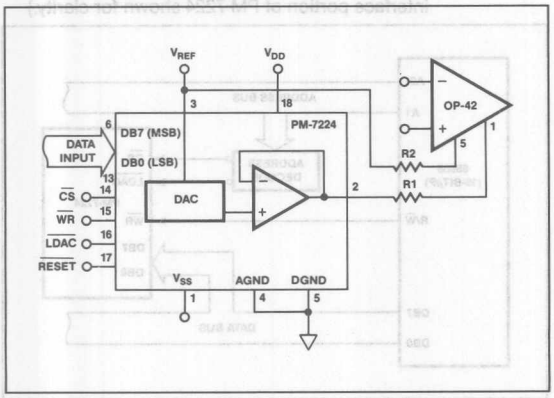
DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right)=-V_{REF}$

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7224 can be used for op amp offset trim adjustments under microprocessor control. Offsets caused by temperature drifts can also be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7224 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 12. A fixed bias current is provided to pin 5 of the op amps offset null pin with R2, and R1 (connected to the DAC's voltage output pin) provides the variable current to pin 1.

FIGURE 12: Op Amp Offset Adjust (See Text)



For a plus or minus (±) offset adjust control, the current through R1 must equal the current through R2 when the PM-7224 is at half scale, binary code = 10000000.

The resistor values R1 and R2 should be chosen to give the required offset adjustment range desired. Lower values provide a larger range; however, resolution will be sacrificed. Reversing the op amp connections, pin 1 and 5, will reverse the offset adjustment direction.

Some op amps are not provided with offset adjustment pins. In these cases, the circuit configuration of Figure 13 can be used. Again, the current through resistor R4 must equal the current through R3 with the PM-7224 at half scale, digital code = 10000000. With the circuit components shown, the maximum adjustment range is ±5mV. Incremental adjustment resolution is 39μV per bit.

MICROPROCESSOR INTERFACING

Interfacing the PM-7224 to a microprocessor is simplified by virtue of its loading structure simplicity. Data from the processor is loaded into the DAC by use of only two control lines, the write strobe ($\overline{WR}$) and chip select ($\overline{CS}$). The data is then output with the $\overline{WR}$ and $\overline{LDAC}$ signal. Figures 14 through 17 show various popular microprocessor interface configurations.

FIGURE 14: PM-7224 to 8085A Interface (Only digital interface portion of PM-7224 shown for clarity.)

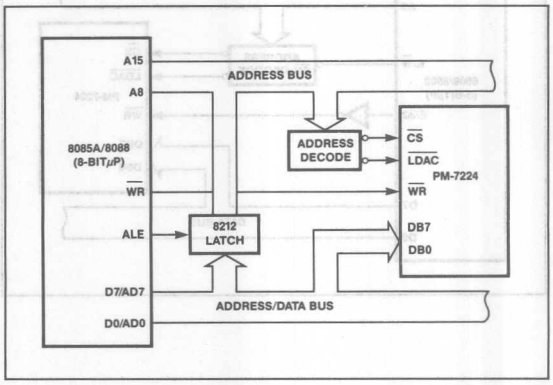


FIGURE 15: PM-7224 to Z-80 Interface (Only digital interface portion of PM-7224 shown for clarity.)

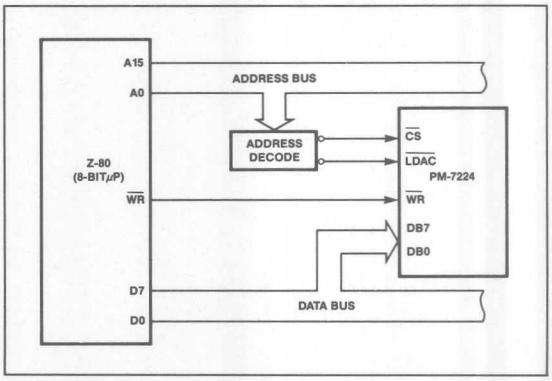


FIGURE 13: Alternate Offset Adjust (See Text)

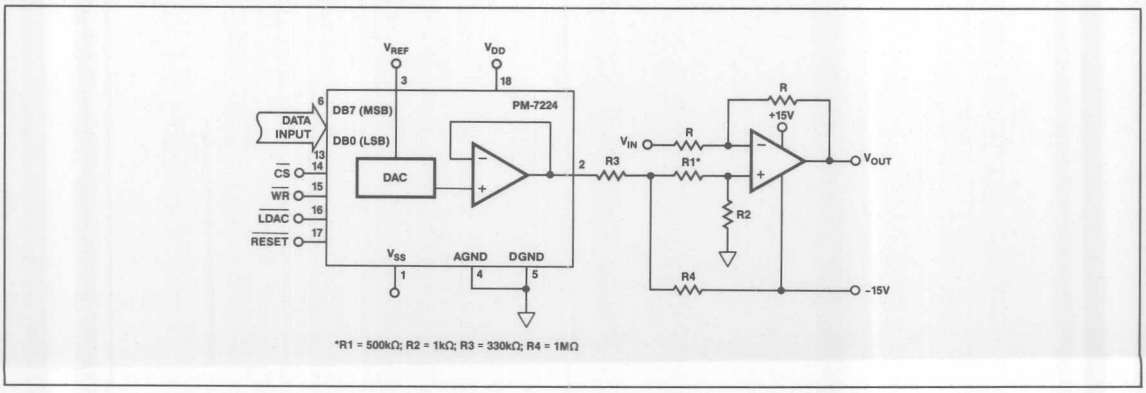


FIGURE 16: PM-7224 to 6809 Interface (Only digital interface portion of PM-7224 shown for clarity.)

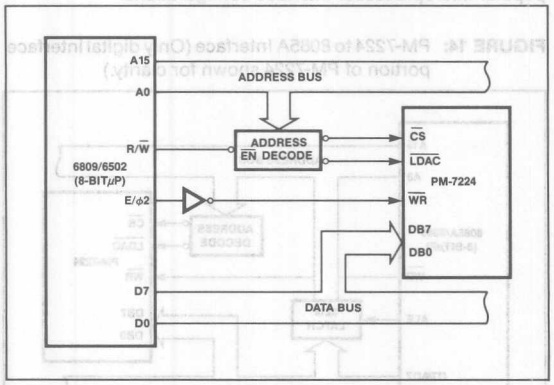
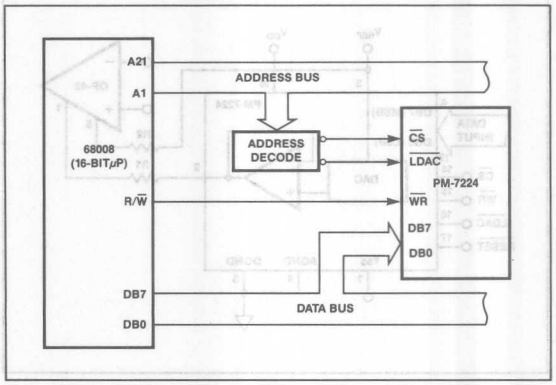


FIGURE 17: PM-7224 to 68008 Microprocessor (Only digital interface portion of PM-7224 shown for clarity.)



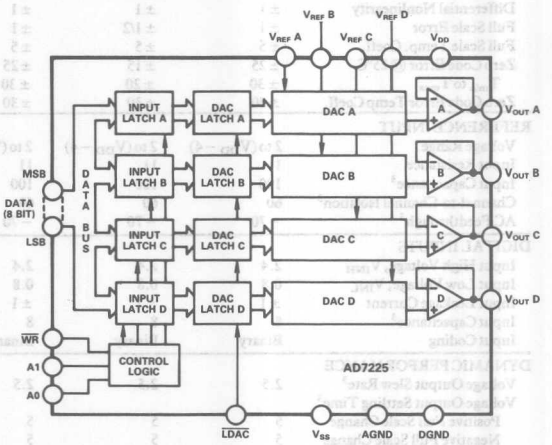
LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

- Four 8-Bit DACs with Output Amplifiers
- Separate Reference Input for Each DAC
- µP Compatible with Double-Buffered Inputs
- Simultaneous Update of All Four Outputs
- Operates with Single or Dual Supplies
- Extended Temperature Range Operation
- No User Trims Required
- Skinny 24-Pin DIP, SOIC and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Versatile Interface Logic
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC
   The AD7225 offers great flexibility in dealing with input signals with a separate reference input provided for each DAC and each reference having variable input voltage capability.

DUAL SUPPLY (All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1	±1/2	±1	±1/2	LSB max	
Full Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	µV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2.5	2.5	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]						
Positive Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT						
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[4]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3,4]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3,4]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[4]	2	2	2	2	V/μs min	
Voltage Output Settling Time[4]						
Positive Full Scale Change	5	5	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	7	7	7	7	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3,4]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3,4]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7225KN	−40°C to +85°C	±2 LSB	N-24
AD7225LN	−40°C to +85°C	±1 LSB	N-24
AD7225KP	−40°C to +85°C	±2 LSB	P-28A
AD7225LP	−40°C to +85°C	±1 LSB	P-28A
AD7225KR	−40°C to +85°C	±2 LSB	R-24
AD7225LR	−40°C to +85°C	±1 LSB	R-24
AD7225BQ	−40°C to +85°C	±2 LSB	Q-24
AD7225CQ	−40°C to +85°C	±1 LSB	Q-24
AD7225TQ	−55°C to +125°C	±2 LSB	Q-24
AD7225UQ	−55°C to +125°C	±1 LSB	Q-24
AD7225TE	−55°C to +125°C	±2 LSB	E-28A
AD7225UE	−55°C to +125°C	±1 LSB	E-28A

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	500mW
Derates above 75°C by	2.0mW/C
Operating Temperature	
Commercial (K, L Versions)	−40°C to +85°C
Industrial (B, C Versions)	−40°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES

[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

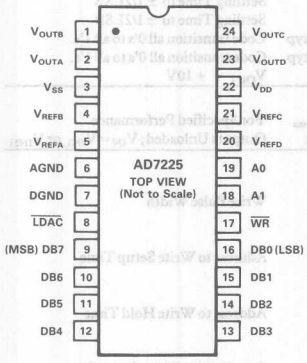
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

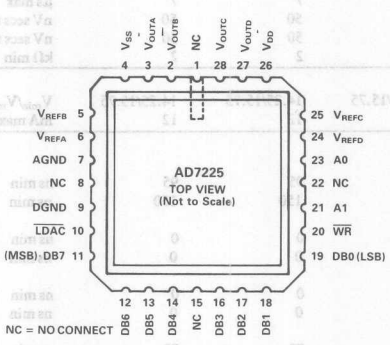


PIN CONFIGURATIONS

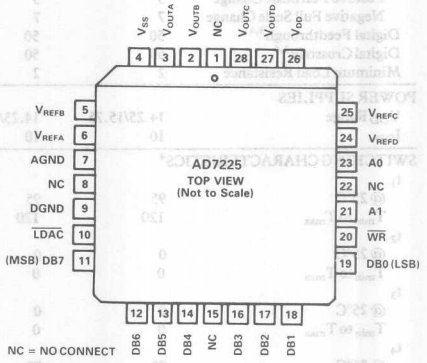
DIP and SOIC



LCCC



PLCC



TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full scale error, relative accuracy, and zero code error. Maximum output voltage is V_{REF} −1LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero code error and full scale error and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output of the DAC due to a change in its digital input code. It is specified in nV secs and is measured at V_{REF} = 0V.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter. It is specified in nV secs and is measured at V_{REF} = 0V.

AC FEEDTHROUGH

AC Feedthrough is the proportion of reference input signal which appears at the output of a converter when that DAC is loaded with all 0's.

CHANNEL-TO-CHANNEL ISOLATION

Channel-to-channel isolation is the proportion of input signal from the reference of one DAC (loaded with all 1's) which appears at the output of one of the other three DACs (loaded with all 0's). The figure given is the worst case for the three other outputs and is expressed as a ratio in dBs.

FULL SCALE ERROR

Full Scale Error is defined as:

Measured Value – Zero Code Error – Ideal Value

$T_A = 25°C$, $V_{DD} = +15V$, $V_{SS} = -5V$ unless otherwise stated.

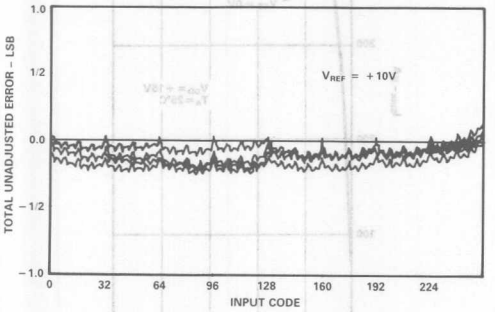


Figure 1. Channel-to-Channel Matching

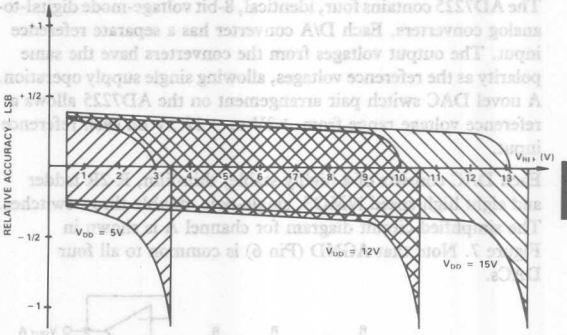


Figure 2. Relative Accuracy vs. V_{REF}

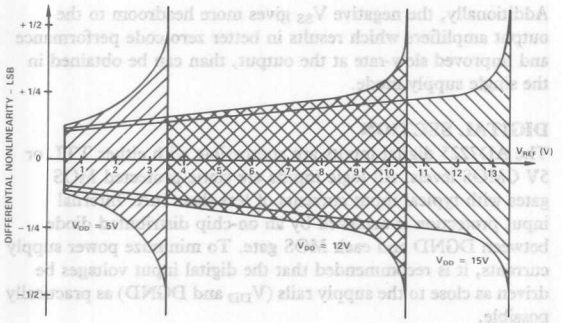


Figure 3. Differential Nonlinearity vs. V_{REF}

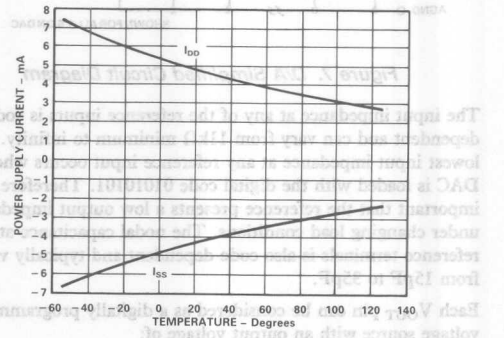


Figure 4. Power Supply Current vs. Temperature

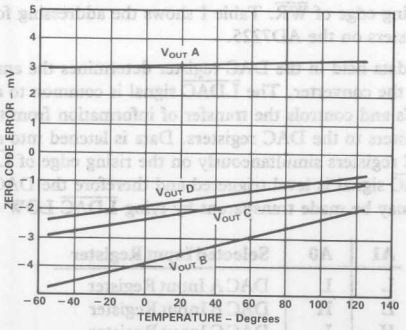


Figure 5. Zero Code Error vs. Temperature

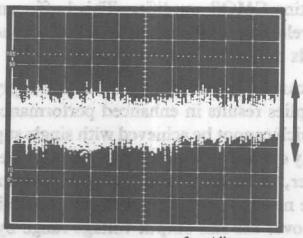


Figure 6. Broadband Noise

CIRCUIT INFORMATION

D/A SECTION

The AD7225 contains four, identical, 8-bit voltage-mode digital-to-analog converters. Each D/A converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, allowing single supply operation. A novel DAC switch pair arrangement on the AD7225 allows a reference voltage range from +2V to +12.5V on each reference input.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for channel A is shown in Figure 7. Note that AGND (Pin 6) is common to all four DACs.

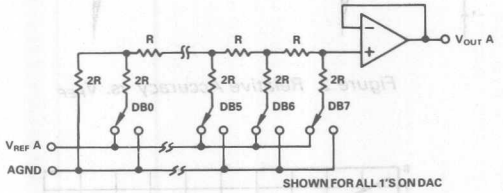


Figure 7. D/A Simplified Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 11kΩ minimum to infinity. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 15pF to 35pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X \cdot V_{REFX}$$

where D_X is fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

OP-AMP SECTION

Each voltage mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF.

The AD7225 can be operated single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with single supply operation. In single supply operation (V_{SS} = 0V = AGND) the sink capability of the amplifier, which is normally 400μA, is reduced as the output voltage nears AGND. The full sink capability of 400μA is maintained over the full output voltage range by tying V_{SS} to −5V. This is indicated in Figure 8.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

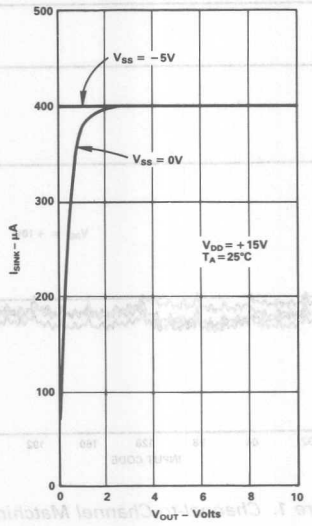


Figure 8. Variation of I_{SINK} with V_{OUT}

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7225 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table I shows the addressing for the input registers on the AD7225.

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC registers may be made transparent by tying $\overline{LDAC}$ LOW (in

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table I. AD7225 Addressing

this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay LOW for t_6 or longer after $\overline{WR}$ goes HIGH to ensure correct data is latched through to the output. Table II shows the truth table for AD7225 operation. Figure 9 shows the input control logic for the part and the write cycle timing diagram is given in Figure 10.

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device not selected
L	H	Input Register of Selected DAC Transparent
↓	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e. Outputs respond to data held in respective input registers)
		Input Registers are Latched
H	↓	All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent
		Output follows Input Data for Selected Channel.

Table II. AD7225 Truth Table

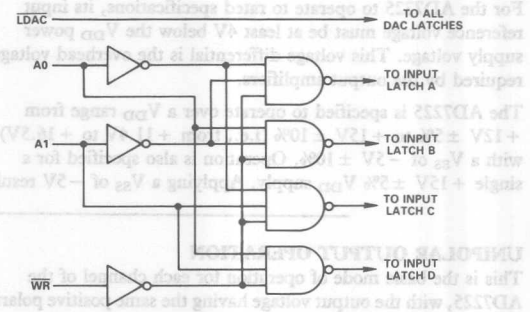


Figure 9. Input Control Logic

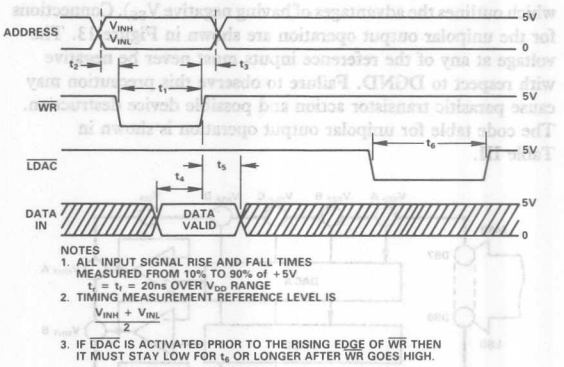


Figure 10. Write Cycle Timing Diagram

GROUND MANAGEMENT AND LAYOUT

Since the AD7225 contains four reference inputs which can be driven from ac sources (see AC REFERENCE SIGNAL section) careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 11 shows the relationship between input frequency and channel-to-channel isolation. Figure 12 shows a printed circuit board layout which is aimed at minimizing crosstalk and feedthrough. The four input signals are screened by AGND. V_{REF} was limited to between 2V and 3.24V to avoid slew rate limiting effects from the output amplifier during measurements.

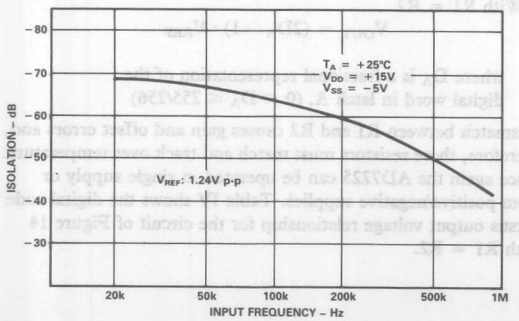


Figure 11. Channel-to-Channel Isolation

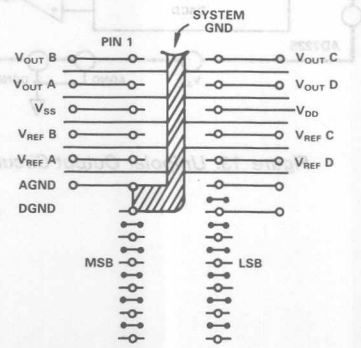


Figure 12. Suggested PCB Layout for AD7225. Layout Shows Component Side (Top View)

supply voltage. This voltage differential is the overhead voltage required by the output amplifiers.

The AD7225 is specified to operate over a V_{DD} range from +12V ±5% to +15V ±10% (i.e., from +11.4V to +16.5V) with a V_{SS} of −5V ±10%. Operation is also specified for a single +15V ±5% V_{DD} supply. Applying a V_{SS} of −5V results in a reduced output range of 0V to +10V. Performance is specified over a wide range of reference voltages from 2V to (V_{DD} − 4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that an output voltage range of 0V to +10V requires a nominal +15V ±5% power supply voltage.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7225, with the output voltage having the same positive polarity as V_{REF}. The AD7225 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 13. The voltage at any of the reference inputs must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table III.

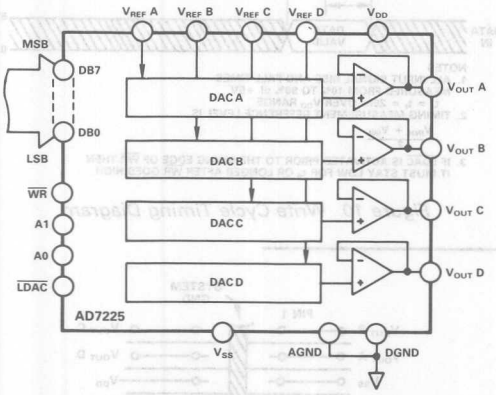


Figure 13. Unipolar Output Circuit

DAC Latch Contents MSB	LSB	Analog Output
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table III. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs of the AD7225 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 14 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7225. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A. ($0 \leq D_A \leq 255/256$)

Mismatch between R1 and R2 causes gain and offset errors and, therefore, these resistors must match and track over temperature. Once again the AD7225 can be operated in single supply or from positive/negative supplies. Table IV shows the digital code versus output voltage relationship for the circuit of Figure 14 with R1 = R2.

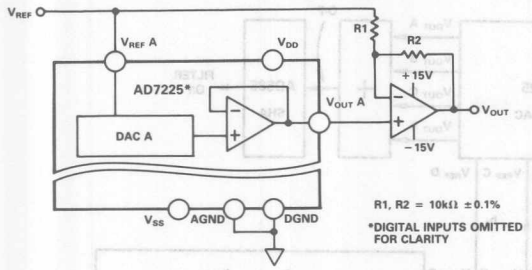


Figure 14. AD7225 Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table IV. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7225 AGND pin can be biased above system GND (AD7225 DGND) to provide an offset "zero" analog output voltage level. Figure 15 shows a circuit configuration to achieve this for channel A of the AD7225. The output voltage, V_{OUT} A, can be expressed as:

$$V_{OUT}\,A = V_{BIAS} + D_A\,(V_{IN})$$

where D_A is a fractional representation of the digital word in DAC latch A. ($0 \leq D_A \leq 255/256$).

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the AD7225. Note that V_{DD} and V_{SS} of the AD7225 should be referenced to DGND.

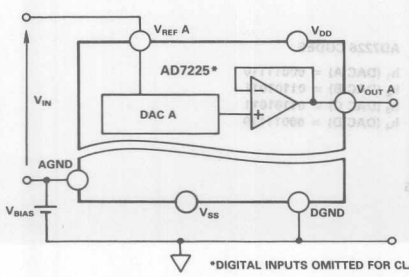


Figure 15. AGND Bias Circuit

AC REFERENCE SIGNAL

In some applications it may be desirable to have ac reference signals. The AD7225 has multiplying capability within the upper (V_{DD} – 4V) and lower (2V) limits of reference voltage when operated with dual supplies. Therefore ac signals need to be ac coupled and biased up before being applied to the reference inputs. Figure 16 shows a sine wave signal applied to V_{REF} A. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. The typical 3dB bandwidth figure for small signal inputs is 800kHz.

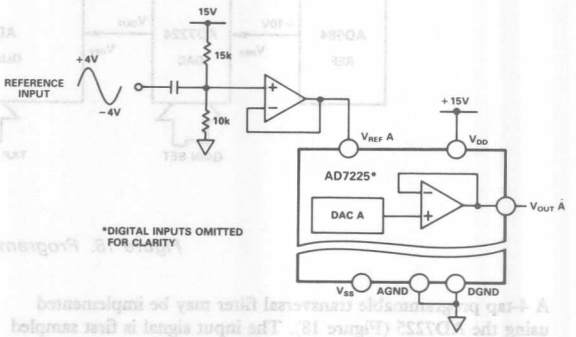


Figure 16. Applying an AC Signal to the AD7225

APPLICATIONS

PROGRAMMABLE TRANSVERSAL FILTER

A discrete-time filter may be described by either multiplication in the frequency domain or convolution in the time domain i.e.

$$Y(\omega) = H(\omega)X(\omega) \quad \text{or} \quad y_n = \sum_{k=1}^{N} h_k x_{n-k+1}$$

The convolution sum may be implemented using the special structure known as the transversal filter (Figure 17). Basically, it consists of an N-stage delay line with N taps weighted by N coefficients, the resulting products being accumulated to form the output. The tap weights or coefficients h_k are actually the non-zero elements of the impulse response and therefore determine the filter transfer function. A particular filter frequency response is realized by setting the coefficients to the appropriate values. This property leads to the implementation of transversal filters whose frequency response is programmable.

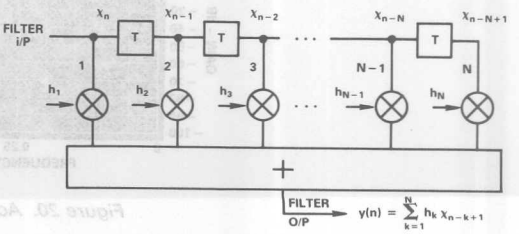


Figure 17. Transversal Filter

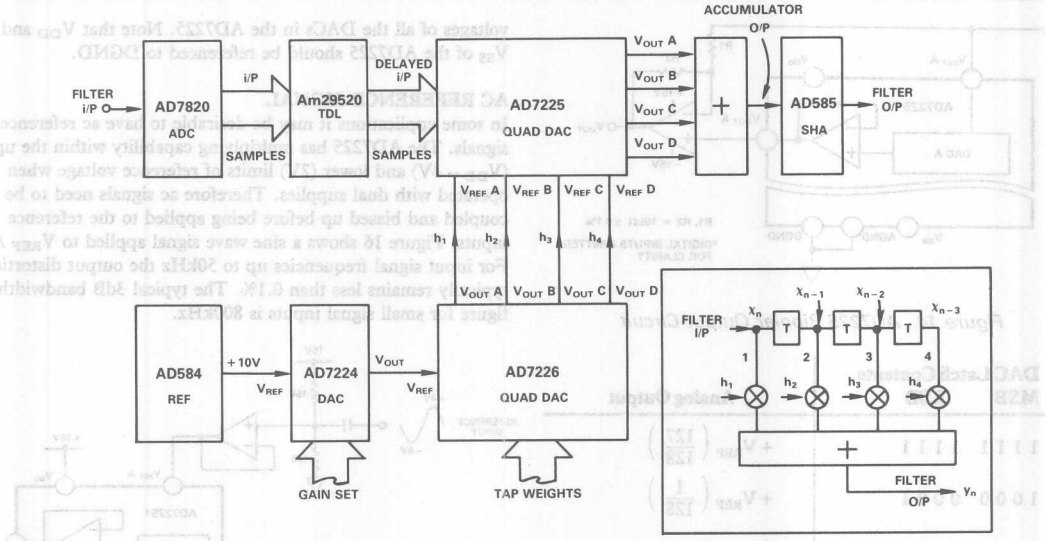


Figure 18. Programmable Transversal Filter

A 4-tap programmable transversal filter may be implemented using the AD7225 (Figure 18). The input signal is first sampled and converted to allow the tapped delay line function to be provided by the Am29520. The multiplication of delayed input samples by fixed, programmable tap weights is accomplished by the AD7225, the four coefficients or reference inputs being set by the digital codes stored in the AD7226. The resultant products are accumulated to yield the convolution sum output sample which is held by the AD585.

Low pass, bandpass and highpass filters may be synthesized using this arrangement. The particular tap weights needed for any desired transfer function may be obtained using the standard Remez Exchange Algorithm. Figure 19 shows the theoretical low pass frequency response produced by a 4-tap transversal filter with the coefficients indicated. Although the theoretical prediction does not take into account the quantization of the input samples and the truncation of the coefficients, nevertheless, there exists a good correlation with the actual performance of the transversal filter (Figure 20).

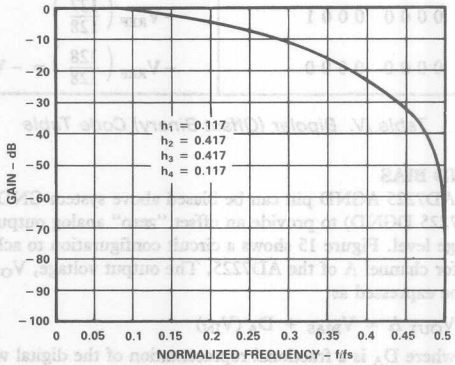


Figure 19. Predicted (Theoretical) Response

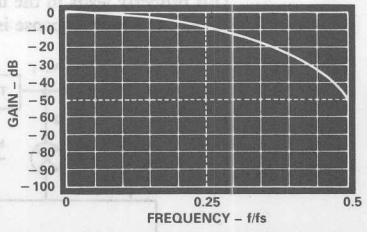


Figure 20. Actual Response

DIGITAL WORD MULTIPLICATION

Since each DAC of the AD7225 has a separate reference input, the output of one DAC can be used as the reference input for another. This means that multiplication of digital words can be performed (with the result given in analog form). For example, if the output from DACA is applied to V_{REF} B then the output from DACB, V_{OUT} B, can be expressed as:

$$V_{OUT}\ B = D_A \cdot D_B \cdot V_{REF}\ A$$

where D_A and D_B are the fractional representations of the digital words in DAC latches A and B respectively.

If $D_A = D_B = D$ then the result is $D^2 \cdot V_{REF}\ A$

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 21 shows one such application. In this case the output waveform, Y, is represented by:

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4) \cdot V_{IN}$$

where x is the digital code which is applied to all four DAC latches.

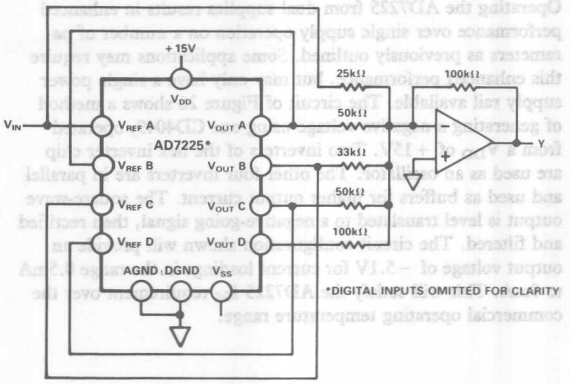


Figure 21. Complex Waveform Generation

MICROPROCESSOR INTERFACE

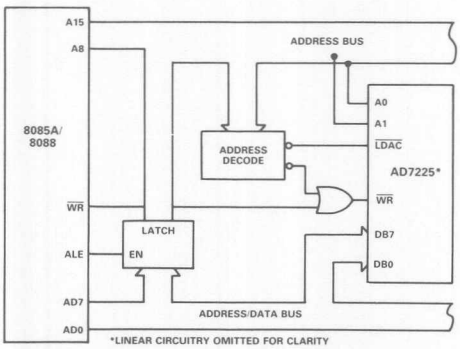


Figure 22. AD7225 to 8085A/8088 Interface, Double-Buffered Mode

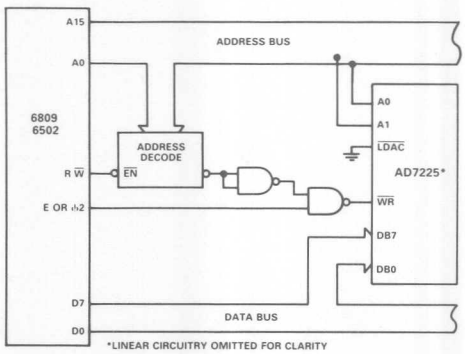


Figure 23. AD7225 to 6809/6502 Interface, Single-Buffered Mode

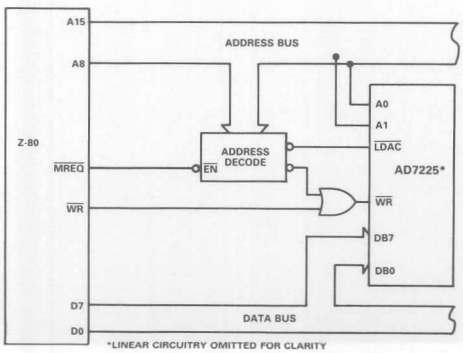


Figure 24. AD7225 to Z-80 Interface Double-Buffered Mode

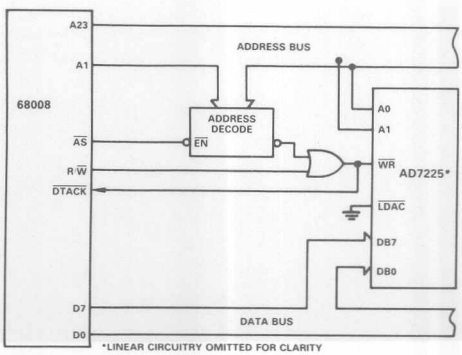


Figure 25. AD7225 to 68008 Interface, Single-Buffered Mode

Operating the AD7225 from dual supplies results in enhanced performance over single supply operation on a number of parameters as previously outlined. Some applications may require this enhanced performance, but may only have a single power supply rail available. The circuit of Figure 26 shows a method of generating a negative voltage using one CD4049, operated from a V_{DD} of +15V. Two inverters of the hex inverter chip are used as an oscillator. The other four inverters are in parallel and used as buffers for higher output current. The square-wave output is level translated to a negative-going signal, then rectified and filtered. The circuit configuration shown will provide an output voltage of −5.1V for current loadings in the range 0.5mA to 9mA. This will satisfy the AD7225 I_{SS} requirement over the commercial operating temperature range.

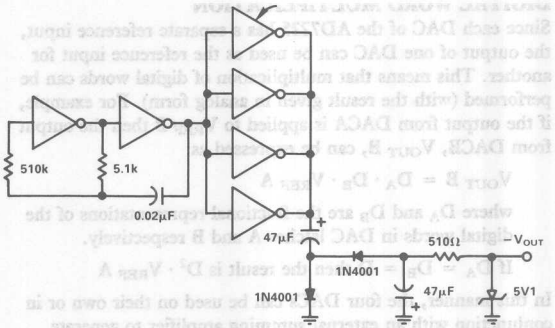


Figure 26. V_{SS} Generation Circuit

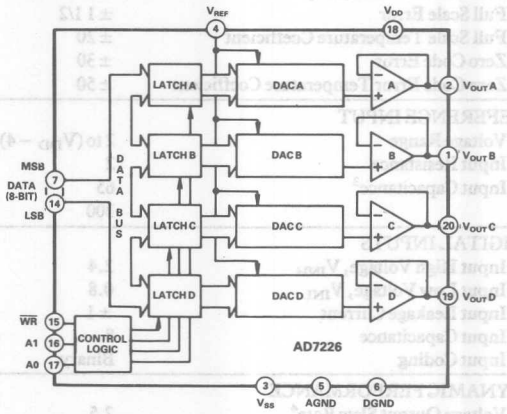
FEATURES

Four 8-Bit DACs with Output Amplifiers
Skinny 20-Pin DIP, SOIC and 20-Terminal Surface Mount Packages
Microprocessor Compatible
TTL/CMOS Compatible
No User Trims
Extended Temperature Range Operation
Single Supply Operation Possible

APPLICATIONS

Process Control
Automatic Test Equipment
Automatic Calibration of Large System Parameters, e.g., Gain/Offset

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7226 contains four 8-bit voltage-output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

The AD7226 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC^2MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching
   Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between the DACs is inherent.
2. Single Supply Operation
   The voltage mode configuration of the DACs allows the AD7226 to be operated from a single power supply rail.
3. Microprocessor Compatibility
   The AD7226 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered.
4. Small Size
   Combining four DACs and four op-amps plus interface logic into 20-pin DIP or SOIC or a 20-terminal surface mount package allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all the analog inputs and outputs at one end of the package and all the digital inputs at the other.

AD7226 – SPECIFICATIONS

Dual Supply (V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = 2V to (V_{DD} −4V)[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1 1/2	LSB max	
Full Scale Temperature Coefficient	±20	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	mV max	
Zero Code Error Temperature Coefficient	±50	µV/°C typ	
REFERENCE INPUT			
Voltage Range	2 to (V_{DD} −4)	V_{MIN} to V_{MAX}	
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2.5	V/µs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	11.4/16.5	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
I_{SS}	11	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
SWITCHING CHARACTERISTICS[4,5]			
Address to Write Setup Time, t_{AS}			
@25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K Version: −40°C to +85°C
B Version: −40°C to +85°C
T Version: −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample Tested at 25°C to ensure compliance.
[5]Switching Characteristics apply for both single and dual supply operation.
Specifications subject to change without notice.

Single Supply (V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} +10V[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT			
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2	V/μs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	μs max	Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	14.25 to 15.75	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K Version: −40°C to +85°C
B Version: −40°C to +85°C
T Version: −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample Tested at 25°C to ensure compliance.
[5]Switching Characteristics apply for both single and dual supply operation.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{SS} to AGND . . . . . −7V, V_{DD}
V_{SS} to DGND . . . . . −7V, V_{DD}
V_{DD} to V_{SS} . . . . . −0.3V, +24V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 500mW
Derates above 75°C by . . . . . 2.0mW/°C
Operating Temperature
Commerical (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTES
[1]Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7226KN	−40°C to +85°C	±2LSB	N-20
AD7226KP	−40°C to +85°C	±2LSB	P-20A
AD7226KR	−40°C to +85°C	±2LSB	R-20
AD7226BQ	−40°C to +85°C	±2LSB	Q-20
AD7226TQ	−55°C to +125°C	±2LSB	Q-20
AD7226TE	−55°C to +125°C	±2LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962–87802.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

TERMINOLOGY

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes full-scale error, relative accuracy and zero code error. Maximum output voltage is V_{REF} − 1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity, is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full-scale error and is normally expressed in LSB's or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL CROSSTALK

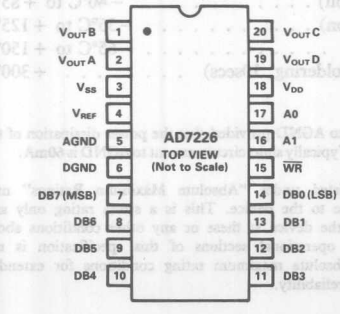
The glitch impulse transferred to the output of one converter due to a change in the digital input code to another of the converters. It is specified in nV secs and is measured at V_{REF}=0V.

FULL-SCALE ERROR

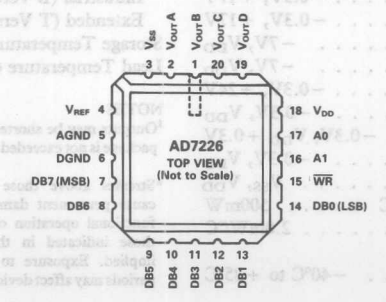
Full-Scale Error is defined as:
Measured Value – Zero Code Error – Ideal Value.

PIN CONFIGURATIONS

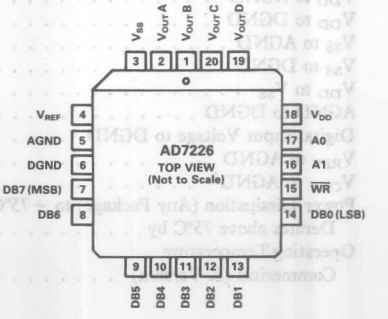
DIP, SOIC



LCCC



PLCC



CIRCUIT INFORMATION

D/A SECTION

The AD7226 contains four, identical, 8-bit, voltage-mode digital-to-analog converters. The output voltages from the converters have the same polarity as the reference voltage allowing single supply operation. A novel DAC switch pair arrangement on the AD7226 allows a reference voltage range from +2V to +12.5V.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for one channel is shown in Figure 1. Note that V_{REF} (pin 4) and AGND (pin 5) are common to all four DACs.

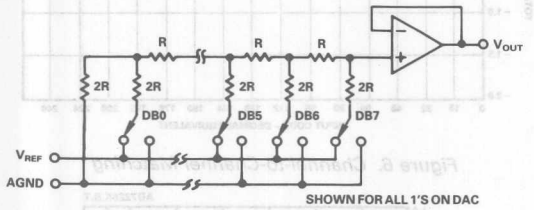


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7226 is the parallel combination of the four individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance (i.e., 2kΩ) occurs when all four DACs are loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminal is also code dependent and typically varies from 100pF to 250pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X V_{REF}$$

where D_X is a fractional representation of the digital input code and can vary from 0 to 255/256.

The source impedance is the output resistance of the buffer amplifier.

OP-AMP SECTION

Each voltage-mode D/A converter output is buffered by a unity gain, noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF. The output stage of this amplifier consists of a bipolar transistor from the V_{DD} line and a current load to V_{SS}, the negative supply for the output amplifiers. This output stage is shown in Figure 2.

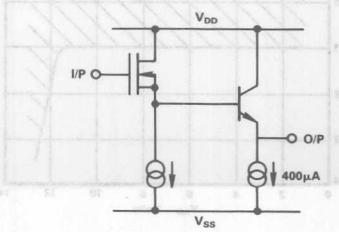


Figure 2. Amplifier Output Stage

The NPN transistor supplies the required output current drive (up to 5mA). The current load consists of NMOS transistors which normally act as a constant current sink of 400μA to V_{SS}, giving each output a current sink capability of approximately 400μA if required.

The AD7226 can be operated single supply or dual supply resulting in different performance in some parameters from the output amplifiers.

In single supply operation (V_{SS} = 0V = AGND), with the output approaching AGND (i.e., digital code approaching all 0's) the current load ceases to act as a current sink and begins to act as a resistive load of approximately 2kΩ to AGND. This occurs as the NMOS transistors come out of saturation. This means that, in single supply operation, the sink capability of the amplifiers is reduced when the output voltage is at or near AGND. A typical plot of the variation of current sink capability with output voltage is shown in Figure 3.

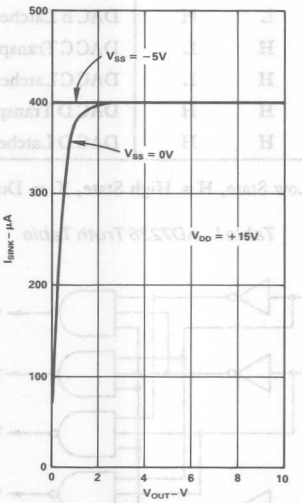


Figure 3. Variation of I_{SINK} with V_{OUT}

If the full sink capability is required with output voltages at or near AGND (=0V), then V_{SS} can be brought below 0V by 5V and thereby maintain the 400μA current sink as indicated in Figure 3. Biasing V_{SS} below 0V also gives additional headroom in the output amplifier which allows for better zero code error performance on each output. Also improved is the slew-rate and the negative-going settling-time of the amplifiers (discussed later).

Each amplifier offset is laser trimmed during manufacture to eliminate any requirement for offset nulling.

DIGITAL SECTION

The digital inputs of the AD7226 are both TTL and CMOS (5V) compatible from V_{DD} = +11.4V to +16.5V. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

Address lines A0 and A1 select which DAC will accept data from the input port. Table I shows the selection table for the four DACs with Figure 4 showing the input control logic. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7226 Control Inputs			AD7226
$\overline{WR}$	A1	A0	Operation
H	X	X	No Operation Device Not Selected
↓	L	L	DAC A Transparent
↑	L	L	DAC A Latched
↓	L	H	DAC B Transparent
↑	L	H	DAC B Latched
↓	H	L	DAC C Transparent
↑	H	L	DAC C Latched
↓	H	H	DAC D Transparent
↑	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

Table I. AD7226 Truth Table

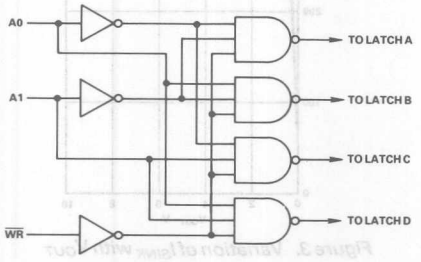
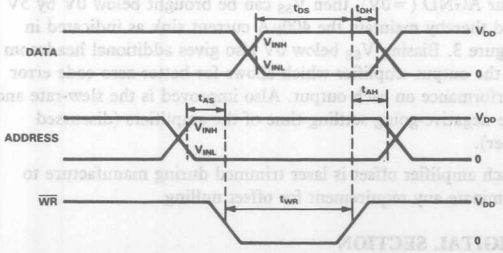


Figure 4. Input Control Logic



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}. $t_r = t_f = 20ns$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$
3. SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS.

Figure 5. Write Cycle Timing Diagram

Typical Performance Characteristics

($T_A = 25°C$, $V_{DD} = +15V$, $V_{SS} = -5V$)

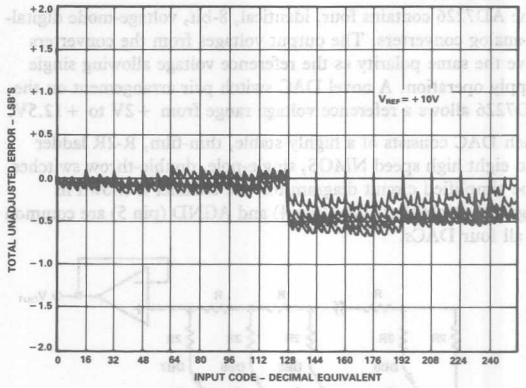


Figure 6. Channel-to-Channel Matching

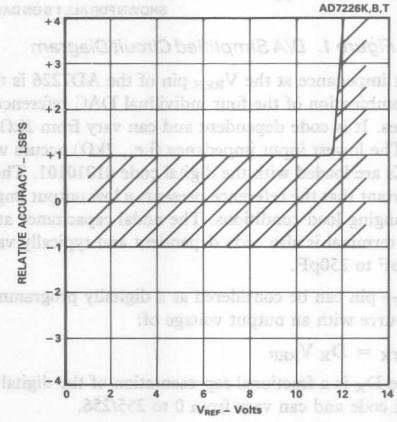


Figure 7. Relative Accuracy vs. V_{REF}

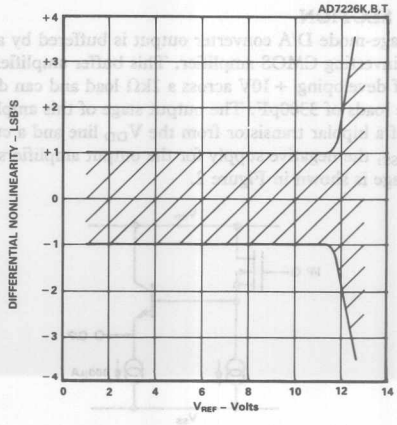


Figure 8. Differential Nonlinearity vs. V_{REF}

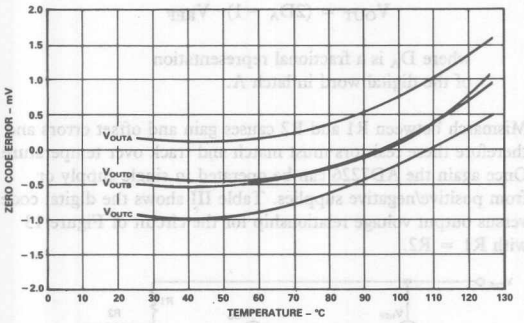


Figure 9. Zero Code Error vs. Temperature

SPECIFICATION RANGES

In order for the DACs to operate to their specifications, the reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

The AD7226 is specified to operate over a V_{DD} range from +12V ±5% to +15V ±10% (i.e., from 11.4V to +16.5V) with a V_{SS} of −5V ±10%. Operation is also specified for a single +15V ±5% V_{DD} supply. Applying a V_{SS} of −5V results in improved zero code error, improved output sink capability with outputs near AGND, and improved negative-going settling-time.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} −4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that in order to achieve an output voltage range of 0V to +10V, a nominal +15V ±5% power supply voltage is required by the AD7226.

SETTLING TIME

The output stage of the buffer amplifiers consists of a bipolar NPN transistor from the V_{DD} line and a constant current load to V_{SS}. V_{SS} is the negative power supply for the output buffer amplifiers. As mentioned in the op-amp section, in single supply operation the NMOS transistor will come out of saturation as the output voltage approaches AGND and will act as a resistive load of approximately 2kΩ to AGND. As a result, the settling-time for negative-going signals approaching AGND in single supply operation will be longer than for dual supply operation where the current load of 400μA is maintained all the way down to AGND. Positive-going settling-time is not affected by V_{SS}.

The settling-time for the AD7226 is limited by the slew-rate of the output buffer amplifiers. This can be seen from Figure 10 which shows the dynamic response for the AD7226 for a full scale change. Figures 11a and 11b show expanded settling-time photographs with the output waveforms derived from a differential input to an oscilloscope. Figure 11a shows the settling-time for a positive-going step and Figure 11b shows the settling-time for a negative-going output step.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7226. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7226 AGND and DGND pins (IN914 or equivalent).

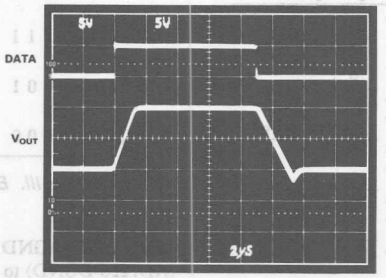


Figure 10. Dynamic Response (V_{SS} = −5V)

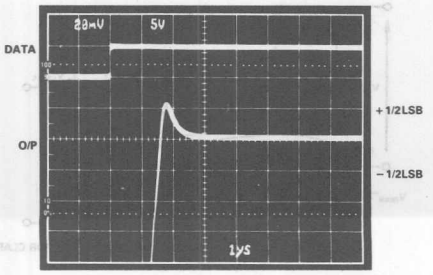


Figure 11a. Positive-Step Settling-Time (V_{SS} = −5V)

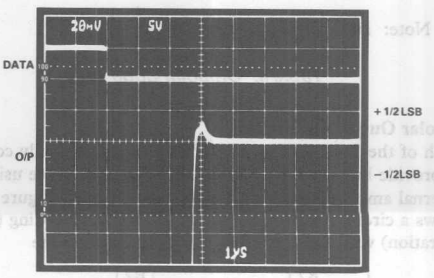


Figure 11b. Negative-Step Settling-Time (V_{SS} = −5V)

Applying the AD7226

Unipolar Output Operation

This is the basic mode of operation for each channel of the AD7226, with the output voltages having the same positive polarity as $+V_{REF}$. The AD7226 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). The code table for unipolar output operation is shown in Table II. Note that the voltage at V_{REF} must never be negative with respect to DGND in order to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 12.

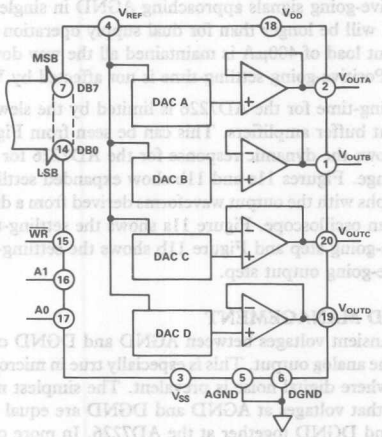


Figure 12. Unipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

Bipolar Output Operation

Each of the DACs of the AD7226 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 13 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7226. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors and therefore these resistors must match and track over temperature. Once again the AD7226 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 13 with R1 = R2.

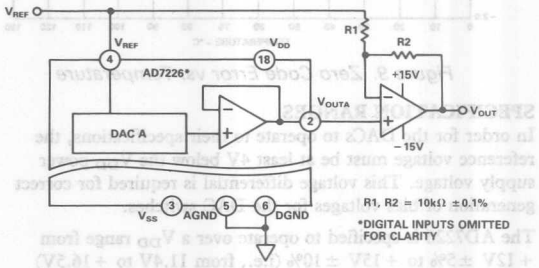


Figure 13. AD7226 Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7226 AGND pin can be biased above system GND (AD7226 DGND) to provide an offset "zero" analog output voltage level. Figure 14 shows a circuit configuration to achieve

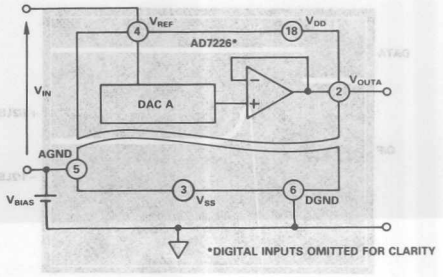


Figure 14. AGND Bias Circuit

this for channel A of the AD7226. The output voltage, V_{OUTA}, can be expressed as:

$$V_{OUTA} = V_{BIAS} + D_A (V_{IN})$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the AD7226. Note that V_{DD} and V_{SS} for the AD7226 should be referenced to DGND.

3-PHASE SINE WAVE

The circuit of Figure 15 shows an application of the AD7226 in the generation of 3-phase sine waves which can be used to control small 3-phase motors. The proper codes for synthesising a full sine wave are stored in EPROM, with the required phase-shift of 120° between the three D/A converter outputs being generated in software.

Data is loaded into the three D/A converters from the sine EPROM via the microprocessor or control logic. Three loops are generated in software with each D/A converter being loaded from a separate loop. The loops run through the look-up table producing successive triads of sinusoidal values with 120° separation which are loaded to the D/A converters producing 3 sine wave voltages 120° apart. A complete sine wave cycle is generated by stepping through the full look-up table. If a 256-element sine wave table is used then the resolution of the circuit will be 1.4° (360°/256). Figure 17 shows typical resulting waveforms. The sine waves can be smoothed by filtering the D/A converter outputs.

The fourth D/A converter of the AD7226, DAC D, may be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. This configuration is shown in Figure 15. The relationship of V_{REF} to V_{IN} is dependent upon digital code and upon the ratio of R_F to R and is given by the formula

$$V_{REF} = \frac{(1 + G)}{(1 + G.D_D)} . V_{IN}$$

where $G = R_F/R$

and D_D is a fractional representation of the digital word in latch D.

Alternatively, for a given V_{IN} and resistance ratio, the required value of D_D for a given value of V_{REF} can be determined from the expression

$$D_D = (1 + R/R_F) \cdot \frac{V_{IN}}{V_{REF}} - \frac{R}{R_F}$$

Figure 16 shows typical plots of V_{REF} versus digital code for three different values of R_F. With $V_{IN} = +2.5V$ and $R_F = 3R$ the peak-to-peak sine wave voltage from the converter outputs will vary between +2.5V and +10V over the digital input code range of 0 to 255.

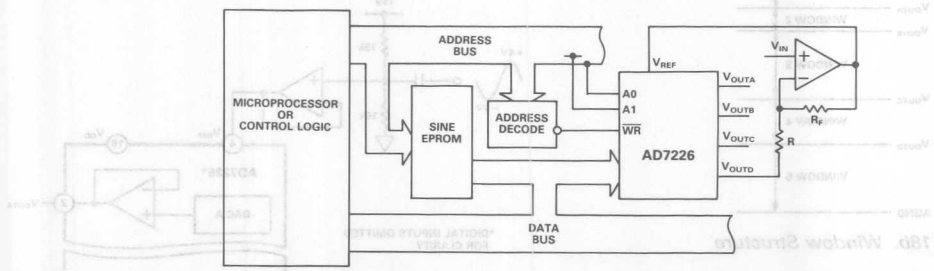


Figure 15. 3–Phase Sine Wave Generation Circuit

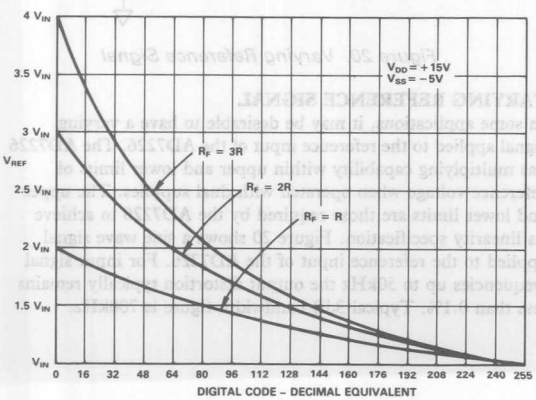


Figure 16. Variation of V_{REF} with Feedback Configuration

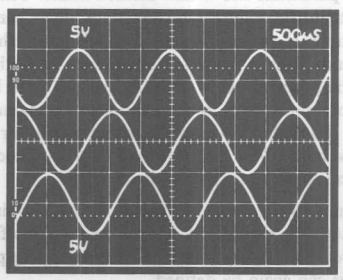


Figure 17. 3-Phase Sine Wave Output

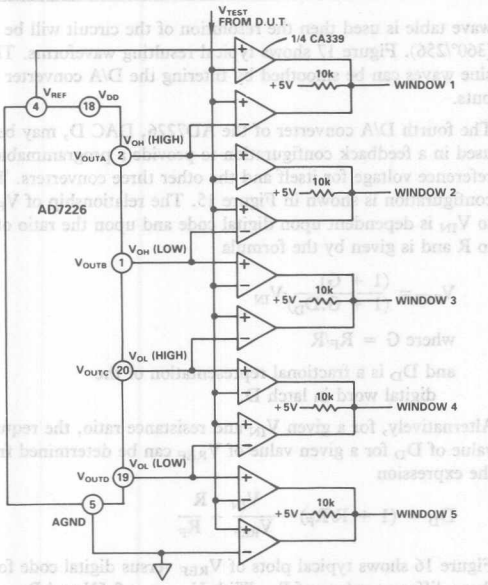


Figure 18a. Logic Level Measurement

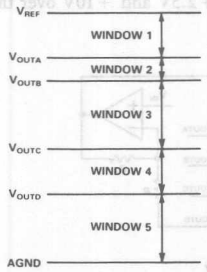


Figure 18b. Window Structure

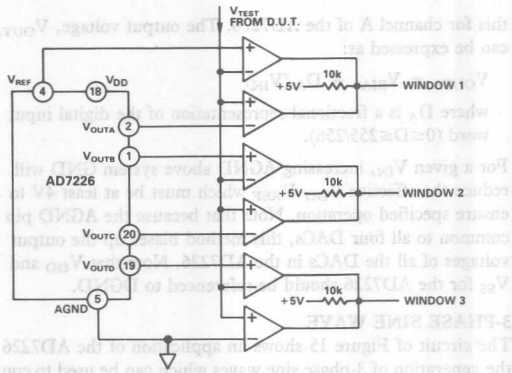


Figure 19a. Overlapping Windows

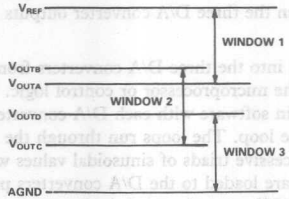


Figure 19b. Window Structure

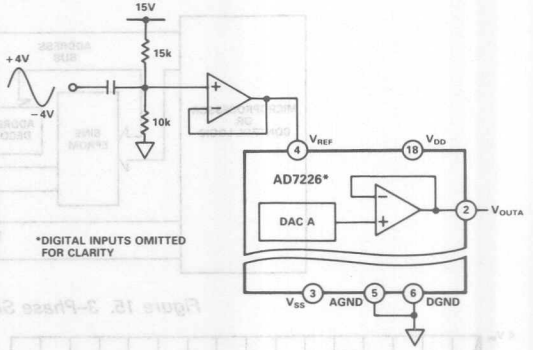


Figure 20. Varying Reference Signal

STAIRCASE WINDOW COMPARATOR

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator of Figure 18a is a circuit which can be used, for example, to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmably set using the AD7226. Each adjacent pair of comparators forms a window of programmable size. If V_{TEST} lies within a window then the output for that window will be high. With a reference of 2.56V applied to the V_{REF} input, the minimum window size is 10mV.

The circuit can easily be adapted to allow for overlapping of windows as shown in Figure 19a. If the three outputs from this circuit are decoded then five different nonoverlapping programmable windows can again be defined.

VARYING REFERENCE SIGNAL

In some applications, it may be desirable to have a varying signal applied to the reference input of the AD7226. The AD7226 has multiplying capability within upper and lower limits of reference voltage when operated with dual supplies. The upper and lower limits are those required by the AD7226 to achieve its linearity specification. Figure 20 shows a sine wave signal applied to the reference input of the AD7226. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. Typical 3dB bandwidth figure is 700kHz.

rammable input offset voltage adjustment for the AD544 op amp. Each output of the AD7226 can be used to trim the input offset voltage on one AD544. The 620kΩ resistor tied to +10V provides a fixed bias current to one offset node. For symmetrical adjustment, this bias current should equal the current in the other offset node with the half-full scale code (i.e. 10000000) on the DAC. Changing the code on the DAC varies the bias current and hence provides offset adjust for the AD544. For example, the input offset voltage on the AD544J, which has a maximum of ±2mV, can be programmably trimmed to ±10μV.

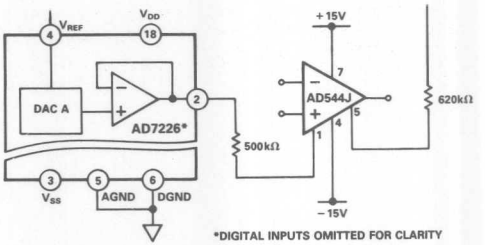


Figure 21. Offset Adjust for AD544

2

Microprocessor Interface

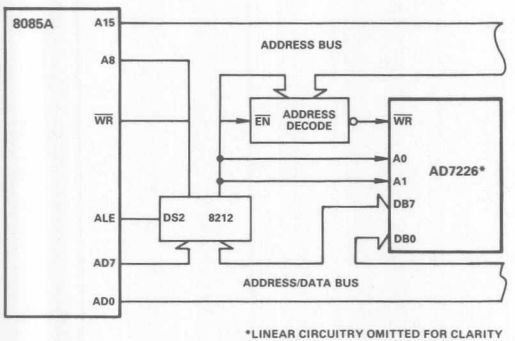


Figure 22. AD7226 to 8085A Interface

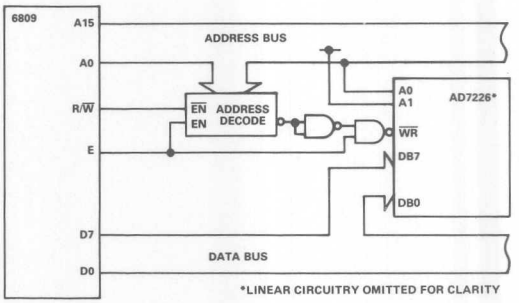


Figure 23. AD7226 to 6809 Interface

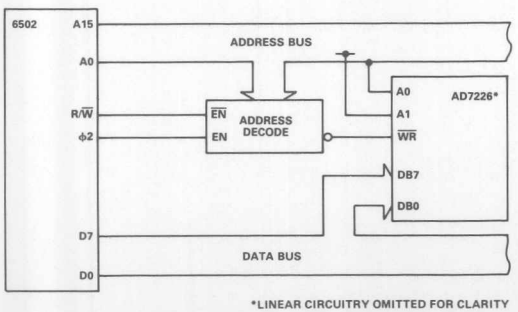


Figure 24. AD7226 to 6502 Interface

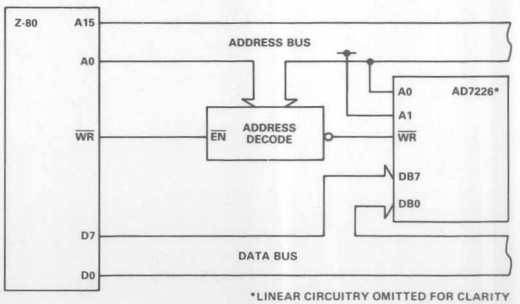


Figure 25. AD7226 to Z-80 Interface

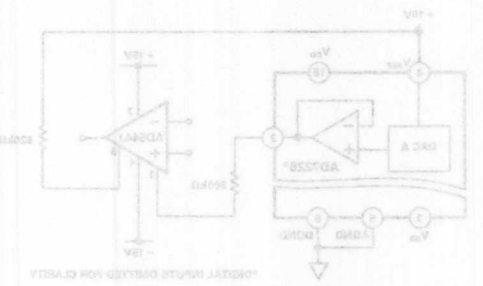


Figure 21. Offset Adjust for AD8441

OFFSET ADJUST

Figure 21 shows how the AD7226 can be used to provide programmable input offset voltage adjustment for the AD8441 op amp. Each output of the AD7226 can be used to trim the input offset voltage on one AD8541. The 620kΩ resistor tied to +10V provides a fixed bias current to one offset node. For symmetrical adjustment, this bias current should equal the current in the other offset node with the half-full scale code (i.e. 10000000) on the DAC. Changing the code on the DAC varies the bias current and hence provides offset adjust for the AD8541. For example, the input offset voltage on the AD8541, which has a maximum of ±2mV, can be programmably trimmed to ± 10μV.

Microprocessor Interface

Figure 22. AD7226 to 8085A Interface

Figure 23. AD7226 to 6809 Interface

Figure 24. AD7226 to 6502 Interface

Figure 25. AD7226 to Z-80 Interface

Quad 8-Bit CMOS D/A Converters With Voltage Output

PM-7226A/PM-7226

FEATURES

- **No Adjustments Required, Total Error ±1/2 LSB Max Over Temperature**
- **Four Voltage Output DACs on a Single Chip**
- **Single (+5V to +15V) or Dual Supply**
- **Improved PM-7226A Version Provides**
  - **Faster 50ns Write Time, All Temperatures**
  - **Tested 5V Specifications**
  - **Reduced Reference Input Transition Current**
  - **Epi-CMOS Processing for Improved Latch-up Resistance**

APPLICATIONS

- **Automatic Test Equipment**
- **Process and Industrial Control**
- **Scientific Instrumentation**
- **Medical Instrumentation**
- **Multichannel Microprocessor Controlled**
  - **System Calibration**
  - **Op Amp Offset and Gain Adjust**
  - **Level and Threshold Setting**

GENERAL DESCRIPTION

The PM-7226 contains four 8-bit voltage output CMOS digital-to-analog converters in a single chip. Also incorporated into this chip are four input latches and interface control logic.

The four latches are under control of one write and two address signals and are fed from a common 8-bit data bus. It allows the PM-7226 to be packaged into a narrow space-saving 20-pin, 300 mil DIP. All digital inputs are TTL/CMOS (5V) compatible. Also, each DAC's input latch is addressable for easy microprocessor interface. The on-board output amplifier can each drive up to 5mA from either a single or dual supply.

Continued

ORDERING INFORMATION †

TOTAL UNADJUSTED ERROR	MILITARY TEMPERATURE	EXTENDED INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
±1/2 LSB	PM7226AR	PM7226ER	PM7226GP
±1 LSB	PM7226BR	PM7226FR	—
±1 LSB	PM7226BRC/883	PM7226FPC	—
±1 LSB	—	PM7226FS	—
±1 LSB	—	PM7226FP	—
±1 LSB	—	PM7226AFR	—
±1 LSB	—	PM7226AFP	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

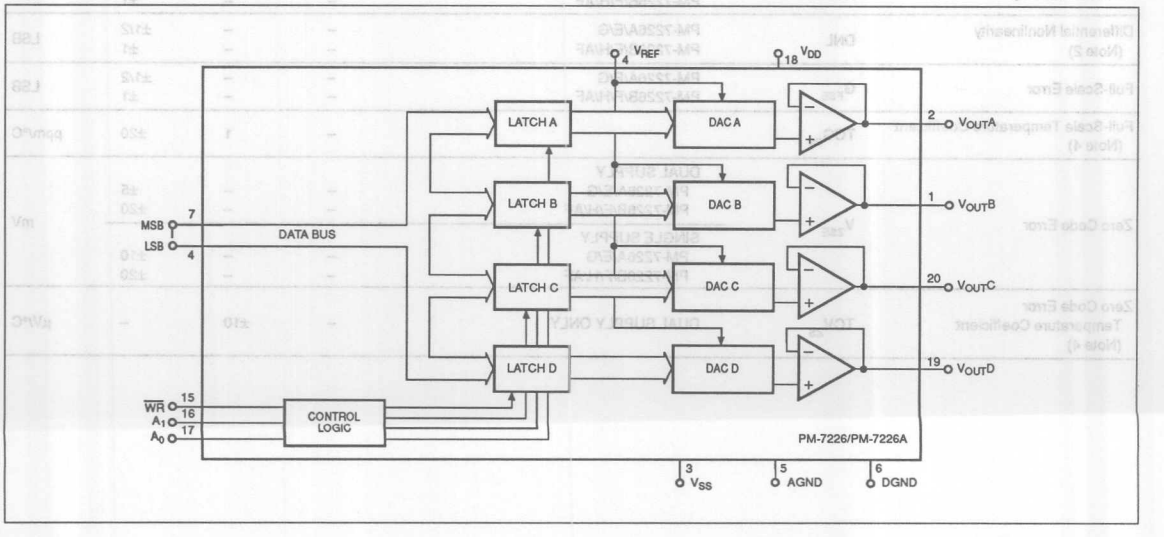
† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

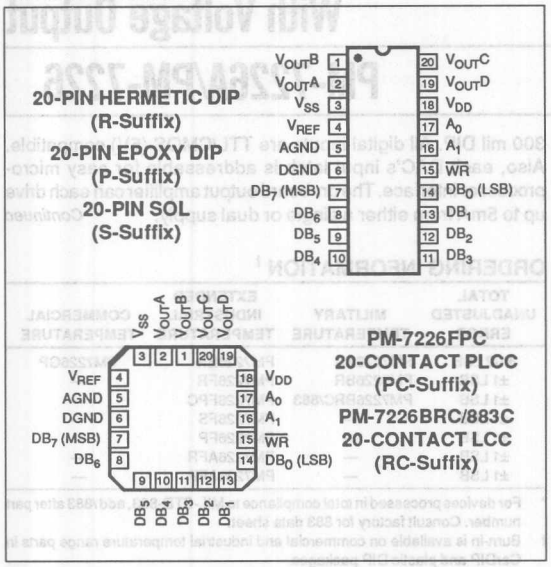
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7226AR	—	MIL
PM7226BR	AD7226TQ	
PM7226ER	—	IND
PM7226FR	AD7226BQ	
PM7226GP	—	COM
PM7226FPC	AD7226KP	
PM7226FP	AD7226KN	

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



GENERAL DESCRIPTION *Continued*

The PM-7226's compact size, low power, and economical cost per channel, make it attractive for applications requiring multiple D/A converters without sacrificing circuit board space. System reliability is also increased due to reduced part count. For higher channel output systems the PM-7226A can be connected with the DAC-8426 to provide a complete eight or higher channel output D/A system with an internal +10V reference in only two IC packages.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7226's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

The PM-7226 and the PM-7226A are improved replacements for the AD7226.

For military temperature range PM-7226A, contact factory for 883 data sheet.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} –4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = –55°C to +125°C apply for PM-7226AR/BR; T_A = –40°C to +85°C apply for PM-7226ER/FR/FP/FPC/FS/AFR/AFP; T_A = 0°C to +70°C apply for PM-7226GP. All specifications apply for DACs A, B, C, and D.

PARAMETER	SYMBOL	CONDITIONS	PM-7226A/PM-7226 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7226A/E/G (Note 7)	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Relative Accuracy	INL	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Full-Scale Error	G_{FSE}	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Full-Scale Temperature Coefficient (Note 4)	TCG_{FS}		–	1	±20	ppm/°C
Zero Code Error	V_{ZSE}	DUAL SUPPLY				mV
		PM-7226A/E/G	–	–	±5	
		PM-7226B/F/H/AF	–	–	±20	
		SINGLE SUPPLY				
		PM-7226A/E/G	–	–	±10	
		PM-7226B/F/H/AF	–	–	±20	
Zero Code Error Temperature Coefficient (Note 4)	TCV_{ZS}	DUAL SUPPLY ONLY	–	±10	–	µV/°C

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} –4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = –55°C to +125°C apply for PM-7226AR/BR; T_A = –40°C to +85°C apply for PM-7226ER/FR/FP/FPC/FS/AFR/AFP; T_A = 0°C to +70°C apply for PM-7226GP. All specifications apply for DACs A, B, C, and D. *Continued*

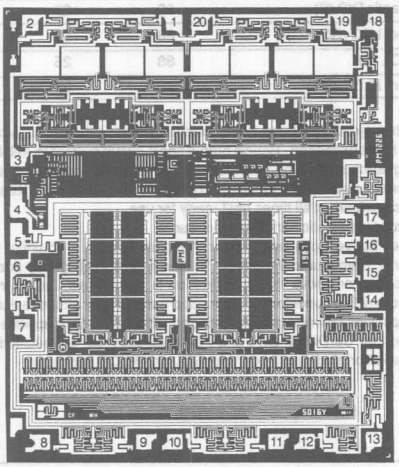
PARAMETER	SYMBOL	CONDITIONS	PM-7226A/PM-7226 MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Input Voltage Range (Note 3)	V_{REF}		2	–	(V_{DD} –4V)	V
Input Resistance	R_{REF}		2	4	–	kΩ
Input Capacitance (Note 4)	C_{REF}	Digital Inputs = all 0s Digital Inputs = all 1s	65 –	– –	– 300	pF
DIGITAL INPUTS						
Digital Inputs High	V_{INH}		2.4	–	–	V
Digital Inputs Low	V_{INL}		–	–	0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	0.1	±1	µA
Digital Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES						
Positive Supply Current (Note 6)	I_{DD}		–	6	12	mA
Negative Supply Current (Note 6)	I_{SS}	DUAL SUPPLY ONLY, V_{SS} = –5V	–	4	10	mA
Power Dissipation	P_{DISS}	V_{DD} = +12V, V_{SS} = 0V	–	72	144	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
V_{OUT} Slew Rate (Note 4)	SR		2.5	4	–	V/µs
V_{OUT} Settling Time (Positive or Negative) (Notes 4, 5)	t_s		–	3	5	µs
Digital Crosstalk (Note 4)	Q		–	10	–	nVs
Minimum Load Resistance	$R_{L(MIN)}$	V_{OUT} = +10V	2	–	–	kΩ
SWITCHING CHARACTERISTICS (Note 4)						
Address to Write Set-Up Time	t_{AS}		0	–	–	ns
Address to Write Hold Time	t_{AH}		0	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}	PM-7226 PM-7226A	90 70	– –	– –	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}	PM-7226 PM-7226A	90 50	– –	– –	ns

NOTES:
1. Includes Full-Scale Error, Relative Accuracy, and Zero Code Error.
2. All devices guaranteed monotonic over the full operating temperature range.
3. V_{DD} –4V is the maximum reference voltage for the above specifications.
4. Guaranteed by design and not subject to production test.
5. V_{REF} = +10V; to where output settles to 1/2 LSB.
6. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
7. V_{DD} = +15V only.

ELECTRICAL CHARACTERISTICS : +5V Supply Operation at V_{DD} = +5V ±5%, V_{SS} = 0 or –5V, AGND = DGND = 0V, V_{REF} = +1.25V, unless otherwise noted. T_A = –40°C to +85°C applies for PM-7226AFR/FP. All specifications apply for DACs A, B, C, and D.

			PM-7226A ONLY			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution	N		8	–	–	Bits
Differential Nonlinearity	DNL	Applies to Codes 2 through 255	–	–	±1	LSB
Full-Scale Error	G_{FSE}		–	–	±4	LSB
Zero Code Error	V_{ZSE}		–	–	30	mV
Reference Input Voltage Range	V_{REF}	$V_{OUT} < (V_{DD} - 3.5V)$	1.2	1.25	1.3	V
Reference Input Resistance	R_{REF}	Digital Inputs all 1s	2	–	–	kΩ
Reference Input Capacitance	C_{REF}	Digital Inputs all 1s	–	–	300	pF
DIGITAL INPUTS (All specifications the same as for V_{DD} = +12V supplies)						
DYNAMIC PERFORMANCE (All specifications are the same as for V_{DD} = +12V supplies.)						
Positive Supply Current	I_{DD}		–	3.5	12	mA
Negative Supply Current	I_{SS}	V_{SS} = –5V only	–	3.5	10	mA
Power Dissipation	P_{DISS}	V_{SS} = 0V	–	17.5	60	mW
SWITCHING CHARACTERISTICS						
Address-to-Write Setup Time	t_{AS}		0	–	–	ns
Address-to-Write Hold Time	t_{AH}		20	–	–	ns
Data Valid-to-Write Setup Time	t_{DS}		180	–	–	ns
Data Valid-to-Write Hold Time	t_{DS}		20	–	–	ns
Write Pulse Width	t_{WR}		120	–	–	ns

DICE CHARACTERISTICS



DIE SIZE 0.129 x 0.152 inch, 19,608 sq. mils
(3.28 x 3.86 mm, 12.65 sq. mm)

1. $V_{OUT}B$
2. $V_{OUT}A$
3. V_{SS}
4. V_{REF}
5. AGND
6. DGND
7. DB_7 (MSB)
8. DB_6
9. DB_5
10. DB_4
11. DB_3
12. DB_2
13. DB_1
14. DB_0 (LSB)
15. $\overline{WR}$
16. A_1
17. A_0
18. V_{DD}
19. $V_{OUT}D$
20. $V_{OUT}C$

Substrate (die backside) is internally connected to V_{DD}.

2

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.
WAFER TEST LIMITS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} –4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = +25°C. All specifications apply for DACs A, B, C, D.

PARAMETER	SYMBOL	CONDITIONS	PM-7226BGC LIMITS	UNITS
Total Unadjusted Error	TUE	V_{DD} = +15V	±1	LSB MAX
Relative Accuracy	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Full-Scale Error	G_{FSE}		±1	LSB MAX
Zero Code Error	V_{ZSE}		±20	mV MSX
Reference Input Voltage Range	V_{REF}		2 to (V_{DD} –4V)	V
Reference Input Resistance	R_{IN}		2	kΩ MIN
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
Positive Supply Current	I_{DD}	V_{IN} = V_{INL} or V_{INH}	12	mA MAX
Negative Supply Current	I_{SS}	V_{IN} = V_{INL} or I_{INH}, V_{SS} = –5V	10	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

otherwise noted)

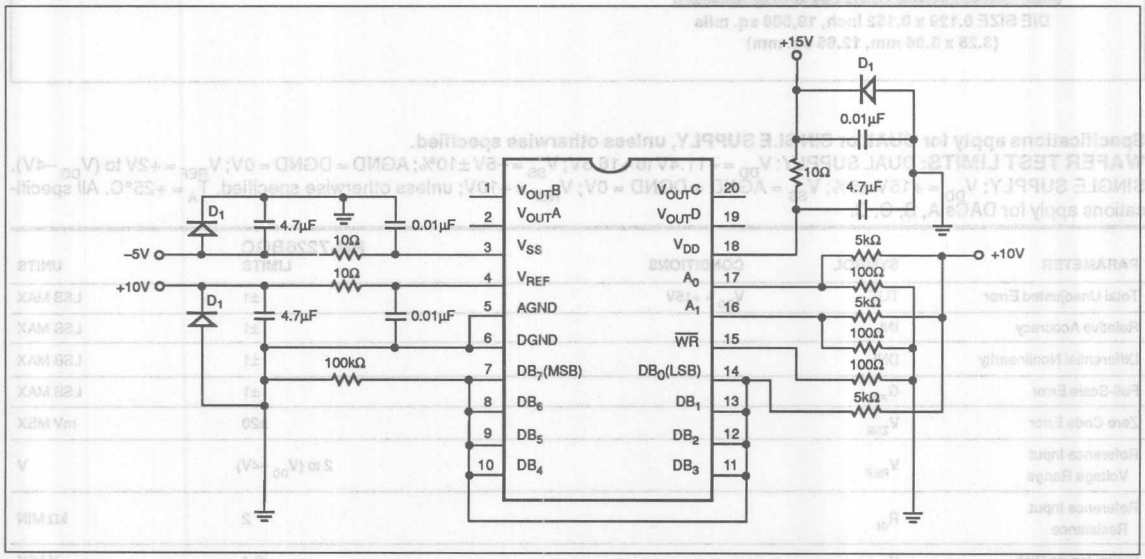
V_{DD} to AGND or DGND ..... –0.3V, +17V
V_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND or DGND ..... –0.3V, V_{DD}
Digital Input Voltage to DGND ..... –0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... –0.3V, V_{DD}
V_{OUT} to AGND (Note 1)
Operating Temperature
AR/BR Versions ..... –55°C to +125°C
ER/FR/FP/FPC/FS/AFR/AFP Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 5)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTES:

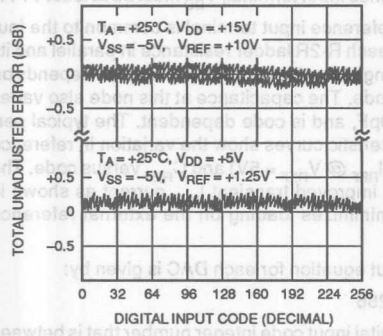
1. Outputs may be shortened to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper antistatic handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
5. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

BURN-IN CIRCUIT

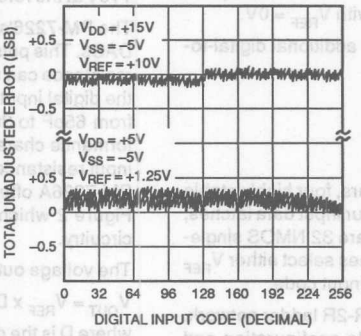


TYPICAL PERFORMANCE CHARACTERISTICS

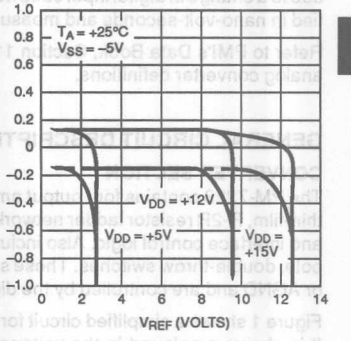
CHANNEL-TO-CHANNEL MATCHING (DACs A, B, C, D SUPERIMPOSED)



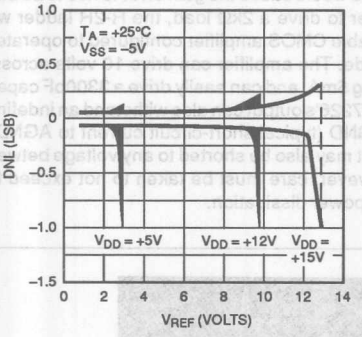
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT T_A = –55°C, +25°C, +125°C (ALL SUPERIMPOSED)



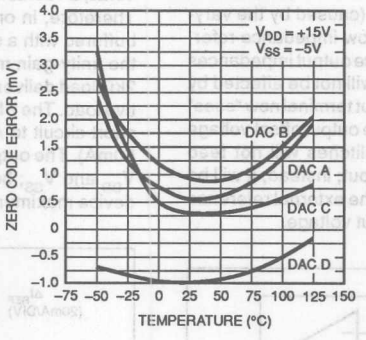
RELATIVE ACCURACY vs V_{REF}



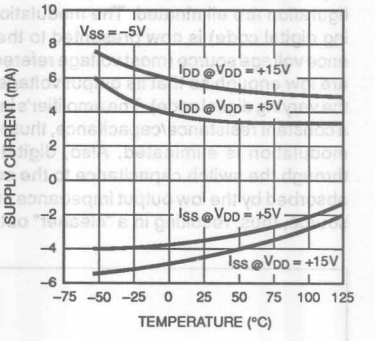
DIFFERENTIAL NONLINEARITY vs V_{REF}



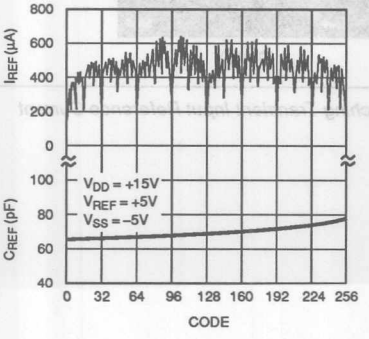
ZERO CODE ERROR vs TEMPERATURE



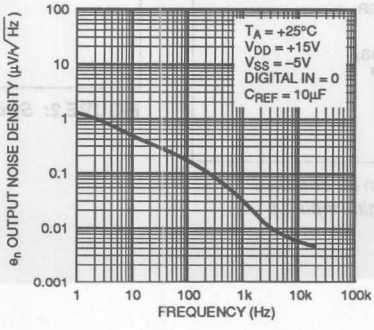
SUPPLY CURRENT vs TEMPERATURE



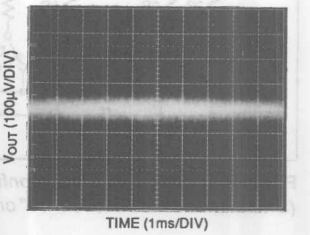
REFERENCE INPUT CURRENT AND CAPACITANCE vs CODE



V_{OUT} NOISE DENSITY vs FREQUENCY



BROADBAND NOISE (DC TO 200kHz)



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes full-scale error, relative accuracy, and zero code error. Ideal full-scale output is V_{REF} – 1 LSB, and 1 LSB is V_{REF} x (2^{-n}).

DIGITAL CROSSTALK

Digital crosstalk is the signal coupled to the output of one DAC due to a change in digital input code from other DACs. It is specified in nano-volt-seconds and measured with V_{REF} = 0V.

Refer to PMI's Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7226 contains four output amplifiers, four highly stable thin-film, R-2R resistor ladder networks, four input data latches, and interface control logic. Also included are 32 NMOS single-pole, double-throw switches. These switches select either V_{REF} or AGND and are controlled by the digital input code.

Figure 1 shows a simplified circuit for the R-2R ladder network. It is shown employed in the voltage mode configuration and connected to an amplifier. The advantages gained in operating the ladder in the voltage mode are twofold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low impedance reference voltage source (most voltage reference output impedances are low enough so that its output voltage will not be affected by the varying digital code). The amplifier's input terminal now "sees" a constant resistance/capacitance, thus the output offset voltage modulation is eliminated. Also, digital glitches will not feed through the switch capacitance to the output; instead, it will be absorbed by the low output impedance of the external reference source, thus, resulting in a "cleaner" output voltage.

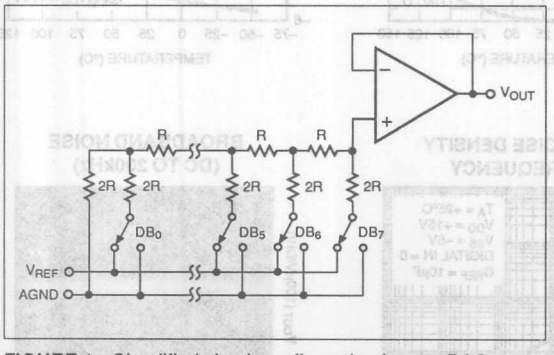


FIGURE 1: *Simplified circuit configuration for one DAC. (Switches are shown for all "1s" on the digital inputs.)*

Note in Figure 1 that the amplifier is configured to operate as a buffer amplifier; no signal inversion takes place from input to output (V_{REF} to V_{OUT}). Also note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the application section on AGND Biasing.

For proper operation, V_{REF} maximum should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The PM-7226's reference input terminal is common to the four DACs. This puts each R-2R ladder resistance in parallel and its resistance can range from 2kΩ to infinity; the value depends on the digital input code. The capacitance at this node also varies from 65pF to 300pF, and is code dependent. The typical performance characteristic curves show the variation in reference input resistance (I_{REF} @ V_{REF} = 5V) and C_{REF} versus code. The PM-7226A offers improved transient I_{REF} current as shown in Figure 2 which minimizes loading on the external reference circuitry.

The voltage output equation for each DAC is given by:

$V_{OUT} = V_{REF} \times D/256$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

Each R-2R resistor ladder network has a typical resistance of 10kΩ; a 100kΩ load would cause the gain error to rise to 23 LSB. Therefore, in order to drive a 2kΩ load, the R-2R ladder was buffered with a stable CMOS amplifier configured to operate in the unity-gain mode. The amplifier can drive 10 volts across a 2kΩ load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7226's output can also withstand an indefinite short circuit to AGND (typical short-circuit current to AGND is 50mA). The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

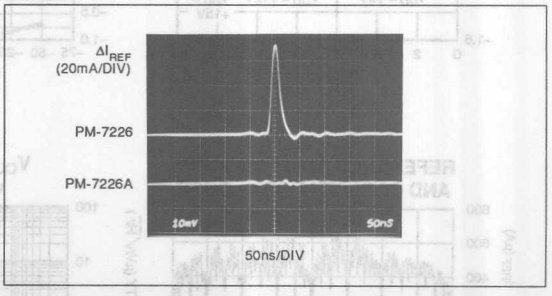


FIGURE 2: *Switching Transient Input Reference Current*

The amplifier's output stage uses an intrinsic NPN bipolar transistor. This transistor provides a low impedance, high output current capability using a small part of the chip area. The transistor is derived from the P–well and the substrate. The emitter of this NPN transistor is loaded with a 450µA NMOS current source referenced to V_{SS}. This allows 450µA to be sunk to the negative supply allowing the amplifier's output to go directly to ground.

A simplified circuit of the output amplifier is shown in Figure 3. Note how the current source is connected between the parasitic NPN output transistor's emitter and V_{SS}. Figure 4 shows a typical plot of the DAC's current sink capability versus output voltage; note that it is for a dual and single supply operation. Let's take a closer look at what happens to its behavior by referring to Figure 4.

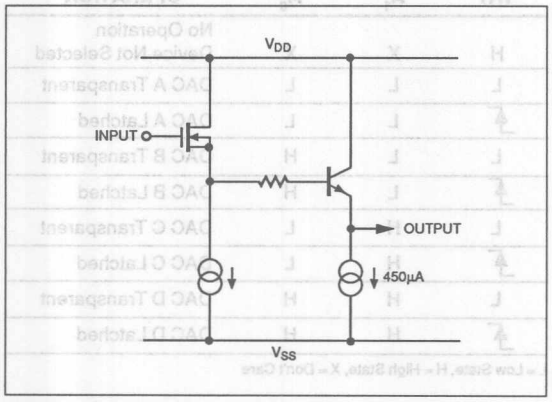


FIGURE 3: *Amplifier Output Stage*

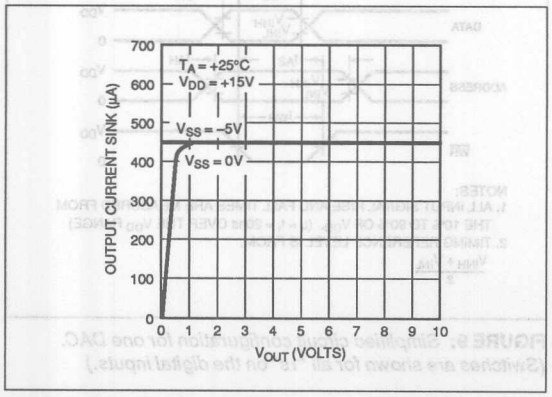


FIGURE 4: *DAC Output Current Sink*

With a dual supply, the current source is still in its high impedance (saturation) state when the output is at 0V. Therefore, the current source has 5V of bias in dual supply operation. When V_{SS} = 0V, however, the current sink capability is reduced as the output voltage approaches 0V; the current source is coming out of its saturation region and starts appearing resistive.

The amplifier's current limiting and buffering abilities are achieved by using an NMOS transistor and a series resistor. The transistor is configured as a source follower and is driving the resistor and NPN output transistor. This is also shown in Figure 3.

Figure 5 displays the combined amplifier source and sink capability to the point of current limiting. This plot was made with the digital inputs set at zero code. Note that the maximum source current available is dependent on the V_{DD} supply voltage.

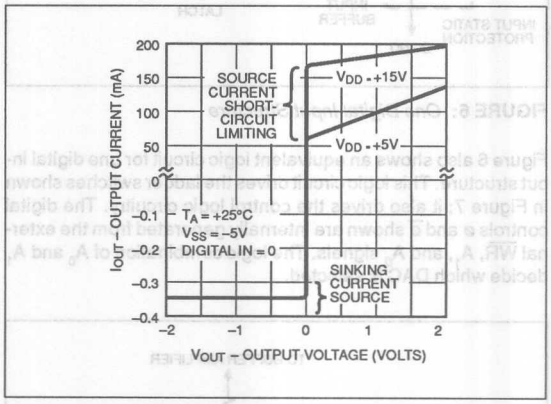


FIGURE 5: *Output Sink-Source Current vs. Voltage*

The amplifier's internal gain stages were designed so that they maintain good gain over its common-mode range; the objective was to maintain good offset performance over the specified voltage range. The amplifier's offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The effect of amplifier offset is included in the data sheet under "total unadjusted error" specification.

DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed such that TTL and CMOS (5V) input levels are converted into internal CMOS logic levels; they are used to drive the internal circuitry. A simple 5V regulator is used to ensure the high-speed timing.

The PM-7226's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. The inputs are protected from electrostatic discharge and build-up with two internal distributed diodes; they are connected from V_{DD} and DGND to each CMOS input gate. Each input has a typical input current of less than 1nA. A simplified input protection scheme is shown in Figure 6.

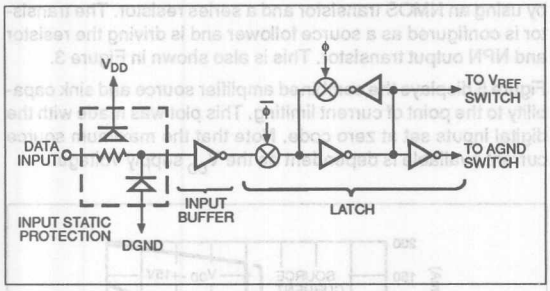


FIGURE 6: *One Digital Input Structure*

Figure 6 also shows an equivalent logic circuit for one digital input structure. This logic circuit drives the ladder switches shown in Figure 7; it also drives the control logic circuitry. The digital controls ø and $\overline{ø}$ shown are internally generated from the external $\overline{WR}$, A_1, and A_0 signals. The logic combination of A_0 and A_1 decide which DAC is selected.

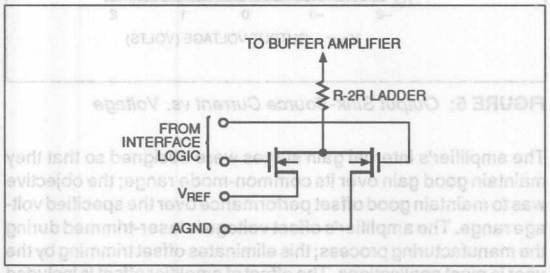


FIGURE 7: *Simplified N-Channel Voltage Steering Switches*

INTERFACE CONTROL LOGIC SECTION

Figure 8 shows the PM-7226's input control logic, and Table 1 the DAC control table. The address lines A_0 and A_1 determines which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation.

Figure 9 shows the PM-7226's write timing diagram. It shows that the selected DAC is transparent when the $\overline{WR}$ signal is low. Some bus systems do not always have data valid for the entire period during which the $\overline{WR}$ signal is low. This allows invalid data to briefly appear at the DAC's digital inputs and cause unwanted glitches at the output. Retiming the write pulse ($\overline{WR}$) so that it only occurs when data is valid will eliminate this problem.

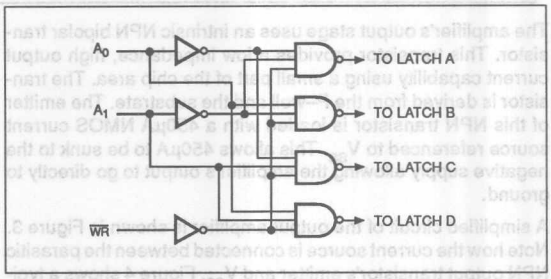


FIGURE 8: *Input Control Logic*

TABLE 1: DAC Control Table

LOGIC CONTROL $\overline{WR}$	A_1	A_0	PM-7226 OPERATION
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
↑	L	L	DAC A Latched
L	L	H	DAC B Transparent
↑	L	H	DAC B Latched
L	H	L	DAC C Transparent
↑	H	L	DAC C Latched
L	H	H	DAC D Transparent
↑	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

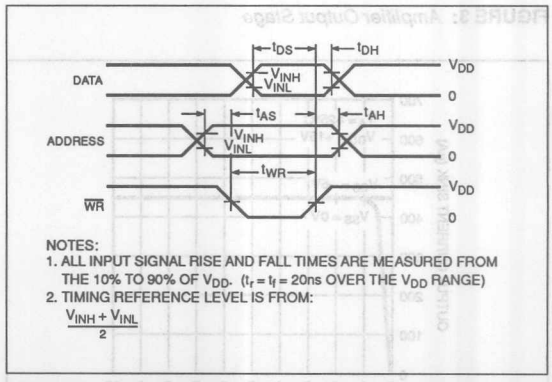


FIGURE 9: *Simplified circuit configuration for one DAC. (Switches are shown for all "1s" on the digital inputs.)*

APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7226 data sheet is specified with dual and single power supply conditions. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V, and a negative supply (V_{SS}) of –5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to V_{SS} –4V. For those applications requiring +10V at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits.

The specified V_{REF} for the single supply specifications is +10V. The V_{REF} voltage range for both dual and single power supply applications must be observed if the PM-7226's multiplying capabilities are to be preserved.

Although the PM-7226 can operate with either a single or dual power supply, improved zero-code error can be obtained by using dual supplies.

DYNAMIC PERFORMANCE

The PM-7226's settling time is limited by the internal amplifier's slew rate as shown in Figure 10. Depicted is the dynamic response for a positive full-scale output voltage swing. Figure 10c shows the expanded view with no evidence of signal overshoot or ringing; note that the typical settling time is 1.85µs. An expanded view of the negative full-scale output voltage swing is shown in Figure 10b. It also shows overshoot at a minimum, and the typical settling time is 2.6µs.

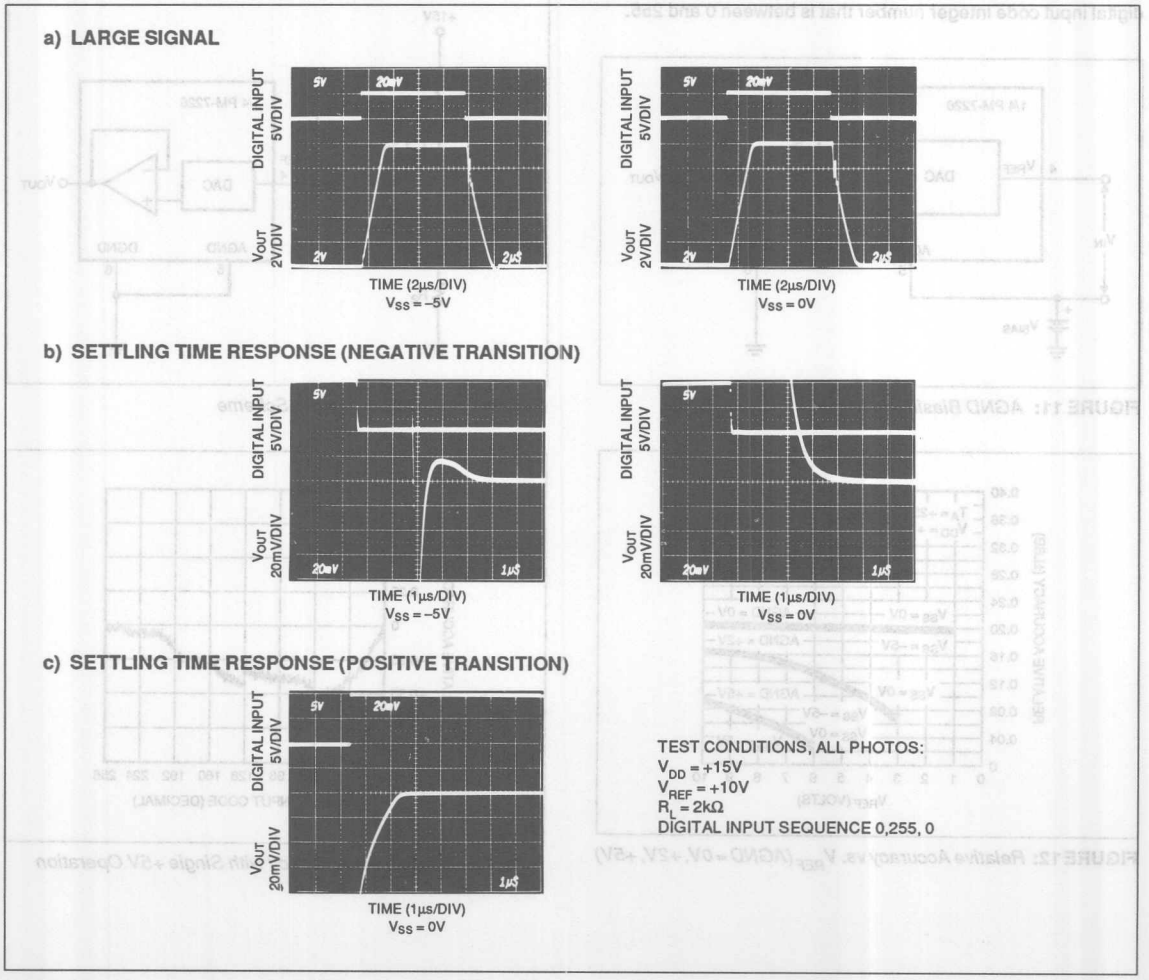


FIGURE 10: *Dynamic Response*

AGND BIASING

Some applications may require the DAC's output voltage level to be offset above ground. This is easily accomplished with the PM-7226; the desired DC offset voltage can be applied to the AGND pin. Raising AGND above DGND affects all four DACs because AGND is common to them. The digital input voltage levels are not affected. Figure 11 shows the circuit configuration and Figure 12 shows the relative accuracy with AGND biased at 0V, +2V, and +5V. The graph shows both a dual and single supply operation with V_{DD} at +15V. It is important to remember that other parameters degrade more pronouncedly than relative accuracy. Note, V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:

$V_{OUT} = AGND\ bias + V_{IN} \times D/256$

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

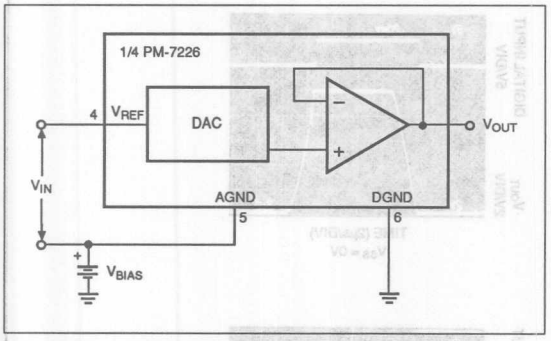


FIGURE 11: *AGND Biasing Scheme*

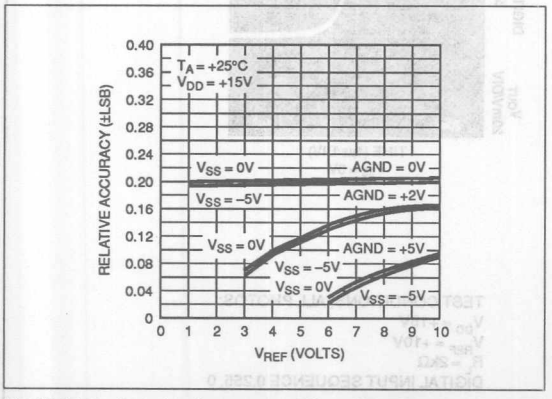


FIGURE 12: *Relative Accuracy vs. V_{REF} (AGND = 0V, +2V, +5V)*

MULTIPLYING OPERATION

Good multiplying capabilities are realized with the PM-7226 if the reference signal level is kept within +2V and V_{DD} –4V. The maximum input signal level is +12.5V for a V_{DD} supply voltage of +16.5V; however, it is recommended that V_{DD} = +15V ±5% and the AC voltage swing vary from +2V to +11V. The signal must be AC coupled and biased up with a voltage divider as shown in Figure 13. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance (the R-2R ladder input resistance varies from 2kΩ to infinity) does not load the resistor divider.

The V_{REF} small-signal frequency response (–3dB bandwidth) for the PM-7226 is typically 1.5MHz. Its small-signal harmonic distortion is less than –57dB at 1kHz and –55dB at 100kHz.

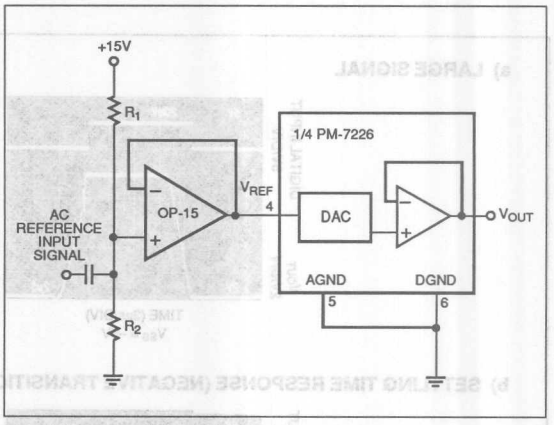


FIGURE 13: *AC Signal Input Scheme*

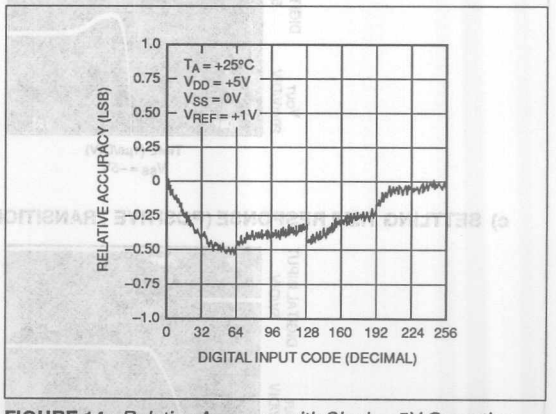


FIGURE 14: *Relative Accuracy with Single +5V Operation*

+5V SINGLE SUPPLY OPERATION

Operation of the improved PM-7226A at a +5V V_{DD} is guaranteed in the separate specification table. Linearity performance specified by DNL is still maintained within ±1 LSB maximum. DNL and offset performance is improved with a –5V supply, see graph in Typical Performance Characteristics section. Input reference voltages must be limited to 1.3V maximum with V_{DD} = 5V. Microprocessor interface timing is slower, but guaranteed to the values provided.

GENERAL GROUND MANAGEMENT

Ground management implies the placement of a system's analog and digital ground currents. Analog and digital ground returns are a source of system errors and must be addressed. Remember, the analog signal is only as good as the integrity of its analog ground.

Different ground management techniques are used depending on the size and type of the overall system. Proper grounding techniques require tying the analog and digital grounds together at the DAC's socket, and each ground return line be brought out separately to their respective power supply grounds. Tying the grounds together at the device socket and at the power supplies, or at more than one location, can create ground loops. This causes noisy digital ground currents to flow through the analog ground paths destroying the analog's ground integrity. Voltage differences of millivolts (and hundreds of millivolts in some systems) can be found in these ground paths.

Other sources of system errors can be introduced by the product of ground noise currents and ground bus impedances. Using large conductors or ground planes between the converter and power supplies will minimize the ground impedances and thus, reduce system errors.

If system requirements dictate the use of common return lines to the power supplies for both the analog and digital grounds, the converter should then be placed as close to the power supplies as possible.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance. These transients and oscillations can also cause system errors.

Bypassing the PM-7226 at the socket with only high frequency decoupling capacitors may not remove these oscillations. An LC tank circuit can be formed by the stray power lead inductance and capacitance. These reactive components can allow oscillations to occur during a digital current step. It is necessary, then, to remove or lower the tank's resonant frequency. The easiest method is to parallel the high frequency decoupling capacitor with a low frequency capacitor.

The high frequency decoupling capacitors should be ceramic and in the range of 0.01µF; the low frequency decoupling capacitors should be tantalum and between 1 to 10µF as close as possible to the device socket.

BASIC APPLICATIONS

UNIPOLAR OPERATION

Figure 15 shows the PM-7226 configured in the unipolar mode of operation; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation.

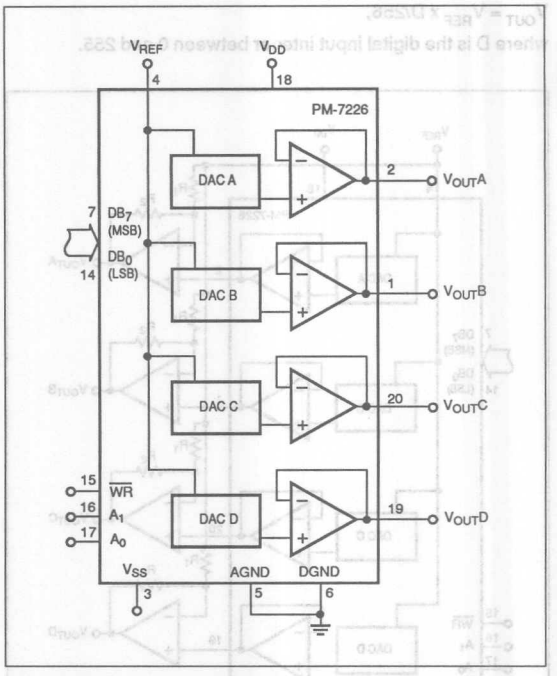


FIGURE 15: *Unipolar Operation*

TABLE 2: Unipolar Code Table (Refer to Figure 15)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT (DAC A, B, C, or D)
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right) = \frac{+V_{REF}}{2}$
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

The table shows that there is no signal inversion between $+V_{REF}$ and V_{OUT}. Note that the analog output voltage is equal to V_{REF} multiplied by the digital input code (hence, multiplying DAC).

The expression for 1 LSB and V_{OUT} is:

1 LSB = $V_{REF} \times 2^{-8}$, or $V_{REF} \times 1/256$

and

$V_{OUT} = V_{REF} \times D/256$,

where D is the digital input integer between 0 and 255.

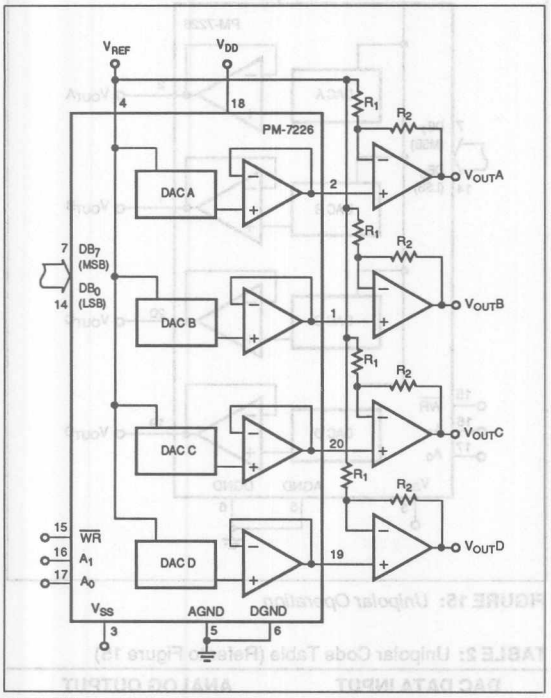


FIGURE 16: *Bipolar Operation*

TABLE 3: Bipolar Code Table (Refer to Figure 16)

DAC DATA INPUT MSB LSB	ANALOG OUTPUT (DAC A, B, C, or D)
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

BIPOLAR OPERATION

Figure 16 illustrates the PM-7226 in the bipolar mode of operation. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; this can be seen in Table 3. This configuration requires an external amplifier and two resistors for each channel requiring bipolar operation.

The output voltage expression is given by:

$V_{OUT} = \left((1 + R_2/R_1) \times D/256 \times V_{REF}\right) - (R_2/R_1 \times V_{REF})$

where D is the digital input code integer between 0 and 255. If $R_1 = R_2$, then V_{OUT} becomes:

$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$

To keep gain and offset errors at a minimum, R_1 and R_2 should be matched to ±0.1% and track over the operating temperature range of interest.

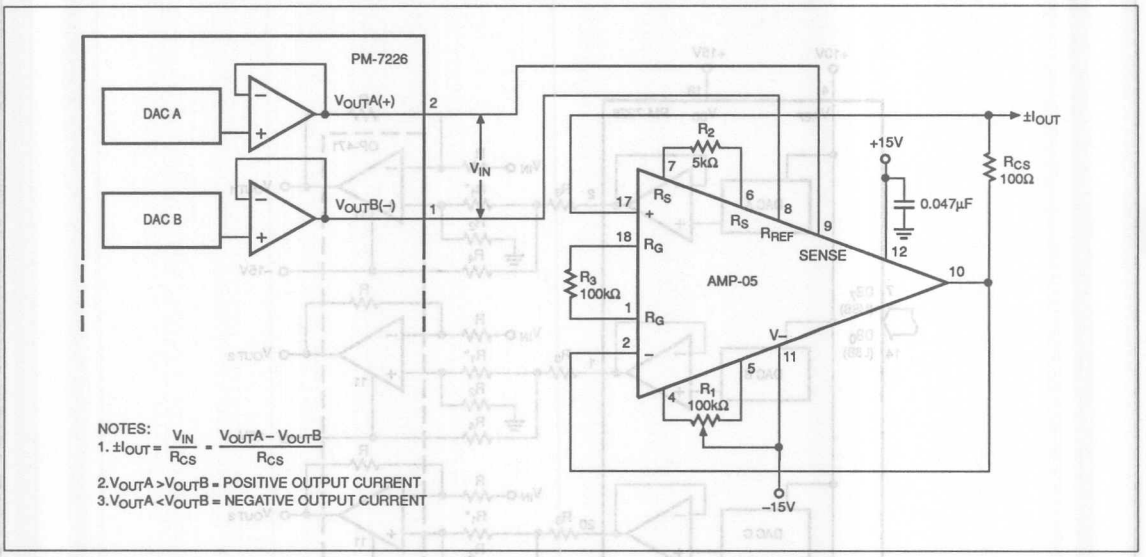


FIGURE 17: *High-Compliance, Digitally-Controlled Current Source*

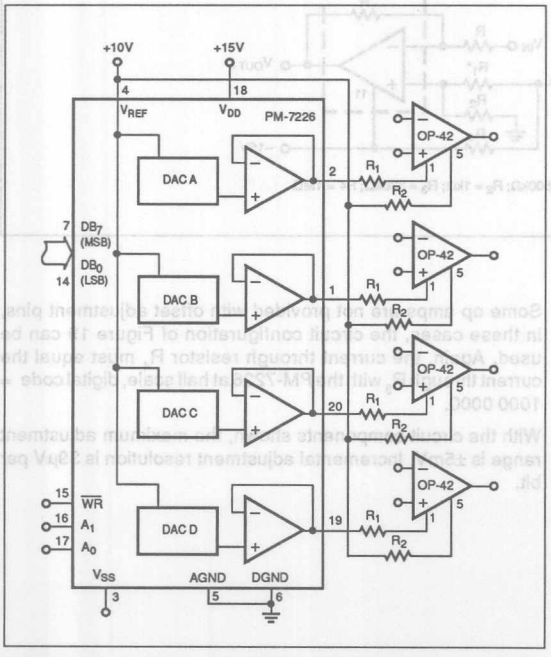


FIGURE 18: *Op Amp Offset Adjust (See Text)*

HIGH-COMPLIANCE BIPOLAR PRECISION CURRENT-SOURCE

Figure 17 shows the PM-7226 controlling a high-compliance, bipolar precision current source using PMI's AMP-05 instrumentation amplifier. The AMP-05's reference and sense pins become differential inputs, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS} in Figure 17. Voltage gain is set at unity, so the transfer function is simply: $I_{OUT} = (V_{OUT}A - V_{OUT}B)/R_{CS}$. Using a 100Ω resistor for R_{CS} limits the output current to ±10mA with a ±1V input.

Potentiometer R_1 trims the output current to zero with the two inputs at 0V. Fine gain adjustment may be accomplished by trimming R_2 or R_3.

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7226 can be used for op amp offset trimming adjustments under microprocessor control. Offset caused by temperature drifts can be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7226 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 18. A fixed bias current is provided to pin 5 of the op amps offset null pins with R_2, and R_1 (connected to the DAC's voltage output pin) providing the variable current to pin 1.

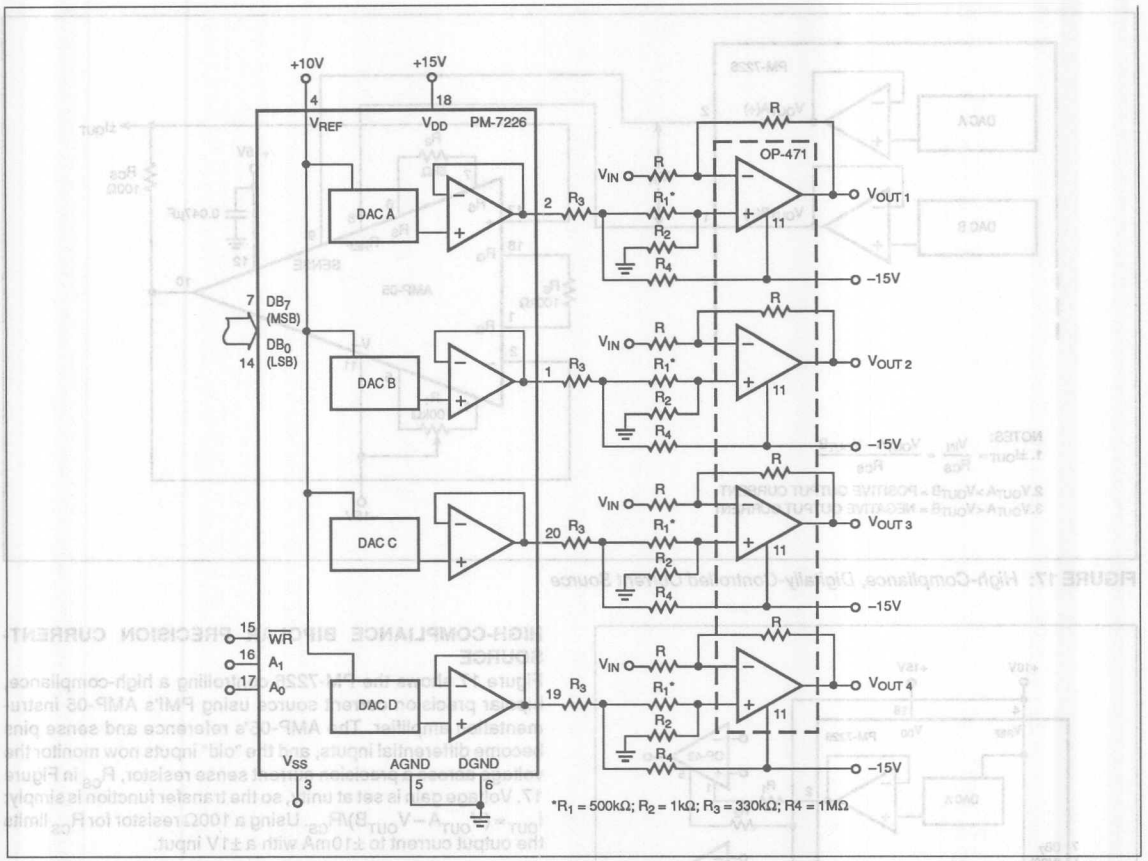


FIGURE 19: *Alternate Offset Adjust (See Text)*

In order to have a plus or minus (±) offset adjust control, the current through R_1 must equal the current through R_2 when the PM-7226 is at half scale, binary code = 1000 0000.

The resistor values (R_1, R_2) should be chosen to give the required offset adjustment range desired. Lower values provide a larger range; however, resolution will be sacrificed. Reversing connections at pins 1 and 5 (of the op amp) will reverse the offset adjustment direction.

Some op amps are not provided with offset adjustment pins, in these cases, the circuit configuration of Figure 19 can be used. Again, the current through resistor R_4 must equal the current through R_3 with the PM-7226 at half scale, digital code = 1000 0000.

With the circuit components shown, the maximum adjustment range is ±5mV. Incremental adjustment resolution is 39µV per bit.

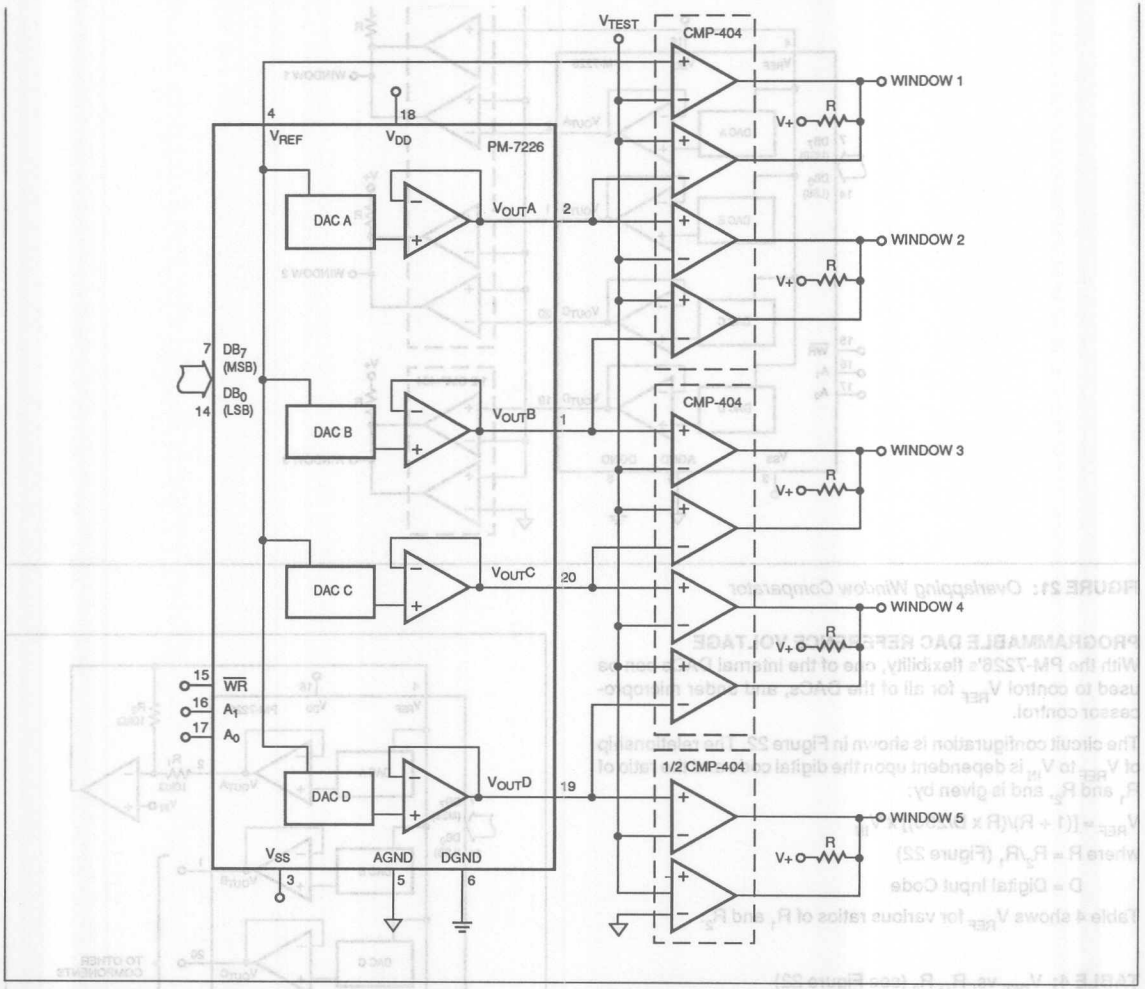


FIGURE 20: *Non-Overlapping Window Comparator*

STAIRCASE WINDOW COMPARATOR

Many applications need to determine whether voltage levels are within predetermined limits. Some requirements are for non-overlapping windows and others for overlapping windows. Both circuit configurations are shown in Figures 20 and 21, respectively.

The non-overlapping circuit uses one PM-7226 and ten comparators; this allows for five voltage windows. These windows range between V_{REF} and analog ground. Figure 20 shows that the first window is between V_{REF} and $V_{OUT}A$. $V_{OUT}A$ is also the upper limit of window 2, the lower limit being $V_{OUT}B$, etc. These limits (window size) can be microprocessor controlled. The relationship $V_{REF} > V_{TEST} > AGND$ apply.

More versatility can be obtained by connecting the output of DAC D ($V_{OUT}D$) to V_{REF}; this allows V_{REF} (which is common to all four DACs) to be under microprocessor control (see Programmable DAC Reference Voltage section). This, however, reduces the windows to four. Overlapping windows (Figure 21) will reduce the windows to three.

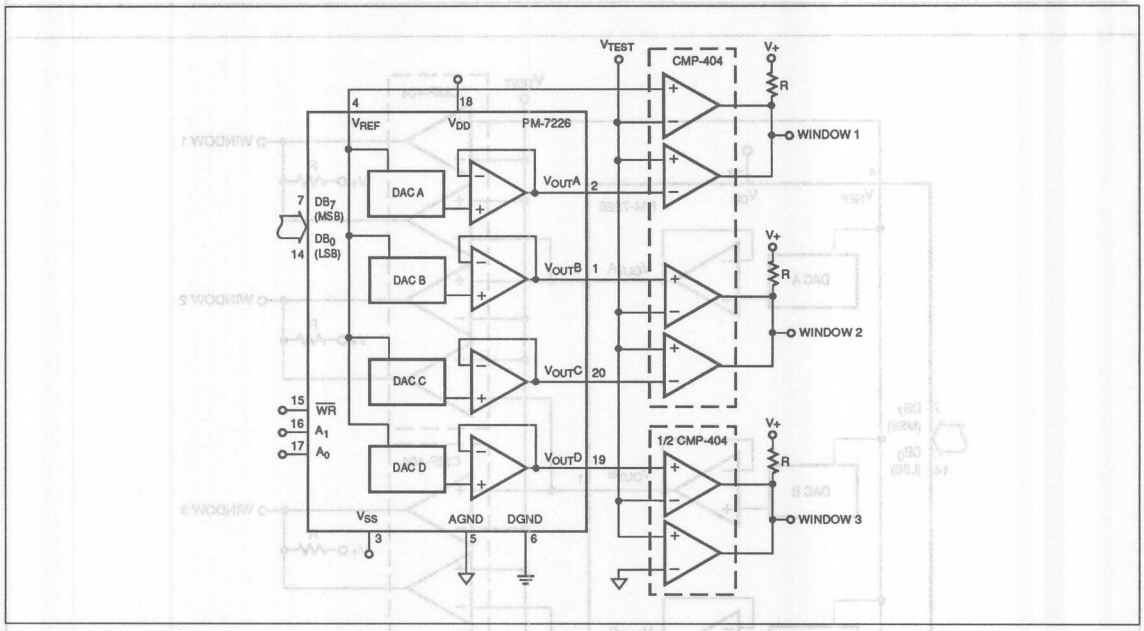


FIGURE 21: *Overlapping Window Comparator*

PROGRAMMABLE DAC REFERENCE VOLTAGE

With the PM-7226's flexibility, one of the internal DACs can be used to control V_{REF} for all of the DACs, and under microprocessor control.

The circuit configuration is shown in Figure 22. The relationship of V_{REF} to V_{IN} is dependent upon the digital code and the ratio of R_1 and R_2, and is given by:

$$V_{REF} = [(1 + R)/(R \times D/256)] \times V_{IN}$$

where $R = R_2/R_1$ (Figure 22)

D = Digital Input Code

Table 4 shows V_{REF} for various ratios of R_1 and R_2.

TABLE 4: V_{REF} vs. R_1, R_2 (see Figure 22)

R_1, R_2	DIGITAL INPUT CODE	V_{REF}
$R_1 = R_2$	0000 0000 (0/256)	$2V_{IN}$
$R_1 = R_2$	1000 0000 (128/256)	$1.3V_{IN}$
$R_1 = R_2$	1111 1111 (255/256)	V_{IN}
$R_2 = 3R_1$	0000 0000 (0/256)	$4V_{IN}$
$R_2 = 3R_1$	1000 0000 (128/256)	$1.6V_{IN}$
$R_2 = 3R_1$	1111 1111 (255/256)	V_{IN}

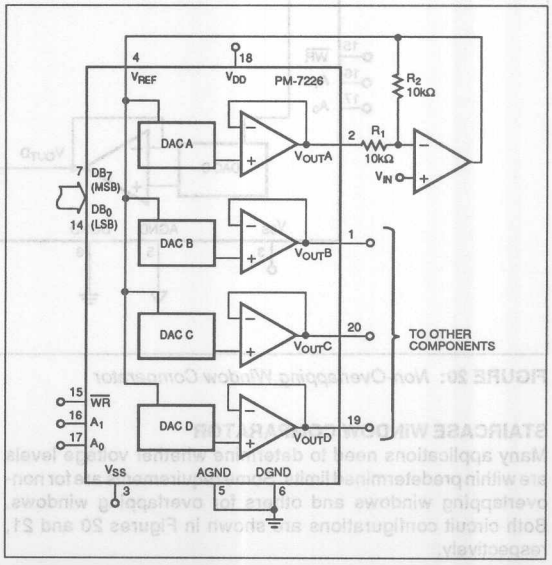


FIGURE 22: *Programmable DAC Reference*

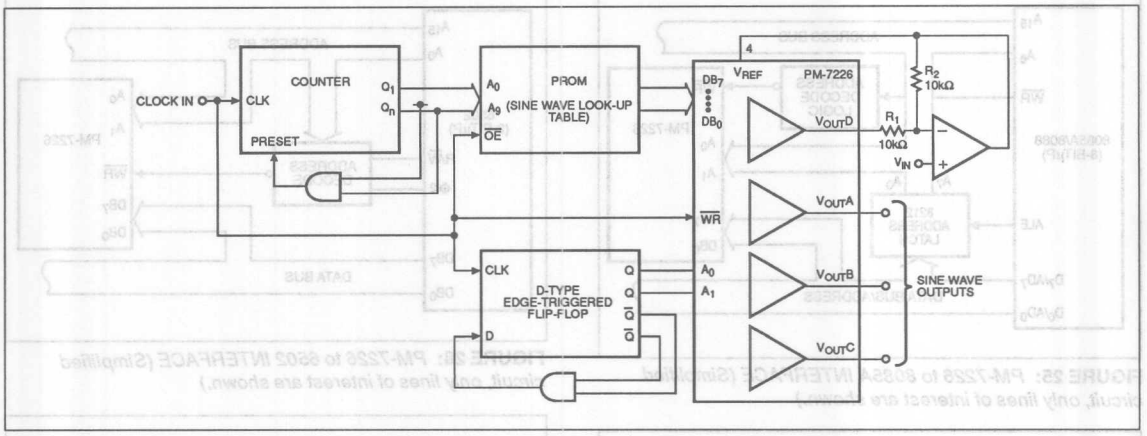


FIGURE 23: *3-Phase Sine Wave Generator Circuit (Using Counter)*

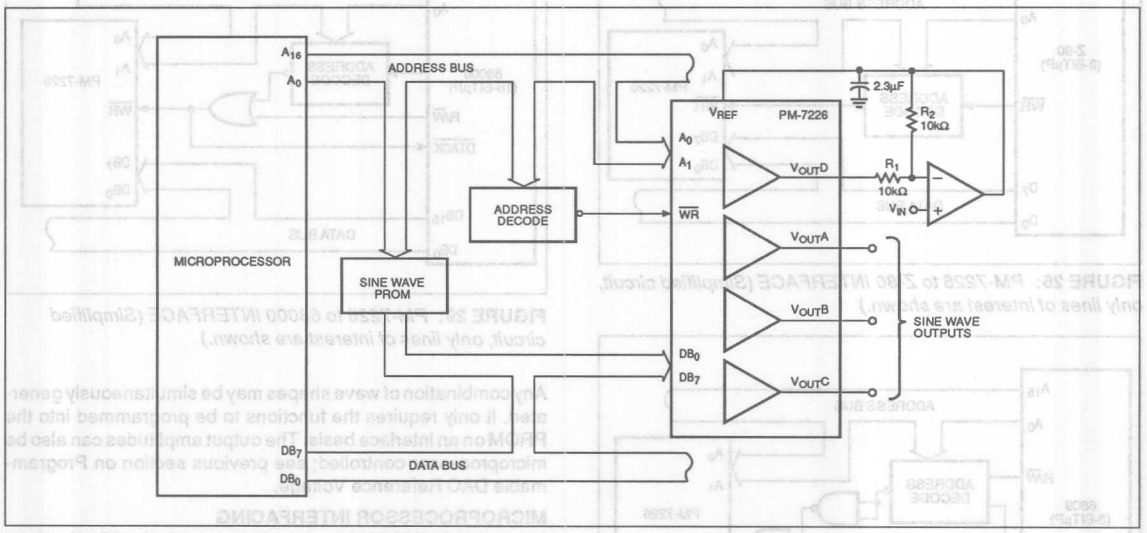


FIGURE 24: *3-Phase Sine Wave Generator Circuit (Under Microprocessor Control)*

This application works best with dual supplies. This is due to the DAC's output-current sink capability as V_{OUT} approaches 0V.

3-PHASE SINE WAVE GENERATION

The PM-7226 is well suited for 3-phase sine wave generation and with amplitude control. These sine waves can be used to control a shaft's rotational angle in small 3-phase synchro motors; some applications are antennas, robotics, and process controls. Other waveforms (such as triangular) may also be generated. The concept revolves around a PROM, counter, and a clock (or a microprocessor).

The sine wave codes are stored in a PROM in sets of three. Each set is 120° apart and has a 1.4° resolution (360°/256). These codes will use 768 memory address spaces (256 x 3).

Figure 23 shows the circuit using a counter, flip-flop, and a PROM; note that a clock is used to control the circuit. The counter counts through the PROM's addresses until the counter has stepped through the PROM's full look-up table; this completes a full cycle. The counter then resets and begins the cycle again when the last address data has been loaded into the PM-7226.

Sine wave generation can also be under microprocessor control; see Figure 24. The processor's software runs 3 phases to three DACs. Each phase is drawn from the PROM's look-up table.

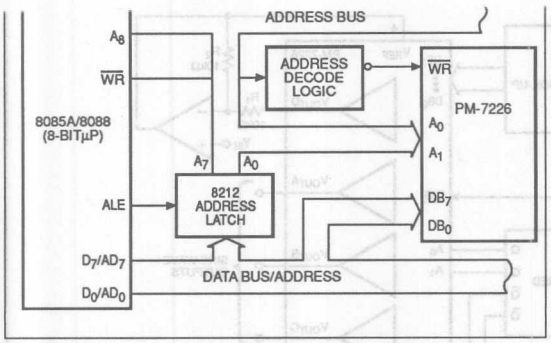


FIGURE 25: *PM-7226 to 8085A INTERFACE (Simplified circuit, only lines of interest are shown.)*

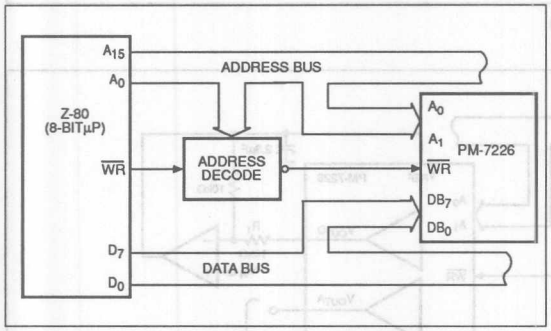


FIGURE 26: *PM-7226 to Z-80 INTERFACE (Simplified circuit, only lines of interest are shown.)*

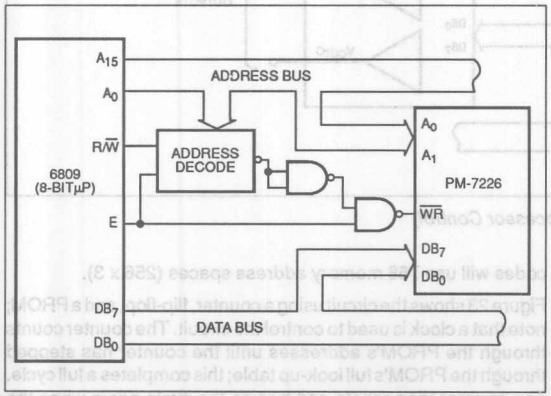


FIGURE 27: *PM-7226 to 6809 INTERFACE (Simplified circuit, only lines of interest are shown.)*

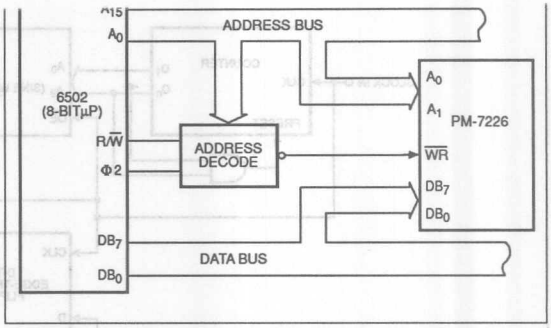


FIGURE 28: *PM-7226 to 6502 INTERFACE (Simplified circuit, only lines of interest are shown.)*

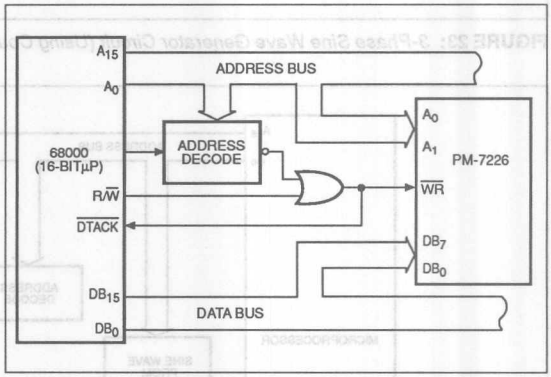


FIGURE 29: *PM-7226 to 68000 INTERFACE (Simplified circuit, only lines of interest are shown.)*

Any combination of wave shapes may be simultaneously generated. It only requires the functions to be programmed into the PROM on an interlace basis. The output amplitudes can also be microprocessor controlled; see previous section on Programmable DAC Reference Voltage.

MICROPROCESSOR INTERFACING

Interfacing the PM-7226 to a microprocessor is simplified by virtue of its loading structure simplicity. Data is loaded into the DAC by use of only three control lines, the write strobe ($\overline{WR}$) and two DAC selection control signals (A_0, A_1).

Figures 25 through 29 show various popular microprocessor interface configurations.

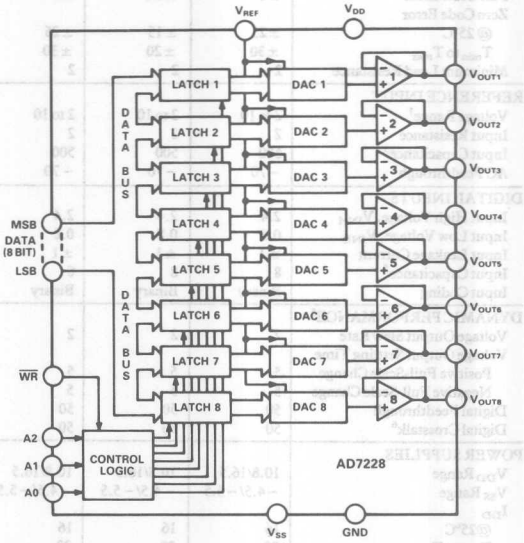
Octal 8-Bit DAC

AD7228

FEATURES

Eight 8-Bit DACs with Output Amplifiers
Operates with Single or Dual Supplies
µP Compatible (95ns $\overline{WR}$ Pulse)
No User Trims Required
Extended Temperature Range Operation
Skinny 24-Pin DIP, SOIC and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7228 contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228 is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC^2MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its DIP and SOIC pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility
   The AD7228 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

AD7228—SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 10.8V to 16.5V; V_{SS} = −5V ±10%; GND = 0V; V_{REF} = +2V to +10V;[1] R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B Versions[2]	L, C Versions	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 10%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5ppm/°C with V_{REF} = +10V
Zero Code Error						
@ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30μV/°C
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V_{min} to V_{max}	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	−70	−70	−70	−70	dB typ	V_{REF} = 8V p-p Sine Wave @ 10kHz/
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	14	14	14	14	mA max	
T_{min} to T_{max}	18	18	20	20	mA max	

SINGLE SUPPLY[7] (V_{DD} = +15V ±10%, V_{SS} = GND = 0V; V_{REF} = +10V; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	Settling Time to ±1/2LSB
Negative Full-Scale Change	7	7	7	7	μs max	Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V.
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	

NOTES
[1]V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
[4]Calculated after zero code error has been adjusted out.
[5]Sample tested at 25°C to ensure compliance.
[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.
[7]Single +5V operation is also possible with degraded performance (see Figure 14).
Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1, 2] (See Figures 1, 2; V_{DD} = +10.8V to +16.5V; V_{SS} = 0V or −5V ±10%)

Parameters	Limit at 25°C All Grades	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	70	90	100	ns min	Data Valid to $\overline{WR}$ Setup Time
t_4	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_5	95	120	150	ns min	Write Pulse Width

NOTES
[1]Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5$ns.
[2]Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$

INTERFACE LOGIC INFORMATION

Address lines A0, A1 and A2 select which DAC accepts data from the input port. Table I shows the selection table for the eight DACs with Figure 1 showing the input control logic. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7228 Control Inputs				AD7228
$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

Table I. AD7228 Truth Table

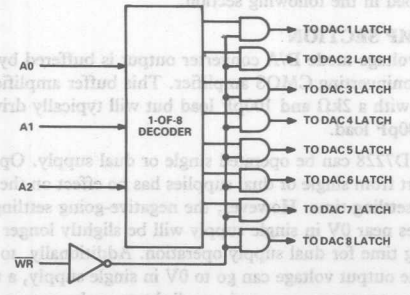
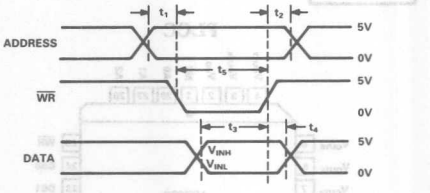


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Figure 2. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +24V
Digital Input Voltage to GND . . . . . −0.3V, V_{DD} +0.3V
V_{REF} to GND . . . . . −0.3V, V_{DD} +0.3V
V_{OUT} to GND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 1000mW
Derates above 75°C by . . . . . 2.0mW/°C
Operating Temperature
Commercial . . . . . −40°C to +85°C
Industrial . . . . . −40°C to +85°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

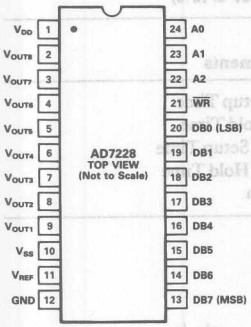
NOTE
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to GND or V_{SS} is 50mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

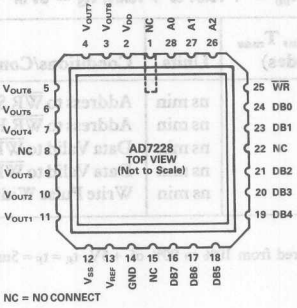
CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



DIP AND SOIC

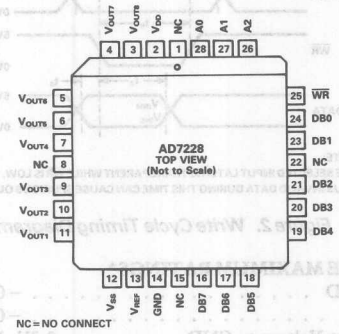


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7228KN	−40°C to +85°C	±2LSB	N-24
AD7228LN	−40°C to +85°C	±1LSB	N-24
AD7228KP	−40°C to +85°C	±2LSB	P-28A
AD7228LP	−40°C to +85°C	±1LSB	P-28A
AD7228KR	−40°C to +85°C	±2LSB	R-24
AD7228LR	−40°C to +85°C	±1LSB	R-24
AD7228BQ	−40°C to +85°C	±2LSB	Q-24
AD7228CQ	−40°C to +85°C	±1LSB	Q-24
AD7228TQ	−55°C to +125°C	±2LSB	Q-24
AD7228UQ	−55°C to +125°C	±1LSB	Q-24
AD7228TE	−55°C to +125°C	±2LSB	E-28A
AD7228UE	−55°C to +125°C	±1LSB	E-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC Drawing #5962-88663.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

D/A SECTION

The AD7228 contains eight identical, 8-bit, voltage-mode digital-to-analog converters. The output voltages from the converters have the same polarity as the reference voltage, allowing single supply operation. A novel DAC switch pair arrangement on the AD7228 allows a reference voltage range from +2V to +10V. Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS switches. The simplified circuit diagram for one channel is shown in Figure 3. Note that V_{REF} and GND are common to all eight DACs.

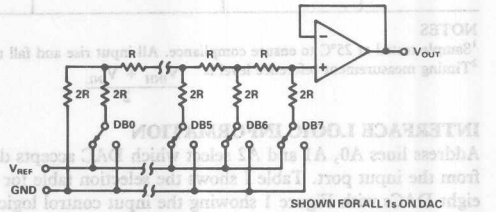


Figure 3. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7228 is the parallel combination of the eight individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance occurs when all eight DACs are loaded with digital code 01010101. Therefore, it is important that the external reference source presents a low output impedance to the V_{REF} terminal of the AD7228 under changing load conditions. Due to transient currents at the reference input during digital code changes a 0.1μF (or greater) decoupling capacitor is recommended on the V_{REF} input for dc applications. The nodal capacitance at the reference terminal is also code dependent and typically varies from 120pF to 350pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage:

$$V_{OUTN} = D_N \cdot V_{REF}$$

where D_N is a fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier as described in the following section.

OP AMP SECTION

Each voltage-mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is tested with a 2kΩ and 100pF load but will typically drive a 2kΩ and 500pF load.

The AD7228 can be operated single or dual supply. Operating the part from single or dual supplies has no effect on the positive-going settling time. However, the negative-going settling time to voltages near 0V in single supply will be slightly longer than the settling time for dual supply operation. Additionally, to ensure that the output voltage can go to 0V in single supply, a transistor on the output acts as a passive pull-down as the output voltage nears 0V. As a result, the sink capability of the amplifier is reduced as the output voltage nears 0V in single supply. In dual supply operation, the full sink capability of 400μA at 25°C is maintained over the entire output voltage range. The single supply output sink capability is shown in Figure 4. The negative V_{SS} also gives improved output amplifier performance allowing an extended input reference voltage range and giving improved slew rate at the output.

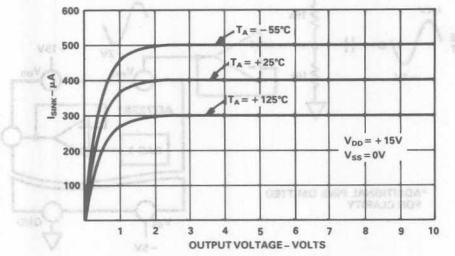


Figure 4. Single Supply Sink Current

The output broadband noise from the amplifier is 300µV peak-to-peak. Figure 5 shows a plot of noise spectral density versus frequency.

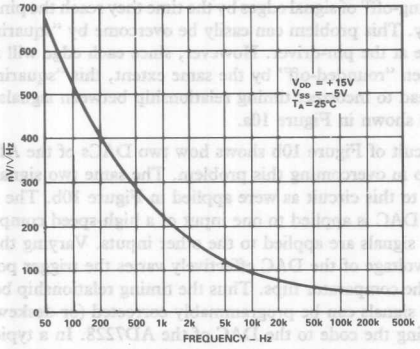


Figure 5. Noise Spectral Density vs. Frequency

DIGITAL INPUTS

The AD7228 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by on-chip distributed diodes.

SUPPLY CURRENT

The AD7228 has a maximum I_{DD} specification of 22mA and a maximum I_{SS} of 20mA over the −55°C to +125°C temperature range. This maximum current specification is actually determined by the current at −55°C. Figure 6 shows a typical plot of power supply current versus temperature.

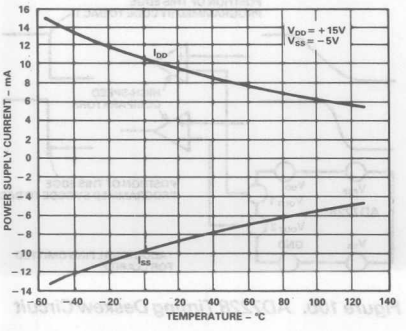


Figure 6. Power Supply Current vs. Temperature

APPLYING THE AD7228

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7228, with the output voltage having the same positive polarity as V_{REF}. Connections for unipolar output operation are shown in Figure 7. The AD7228 can be operated from single or dual supplies as outlined earlier. The voltage at the reference input must never be negative with respect to GND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

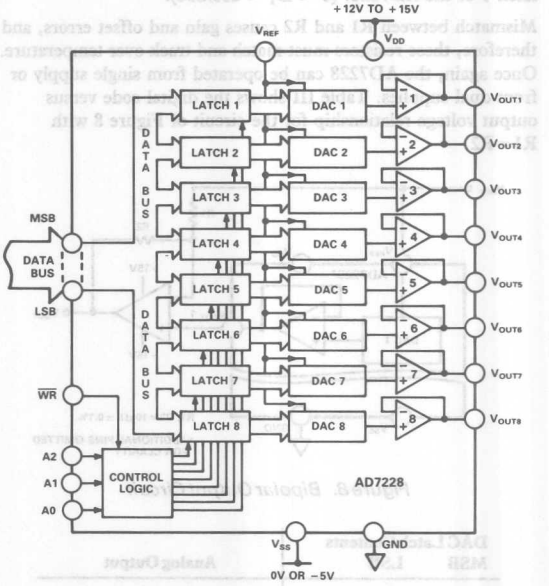


Figure 7. Unipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs on the AD7228 can be individually configured for bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 8 shows a circuit used to implement offset binary coding (bipolar operation) with DAC 1 of the AD7228. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_1 \cdot V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_1 - 1) \cdot (V_{REF})$$

where D_1 is a fractional representation of the digital word in latch 1 of the AD7228. ($0 \leq D_1 \leq 255/256$).

Mismatch between R1 and R2 causes gain and offset errors, and therefore, these resistors must match and track over temperature. Once again, the AD7228 can be operated from single supply or from dual supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 8 with R1 = R2.

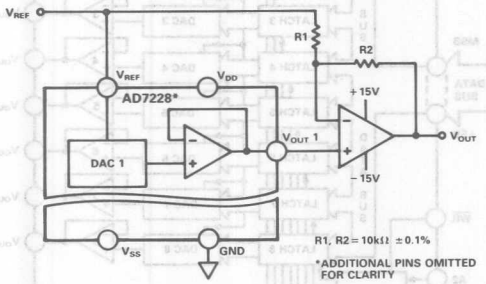


Figure 8. Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar Code Table

AC REFERENCE SIGNAL

In some applications it may be desirable to have an ac signal applied as the reference input to the AD7228. The AD7228 has multiplying capability within the upper (+10V) and lower (+2V) limits of reference voltage when operated with dual supplies. Therefore, ac signals need to be ac coupled and biased up before being applied to the reference input. Figure 9 shows a sine-wave signal applied to the reference input of the AD7228. For input frequencies up to 50kHz, the output distortion typically remains less than 0.1%. The typical 3dB bandwidth for small signal inputs is 800kHz.

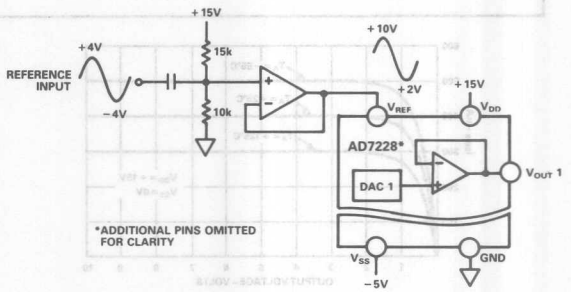


Figure 9. Applying a AC Signal to the AD7228

TIMING DESKEW

A common problem in ATE applications is the slowing or "rounding-off" of signal edges by the time they reach the pin-driver circuitry. This problem can easily be overcome by "squaring-up" the edge at the pin-driver. However, since each edge will not have been "rounded-off" by the same extent, this "squaring-up" could lead to incorrect timing relationship between signals. This effect is shown in Figure 10a.

The circuit of Figure 10b shows how two DACs of the AD7228 can help in overcoming this problem. The same two signals are applied to this circuit as were applied in Figure 10b. The output of each DAC is applied to one input of a high-speed comparator, and the signals are applied to the other inputs. Varying the output voltage of the DAC effectively varies the trigger point at which the comparator flips. Thus the timing relationship between the two signals can be programmably corrected (or deskewed) by varying the code to the DAC of the AD7228. In a typical application, the code is loaded to the DACs for correct timing relationships during the calibration cycle of the instrument.

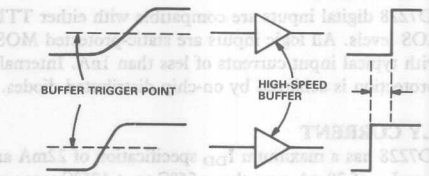


Figure 10a. Time Skewing Due to Slowing of Edges

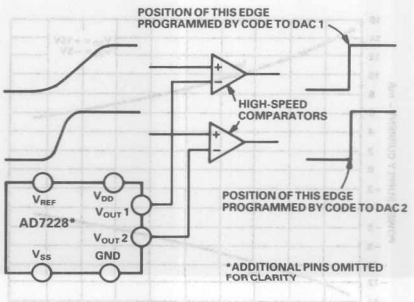


Figure 10b. AD7228 Timing Deskew Circuit

COARSE/FINE ADJUST

The DACs on the AD7228 can be paired together to form a coarse/fine adjust function as indicated in Figure 11. The function is achieved using one external op amp and a few resistors per pair of DACs.

DAC1 is the most significant or coarse DAC. Data is first loaded to this DAC to coarsely set the output voltage. DAC2 is then used to fine tune this output voltage. Varying the ratio of R1 to R2 varies the relative effect of the coarse and fine DACs on the output voltage. For the resistor values shown, DAC2 has a resolution of 150μV in a 10V output range. Since each DAC on the AD7228 is guaranteed monotonic, the coarse adjustment and fine adjustment are each monotonic. One application for this is as a set-point controller (see "Circuit Applications of the AD7226 Quad CMOS DAC" available from Analog Devices, Publication Number E873-15-11/84).

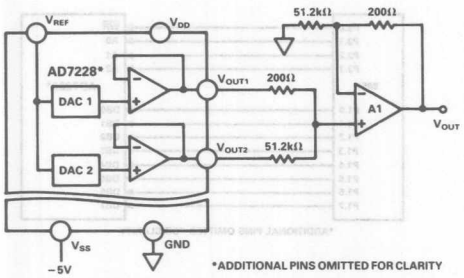


Figure 11. Coarse/Fine Adjust Circuit

SELF-PROGRAMMABLE REFERENCE

The circuit of Figure 12 shows how one DAC of the AD7228, in this case DAC1, may be used in a feedback configuration to provide a programmable reference for itself and the other seven converters. The relationship of V_{REF} to V_{IN} is expressed by

$$V_{REF} = \frac{(1+G)}{(1+G \cdot D_1)} \cdot V_{IN} \quad \text{where } G = R2/R1$$

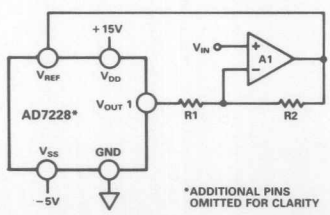


Figure 12. Self-Programmable Reference

Figure 13 shows typical plots of V_{REF} versus digital code, D_1, for three different values of G. With V_{IN} = 2.5V and G = 3 the voltage at the output varies between 2.5V and 10V giving an effective 10-bit dynamic range to the other seven converters. For correct operation of the circuit, V_{SS} should be −5V and R1 greater than 6.8kΩ.

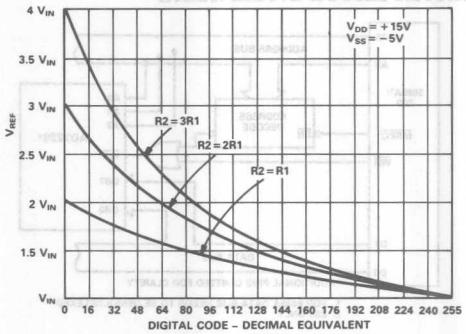


Figure 13. Variation of V_{REF} with Feedback Configuration

5V SINGLE SUPPLY OPERATION

The AD7228 can be operated from a single +5V power supply resulting in only slightly degraded accuracy performance from the part. Figure 14 shows a typical plot of relative accuracy for the part with 5V V_{DD} and a reference voltage of +1.23V. One important parameter which retains its specified performance is differential nonlinearity which remains within ±1LSB ensuring that the DACs on the AD7228 remain monotonic over the output voltage range.

The output transfer function sits on top of the amplifier offset voltage. Since the reference voltage is reduced, the offset voltage amounts to a few LSBs. For parts with a true negative offset (when V_{SS} = −5V), the transfer function does not move off the bottom rail for the first few LSBs of code. After this the transfer function will continue as normal. The relative accuracy plot of Figure 14 is for a part with a true positive offset.

The required overhead voltage of 3.5V must be maintained between V_{DD} and the reference voltage which limits the reference voltage range. However, operating the part from a single +5V supply gives a considerable reduction in power dissipation (to typically 50mW). The digital input threshold levels and digital input currents are not affected by operating the part from the single +5V supply.

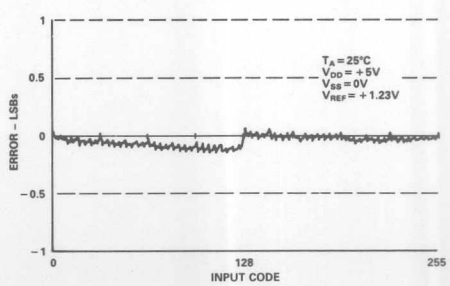


Figure 14. Relative Accuracy at +5V V_{DD}

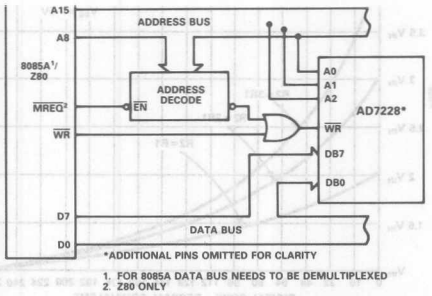


Figure 15. AD7228 to 8085A/Z80 Interface

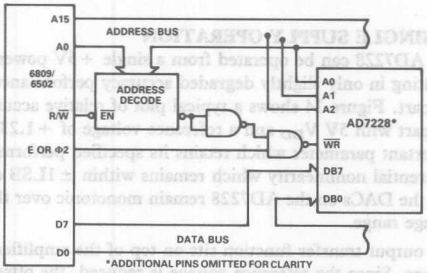


Figure 16. AD7228 to 6809/6502 Interface

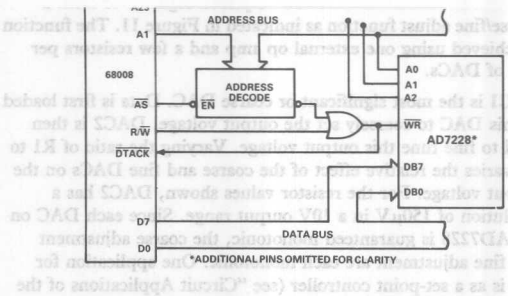


Figure 17. AD7228 to 68008 Interface

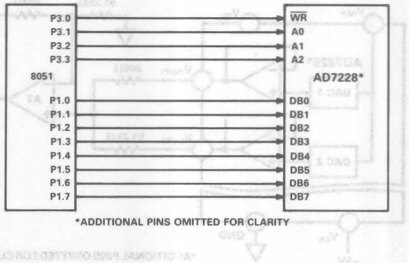


Figure 18. AD7228 to MCS-51 Interface

ANALOG DEVICES

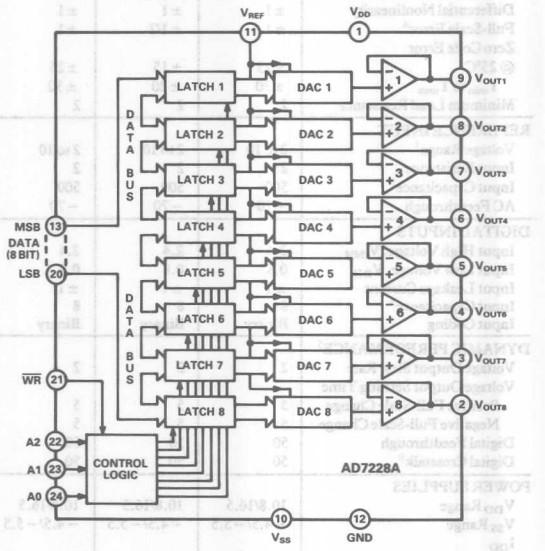
LC²MOS Octal 8-Bit DAC

AD7228A

FEATURES

Eight 8-Bit DACs with Output Amplifiers
Operates with Single or Dual Supplies
µP Compatible (95ns $\overline{WR}$ Pulse)
No User Trims Required
Skinny 24-Pin DIPs, SOIC, and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7228A contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply +15V operation using a reference of +10V and single supply +5V operation using a reference of +1.23V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228A is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228A. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility
   The AD7228A has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

AD7228A—SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 10.8V to 16.5V; V_{SS} = −5V ±10%; GND = 0V; V_{REF} = +2V to +10V[1]; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AB Version[2]	AC Version	AT Version	AU Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 10%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5ppm/°C with V_{REF} = +10V
Zero Code Error						
@ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30μV/°C
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V_{min} to V_{max}	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	−70	−70	−70	−70	dB typ	V_{REF} = 8V p-p Sine Wave @ 10kHz/
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	14	14	14	14	mA max	
T_{min} to T_{max}	18	18	20	20	mA max	

SINGLE SUPPLY[7] (V_{DD} = +15V ±10%, V_{SS} = GND = 0V; V_{REF} = +10V; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	Settling Time to ±1/2LSB
Negative Full-Scale Change	7	7	7	7	μs max	Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V.
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	

NOTES
[1]V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
[2]Temperature ranges are as follows:
AB, C Versions; −40°C to +85°C
AT, U Versions; −55°C to +125°C
[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
[4]Calculated after zero code error has been adjusted out.
[5]Sample tested at 25°C to ensure compliance.
[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.
[7]Single +5V operation is also possible with degraded performance (see Figure 14).
Specifications subject to change without notice.

+5V SUPPLY OPERATION (V_{DD} = +5V ± 5%, V_{SS} = 0 to −5V ± 10%, GND = 0V, V_{REF} = +1.25V, R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7228AB	AD7228AC	AD7228AT	AD7228AU	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy	±2	±2	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±4	±2	±4	±2	LSB max	
Zero Code Error						
@ 25°C	±30	±20	±30	±20	mV max	
T_{min} to T_{max}	±40	±30	±40	±30	mV max	
REFERENCE INPUT						
Reference Input Range	1.2	1.2	1.2	1.2	V min	
	1.3	1.3	1.3	1.3	V max	
Reference Input Resistance	2	2	2	2	kΩ min	
Reference Input Capacitance	500	500	500	500	pF max	
POWER REQUIREMENTS						
Positive Supply Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	For Specified Performance
Positive Supply Current						
@ 25°C	16	16	16	16	μA max	
T_{min} to T_{max}	20	20	22	22	μA max	
Negative Supply Current						
@ 25°C	14	14	14	14	μA max	
T_{min} to T_{max}	18	18	20	20	μA max	

NOTES
All other specifications as per Dual Supply Specifications except for negative full-scale settling-time when V_{SS} = 0V.
Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1, 2] (See Figures 1, 2; V_{DD} = +5V ± 5% or +10.8V to +16.5V; V_{SS} = 0V or −5V ± 10%)

Parameters	Limit at 25°C All Grades	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	70	90	100	ns min	Data Valid to $\overline{WR}$ Setup Time
t_4	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_5	95	120	150	ns min	Write Pulse Width

NOTES
[1]Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5$ns.
[2]Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$

INTERFACE LOGIC INFORMATION

Address lines A0, A1 and A2 select which DAC accepts data from the input port. Table I shows the selection table for the eight DACs with Figure 1 showing the input control logic. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7228A Control Inputs				AD7228A
$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
↑	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

Table I. AD7228A Truth Table

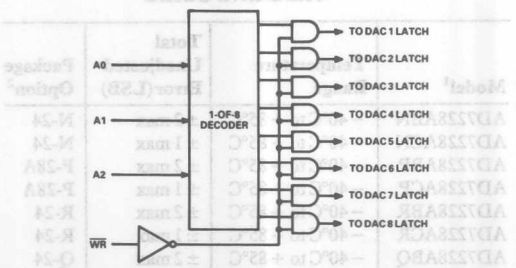
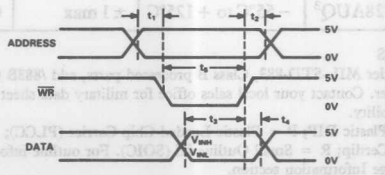


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Figure 2. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
Digital Input Voltage to GND	−0.3V, V_{DD}
V_{REF} to GND	−0.3V, V_{DD}
V_{OUT} to GND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	1000mW
Derates above 75°C by	2.0mW/°C
Operating Temperature	
Commercial	−40°C to +85°C
Industrial	−40°C to +85°C
Extended	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTE
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to GND or V_{SS} is 50mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

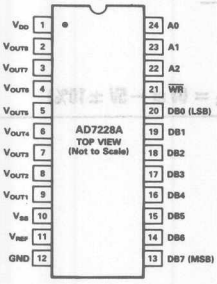
CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

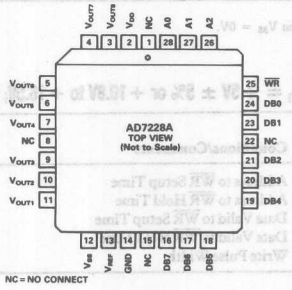


PIN CONFIGURATIONS

DIP AND SOIC



PLCC



ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7228ABN	−40°C to +85°C	±2 max	N-24
AD7228ACN	−40°C to +85°C	±1 max	N-24
AD7228ABP	−40°C to +85°C	±2 max	P-28A
AD7228ACP	−40°C to +85°C	±1 max	P-28A
AD7228ABR	−40°C to +85°C	±2 max	R-24
AD7228ACR	−40°C to +85°C	±1 max	R-24
AD7228ABQ	−40°C to +85°C	±2 max	Q-24
AD7228ACQ	−40°C to +85°C	±1 max	Q-24
AD7228ATQ[3]	−55°C to +125°C	±2 max	Q-24
AD7228AUQ[3]	−55°C to +125°C	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]These grades will be available to /883B processing only.

CIRCUIT INFORMATION
D/A SECTION

The AD7228A contains eight identical, 8-bit, voltage-mode digital-to-analog converters. The output voltages from the converters have the same polarity as the reference voltage, allowing single supply operation. A novel DAC switch pair arrangement on the AD7228A allows a reference voltage range from +2V to +10V. Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS switches. The simplified circuit diagram for one channel is shown in Figure 3. Note that V_{REF} (Pin 11) and GND (Pin 12) are common to all eight DACs.

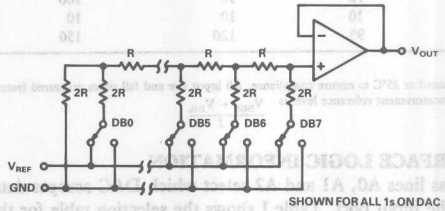


Figure 3. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7228A is the parallel combination of the eight individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance occurs when all eight DACs are loaded with digital code 01010101. Therefore, it is important that the external reference source presents a low output impedance to the V_{REF} terminal of the AD7228A under changing load conditions. Due to transient currents at the reference input during digital code changes a 0.1μF (or greater) decoupling capacitor is recommended on the V_{REF} input for dc applications. The nodal capacitance at the reference terminal is also code dependent and typically varies from 120pF to 350pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage:

$$V_{OUTN} = D_N \cdot V_{REF}$$

where D_N is a fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier as described in the following section.

OP AMP SECTION

Each voltage-mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is tested with a 2kΩ and 100pF load but will typically drive a 2kΩ and 500pF load.

The AD7228A can be operated single or dual supply. Operating the part from single or dual supplies has no effect on the positive-going settling time. However, the negative-going settling time to voltages near 0V in single supply will be slightly longer than the settling time for dual supply operation. Additionally, to ensure that the output voltage can go to 0V in single supply, a transistor on the output acts as a passive pull-down as the output voltage nears 0V. As a result, the sink capability of the amplifier is reduced as the output voltage nears 0V in single supply. In dual supply operation, the full sink capability of 400μA at 25°C is maintained over the entire output voltage range. The single supply output sink capability is shown in Figure 4. The negative V_{SS} also gives improved output amplifier performance allowing an extended input reference voltage range and giving improved slew rate at the output.

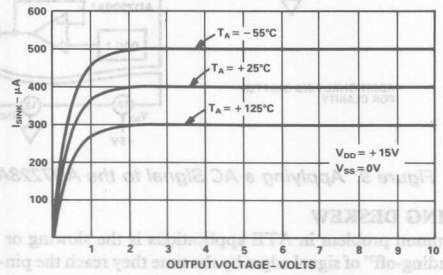


Figure 4. Single Supply Sink Current

The output broadband noise from the amplifier is 300μV peak-to-peak. Figure 5 shows a plot of noise spectral density versus frequency.

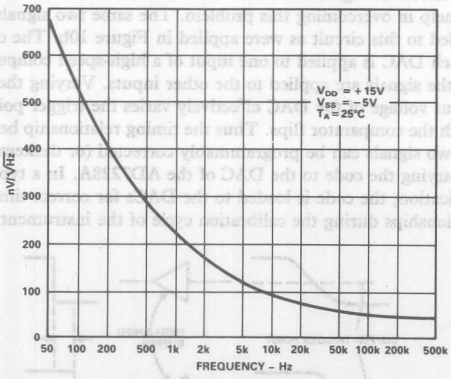


Figure 5. Noise Spectral Density vs. Frequency

DIGITAL INPUTS

The AD7228A digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by on-chip distributed diodes.

SUPPLY CURRENT

The AD7228A has a maximum I_{DD} specification of 22mA and a maximum I_{SS} of 20mA over the −55°C to +125°C temperature range. This maximum current specification is actually determined by the current at −55°C. Figure 6 shows a typical plot of power supply current versus temperature.

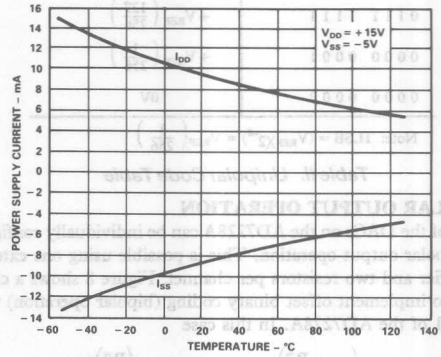


Figure 6. Power Supply Current vs. Temperature

APPLYING THE AD7228A
UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7228A, with the output voltage having the same positive polarity as V_{REF}. Connections for unipolar output operation are shown in Figure 7. The AD7228A can be operated from single or dual supplies as outlined earlier. The voltage at the reference input must never be negative with respect to GND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

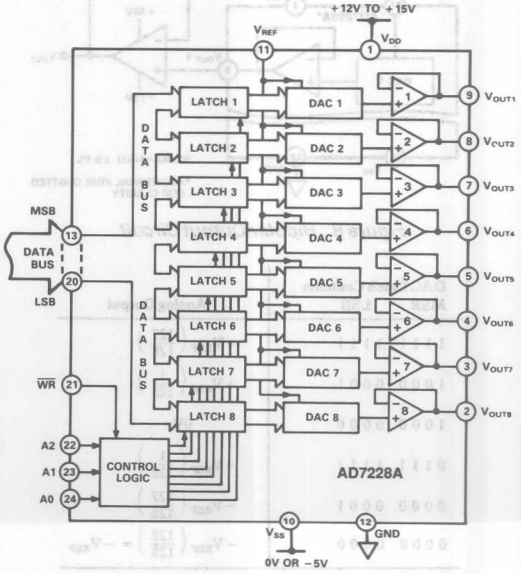


Figure 7. Unipolar Output Circuit

MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs on the AD7228A can be individually configured for bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 8 shows a circuit used to implement offset binary coding (bipolar operation) with DAC 1 of the AD7228A. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_1 \cdot V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_1 - 1) \cdot (V_{REF})$$

where D_1 is a fractional representation of the digital word in latch 1 of the AD7228A. ($0 \leq D_1 \leq 255/256$)

Mismatch between R1 and R2 causes gain and offset errors, and therefore, these resistors must match and track over temperature.

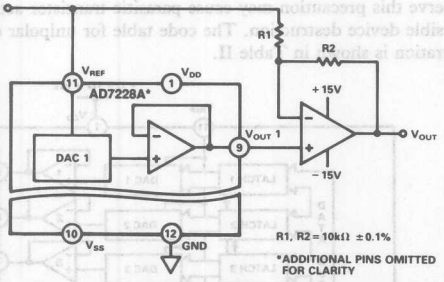


Figure 8. Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar Code Table

or from dual supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 8 with R1 = R2.

AC REFERENCE SIGNAL

In some applications it may be desirable to have an ac signal applied as the reference input to the AD7228A. The AD7228A has multiplying capability within the upper (+10V) and lower (+2V) limits of reference voltage when operated with dual supplies. Therefore, ac signals need to be ac coupled and biased up before being applied to the reference input. Figure 9 shows a sine-wave signal applied to the reference input of the AD7228A. For input frequencies up to 50kHz, the output distortion typically remains less than 0.1%. The typical 3dB bandwidth for small signal inputs is 800kHz.

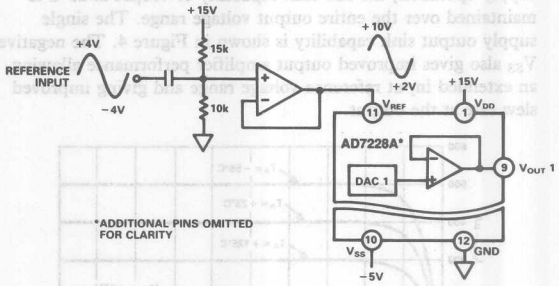


Figure 9. Applying a AC Signal to the AD7228A

TIMING DESKEW

A common problem in ATE applications is the slowing or "rounding-off" of signal edges by the time they reach the pin-driver circuitry. This problem can easily be overcome by "squaring-up" the edge at the pin-driver. However, since each edge will not have been "rounded-off" by the same extent, this "squaring-up" could lead to incorrect timing relationship between signals. This effect is shown in Figure 10a.

The circuit of Figure 10b shows how two DACs of the AD7228A can help in overcoming this problem. The same two signals are applied to this circuit as were applied in Figure 10b. The output of each DAC is applied to one input of a high-speed comparator, and the signals are applied to the other inputs. Varying the output voltage of the DAC effectively varies the trigger point at which the comparator flips. Thus the timing relationship between the two signals can be programmably corrected (or deskewed) by varying the code to the DAC of the AD7228A. In a typical application, the code is loaded to the DACs for correct timing relationships during the calibration cycle of the instrument.

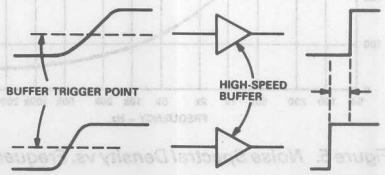


Figure 10a. Time Skewing Due to Slowing of Edges

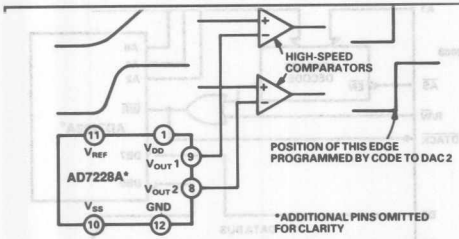


Figure 10b. AD7228A Timing Deskew Circuit

COARSE/FINE ADJUST

The DACs on the AD7228A can be paired together to form a coarse/fine adjust function as indicated in Figure 11. The function is achieved using one external op amp and a few resistors per pair of DACs.

DAC1 is the most significant or coarse DAC. Data is first loaded to this DAC to coarsely set the output voltage. DAC2 is then used to fine tune this output voltage. Varying the ratio of R1 to R2 varies the relative effect of the coarse and fine DACs on the output voltage. For the resistor values shown, DAC2 has a resolution of 150μV in a 10V output range. Since each DAC on the AD7228A is guaranteed monotonic, the coarse adjustment and fine adjustment are each monotonic. One application for this is as a set-point controller (see "Circuit Applications of the AD7226 Quad CMOS DAC" available from Analog Devices, Publication Number E873-15-11/84).

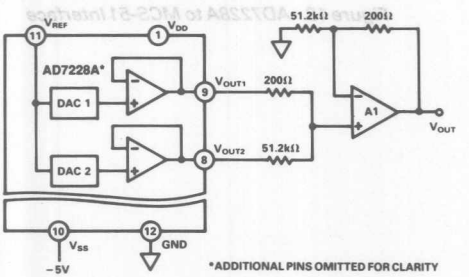


Figure 11. Coarse/Fine Adjust Circuit

SELF-PROGRAMMABLE REFERENCE

The circuit of Figure 12 shows how one DAC of the AD7228A, in this case DAC1, may be used in a feedback configuration to provide a programmable reference for itself and the other seven converters. The relationship of V_{REF} to V_{IN} is expressed by

$$V_{REF} = \frac{(1+G)}{(1+G \cdot D_1)} \cdot V_{IN} \quad \text{where } G = R2/R1$$

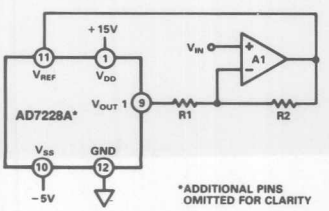


Figure 12. Self-Programmable Reference

voltage at the output varies between 2.5V and 10V giving an effective 10-bit dynamic range to the other seven converters. For correct operation of the circuit, V_{SS} should be −5V and R1 greater than 6.8kΩ.

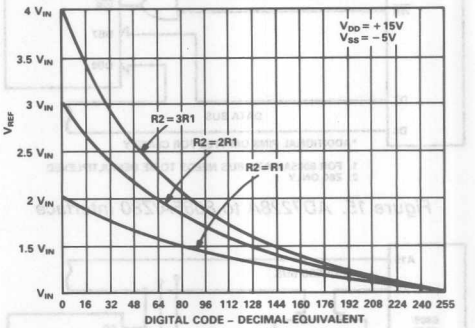


Figure 13. Variation of V_{REF} with Feedback Configuration

5V SINGLE SUPPLY OPERATION

The AD7228A can be operated from a single +5V power supply resulting in only slightly degraded accuracy performance from the part. Figure 14 shows a typical plot of relative accuracy for the part with 5V V_{DD} and a reference voltage of +1.23V. One important parameter which retains its specified performance is differential nonlinearity which remains within ±1LSB ensuring that the DACs on the AD7228A remain monotonic over the output voltage range.

The output transfer function sits on top of the amplifier offset voltage. Since the reference voltage is reduced, the offset voltage amounts to a few LSBs. For parts with a true negative offset (when $V_{SS} = -5V$), the transfer function does not move off the bottom rail for the first few LSBs of code. After this the transfer function will continue as normal. The relative accuracy plot of Figure 14 is for a part with a true positive offset.

The required overhead voltage of 3.5V must be maintained between V_{DD} and the reference voltage which limits the reference voltage range. However, operating the part from a single +5V supply gives a considerable reduction in power dissipation (to typically 50mW). The digital input threshold levels and digital input currents are not affected by operating the part from the single +5V supply.

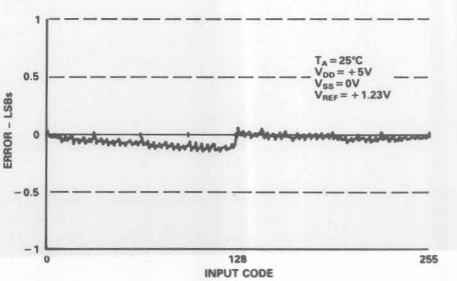


Figure 14. Relative Accuracy at +5V V_{DD}

MICROPROCESSOR INTERFACING

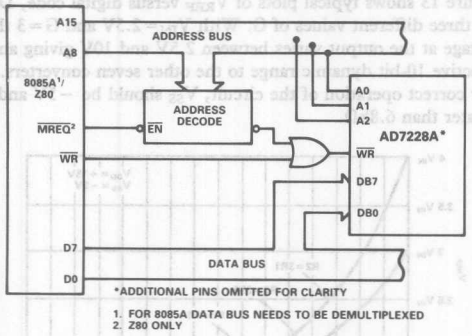


Figure 15. AD7228A to 8085A/Z80 Interface

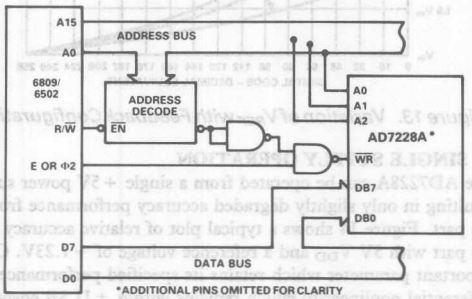


Figure 16. AD7228A to 6809/6502 Interface

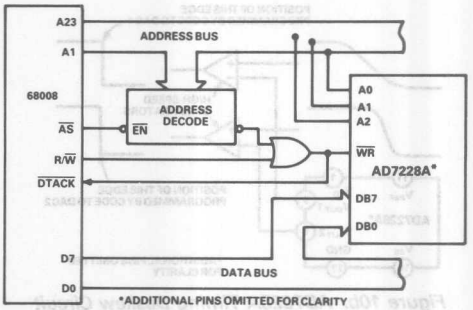


Figure 17. AD7228A to 68008 Interface

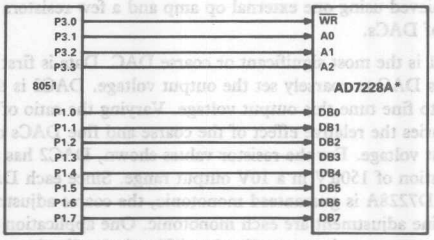


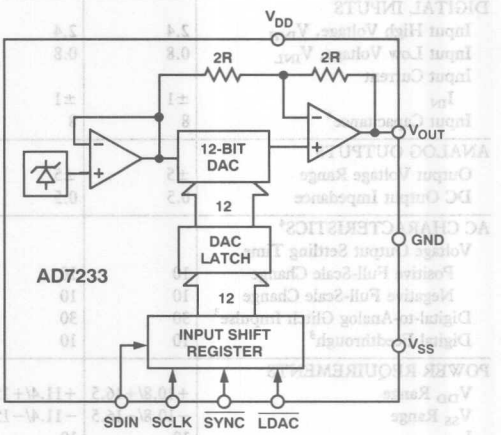
Figure 18. AD7228A to MCS-51 Interface

LC²MOS
12-Bit Serial Mini-DIP DACPORT
AD7233

FEATURES
12-Bit CMOS DAC with
On-Chip Voltage Reference
Output Amplifier
−5 V to +5 V Output Range
Serial Interface
300 kHz DAC Update Rate
Small Size : 8-Pin Mini-DIP
Nonlinearity : ±1/2 LSB T_{min} to T_{max}
Low Power Dissipation: 100 mW typical

APPLICATIONS
Process Control
Industrial Automation
Digital Signal Processing Systems
Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7233 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference all in an 8-pin package. No external trims are required to achieve full specified performance. The data format is 2s complement, and the output range is −5 V to +5 V.

The AD7233 features a fast, versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. When the $\overline{SYNC}$ input is taken low, data on the SDIN pin is clocked into the input shift register on each falling edge of SCLK. On completion of the 16-bit data transfer, bringing $\overline{LDAC}$ low updates the DAC latch with the lower 12 bits of data and updates the output. Alternatively, $\overline{LDAC}$ can be tied permanently low, and in this case the DAC register is automatically updated with the contents of the shift register when all sixteen data bits have been clocked in. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz.

For applications which require greater flexibility and unipolar output ranges with single supply operation, please refer to the AD7243 data sheet.

The AD7233 is fabricated on Linear Compatible CMOS (LC^2MOS), an advanced, mixed-technology process. It is packaged in an 8-pin DIP package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT™
   The AD7233 is a complete, voltage output, 12-bit DAC on a single chip. This single-chip design is inherently more reliable than multichip designs.
2. Simple 3-Wire Interface to Most Microcontrollers and DSP Processors.
3. DAC Update Rate—300 kHz.
4. Space Saving 8-Pin Package.

DACPORT is a trademark of Analog Devices, Inc.

AD7233—SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V,[2] V_{SS} = −12 V to −15 V,[2] GND= 0 V, R_L = 2 kΩ, C_L = 100 pF to GND. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A	B	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error[3]	±6	±6	LSB max	DAC Latch Contents 0000 0000 0000
Full-Scale Error[3]	±8	±8	LSB max	
Full-Scale Temperature Coefficient	±30	±30	ppm of FSR/°C typ	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN}	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[4]	8	8	pF max	
ANALOG OUTPUTS				
Output Voltage Range	±5	±5	V	
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	μs max	Typically 3 μs; DAC Latch 100. . .000 to 011. . .111
Negative Full-Scale Change	10	10	μs max	Typically 5 μs; DAC Latch 011. . .111 to 100. . .000
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and all 1s
Digital Feedthrough[3]	10	10	nV secs typ	$\overline{LDAC}$ = High
POWER REQUIREMENTS				
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range	−10.8/−16.5	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	mA max	Output Unloaded; Typically 7 mA
I_{SS}	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C.
[2]Power Supply Tolerance: A Version: ±10%; B Version: ±5%.
[3]See Terminology.
[4]Sample tested @ 25°C to ensure compliance.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7233AN	−40°C to +85°C	±1 LSB	N-8
AD7233BN	−40°C to +85°C	±1/2 LSB	N-8

*N = Plastic DIP. For outline information see Package Information section.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +10.8 V to +16.5 V, V_{SS} = −10.8 V to −16.5 V, GND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	190	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	100	100	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low

NOTES
[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 3.
[3]SCLK Mark/Space Ratio range is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . −0.3 V to +17 V
V_{SS} to GND . . . . . +0.3 V to −17 V
V_{OUT}[1] to GND . . . . . −6 V to V_{DD} +0.3 V
Digital Inputs to GND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

BIPOLAR ZERO ERROR

Bipolar zero error is the voltage measured at V_{OUT} when the DAC is loaded with all 0s. It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

FULL-SCALE ERROR

Full-scale error is a measure of the output error when the amplifier output is at full scale (full scale is either positive or negative full scale).

DIGITAL-TO-ANALOG GLITCH IMPULSE

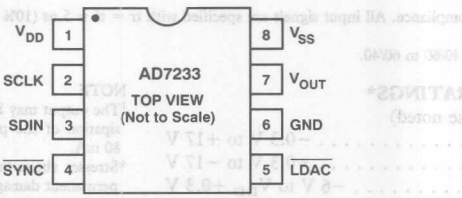
This is the voltage spike that appears at the output of the DAC when the digital code in the DAC latch changes before the output settles to its final value. The energy in the glitch is specified in nV secs, and is measured for an all codes change (0000 0000 0000 to 1111 1111 1111).

DIGITAL FEEDTHROUGH

This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7233. It is measured with $\overline{LDAC}$ held high.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{DD}	Positive Supply (+12 V to +15 V).
2	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
3	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
4	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
5	$\overline{LDAC}$	Load DAC, Logic Input. Updates the DAC output. The DAC output is updated on the falling edge of this signal, or alternatively if this line in permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK pulse.
6	GND	Ground pin = 0 V.
7	V_{OUT}	Analog Output Voltage. This is the buffered DAC output voltage (−5 V to +5 V).
8	V_{SS}	Negative Supply (−12 V to −15 V).



CIRCUIT INFORMATION

D/A Section

The AD7233 contains a 12-bit voltage-mode D/A converter consisting of highly stable thin-film resistors and high speed NMOS single-pole, double-throw switches.

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The buffer amplifier is capable of developing ±5 V across a 2 kΩ load to GND.

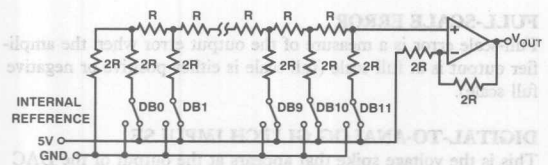


Figure 1. Simplified D/A Converter

DIGITAL INTERFACE

The AD7233 contains an input serial to parallel shift register and a DAC latch. A simplified diagram of the input loading circuitry is shown in Figure 2. Serial data on the SDIN input is loaded to the input register under control of $\overline{SYNC}$ and SCLK. When a complete word is held in the shift register it may then be loaded into the DAC latch under control of $\overline{LDAC}$. Only the data in the DAC latch determines the analog output on the AD7233.

A low $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7233 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore either a continuous clock or a burst clock source may be used to clock in the data.

The $\overline{SYNC}$ input should be taken high after the complete 16-bit word is loaded in.

Although 16 bits of data are clocked into the input register, only the latter 12 bits get transferred into the DAC latch. The first 4 bits in the 16 bit stream are don't cares since their value does not affect the DAC latch data. Therefore the data format is 4 don't cares followed by the 12-bit data word with the LSB as the last bit in the serial stream.

There are two ways in which the DAC latch and hence the analog output may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes is selected.

If $\overline{LDAC}$ = 0 then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1 then the automatic update is disabled and the DAC latch is updated by taking $\overline{LDAC}$ low any time after the 16-bit data transfer is complete. The update now occurs on the falling edge of $\overline{LDAC}$. This facility is useful for simultaneous update in multi-DAC systems. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated.

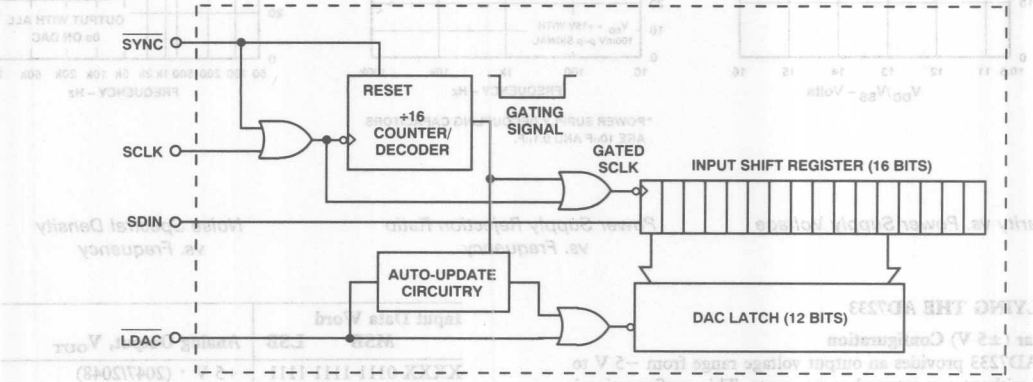


Figure 2. AD7233 Simplified Loading Structure

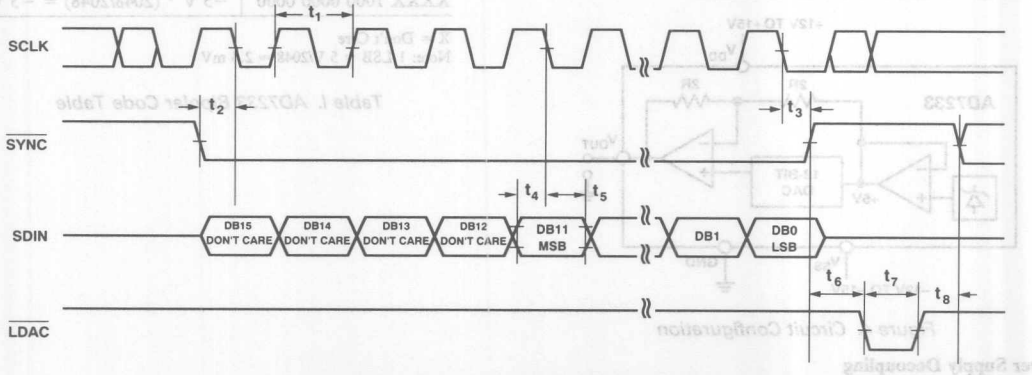
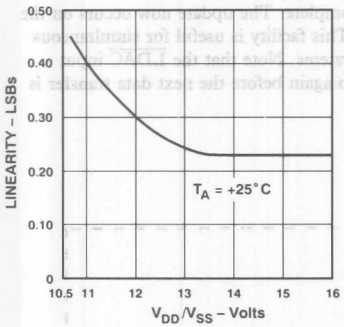
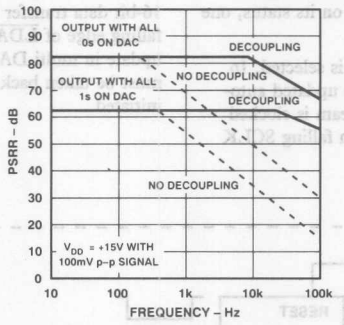


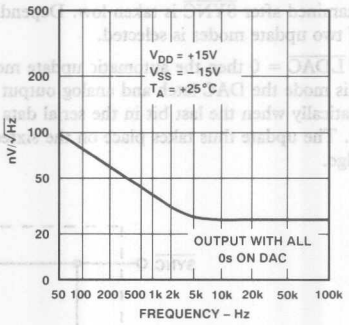
Figure 3. AD7233 Timing Diagram



Linearity vs. Power Supply Voltage



Power Supply Rejection Ratio vs. Frequency



Noise Spectral Density vs. Frequency

*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF AND 0.1μF.

APPLYING THE AD7233

Bipolar (±5 V) Configuration

The AD7233 provides an output voltage range from −5 V to +5 V without any external components. This configuration is shown in Figure 4. The data format is 2s complement. The output code table is shown in Table I. If offset binary coding is required, then this can be done by inverting the MSB in software before the data is loaded to the AD7233.

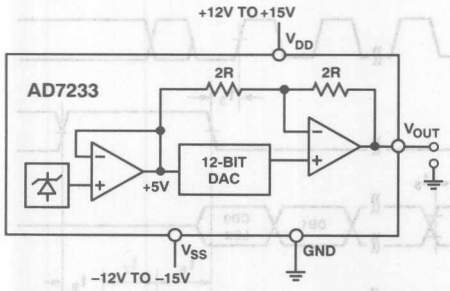


Figure 4. Circuit Configuration

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXX 0111 1111 1111	+5 V · (2047/2048)
XXXX 0000 0000 0001	+5 V · (1/2048)
XXXX 0000 0000 0000	0 V
XXXX 1111 1111 1111	−5 V · (1/2048)
XXXX 1000 0000 0001	−5 V · (2047/2048)
XXXX 1000 0000 0000	−5 V · (2048/2048) = −5 V

X = Don't Care
Note: 1 LSB = 5 V/2048 ≈ 2.4 mV

Table I. AD7233 Bipolar Code Table

Power Supply Decoupling

To achieve optimum performance when using the AD7233, the V_{DD} and V_{SS} lines should each be decoupled to GND using 0.1 μF capacitors. In very noisy environments it is recommended that 10 μF capacitors be connected in parallel with the 0.1 μF capacitors.

which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7233 requires a 16-bit data word with data valid on the falling edge of SCLK. For all of the interfaces, the DAC update may be done automatically when all the data is clocked in or it may done under control of $\overline{\text{LDAC}}$.

Figures 5 to 8 show the AD7233 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7233–ADSP-2101/ADSP-2102 Interface

Figure 5 shows a serial interface between the AD7233 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ ADSP-2102 contains two serial ports, and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ADSP-2102 is clocked into the AD7233 on the falling edge of SCLK. When the data transfer is complete $\overline{\text{TFS}}$ is taken high. In the interface shown the DAC is updated using an external timer which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, the $\overline{\text{LDAC}}$ input could be hardwired low, and in this case the automatic update mode is selected whereby the DAC update takes place automatically on the 16th falling edge of SCLK.

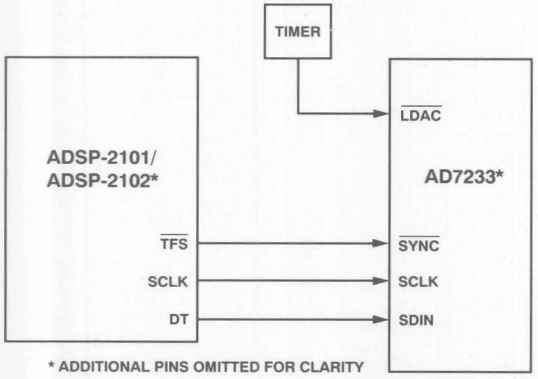


Figure 5. AD7233 to ADSP-2101/ADSP-2102 Interface

AD7233–DSP56000 Interface

A serial interface between the AD7233 and the DSP56000 is shown in Figure 6. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to the AD7233 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7233.

The $\overline{\text{LDAC}}$ input of the AD7233 is connected to GND so the update of the DAC latch takes place automatically on the 16th falling edge of SCLK. An external timer could also be used as in the previous interface if an external update is required.

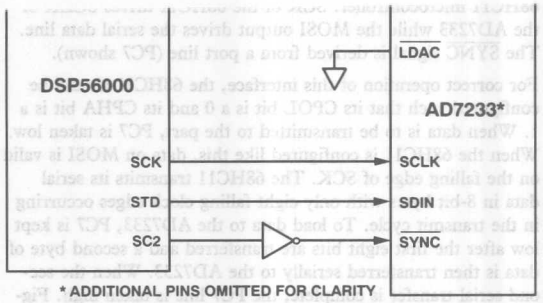


Figure 6. AD7233 to DSP56000 Interface

AD7233–87C51 Interface

A serial interface between the AD7233 and the 87C51 microcontroller is shown in Figure 7. TXD of the 87C51 drives SCLK of the AD7233 while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is derived from the port line P3.3.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7233 and the last bit to be sent is the LSB of the word to be loaded to the AD7233. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7233, P3.3 is kept low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7233. When the second serial transfer is complete, the P3.3 line is taken high.

Figure 7 shows the $\overline{\text{LDAC}}$ input of the AD7233 hardwired low. As a result, the DAC latch and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{\text{SYNC}}$ signal for the DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ input is driven from a timer, can be used.

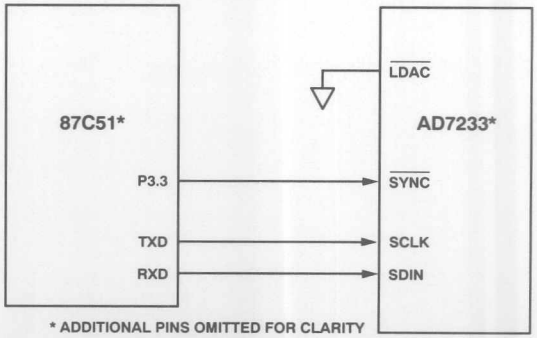


Figure 7. AD7233 to 87C51 Interface

AD7233–68HC11 Interface

Figure 8 shows a serial interface between the AD7233 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7233 while the MOSI output drives the serial data line. The $\overline{SYNC}$ signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7233, PC7 is kept low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7233. When the second serial transfer is complete, the PC7 line is taken high. Figure 8 shows the $\overline{LDAC}$ input of the AD7233 hardwired low. As a result, the DAC latch and the analog output of the DAC will be updated on the sixteenth falling edge of SCK after the respective $\overline{SYNC}$ signal has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{LDAC}$ input is driven from a timer, can be used.

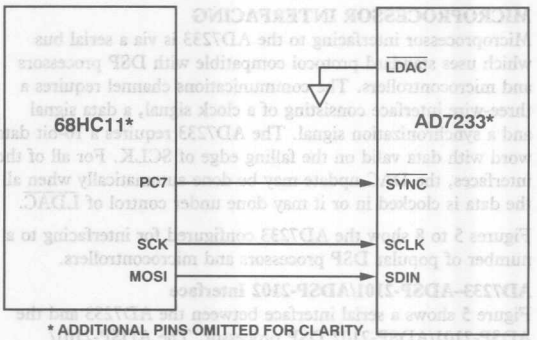


Figure 8. AD7233 to 68HC11 Interface

LC²MOS Dual 12-Bit DACPORTs

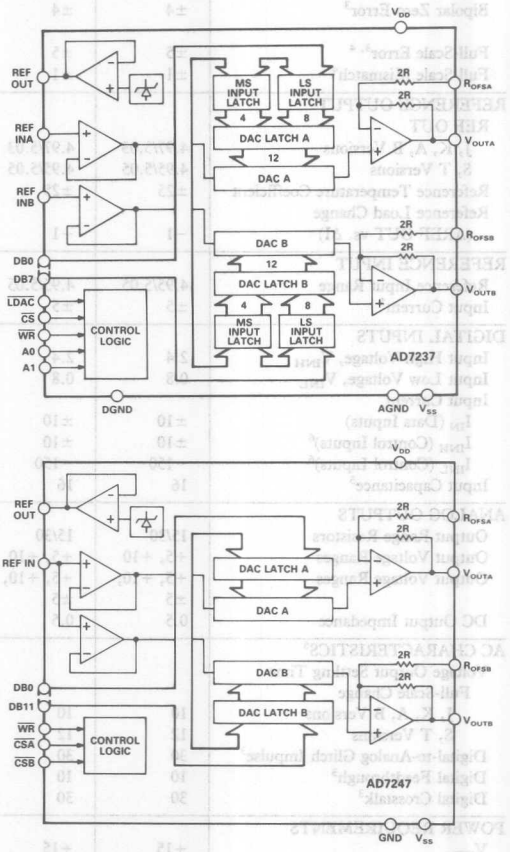
AD7237/AD7247

FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Parallel Loading Structure: AD7247
(8+4) Loading Structure: AD7237
Single or Dual Supply Operation
Low Power – 165 mW typ in Single Supply

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7237/AD7247 is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237 has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237 updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237/AD7247 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3″ wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

DACPORT is a trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD7237/AD7247 is a dual 12-bit DACPORT™ on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. Between them, the AD7237 and AD7247 offer a versatile interface arrangement to either 8-bit or 16-bit data bus structures.

AD7237/AD7247—SPECIFICATIONS (V_{DD} = +15 V[1] ±5%, V_{SS} = 0 V or −15 V[1] ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A, S[2]	K, B, T	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	LSB max	V_{SS} = 0 V or −15 V. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±4	±4	LSB max	V_{SS} = −15 V. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 4]	±5	±5	LSB max	
Full-Scale Mismatch[4]	±1	±1	LSB typ	
REFERENCE OUTPUT				
REF OUT				
J, K, A, B Versions	4.97/5.03	4.97/5.03	Vmin/Vmax	
S, T Versions	4.95/5.05	4.95/5.05	Vmin/Vmax	
Reference Temperature Coefficient	±25	±25	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–100 μA)
REFERENCE INPUT				
Reference Input Range	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current[5]	±5	±5	μA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
I_{INH} (Control Inputs)[6]	±10	±10	μA max	V_{IN} = V_{DD}
I_{INL} (Control Inputs)[6]	−150	−150	μA max	V_{IN} = 0 V
Input Capacitance[5]	16	16	pF max	
ANALOG OUTPUTS				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges	+5, +10	+5, +10	V	V_{SS} = 0 V. Pin Strappable
Output Voltage Ranges	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −15 V. Pin Strappable
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Full-Scale Change				V_{DD} = +15 V, V_{SS} = −15 V
J, K, A, B Versions	10	10	μs max	
S, T Versions	12	12	μs max	
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	
Digital Feedthrough[3]	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	nV secs typ	
POWER REQUIREMENTS				
V_{DD}	+15	+15	V nom	±5% for Specified Performance Unless Otherwise Stated
V_{SS}	−15	−15	V nom	±5% for Specified Performance Unless Otherwise Stated
I_{DD}	15	15	mA max	Output Unloaded. Typically 11 mA
I_{SS} (Dual Supplies)	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES

[1]Parts are functional at V_{DD} = +12 V ±10% and V_{SS} = 0 V or −12 V ±10%. See typical performance graphs.

[2]Temperature ranges are as follows: J, K Versions, −40°C to +85°C; A, B Versions, −40°C to +85°C; S, T Versions, −55°C to +125°C.

[3]See Terminology.

[4]Measured with respect to REF IN and includes unipolar/bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

[6]Control inputs are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$ for the AD7237 and $\overline{CSA}$, $\overline{CSB}$ and $\overline{WR}$ for the AD7247.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +15 V ±5%; V_{SS} = 0 V or −15 V ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247])

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	130	150	ns min	$\overline{WR}$ Pulse Width
t_4	128	150	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5[3]	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[4]	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[4]	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[4]	100	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 5 and 7.
[3]If 0 ns<t_2<10 ns, add t_2 to t_5. If t_2≥10 ns, add 10 ns to t_5.
[4]AD7237 only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247) . . . . . −0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237) . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND (AD7237) . . . . . −0.3 V , V_{DD} +0.3 V
V_{OUTA}[1], V_{OUTB}[1] to AGND (GND)
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
REF OUT to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND) . . . . . −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]Short-circuit current is typically 80mA. The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237JN	−40°C to +85°C	±1 max	N-24
AD7237KN	−40°C to +85°C	±1/2 max	N-24
AD7237JR	−40°C to +85°C	±1 max	R-24
AD7237KR	−40°C to +85°C	±1/2 max	R-24
AD7237AQ	−40°C to +85°C	±1 max	Q-24
AD7237BQ	−40°C to +85°C	±1/2 max	Q-24
AD7237SQ	−55°C to +125°C	±1 max	Q-24
AD7237TQ	−55°C to +125°C	±1/2 max	Q-24
AD7247JN	−40°C to +85°C	±1 max	N-24
AD7247KN	−40°C to +85°C	±1/2 max	N-24
AD7247JR	−40°C to +85°C	±1 max	R-24
AD7247KR	−40°C to +85°C	±1/2 max	R-24
AD7247AQ	−40°C to +85°C	±1 max	Q-24
AD7247BQ	−40°C to +85°C	±1/2 max	Q-24
AD7247SQ	−55°C to +125°C	±1 max	Q-24
AD7247TQ	−55°C to +125°C	±1/2 max	Q-24

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC). For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



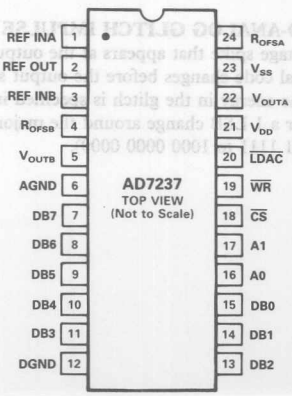
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8–10	DB6–DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply, +15 V.
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply, −15 V.
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7247 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to + 10 V and ± 5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9–DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply, +15 V.
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply, −15 V.
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247 is 5 V.

AD7237 PIN CONFIGURATIONS

DIP and SOIC



AD7247 PIN CONFIGURATIONS

DIP and SOIC



TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifiers of the AD7237/AD7247 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1. This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

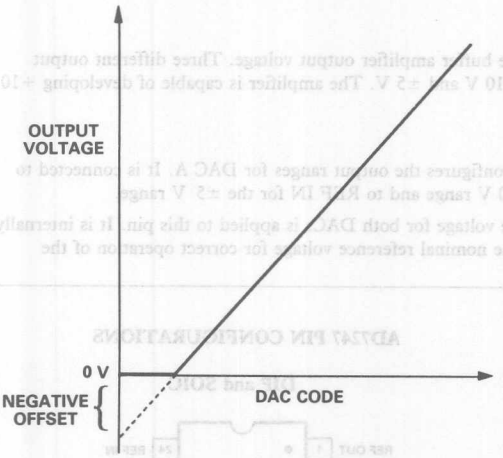


Figure 1. Effect of Negative Offset (Single Supply)

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7237/AD7247 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset, i.e., linearity is measured between Codes 3 and 4095.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the measured output voltage from V_{OUTA} or V_{OUTB} with all zeros loaded into the DAC latches when the DACs are configured for unipolar output. It is a combination of the offset errors of the DAC and output amplifier.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the voltage measured at V_{OUTA} or V_{OUTB} when the DAC is connected in the bipolar mode and loaded with code 2048. It is due to a combination of offset errors in the DAC, amplifier offset and mismatch in the application resistors around the amplifier.

FULL-SCALE ERROR

Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse injected for the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

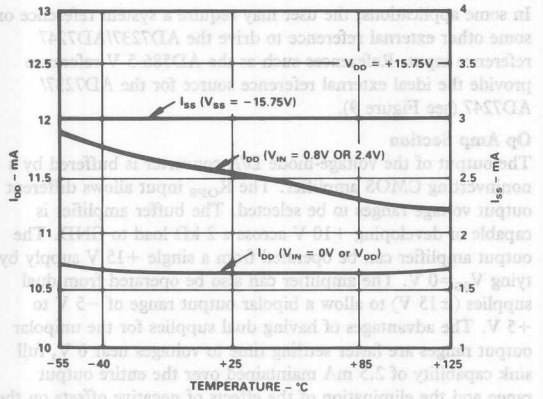
For the AD7237 it is measured with $\overline{LDAC}$ held high. For the AD7247 it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

DIGITAL CROSSTALK

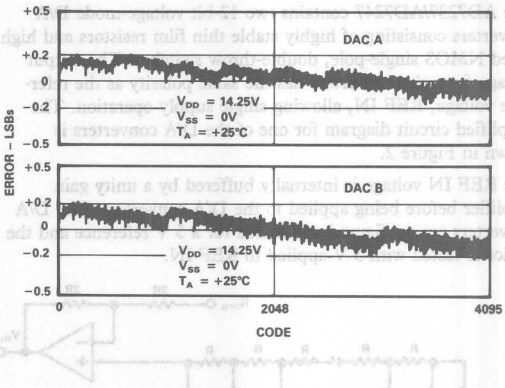
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code to the DAC latch of the other converter. It is specified in nV secs.

DIGITAL-TO-ANALOG GLITCH IMPULSE

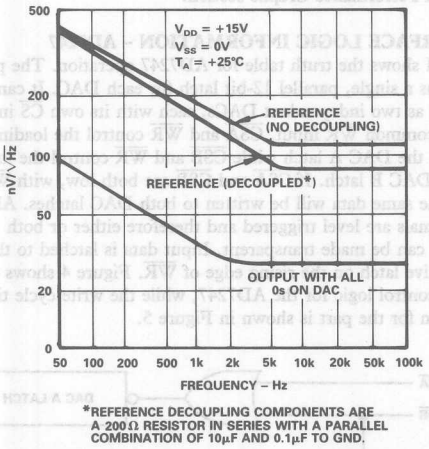
This is the voltage spike that appears at the output of the DAC when the digital code changes before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).



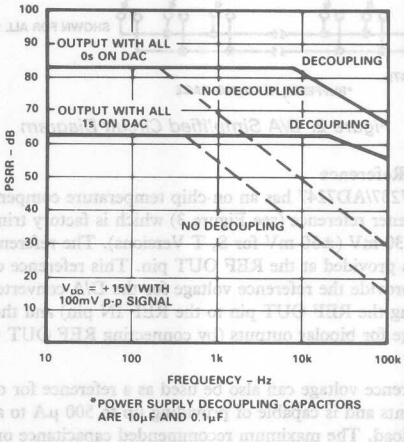
Power Supply Current vs.Temperature



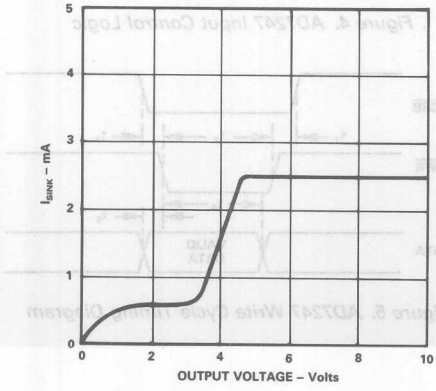
DAC-to-DAC Linearity Matching



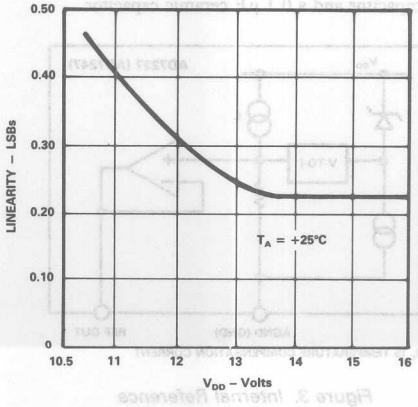
Noise Spectral Density vs. Frequency



Power Supply Rejection Ratio vs. Frequency



Single Supply Sink Current vs. Output Voltage



Linearity vs. Power Supply Voltage

CIRCUIT INFORMATION

D/A Section

The AD7237/AD7247 contains two 12-bit voltage-mode D/A converters consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The output voltage from the converters has the same polarity as the reference voltage, REF IN, allowing single supply operation. The simplified circuit diagram for one of the D/A converters is shown in Figure 2.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converters. The D/A converters are configured and scaled for a 5 V reference and the device is tested with 5 V applied to REF IN.

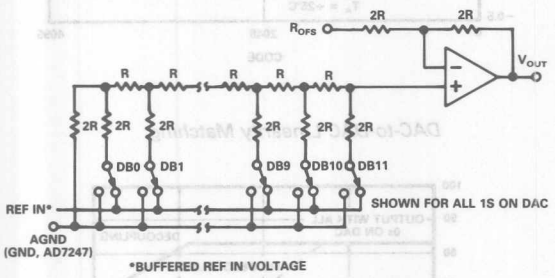


Figure 2. D/A Simplified Circuit Diagram

Internal Reference

The AD7237/AD7247 has an on-chip temperature compensated buried Zener reference (see Figure 3) which is factory trimmed to 5 V ±30 mV (±50 mV for S, T Versions). The reference voltage is provided at the REF OUT pin. This reference can be used to provide the reference voltage for the D/A converter (by connecting the REF OUT pin to the REF IN pin) and the offset voltage for bipolar outputs (by connecting REF OUT to R_{OFS}).

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND (GND) with a 200 Ω resistor in series with parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

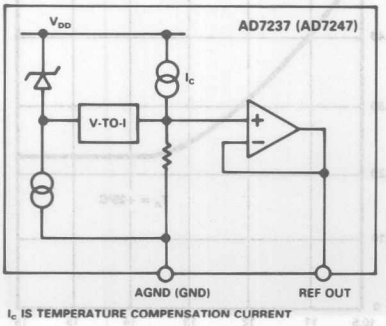


Figure 3. Internal Reference

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7237/AD7247 reference input. References such as the AD586 5 V reference provide the ideal external reference source for the AD7237/AD7247 (see Figure 9).

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows different output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to GND. The output amplifier can be operated from a single +15 V supply by tying V_{SS}=0 V. The amplifier can also be operated from dual supplies (±15 V) to allow a bipolar output range of −5 V to +5 V. The advantages of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0 V, full sink capability of 2.5 mA maintained over the entire output range and the elimination of the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the single supply output sink capability of the amplifier is shown in the Typical Performance Graphs section.

INTERFACE LOGIC INFORMATION – AD7247

Table I shows the truth table for AD7247 operation. The part contains a single, parallel 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. If $\overline{CSA}$ and $\overline{CSB}$ are both low, with $\overline{WR}$ low, the same data will be written to both DAC latches. All control signals are level triggered and therefore either or both latches can be made transparent. Input data is latched to the respective latch on the rising edge of $\overline{WR}$. Figure 4 shows the input control logic for the AD7247, while the write cycle timing diagram for the part is shown in Figure 5.

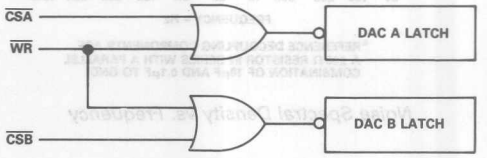


Figure 4. AD7247 Input Control Logic

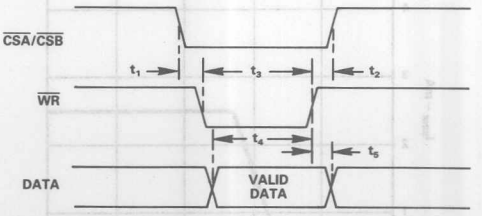


Figure 5. AD7247 Write Cycle Timing Diagram

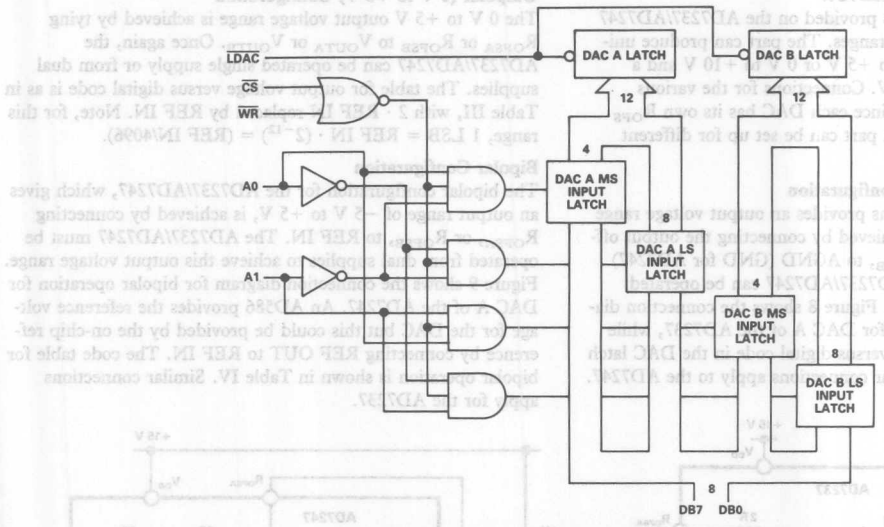


Figure 6. AD7237 Input Control Logic

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X = Don't Care

Table I. AD7247 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

Table II. AD7237 Truth Table

INTERFACE LOGIC INFORMATION – AD7237

The input loading structure on the AD7237 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC – an input latch and a DAC latch. Each input latch is further subdivided into a least significant 8-bit latch and a most significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7237 is shown in Figure 6, while the write cycle timing diagram is shown in Figure 7.

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The selection of the input latches is shown in the truth table for AD7237 operation in Table II.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. Both DAC latches, and hence both analog outputs, are updated at the same time. The $\overline{LDAC}$ signal is level triggered and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7237s.

However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

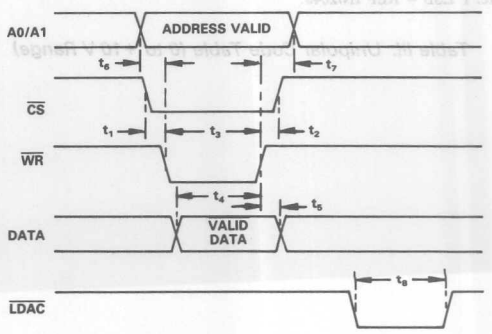


Figure 7. AD7237 Write Cycle Timing Diagram

APPLYING THE AD7237/AD7247

The internal scaling resistors provided on the AD7237/AD7247 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input the two DACs on each part can be set up for different output ranges.

Unipolar (0 V to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor, R_{OFSA}, or R_{OFSB}, to AGND (GND for AD7247). In this configuration, the AD7237/AD7247 can be operated from single or dual supplies. Figure 8 shows the connection diagram for unipolar operation for DAC A of the AD7237, while the table for output voltage versus digital code in the DAC latch is shown in Table III. Similar connections apply to the AD7247.

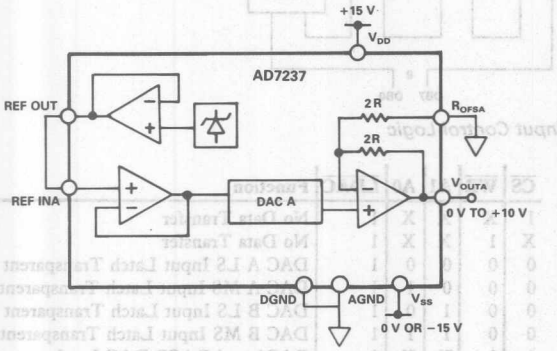


Figure 8. Unipolar (0 to +10 V) Configuration

DAC Latch Contents

MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+2 · REF IN · (4095/4096)
1000 0000 0001	+2 · REF IN · (2049/4096)
1000 0000 0000	+2 · REF IN · (2048/4096) = +REF IN
0111 1111 1111	+2 · REF IN · (2047/4096)
0000 0000 0001	+2 · REF IN · (1/4096)
0000 0000 0000	0 V

Note: 1 LSB = REF IN/2048.

Table III. Unipolar Code Table (0 to +10 V Range)

Unipolar (0 V to +5 V) Configuration

The 0 V to +5 V output voltage range is achieved by tying R_{OFSA} or R_{OFSB} to V_{OUTA} or V_{OUTB}. Once again, the AD7237/AD7247 can be operated single supply or from dual supplies. The table for output voltage versus digital code is as in Table III, with 2 · REF IN replaced by REF IN. Note, for this range, 1 LSB = REF IN · (2^{-12}) = (REF IN/4096).

Bipolar Configuration

The bipolar configuration for the AD7237/AD7247, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFSA}, or R_{OFSB}, to REF IN. The AD7237/AD7247 must be operated from dual supplies to achieve this output voltage range. Figure 9 shows the connection diagram for bipolar operation for DAC A of the AD7247. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REF OUT to REF IN. The code table for bipolar operation is shown in Table IV. Similar connections apply for the AD7237.

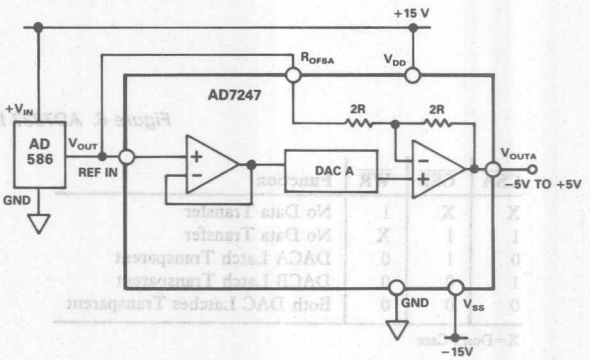


Figure 9. Bipolar Configuration

DAC Latch Contents

MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+REF IN · (2047/2048)
1000 0000 0001	+REF IN · (1/2048)
1000 0000 0000	0 V
0111 1111 1111	−REF IN · (1/2048)
0000 0000 0001	−REF IN · (2047/2048)
0000 0000 0000	−REF IN · (2048/2048) = −REF IN

Note: 1 LSB = REF IN/2048.

Table IV. Bipolar Code Table

MICROPROCESSOR INTERFACING – AD7247

Figures 10 to 12 show interfaces between the AD7247 and the ADSP-2101 DSP processor and the 8086 and 68000 16-bit microprocessors. In all three interfaces, the AD7247 is memory-mapped with a separate memory address for each DAC.

AD7247 – ADSP-2101 Interface

Figure 10 shows an interface between the AD7247 and the ADSP-2101. The 12-bit word is written to the selected DAC latch of the AD7247 in a single instruction, and the analog output responds immediately. Depending on the clock frequency of the ADSP-2101, either one or two wait states will have to be programmed into the data memory wait state control register of the ADSP-2101.

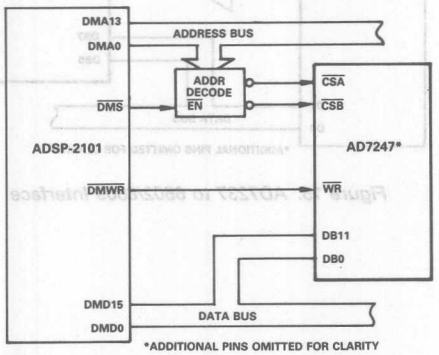


Figure 10. AD7247 to ADSP-2101 Interface

AD7247 – 8086 Interface

Figure 11 shows an interface between the AD7247 and the 8086 microprocessor. The 12-bit word is written to the selected DAC latch of the AD7247 in a single MOV instruction, and the analog output responds immediately.

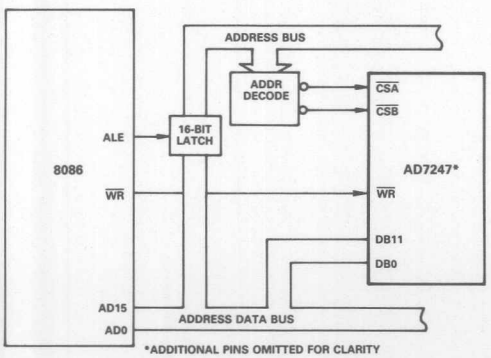


Figure 11. AD7247 to 8086 Interface

AD7247 – MC68000 Interface

Interfacing between the AD7247 and the MC68000 microprocessor is achieved using the circuit of Figure 12. Once again, the 12-bit word is written to the selected DAC latch of the AD7247 in a single MOVE instruction. $\overline{CSA}$ and $\overline{CSB}$ have to be AND-gated to provide a $\overline{DTACK}$ signal for the MC68000 when either DAC latch is selected.

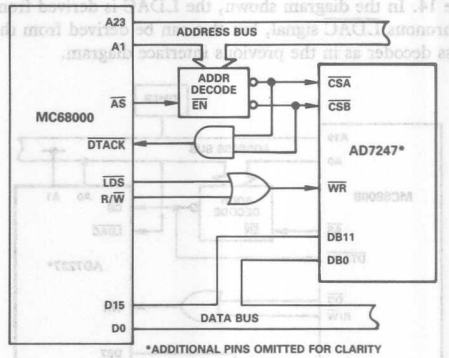


Figure 12. AD7247 to MC68000 Interface

MICROPROCESSOR INTERFACING – AD7237

Figures 13 to 15 show the AD7237 configured for interfacing to microprocessors with 8-bit databus systems. In all cases, data is right-justified, and the AD7237 is memory-mapped with the two lowest address lines of the microprocessor address bus driving the A0 and A1 inputs of the converter.

AD7237 – 8085A/8088 Interface

Figure 13 shows the connection diagram for interfacing the AD7237 to both the 8085A and the 8088. This scheme is also suited to the Z80 microprocessor, but the Z80 address/databus does not have to be demultiplexed. The AD7237 requires five separate memory addresses, one for the each MS latch and one for each LS latch and one for the common $\overline{LDAC}$ input. Data is written to the respective input latch in two write operations.

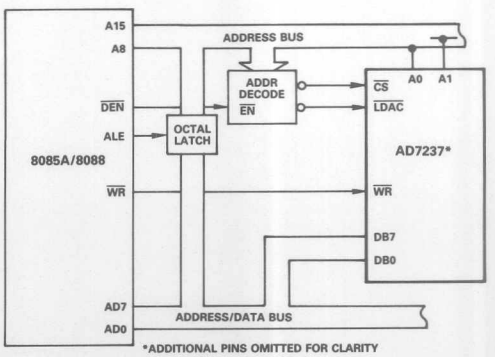


Figure 13. AD7237 to 8085A/8088 Interface

latches and updates both analog outputs. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7237s for simultaneous updating of a number of voltage channels.

AD7237 – 68008 Interface

An interface between the AD7237 and the 68008 is shown in Figure 14. In the diagram shown, the $\overline{LDAC}$ is derived from an asynchronous $\overline{LDAC}$ signal, but this can be derived from the address decoder as in the previous interface diagram.

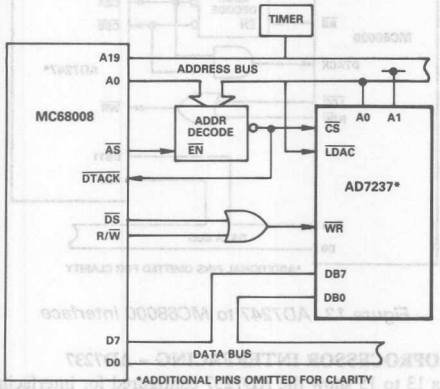


Figure 14. AD7237 to 68008 Interface

AD7237 is as outlined for the 8085A/8088 interface. For the 6502 microprocessor, the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

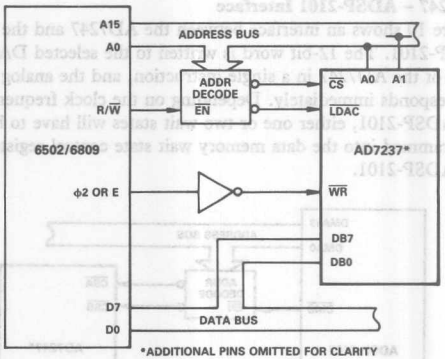


Figure 15. AD7237 to 6502/6809 Interface

LC²MOS Dual, Complete, 12-Bit/14-Bit Serial DACs

AD7242/AD7244

2

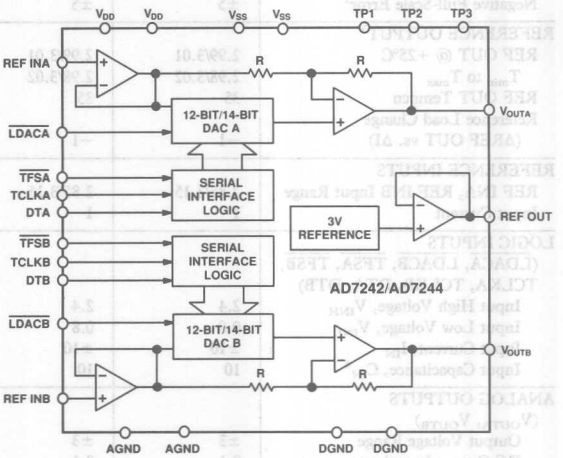
FEATURES

Two 12-Bit/14-Bit DACs with Output Amplifiers
- **AD7242: 12-Bit Resolution**
- **AD7244: 14-Bit Resolution**

On-Chip Voltage Reference
Fast Settling Time
- **AD7242: 3 μs to ±1/2 LSB**
- **AD7244: 4 μs to ±1/2 LSB**

High Speed Serial Interface
Operates from ±5 V Supplies
Low Power – 130 mW typ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7242/AD7244 is a fast, complete, dual 12-bit/14-bit voltage output D/A converter. It consists of a 12-bit/14-bit DAC, 3 V buried Zener reference, DAC output amplifiers and high speed serial interface logic.

Interfacing to both DACs is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. Asynchronous control of DAC updating for both DACs is made possible with a separate $\overline{\text{LDAC}}$ input for each DAC.

The AD7242/AD7244 operates from ±5 V power supplies, providing an analog output range of ±3 V. A REF OUT/REF IN function allows the DACs to be driven from the on-chip 3 V reference or from an external reference source.

The AD7242/AD7244 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3 inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic small outline (SOIC) package. The AD7242 and AD7244 are available in the same pinout to allow easy upgrade from 12-bit to 14-bit performance.

PRODUCT HIGHLIGHTS

1. Complete, Dual 12-Bit/14-Bit DACs
   The AD7242/AD7244 provides the complete function for generating voltages to 12-bit/14-bit resolution. The part features an on-chip reference, output buffer amplifiers and two 12-bit/14-bit D/A converters.
2. High Speed Serial Interface
   The AD7242/AD7244 provides a high speed, easy-to-use, serial interface allowing direct interfacing to DSP processors and microcontrollers. A separate serial port is provided for each DAC.
3. Small Package Size
   The AD7242/AD7244 is available in a 24-pin DIP and a 28-pin SOIC package offering considerable space saving over comparable solutions.

AD7242/AD7244—SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, REF INA = REF INB = +3 V. V_{OUTA}, V_{OUTB} load to AGND: R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7242 J, A Versions[1]	AD7242 K, B Versions[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	LSB max	
Positive Full-Scale Error[2]	±5	±5	LSB max	
Negative Full-Scale Error[2]	±5	±5	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS ($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	μs max	Typically 2 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	27	27	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	195	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; A, B Versions: −40°C to +85°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

AD7242 ORDERING GUIDE

Model	Temperature Range	Integral Nonlinearity	Package Option*
AD7242JN	0°C to +70°C	±1 LSB max	N-24
AD7242KN	0°C to +70°C	±1/2 LSB max	N-24
AD7242JR	0°C to +70°C	±1 LSB max	R-28
AD7242KR	0°C to +70°C	±1/2 LSB max	R-28
AD7242AQ	−40°C to +85°C	±1 LSB max	Q-24
AD7242BQ	−40°C to +85°C	±1/2 LSB max	Q-24

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

Parameter	AD7244 J/A Versions[1]	AD7244 S Version[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	LSB max	
Positive Full-Scale Error[2]	±10	±10	LSB max	
Negative Full-Scale Error[2]	±10	±10	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS ($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	Typically 2.5 μs
Negative Full-Scale Change	4	4	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	27	28	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	13	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	205	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J Version: 0°C to +70°C; A Version: −40°C to +85°C; S Version: −55°C to +125°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

AD7244 ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Option[2]
AD7244JN	0°C to +70°C	±2 LSB max	N-24
AD7244JR	0°C to +70°C	±2 LSB max	R-28
AD7244AQ	−40°C to +85°C	±2 LSB max	Q-24
AD7244SQ[3]	−55°C to +125°C	±2 LSB max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_2	75	100	ns min	TCLK Falling Edge to $\overline{TFS}$
t_3[3]	150	200	ns min	TCLK Cycle Time
t_4	30	40	ns min	Data Valid to TCLK Setup Time
t_5	75	100	ns min	Data Valid to TCLK Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 6.
[3]TCLK Mark/Space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
REF INA, REF INB to AGND . . . . −0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
J, K Versions . . . . . 0°C to +70°C
A, B Versions . . . . . −40°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 550 mW
Derates above +75°C by . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

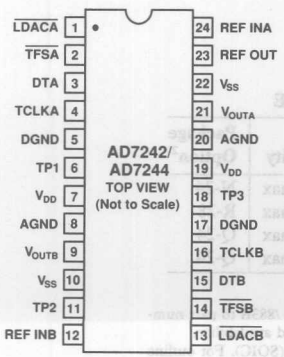
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

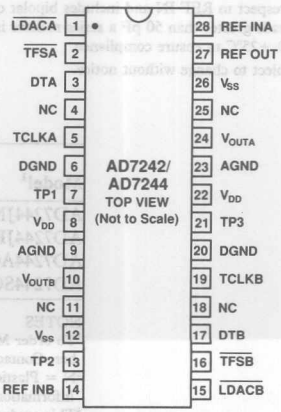


PIN CONFIGURATIONS

DIP



SOIC



NC = NO CONNECT

DIP Pin No.	Mnemonic	Description
1	$\overline{\text{LDACA}}$	Load DAC, Logic Input. A new word is transferred into DAC Latch A from input Latch A on the falling edge of this signal. If $\overline{\text{LDACA}}$ is hard-wired low, data is transferred from input Latch A to DAC Latch A on the sixteenth falling edge of TCLKA after $\overline{\text{TFSA}}$ goes low.
2	$\overline{\text{TFSA}}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for DACA data with serial data expected after the falling edge of this signal.
3	DTA	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{\text{TFSA}}$ and TCLKA to transfer serial data to input Latch A.
4	TCLKA	Transmit Clock, Logic Input. Serial data bits for DACA are latched on the falling edge of TCLKA when $\overline{\text{TFSA}}$ is low.
5	DGND	Digital Ground. Both DGND pins for the device must be tied together at the device.
6	TP1	Test Pin 1. Used when testing the device. Do not connect anything to this pin.
7	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins for the device must be tied together at the device.
8	AGND	Analog Ground. Both AGND pins for the device must be tied together at the device.
9	V_{OUTB}	Analog Output Voltage from DACB. This output comes from a buffer amplifier. The range is bipolar, ±3 V with REF INB = +3 V.
10	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins for the device must be tied together at the device.
11	TP2	Test Pin 2. Used when testing the device. Do not connect anything to this pin.
12	REF INB	DACB Voltage Reference Input. The voltage reference for DACB is applied to this pin. It is internally buffered before being applied to DACB. The nominal reference voltage for correct operation of the AD7242/AD7244 is 3 V.
13	$\overline{\text{LDACB}}$	Load DAC, Logic Input. A new word is transferred into DAC Latch B from input Latch B on the falling edge of this signal. If $\overline{\text{LDACB}}$ is hard-wired low, data is transferred from input Latch B to DAC Latch B on the sixteenth falling edge of TCLKB after $\overline{\text{TFSB}}$ goes low.
14	$\overline{\text{TFSB}}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for DACB data with serial data expected after the falling edge of this signal.
15	DTB	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{\text{TFSB}}$ and TCLKB to transfer serial data to input Latch B.
16	TCLKB	Transmit Clock, Logic Input. Serial data bits for DACB are latched on the falling edge of TCLKB when $\overline{\text{TFSB}}$ is low.
17	DGND	Digital Ground. Both DGND pins for the device must be tied together at the device.
18	TP3	Test Pin 3. Used when testing the device. Do not connect anything to this pin.
19	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins for the device must be tied together at the device.
20	AGND	Analog Ground. Both AGND pins for the device must be tied together at the device.
21	V_{OUTA}	Analog Output Voltage from DACA. This output comes from a buffer amplifier. The range is bipolar, ±3 V with REF INA = +3 V.
22	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins for the device must be tied together at the device.
23	REF OUT	Voltage Reference Output. To operate the DACs with this internal reference, REF OUT should be connected to both REF INA and REF INB. The external load capability of the reference is 500 μA.
24	REF INA	DACA Voltage Reference Input. The voltage reference for DACA is applied to this pin. It is internally buffered before being applied to DACA. The nominal reference voltage for correct operation of the AD7242/AD7244 is 3 V.

CIRCUIT DESCRIPTION

The AD7242/AD7244 contains two 12-bit/14-bit D/A converters, each with an output buffer amplifier. The part also contains a reference input buffer amplifier for each DAC and an on-chip 3 V reference.

D/A Section

The AD7242/AD7244 contains two 12-bit/14-bit voltage-mode D/A converters, each consisting of highly stable thin film resistors and high speed single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 1. The three MSBs of the data word are decoded to drive the seven switches A–G. On the AD7242, the 9 LSBs switch a 9-bit R-2R ladder structure while on the AD7244, the 11 LSBs switch an 11-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converters and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3 V reference, and the device is tested with 3 V applied to REF IN. Operating the AD7242/AD7244 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

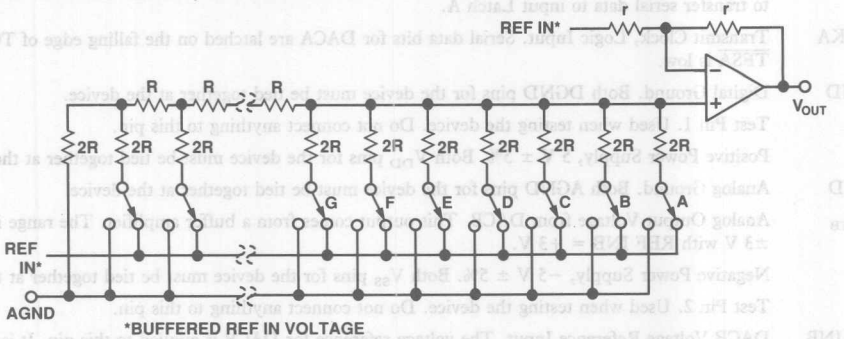


Figure 1. DAC Ladder Structure

Internal Reference

The on-chip reference is a temperature-compensated buried Zener reference which is factory trimmed for 3 V ±10 mV. The reference can be used to provide both the reference voltage for the two D/A converters and the bipolar biasing circuitry. This is achieved by connecting REF OUT to REF INA and REF INB.

The reference voltage can also be used for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on the reference output pin for normal operation is 50 pF. If the reference output is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor should be placed in series with the capacitive load. Decoupling the REF OUT pin with a series 200 Ω resistor and a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor as in Figure 2 reduces the noise spectral density of the reference (see Figure 4). Using this decoupling scheme to generate the reference voltage for REF INA and REF INB gives a channel-to-channel isolation number of 110 dB (connecting REF OUT directly to REF INA and REF INB gives 80 dB). The channel-to-channel isolation is 110 dB using an external reference.

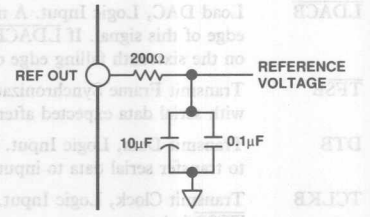


Figure 2. Circuit Connection for REF OUT with an External Capacitive Load of Greater Than 50 pF

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7242/AD7244 reference inputs. Figure 3 shows how the AD586 reference can be conditioned to provide the 3 V reference required by the AD7242/AD7244 reference inputs.

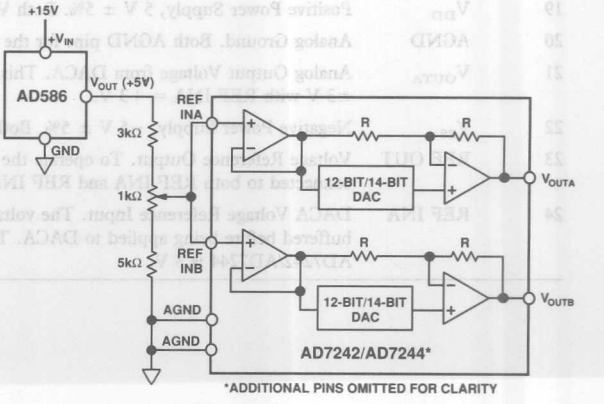


Figure 3. AD586 Driving AD7242/AD7244 Reference Inputs

Output Amplifier

The outputs from each of the voltage-mode DACs are buffered by a noninverting amplifier. The buffer amplifier is capable of developing ±3 V across a 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the respective $\overline{LDAC}$ input. The output voltage settling time, to within 1/2 LSB of its final value, is typically less than 2 μs for the AD7242 and 2.5 μs for the AD7244.

The small signal (200 mV p–p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 30 nV/√Hz at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. Figure 4 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for the on-chip reference (including and excluding the decoupling components).

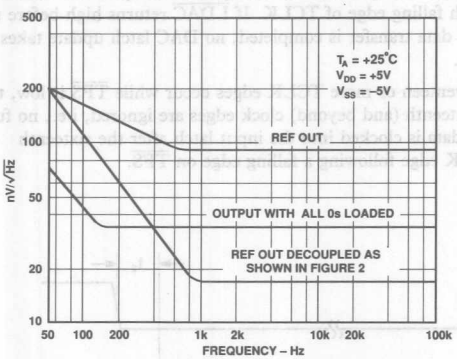


Figure 4. Noise Spectral Density vs. Frequency

TRANSFER FUNCTION

The basic circuit configuration for the AD7242/AD7244 is shown in Figure 5. Table I and Table II show the ideal input code to output voltage relationship for the AD7242 and AD7244 respectively. Input coding for the AD7242/AD7244 is 2s complement.

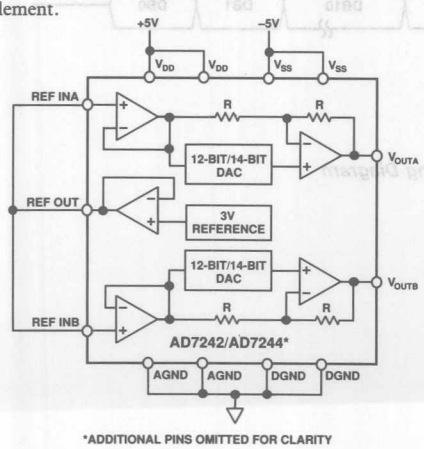


Figure 5. Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
01 11 1111 1111	+2.998535 V
01 11 1111 1110	+2.99707 V
00 00 0000 0001	+0.001465 V
00 00 0000 0000	0 V
11 11 1111 1111	−0.001465 V
10 00 0000 0001	−2.998535 V
10 00 0000 0000	−3 V

*Assuming REF IN = +3 V.

Table I. AD7242 Ideal Input/Output Code Table Code

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
01 1111 1111 1111	+2.999634 V
01 1111 1111 1110	+2.99268 V
00 0000 0000 0001	+0.000366 V
00 0000 0000 0000	0 V
11 1111 1111 1111	−0.000366 V
10 0000 0000 0001	−2.999634 V
10 0000 0000 0000	−3 V

*Assuming REF IN = +3 V.

Table II. AD7244 Ideal Input/Output Code Table Code

For the AD7242, the output voltage can be expressed in terms of the input code, N, using the following relationship:

$$V_{OUT} = \frac{2 \cdot N \cdot REF\ IN}{4096}$$

where $-2048 \le N \le +2047$

For the AD7244, the output voltage can be expressed in terms of the input code, N, using the following relationship:

$$V_{OUT} = \frac{2 \cdot N \cdot REF\ IN}{16384}$$

where $-8192 \le N \le +8191$

TIMING AND CONTROL

Communication with the AD7242/AD7244 is via six serial logic inputs. These consist of separate serial clocks, word framing and data lines for each DAC. DAC updating is controlled by two digital inputs, $\overline{LDACA}$ for updating V_{OUTA} and $\overline{LDACB}$ for updating V_{OUTB}. These inputs can be asserted independently of the microprocessor by an external timer when precise updating intervals are required. Alternatively, the $\overline{LDACA}$ and $\overline{LDACB}$ inputs can be driven from a decoded address bus allowing the microprocessor control over DAC updating as well as data communication to the AD7242/AD7244 input latches.

The AD7242/AD7244 contains two latches per DAC, an input latch and a DAC latch. Data must be loaded to the input latch under the control of TCLKA, $\overline{TFSA}$ and DTA for input Latch A and TCLKB, $\overline{TFSB}$ and DTB for input Latch B. Data is then transferred from input Latch A to DAC Latch A under the control of the $\overline{LDACA}$ signal while $\overline{LDACB}$ controls the loading of DAC Latch B from input Latch B. Only the data held in the DAC latches determines the analog outputs of the AD7242/AD7244.

Data is loaded to the input latches under control of the respective TCLK, $\overline{TFS}$ and DT signals. The AD7242/AD7244 expects a 16-bit stream of serial data on its DT inputs. Data must be valid on the falling edge of TCLK. The $\overline{TFS}$ input provides the frame synchronization signal which tells the AD7242/AD7244 that valid serial data will be available on the DT input for the next 16 falling edges of TCLK. Figure 6 shows the timing diagram for operation of either of the two serial input ports on the part.

Although 16 bits of data are clocked into the input latch, only 12 bits are transferred into the DAC latch for the AD7242 and 14-bits are transferred for the AD7244. Therefore, 4 bits in the AD7242 data stream and 2 bits in the AD7244 data stream are don't cares since their value does not affect the DAC latch data. The bit positions are the don't cares followed by the DAC data starting with the MSB (see Figure 6).

The respective $\overline{LDAC}$ signals control the transfer of data to the respective DAC latches. Normally, data is loaded to the DAC latch on the falling edge of $\overline{LDAC}$. However, if $\overline{LDAC}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of TCLK. If $\overline{LDAC}$ goes low during the loading of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{LDAC}$. If $\overline{LDAC}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of TCLK. If $\overline{LDAC}$ returns high before the serial data transfer is completed, no DAC latch update takes place.

If seventeen or more TCLK edges occur while $\overline{TFS}$ is low, the seventeenth (and beyond) clock edges are ignored, i.e., no further data is clocked into the input latch after the sixteenth TCLK edge following a falling edge on $\overline{TFS}$.

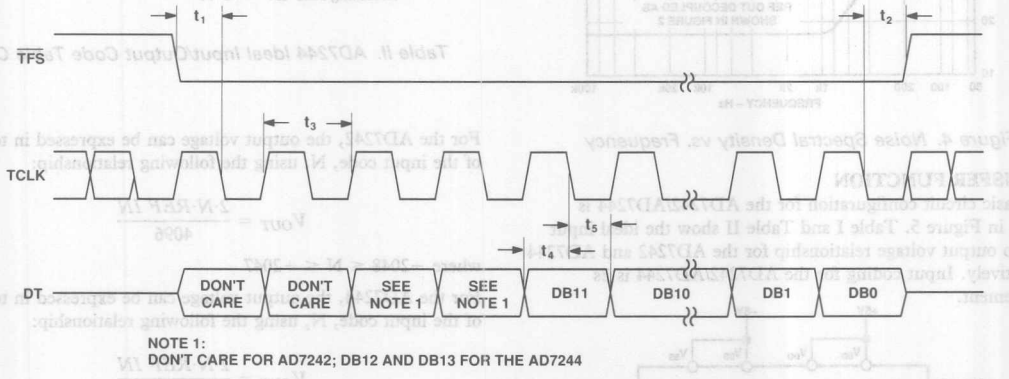


Figure 6. AD7242/AD7244 Timing Diagram

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7242/AD7244 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communication interface consists of a separate transmit section for each of the DACs. Each section has a clock signal, a data signal and a frame or strobe pulse.

Figures 7 through 11 show the AD7242/AD7244 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7242/AD7244 to ADSP-2101/ADSP-2102 Interface

Figure 7 shows a serial interface between the AD7242/AD7244 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ADSP-2102 has two serial ports and in the interface shown both serial ports are used, one for each DAC. Both serial ports do not have to be used; in the case where only one serial port is used, an extra line (DACA/$\overline{\text{DACB}}$ as shown in the other serial interfaces) would have to decode the one $\overline{\text{TFS}}$ line to provide $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ lines for the AD7242/AD7244.

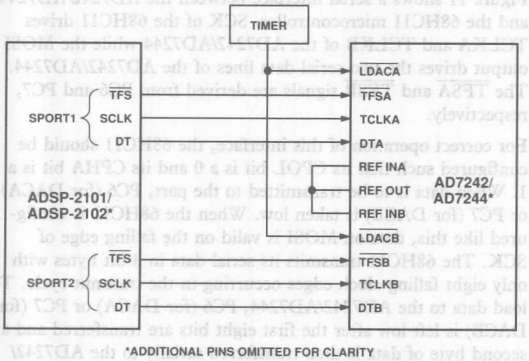


Figure 7. AD7242/AD7244 to ADSP-2101/ADSP-2102 Interface

The three serial lines of the first serial port, SPORT1, of the ADSP-2101/ADSP-2102 connect directly to the three serial input lines of DACA of the AD7242/AD7244. The three serial lines of SPORT2 connect directly to the three serial lines on the DACB serial input port. Data from the ADSP-2101/ADSP-2102 is valid on the falling edge of SCLK. A common LDAC signal is used to drive the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs. This is shown to be generated from a timer or clock recovery circuit but another control or address line of the ADSP-2101/ADSP-2102 could be used to drive these inputs. Alternatively, the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244 could be hardwired low and in this case the update of the DAC latches and analog outputs takes place on the 16th falling edge of SCLK (after the respective $\overline{\text{TFS}}$ signal goes low).

AD7242/AD7244 to DSP56000 Interface

A serial interface between the AD7242/AD7244 and the DSP56000 is shown in Figure 8. The DSP56000 is configured for normal mode, asynchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to both the TCLKA and TCLKB inputs of the AD7242/AD7244. Data from the DSP56000 is valid on the falling edge of SCK. The serial data line, STD, is drives the DTA and DTB serial input data lines of the AD7242/AD7244.

The SC2 output provides the framing pulse for valid data. This is an active high output and is gated with a DACA/$\overline{\text{DACB}}$ control line before being applied to the $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ inputs of the AD7242/AD7244. The DACA/$\overline{\text{DACB}}$ line determines which DAC serial data is to be transferred to, i.e., which $\overline{\text{TFS}}$ line is active when SC2 is active.

As in the previous interface, a common $\overline{\text{LDAC}}$ input is shown driving the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244. Once again, these $\overline{\text{LDAC}}$ inputs could be hardwired low, in which case V_{OUTA} or V_{OUTB} will be updated on the sixteenth falling edge of SCK after the $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ input goes low.

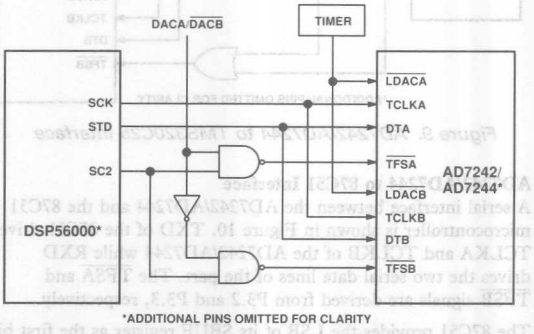


Figure 8. AD7242/AD7244 to DSP56000 Interface

AD7242/AD7244 to TMS320C25 Interface

Figure 9 shows a serial interface between the AD7242/AD7244 and the TMS320C25 DSP processor. In this interface, the CLKX and FSX signals of the TMS320C25 are generated from the clock/timer circuitry. The FSX pin of the TMS320C25 must be configured as an input. CLKX is used to provide both the TCLKA and TCLKB inputs of the AD7242/AD7244. DX of the TMS320C25 is also routed to the serial data line of each input port of the AD7242/AD7244.

Data from the TMS32020 is valid on the falling edge of CLKX after FSX goes low. This FSX signal is gated with the DACA/$\overline{\text{DACB}}$ control line to determine whether $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ goes low when FSX goes low.

The clock/timer circuitry also generates the $\overline{\text{LDAC}}$ signal for the AD7242/AD7244 to synchronize the update of the outputs with the serial transmission. As in the previous interface diagrams, a common $\overline{\text{LDAC}}$ input is shown driving the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244. Once again, these $\overline{\text{LDAC}}$ inputs could be hardwired low, in which case V_{OUTA} or V_{OUTB} will be updated on the sixteenth falling edge of CLKX after the $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ input goes low.

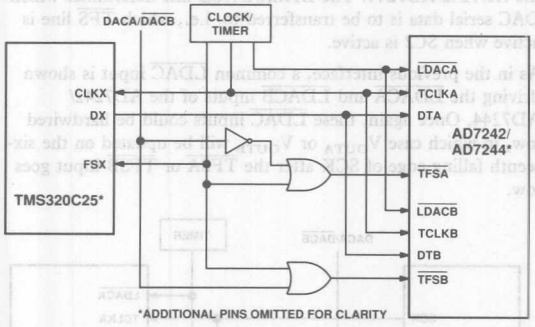


Figure 9. AD7242/AD7244 to TMS320C25 Interface

AD7242/AD7244 to 87C51 Interface

A serial interface between the AD7242/AD7244 and the 87C51 microcontroller is shown in Figure 10. TXD of the 87C51 drives TCLKA and TCLKB of the AD7242/AD7244 while RXD drives the two serial data lines of the part. The $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ signals are derived from P3.2 and P3.3, respectively.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7242/AD7244 and the last bit to be sent is the LSB of the word to be loaded to the AD7242/AD7244. When data is to be transmitted to the part, P3.2 (for DACA) or P3.3 (for DACB) is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7242/AD7244, P3.2 (for DACA) or P3.3 (for DACB) is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7242/AD7244. When the second serial transfer is complete, the P3.2 line (for DACA) or the P3.3 line (for DACB) is taken high.

Figure 10 shows both $\overline{\text{LDAC}}$ inputs of the AD7242/AD7244 hardwired low. As a result, the DAC latch and the analog output of one of the DACs will be updated on sixteenth falling edge of TXD after the respective $\overline{\text{TFS}}$ signal for that DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ inputs are driven from a timer, can be used.

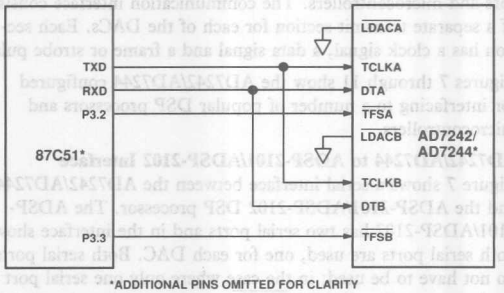


Figure 10. AD7242/AD7244 to 87C51 Interface

AD7242/AD7244 to 68HC11 Interface

Figure 11 shows a serial interface between the AD7242/AD7244 and the 68HC11 microcontroller. SCK of the 68HC11 drives TCLKA and TCLKB of the AD7242/AD7244 while the MOSI output drives the two serial data lines of the AD7242/AD7244. The $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ signals are derived from PC6 and PC7, respectively.

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC6 (for DACA) or PC7 (for DACB) is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7242/AD7244, PC6 (for DACA) or PC7 (for DACB) is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7242/AD7244. When the second serial transfer is complete, the PC6 line (for DACA) or the PC7 line (for DACB) is taken high.

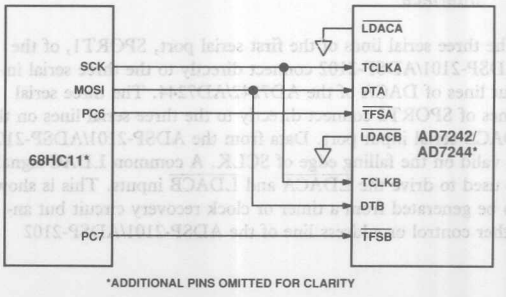


Figure 11. AD7242/AD7244 to 68HC11 Interface

Figure 11 shows both $\overline{\text{LDAC}}$ inputs of the AD7242/AD7244 hardwired low. As a result, the DAC latch and the analog output of one of the DACs will be updated on the sixteenth falling edge of SCK after the respective $\overline{\text{TFS}}$ signal for that DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ inputs are driven from a timer, can be used.

APPLYING THE AD7242/AD7244

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7242 works on an LSB size of 1.465 mV, while the AD7244 works on an LSB size of 366 μV. Therefore, the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feed through to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7242/AD7244. Connect all analog grounds to this star ground and also connect the AD7242/AD7244 DGND pins to this ground. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the signal leads on the V_{OUTA} and V_{OUTB} signals and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC outputs and their destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

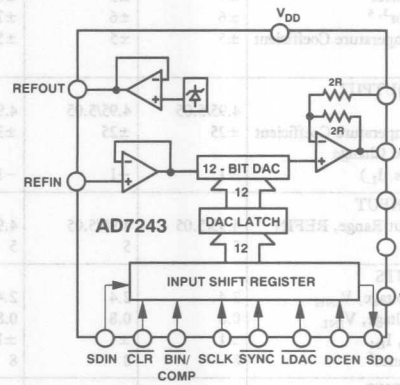
LC²MOS 12-Bit Serial DACPORT

AD7243

FEATURES
- 12-Bit CMOS DAC with
  - On-Chip Voltage Reference
  - Output Amplifier
- 3 Selectable Output Ranges
  - −5 V to +5 V, 0 to +5 V, 0 to +10 V
- Serial Interface
- 300 kHz DAC Update Rate
- Small Size: 16-Pin DIP or SOIC
- Nonlinearity: ±1/2 LSB T_{min} to T_{max}
- Low Power Dissipation: 100 mW typical

APPLICATIONS
- Process Control
- Industrial Automation
- Digital Signal Processing Systems
- Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7243 is a complete 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.

The output amplifier is capable of developing +10 V across a 2 kΩ load. The output voltage ranges with single supply operation are 0 to +5 V or 0 to +10 V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

The data format is natural binary in both unipolar ranges, while either offset binary or 2s complement format may be selected in the bipolar range. A $\overline{CLR}$ function is provided which sets the output to 0 V in both unipolar ranges and in the 2s complement bipolar range, while with offset binary data format, the output is set to −REFIN. This function is useful as a power-on reset as it allows the output to be set to a known voltage level.

The AD7243 features a fast versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz. A serial data output capability is also provided which allows daisy chaining in multi-DAC systems. This feature allows any number of DACs to be used in a system with a simple 4-wire interface. All DACs may be updated simultaneously using $\overline{LDAC}$.

The AD7243 is fabricated on Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process. It is packaged in 16-pin DIP and 16-pin SOIC packages.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT™
   The AD7243 is a complete, voltage output, 12-bit DAC on a single chip. The single chip design is inherently more reliable than multichip designs.
2. Single or Dual Supply Operation.
3. Minimum 3-wire interface to most DSP processors.
4. DAC Update Rate–300 kHz.
5. Serial Data Output allows easy daisy-chaining in multiple DAC systems.

DACPORT is a trademark of Analog Devices, Inc.

AD7243—SPECIFICATIONS

(V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V, REFIN = +5 V, R_L = 2 kΩ, C_L = 100 pF to AGND. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A[2]	B[2]	S[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±4	±4	±5	LSB max	V_{SS} = 0 V or −12 V to −15 V;[1] DAC Latch Contents All 0s
Bipolar Zero Error[3]	±5	±5	±6	LSB max	V_{SS} = −12 V to −15 V[1]; DAC Latch Contents All 0s
Full-Scale Error[3, 4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔREFOUT vs. I_L)	−1	−1	−1	mV max	Reference Load Current (I_L) Change (0–100 μA)
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ±1% for Specified Performance
Input Current	5	5	5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
DIGITAL OUTPUT					
Serial Data Out (SDO)					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.0 mA
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 400 μA
ANALOG OUTPUT					
Output Range Resistor, R_{OFS}	15/30	15/30	15/30	kΩ min/ max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = −12 V to −15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	12	μs max	Typically 3 μs
Negative Full-Scale Change	10	10	10	μs max	Typically 5 μs; V_{SS} = −12 V to −15 V[1]
Negative Full-Scale Change	10	10	10	μs typ	V_{SS} = 0 V
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and All 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	LDAC = High
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range (Dual Supplies)	−10.8/−16.5	−11.4/−15.75	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	12	mA max	Output Unloaded; Typically 7 mA
I_{SS} (Dual Supplies)	4	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Power Supply Tolerance A Version: ±10%; B, S Versions: ±5%.
[2]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[3]See terminology.
[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.
[5]Sample tested @ +25°C to ensure compliance.
[6]0 to +10 V output range is available only with $V_{DD} \geq +14.25$ V.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD7243AN	−40°C to +85°C	±1 LSB	N-16
AD7243BN	−40°C to +85°C	±1/2 LSB	N-16
AD7243AR	−40°C to +85°C	±1 LSB	R-16
AD7243BR	−40°C to +85°C	±1/2 LSB	R-16
AD7243AQ	−40°C to +85°C	±1 LSB	Q-16
AD7243BQ	−40°C to +85°C	±1/2 LSB	Q-16
AD7243SQ[2]	−55°C to +125°C	±1 LSB	Q-16

NOTES
[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.
[2]Available to /883B processing only. Contact your local sales office for military data sheet.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +10.8 V to +16.5 V, V_{SS} = 0 V or −10.8 V to −16.5 V, AGND = DGND = 0 V, R_L = 2kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	190	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	100	100	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low
t_9	75	75	ns min	$\overline{CLR}$ Pulse Width
t_{10}[4]	120	180	ns max	SCLK Falling Edge to SDO Valid

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 7 & 8.
[3]SCLK mark/space ratio range is 40/60 to 60/40.
[4]SDO load capacitance is no greater than 50 pF.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND, DGND . . . . . −0.3 V to +17 V
V_{SS} to AGND, DGND . . . . . +0.3 V to −17 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{OUT}[1] to AGND . . . . . −6 V to V_{DD} + 0.3 V
REFOUT to AGND . . . . . 0 V to V_{DD}
REFIN to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
SDO to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

NOTES
[1]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TERMINOLOGY

Bipolar Zero Error
Bipolar Zero Error is the voltage measured at V_{OUT} when the DAC is configured for bipolar output and loaded with all 0s (2s Complement Coding) or with 1000 0000 0000 (Offset Binary Coding). It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

Full-Scale Error
Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

Digital-to-Analaog Glitch Impulse
This is the voltage spike that appears at V_{OUT} when the digital code in the DAC latch changes, before the output settles to its final value. The energy in the glitch is specified in nV secs, and is measured for an all codes change from 0000 0000 0000 to 1111 1111 1111.

Digital Feedthrough
This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7243. It is measured with $\overline{LDAC}$ held high.

TERMINOLOGY (CONTINUED)

Relative Accuracy (Linearity)
Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Single Supply Linearity and Gain Error
The output amplifier on the AD7243 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1.

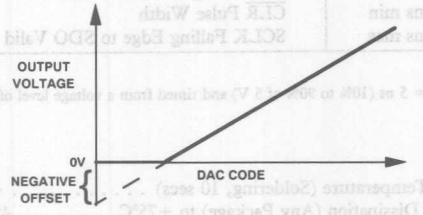


Figure 1. Effect of Negative Offset (Single Supply)

This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7243 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the A and B versions the linearity is measured between Codes 3 and 4095. For the S grade, linearity is measured between Code 5 and Code 4095.

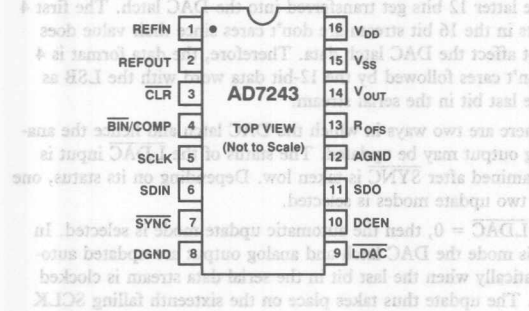
Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Unipolar Offset Error
Unipolar Offset Error is the measured output voltage from V_{OUT} with all zeros loaded into the DAC latch when the DAC is configured for unipolar output. It is due to a combination of the offset errors in the DAC and output amplifier.

PIN FUNCTION DESCRIPTION (DIP & SOIC PIN NUMBERS)

Pin	Mnemonic	Description
1	REFIN	Voltage Reference Input. It is internally buffered before being applied to the DAC. The nominal reference voltage for specified operation of the AD7243 is 5 V.
2	REFOUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part using its internal reference, REFOUT should be connected to REFIN.
3	$\overline{CLR}$	Clear, Logic Input. Taking this input low sets V_{OUT} to 0 V in both unipolar ranges and the 2s complement bipolar range and to −REFIN in the offset binary bipolar range.
4	$\overline{BIN}$/COMP	Logic Input . This input selects the data format to be either binary or 2s complement. In both unipolar ranges, natural binary format is selected by connecting this input to a logic "0." In the bipolar configuration, offset binary format is selected with a logic "0" while a logic "1" selects 2s complement format.
5	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
6	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
7	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
8	DGND	Digital Ground. Ground reference for all digital circuitry.
9	$\overline{LDAC}$	Load DAC, Logic Input. Updates the DAC output. The DAC output is updated on the falling edge of this signal or alternatively if this line is permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK pulse.
10	DCEN	Daisy-Chain Enable, Logic Input. Connect this pin high if a daisy-chain interface is being used, otherwise this pin must be connected low.
11	SDO	Serial Data Out, Logic Output. With DCEN at Logic "1" this output is enabled, and the serial data in the input shift register is clocked out on each falling SCLK edge.
12	AGND	Analog Ground. Ground reference for all analog circuitry.
13	R_{OFS}	Output Offset Resistor for the amplifier. It is connected to V_{OUT} for the +5 V range, to AGND for the +10 V range and to REFIN for the −5 V to +5 V range.
14	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and −5 V to +5 V.
15	V_{SS}	Negative Power Supply (used for the output amplifier only, may be connected to 0 V for single supply operation or to −12 V to −15 V for dual supplies).
16	V_{DD}	Positive Power Supply (+12 V to +15 V).

PIN CONFIGURATION
DIP and SOIC



CIRCUIT INFORMATION

D/A Section

The AD7243 contains a 12-bit voltage mode D/A converter consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The output voltage from the converter has the same polarity as the reference voltage, REFIN, allowing single supply operation.

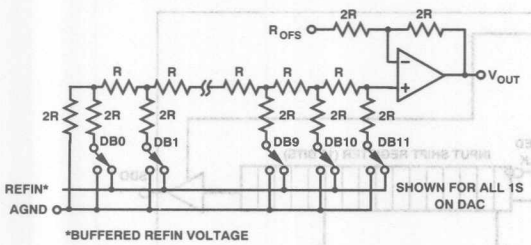


Figure 2. D/A Simplified Circuit Diagram

Internal Reference

The AD7243 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 5 V ± 50 mV. The reference voltage is provided at the REFOUT pin. This reference can be used to provide the reference voltage for the D/A converter (by connecting the REFOUT pin to the REFIN pin.)

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REFOUT for normal operation is 50 pF. If the reference is required for external use with capacitive loads greater than 50 pF then it should be decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

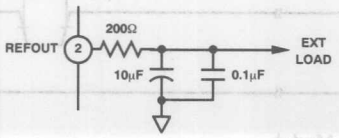


Figure 3. Reference Decoupling Scheme

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7243. References such as the AD586 provide an ideal external reference source (see Figure 10). The REFIN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter. The D/A converter is scaled for a 5 V reference and the device is tested with 5 V applied to REFIN. Other reference voltages may be used with degraded performance. Figure 4 shows the typical degradation in linearity vs. REFIN.

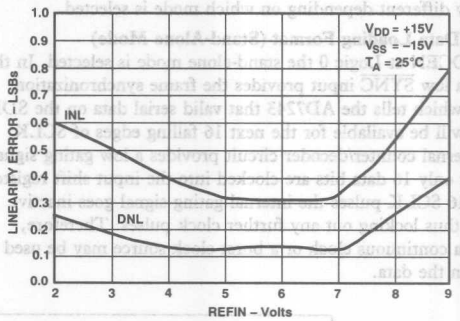


Figure 4. Typical Linearity vs. REFIN Voltage

Op Amp Section

The output of the voltage mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows three output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to AGND.

The output amplifier can be operated from a single +12 V to +15 V supply by tying V_{SS} = 0 V.

The amplifier can also be operated from dual supplies to allow an additional bipolar output range of −5 V to +5 V. Dual supplies are necessary for the bipolar output range but can also be used for the unipolar ranges to give faster settling time to voltages near 0 V, to allow full sink capability of 2.5 mA over the entire output range and to eliminate the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the output sink capability of the amplifier is shown in Figure 5.

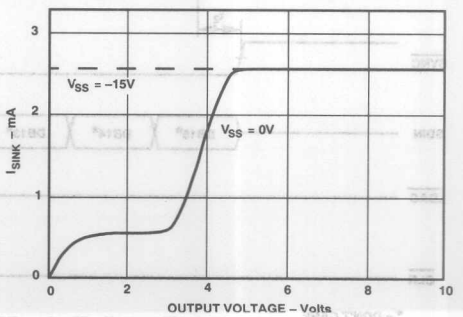


Figure 5. Amplifier Sink Current

DIGITAL INTERFACE

The AD7243 contains an input serial to parallel shift register and a DAC latch. A simplified diagram of the input loading circuitry is shown in Figure 6. Serial data on the SDIN input is loaded to the input register under control of DCEN, $\overline{SYNC}$ and SCLK. When a complete word is held in the shift register, it may then be loaded into the DAC latch under control of $\overline{LDAC}$. Only the data in the DAC latch determines the analog output on the AD7243.

The DCEN (daisy-chain enable) input is used to select either a stand-alone mode or a daisy-chain mode. The loading format is slightly different depending on which mode is selected.

Serial Data Loading Format (Stand-Alone Mode)

With DCEN at Logic 0 the stand-alone mode is selected. In this mode a low $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7243 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore, either a continuous clock or a burst clock source may be used to clock in the data.

The $\overline{SYNC}$ input should be taken high after the complete 16-bit word is loaded in.

Although 16 bits of data are clocked into the input register, only the latter 12 bits get transferred into the DAC latch. The first 4 bits in the 16 bit stream are don't cares since their value does not affect the DAC latch data. Therefore, the data format is 4 don't cares followed by the 12-bit data word with the LSB as the last bit in the serial stream.

There are two ways in which the DAC latch and hence the analog output may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes is selected.

If $\overline{LDAC}$ = 0, then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1, then the automatic update is disabled and the DAC latch is updated by taking $\overline{LDAC}$ low any time after the 16-bit data transfer is complete. The update now occurs on the falling edge of $\overline{LDAC}$. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated.

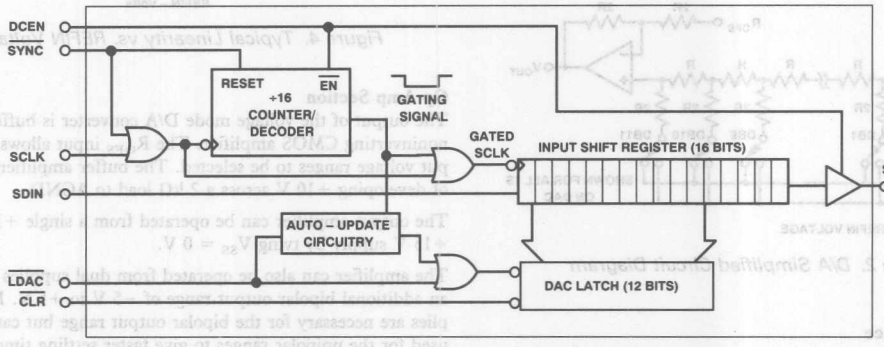


Figure 6. Simplified Loading Structure

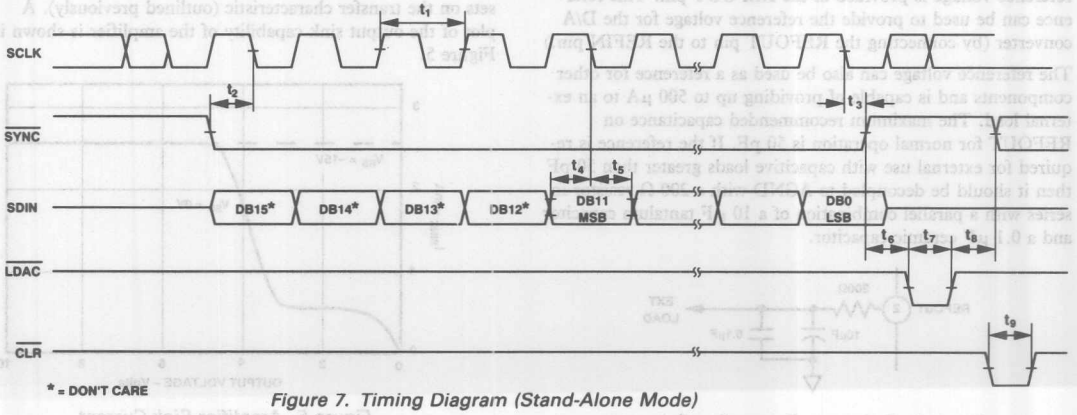


Figure 7. Timing Diagram (Stand-Alone Mode)

Serial Data Loading Format (Daisy-Chain Mode)

By connecting DCEN high the daisy-chain mode is enabled. This mode of operation is designed for multi-DAC systems where several AD7243s may be connected in cascade (see Figure 16). In this mode the internal gating circuitry on SCLK is disabled, and a serial data output facility is enabled. The internal gating signal is permanently active (low) so that the SCLK signal is continuously applied to the input shift register when $\overline{SYNC}$ is low. The data is clocked into the register on each falling SCLK edge after $\overline{SYNC}$ going low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. By connecting this line to the SDIN input on the next AD7243 in the chain, a multi-DAC interface may be constructed. Sixteen SCLK pulses are required for each DAC in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{SYNC}$ should be taken high. This prevents any further data being clocked into the input register.

A continuous SCLK source may be used if it can be arranged that $\overline{SYNC}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC latches with the lower 12 bits of data in each input register. All analog outputs are therefore updated simultaneously on the falling edge of $\overline{LDAC}$.

Clear Function ($\overline{CLR}$)

The clear function bypasses the input shift register and loads the DAC Latch with all 0s. It is activated by taking $\overline{CLR}$ low. In all ranges except the Offset Binary bipolar range (−5 V to +5 V) the output voltage is reset to 0 V. In the offset binary bipolar range the output is set to −REFIN. The clear function is especially useful at power-up as it enables the output to be reset to a known state.

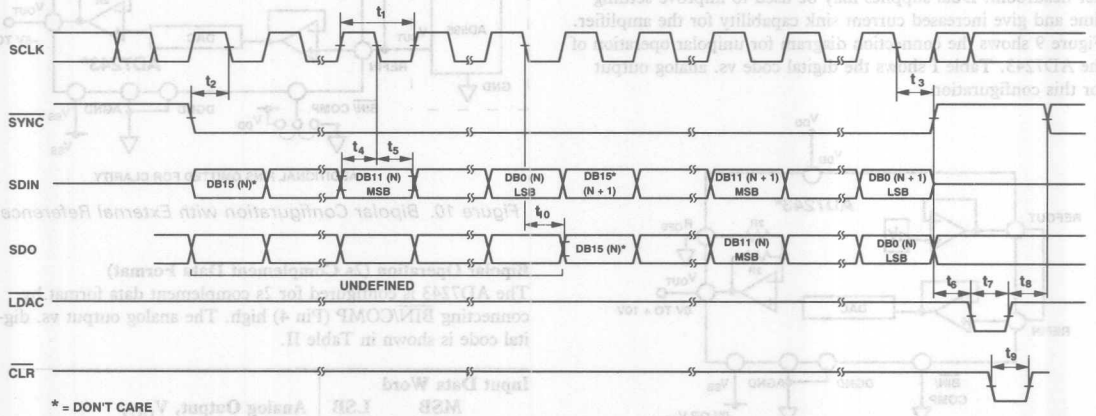


Figure 8. Timing Diagram (Daisy-Chain Mode)

APPLYING THE AD7243

Power Supply Decoupling:
To achieve optimum performance when using the AD7243, the V_{DD} and V_{SS} lines should each be decoupled to DGND using 0.1 μF capacitors. In noisy environments it is recommended that 10 μF capacitors be connected in parallel with the 0.1μF capacitors.

The internal scaling resistors provided on the AD7243 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below.

Unipolar (0 V to +10 V) Configuration
The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor R_{OFS} (Pin 13) to AGND. Natural Binary data format is selected by connecting $\overline{BIN}$/COMP (Pin 4) to DGND. In this configuration, the AD7243 can be operated using either single or dual supplies. Note that the V_{DD} supply must be ≥ +14.25 V for this range in order to maintain sufficient amplifier headroom. Dual supplies may be used to improve settling time and give increased current sink capability for the amplifier. Figure 9 shows the connection diagram for unipolar operation of the AD7243. Table I shows the digital code vs. analog output for this configuration.

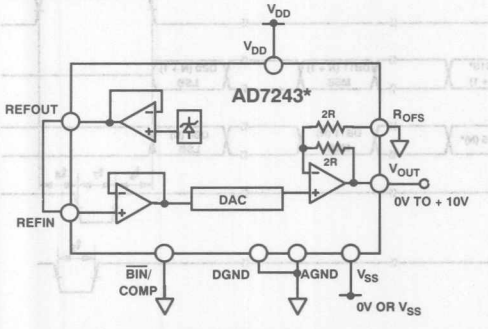


Figure 9. Unipolar (0 to +10 V) Configuration

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXX 1111 1111 1111	+2REFIN · (4095/4096)
XXXX 1000 0000 0001	+2REFIN · (2049/4096)
XXXX 1000 0000 0000	+2REFIN · (2048/4096) = +REFIN
XXXX 0111 1111 1111	+2REFIN · (2047/4096)
XXXX 0000 0000 0001	+2REFIN · (1/4096)
XXXX 0000 0000 0000	0 V

X = Don't Care.
Note: 1 LSB = 2REFIN/4096.

Table I. Unipolar Code Table (0 to +10 V Range)

Unipolar (0 V to +5 V) Configuration
The 0 V to +5 V output voltage range is achieved by connecting R_{OFS} to V_{OUT}. Once again, the AD7243 can be operated using either single or dual supplies. The table for output voltage vs. digital code is as in Table I, with 2REFIN replaced by REFIN. Note, for this range, 1 LSB = REFIN · (2^{-12}) = (REFIN/4096).

Bipolar (±5 V) Configuration
The bipolar configuration for the AD7243, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFS} to REFIN. The AD7243 must be operated from dual supplies to achieve this output voltage range. Either offset binary or 2s complement data format may be selected. Figure 10 shows the connection diagram for bipolar operation. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REFOUT to REFIN.

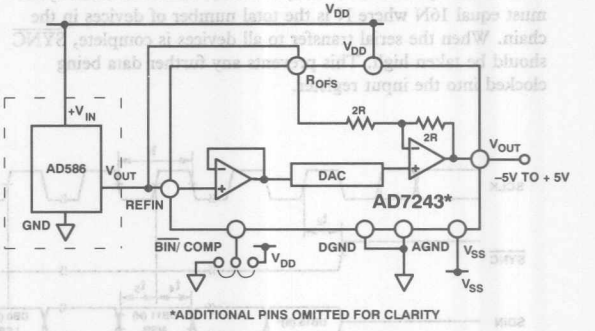


Figure 10. Bipolar Configuration with External Reference

Bipolar Operation (2s Complement Data Format)
The AD7243 is configured for 2s complement data format by connecting $\overline{BIN}$/COMP (Pin 4) high. The analog output vs. digital code is shown in Table II.

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXX 0111 1111 1111	+REFIN · (2047/2048)
XXXX 0000 0000 0001	+REFIN · (1/2048)
XXXX 0000 0000 0000	0 V
XXXX 1111 1111 1111	−REFIN · (1/2048)
XXXX 1000 0000 0001	−REFIN · (2047/2048)
XXXX 1000 0000 0000	−REFIN · (2048/2048)= −REFIN

X = Don't Care.
Note: 1 LSB = REFIN/2048.

Table II. 2s Complement Bipolar Code Table

Bipolar Operation (Offset Binary Data Format)
The AD7243 is configured for Offset Binary data format by connecting $\overline{BIN}$/COMP (Pin 4) low. The analog output vs. digital code may be obtained by inverting the MSB in Table II.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7243 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7243 requires a 16-bit data word with data valid on the falling edge of SCLK. For all the interfaces, the DAC update may be done automatically when all the data is clocked in or it may be done under control of $\overline{\text{LDAC}}$.

Figures 11 to 16 show the AD7243 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7243–ADSP-2101/ADSP-2102 Interface

Figure 11 shows a serial interface between the AD7243 and the ADSP-2101/ ADSP-2102 DSP processor. The ADSP-2101/ ADSP-2102 contains two serial ports, and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ADSP-2102 is clocked into the AD7243 on the falling edge of SCLK. When the data transfer is complete, $\overline{\text{TFS}}$ is taken high. In the interface shown the DAC is updated using an external timer which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, the $\overline{\text{LDAC}}$ input could be hard wired low and in this case the update takes place automatically on the sixteenth falling edge of SCLK.

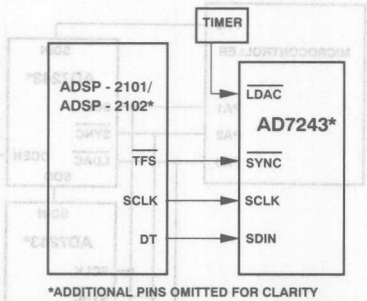


Figure 11. AD7243–ADSP-2101/ADSP-2102

AD7243–DSP56000 Interface

A serial interface between the AD7243 and the DSP56000 is shown in Figure 12. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a "0." SCK is internally generated on the DSP56000 and applied to the AD7243 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7243.

The $\overline{\text{LDAC}}$ input of the AD7243 is connected to DGND so the update of the DAC latch takes place automatically on the sixteenth falling edge of SCLK. An external timer could also be used as in the previous interface if an external update is required.

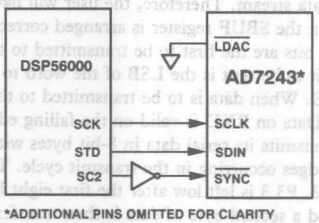


Figure 12. AD7243–DSP56000 Interface

AD7243–TMS32020 Interface

Figure 13 shows a serial interface between the AD7243 and the TMS32020 DSP processor. In this interface, the CLKX and FSX signals for the TMS32020 should be generated using external clock/timer circuitry. The FSX pin of the TMS32020 must be configured as an input. Data from the TMS32020 is valid on the falling edge of CLKX.

The clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal for the AD7243 to synchronize the update of the output with the serial transmission. Alternatively, the automatic update mode may be selected by connecting $\overline{\text{LDAC}}$ to DGND.

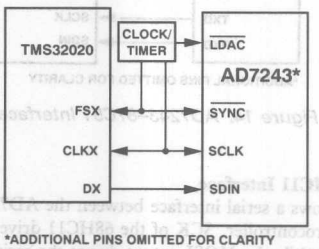


Figure 13. AD7243–TMS32020 Interface

AD7243–87C51 Interface

A serial interface between the AD7243 and the 87C51 microcontroller is shown in Figure 14. TXD of the 87C51 drives SCLK of the AD7243, while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is derived from the port line P3.3

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7243 and the last bit to be sent is the LSB of the word to be loaded to the AD7243. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7243, P3.3 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7243. When the second serial transfer is complete, the P3.3 line is taken high.

Figure 14 shows the $\overline{LDAC}$ input of the AD7243 hard wired low. As a result, the DAC latch and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{SYNC}$ signal for the DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{LDAC}$ input is driven from a timer, can be used.

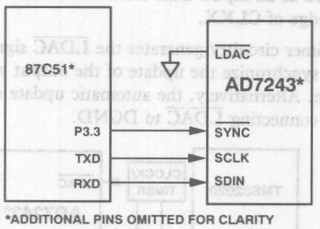


Figure 14. AD7243–87C51 Interface

AD7243–68HC11 Interface

Figure 15 shows a serial interface between the AD7243 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7243 while the MOSI output drives the serial data line of the AD7243. The $\overline{SYNC}$ signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7243, PC7 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7243. When the second serial transfer is complete, the PC7 line is taken high.

Figure 15 shows the $\overline{LDAC}$ input of the AD7243 hardwired low. As a result, the DAC latch and the analog output of the DAC will be updated on the sixteenth falling edge of SCK after the respective $\overline{SYNC}$ signal has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{LDAC}$ input is driven from a timer, can be used.

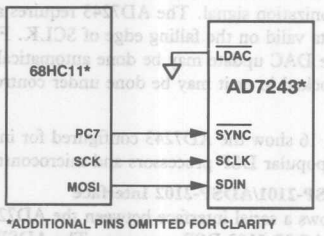


Figure 15. AD7243–68HC11 Interface

Multiple DAC Daisy-Chain Interface

A multi-DAC serial interface is shown in Figure 16. This scheme may be used with all of the interfaces previously discussed if more than one DAC is required in a system. To enable the facility the DCEN pin must be connected high on all devices, including the last device in the chain.

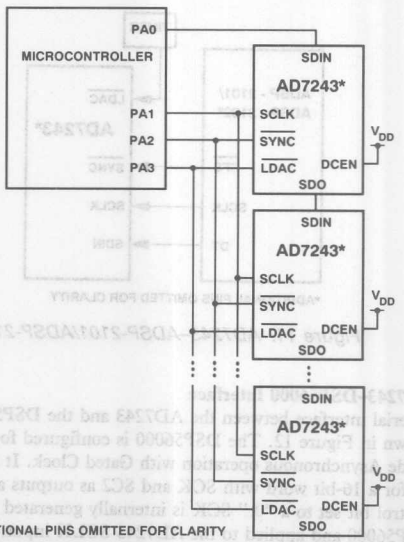


Figure 16. AD7243 Daisy-Chain Configuration

Common clock, data, and synchronization signals are applied to all DACs in the chain. The loading sequence starts by taking $\overline{SYNC}$ low. The data is then clocked into the input registers on the falling edge of SCLK. Sixteen clock pulses are required for each DAC in the chain. The data ripples through the input registers with the first 16-bit word filling the last register in the chain after 16N clock pulses where N= the total number of DACs in the chain.

When valid data has been loaded into all the registers, the $\overline{SYNC}$ input should be taken high and a common $\overline{LDAC}$ pulse used to update all the DACs simultaneously.

APPLICATIONS

OPTO-ISOLATED INTERFACE

In many process control type applications it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3 kV. The serial loading structure of the AD7243 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum.

Figure 17 shows a 4-channel isolated interface using the AD7243. The DCEN pin must be connected high to enable the daisy-chain facility. Four channels with 12-bit resolution are provided in the circuit shown, but this may be expanded to accommodate any number of DAC channels without any extra isolation circuitry.

The sequence of events to program the output channels is as follows.

1. Take the $\overline{SYNC}$ line low.
2. Transmit the data as four 16-bit words. A total of 64 clock pulses is required to clock the data through the chain.
3. Take the $\overline{SYNC}$ line high.
4. Pulse the $\overline{LDAC}$ line low. This updates all output channels simultaneously on the falling edge of $\overline{LDAC}$.

To reduce the number of opto-couplers, the $\overline{LDAC}$ line could be driven from a one shot which is triggered by the rising edge on the $\overline{SYNC}$ line. A low level pulse of 50 ns duration or greater is all that is required to update the outputs.

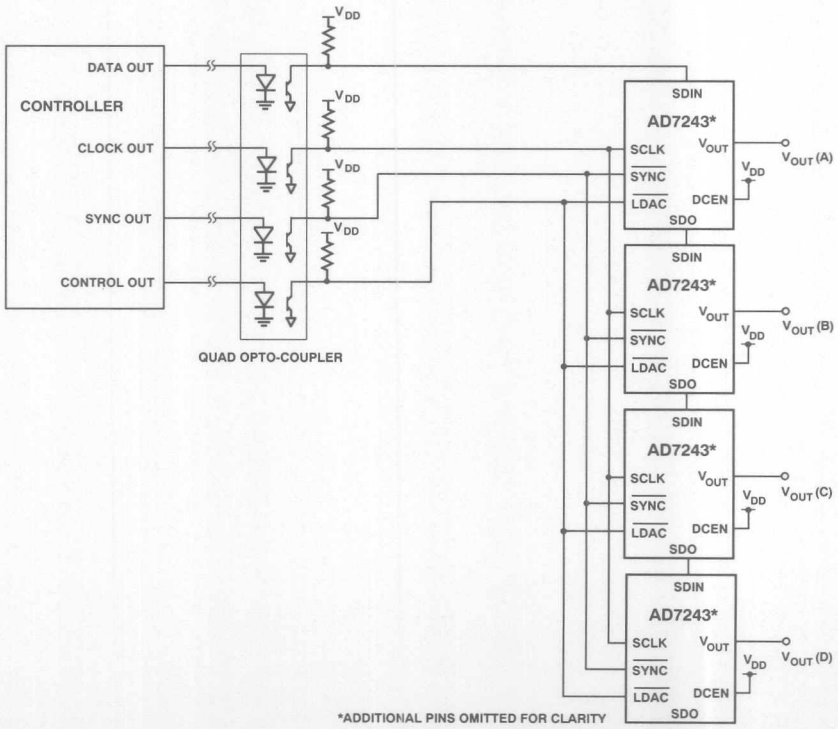


Figure 17. Four-Channel Opto-Isolated Interface

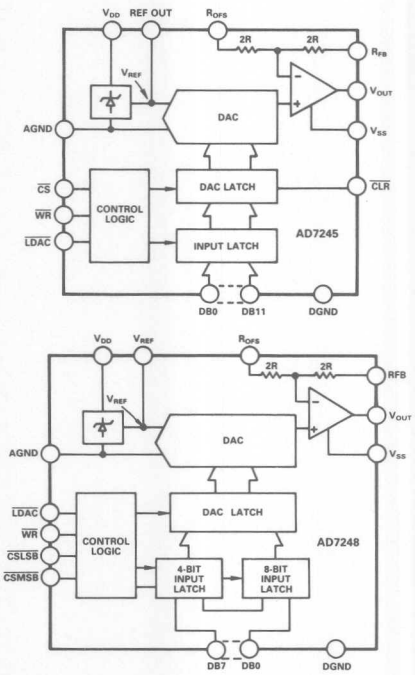
LC²MOS 12-Bit DACPORTS

AD7245/AD7248

FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Parallel Loading Structure: AD7245
(8+4) Loading Structure: AD7248
Single or Dual Supply Operation
Fast Digital Interface (80ns $\overline{WR}$ Pulse)
Low Power (65mW typ)
0.3", Skinny, 20- and 24-Pin DIP
20- and 28-Terminal Surface Mount Packages
NOTE: AD7245A/AD7248A IS RECOMMENDED FOR NEW DESIGNS

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7245/AD7248 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The part features double-buffered interface logic with a 12-bit input latch and 12-bit DAC latch. The data held in the DAC latch determines the analog output of the converter. The AD7245 accepts 12-bit parallel data which is latched into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248 has an 8-bit-wide data bus, and data is loaded to the input latch in two write operations, an 8-bit LSB load and a 4-bit MSB load. The input data must be right justified. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch. The AD7245 also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.

The on-chip 5V buried Zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V when using single supply and 0 to +5V, −5V to +5V when operated in dual supplies. The output amplifier is capable of developing +10V across a 2kΩ load to GND.

The AD7245/AD7248 is fabricated in an all ion-implanted, high-speed linear, compatible CMOS (LC²MOS) process. The AD7245 is packaged in a small, 0.3"-wide, 24-pin DIP and 28-terminal surface mount packages. The AD7248 is available in a 0.3"-wide, 20-pin DIP and 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT™
   The AD7245/AD7248 is a complete, voltage output, 12-bit DAC on one chip. This single-chip design of the DAC reference and output amplifier is inherently more reliable than multichip designs.
2. Microprocessor Compatibility
   The parallel loading structure of the AD7245 allows connection to microprocessors with a 16-bit-wide data bus. The AD7248 is aimed at microprocessors which have an 8-bit-wide data bus structure. The high-speed logic of both parts allows direct interfacing to most modern microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245/AD7248 in multiple DAC systems.

DACPORT is a trademark of Analog Devices, Inc.

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REV. A

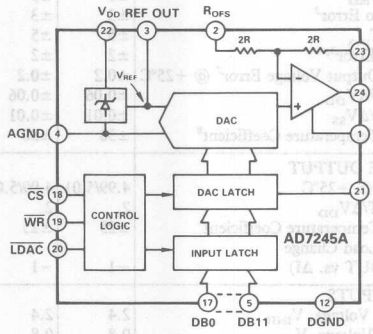
LC²MOS 12-Bit DACPORTs

AD7245A/AD7248A

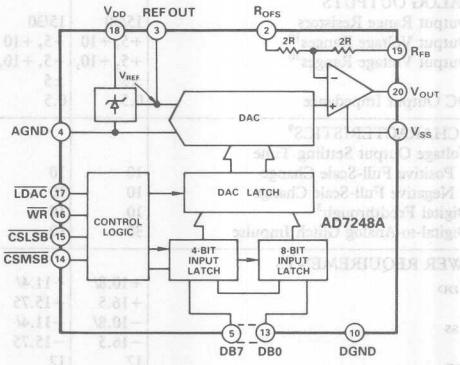
FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Improved AD7245/AD7248:
12 V to 15 V Operation
±1/2 LSB Linearity Grade
Faster Interface–40 ns typ Data Setup Time
Extended Plastic Temperature Range (–40°C to +85°C)
Single or Dual Supply Operation
Low Power–65 mW typ in Single Supply
Parallel Loading Structure: AD7245A
(8+4) Loading Structure: AD7248A

AD7245A FUNCTIONAL BLOCK DIAGRAM



AD7248A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7245A/AD7248A is an enhanced version of the industry standard AD7245/AD7248. Improvements include operation from 12 V to 15 V supplies, a ±1/2 LSB linearity grade, faster interface times and better full scale and reference variations with V_{DD}. Additional features include extended temperature range operation for commercial and industrial grades.

The AD7245A/AD7248A is a complete, 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and double-buffered interface logic. The AD7245A accepts 12-bit parallel data which is loaded into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248A has an 8-bit wide data bus with data loaded to the input latch in two write operations. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch and updates the analog output. The AD7245A also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented.

The on-chip 5 V buried Zener diode provides a low noise, temperature compensated reference for the DAC. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7245A/AD7248A is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7245A is available in a small, 0.3″ wide, 24-pin DIP and SOIC and in 28-terminal surface mount packages. The AD7248A is packaged in a small, 0.3″ wide, 20-pin DIP and SOIC and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. The AD7245A/AD7248A is a 12-bit DACPORT™ on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multi-chip designs.
2. The improved interface times on the part allows easy, direct interfacing to most modern microprocessors.
3. The AD7245A/AD7248A features a wide power supply range allowing operation from 12 V supplies.

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Parameter	Version	Version	Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error at +25°C[3]	±3	±3	±3	LSB max	V_{SS} = 0 V or −12 V to −15 V[4]
T_{min} to T_{max}	±5	±5	±5	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
Bipolar Zero Error[3]	±3	±3	±3	LSB max	R_{OFS} connected to REF OUT; V_{SS} = −12 V to −15 V[4]
T_{min} to T_{max}	±5	±5	±5	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
DAC Gain Error[3, 6]	±2	±2	±2	LSB max	
Full-Scale Output Voltage Error[7] @ +25°C	±0.2	±0.2	±0.2	% of FSR max	V_{DD} = +15 V
ΔFull Scale/ΔV_{DD}	±0.06	±0.06	±0.06	% of FSR/V max	V_{DD} = +12 V to +15 V[4]
ΔFull Scale/ΔV_{SS}	±0.01	±0.01	±0.01	% of FSR/V max	V_{SS} = −12 V to −15 V[4]
Full-Scale Temperature Coefficient[8]	±30	±30	±40	ppm of FSR/°C max	V_{DD} = +15 V
REFERENCE OUTPUT					
REF OUT @ +25°C	4.99/5.01	4.99/5.01	4.99/5.01	V min/V max	V_{DD} = +15 V
ΔREF OUT/ΔV_{DD}	2	2	2	mV/V max	V_{DD} = +12 V to +15 V[4]
Reference Temperature Coefficient	±25	±25	±35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–100 μA)
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[9]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges[10]	+5, +10	+5, +10	+5, +10	V	V_{SS} = 0 V; Pin Strappable
Output Voltage Ranges[10]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −12 V to −15 V;[4] Pin Strappable
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[9]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	10	μs max	DAC Latch All 0s to All 1s
Negative Full-Scale Change	10	10	10	μs max	DAC Latch All 1s to All 0s; V_{SS} = −12 V to −15 V[4]
Digital Feedthrough[3]	10	10	10	nV-s typ	
Digital-to-Analog Glitch Impulse	30	30	30	nV-s typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/ +16.5	+11.4/ +15.75	+11.4/ +15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
V_{SS}	−10.8/ −16.5	−11.4/ −15.75	−11.4/ −15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
I_{DD}	12	12	12	mA max	Output Unloaded; Typically 5 mA
I_{SS} (Dual Supplies)	3	3	5	mA max	Output Unloaded;Typically 2 mA

NOTES

[1]Power supply tolerance is ±10% for A Version and ±5% for B and S Versions.

[2]Temperature ranges are as follows: A/B Versions; −40°C to +85°C; S Version; −55°C to +125°C.

[3]See Terminology.

[4]With appropriate power supply tolerances.

[5]FSR means Full-Scale Range and is 5 V for the 0 to +5 V output range and 10 V for both the 0 to +10 V and ±5 V output ranges.

[6]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

[7]This error is calculated with respect to an ideal 4.9988 V on the 0 to +5 V and ±5 V ranges; it is calculated with respect to an ideal 9.9976 V on the 0 to +10 V range. It includes the effects of internal voltage reference, gain and offset errors.

[8]Full-Scale TC = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = +25°C to T_{min} or T_{max}.

[9]Sample tested at +25°C to ensure compliance.

[10]0 to +10 V output range is available only when $V_{DD} \geq +14.25$ V.

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1] (V_{DD} = +12 V to +15 V;[2] V_{SS} = 0 V or −12 V to −15 V;[2] See Figures 5 and 7.)

Parameter	A, B Versions	S Version	Units	Conditions
t_1				
@ +25°C	55	55	ns typ	Chip Select Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_2				
@ +25°C	40	40	ns typ	Write Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_3				
@ +25°C	0	0	ns min	Chip Select to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@ +25°C	0	0	ns min	Chip Select to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@ +25°C	40	40	ns typ	Data Valid to Write Setup Time
T_{min} to T_{max}	80	80	ns min	
t_6				
@ +25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	
t_7				
@ +25°C	40	40	ns typ	Load DAC Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_8				
@ +25°C	40	40	ns typ	Clear Pulse Width
T_{min} to T_{max}	80	100	ns min	

NOTE
[1]Sample tested at +25°C to ensure compliance.
[2]Power supply tolerance is ±10% for A Version and ±5% for B and S Versions.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +17 V
V_{DD} to DGND . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND . . . . . −0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . . −0.3 V, V_{DD} +0.3 V
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
V_{OUT} to V_{SS}[1] . . . . . 0 V, +24 V
V_{OUT} to V_{DD}[1] . . . . . −32 V, 0 V
REF OUT[1] to AGND . . . . . 0 V, V_{DD}
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

Operating Temperature
Commercial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. V_{OUT} short circuit current is typically 80 mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD7245A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7245AAN	−40°C to +85°C	±1 LSB max	N-24
AD7245ABN	−40°C to +85°C	±1/2 LSB max	N-24
AD7245AAQ	−40°C to +85°C	±1 LSB max	Q-24
AD7245ASQ[3]	−55°C to +125°C	±1 LSB max	Q-24
AD7245AAP	−40°C to +85°C	±1 LSB max	P-28A
AD7245AAR	−40°C to +85°C	±1 LSB max	R-24
AD7245ABR	−40°C to +85°C	±1/2 LSB max	R-24
AD7245ASE[3]	−55°C to +125°C	±1 LSB max	E-28A

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[2]This grade will be available to /883B processing only.

AD7248A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7248AAN	−40°C to +85°C	±1 LSB max	N-20
AD7248ABN	−40°C to +85°C	±1/2 LSB max	N-20
AD7248AAQ	−40°C to +85°C	±1 LSB max	Q-20
AD7248ASQ[3]	−55°C to +125°C	±1 LSB max	Q-20
AD7248AAP	−40°C to +85°C	±1 LSB max	P-20A
AD7248AAR	−40°C to +85°C	±1 LSB max	R-20
AD7248ABR	−40°C to +85°C	±1/2 LSB max	R-20

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[2]This grade will be available to /883B processing only.

TERMINOLOGY

RELATIVE ACCURACY
Relative Accuracy, or end-point nonlinearity, is a measure of the actual deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH
Digital Feedthrough is the glitch impulse injected from the digital inputs to the analog output when the inputs change state. It is measured with $\overline{LDAC}$ high and is specified in nV-s.

DAC GAIN ERROR
DAC Gain Error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been allowed for. It is, therefore defined as:

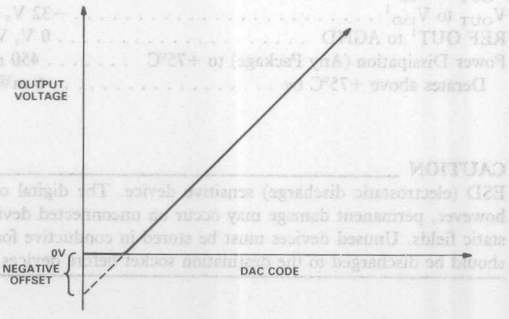
Measured Value—Offset—Ideal Value

where the ideal value is calculated relative to the actual reference value.

UNIPOLAR OFFSET ERROR
Unipolar Offset Error is a combination of the offset errors of the voltage mode DAC and the output amplifier and is measured when the part is configured for unipolar outputs. It is present or all codes and is measured with all 0s in the DAC register.

BIPOLAR ZERO OFFSET ERROR
Bipolar Zero Offset Error is measured when the part is configured for bipolar output and is a combination of errors from the DAC and output amplifier. It is present for all codes and is measured with a code of 2048 (decimal) in the DAC register.

SINGLE SUPPLY LINEARITY AND GAIN ERROR
The output amplifier of the AD7245A/AD7248A can have a true negative offset even when the part is operated from a single positive power supply. However, because the lower supply rail to the part is 0 V, the output voltage cannot actually go negative. Instead the output voltage sits on the lower rail and this results in the transfer function shown across. This is an offset effect and the transfer function would have followed the dotted line if the output voltage could have gone negative. Normally, linearity is measured after offset and full scale have been adjusted or allowed for. On the AD7245A/AD7248A the negative offset is allowed for by calculating the linearity from the code which the amplifier comes off the lower rail. This code is given by the negative offset specification. For example, the single supply linearity specification applies between Code 3 and Code 4095 for the 25°C specification and between Code 5 and Code 4095 over the T_{min} to T_{max} temperature range. Since gain error is also measured after offset has been allowed for, it is calculated between the same codes as the linearity error. Bipolar linearity and gain error are measured between Code 0 and Code 4095.



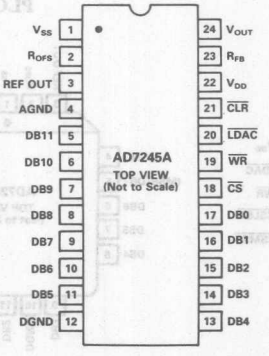
AD7245A PIN FUNCTION DESCRIPTION
(DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB11	Data Bit 11. Most Significant Bit (MSB).
6–11	DB10–DB5	Data Bit 10 to Data Bit 5.
12	DGND	Digital Ground.
13–16	DB4–DB1	Data Bit 4 to Data Bit 1.
17	DB0	Data Bit 0. Least Significant Bit (LSB).
18	$\overline{CS}$	Chip Select Input (Active LOW). The device is selected when this input is active.
19	$\overline{WR}$	Write Input (Active LOW). This is used in conjunction with $\overline{CS}$ to write data into the input latch of the AD7245A.
20	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
21	$\overline{CLR}$	Clear Input (Active LOW). When this input is active the contents of the DAC latch are reset to all 0s.
22	V_{DD}	Positive Supply Voltage.
23	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
24	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V or −5 V to +5 V.

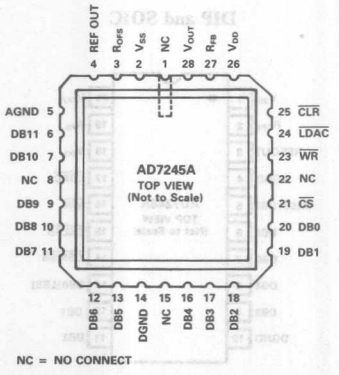
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AD7245A PIN CONFIGURATIONS

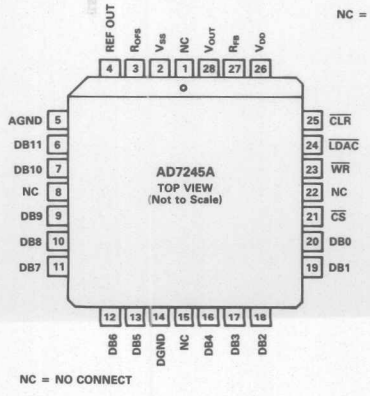
DIP and SOIC



LCCC



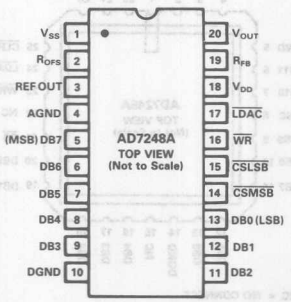
PLCC



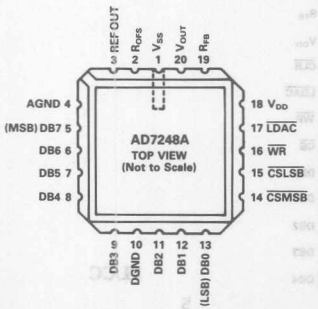
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB7	Data Bit 7.
6	DB6	Data Bit 6.
7	DB5	Data Bit 5.
8	DB4	Data Bit 4.
9	DB3	Data Bit 3/Data Bit 11 (MSB).
10	DGND	Digital Ground.
11	DB2	Data Bit 2/Data Bit 10.
12	DB1	Data Bit 1/Data Bit 9.
13	DB0	Data Bit 0 (LSB)/Data Bit 8.
14	$\overline{CSMSB}$	Chip Select Input for MS Nibble. (Active LOW). This selects the upper 4 bits of the input latch. Input data is right justified.
15	$\overline{CSLSB}$	Chip Select Input for LS byte. (Active LOW). This selects the lower 8 bits of the input latch.
16	$\overline{WR}$	Write Input This is used in conjunction with $\overline{CSMSB}$ and $\overline{CSLSB}$ to load data into the input latch of the AD7248A.
17	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
18	V_{DD}	Positive Supply Voltage.
19	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
20	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V or −5 V to +5 V.

AD7248A PIN CONFIGURATIONS

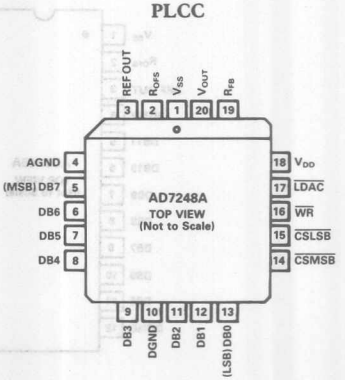
DIP and SOIC

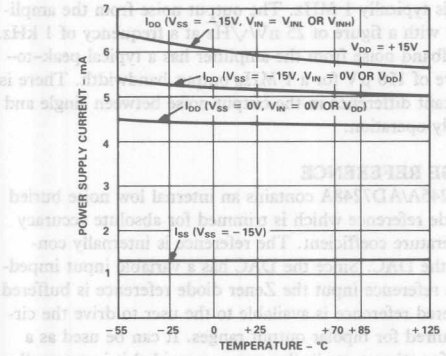


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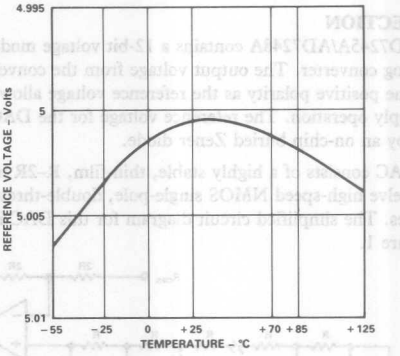


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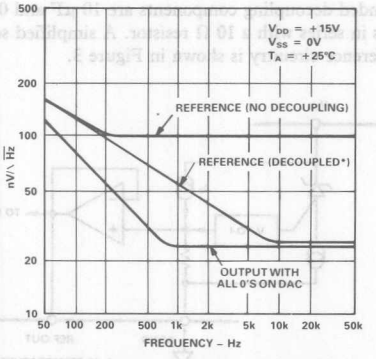




Power Supply Current vs. Temperature

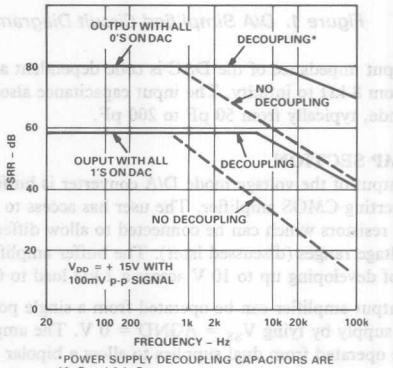


Reference Voltage vs. Temperature



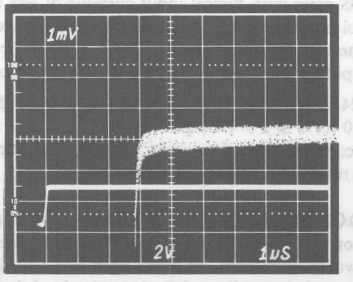
*REFERENCE DECOUPLING COMPONENTS AS PER FIGURE 8

Noise Spectral Density vs. Frequency

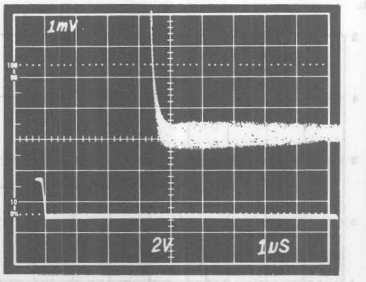


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF and 0.1μF

Power Supply Rejection Ration vs. Frequency



Positive-Going Settling Time (V_{DD} = +15 V, V_{SS} = −15 V)



Negative Going Settling Time (V_{DD} = +15 V, V_{SS} = −15 V)

CIRCUIT INFORMATION

D/A SECTION

The AD7245A/AD7248A contains a 12-bit voltage mode digital-to-analog converter. The output voltage from the converter has the same positive polarity as the reference voltage allowing single supply operation. The reference voltage for the DAC is provided by an on-chip buried Zener diode.

The DAC consists of a highly stable, thin-film, R–2R ladder and twelve high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

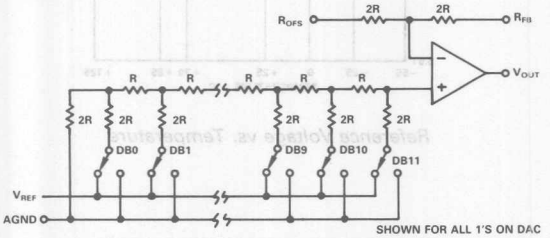


Figure 1. D/A Simplified Circuit Diagram

The input impedance of the DAC is code dependent and can vary from 8 kΩ to infinity. The input capacitance also varies with code, typically from 50 pF to 200 pF.

OP AMP SECTION

The output of the voltage mode D/A converter is buffered by a noninverting CMOS amplifier. The user has access to two gain setting resistors which can be connected to allow different output voltage ranges (discussed later). The buffer amplifier is capable of developing up to 10 V across a 2 kΩ load to GND.

The output amplifier can be operated from a single positive power supply by tying V_{SS} = AGND = 0 V. The amplifier can also be operated from dual supplies to allow a bipolar output range of −5 V to +5 V. The advantages of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0 V, full sink capability of 2.5 mA maintained over the entire output range and elimination of the effects of negative offset on the transfer characteristic (outlined previously). Figure 2 shows the sink capability of the amplifier for single supply operation.

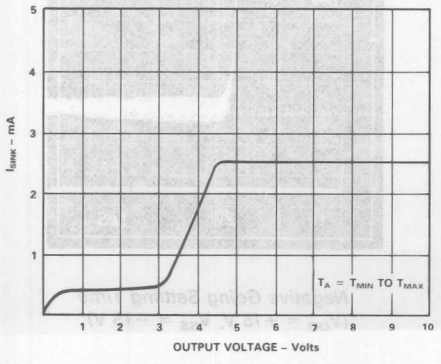


Figure 2. Typical Single Supply Sink Current vs. Output Voltage

The small signal (200 mV p–p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 25 nV/$\sqrt{\text{Hz}}$ at a frequency of 1 kHz. The broadband noise from the amplifier has a typical peak–to–peak figure of 150 μV for a 1 MHz output bandwidth. There is no significant difference in the output noise between single and dual supply operation.

VOLTAGE REFERENCE

The AD7245A/AD7248A contains an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. The reference is internally connected to the DAC. Since the DAC has a variable input impedance at its reference input the Zener diode reference is buffered. This buffered reference is available to the user to drive the circuitry required for bipolar output ranges. It can be used as a reference for other parts in the system provided it is externally buffered. The reference will give long-term stability comparable with the best discrete Zener reference diodes. The performance of the AD7245A/AD7248A is specified with internal reference, and all the testing and trimming is done with this reference. The reference should be decoupled at the REF OUT pin and recommended decoupling components are 10 μF and 0.1 μF capacitors in series with a 10 Ω resistor. A simplified schematic of the reference circuitry is shown in Figure 3.

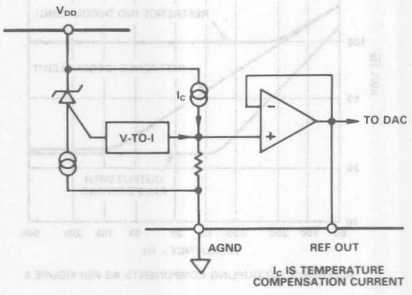


Figure 3. Internal Reference

DIGITAL SECTION

The AD7245A/AD7248A digital inputs are compatible with either TTL or 5 V CMOS levels. All data inputs are static protected MOS gates with typical input currents of less than 1 nA. The control inputs sink higher currents (150 μA max) as a result of the fast digital interfacing. Internal input protection of all logic inputs is achieved by on-chip distributed diodes.

The AD7245A/AD7248A features a very low digital feedthrough figure of 10 nV-s in a 5 V output range. This is due to the voltage mode configuration of the DAC. Most of the impulse is actually as a result of feedthrough across the package.

INTERFACE LOGIC INFORMATION—AD7245A

Table I shows the truth table for AD7245A operation. The part contains two 12-bit latches, an input latch and a DAC latch. $\overline{CS}$ and $\overline{WR}$ control the loading of the input latch while $\overline{LDAC}$ controls the transfer of information from the input latch to the DAC latch. All control signals are level triggered; and therefore, either or both latches may be made transparent, the input latch by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC latch by keeping $\overline{LDAC}$ "LOW." Input data is latched on the rising edge of $\overline{WR}$.

The data held in the DAC latch determines the analog output of the converter. Data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. This $\overline{LDAC}$ signal is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. For example, if $\overline{LDAC}$ goes LOW while $\overline{WR}$ is "LOW", then the $\overline{LDAC}$ signal must stay LOW for t_7 or longer after $\overline{WR}$ goes high to ensure correct data is latched through to the output.

Table I. AD7245A Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Latches are Transparent
H	H	H	X	Both Latches are Latched
H	H	X	H	Both Latches are Latched
H	H	L	L	Input Latches Transparent
H	H	↓	L	Input Latches Latched
H	L	H	H	DAC Latches Transparent
H	↓	H	H	DAC Latches Latched
L	X	X	X	DAC Latches Loaded with all 0s
↓	H	H	H	DAC Latches Latched with All 0s and Output Remains at 0 V or −5 V
↓	L	L	L	Both Latches are Transparent and Output Follows Input Data

H = High State L = Low State X = Don't Care

The contents of the DAC latch are reset to all 0s by a low level on the $\overline{CLR}$ line. With both latches transparent, the $\overline{CLR}$ line functions like a zero override with the output brought to 0 V in the unipolar mode and −5 V in the bipolar mode for the duration of the $\overline{CLR}$ pulse. If both latches are latched, a "LOW" pulse on the $\overline{CLR}$ input latches all 0s into the DAC latch and the output remains at 0 V (or −5 V) after the $\overline{CLR}$ line has returned "HIGH." The $\overline{CLR}$ line can be used to ensure powerup to 0 V on the AD7245A output in unipolar operation and is also useful, when used as a zero override, in system calibration cycles.

Figure 4 shows the input control logic for the AD7245A and the write cycle timing for the part is shown in Figure 5.

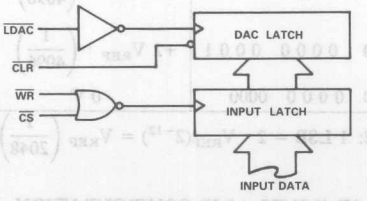
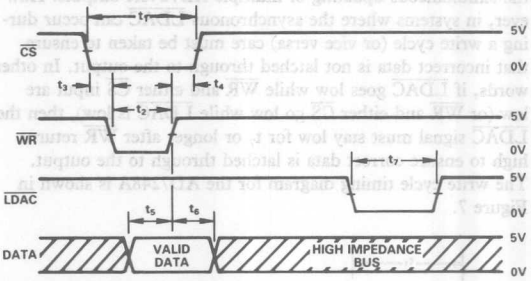


Figure 4. AD7245A Input Control Logic



NOTES
1. SEE TIMING SPECIFICATIONS.
2. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V, $t_r = t_f = 5ns$.
3. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$
4. IF $\overline{LDAC}$ IS ACTIVATED WHILE $\overline{WR}$ IS LOW THEN $\overline{LDAC}$ MUST STAY LOW FOR t_7 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 5. AD7245A Write Cycle Timing Diagram

INTERFACE LOGIC INFORMATION – AD7248A

The input loading structure on the AD7248A is configured for interfacing to microprocessors with an 8-bit wide data bus. The part contains two 12-bit latches—an input latch and a DAC latch. Only the data held in the DAC latch determines the analog output from the converter. The truth table for AD7248A operation is shown in Table II, while the input control logic diagram is shown in Figure 6.

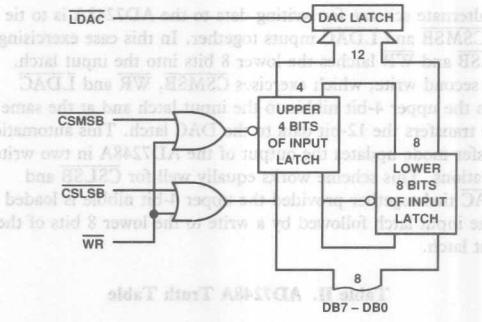


Figure 6. AD7248A Input Control Logic

$\overline{CSMSB}$, $\overline{CSLSB}$ and $\overline{WR}$ control the loading of data from the external data bus to the input latch. The eight data inputs on the AD7248A accept right justified data. This data is loaded to the input latch in two separate write operations. $\overline{CSLSB}$ and $\overline{WR}$ control the loading of the lower 8-bits into the 12-bit wide latch. The loading of the upper 4-bit nibble is controlled by $\overline{CSMSB}$ and $\overline{WR}$. All control inputs are level triggered, and input data for either the lower byte or upper 4-bit nibble is latched into the input latches on the rising edge of $\overline{WR}$ (or either $\overline{CSMSB}$ or $\overline{CSLSB}$). The order in which the data is loaded to the input latch (i.e., lower byte or upper 4-bit nibble first) is not important.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latch to the DAC latch. This $\overline{LDAC}$ signal is also level triggered, and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in

the simultaneous updating of multiple AD7248A outputs. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ goes low while $\overline{WR}$ and either $\overline{CS}$ input are low (or $\overline{WR}$ and either $\overline{CS}$ go low while $\overline{LDAC}$ is low), then the $\overline{LDAC}$ signal must stay low for t_7 or longer after $\overline{WR}$ returns high to ensure correct data is latched through to the output. The write cycle timing diagram for the AD7248A is shown in Figure 7.

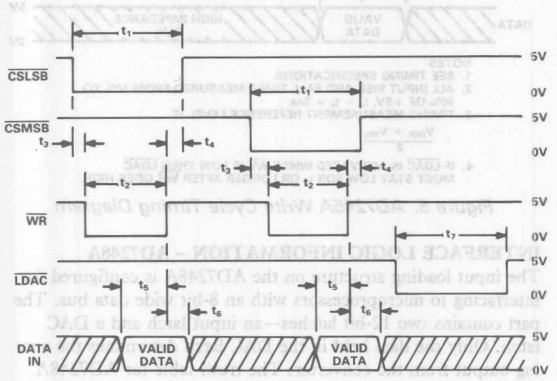


Figure 7. AD7248A Write Cycle Timing Diagram

An alternate scheme for writing data to the AD7248A is to tie the $\overline{CSMSB}$ and $\overline{LDAC}$ inputs together. In this case exercising $\overline{CSLSB}$ and $\overline{WR}$ latches the lower 8 bits into the input latch. The second write, which exercises $\overline{CSMSB}$, $\overline{WR}$ and $\overline{LDAC}$ loads the upper 4-bit nibble to the input latch and at the same time transfers the 12-bit data to the DAC latch. This automatic transfer mode updates the output of the AD7248A in two write operations. This scheme works equally well for $\overline{CSLSB}$ and $\overline{LDAC}$ tied together provided the upper 4-bit nibble is loaded to the input latch followed by a write to the lower 8 bits of the input latch.

Table II. AD7248A Truth Table

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
L	H	L	H	Load LS Byte into Input Latch
L	H	↓	H	Latches LS Byte into Input Latch
↓	H	L	H	Latches LS Byte into Input Latch
H	L	L	H	Loads MS Nibble into Input Latch
H	L	↓	H	Latches MS Nibble into Input Latch
H	↓	L	H	Latches MS Nibble into Input Latch
H	H	H	L	Loads Input Latch into DAC Latch
H	H	H	↓	Latches Input Latch into DAC Latch
H	L	L	L	Loads MS Nibble into Input Latch and Loads Input Latch into DAC Latch
H	H	H	H	No Data Transfer Operation

H = High State L = Low State

APPLYING THE AD7245A/AD7248A

The internal scaling resistors provided on the AD7245A/AD7248A allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of −5 V to +5 V. Connections for the various ranges are outlined below.

UNIPOLAR (0 V TO +10 V) CONFIGURATION

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the bipolar offset resistor, R_{OFS}, to AGND and connecting R_{FB} to V_{OUT}. In this configuration the AD7245A/AD7248A can be operated single supply (V_{SS} = 0 V = AGND). If dual supply performance is required, a V_{SS} of −12 V to −15 V should be applied. Figure 8 shows the connection diagram for unipolar operation while the table for output voltage versus the digital code in the DAC latch is shown in Table III.

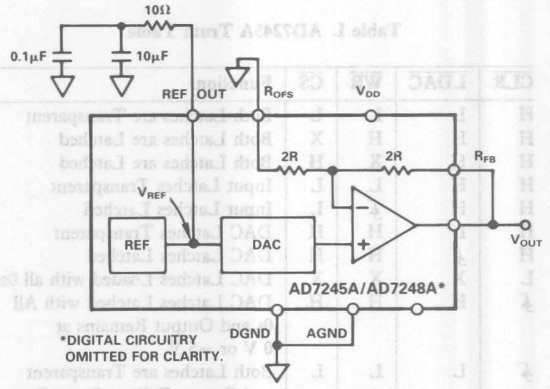


Figure 8. Unipolar (0 to +10 V) Configuration

Table III. Unipolar Code Table (0 V to +10 V Range)

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+2\ V_{REF} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0001	$+2\ V_{REF} \cdot \left(\frac{2049}{4096}\right)$
1000 0000 0000	$+2\ V_{REF} \cdot \left(\frac{2048}{4096}\right) = +V_{REF}$
0111 1111 1111	$+2\ V_{REF} \cdot \left(\frac{2047}{4096}\right)$
0000 0000 0001	$+2\ V_{REF} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

NOTE: $1\ LSB = 2 \cdot V_{REF}(2^{-12}) = V_{REF}\left(\frac{1}{2048}\right)$

UNIPOLAR (0 V TO +5 V) CONFIGURATION

The 0 V to +5 V output voltage range is achieved by tying R_{OFS}, R_{FB} and V_{OUT} together. For this output range the AD7245A/AD7248A can be operated single supply (V_{SS} = 0 V) or dual supply. The table for output voltage versus digital code is as in Table III, with $2 \cdot V_{REF}$ replaced by V_{REF}. Note that for this range

$$1\ LSB = V_{REF}(2^{-12}) = V_{REF} \cdot \frac{1}{4096} \cdot$$

BIPOLAR CONFIGURATION

The bipolar configuration for the AD7245A/AD7248A, which gives an output voltage range from −5 V to +5 V, is achieved by connecting the R_{OFS} input to REF OUT and connecting R_{FB} and V_{OUT}. The AD7245A/AD7248A must be operated from dual supplies to achieve this output voltage range. The code table for bipolar operation is shown in Table IV.

Table IV. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF} \cdot \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{REF} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF} \cdot \left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF} \cdot \left(\frac{2048}{2048}\right) = -V_{REF}$

NOTE: $1\ LSB = 2 \cdot V_{REF}(2^{-11}) = V_{REF}\left(\frac{1}{2048}\right)$

AGND BIAS

The AD7245A/AD7248A AGND pin can be biased above system GND (AD7245A/AD7248A DGND) to provide an offset "zero" analog output voltage level. With unity gain on the amplifier ($R_{OFS} = V_{OUT} = R_{FB}$) the output voltage, V_{OUT} is expressed as:

$$V_{OUT} = V_{BIAS} + D \cdot V_{REF}$$

where D is a fractional representation of the digital word in the DAC latch and V_{BIAS} is the voltage applied to the AD7245A/AD7248A AGND pin.

Because the current flowing out of the AGND pin varies with digital code, the AGND pin should be driven from a low impedance source. A circuit configuration is outlined for AGND bias in Figure 9 using the AD589, a +1.23 V bandgap reference.

If a gain of 2 is used on the buffer amplifier the output voltage, V_{OUT} is expressed as

$$V_{OUT} = 2(V_{BIAS} + D \cdot V_{REF})$$

In this case care must be taken to ensure that the maximum output voltage is not greater than V_{DD} −3 V. The $V_{DD}-V_{OUT}$ overhead must be greater than 3 V to ensure correct operation of the part. Note that V_{DD} and V_{SS} for the AD7245A/AD7248A must be referenced to DGND (system GND). The entire circuit can be operated in single supply with the V_{SS} pin of the AD7245A/AD7248A connected to system GND.

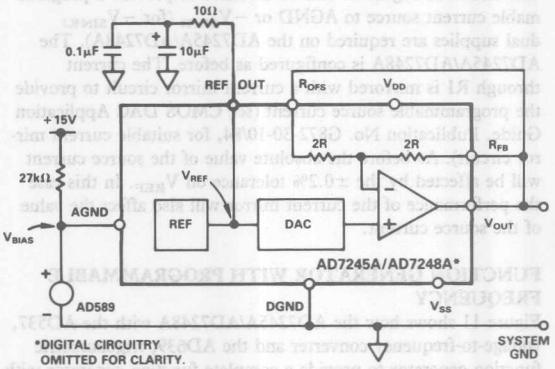


Figure 9. AGND Bias Circuit

PROGRAMMABLE CURRENT SINK

Figure 10 shows how the AD7245A/AD7248A can be configured with a power MOSFET transistor, the VN0300M, to provide a programmable current sink from V_{DD} or V_{SOURCE}. The VN0300M is placed in the feedback of the AD7245A/AD7248A amplifier. The entire circuit can be operated in single supply by tying the V_{SS} of the AD7245A/AD7248A to AGND. The sink current, I_{SINK}, can be expressed as:

$$I_{SINK} = \frac{D \cdot V_{REF}}{R1}$$

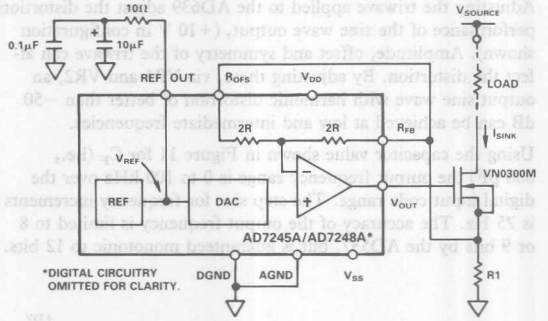


Figure 10. Programmable Current Sink

Using the VN0300M, the voltage drop across the load can typically be as large as V_{SOURCE} −6 V) with V_{OUT} of the DAC at +5 V. Therefore, for a current of 50 mA flowing in the R1 (with all 1s in the DAC register) the maximum load is 200 Ω with V_{SOURCE} = +15 V. The VN0300M can actually handle currents up to 500 mA and still function correctly in the circuit, but in practice the circuit must be used with larger values of V_{SOURCE} otherwise it requires a very small load.

Since the tolerance value on the reference voltage of the AD7245A/AD7248A is ±0.2%, then the absolute value of I_{SINK} can vary by ±0.2% from device to device for a fixed value of R1.

Because the input bias current of the AD7245A/AD7248A's op amp is only of the order of picoamps, its effect on the sink current is negligible. Tying the R_{OFS} input to R_{FB} input reduces this effect even further and prevents noise pickup which could occur if the R_{OFS} pin was left unconnected.

The circuit of Figure 10 can be modified to provide a programmable current source to AGND or $-V_{SINK}$ (for $-V_{SINK}$, dual supplies are required on the AD7245A/AD7248A). The AD7245A/AD7248A is configured as before. The current through R1 is mirrored with a current mirror circuit to provide the programmable source current (see CMOS DAC Application Guide, Publication No. G872-30-10/84, for suitable current mirror circuit). As before the absolute value of the source current will be affected by the ±0.2% tolerance on V_{REF}. In this case the performance of the current mirror will also affect the value of the source current.

FUNCTION GENERATOR WITH PROGRAMMABLE FREQUENCY

Figure 11 shows how the AD7245A/AD7248A with the AD537, voltage-to-frequency converter and the AD639, trigonometric function generator to provide a complete function generator with programmable frequency. The circuit provides square wave, triwave and sine wave outputs, each output of ±10 V amplitude.

The AD7245A/AD7248A provides a programmable voltage to the AD537 input. Since both the AD7245A/AD7248A and AD537 are guaranteed monotonic, the output frequency will always increase with increasing digital code. The AD537 provides a square wave output which is conditioned for ±10 V by amplifier A1. The AD537 also provides a differential triwave output. This is conditioned by amplifiers A2 and A3 to provide the ±1.8 V triwave required at the input of the AD639. The triwave is further scaled by amplifier A4 to provide a ±10 V output.

Adjusting the triwave applied to the AD639 adjust the distortion performance of the sine wave output, (+10 V in configuration shown). Amplitude, offset and symmetry of the triwave can affect the distortion. By adjusting these, via VR1 and VR2, an output sine wave with harmonic distortion of better than −50 dB can be achieved at low and intermediate frequencies.

Using the capacitor value shown in Figure 11 for C_F (i.e., 680 pF) the output frequency range is 0 to 100 kHz over the digital input code range. The step size for frequency increments is 25 Hz. The accuracy of the output frequency is limited to 8 or 9 bits by the AD537, but is guaranteed monotonic to 12 bits.

MICROPROCESSOR INTERFACING—AD7245A

AD7245A—8086A INTERFACE

Figure 12 shows the 8086 16-bit processor interfacing to the AD7245A. In the setup shown the double buffering feature of the DAC is not used and the $\overline{LDAC}$ input is tied LOW. AD0–AD11 of the 16-bit data bus are connected to the AD7245A data bus (DB0–DB11). The 12-bit word is written to the AD7245A in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 12 is given in Table V.

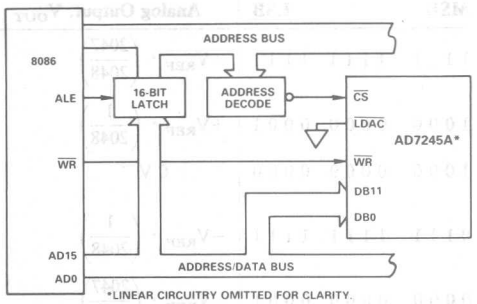


Figure 12. AD7245A to 8086 Interface

Table V. Sample Program for Loading AD7245A from 8086

ASSUME DS : DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CS, CS	: DEFINE DATA SEGMENT REGISTER
02	8ED9	MOV DS, CX	: EQUAL TO CODE SEGMENT REGISTER
04	BF00D0	MOV DI, #D000	: LOAD DI WITH D000
07	C705 "YZWX"	MOV MEM, #YZWX	: DAC LOADED WITH WXYZ
0B	EA00 00		: CONTROL IS RETURNED TO
0E	00 FF		THE MONITOR PROGRAM

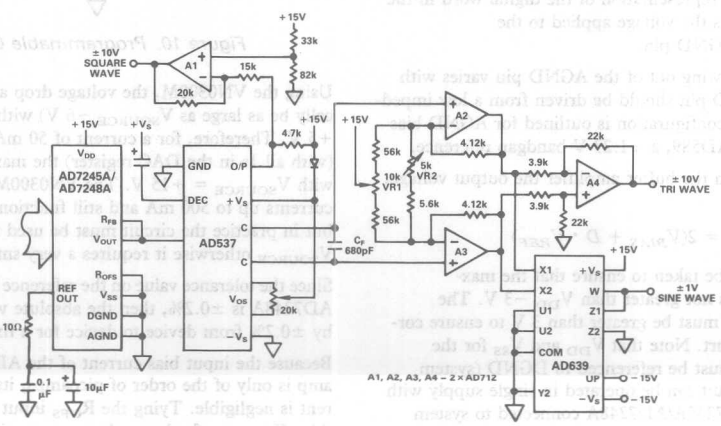


Figure 11. Programmable Function Generator

allows the user to simultaneously update all DACs. In Figure 13, a 12-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought LOW, updating all the DACs simultaneously.

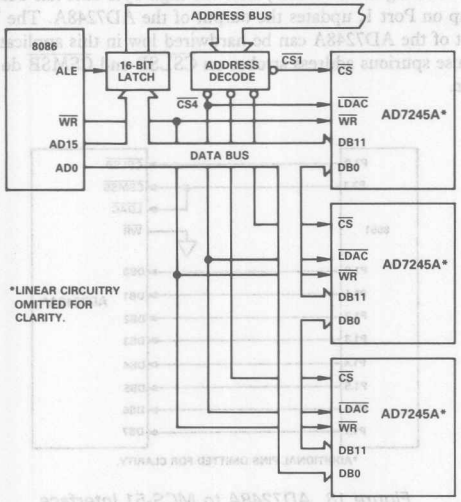


Figure 13. AD7245A to 8086 Multiple DAC Interface

AD7245A—MC68000 INTERFACE

Interfacing between the MC68000 and the AD7245A is accomplished using the circuit of Figure 14. Once again the AD7245A is used in the single buffered mode. A software routine for loading data to the AD7245A is given in Table VI. In this example the AD7245A is located at address E000, and the 12-bit word is written to the DAC in one MOVE instruction.

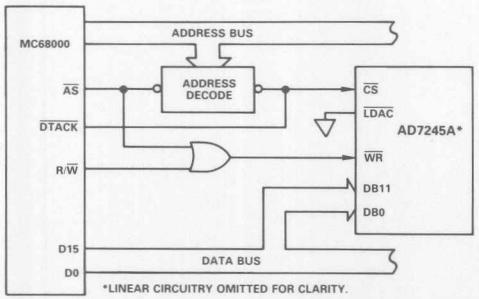


Figure 14. AD7245A to 68000 Interface

01000	MOVE.W	#X,D0	The desired DAC data, X, is loaded into Data Register 0. X may be any value between 0 and 4094 (decimal) or 0 and OFFF (hexadecimal).
	MOVE.W	D0,$E000	The Data X is transferred between D0 and the DAC Latch.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	#14	

MICROPROCESSOR INTERFACE—AD7248A

Figure 15 shows the connection diagram for interfacing the AD7248A to both the 8085A and 8088 microprocessors. This scheme is also suited to the Z80 microprocessor, but the Z80 address/data bus does not have to be demultiplexed. Data to be loaded to the AD7248A is right justified. The AD7248A is memory mapped with a separate memory address for the input latch high byte, the input latch low byte and the DAC latch. Data is first written to the AD7248A input latch in two write operations. Either the high byte or the low byte data can be written first to the AD7248A input latch. A write to the AD7248A DAC latch address transfers the input latch data to the DAC latch and updates the output voltage. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7248As for simultaneous updating of a number of voltage channels.

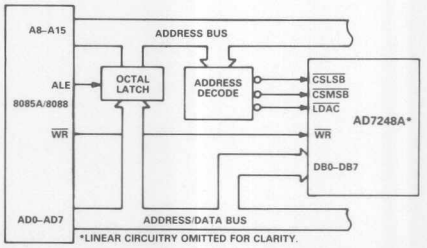


Figure 15. AD7248A to 8085A/8088 Interface

A connection diagram for the interface between the AD7248A and 68008 microprocessor is shown in Figure 16. Once again the AD7248A acts as a memory mapped device and data is right justified. In this case the AD7248A is configured in the automatic transfer mode which means that the high byte of the input latch has the same address as the DAC latch. Data is written to the AD7248A by first writing data to the AD7248A low byte. Writing data to the high byte of the input latch also transfers the input latch contents to the DAC latch and updates the output.

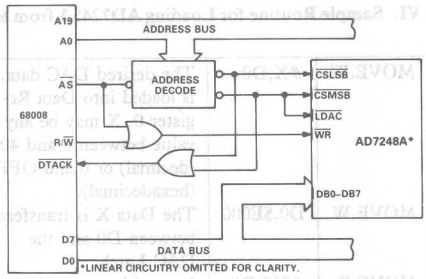


Figure 16. AD7248A to 68008 Interface

An interface circuit for connections to the 6502 or 6809 microprocessors is shown in Figure 17. Once again, the AD7248A is memory mapped and data is right justified. The procedure for writing data to the AD7248A is as outlined for the 8085A/8088. For the 6502 microprocessor the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

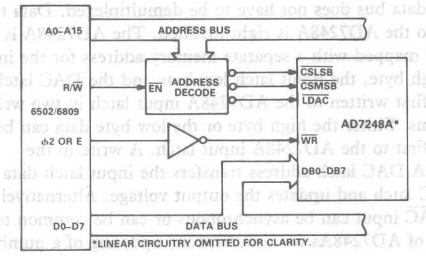


Figure 17. AD7248A to 6502/6809 Interface

Figure 18 shows a connection diagram between the AD7248A and the 8051 microprocessor. The AD7248A is port mapped in this interface and is configured in the automatic transfer mode. Data to be loaded to the input latch low byte is output to Port 1. Output Line P3.0, which is connected to $\overline{CSLSB}$ of the AD7248A, is pulsed to load data into the low byte of the input latch. Pulsing the P3.1 line, after the high byte data has been set up on Port 1, updates the output of the AD7248A. The $\overline{WR}$ input of the AD7248A can be hardwired low in this application because spurious address strobes on $\overline{CSLSB}$ and $\overline{CSMSB}$ do not occur.

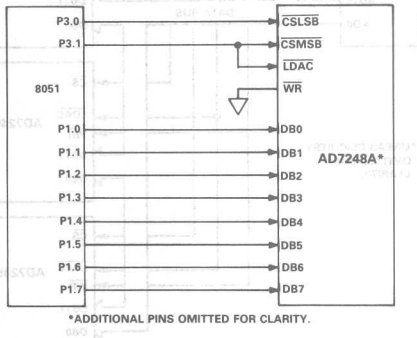


Figure 18. AD7248A to MCS-51 Interface

CMOS 8-Bit Buffered Multiplying DAC

AD7524

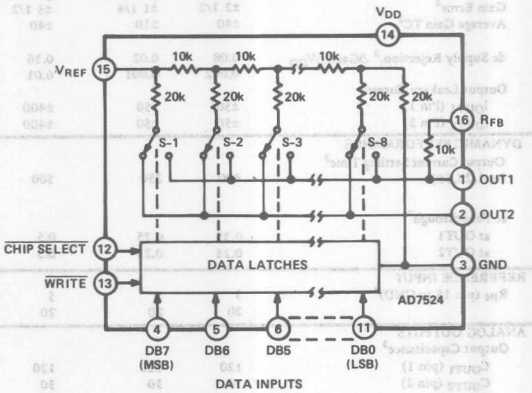
FEATURES

- Microprocessor Compatible (6800, 8085, Z80, etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- End Point Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

ORDERING GUIDE

Model[1]	Temperature Range	Nonlinearity (V_{DD} = +15V)	Package Option[2]
AD7524JN	−40°C to +85°C	±1/2LSB	N-16
AD7524KN	−40°C to +85°C	±1/4LSB	N-16
AD7524LN	−40°C to +85°C	±1/8LSB	N-16
AD7524JP	−40°C to +85°C	±1/2LSB	P-20A
AD7524KP	−40°C to +85°C	±1/4LSB	P-20A
AD7524LP	−40°C to +85°C	±1/8LSB	P-20A
AD7524JR	−40°C to +85°C	±1/2LSB	R-16A
AD7524KR	−40°C to +85°C	±1/4LSB	R-16A
AD7524LR	−40°C to +85°C	±1/8LSB	R-16A
AD7524AQ	−40°C to +85°C	±1/2LSB	Q-16
AD7524BQ	−40°C to +85°C	±1/4LSB	Q-16
AD7524CQ	−40°C to +85°C	±1/8LSB	Q-16
AD7524SQ	−55°C to +125°C	±1/2LSB	Q-16
AD7524TQ	−55°C to +125°C	±1/4LSB	Q-16
AD7524UQ	−55°C to +125°C	±1/8LSB	Q-16
AD7524SE	−55°C to +125°C	±1/2LSB	E-20A
AD7524TE	−55°C to +125°C	±1/4LSB	E-20A
AD7524UE	−55°C to +125°C	±1/8LSB	E-20A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

STATIC PERFORMANCE						
Resolution		8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC measured from +25°C to T_{min} or from +25°C to T_{max}
dc Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} to 0V.
ac Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10V, 100kHz sine wave; DB0–DB7 =
at OUT2	0.25	0.25	0.5	0.5	% FSR max	0V; $\overline{WR}$, $\overline{CS}$ = 0V
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0V
SWITCHING CHARACTERISTICS						See timing diagram. $t_{WR} = t_{CS}$
Chip Select to Write Setup Time[5] t_{CS}						
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width t_{WR}						$t_{CS} \geq t_{WR}, t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	μA max	All Digital Inputs 0V or V_{DD}

NOTES

[1]Temperate ranges as follows: J, K, L versions: −40°C to +85°C
A, B, C versions: −40°C to +85°C
S, T, U versions: −55°C to +125°C

[2]Gain error is measured using internal feedback resistor. Full Scale Range (FRS) = V_{REF}.

[3]Guaranteed, not tested.

[4]DAC thin-film resistor temperature coefficient is approximately −300ppm/°C.

[5]AC parameter, sample tested @ 25°C to ensure conformance to specifications.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
V_{RFB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage to GND	−0.3V to V_{DD} +0.3V
OUT1, OUT2 to GND	−0.3V to V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commerical (J, K, L)	−40°C to +85°C
Industrial (A, B, C)	−40°C to +85°C
Extended (S, T, U)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

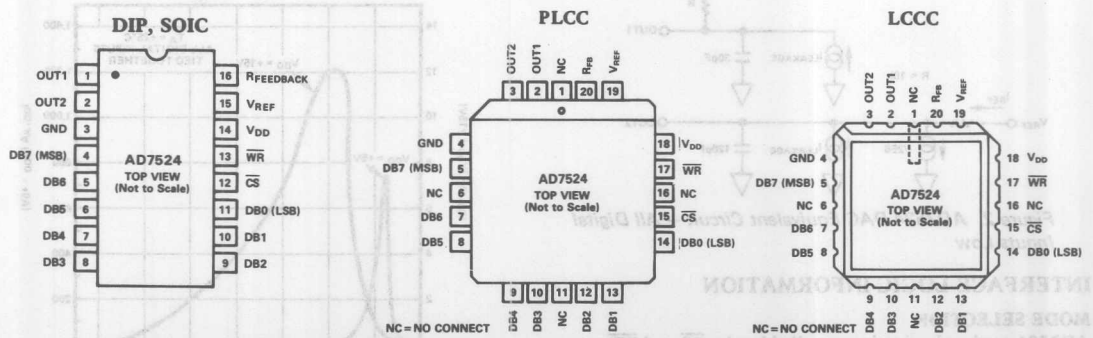
GAIN ERROR: Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in LSBs. Gain Error is adjustable to zero with an external potentiometer.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

PIN CONFIGURATIONS



CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

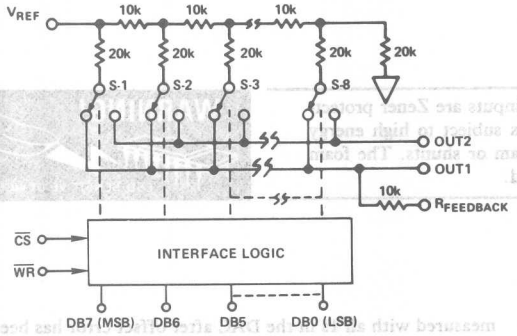


Figure 1. AD7524 Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120pF appears at that terminal.

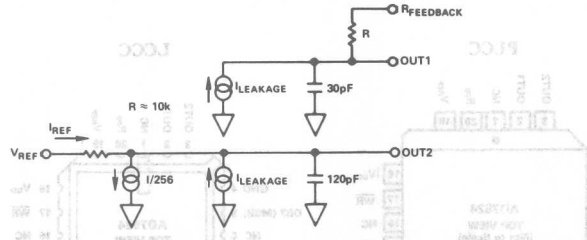


Figure 2. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

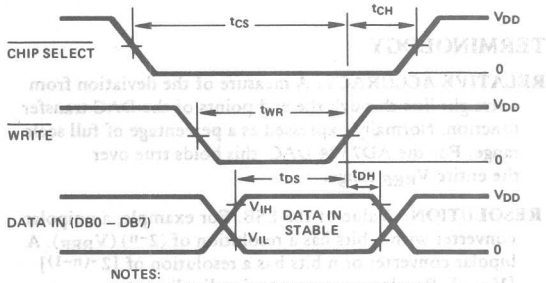
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{wr} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10$ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

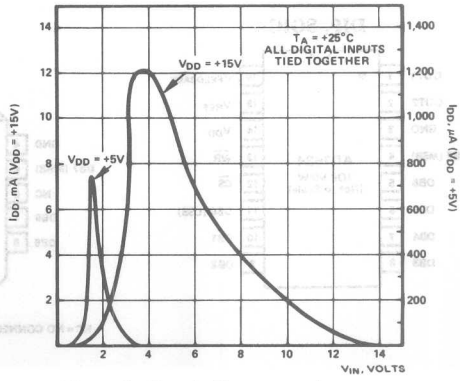


Figure 3. Supply Current vs. Logic Level

Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5V and V_{DD} = +15V are shown above.

ANALOG CIRCUIT CONNECTIONS

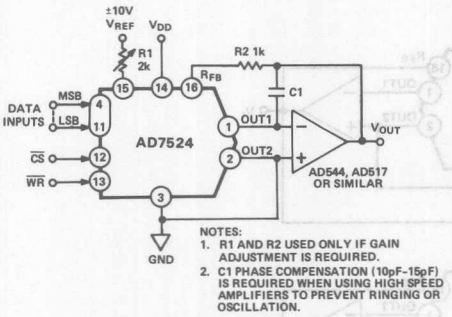


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

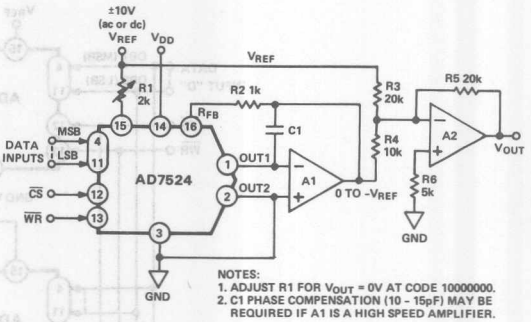


Figure 5. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table I. Unipolar Binary Code Table

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$+V_{REF}\left(\frac{127}{128}\right)$
10000001		$+V_{REF}\left(\frac{1}{128}\right)$
10000000		0
01111111		$-V_{REF}\left(\frac{1}{128}\right)$
00000001		$-V_{REF}\left(\frac{127}{128}\right)$
00000000		$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

Table II. Bipolar (Offset Binary) Code Table

MICROPROCESSOR INTERFACE

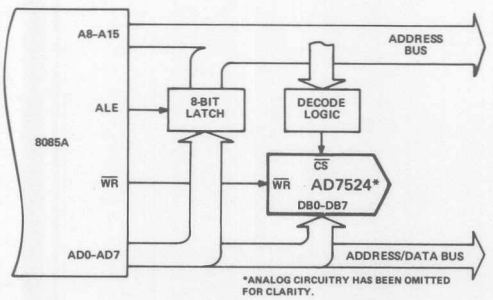


Figure 6. AD7524/8085A Interface

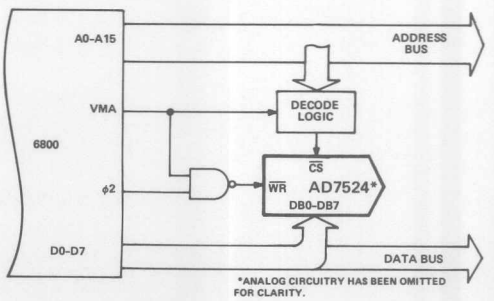
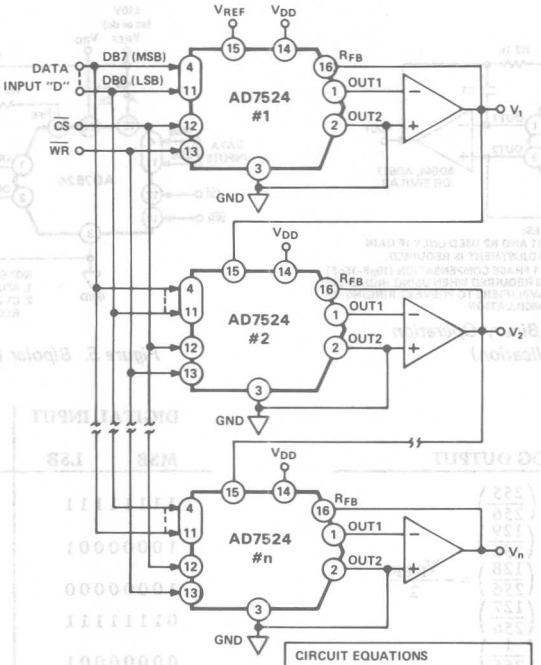


Figure 7. AD7524/MC6800 Interface



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \cdots \frac{DB0}{2^8}$$

and

$DB_n = 1$ or 0

FEATURES

- ±1/8 LSB Maximum Nonlinearity Over Temperature
- ±0.002 LSB Maximum Zero-Scale Error (I_{LKG} 10nA)
- ±1 LSB Maximum Gain Error Over Temperature
- Microprocessor Compatible
- Improved Resistance to ESD
- Latch-up Resistant; No Schottky Diodes Required
- 5mW @ +5V Maximum Power Consumption
- Available in Die Form

APPLICATIONS

- Microprocessor Controlled Circuits
- Precision AGC Circuits
- Bus Structured Instruments
- Function Generators
- Digitally Controlled Attenuators and Power Supplies

ORDERING INFORMATION †

NON-LINEARITY V_{DD} = +15V	GAIN ERROR	PACKAGE MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE COMMERCIAL TEMPERATURE 0°C to +70°C
±1/8 LSB	±1 LSB	PM7524AQ	PM7524EQ	PM7524GP
±1/4 LSB	±1.5 LSB	PM7524BQ	PM7524FQ	–
±1/4 LSB	±1.5 LSB	PM7524BRC/883	PM7524FPC	–
±1/4 LSB	±1.5 LSB	–	PM7524FS	–
±1/4 LSB	±1.5 LSB	–	PM7524FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-7524 is an 8-bit monolithic multiplying digital-to-analog converter with input latches. It is compatible with all popular 8-bit microprocessors including the 6800, 8080, 8085, and Z80. Its load cycle is similar to that of a RAM's write cycle.

PMI's tightly controlled thin-film resistor processing provides 1/8 LSB linearity without laser trimming. The design incorporates a matching MOS transistor switch in series with the R-2R ladder terminating resistor and output op amp's feedback resistor. This allows the DAC to achieve an excellent gain tempco and improved power supply rejection.

The PM-7524 exhibits excellent performance on a single +5V to +15V power supply. It is TTL compatible at +5V and dissipates less than 50mW; using 0V or V_{DD} at the digital inputs, the device dissipates less than 50μW at +5V and 150μW at +15V. At +15V it is CMOS compatible.

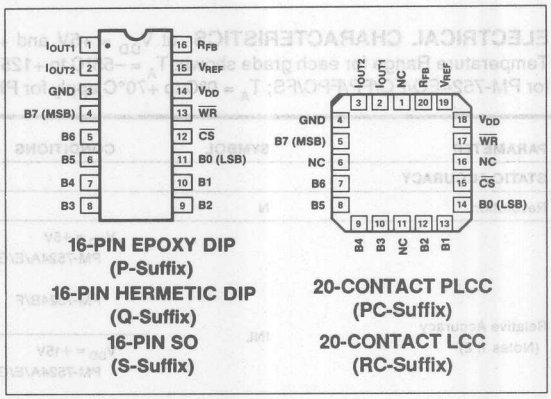
PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

The PM-7524 is manufactured using thin-film resistors on an advanced oxide-isolated silicon-gate CMOS process.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7524AQ	AD7524UD	MIL
PM7524BQ	AD7524TD	
PM7524BQ	AD7524SD	
PM7524EQ	AD7524CD	IND
PM7524FQ	AD7524BD	
PM7524FQ	AD7524AD	
PM7524GP	AD7524LN	COM
PM7524FP	AD7524KN	
PM7524FPC	AD7524KP	

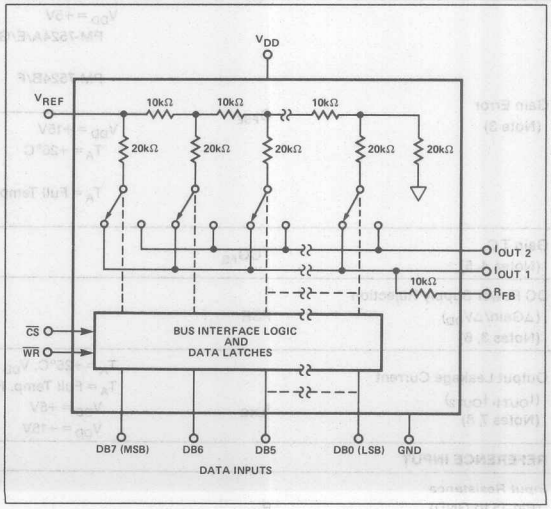
PIN CONNECTIONS



16-PIN EPOXY DIP (P-Suffix)
16-PIN HERMETIC DIP (Q-Suffix)
16-PIN SO (S-Suffix)

20-CONTACT PLCC (PC-Suffix)
20-CONTACT LCC (RC-Suffix)

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) ..... –0.3V, +17V
V_{REF} (to GND) ..... ±25V
R_{FB} (to GND) ..... ±25V
Digital Input Voltage to GND ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}
Operating Temperature Range
Military (AQ, BQ, BRC Versions) ..... –55°C to +125°C
Industrial (EQ, FQ, FP, FPC, FS Versions) . –40°C to +85°C
Commercial (GP Version) ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (TC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = –55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = –40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7524 MIN	PM-7524 TYP	PM-7524 MAX	UNITS
STATIC ACCURACY						
Resolution	N		—	—	8	Bits
Relative Accuracy (Notes 1, 2)	INL	V_{DD} = +5V				
		PM-7524A/E/G	—	—	±0.1	%FSR
			—	—	(±1/4)	(LSB)
		PM-7524B/F	—	—	±0.2	%FSR
			—	—	(±1/2)	(LSB)
		V_{DD} = +15V				
		PM-7524A/E/G	—	—	±0.05	%FSR
			—	—	(±1/8)	(LSB)
		PM-7524B/F	—	—	±0.1	%FSR
			—	—	(±1/4)	(LSB)
Gain Error (Note 3)	G_{FSE}	V_{DD} = +5V				
		PM-7524A/E/G	—	—	±0.4	%FSR
			—	—	(±1)	(LSB)
		PM-7524B/F	—	—	±0.8	%FSR
			—	—	(±2)	(LSB)
		V_{DD} = +15V				
		T_A = +25°C	—	—	±0.4	%FSR
			—	—	(±1)	(LSB)
		T_A = Full Temp. Range	—	—	±0.6	%FSR
			—	—	(±1.5)	(LSB)
Gain T.C. (Notes 4, 5)	TCG_{FS}		—	±0.001	—	%FSR/°C
DC Power Supply Rejection ($\Delta Gain/\Delta V_{DD}$) (Notes 3, 6)	PSR		—	0.002	0.01	%FSR/%
Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 7, 8)	I_{LKG}	T_A = +25°C, V_{DD} = +5V, +15V	—	—	10	
		T_A = Full Temp. Range				
		V_{DD} = +5V	—	—	200	nA
		V_{DD} = +15V	—	—	100	
REFERENCE INPUT						
Input Resistance (Pin 15 to GND) (Note 11)	R_{IN}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = −55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = −40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted. *Continued*

			PM-7524			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY						
Supply Current (Digital Inputs = X)	I_{DD}	X = V_{IL} or V_{IH}	—	—	1	mA
		X = 0V or V_{DD}				
		T_A = 25°C	—	—	10	µA
		T_A = Full Temp. Range	—	—	25	
ANALOG OUTPUTS						
Output Capacitance (Note 4)	C_O	DB0–DB7 = V_{DD} (Note 12)				
		C_{OUT1} (Pin 1)	—	—	120	pF
		C_{OUT2} (Pin 2)	—	—	30	
		DB0–DB7 = 0V (Note 13)				
		C_{OUT1}	—	—	30	pF
		C_{OUT2}	—	—	120	
DIGITAL INPUTS						
Digital Inputs High	V_{IH}	V_{DD} = +5V	+2.4	—	—	V
		V_{DD} = +15V	+13.5	—	—	
Digital Inputs Low	V_{IL}	V_{DD} = +5V	—	—	+0.8	V
		V_{DD} = +15V	—	—	+1.5	
Input Current (V_{IN} = 0V or V_{DD})	I_{IN}	T_A = 25°C	—	—	±1	µA
		T_A = Full Temp. Range	—	—	±10	
Input Capacitance (V_{IN} = 0V) (Note 4)	C_{IN}	DB0–DB7	—	—	5	pF
		$\overline{WR}$, $\overline{CS}$	—	—	20	
SWITCHING CHARACTERISTICS (Notes 4, 14)						
Chip Select to Write Setup Time (t_{WR} = t_{CS}) (Note 14)	t_{CS}	V_{DD} = +5V				
		T_A = +25°C	170	—	—	nA
		T_A = Full Temp. Range				
		PM-7524A/B	240	—	—	
		PM-7524E/F/G	220	—	—	
		V_{DD} = +15V				
		T_A = +25°C	100	—	—	nA
		T_A = Full Temp. Range				
		PM-7524A/B	150	—	—	
		PM-7524E/F/G	130	—	—	
Chip Select to Write Hold Time	t_{CH}		0	—	—	ns
Write Pulse Width ($t_{CH} \geq t_{WR}$, $t_{CH} \geq 0$)	t_{WR}	V_{DD} = +5V				
		T_A = +25°C	150	—	—	ns
		T_A = Full Temp. Range				
		PM-7524A/B	220	—	—	
		PM-7524E/F/G	200	—	—	
		V_{DD} = +15V				
		T_A = +25°C	100	—	—	ns
		T_A = Full Temp. Range				
		PM-7524A/B	150	—	—	
		PM-7524E/F/G	130	—	—	

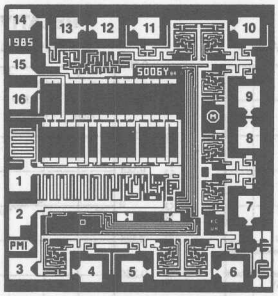
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = –55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = –40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7524 MIN	PM-7524 TYP	PM-7524 MAX	UNITS
		V_{DD} = +5V				
		T_A = +25°V	135	—	—	ns
		T_A = Full Temp. Range	170	—	—	
Data Setup Time	t_{DS}	V_{DD} = +15V				
		T_A = +25°C	60	—	—	
		T_A = Full Temp. Range				ns
		PM-7524A/B	100	—	—	
		PM-7524E/F/G	80	—	—	
Data Hold Time	t_{DH}		10	—	—	ns
DYNAMIC PERFORMANCE						
		V_{DD} = +5V				
		T_A = +25°C	—	—	150	
Propagation Delay		T_A = Full Temp. Range				ns
(From Digital Input		PM-7524A/B	—	—	200	
to 90% of Final	t_{PD}	PM-7524E/F/G	—	—	175	
Analog Output Current)		V_{DD} = +15V				
(Notes 4, 9)		T_A = +25°C	—	—	65	
		T_A = Full Temp. Range				ns
		PM-7524A/B	—	—	90	
		V_{DD} = +5V				
Output Current		T_A = +25°C	—	—	300	
Settling Time		T_A = Full Temp. Range	—	—	350	
(To 1/2 LSB)	t_S	V_{DD} = +15V				ns
(Notes 4, 9, 15)		T_A = +25°C	—	—	200	
		T_A = Full Temp. Range	—	—	250	
AC Feedthrough						
I_{OUT1}, I_{OUT2}	FT		—	—	0.25	%FSR
(Note 4)						
		V_{DD} = +5V				
Digital Charge		T_A = +25°C	—	50	—	
Injection	Q	V_{DD} = +15V				nV/s
(Note 16)		T_A = +25°C	—	55	—	

NOTES:

1. Guaranteed monotonic over full temperature range and at V_{DD} = +5V and +15V.
2. FSR (Full Scale Range) = V_{REF} – 1LSB.
3. Using internal feedback resistor.
4. Guaranteed by design and not production tested.
5. Gain TC measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
6. ΔV_{DD} = ±10%.
7. DB0–DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT1}.
8. DB0–DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT2}.
9. I_{OUT1} load = 100Ω; C_{EXT} = 13pF; $\overline{WR}$ = $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.
10. V_{REF} = ±10V, f = 100kHz; DB0–DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V.
11. Temperature coefficient approximately equals +50ppm/°C.
12. DB0–DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V.
13. DB0–DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V.
14. See Timing Diagram.
15. Extrapolated: t_S (1/2 LSB) = t_{PD} + 6.2τ, where τ = the measured first time constant of the final RC decay.
16. V_{REF} = 0V; Digital Inputs = 0V to V_{DD}.

DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.076 inch, 5320 sq. mils
(1.78 × 1.93 mm, 3.43 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. DB7 (MSB)
5. DB6
6. DB5
7. DB4
8. DB3
9. DB2
10. DB1
11. $\overline{DB0}$ (LSB)
12. $\overline{CS}$
13. $\overline{WR}$
14. V_{DD}
15. V_{REF}
16. R_{FB}

2

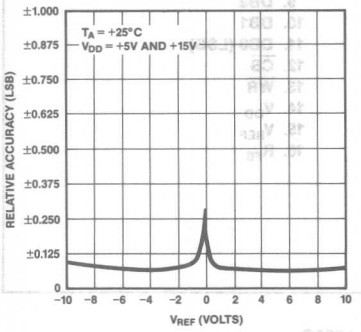
WAFER TEST LIMITS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	PM-7524G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Relative Accuracy (Notes 1, 2)	INL	V_{DD} = +5V	±0.2 (±1/2)	%FSR (LSB) MAX
		V_{DD} = +15V	±0.1 (±1/4)	%FSR (LSB) MAX
Gain Error (Note 3)	G_{FSE}	V_{DD} = +5V	±0.8 (±2)	%FSR (LSB) MAX
		V_{DD} = +15V	±0.4 (±1)	%FSR (LSB) MAX
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$) (Notes 3, 4)	PSRR		0.01	%FSR/% MAX
Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 5, 6)	I_{LKG}		10	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}	(Note 7)	7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Inputs High	V_{IH}	V_{DD} = +5V V_{DD} = +15V	+2.4 +13.5	V MIN
Digital Inputs Low	V_{IL}	V_{DD} = +5V V_{DD} = +15V	+0.8 +1.5	V MAX
Input Current (V_{IN} = 0V or V_{DD})	I_{IN}		±1	μA
POWER SUPPLY				
Supply Current (Digital Inputs = X)	I_{DD}	X = V_{IL} or V_{IH}	1	mA
		X = 0V or V_{DD}	10	μA

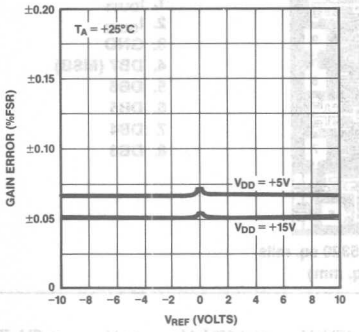
NOTES:
1. Guaranteed monotonic over full temperature range and at V_{DD} = +5V and +15V.
2. FSR (Full Scale Range) = V_{REF} − 1 LSB.
3. Using internal feedback resistor.
4. ΔV_{DD} = ±10%.
5. DB0–DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT1}.
6. DB0–DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT2}.
7. Temperature coefficient approximately equals +50ppm/°C.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

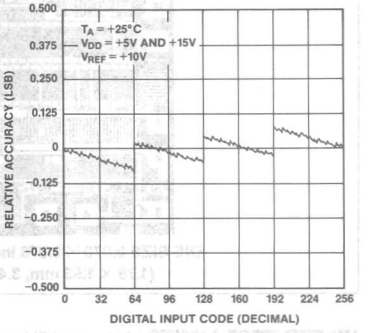
RELATIVE ACCURACY vs REFERENCE VOLTAGE



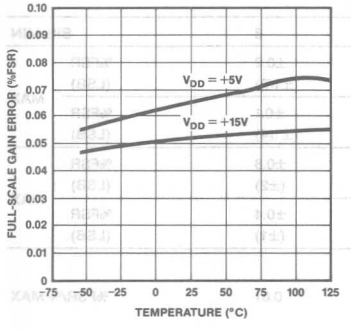
GAIN ERROR vs REFERENCE VOLTAGE



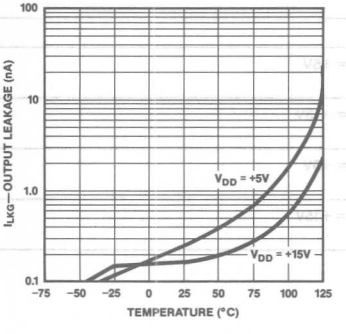
RELATIVE ACCURACY vs DIGITAL INPUT CODE



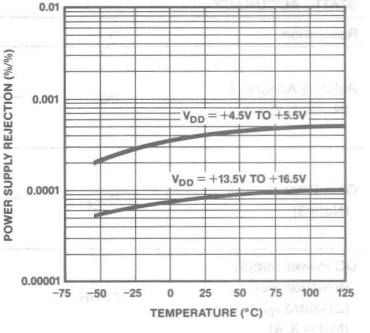
FULL-SCALE GAIN ERROR vs TEMPERATURE



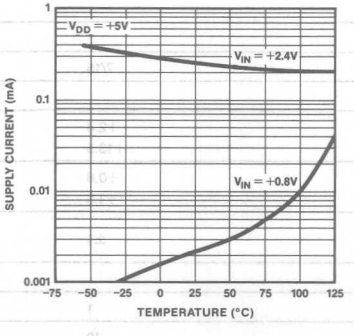
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



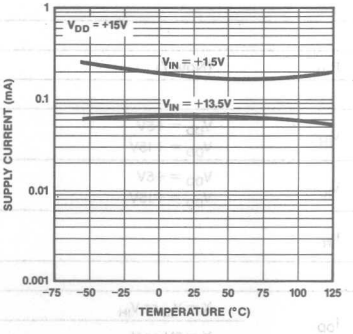
POWER SUPPLY REJECTION vs TEMPERATURE



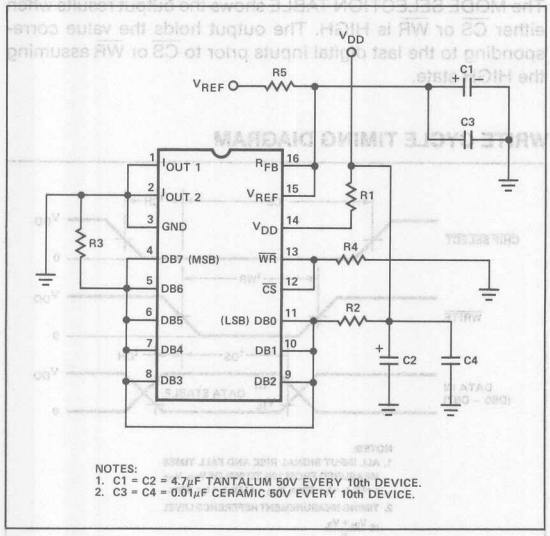
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



BURN-IN CIRCUIT



DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

PROPAGATION DELAY

The time for the output current to reach 90% of its final value from a given digital input signal.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideal output is equal to V_{REF} – 1 LSB.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from $I_{OUT\,1}$ and $I_{OUT\,2}$ terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on $I_{OUT\,1}$ terminal with all digital inputs low or on $I_{OUT\,2}$ terminal when all inputs are high.

CIRCUIT DESCRIPTION

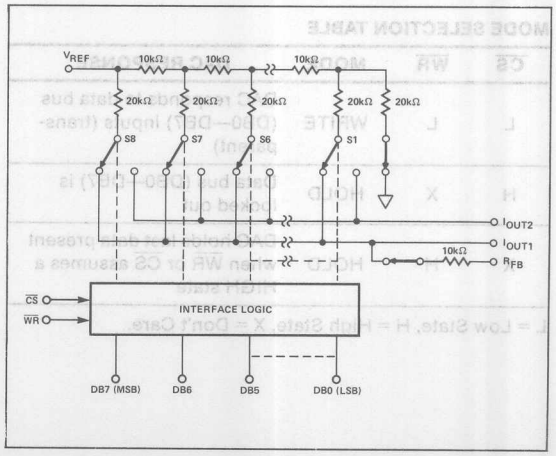
CIRCUIT INFORMATION

The PM-7524 is an 8-bit multiplying CMOS digital-to-analog converter with on-board data latches. It is fabricated using a highly stable thin-film R-2R resistor ladder network and eight N-channel current switches. A voltage or current reference and an operational amplifier are all that is required in the majority of applications.

Figure 1 shows a simplified circuit of the PM-7524 converter. The R-2R ladder, current steering switches, and interface logic are shown. The switches are binarily weighted and switch the ladder current between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines; this switching allows a constant current to be maintained in each resistor leg regardless of the switch state.

The simplified circuit of Figure 1 also shows the matching switches in series with the ladder terminating and R_{FB} (feedback) resistors. These switches are designed to temperature-track the ladder current-steering switches and improve power supply rejection. Both switches are MOS transistors that have their gate turn-on voltage derived from V_{DD} supply. This means the terminating and feedback resistors are open-circuit when V_{DD} power is off. If R_{FB} is used as part of an op amp's feedback element, and the op amp's supply comes on before the DAC, the op amp's output will go to the rails. It remains in this open-loop condition until the DAC's V_{DD} is applied. In applications where the op amp's supply must come on before the DAC, a voltage clamp or external feedback resistor may be necessary.

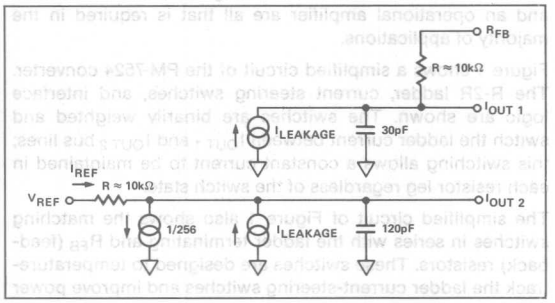
FIGURE 1: PM-7524 Functional Diagram



EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an equivalent circuit for the PM-7524 with all digital inputs LOW. The $I_{OUT\ 1}$ and $I_{OUT\ 2}$ leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder termination resistor. The situation is reversed with all digital inputs HIGH, i.e., the current output is now switched to the $I_{OUT\ 1}$ terminal. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 2: PM-7524 Equivalent Circuit (All Digital Inputs LOW)



INTERFACE LOGIC

MODE SELECTION

The mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

The PM-7524 is in the WRITE mode when both the $\overline{CS}$ and $\overline{WR}$ are both LOW; the input latches are transparent and the output immediately follows the data input logic. See the MODE SELECTION TABLE.

MODE SELECTION TABLE

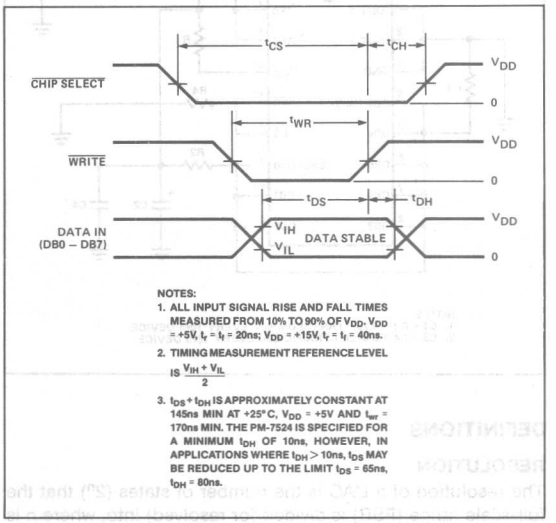
$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0—DB7) inputs (transparent)
H	X	HOLD	Data bus (DB0—DB7) is locked out
X	H	HOLD	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumes a HIGH state

L = Low State, H = High State, X = Don't Care.

HOLD MODE

The MODE SELECTION TABLE shows the output results when either $\overline{CS}$ or $\overline{WR}$ is HIGH. The output holds the value corresponding to the last digital inputs prior to $\overline{CS}$ or $\overline{WR}$ assuming the HIGH state.

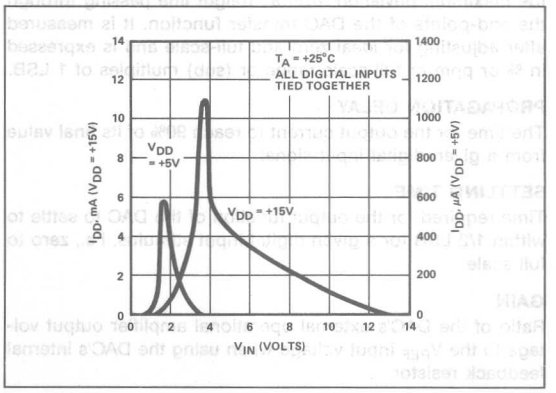
WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ IS APPROXIMATELY CONSTANT AT 145ns MIN AT +25°C, V_{DD} = +5V AND t_{WR} = 170ns MIN. THE PM-7524 IS SPECIFIED FOR A MINIMUM t_{DH} OF 10ns, HOWEVER, IN APPLICATIONS WHERE $t_{DH} > 10$ns, t_{DS} MAY BE REDUCED UP TO THE LIMIT t_{DS} = 65ns, t_{DH} = 80ns.

Supply current (I_{DD}) versus Logic input voltage (V_{IN}) is shown in Figure 3. This plot shows the supply current for both V_{DD} = +5V and V_{DD} = +15V.

FIGURE 3: Supply Current vs Logic Level



APPLICATIONS

FIGURE 4: Unipolar Binary Operation (2-Quadrant Multiplication)

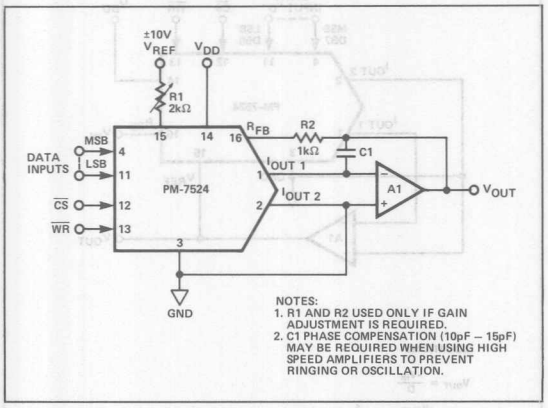


TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTE:

$1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

FIGURE 5: Bipolar (4-Quadrant) Operation

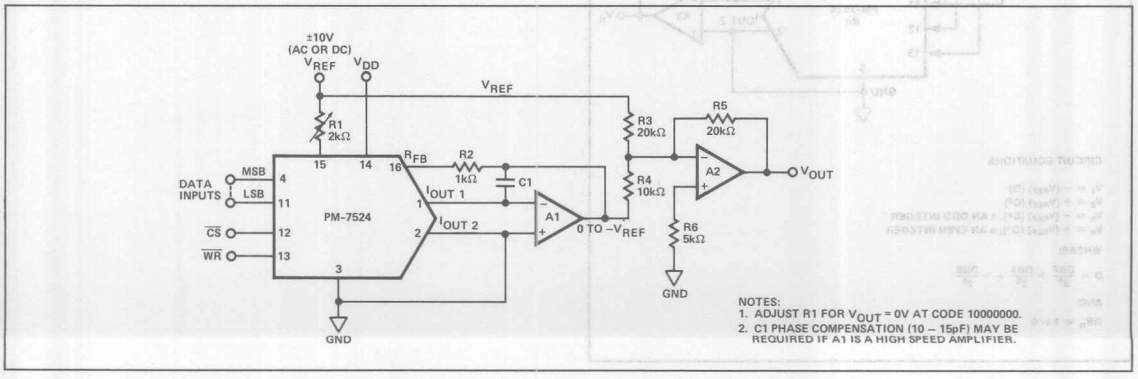


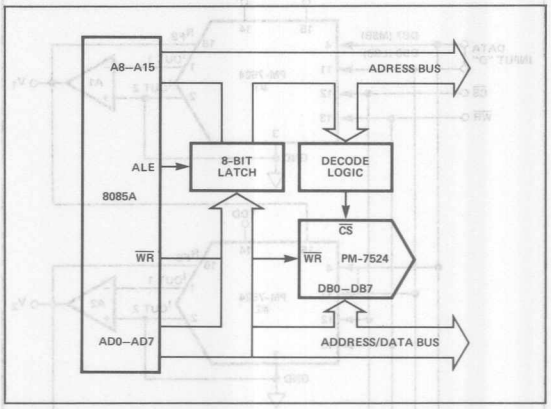
TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

NOTE:

$1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

FIGURE 6: PM-7524/8085A Interface



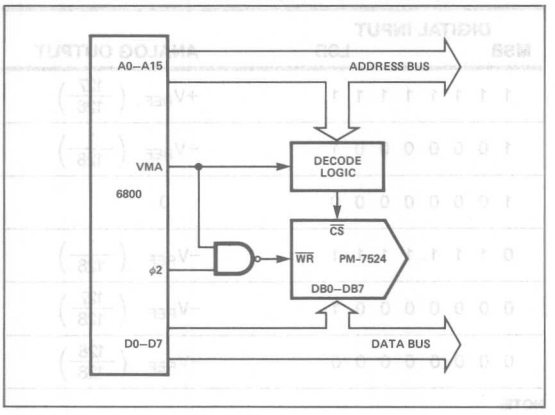
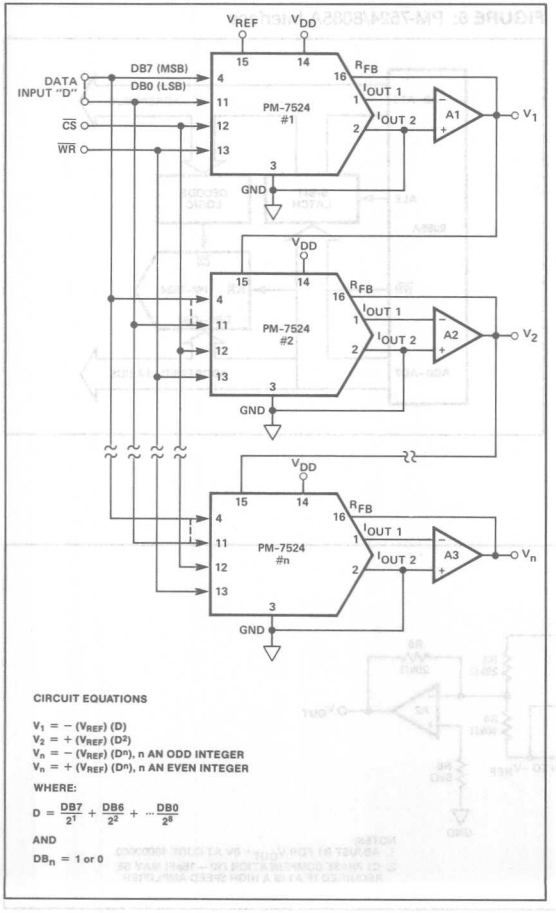


FIGURE 8: Power Generation Connection



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n AN ODD INTEGER
$V_n = +(V_{REF})(D^n)$, n AN EVEN INTEGER

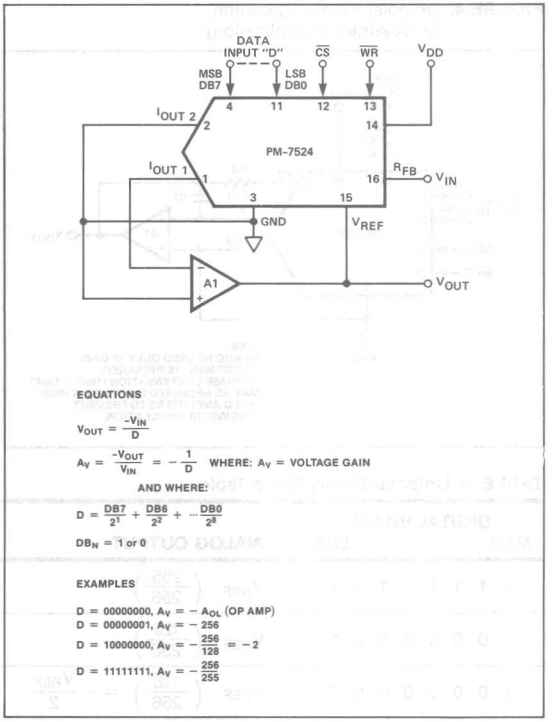
WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

AND

DB_n = 1 or 0

FIGURE 9: Divider (Digitally Controlled Gain)



EQUATIONS

$$V_{OUT} = \frac{-V_{IN}}{D}$$

$$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ WHERE: A_V = VOLTAGE GAIN

AND WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

DB_N = 1 or 0

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$

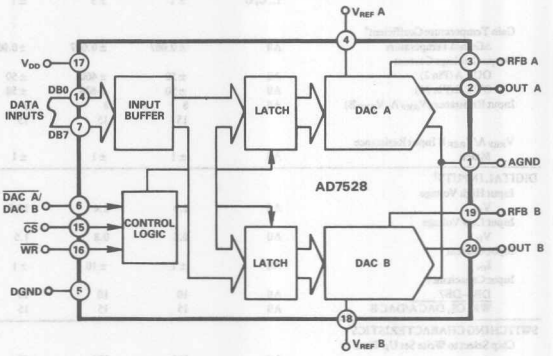
FEATURES

On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- **Gain/Attenuation**
- **Filter Parameters**
- **Stereo Audio Circuits**
- **X–Y Graphics**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3″ wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

AD7528—SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±½	±½	±½	±½	LSB max	
	L, C, U	±½	±½	±½	±½	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are J, K, L Versions: −40°C to +85°C
A, B, C Versions: −40°C to +85°C
S, T, U Versions: −55°C to +125°C
[2]Specification applies to both DACs in AD7528.
[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
[4]Guaranteed by design but not production tested.
[5]These characteristics are for design guidance only and are not subject to test.
[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L) Grades	−40°C to +85°C
Industrial (A, B, C) Grades	−40°C to +85°C
Extended (S, T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	−40°C to +85°C	±1LSB	±4LSB	N-20
AD7528KN	−40°C to +85°C	±1/2LSB	±2LSB	N-20
AD7528LN	−40°C to +85°C	±1/2LSB	±1LSB	N-20
AD7528JP	−40°C to +85°C	±1LSB	±4LSB	P-20A
AD7528KP	−40°C to +85°C	±1/2LSB	±2LSB	P-20A
AD7528LP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7528JR	−40°C to +85°C	±1LSB	±4LSB	R-20
AD7528KR	−40°C to +85°C	±1/2LSB	±2LSB	R-20
AD7528LR	−40°C to +85°C	±1/2LSB	±1LSB	R-20
AD7528AQ	−40°C to +85°C	±1LSB	±4LSB	Q-20
AD7528BQ	−40°C to +85°C	±1/2LSB	±2LSB	Q-20
AD7528CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-20
AD7528SQ	−55°C to +125°C	±1LSB	±4LSB	Q-20
AD7528TQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-20
AD7528UQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-20
AD7528SE	−55°C to +125°C	±1LSB	±4LSB	E-20A
AD7528TE	−55°C to +125°C	±1/2LSB	±2LSB	E-20A
AD7528UE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."
[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal maximum output is V_{REF} − 1LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

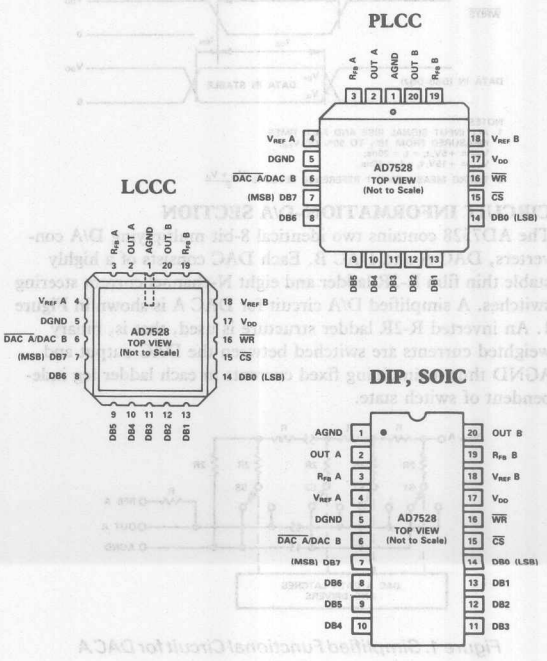
Digital to Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay:
This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS



input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:
Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:
When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

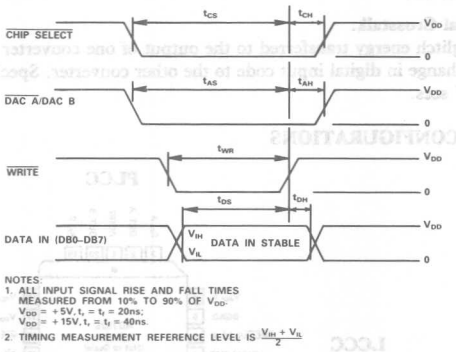
Hold Mode:
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



CIRCUIT INFORMATION–D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

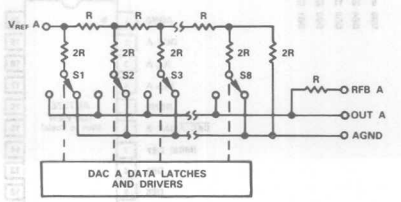


Figure 1. Simplified Functional Circuit for DAC A

AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. $g(V_{REF} A, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

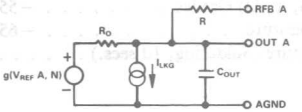


Figure 2. Equivalent Analog Output Circuit of DAC A

For further information on CMOS multiplying D/A converters refer to "Appplication Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

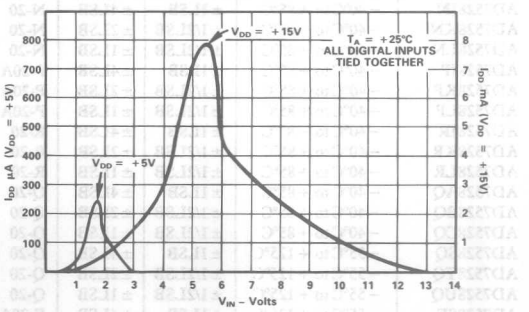
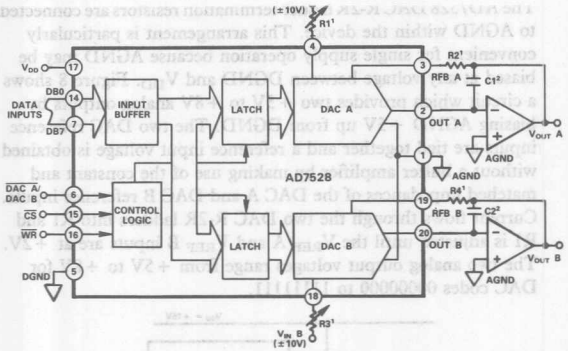
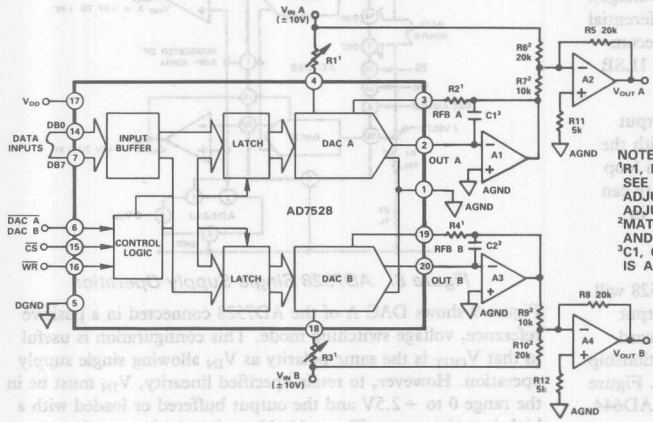


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
[2]C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH.
ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
[3]C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	J/A/S	K/B/T	L/C/U
R1;R3	1k	500	200
R2;R4	330	150	82

Table III. Recommended Trim Resistor Values vs. Grade

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7528. In more complex systems where the AGND–DGND intertie is on the back-plane, it is recommended that diodes be connected in inverse parallel between the AD7528 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7528 and the AD644 dual op-amp which minimizes feedthrough and crosstalk.

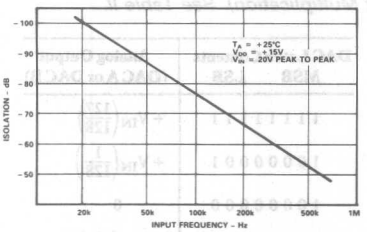


Figure 6. Channel to Channel Isolation

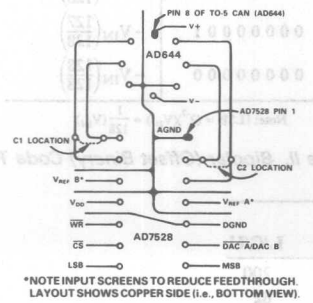


Figure 7. Suggested P.C. Board Layout for AD7528 with AD644 Dual Op-Amp

SINGLE SUPPLY APPLICATIONS

The AD7528 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit which provides two +5V to +8V analog outputs by biasing AGND +5V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2V. The two analog output voltages range from +5V to +8V for DAC codes 00000000 to 11111111.

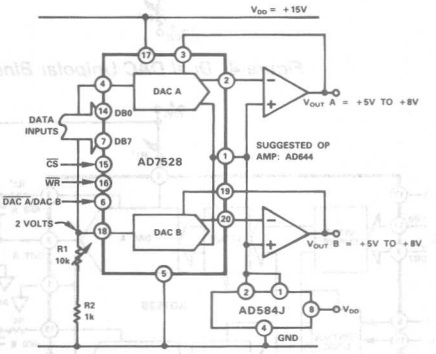


Figure 8. AD7528 Single Supply Operation

Figure 9 shows DAC A of the AD7528 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 to +2.5V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC V_{REF} A pin.

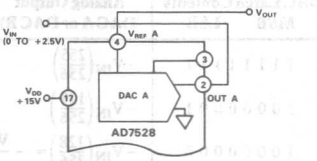


Figure 9. AD7528 in Single Supply, Voltage Switching Mode

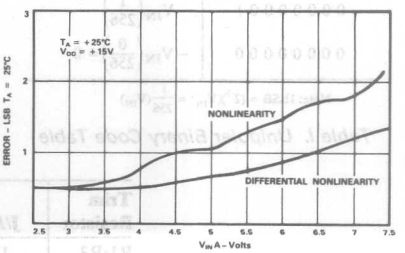


Figure 10. Typical AD7528 Performance in Single Supply Voltage Switching Mode (K/B/T, L/C/U Grades)

MICROPROCESSOR INTERFACE

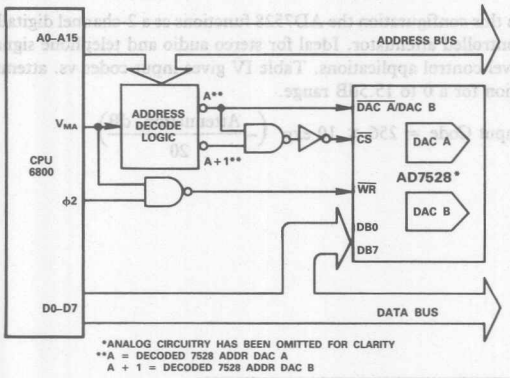


Figure 11. AD7528 Dual DAC to 6800 CPU Interface

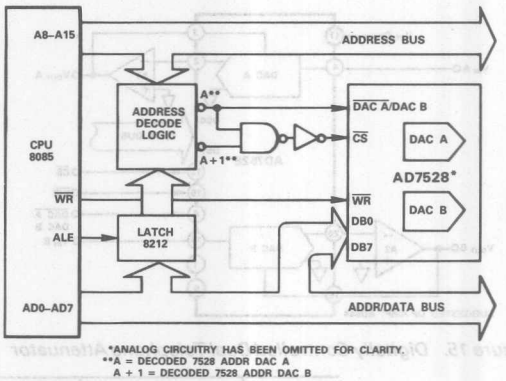


Figure 12. AD7528 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

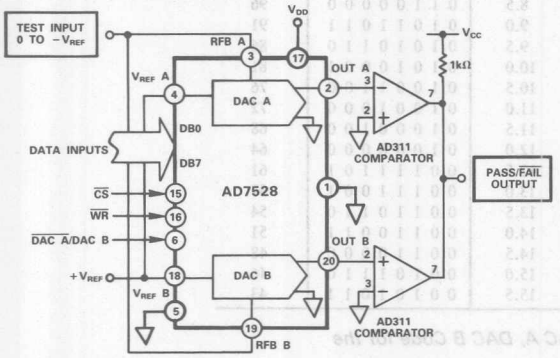


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7528 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

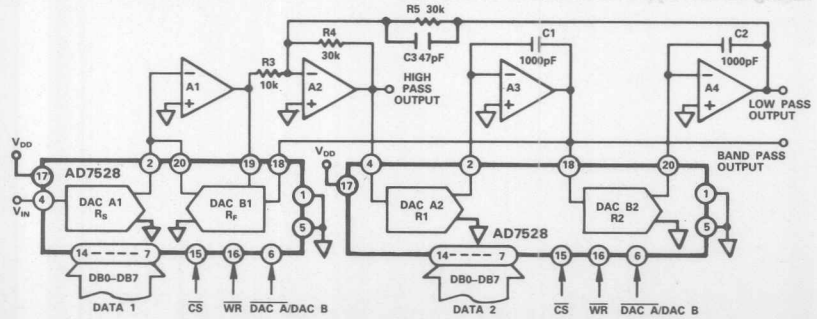


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals
$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is fc = 0 to 15kHz and Q = 0.3 to 4.5.

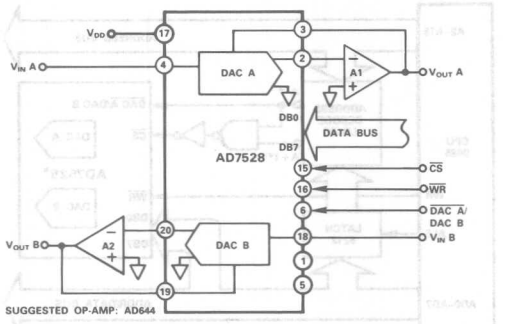


Figure 15. Digitally Controlled Dual Telephone Attenuator

In this configuration the AD7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 to 15.5dB range.

$$\text{Input Code} = 256 \times 10 \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

For futher applications information the reader is referred to Analog Devices Application Note on the AD7528.

Dual 8-Bit Buffered Multiplying CMOS D/A Converter

PM-7528

FEATURES

- On-Chip Latches For Both DACs
- +5V To +15V Single Supply Operation
- DACs Matched To 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible
- 8-Bit Endpoint Linearity (±1/2 LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible
- Improved ESD Resistance
- Automatically Insertable Cerdip and Plastic Packages
- Available in Surface Mount SO, PLCC and LCC Packages
- Available in Die Form

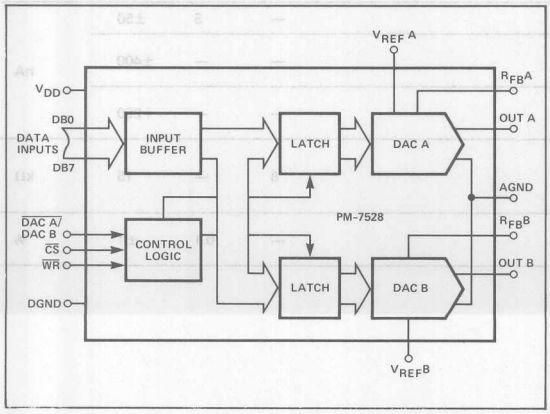
APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control Of Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal For Battery-Operated Equipment

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7528AR	AD7528UD	MIL
PM7528BR	AD7528TD	
PM7528BR	AD7528SD	
PM7528ER	AD7528CQ	IND
PM7528FR	AD7528BQ	
PM7528FR	AD7528AQ	
PM7528GP	PM7528GP	COM
PM7528FP	AD7528LN	
PM7528FPC	AD7528KP	

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

RELATIVE ACCURACY	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE –55°C TO +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C TO +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C TO +70°C
±1/2 LSB	±1 LSB	PM7528AR	PM7528ER	PM7528GP
±1/2 LSB	±1 LSB	PM7528ARC/883	–	–
±1/2 LSB	±2 LSB	PM7528BR	PM7528FR	–
±1/2 LSB	±2 LSB	PM7528BRC/883	PM7528FP	–
±1/2 LSB	±2 LSB	–	PM7528FPC	–
±1/2 LSB	±2 LSB	–	PM7528FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

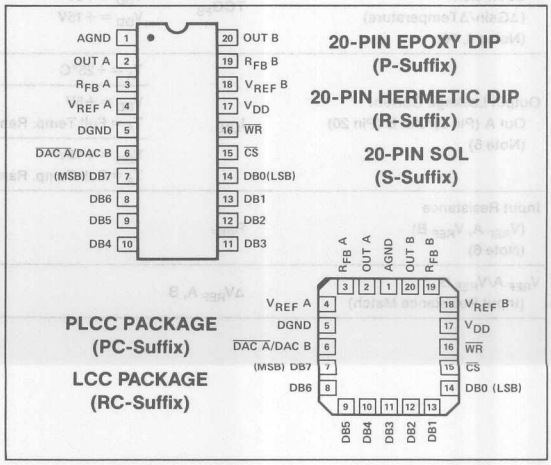
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-7528 contains two 8-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The PM-7528 consists of two thin-film R-2R resistor-ladder networks, tracking span resistors, two data latches, one input buffer, and control logic. Operation from a 5 to 15 volt single power supply dissipates only 20mW of power in a space saving 20-pin 0.3" wide DIP. The PM-7528 features circuitry designed to protect against damage from electrostatic discharges.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line $\overline{\text{DAC A}}$/DAC B. The 8-bit wide input data path provides TTL/CMOS compatibility. The data load cycle is similar to the write cycle of a random access memory. The PM-7528 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS
(T_A=+25°C, unless otherwise noted)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... 0V, V_{DD}
Digital Input Voltage to DGND ..... –0.3V, +15V
$V_{PIN\ 2}$, $V_{PIN\ 20}$ to AGND ..... –0.3V, +15V
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V
Operating Temperature Range
AR, ARC, BR,BRC Versions ..... –55°C to ±125°C
ER, FR, FP, FPC, FS Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	80	15	°C/W
20-Pin Plastic DIP (P)	74	32	°C/W
20-Contact LCC (RC)	76	36	°C/W
20-Pin SO (S)	89	27	°C/W
20-Contact PLCC (PC)	98	38	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS
at V_{DD} = +5V or +15V, $V_{REF}A$ = $V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A= –55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = –40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
STATIC ACCURACY (Note 1)							
Resolution	N			8	—	—	Bits
Relative Accuracy (Note 2)	NL			—	—	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL			—	—	±1	LSB
Full Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C	PM7528A/E/G	—	—	±1	LSB
			PM7528B/F	—	—	±2	
		V_{DD} = +5V, T_A = Full Temp. Range	PM7528A/E/G	—	—	±3	
			PM7528B/F	—	—	±4	
		V_{DD} = +15V, T_A = Full Temp. Range	PM7528A/E/G	—	—	±1	
			PM7528B/F	—	—	±3	
Gain Temperature Coefficient (ΔGain/ΔTemperature) (Notes 4, 10)	TCG_{FS}	V_{DD} = +5V		—	—	±0.007	%/°C
		V_{DD} = +15V		—	—	+0.0035	
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C		—	5	±50	nA
		V_{DD} = +5V, T_A = Full Temp. Range		—	—	±400	
		V_{DD} = +15V, T_A = Full Temp. Range		—	—	+200	
Input Resistance (V_{REF} A, V_{REF} B) (Note 6)	R_{REF}			8	—	15	kΩ
V_{REF} A/V_{REF} B (Input Resistance Match)	ΔV_{REF} A, B			—	0.1	±1	%

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = –55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = –40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}	V_{DD} = +5V	2.4	—	—	V
		V_{DD} = +15V	13.5	—	—	
Digital Input Low (Note 8)	V_{INL}	V_{DD} = +5V	—	—	0.8	V
		V_{DD} = +15V	—	—	1.5	
Input Current (Note 7)	I_{IN}	T_A = +25°C	—	.001	±1	µA
		T_A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 10)	C_{IN}	DB0-DB7	—	—	10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B	—	—	15	
SWITCHING CHARACTERISTICS at V_{DD} = +5V (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	T_A = +25°C	200	—	—	ns
		T_A = Full Temp. Range	230	—	—	
Chip Select to Write Hold Time	t_{CH}	T_A = +25°C	20	—	—	ns
		T_A = Full Temp. Range	30	—	—	
DAC Select to Write Set-Up Time	t_{AS}	T_A = +25°C	200	—	—	ns
		T_A = Full Temp. Range	230	—	—	
DAC Select to Write Hold Time	t_{AH}	T_A = +25°C	20	—	—	ns
		T_A = Full Temp. Range	30	—	—	
Data Valid to Write Set-Up Time	t_{DS}	T_A = +25°C	110	—	—	ns
		T_A = Full Temp. Range	130	—	—	
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	180	—	—	ns
		T_A = Full Temp. Range	200	—	—	
SWITCHING CHARACTERISTICS at V_{DD} = +15V (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	T_A = +25°C	60	—	—	ns
		T_A = Full Temp. Range	80	—	—	
Chip Select to Write Hold Time	t_{CH}	T_A = +25°C	10	—	—	ns
		T_A = Full Temp. Range	15	—	—	
DAC Select to Write Set-Up Time	t_{AS}	T_A = +25°C	60	—	—	ns
		T_A = Full Temp. Range	80	—	—	
DAC Select to Write Hold Time	t_{AH}	T_A = +25°C	10	—	—	ns
		T_A = Full Temp. Range	15	—	—	
Data Valid to Write Set-Up Time	t_{DS}	T_A = +25°C	50	—	—	ns
		T_A = Full Temp. Range	70	—	—	
Data Valid to Write Hold Time	t_{DH}		10	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	60	—	—	ns
		T_A = Full Temp. Range	80	—	—	

PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
POWER SUPPLY (Note 12)						
Supply Current (Note 21)	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	1	mA
		All Digital Inputs 0V or V_{DD}	—	—	100	μA
AC PERFORMANCE CHARACTERISTICS (Note 13)						
DC Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$) (Note 14)	PSRR	$V_{DD} = +5V$ $T_A = +25°C$	—	—	0.02	%/%
		T_A = Full Temp. Range	—	—	0.04	
		$V_{DD} = +15V$ $T_A = +25°C$	—	—	0.01	
		T_A = Full Temp. Range	—	—	0.02	
Propagation Delay (Notes 15, 16, 17)	t_{pD}	$V_{DD} = +5V$ $T_A = +25°C$	—	—	220	ns
		T_A = Full Temp. Range	—	—	270	
		$V_{DD} = +15V$ $T_A = +25°C$	—	—	80	
		T_A = Full Temp. Range	—	—	100	
Current Settling Time (Notes 16, 17, 22)	t_s	$V_{DD} = +5V$ $T_A = +25°C$	—	—	350	ns
		T_A = Full Temp. Range	—	—	400	
		$V_{DD} = +15V$ $T_A = +25°C$	—	—	180	
		T_A = Full Temp. Range	—	—	200	
Digital Charge Injection (Note 18)	Q	$T_A = +25°C$ $V_{DD} = +5V$	—	160	—	nVs
		$V_{DD} = +15V$	—	440	—	
Output Capacitance	C_{OUT} A C_{OUT} B	DAC Latches Loaded with 00000000	— —	— —	50 50	pF
	C_{OUT} A C_{OUT} B	DAC Latches Loaded with 11111111	— —	— —	120 120	
AC Feedthrough (Note 19)	FT_A	V_{REF} A to OUT A; $T_A = +25°C$	—	—	−70	dB
		T_A = Full Temp. Range	—	—	−65	
	FT_B	V_{REF} B to OUT B; $T_A = +25°C$	—	—	−70	
		T_A = Full Temp. Range	—	—	−65	

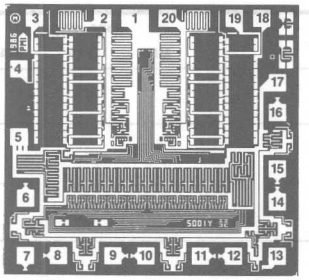
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = –55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = –40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
AC PERFORMANCE CHARACTERISTICS (Note 13)						
Channel-to-Channel Isolation (Note 20)	CCI_{BA}	V_{REF} A to OUT B; V_{REF} A = $20V_{p-p}$ Sinewave @ f = 100kHz V_{REF} B = 0V. T_A = +25°C	—	–77	—	dB
	CCI_{AB}	V_{REF} B to OUT A; V_{REF} B = $20V_{p-p}$ Sinewave @ f = 100kHz V_{REF} A = 0V. T_A = +25°C	—	–77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. T_A = +25°C V_{DD} = +5V	—	30	—	nVs
		V_{DD} = +15V	—	60	—	
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz. T_A = +25°C	—	–85	—	dB

NOTES:

1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All grades guaranteed to be monotonic over the full operating temperature range.
4. Measured using internal R_{FB} A and R_{FB} B. Both DAC latches loaded with 11111111. Gain error is adjustable using circuits of Figures 5 and 6.
5. DAC loaded with 00000000.
6. Input resistance TC = +50ppm/°C; typical input resistance = 11kΩ.
7. V_{IN} = 0V or V_{DD}.
8. For all data bits DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B.
9. Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
10. Guaranteed and not tested.
11. See timing diagram.
12. See Figure 3.
13. These characteristics are for design guidance only and are not subject to test.
14. $\Delta V_{DD} = \pm 5\%$.
15. From digital input to 90% of final analog-output current.
16. V_{REF} A = V_{REF} B = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
17. $\overline{WR}$, $\overline{CS}$ = 0V, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
18. For code transition 00000000 to 11111111.
19. V_{REF} A, V_{REF} B = $20V_{p-p}$ Sinewave @ f = 100kHz.
20. Both DAC latches loaded with 11111111.
21. I_{DD} = 500μA at T_A = Full Temp. Range.
22. Extrapolated: t_s (1/2 LSB) = $t_pD + 6.2\tau$, where τ = the measured first time constant of the final RC decay.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.092 inch, 7,192 sq. mils
(2.184 × 2.337 mm, 5.105 sq. mm)

1. ANALOG GROUND (AGND)
2. OUTPUT A (OUT A)
3. DAC A FEEDBACK RESISTOR ($R_{FB}A$)
4. DAC A REFERENCE INPUT ($V_{REF}A$)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC\ A}$/DAC B)
7. DIGITAL INPUT DB7 (MSB)
8. DIGITAL INPUT DB6
9. DIGITAL INPUT DB5
10. DIGITAL INPUT DB4
11. DIGITAL INPUT DB3
12. DIGITAL INPUT DB2
13. DIGITAL INPUT DB1
14. DIGITAL INPUT DB0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. DAC B FEEDBACK RESISTOR ($R_{FB}B$)
20. OUTPUT B (OUT B)

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted.

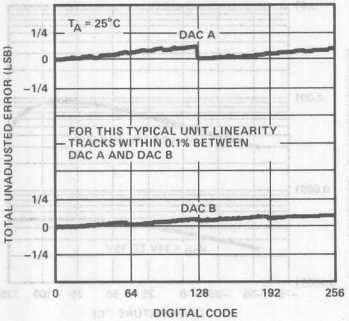
PARAMETER	SYMBOL	CONDITIONS	PM-7528G LIMIT	UNITS
Relative Accuracy	NL	Endpoint Linearity Error	±½	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 11111111	±2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 00000000 Pad 2 and 20	±50	nA MAX
Input Resistance	R_{REF}	Pad 4 and 18	8/15	KΩMIN/ KΩMAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\Delta V_{REF}A, B$		±1	% MAX
Digital Input High	V_{IH}	V_{DD} = 5V V_{DD} = 15V	2.4 13.5	V_{MIN}
Digital Input Low	V_{IL}	V_{DD} = 5V V_{DD} = 15V	0.8 1.5	V_{MAX}
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	1 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	V_{DD} = ±5%	0.02	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

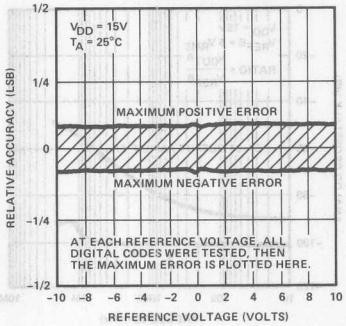
TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted. (Note 13)

PARAMETER	SYMBOL	CONDITIONS	PM-7528G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		6	pF
Output Capacitance	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 00000000	22 22	pF
	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 11111111	40 40	pF
Propagation Delay (Notes 15, 16, 17)	t_{pD}	V_{DD} = 15V V_{DD} = 5V	70 150	ns

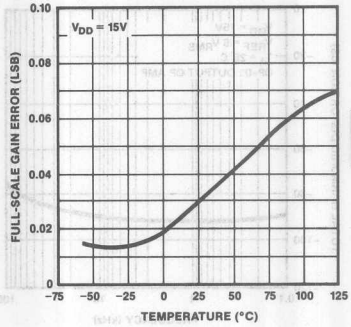
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT



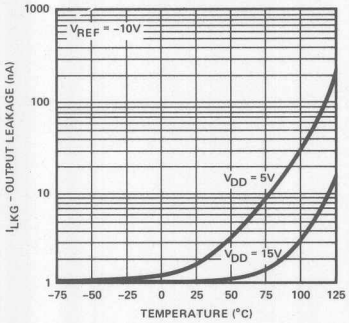
RELATIVE ACCURACY vs REFERENCE VOLTAGE



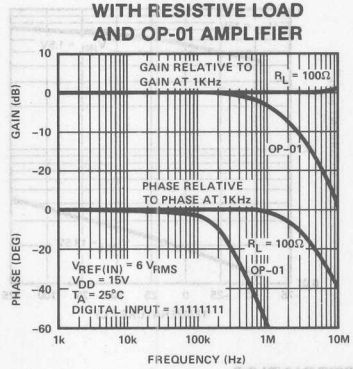
FULL-SCALE GAIN ERROR vs TEMPERATURE



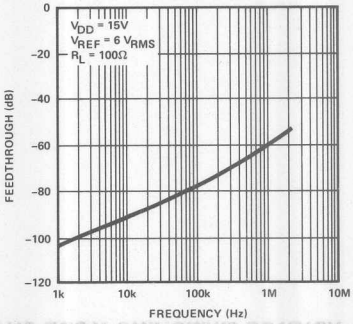
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



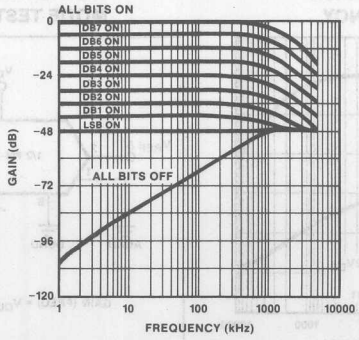
GAIN AND PHASE SHIFT vs FREQUENCY WITH RESISTIVE LOAD AND OP-01 AMPLIFIER



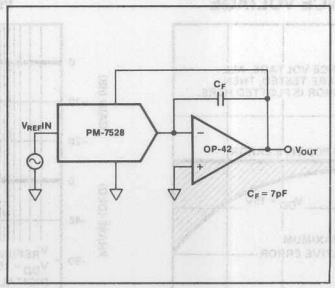
FEEDTHROUGH vs FREQUENCY



GAIN ($V_{OUT}/V_{REF}IN$) vs FREQUENCY

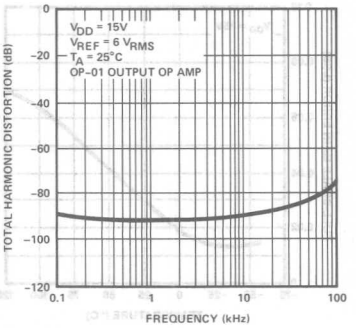


TEST CIRCUIT FOR GAIN vs FREQUENCY

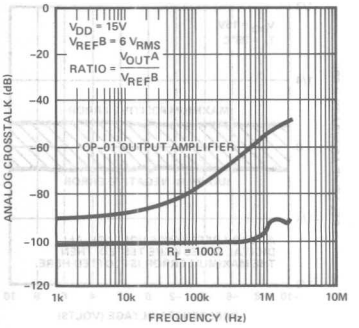


TYPICAL PERFORMANCE CHARACTERISTICS

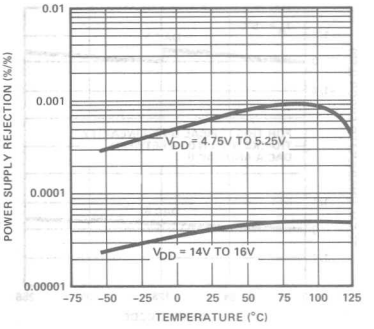
TOTAL HARMONIC DISTORTION vs FREQUENCY



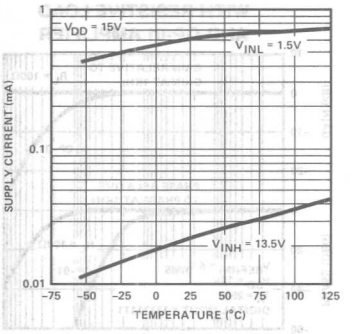
ANALOG CROSSTALK vs FREQUENCY



POWER SUPPLY REJECTION vs TEMPERATURE

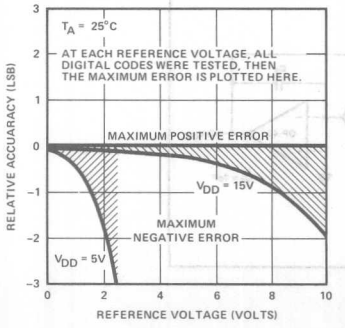


SUPPLY CURRENT vs TEMPERATURE

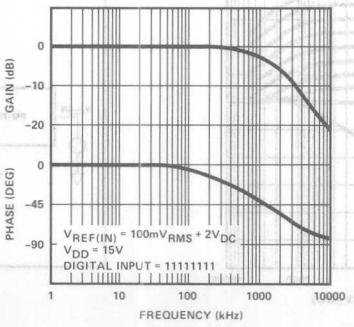


VOLTAGE SWITCHING MODE CHARACTERISTICS

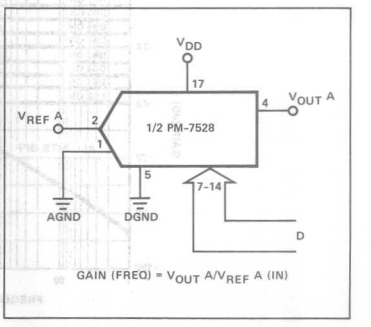
RELATIVE ACCURACY vs REFERENCE VOLTAGE



GAIN AND PHASE vs FREQUENCY



VOLTAGE SWITCHING MODE TEST CIRCUIT



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Relative accuracy, or endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale, and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error, or full-scale error, is a measure of the output error between an ideal DAC and the actual device output. The ideal full-scale output is V_{REF} minus 1 LSB. Gain error of both DAC's in the PM-7528 is adjustable to zero with external resistance.

OUTPUT CAPACITANCE

Capacitance from OUT A or OUT B to AGND.

DIGITAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change states. This is normally specified as the area of the glitch in either pAsecs or nVsecs, depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REF} A, V_{REF} B = AGND.

PROPAGATION DELAY

This is a measure of the internal delays of the circuit. It is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

The portion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK

The glitch energy transferred to the output of one converter, due to a change in digital input code to the other converter, specified in nVsec.

AC FEEDTHROUGH

AC signal due to capacitive coupling from V_{REF} to output with all switches "off."

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

MODE SELECTION

The inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0–DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

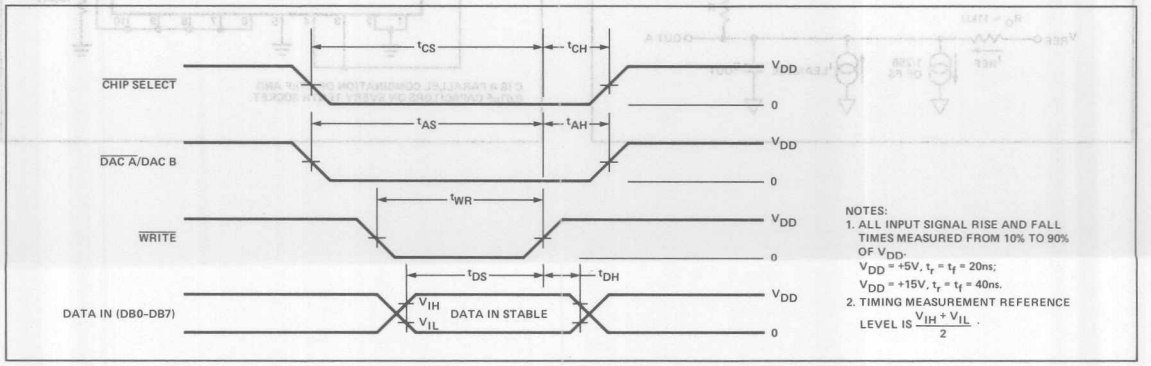
$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

CIRCUIT INFORMATION—D/A SECTION

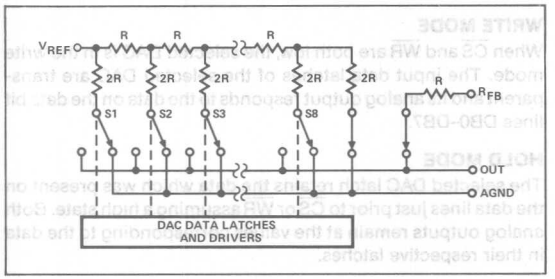
The PM-7528 contains two identical 8-bit multiplying digital-to-analog converters, DAC A and DAC B. Each DAC includes a stable thin-film R-2R resistor ladder and eight NMOS current steering switches. Figure 1 shows a simplified equivalent circuit

WRITE CYCLE TIMING DIAGRAM



of either DAC. The inverted R-2R ladder takes a voltage or current reference and divides it in a binary manner among the eight current steering switches. The number of switches selected to the output (OUT) add their currents together forming an analog output current representation of the switch selection. The DAC OUT and analog ground (AGND) should be maintained at the same voltage for proper operation. The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves linearity performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

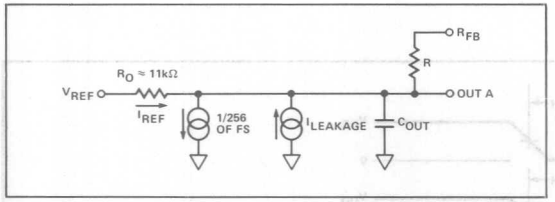
FIGURE 1: Simplified functional circuit for DAC A or DAC B.



EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit of DAC A shown in Figure 2 is similar to DAC B. DAC A and DAC B both share the analog ground pin 1 (AGND). With all digital inputs high, the reference current flows to OUT A. A small leakage current ($I_{LEAKAGE}$) flows across internal junctions, doubling every 10°C. The R-2R ladder termination resistor generates a constant 1/256 current which is 1 LSB of the reference current (I_{REF}). C_{OUT} is the parallel combination of the NMOS current steering switches. The value of C_{OUT} depends on the number of switches connected to the output. The range of C_{OUT} is 50pF to 120pF maximum. The equivalent output resistance R_O varies with input code from 0.8R to 3R, where R is the nominal ladder resistor of the R-2R ladder.

FIGURE 2: PM-7528 DAC A equivalent circuit. All digital inputs high.

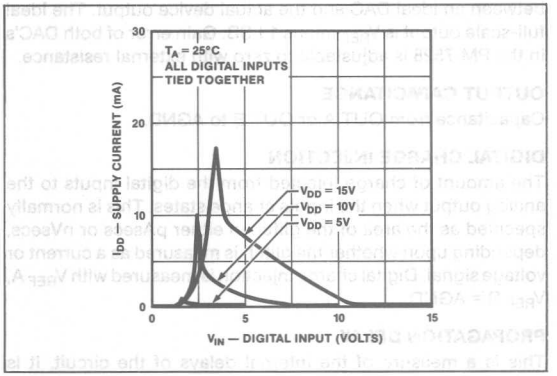


CIRCUIT INFORMATION—DIGITAL SECTION

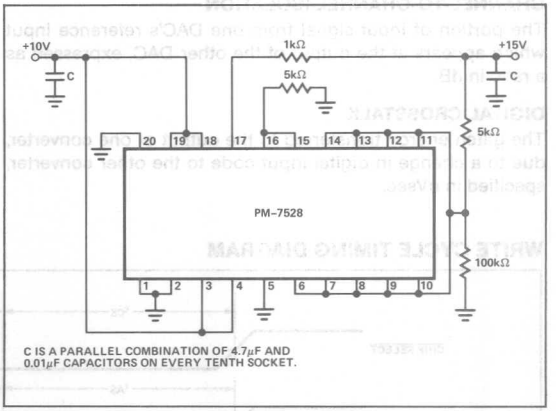
The digital inputs provide TTL input compatibility (V_{INH} = 2.4, V_{INL} = 0.8V) when the PM-7528 operates with V_{DD} of +5V. The digital inputs effect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition voltage. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption. When operating the PM-7528 from CMOS logic the digital inputs are driven very close to the supply rails, minimizing power consumption.

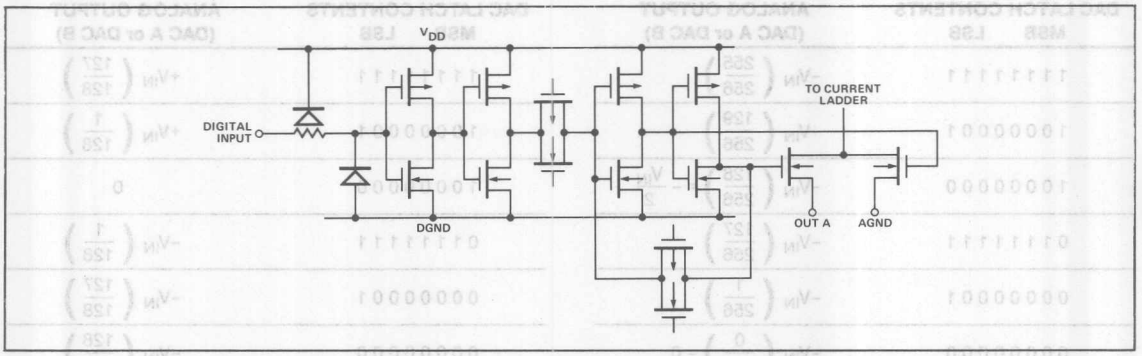
Digital input protection from electrostatic discharge and electrostatic buildup occurs in the input network shown in Figure 4.

FIGURE 3: Typical plots of supply current, I_{DD} vs logic input voltage (V_{IN}), for V_{DD} = +5V, +10V, and +15V.



BURN-IN CIRCUIT





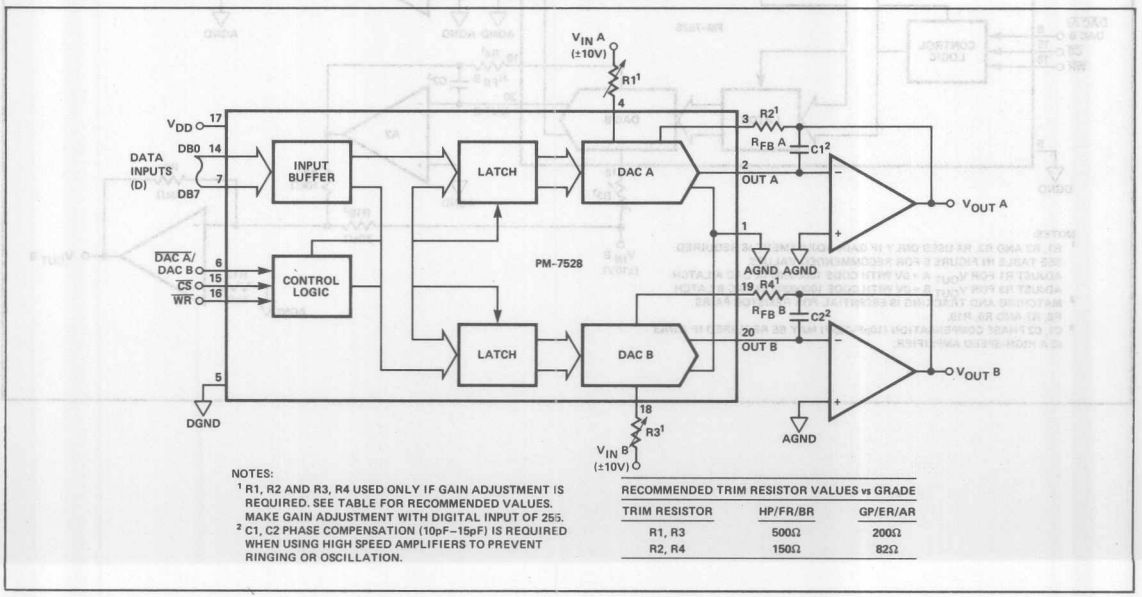
2

APPLICATIONS INFORMATION

The most common application of this DAC is voltage output operation. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 5. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB0 thru DB7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of ±25 volts for both DC or AC signals. The circuit in Figure 5 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation connect the PM-7528 as shown in Figure 6. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB0 thru DB7. This circuit provides full four-quadrant multiplication able to accept both polarities on all inputs as well as the circuit output.

FIGURE 5: Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.



NOTES:
[1] R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE FOR RECOMMENDED VALUES. MAKE GAIN ADJUSTMENT WITH DIGITAL INPUT OF 255.
[2] C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

RECOMMENDED TRIM RESISTOR VALUES vs GRADE

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

TABLE 1: Unipolar Binary Code Table. See Figure 5.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{0}{256}\right) = 0$

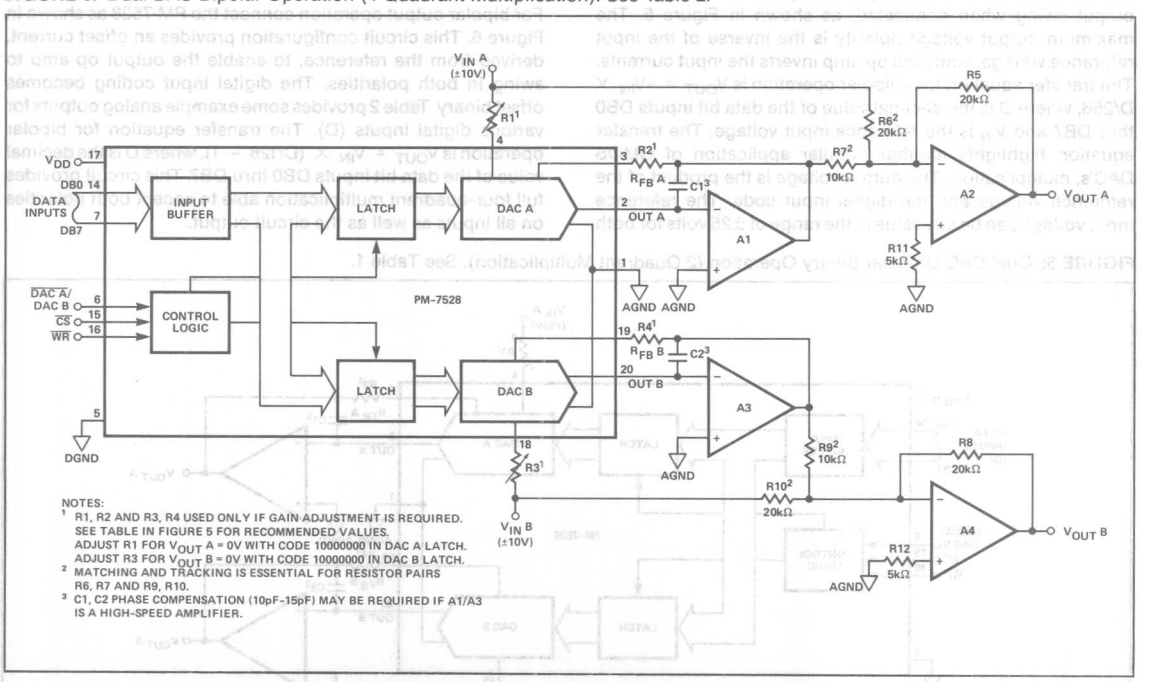
NOTE: 1 LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

TABLE 2: Bipolar (Offset Binary) Code Table. See Figure 6.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

FIGURE 6: Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.



APPLICATION HINTS

To ensure system performance consistent with PM-7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the PM-7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7528. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes (1N914 or equivalent) be connected in inverse parallel between the PM-7528 AGND and DGND pins.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of 0.67 V_{OS} (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH-FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a phase-compensation capacitor in parallel with the feedback resistor.
4. DYNAMIC PERFORMANCE: The dynamic performance of the two DACs in the PM-7528 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
5. CIRCUIT LAYOUT SUGGESTIONS: Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1μF) is recommended across V_{DD} to DGND.

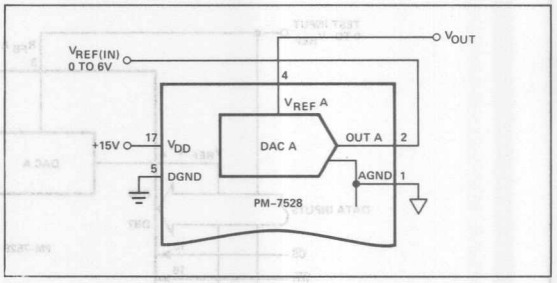
SINGLE SUPPLY OPERATION, VOLTAGE SWITCHING

With the PM-7528 connected in the voltage switching mode of operation, Figure 7, only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, linearity error versus input reference voltage, shows that to maintain a $\pm 1/2$ LSB maximum linearity error, V_{REF} should be less than 1.5 volts for $V_{DD} = 5$ volts or less than 6 volts for $V_{DD} = 15$ volts. The gain-phase response graph shows a dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when $V_{DD} = 5$ volts. Additionally settling time measures 400 to 500 nano seconds for a digital input change of 255 to 0 when $V_{DD} = 5V$.

The output terminal in the voltage switching mode has a constant output resistance (≈ 11K Ω) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.

FIGURE 7: PM-7528 in Single Supply, Voltage Switching Mode



SINGLE SUPPLY, CURRENT SWITCHING

An alternate single-supply operating mode of the PM-7528 results when offsetting the analog ground. Figure 8 shows the method of connection. The advantage of this connection method is the ability to set the output voltage swing in the center of the supply voltage. This allows use of lower cost op amps that would not work in single-supply voltage-switching applications.

The transfer equation in this mode of operation is;

$V_{OUT}(D) = D/256\ (AGND - V_{REF}) + AGND$

where D is the whole number binary input

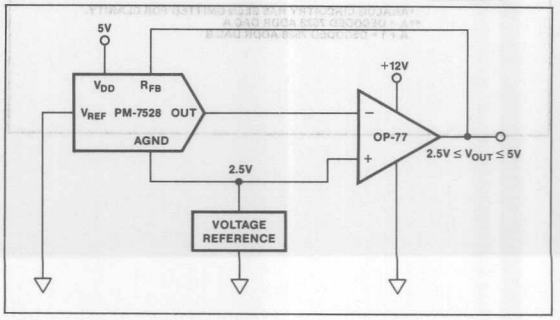
A popular connection in the current-steering single-supply mode consists of a 2.5 volt reference connected to AGND, the V_{REF} input grounded, V_{DD} connected to 5 volts and the external (V+) op amp tied to 12 volts. This hookup results in the following transfer equation;

$V_{OUT}(D) = 2.5\ (1 + D/256)$

where $V_{OUT}\ (255) = 2.5\ (1 + 255/256) = 5V$
$V_{OUT}\ (0) = 2.5V$

To maintain best linearity keep AGND equal to or less than 2.5 volts when V_{DD} is 5 volts.

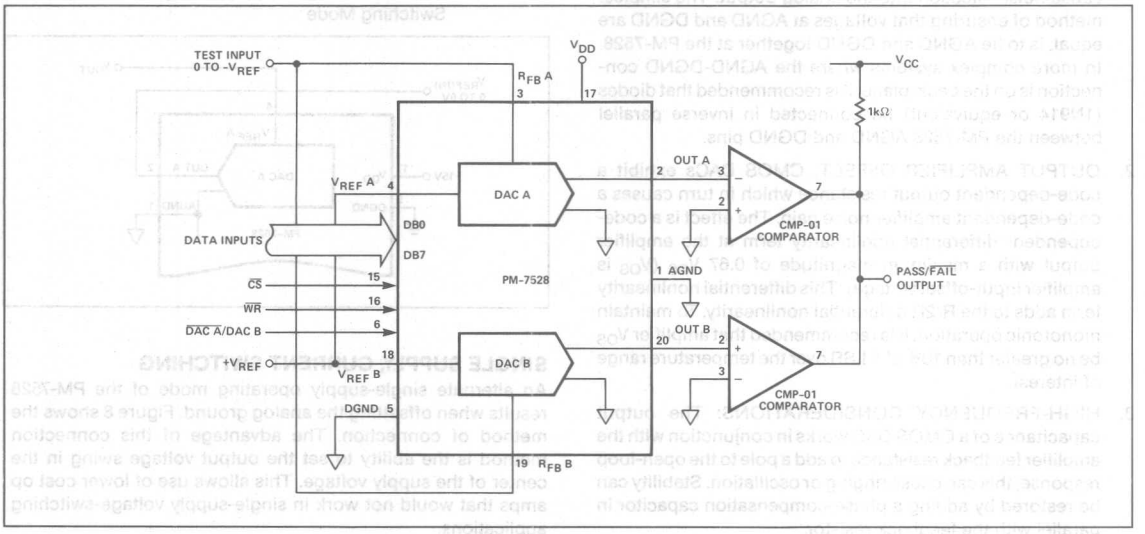
FIGURE 8: PM-7528 in Single Supply, Current-Steering Mode



PROGRAMMABLE WINDOW COMPARATOR

A programmable window-comparator in Figure 9 will determine if voltage inputs applied to the DAC feedback resistors are within limits programmed into the PM-7528 data latches. The input signal range depends on the reference and polarity, that is the test input range is 0 to minus V_{REF}. The A and B data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output to logic high.

FIGURE 9: Digitally Programmable Window Comparator (Upper and Lower Limit Detector).



MICROPROCESSOR INTERFACE

FIGURE 10: PM-7528 Dual DAC to 6800 CPU Interface.

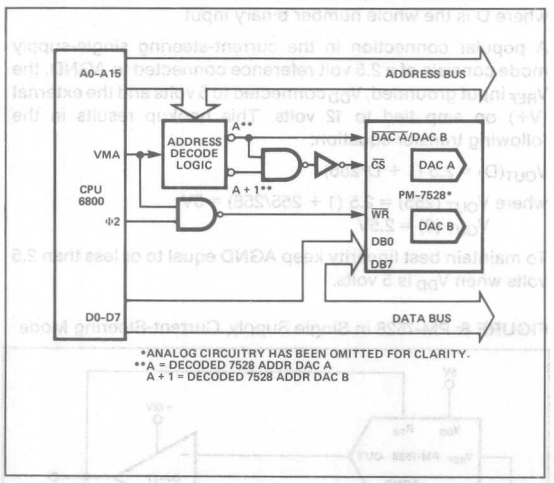
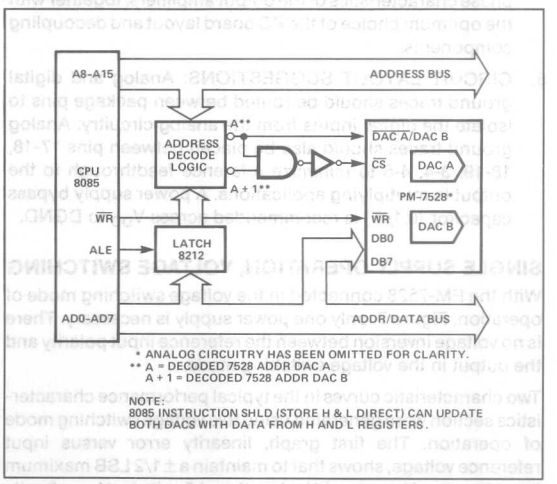


FIGURE 11: PM-7528 Dual DAC to 8085 CPU Interface.



DIGITALLY CONTROLLED SIGNAL ATTENUATOR

Figure 12 shows the PM-7528 configured as a two-channel programmable attenuator. Applications include stereo, audio, and telephone signal-level control applications. In order to generate logarithmic attenuation, Table 4 was generated based on the equation:

$$\text{Digital Input} = 256 \times \exp\left(\frac{-\text{Attenuation (dB)}}{20}\right)$$

FIGURE 12: Digitally-Controlled Dual Telephone Attenuator.

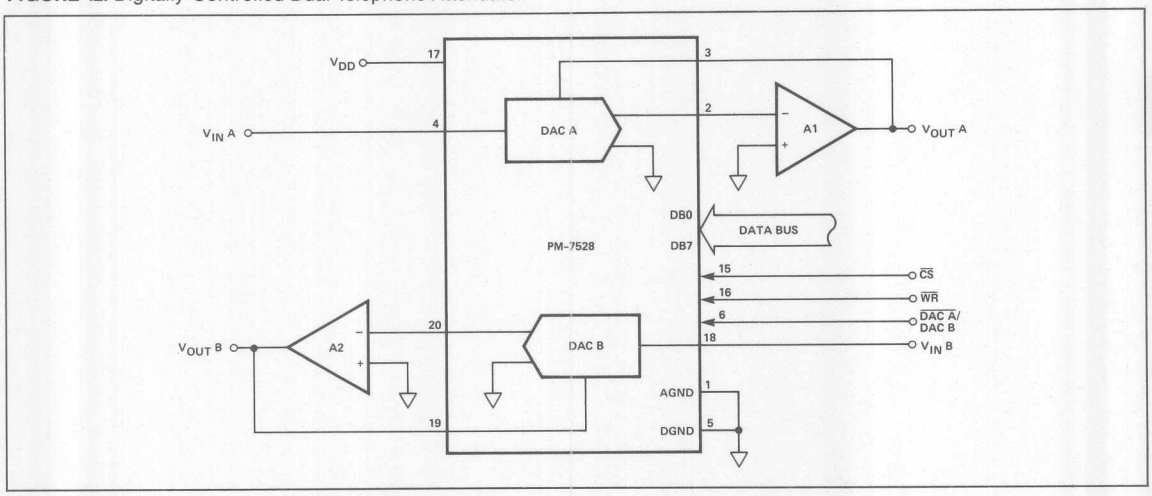


TABLE 4: Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 12

ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL	ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

CMOS Low Cost 10-Bit Multiplying DAC

AD7533

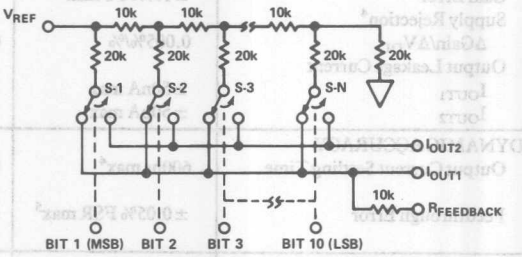
FEATURES

- Lowest Cost 10-Bit DAC
- Low Cost AD7520 Replacement
- Linearity: 1/2, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface
- Latch Free (Protection Schottky Not Required)
- End-Point Linearity

APPLICATIONS

- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Nonlinearity (% FSR max)	Package Option[3]
AD7533JN	−40°C to +85°C	±0.2	N-16
AD7533KN	−40°C to +85°C	±0.1	N-16
AD7533LN	−40°C to +85°C	±0.05	N-16
AD7533JP	−40°C to +85°C	±0.2	P-20A
AD7533KP	−40°C to +85°C	±0.1	P-20A
AD7533LP	−40°C to +85°C	±0.05	P-20A
AD7533JR	−40°C to +85°C	±0.2	R-16
AD7533KR	−40°C to +85°C	±0.1	R-16
AD7533LR	−40°C to +85°C	±0.05	R-16
AD7533AQ	−40°C to +85°C	±0.2	Q-16
AD7533BQ	−40°C to +85°C	±0.1	Q-16
AD7533CQ	−40°C to +85°C	±0.05	Q-16
AD7533SQ	−55°C to +125°C	±0.2	Q-16
AD7533TQ	−55°C to +125°C	±0.1	Q-16
AD7533UQ	−55°C to +125°C	±0.05	Q-16
AD7533SE	−55°C to +125°C	±0.2	E-20A
AD7533TE	−55°C to +125°C	±0.1	E-20A
AD7533UE	−55°C to +125°C	±0.05	E-20A

NOTES

[1]Analog Devices reserves the right to ship ceramic (package outline D-16) packages in lieu of cerdip (package outline Q-16) packages.

[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.

[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7533—SPECIFICATIONS (V_{DD} = +15V, V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

Parameter	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533J, A, S Versions	±0.2% FSR max	±0.2% FSR max	
AD7533K, B, T Versions	±0.1% FSR max	±0.1% FSR max	
AD7533L, C, U Versions	±0.05% FSR max	±0.05% FSR max	
Gain Error[2, 3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1}	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2}	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[4]	800ns[5]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[5]	±0.1% FSR max[5]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sine wave.
REFERENCE INPUT			
Input Resistance (Pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1}	100pF max[5]	100pF max[5]	Digital Inputs = V_{INH}
C_{OUT2}	35pF max[5]	35pF max[5]	
C_{OUT1}	35pF max[5]	35pF max[5]	Digital Inputs = V_{INL}
C_{OUT2}	100pF max[5]	100pF max[5]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	8pF max[5]	8pF max[5]	
POWER REQUIREMENTS			
V_{DD}	+15V ± 10%	+15V ± 10%	Rated Accuracy
V_{DD} Range[5]	+5V to +16V	+5V to +16V	Functionality with Degraded Performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES
[1]"FSR" is Full-Scale Range.
[2]Full Scale (FS) = (V_{REF})
[3]Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[4]AC parameter, sample tested to ensure specification compliance.
[5]Guaranteed, not tested.
[6]Absolute temperature coefficient is approximately −300ppm/°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V to V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L Versions)	−40°C to +85°C
Industrial (A, B, C Versions	−40°C to +85°C
Extended (S, T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution fo $[2^{-(n-1)}]$ (V_{REF}). Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustble to zero with an external potentiometer.

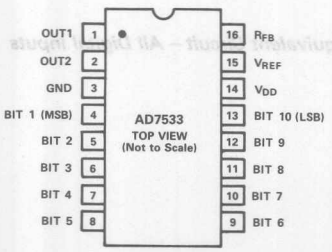
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

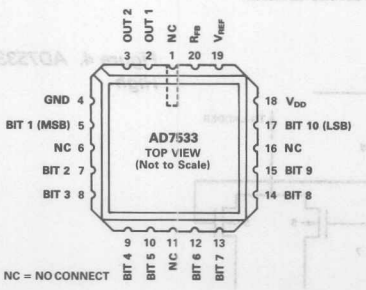
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

PIN CONFIGURATIONS

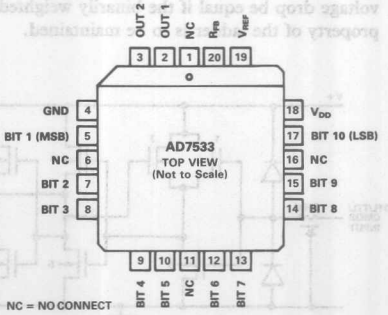
DIP, SOIC



LCCC



PLCC



CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

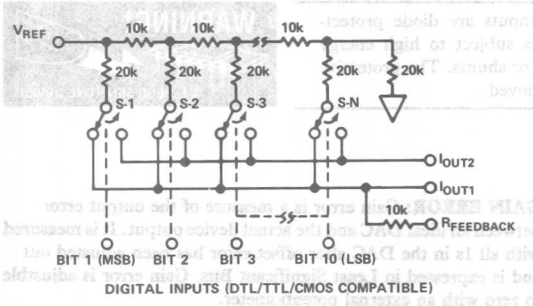


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20Ω, switch 2 for 40Ω, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

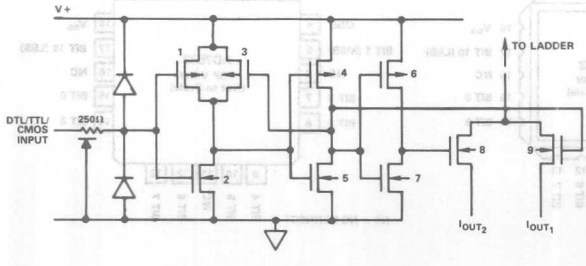


Figure 2. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

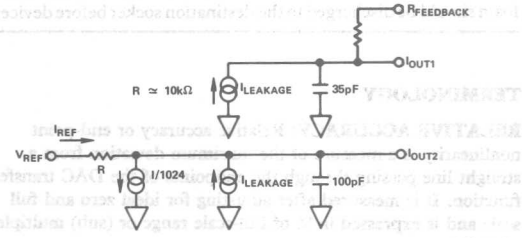


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

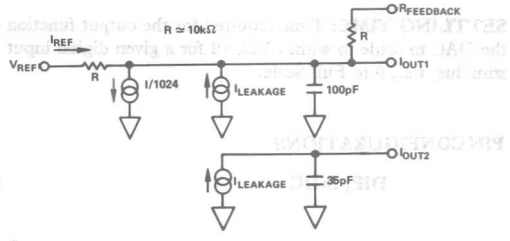


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTE:
1. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

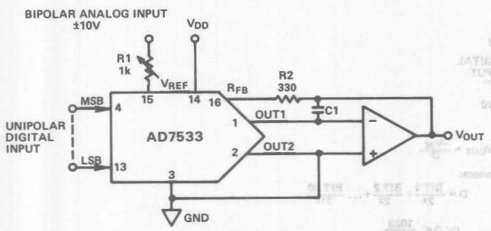
Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

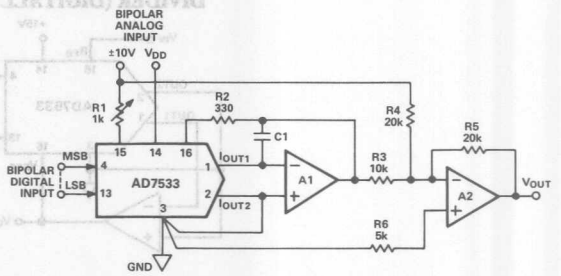
NOTE
1. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

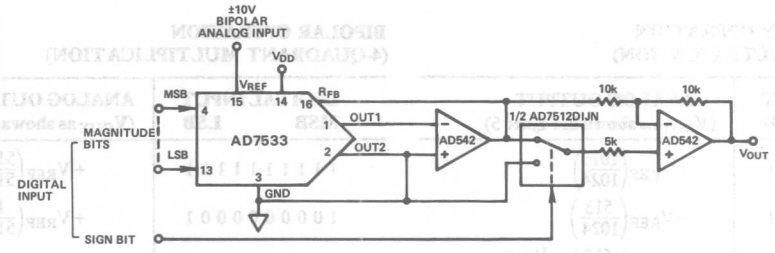


NOTES
1. R3, R4 AND R5 SELECTED FOR MATCHING AND TRACKING.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5-15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

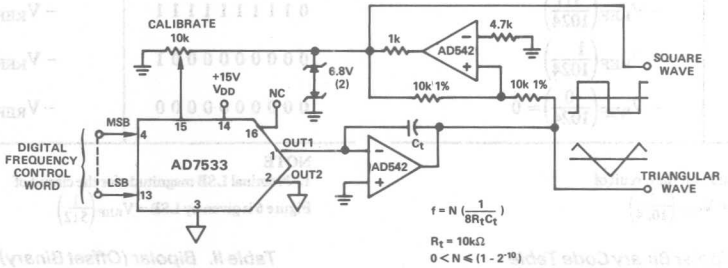
Figure 6. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS

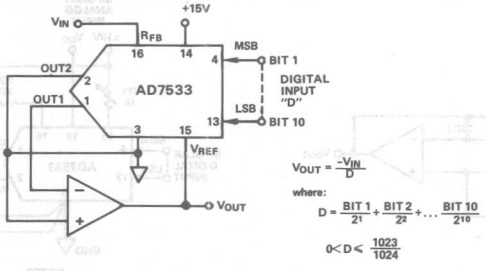
10-BIT AND SIGN MULTIPLYING DAC



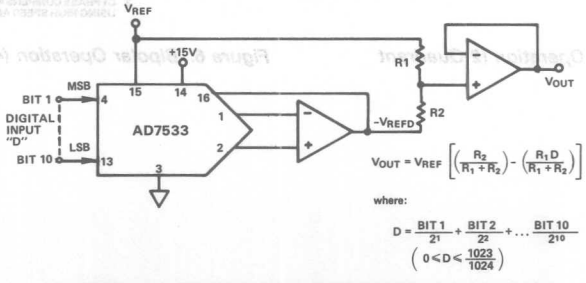
PROGRAMMABLE FUNCTION GENERATOR



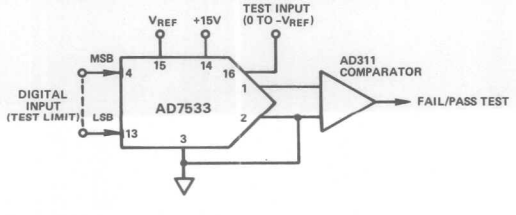
DIVIDER (DIGITALLY CONTROLLED GAIN)



MODIFIED SCALE FACTOR AND OFFSET



DIGITALLY PROGRAMMABLE LIMIT DETECTOR



FEATURES

- 10-Bit Resolution
- Full Four-Quadrant Multiplication
- Nonlinearity: 1/2 or 1 LSB
- TTL/CMOS Compatible
- Improved Gain Error and Linearity Error from +5V to +15V
- Low Power Consumption
- Low Feedthrough Error
- Low Cost
- AD7520 and AD7533 Replacement
- Full Temperature Operation
- Improved ESD Protection
- Available in Die Form

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratiometric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters
- Linear Automatic Gain Control

ORDERING INFORMATION †

	PACKAGE		
NONLINEARITY	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±0.05% (±1/2 LSB)	PM7533AQ	PM7533EQ	PM7533GP
±0.1% (±1 LSB)	PM7533BQ	PM7533FQ	–
±0.1% (±1 LSB)	–	PM7533FP	–
±0.1% (±1 LSB)	–	PM7533FPC	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7533AQ	AD7533UD	MIL
PM7533BQ	AD7533TD	
PM7533BQ	AD7533SD	
PM7533EQ	AD7533CD	IND
PM7533FQ	AD7533BD	
PM7533FQ	AD7533AD	
PM7533GP	AD7533LN	COM
PM7533FP	AD7533LN	
PM7533FPC	AD7533KP	

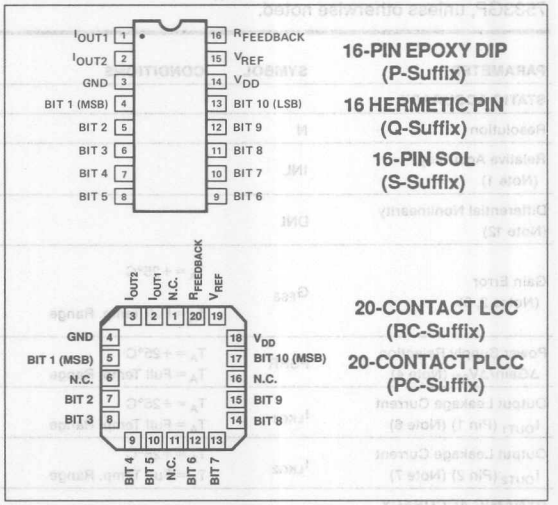
GENERAL DESCRIPTION

The PM-7533 is a 10-bit 4-quadrant multiplying DAC. It is manufactured using thin film on an oxide-isolated, silicon-gate, monolithic CMOS wafer fabrication process. PMI's advanced thin-film resistor processing provides true 10-bit linearity and excellent long-term stability without laser trimming.

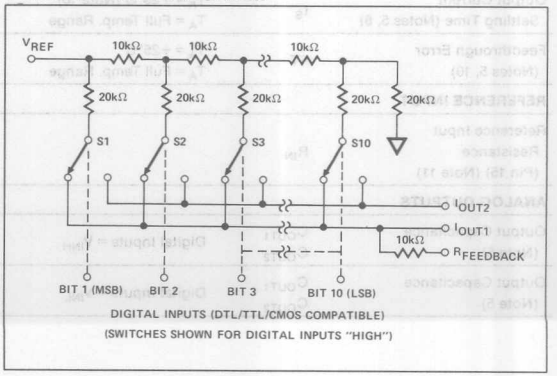
The PM-7533 is pin and function equivalent to the AD7520 and AD7533.

The PMI PM-7533 applications flexibility allows direct interface to TTL or CMOS circuitry and operation from +5V to +15V power supplies. Output scaling is provided by the internal feedback resistor and an external op amp; both positive and negative reference voltages can be accommodated.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



V_{DD} (to GND)	−0.3V, +17V
V_{REF} (to GND)	±25V
R_{FB} (to GND)	±25V
Digital Input Voltage Range	−0.3 to V_{DD}
Output Voltage (Pin 1, Pin 2)	−0.3 to V_{DD}
Operating Temperature Range	
Military (AQ, BQ Versions)	−55°C to +125°C
Industrial (EQ, FQ, FP, FPC)	−40°C to +85°C
Commercial (GP Version)	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:

1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, = −55°C to +125°C apply for PM-7533AQ/BQ, T_A = −40°C to +85°C apply for PM-7533EQ/FQ/FP/FPC/FS, T_A = 0°C to +70°C apply for PM-7533GP, unless otherwise noted.

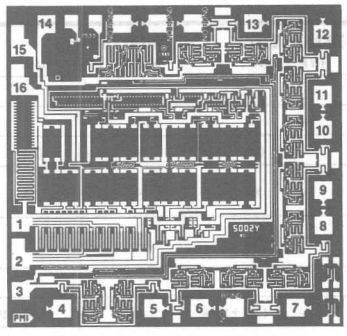
PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G MIN	TYP	MAX	PM-7533B/F/H MIN	TYP	MAX	UNITS
STATIC ACCURACY									
Resolution	N		10	—	—	10	—	—	Bits
Relative Accuracy (Note 1)	INL		—	—	±0.05	—	—	±0.1	% FSR
			—	—	(±1/2)	—	—	(±1)	(LSB)
Differential Nonlinearity (Note 12)	DNL		—	—	±0.1	—	—	±0.1	% FSR
			—	—	(±1)	—	—	(±1)	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C	—	—	±1.4	—	—	±1.4	% FS
			—	—	(±14)	—	—	(±14)	(LSB)
		T_A = Full Temp. Range	—	—	±1.5	—	—	±1.5	% FS
			—	—	(±15)	—	—	(±15)	(LSB)
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ (Note 4)	PSRR	T_A = +25°C	—	—	0.005	—	—	0.005	%/%
		T_A = Full Temp. Range	—	—	0.008	—	—	0.008	
Output Leakage Current I_{OUT1} (Pin 1) (Note 6)	I_{LKG1}	T_A = +25°C	—	—	±50	—	—	±50	nA
		T_A = Full Temp. Range	—	—	±200	—	—	±200	
Output Leakage Current I_{OUT2} (Pin 2) (Note 7)	I_{LKG2}	T_A = +25°C	—	—	±50	—	—	±50	nA
		T_A = Full Temp. Range	—	—	±200	—	—	±200	
DYNAMIC ACCURACY									
Output Current Settling Time (Notes 5, 8)	t_S	T_A = +25°C (Note 10)	—	—	600	—	—	600	ns
		T_A = Full Temp. Range	—	—	800	—	—	800	
Feedthrough Error (Notes 5, 10)	FT	T_A = +25°C	—	—	±0.05	—	—	±0.05	% FSR
		T_A = Full Temp. Range	—	—	±0.1	—	—	±0.1	
REFERENCE INPUT									
Reference Input Resistance (Pin 15) (Note 11)	R_{IN}		5	—	20	5	—	20	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 5)	C_{OUT1}	Digital Inputs = V_{INH}	—	—	100	—	—	220	pF
	C_{OUT2}		—	—	35	—	—	60	
Output Capacitance (Note 5)	C_{OUT1}	Digital Inputs = V_{INL}	—	—	60	—	—	120	pF
	C_{OUT2}		—	—	100	—	—	165	

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = –55°C to +125°C apply for PM-7533AQ/BQ, T_A = –40°C to +85°C apply for PM-7533EQ/FQ/FP/FPC/FS, T_A = 0°C to +70°C apply for PM-7533GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G MIN	PM-7533A/E/G TYP	PM-7533A/E/G MAX	PM-7533B/F MIN	PM-7533B/F TYP	PM-7533B/F MAX	UNITS
DIGITAL INPUTS									
Digital Input High	V_{INH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V_{INL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V and V_{DD}	—	—	±1	—	—	±1	µA
Input Capacitance (Note 5)	C_{IN}		—	—	10	—	—	10	pF
POWER REQUIREMENTS									
Power Supply Voltage	V_{DD}		—	—	+15 ±10%	—	—	+15 ±10%	V
Power Supply Voltage Range	PSR	Accuracy is not guaranteed over this range	+5	—	+16	+5	—	+16	V
Supply Current	I_{DD}	Digital inputs = V_{INL} or V_{INH}	—	—	2	—	—	2	mA

NOTES:
1. "FSR" is full-scale range.
2. Full-scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$; Digital inputs = V_{INH}.
3. Maximum gain change from T_A = +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
4. Digital inputs = V_{INH}, V_{DD} = +14V to +17V.
5. Guaranteed and not tested.
6. Digital inputs = V_{INL}.
7. Digital inputs = V_{INH}.
8. Settles to 0.05% FSR; R_{LOAD} = 100Ω; digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}.
9. AC parameters sample tested to ensure spec compliance.
10. Digital input = V_{INL}; V_{REF} = 20V_{p-p}, f = 100kHz Sinewave.
11. Absolute temperature coefficient is approximately +50ppm/°C.
12. All grades guaranteed monotonic.

DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.591 × 2.540 mm, 6.58 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT BIT 1 (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT BIT 2
6. DIGITAL INPUT BIT 3
7. DIGITAL INPUT BIT 4
8. DIGITAL INPUT BIT 5
9. DIGITAL INPUT BIT 6
10. DIGITAL INPUT BIT 7
11. DIGITAL INPUT BIT 8
12. DIGITAL INPUT BIT 9
13. DIGITAL INPUT BIT 10 (LEAST SIGNIFICANT BIT)
14. POSITIVE POWER SUPPLY
15. REFERENCE INPUT VOLTAGE
16. INTERNAL FEEDBACK RESISTOR

WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		10	Bits MIN
Relative Accuracy (Notes 1, 2)	INL		±0.1 (±1)	% FSR (LSB) MAX
Differential Nonlinearity (Note 10)	DNL		±0.1 (±1)	%FSR (LSB) MAX
Gain Error (Notes 2, 3, 4)	G_{FSE}		±1.4 (±14)	% FS (LSB) MAX
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ (Notes 2, 5, 6)	PSR		0.005	%/% MAX
Output Leakage Current I_{OUT1} (Notes 2, 7)	I_{LKG1}		±50	nA MAX
Output Leakage Current I_{OUT2} (Notes 2, 8)	I_{LKG2}		±50	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Notes 2, 9)	R_{IN}		5/20	kΩ MIN/MAX

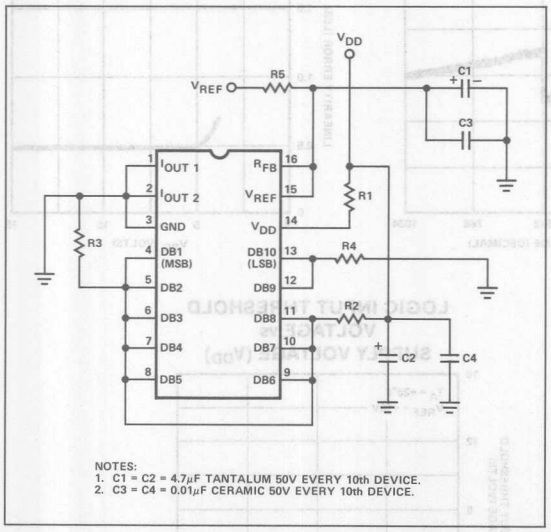
WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
DIGITAL INPUTS				
Digital Input High (Note 2)	V_{INH}		2.4	V MIN
Digital Input Low (Note 2)	V_{INL}		0.8	V MAX
Input Leakage Current (Note 2)	I_{IN}	V_{IN} = 0V and V_{DD}	±1	μA MAX
POWER REQUIREMENTS				
Power Supply Voltage	V_{DD}		+15 ±10%	V MAX
Supply Current (Note 2)	I_{DD}	Digital Inputs = V_{NL} or V_{INH}	2	mA MAX

NOTES:
1. "FSR" is full-scale range.
2. DICE final electrical tests are: relative accuracy, gain error, output leakage current, V_{INH}, V_{INL}, PSR, R_{IN}, I_{IN} and I_{DD} at +25°C.
3. Full-scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$; Digital inputs = V_{INH}.
4. Maximum gain change from T_A = +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
5. Digital inputs = V_{INH}, V_{DD} = +14V to +17V.
6. Guaranteed and not tested.
7. Digital inputs = V_{INL}.
8. Digital inputs = V_{INH}.
9. Absolute temperature coefficient is approximately +300ppm/°C.
10. Guaranteed monotonic.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

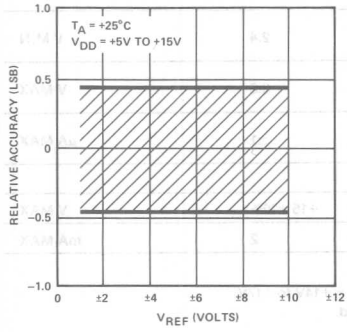
BURN-IN CIRCUIT



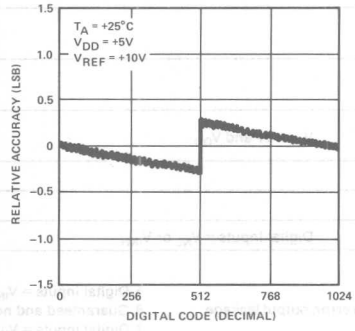
NOTES:
1. C1 = C2 = 4.7μF TANTALUM 50V EVERY 10th DEVICE.
2. C3 = C4 = 0.01μF CERAMIC 50V EVERY 10th DEVICE.

TYPICAL PERFORMANCE CHARACTERISTICS

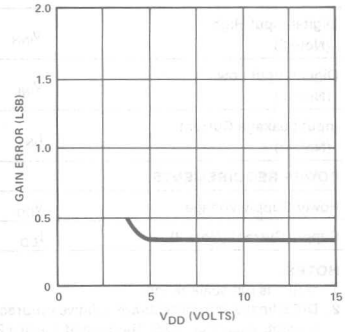
RELATIVE ACCURACY (NONLINEARITY) vs V_{REF}



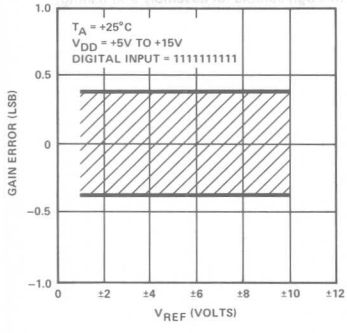
RELATIVE ACCURACY (NONLINEARITY) vs DIGITAL CODE



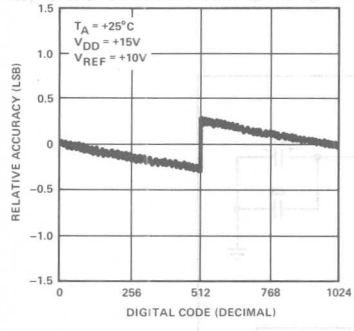
GAIN ERROR vs SUPPLY VOLTAGE



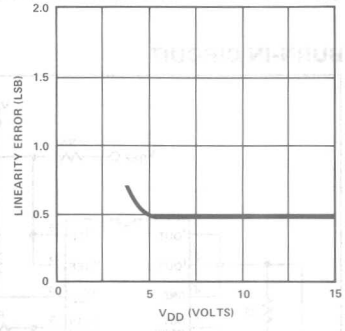
GAIN ERROR vs V_{REF}



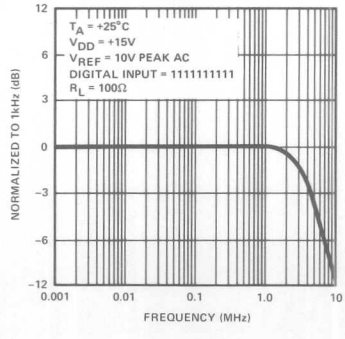
RELATIVE ACCURACY (NONLINEARITY) vs DIGITAL CODE



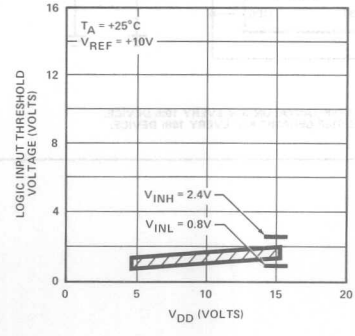
LINEARITY ERROR vs SUPPLY VOLTAGE



V_{REF} FREQUENCY RESPONSE



LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point (nonlinearity) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

CIRCUIT DESCRIPTION

The PM-7533 is a 10-bit multiplying D/A converter. It consists of a silicon-chrome thin-film R-2R resistor ladder network and ten pairs of NMOS current steering switches, all on a monolithic chip. The NMOS current steering switches are controlled by CMOS inverters. Most applications require the addition of only an operational amplifier and a current or voltage reference.

An inverted R-2R ladder network in a simplified D/A converter circuit is shown in Figure 1. The current through each ladder leg is switched between I_{OUT1} and I_{OUT2} under the control of the digital inputs. This allows a constant current to be maintained in each ladder leg regardless of the digital-input switch states.

The design incorporates a matching MOS transistor in series with the feedback and terminating resistors. These MOS transistors, shown as switches in Figure 1, provide improved gain and linearity performance over the operating temperature range. The resulting typical gain temperature coefficient is 2ppm/°C.

FIGURE 1: Simplified DAC Circuit

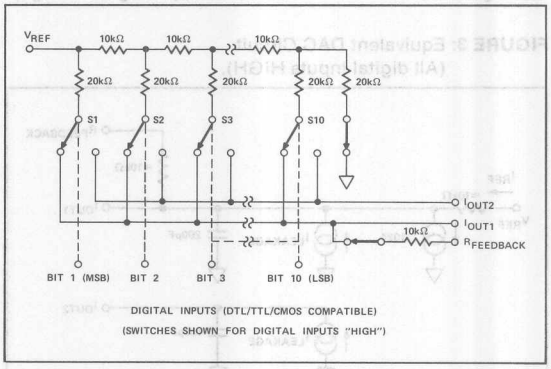
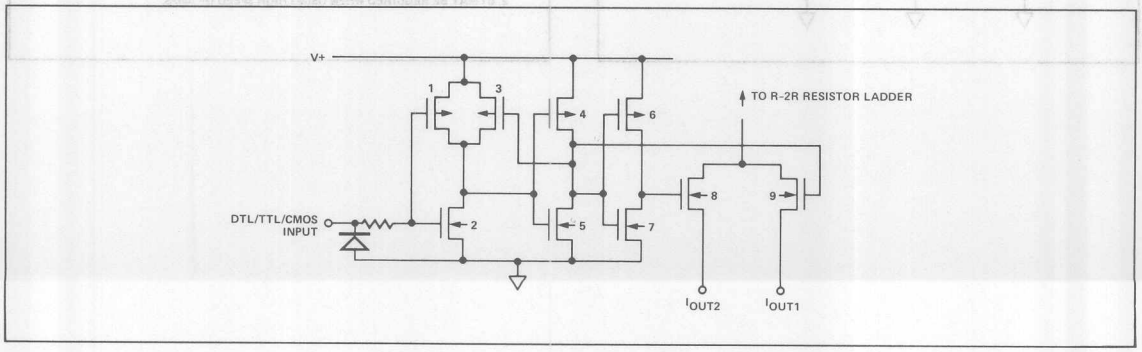


Figure 2 shows one of ten digital input CMOS inverters driving an NMOS switch. The size of devices 1, 2, and 3 are optimized to make the digital inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives the two inverters (4, 5) and (6, 7), which drives the two NMOS switches (8 and 9). The switch "ON" resistances are binarily-scaled so that the voltage drop across each switch is the same; that is, switch S1 in Figure 1 (8 and 9 of Figure 2) was designed for an "ON" resistance of 20 ohms, switch S2 for 40 ohms, etc. With a 10V reference input, switch S1 current is 0.5mA, switch S2 is 0.25mA, etc. This will maintain a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal so that the D/A converter accuracy is maintained.

FIGURE 2: CMOS Switch



EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits of the DAC with all digital inputs high and low respectively. With all digital inputs in the high state as shown in Figure 3, the reference current is switched to the I_{OUT1} terminal, and the I_{OUT2} terminal is open-circuited. Only the output capacitance, surface, leakages, and junction leakages appear at the I_{OUT2} terminal. The 1/1024 current source is a constant 1-bit current drain through the termination resistor of the R-2R ladder network. The $I_{LEAKAGE}$ current source represents a combination of surface and junction leakages to the substrate. The "ON" capacitance of the output NMOS switch is higher on the I_{OUT1} terminal when all digital inputs are high (MOS transistor gate capacitance increases with applied gate voltage).

FIGURE 3: Equivalent DAC Circuit (All digital inputs HIGH).

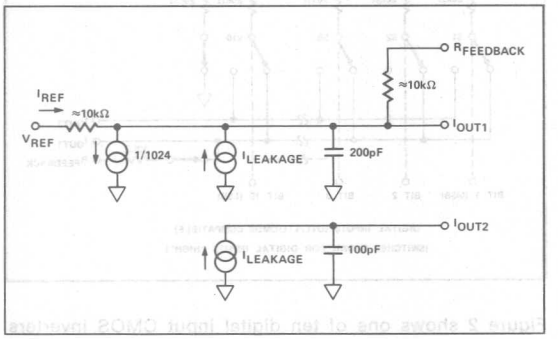
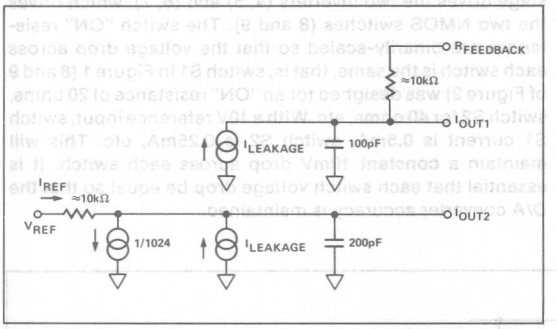


FIGURE 4: Equivalent DAC Circuit (All digital inputs LOW).



When the conditions are reversed with all digital inputs low as shown in Figure 4, the I_{OUT1} terminal is open-circuited and the current is directed towards the I_{OUT2} terminal.

APPLICATIONS INFORMATION

Figure 5 shows a simple unipolar circuit using the PM-7533. Resistors R1 and R2 are used to trim for full scale. Full-scale output voltage = $-V_{REF} \times (1023/1024)$ with all digital inputs high. Full scale can also be adjusted using V_{REF} thereby eliminating resistors R1 and R2. In many applications, R1 and R2 are not required. Zero-scale output voltage (with all digital inputs low) should be adjusted to less than 10% of 1 LSB using the op amp offset adjust. This will help to keep the nonlinearity errors to a minimum. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps.

The circuit of Figure 5 can be used either as a fixed reference digital-to-analog converter, or can be used with an AC signal at the V_{REF} terminal. Used with a fixed reference voltage, the output voltage range will be from zero to $-V_{REF}$, (the op amp inverts the voltage). The circuit behaves as an attenuator when used with an AC V_{REF} signal. The input voltage range is ±20V, but this voltage will be limited by the op amp voltage range. The digital-input-code versus analog-output-voltage is shown is Table 1. The transfer function is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots \frac{A_{10}}{2^{10}}\right)$$

where $A_1 \ldots A_{10}$ assumes a value of 1 for an ON bit and 0 for an OFF bit.

FIGURE 5: Unipolar Binary Operation (2-Quadrant Multiplication)

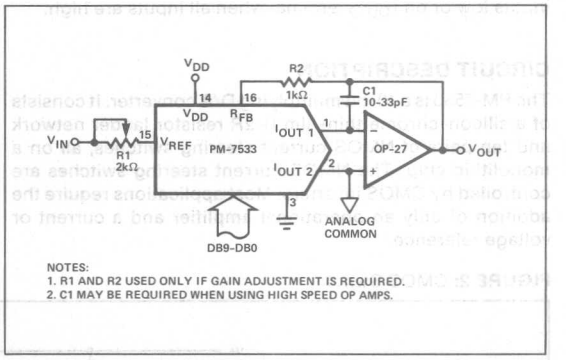


TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right) = \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal full scale for the circuit of Figure 5 is given by
   $FS = -V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by
   $LSB = V_{REF}\left(\frac{1}{1024}\right)$ or $V_{REF}(2^{-n})$

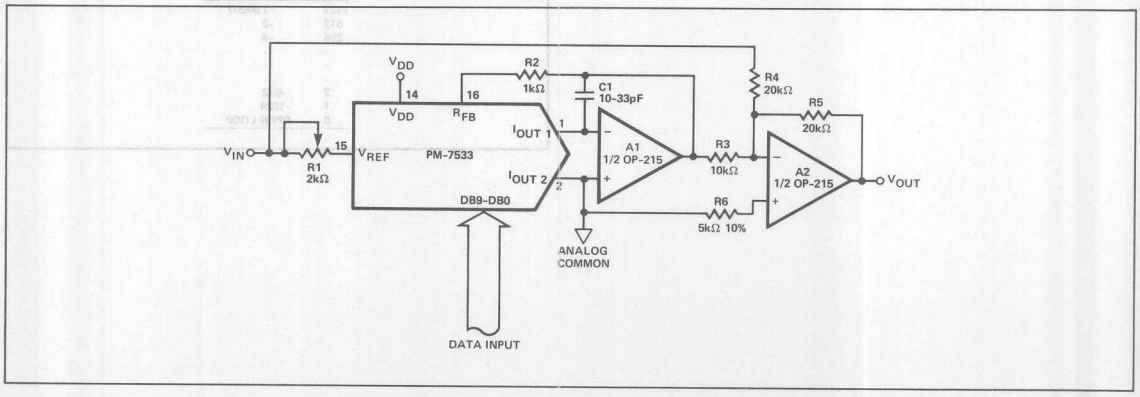
Figure 6 shows a simple bipolar output circuit using the PM-7533 and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF}. Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF}. Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{REF} voltage or R5. The zero-scale output voltage is adjusted while the digital inputs are set to 1000000000 and adjusting R1 for a zero output voltage (less than 10% of 1 LSB). Resistors R3, R4 and R5 must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors R1 and R2 temperature coefficients must be taken into account if they are used. C1 phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 6 is given by
   $FSR = V_{REF}\left(\frac{512}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by
   $LSB = V_{REF}\left(\frac{1}{512}\right)$

FIGURE 6: Bipolar Operation (4-Quadrant Multiplication)



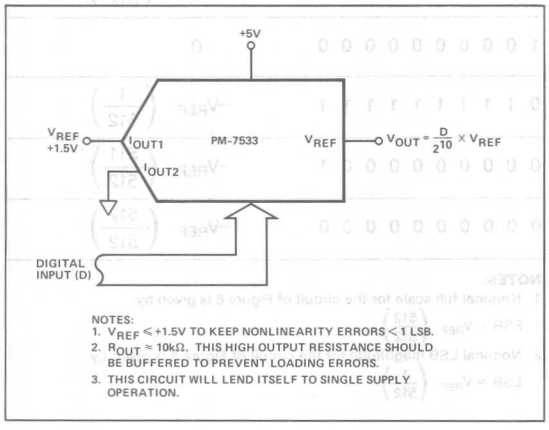
The PM-7533 may be used in the voltage output operation as shown in Figure 7. This circuit configuration will lend itself to single-supply operation because signal inversion does not occur. The output should be buffered due to its high output resistance (10kΩ) to prevent loading errors. The reference voltage should be kept to +1.5 volts maximum to keep nonlinearity errors to less than 1 LSB as shown in Figure 8.

By connecting the DAC in the feedback of an op amp as shown in Figure 9, the circuit behaves as a programmable gain amplifier (analog/digital divider). The transfer function is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots \frac{A_{10}}{2^{10}}} \right)$$

where $A_1 \ldots A_{10}$ assumes a value of 1 or 0.

FIGURE 7: Voltage Output Operation



NOTES:
1. $V_{REF} \leq +1.5V$ TO KEEP NONLINEARITY ERRORS < 1 LSB.
2. $R_{OUT} \approx 10k\Omega$. THIS HIGH OUTPUT RESISTANCE SHOULD BE BUFFERED TO PREVENT LOADING ERRORS.
3. THIS CIRCUIT WILL LEND ITSELF TO SINGLE SUPPLY OPERATION.

FIGURE 8: Voltage Mode

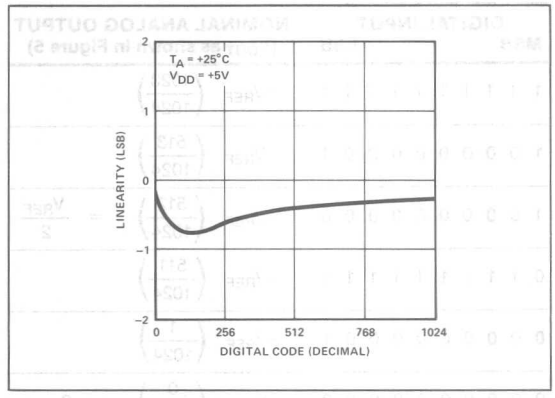
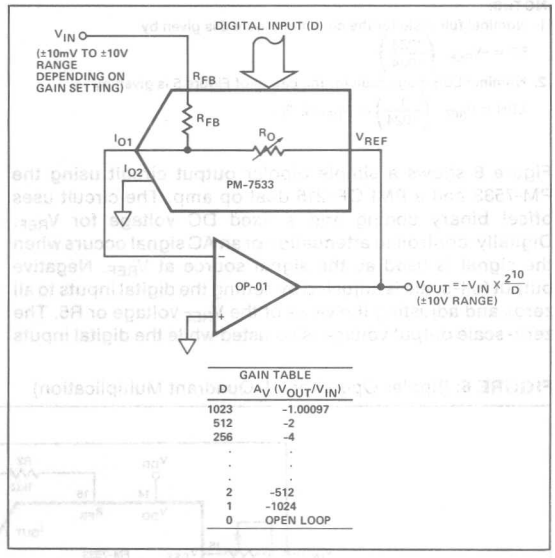


FIGURE 9: Programmable Gain Amplifier



GAIN TABLE

D	A_V (V_{OUT}/V_{IN})
1023	-1.00097
512	-2
256	-4
.	.
.	.
.	.
2	-512
1	-1024
0	OPEN LOOP

ANALOG DEVICES

LC²MOS µP-Compatible 14-Bit DAC

AD7534

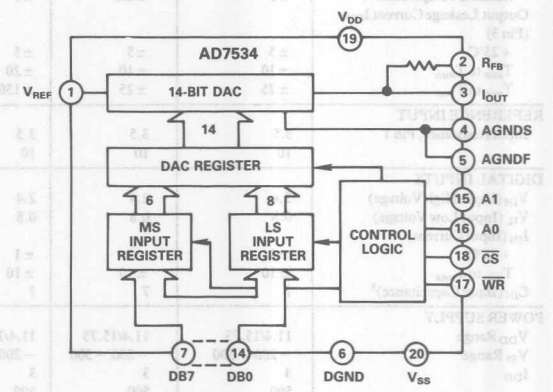
FEATURES

- All Grades 14-Bit Monotonic Over the Full Temperature Range
- Full 4-Quadrant Multiplication
- Microprocessor-Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Small 20-Pin DIP and Surface Mount Package
- Low Output Leakage (<20nA) Over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio Reconstruction
- High Precision Servo Control
- Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7534 is a 14-bit monolithic CMOS D/A converter which uses thin-film resistors and laser trimming to achieve excellent linearity.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

A novel low leakage configuration (patent pending) enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op amp. The AD7534 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Montonicity
   The AD7534 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 20) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin DIP and 20-terminal surface mount package.

AD7534—SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic over temperature.
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5 10	3.5 10	3.5 10	3.5 10	kΩ min kΩ max	Typical Input Resistance = 6kΩ
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over this range.
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV, Output Amplifier is AD544 except where stated).

Parameter	V_{DD} = +11.4V to +15.75V T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	100	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz – 100kHz)	15	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	140	160	180	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (Pin 19) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 20) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 7–18) to DGND . . −0.3V, V_{DD}
V_{PIN3} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full Scale Error	Package Option*
AD7534JN	0°C to +70°C	±2LSB	±8LSB	N-20
AD7534KN	0°C to +70°C	±1LSB	±4LSB	N-20
AD7534JP	0°C to +70°C	±2LSB	±8LSB	P-20A
AD7534KP	0°C to +70°C	±LSB	±4LSB	P-20A
AD7534AQ	−25°C to +85°C	±2LSB	±8LSB	Q-20
AD7534BQ	−25°C to +85°C	±1LSB	±4LSB	Q-20
AD7534SQ	−55°C to +125°C	±2LSB	±8LSB	Q-20
AD7534TQ	−55°C to +125°C	±1LSB	±4LSB	Q-20

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL TO ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

OUTPUT CAPACITANCE

Capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT

Current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

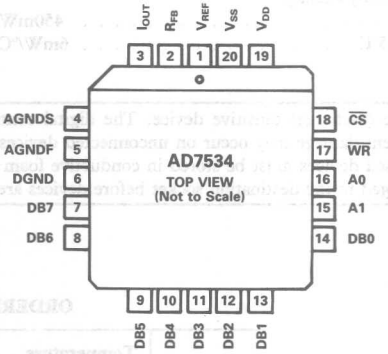
AC error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

PIN CONFIGURATIONS

DIP



PLCC



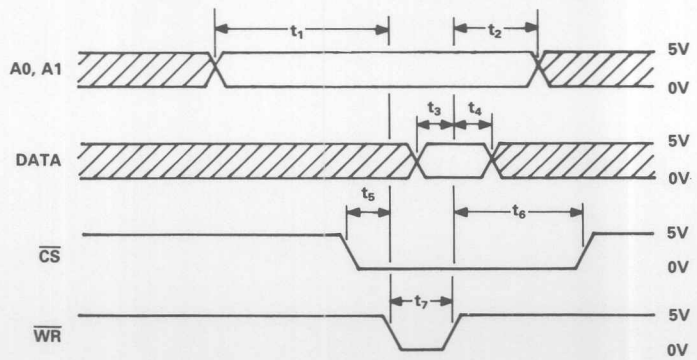
Pin Function Description — AD7534

Pin	Function	Description
1	V_{REF}	Reference Input Voltage
2	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
3	I_{OUT}	Current Output Terminal
4	AGNDS	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
5	AGNDF	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
6	DGND	Digital Ground
7	DB7	Data Bit 7
8	DB6	Data Bit 6
9	DB5	Data Bit 5 or Data Bit 13 (DAC MSB)
10	DB4	Data Bit 4 or Data Bit 12
11	DB3	Data Bit 3 or Data Bit 11
12	DB2	Data Bit 2 or Data Bit 10
13	DB1	Data Bit 1 or Data Bit 9
14	DB0	Data Bit 0 or Data Bit 8
15	A1	Address line 1
16	A0	Address line 0
17	$\overline{WR}$	Write input. Active low.
18	$\overline{CS}$	Chip Select Input. Active low.

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X[1]	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus[2]
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

NOTES
1. X = Don't Care
2. When $A_1 = 0$, $A_0 = 0$ all DAC registers are transparent, so by placing all 0's or all 1's on the data inputs the user can load the DAC to zero or full scale output in one write operation. This facility simplifies system calibration.

19	V_{DD}	+12V to +15V supply input.
20	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4, 5 or 6 for recommended circuitry.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7534 Timing Diagram

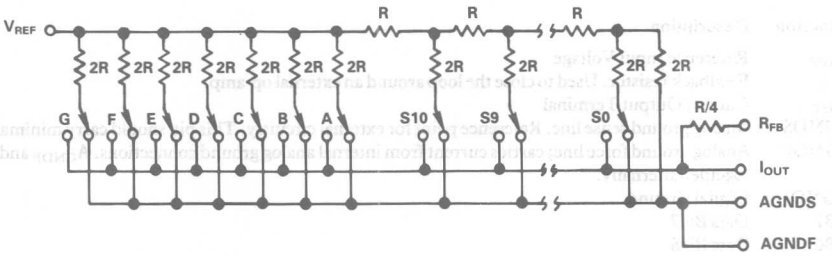


Figure 2. Simplified Circuit Diagram for the AD7534 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7534 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word drive an inverted R-2R ladder which steers the binarily weighted current available to it between I_{OUT} and AGNDF.

If I is taken as the input current at V_{REF} the input current to the R-2R ladder is I/8. 7/8 I flows in the parallel ladder structure. Switches A-G steer binarily weighted current between I_{OUT} and AGNDF.

The input resistance at V_{REF} is constant and may be driven by a voltage source or a current source of positive or negative polarity.

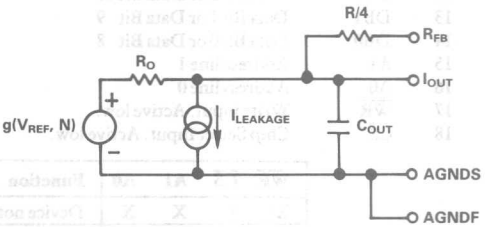


Figure 3. AD7534 Equivalent Analog Output Circuit

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7534 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the R-2R ladder, N.

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

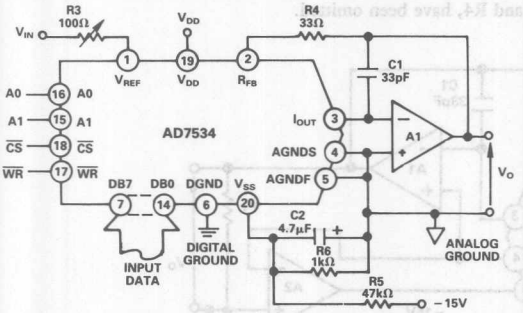


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7534

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Calibration codes for zero and full scale adjust (all 0's, all 1's) can be loaded in one write operation (see Pin Function Description).

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e., ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

In fixed reference applications full scale can also be adjusted by omitting R3 and R4 and trimming the reference voltage magnitude.

For high temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7534, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R3 for V_O = 0V. Alternatively, one can omit R3 and R4 and adjust the ratio of R7 and R8 for V_O = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R9.

Resistors R7, R8 and R9 should be matched to 0.003%. Mismatch of R7 and R8 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficient match.

The code table for Figure 5 is given in Table II.

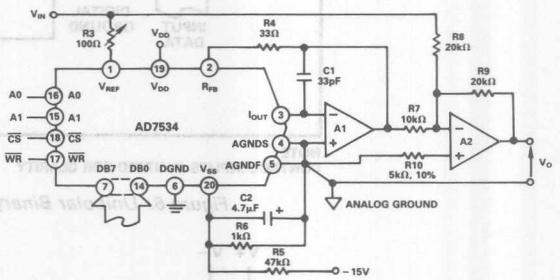


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

Since the AD7534 is specified for high accuracy, it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, AGNDS and AGNDF are externally shorted and A2 is not used. Voltage drops due to bond wire resistances are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used. Here, A2 is used to maintain AGNDS at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated.

Figure 7 shows a Printed Circuit Board layout for the AD7534 with a single output amplifier. The input to V_{REF} (pin 1) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough. The tracks connecting I_{OUT} and AGNDS to the inverting and noninverting op amp inputs are kept as short as possible. Gain trim components, R3 and R4, have been omitted.

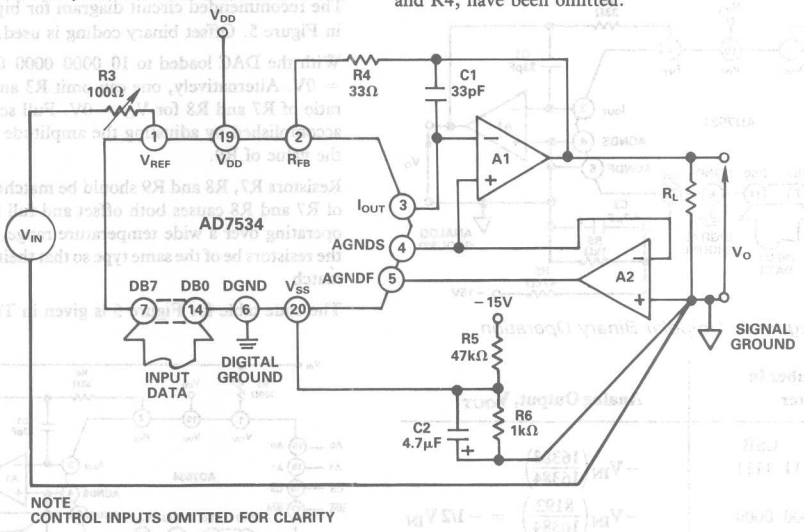


Figure 6. Unipolar Binary Operation with Forced Ground

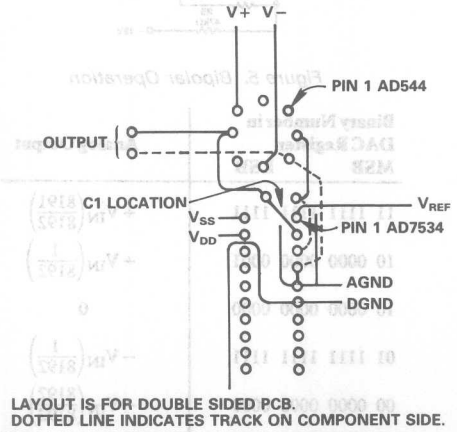


Figure 7. Suggested Layout for AD7534 Incorporating Output Amplifier

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for minimum potential at AGNDS. This potential should be ≤30μV with respect to Signal Ground.
3. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7534 features a leakage reduction configuration to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 20) is tied to AGND then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4, 5 and 6. A simple resistor divider (R5, R6) produces $-312mV$ from $-15V$. The capacitor C2 in parallel with R6 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP AMP SELECTION

In choosing an amplifier to be used with the AD7534, three parameters are of prime importance. These are Input Offset Voltage (V_{OS}), Input Bias Current, (I_{BIAS}) and Offset Voltage Drift. To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than $30\mu V$ while I_{BIAS} should be less than 2nA. Also the open loop gain of the amplifier must be sufficiently high to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. Thus for a max output of 10V, A_{VOL} must be greater than 340,000.

An amplifier with low offset voltage drift is required to give the desired system accuracy over an operating temperature range.

At low frequencies the AD OP-07 satisfies the above requirements and in most cases will not need an offset adjust potentiometer.

For high frequency operation, one may use a wide bandwidth amplifier such as the AD544 or the LF356 with either an offset adjust potentiometer or automatic nulling circuitry.

The choice of amplifier depends entirely on the required system accuracy, the required temperature range, and the operating frequency.

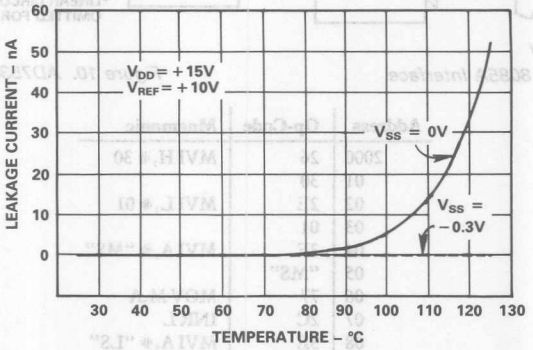


Figure 8. Graph of Typical Leakage Current vs. Temperature for AD7534

processor is given in Figure 9. The microprocessor sees the DAC as four memory locations, identified by address lines A0, A1. In standard operation, three of these memory locations are used. A sample program for loading the DAC with a 14-bit word is given in Table III. The AD7534 has address locations 3000–3003.

The six MSBs are written into location 3001, and the eight LSBs are written to 3002. Then with a write instruction to 3003 using the circuit of Figure 10. The bottom 8 bits (AD0–AD7) of the 16-bit data bus are connected to the DAC data bus. The 14-bit word is loaded in two bytes using the MOV instruction. A further MOV loads the DAC register and causes the analog data to appear at the converter output. For the example given here, the appropriate DAC register addresses are D002, D004, D006. The program for loading the DAC is given below in Table IV.

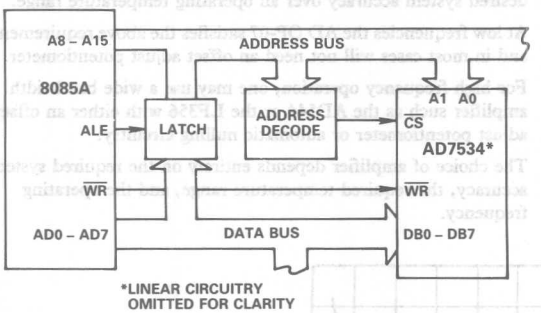


Figure 9. AD7534 – 8085A Interface

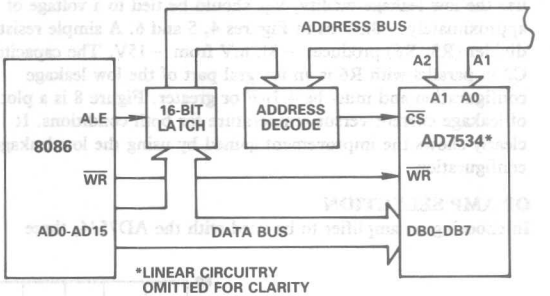


Figure 10. AD7534 – 8086 Interface Circuit

Address	Op-Code	Mnemonic
2000	26	MVI H,# 30
01	30	
02	2E	MVI L,# 01
03	01	
04	3E	MVI A,# "MS"
05	"MS"	
06	77	MOV M,A
07	2C	INR L
08	3E	MVI A,# "LS"
09	"LS"	
0A	77	MOV M, A
0B	2C	INR L
0C	77	MOV M,A
200D	CF	RST I

Table III. Program Listing for Figure 9

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	:	DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	:	TO CODE SEGMENT REGISTER
04	BF02D0	MOV DI, # D002	:	LOAD DI WITH D002
07	C605"MS"	MOV MEM,# "MS"	:	MS INPUT REGISTER LOADED WITH "MS"
0A	47	INC DI		
0B	47	INC DI		
0C	C605"LS"	MOV MEM,# "LS"	:	LS INPUT REGISTER LOADED WITH "LS"
0F	47	INC DI		
10	47	INC DI		
11	C60500	MOV MEM, # 00	:	CONTENTS OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER.
14	EA0000	JMP MEM	:	CONTROL IS RETURNED TO THE MONITOR
17	00FF			PROGRAM

Table IV. Sample Program for Loading AD7534 from 8086

AD7534 – MC6809 INTERFACE

Figure 11 shows an interface circuit which enables the AD7534 to be programmed using the MC6809 8-bit microprocessor. By making use of the 16-bit D Accumulator, the transfer of data is simplified. The two key processor instructions are:

LDD Load D Accumulator from memory.
STD Store D Accumulator to memory.

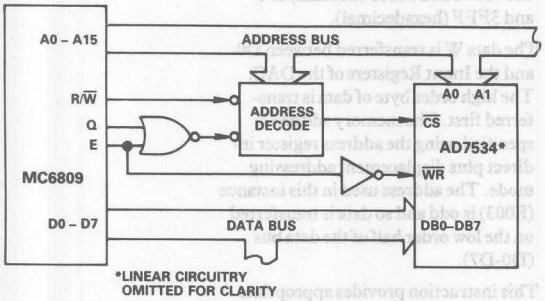


Figure 11. AD7534 – MC6809 Interface Circuit

AD7534 – 6502 INTERFACE

The interface circuit for the 6502 microprocessor is shown in Figure 12.

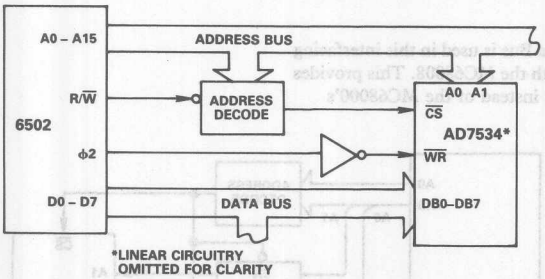


Figure 12. AD7534 – 6502 Interface

AD7534 – Z80 INTERFACE

Interfacing to the Z80 microprocessor requires a minimal amount of extra components. The circuit consists of the Z80 processor, the AD7534 and an address decoder for the DAC. Figure 13, below, illustrates the circuit.

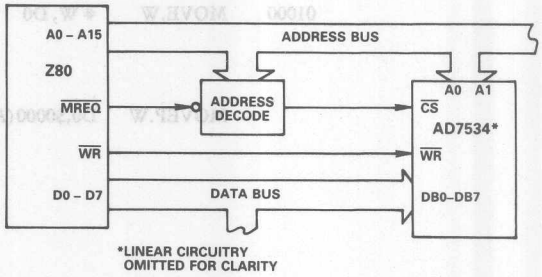


Figure 13. AD7534 – Z80 Interface

2

AD7534 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7534 is accomplished using the circuit of Figure 14. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
                ·A2 E003
01000   MOVE.W    # W, D0
        MOVEP.W   D0,$0000 (A2)
        MOVE.W    D0,$E006
        MOVE.B    # 228,D7
        TRAP      # 14
```

Address Register 2 is loaded with E003.

The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 16383 (decimal) or 0 and 3FFF (hexadecimal).

The data W is transferred between D0 and the Input Registers of the DAC. The high order byte of data is transferred first. The memory address is specified using the address register indirect plus displacement addressing mode. The address used in this instance (E003) is odd and so data is transferred on the low order half of the data bus (D0-D7).

This instruction provides appropriate signals to transfer the data W from the DAC Input Registers to the DAC Register, which controls the switches in the 14-bit D/A structure.

Control is returned to the System Monitor Program using these two insructions.

Since only the lower half of the Data Bus is used in this interfacing system, it is also suitable for use with the MC68008. This provides the user with an eight bit data bus instead of the MC68000's sixteen bit data bus.

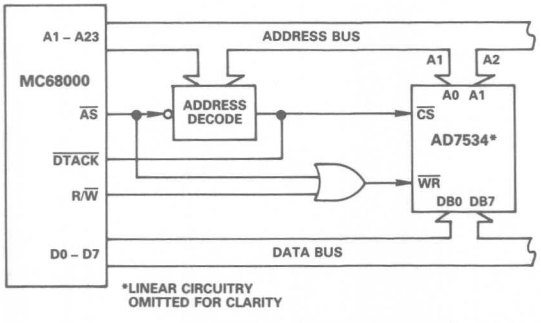


Figure 14. AD7534 – MC68000 Interface

DIGITAL FEEDTHROUGH

In the preceeding interface configurations, most digital inputs to the AD7534 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 15 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.

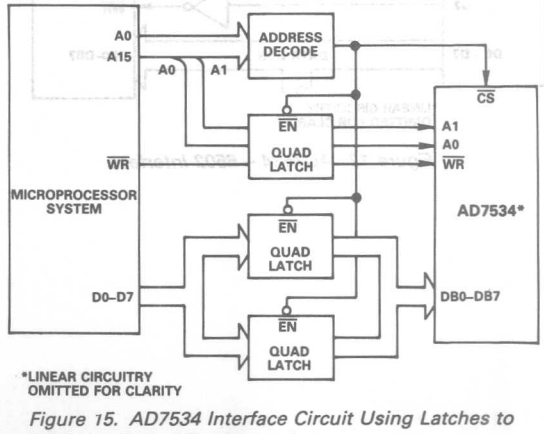


Figure 15. AD7534 Interface Circuit Using Latches to Minimize Digital Feedthrough

LC²MOS
µP Compatible 14-Bit DAC
AD7535

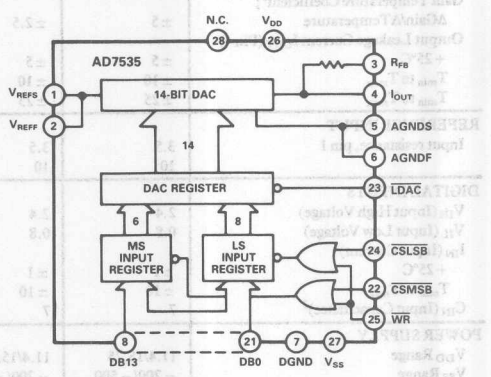
FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Full 4 Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7535 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

Standard Chip Select and Memory Write logic is used to access the DAC.

A novel low leakage configuration (patent pending) enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7535 is manufactured using the Linear Compatible CMOS (LC^2MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7535 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 27) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors. When interfacing to 8-bit processors $\overline{CSMSB}$ and $\overline{CSLSB}$ are separate and the 8-bit data bus is connected to both the MS Input Register and the LS Input Register. For straight 14-bit parallel loading $\overline{CSMSB}$ and $\overline{CSLSB}$ are tied together giving one chip select to load the 14-bit word.

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 4)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input resistance, pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD544 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz – 100kHz)	15	–	$nV\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AQ, BQ Versions: −25°C to +85°C
SQ, TQ Versions: −55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND . . . . . −0.3V, +17V
V_{SS} (pin 27) to AGND . . . . . −15V, +0.3V
V_{REFS} (pin 1) to AGND . . . . . ±25V
V_{REFF} (pin 2) to AGND . . . . . ±25V
V_{RFB} (pin 3) to AGND . . . . . ±25V
Digital Input Voltage (pins 8–25) to DGND . . −0.3V, V_{DD}
V_{PIN4} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial Plastic (J, K Versions) . . . . . 0 to +70°C
Industrial Ceramic (A, B Versions) . . . . −25°C to +85°C
Extended Ceramic (S, T Versions) . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option*
AD7535JN	0°C to +70°C	±2LSB	±8LSB	N-28
AD7535KN	0°C to +70°C	±1LSB	±4LSB	N-28
AD7535JP	0°C to +70°C	±2LSB	±8LSB	P-28A
AD7535KP	0°C to +70°C	±1LSB	±4LSB	P-28A
AD7535AQ	−25°C to +85°C	±2LSB	±8LSB	Q-28
AD7535BQ	−25°C to +85°C	±1LSB	±4LSB	Q-28
AD7535SQ	−55°C to +125°C	±2LSB	±8LSB	Q-28
AD7535TQ	−55°C to +125°C	±1LSB	±4LSB	Q-28
AD7535SE	−55°C to +125°C	±2LSB	±8LSB	E-28A
AD7535TE	−55°C to +125°C	±1LSB	±4LSB	E-28A

*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT

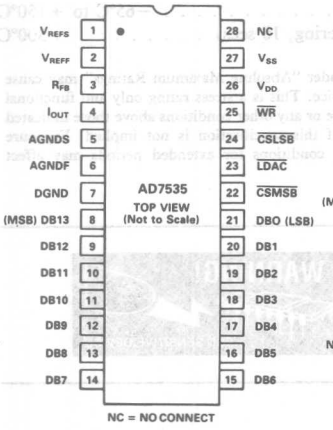
Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

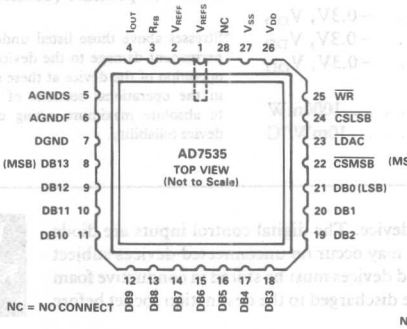
This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

PIN CONFIGURATIONS

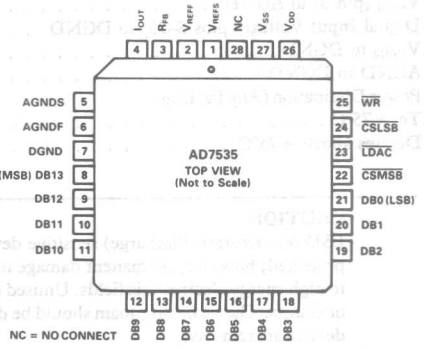
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LCCC



PLCC

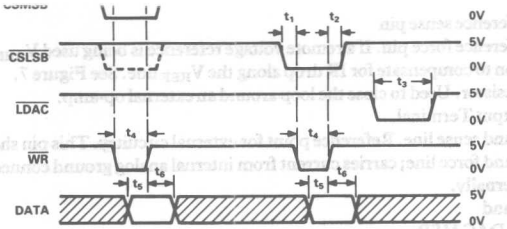


Pin	Function	Description
1	V_{REFS}	Voltage Reference sense pin
2	V_{REFF}	Voltage Reference force pin. If a remote voltage reference is being used V_{REFF} and V_{REFS} can be used in a Kelvin configuration to compensate for IR drop along the V_{REF} line. See Figure 7.
3	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
4	I_{OUT}	Current Output Terminal.
5	A_{GNDS}	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
6	A_{GNDF}	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13. DAC MSB
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0. DAC LSB
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active LOW input.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active LOW.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input.
25	$\overline{WR}$	Write input. Active LOW.

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

26	V_{DD}	+ 12V to + 15V supply input
27	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 4, 5, 6 or 7 for recommended circuitry.
28	N.C.	No connection



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7535 Timing Diagram

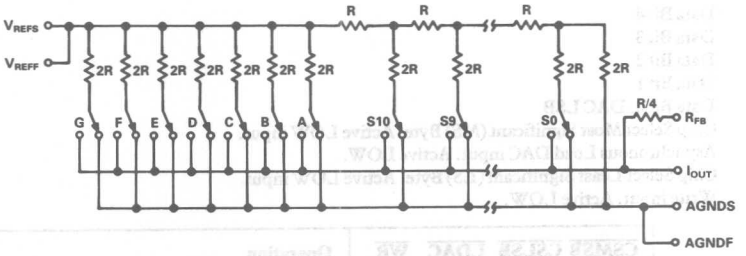


Figure 2. Simplified Circuit Diagram for the AD7535 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7535 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word consist of an R-2R ladder operated in a current steering configuration.

The R-2R ladder current is 1/8 of the total reference input current. 7/8 I flows in the parallel ladder structure. Switches A-G steer equally weighted currents between I_{OUT} and A_{GNDF}.

Since the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7535 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference

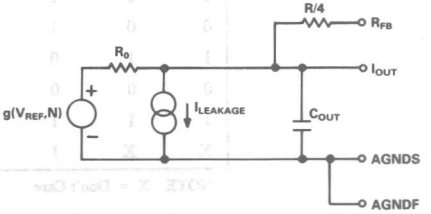


Figure 3. AD7535 Equivalent Analog Output Circuit

input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

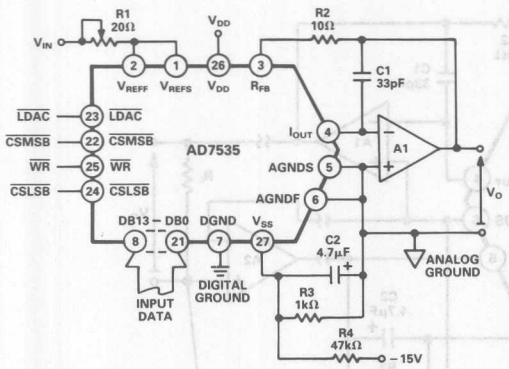


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7535

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

For high temperature applications resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7535, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0V$. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0V$. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

Resistors R5, R6 and R7 should be ratio matched to 0.006%. Mismatch of R5 and R6 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

A range of precision voltage dividers, manufactured by Vishay, offers a suitable solution to implementing the bipolar circuit described above. The resistor networks are TCR and Ratio Matched, giving excellent performance over temperature.

The code table for Figure 5 is given in Table II.

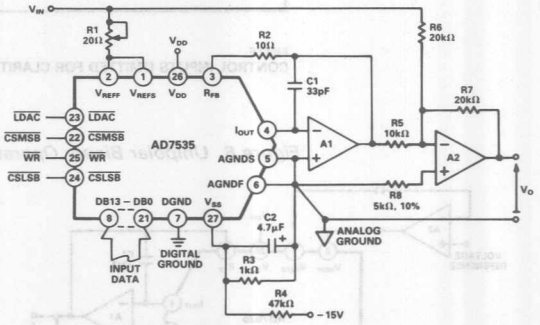


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

Since the AD7535 is specified for high accuracy it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, the AD7535 is connected with the signal ground for the load located close to the DAC. There is no possibility of a voltage drop along the signal ground due to track resistance.

If the signal ground for the load is located at a distance from the DAC then the configuration of Figure 6 should be used. A_2 compensates for the error due to IR voltage drop between the DAC's internal Analog ground and the load signal ground.

Figure 7 shows a remote voltage reference driving the AD7535. Op-amps A2 and A3 compensate for voltage drops along the reference input line and the analog ground line.

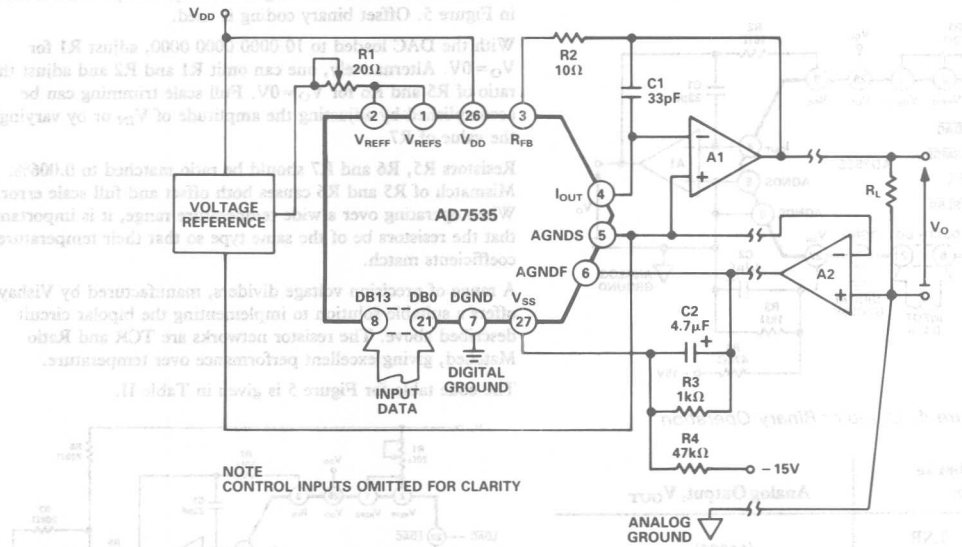


Figure 6. Unipolar Binary Operation with Forced Ground for Remote Load

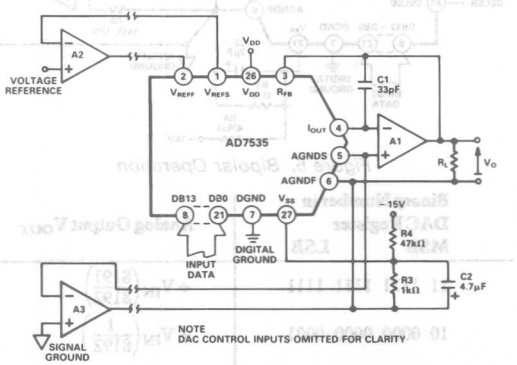


Figure 7. Driving the AD7535 with a Remote Voltage Reference

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for a minimum potential at AGNDS. This potential should be $\leq 30\mu V$ with respect to Signal Ground. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. $\leq 30\mu V$).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7535 features a leakage reduction configuration (patent pending) to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 27) is tied to A_{GND} then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4, 5, 6 and 7. A simple resistor divider (R3, R4) produces approximately $-300mV$ from $-15V$. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP-AMP SELECTION

In choosing an amplifier to be used with the AD7535, three parameters are of prime importance. These are (1) Input Offset Voltage (V_{OS}), (2) Input Bias Current (I_B), (3) Offset Voltage Drift (TC V_{OS}). To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than $30\mu V$ while I_B should be less than 2nA. It is important that the amplifier Open Loop Gain, A_{VOL}, be sufficiently large to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. For a maximum output of 10V, A_{VOL} must be greater than 340,000.

The AD OP-07 series of op-amps have a very low V_{OS} ($25\mu V$) and can be used as the output amplifier for the AD7535 without any external adjustment of Offset Voltage. In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A2. Settling time to 0.003% for the AD OP-07 is typically greater than $50\mu s$.

For faster settling time, one can use the AD544 series of op amps. Typically this settles to 0.003% (14-bits) in $5\mu s$. Even faster settling time can be achieved using the HA-2620 series of op-amps.

For operation over a wide temperature range Offset Voltage Drift and Bias Current Drift are critical parameters. The OP-27 and OP-37 series of op-amps exhibit extremely low Offset Voltage Drift and the AD544 has very low Bias Current Drift.

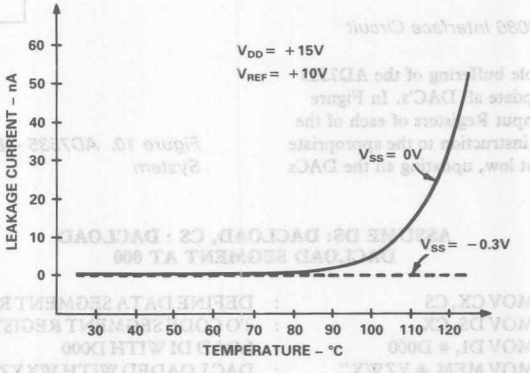


Figure 8. Graph of Typical Leakage Current vs Temperature for AD7535

MICROPROCESSOR INTERFACING

AD7535 – 8086A INTERFACE

The versatility of the AD7535 loading structure allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this setup the double buffering feature of the DAC is not used. AD0–AD13 of the 16-bit data bus are connected to the DAC data bus (DB0–DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III.

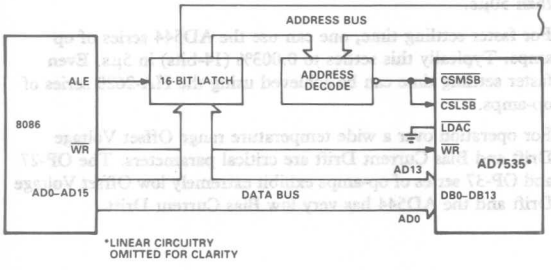


Figure 9. AD7535 – 8086 Interface Circuit

In a multiple DAC system the double buffering of the AD7535 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e. $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

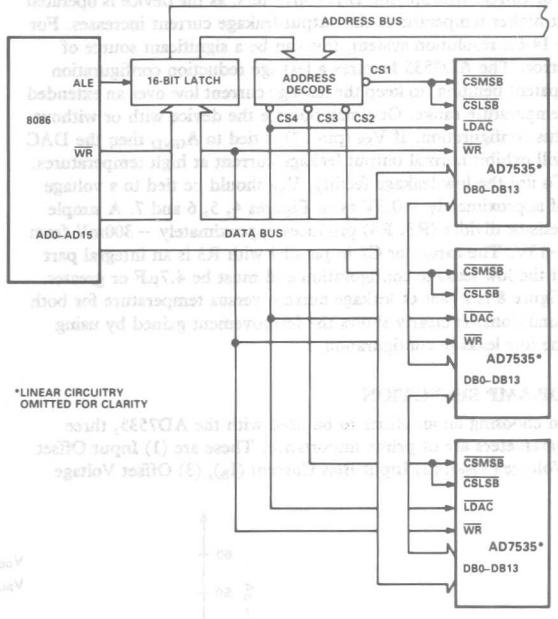


Figure 10. AD7535 – 8086 Interface: Multiple DAC System

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	:	DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	:	TO CODE SEGMENT REGISTER
04	BF00D0	MOV DI, # D000	:	LOAD DI WITH D000
07	C705"YZWX"	MOV MEM, # YZWX"	:	DAC LOADED WITH WXYZ
0B	EA0000		:	CONTROL IS RETURNED TO THE
0E	00FF			MONITOR PROGRAM

Table III. Sample Program for Loading AD7535 from 8086

AD7535 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7535 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
01000   MOVE.W    #W,D0       The desired DAC data, W, is loaded into
                                Data Register 0. W may be any value
                                between 0 and 16383 (decimal) or 0
                                and 3FFF (hexademical).
        MOVE.W    D0,$E000    The data W is transferred between D0
                                and the DAC Register.
        MOVE.B    #228,D7     Control is returned to the System
                                Monitor Program using these two
        TRAP      #14         instructions.
```

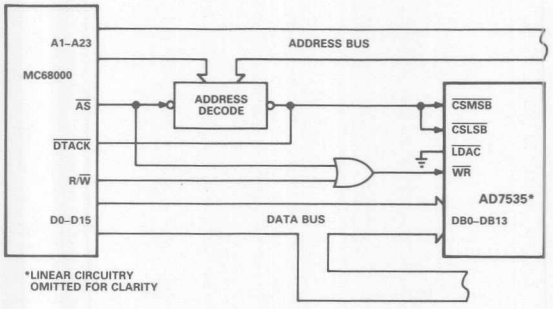


Figure 11. AD7535 – MC68000 Interface

AD7535 – Z80 INTERFACE

Though the AD7535 is primarily intended for use either with 16-bit microprocessors or in stand alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the Z80 microprocessor.

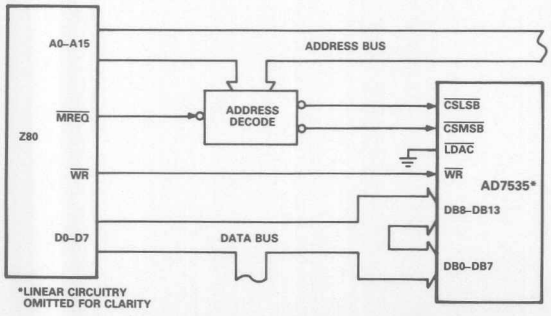


Figure 12. AD7535 – Z80 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7535 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

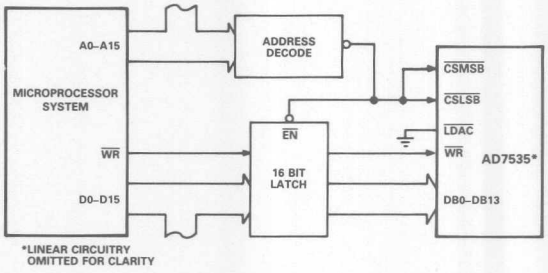


Figure 13. AD7535 Interface Circuit Using Latches to Minimize Digital Feedthrough

LC²MOS 14-Bit µP Compatible DAC

AD7536

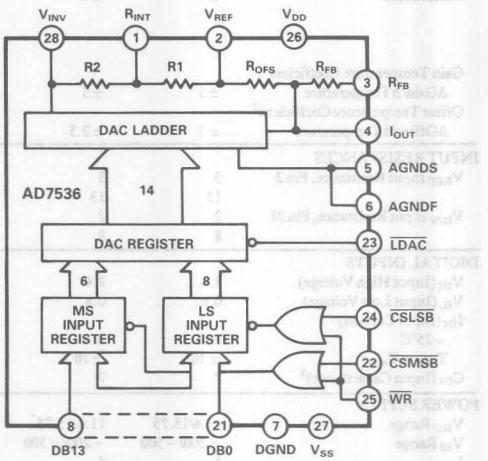
FEATURES

- Full 4-Quadrant Multiplication without External Resistors
- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Gain Temperature Coefficient, 2ppm/°C

APPLICATIONS

- Control and Measurement in High Temperature Environments
- Digital Audio
- Precision Servo Control
- All Microprocessor Based Control Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7536 is a 14-bit monolithic CMOS D/A converter. The part is laser trimmed and specified as a dedicated bipolar DAC. The resistors needed for 4-quadrant multiplication are contained on the chip. Thus, the user requires only the AD7536, a voltage reference and two op-amps for bipolar operation. The AD7536 has the same low leakage configuration (patent pending) as the other members of the 14-bit CMOS DAC family. The excellent output leakage current characteristics also ensure exceptional stability of linearity and gain error over the full temperature range.

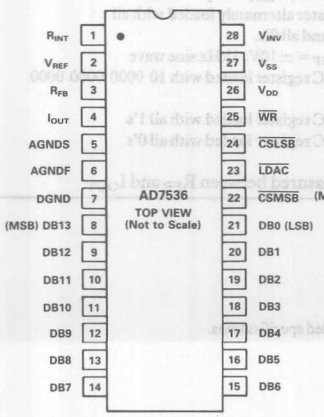
The device is speed compatible with most microprocessors and accepts TTL or 5V CMOS logic level inputs. There is standard Chip Select and Memory Write logic for easy interfacing. The AD7536 has full protection against CMOS "latch-up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp.

PRODUCT HIGHLIGHTS

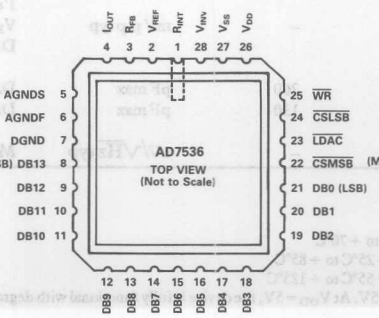
1. Bipolar Operation
   The AD7536 gives the user 4-Quadrant Multiplication without any external resistors.
2. Guaranteed Monotonicity
   14-bit monotonicity is guaranteed over the full temperature range for all grades.
3. Low Output Leakage
   The device has excellent output leakage current characteristics at all temperatures.

PIN CONFIGURATIONS

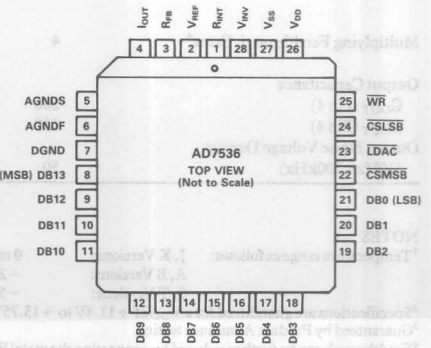
DIP



LCCC



PLCC



AD7536—SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	1LSB = $2V_{REF}/2^{14}$
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic over temperature.
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Gain Error	±16	±8	±16	±8	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Offset Error	±4	±4	±4	±4	LSB max	Error due to mismatch between R_{FB} and offset resistor. It also includes leakage current to I_{OUT} and is measured when DAC is loaded with all 0's.
Gain Temperature Coefficient[3], ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical Value is 2ppm/°C
Offset Temperature Coefficient[3] ΔOffset/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical Value is 1ppm/°C
INPUT RESISTANCES						
V_{REF} Input Resistance, Pin 2	3	3	3	3	kΩ min	Typical Input Resistance = 6kΩ
	13	13	13	13	kΩ max	
V_{INV} Input Resistance, Pin 28	2	2	2	2	kΩ min	Typical Input Resistance = 4kΩ
	8	8	8	8	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}
Power Supply Rejection ΔGain/ΔV_{DD}	±0.02	±0.02	±0.02	±0.02	% per % max	$\Delta V_{DD} = V_{DD}$ max − V_{DD} min

AC PERFORMANCE CHARACTERISTICS These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	4	–	mV p-p typ	V_{REF} = ±10V, 1kHz sine wave DAC register loaded with 10 0000 0000 0000
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	50	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

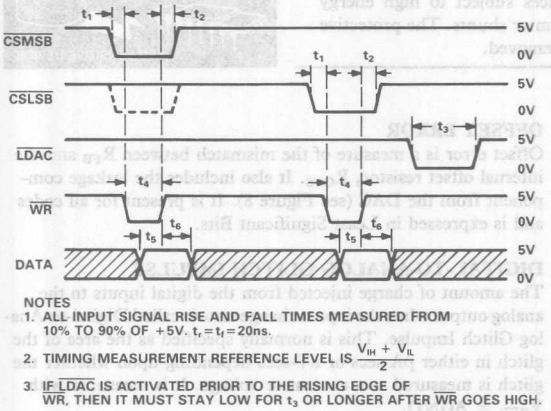
Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, $V_{PIN4} = V_{PIN5}$ = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	$\overline{LDAC}$ Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7536 Timing Diagram

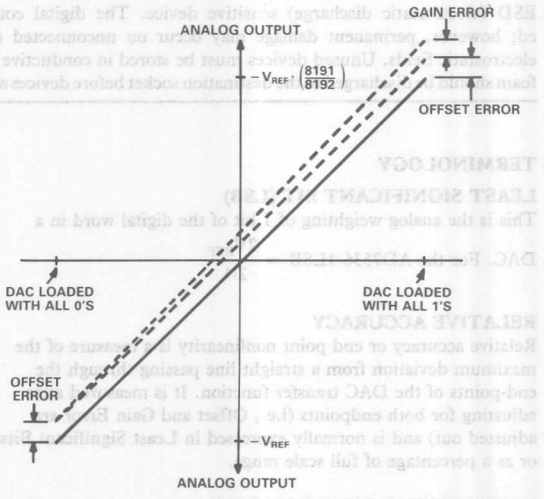


Figure 2. AD7536 Transfer Function

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full Scale Error	Package Option*
AD7536JN	0°C to +70°C	±2LSB	±16LSB	N-28
AD7536KN	0°C to +70°C	±1LSB	±8LSB	N-28
AD7536JP	0°C to +70°C	±2LSB	±16LSB	P-28A
AD7536KP	0°C to +70°C	±1LSB	±8LSB	P-28A
AD7536AQ	−25°C to +85°C	±2LSB	±16LSB	Q-28
AD7536BQ	−25°C to +85°C	±1LSB	±8LSB	Q-28
AD7536SQ	−55°C to +125°C	±2LSB	±16LSB	Q-28
AD7536TQ	−55°C to +125°C	±1LSB	±8LSB	Q-28
AD7536SE	−55°C to +125°C	±2LSB	±16LSB	E-28A
AD7536TE	−55°C to +125°C	±1LSB	±8LSB	E-28A

*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND	−0.3V, +17V
V_{SS} (pin 27) to AGND	−15V, +0.3V
V_{REF} (pin 2) to AGND	±25V
V_{INV} (pin 28) to AGND	±25V
R_{INT} (pin 1) to AGND	±25V
R_{FB} (pin 3) to AGND	±25V
Digital Input Voltage (pins 8–25) to DGND	−0.3V, V_{DD}
V_{PIN4} to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation (Any package)	
To +75°C	1000mW
Operating Temperature Range	
Commercial Plastic (J, K Versions)	0 to +70°C
Industrial Ceramic (A, B Versions)	−25°C to +85°C
Extended Ceramic (S, T Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7536 1LSB = $\frac{2V_{REF}}{2^{14}}$

RELATIVE ACCURACY

Relative accuracy or end point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., Offset and Gain Error are adjusted out) and is normally expressed in Least Significant Bits or as a percentage of full scale range.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of +1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output with all one's loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

OFFSET ERROR

Offset error is a measure of the mismatch between R_{FB} and the internal offset resistor, R_{OFS}. It also includes the leakage component from the DAC (see Figure 8). It is present for all codes and is expressed in Least Significant Bits.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

LEAKAGE CURRENT

Leakage current flows into I_{OUT} from the 14-bit DAC when all the DAC switches are off. It contributes to the Linearity, Gain and Offset error (see Figure 8).

MULTIPLYING FEEDTHROUGH ERROR

This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded with 10 0000 0000 0000.

Pin	Function	Description
1	R_{INT}	Contact point for internal resistors R1 and R2 which perform the inverting function on V_{REF} with external op-amp. See Figure 3.
2	V_{REF}	Reference input to the DAC. It is internally connected to R_{OFS} and R1. See Figure 3.
3	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
4	I_{OUT}	Current Output Terminal.
5	A_{GNDS}	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
6	A_{GNDF}	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13. DAC MSB
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0. DAC LSB
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active LOW input.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active LOW.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input.
25	$\overline{WR}$	Write input. Active LOW.

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

26	V_{DD}	Power supply input. Specifications apply for $V_{DD} = +12V \pm 5\%$ to $+15V \pm 5\%$.
27	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 5 or 6 for recommended circuitry.
28	V_{INV}	This pin must be connected to the output of the external inverting op-amp. See Figure 3.

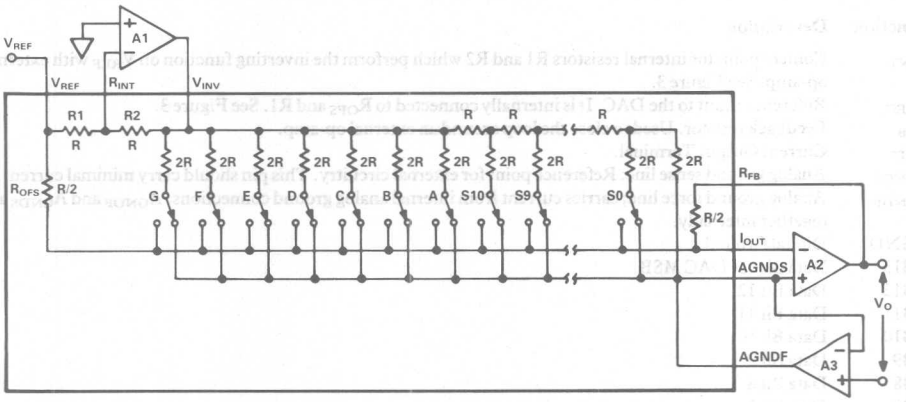


Figure 3. Simplified Circuit Diagram of the AD7536 D/A Section Showing Connection of External Op-Amps

CIRCUIT INFORMATION – D/A SECTION

Figure 3 is a simplified circuit diagram of the AD7536 D/A section and it also shows the external op-amp connection. The device is a 14-bit DAC with three extra resistors on chip for bipolar operation. It is configured so that the coding is Offset Binary. The 14-bit DAC consists of an R-2R ladder for the lower eleven bits (switches S0–S10). The three MSB's are decoded to drive switches A–G sequentially. Each of these carries an equally weighted current which is also equal to the current in the R-2R ladder. R_{OFS} has the same magnitude as R_{FB} so that the output is offset by a constant $-V_{REF}$. R1 and R2 (together with external op-amp A1) invert V_{REF} and apply it to the 14-bit DAC (V_{INV}). See Table I for complete Offset Binary Code Table.

To eliminate any slight variations in analog ground potential with changing code, there are two analog ground pins. AGNDF sinks all the current flowing through the switches to ground while AGNDS is used as a reference point with minimal current flowing in it. Figure 3 shows A3 maintaining AGNDS at Signal Ground. The connection of AGNDS and AGNDF may be changed depending on required system accuracy and output drive requirements (see Figures 5 and 6).

EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows an equivalent output circuit for the analog section of the AD7536 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R0 denotes the equivalent output resistance of the DAC and associated resistors. This varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending on the digital input. g(V_{REF}, N) is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the circuit transfer function, N.

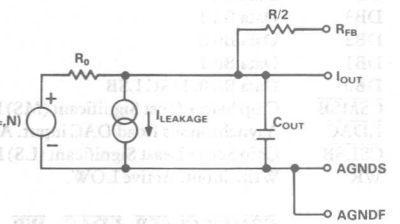


Figure 4. AD7536 Equivalent Analog Output Circuit

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

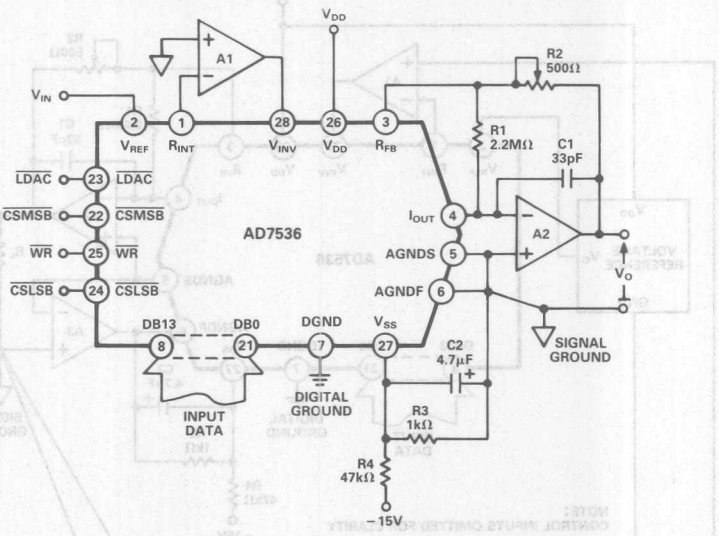


Figure 5. AD7536 Operation

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 5 shows the AD7536 connected for bipolar operation. Specified accuracy is attained without the need for expensive closely matched external resistors. R1 and R2 provide an optional gain adjustment and capacitor C1 helps prevent overshoot and ringing when high-speed op-amps are used. The −300mV bias voltage for V_{SS} is derived from R3, R4 and C2. Op-amp A3 (Figure 3 and Figure 6) is omitted from Figure 5. AGNDS and AGNDF are externally shorted to Signal Ground.

Table I shows the Offset Binary Code Table obtained with the circuit of Figure 5. It should be noted that the user can get a 2's Complement transfer function by inverting the MSB of the DAC word.

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
00 0000 0000 0001	$-V_{IN}\left(\frac{8191}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right) = -V_{IN}$

Table I. Offset Binary Code Table for AD7536

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 5.

Offset Adjustment

1. Adjust offset of amplifier A1 so that potential at R_{INT} is <10μV with respect to Signal Ground.
2. Load DAC register with 10 0000 0000 0000.
3. Adjust offset of amplifier A2 until V_O = 0V (<10μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R2 so that $V_O = +V_{IN}\frac{(8191)}{(8192)}$

For high-temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Offset Error, Full Scale Error and Gain T.C. specifications of the AD7536, trimming of the Offset and Gain is not necessary.

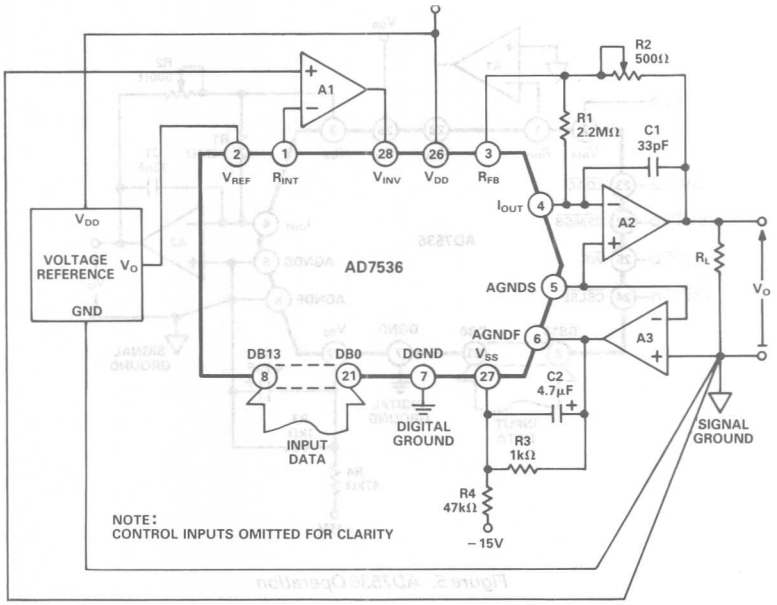


Figure 6. AD7536 Operation with Forced Ground

GROUNDING CONSIDERATIONS

In the circuits of Figures 5 and 6, with $V_{REF} = +10V$, 1LSB has a value of 1.2mV. So, factors which are not important in less accurate systems must, in this case, be given careful consideration. Among these, the whole question of grounding is crucial. Voltage reference ground, the I_{OUT} pin on the DAC, the noninverting pin of A1 and SIGNAL GROUND must all be at the same potential. Note that in Figure 5, AGNDS and AGNDF are externally shorted and A3 is not used. Voltage drops due to bond wire resistance are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used.

Here, A3 is used to maintain AGNDS at Signal Ground potential. I_{OUT} is also at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated. If A3 is not a low offset voltage (<100μV) op-amp, it should be trimmed with a potentiometer until the voltage at AGNDS is <10μV with respect to SIGNAL GROUND. Figure 7 shows how the circuit of Figure 5 might be be laid out. Gain trim components R1 and R2 have been omitted for clarity. Note how the input to V_{REF} (pin 2) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough.

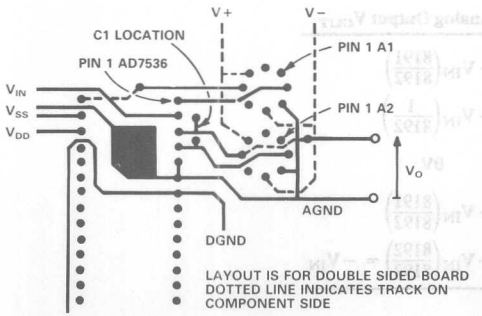


Figure 7. Suggested Layout for AD7536 Circuit of Figure 5

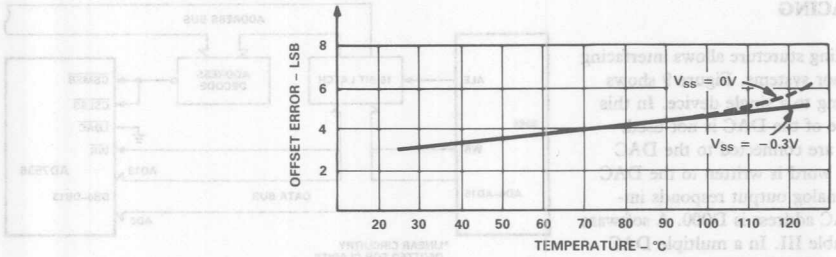


Figure 8. Typical Graph of Offset Error vs. Temperature With and Without Low Leakage Configuration

LOW LEAKAGE CONFIGURATION

Leakage current in CMOS D/A converters has two components. Current leaks from V_{DD} into the I_{OUT} line and is present at all DAC codes. There is also leakage across the off switches in the DAC. The polarity of this current depends on V_{INV} and its magnitude is related to the code in the DAC register. At high temperatures (above 90°C) it is normal for the leakage current to increase dramatically. By its nature it will affect all critical dc parameters (Linearity Error, Gain Error and Offset Error). The AD7536 features a leakage reduction configuration (patent pending) to keep the leakage current low (typically <10nA) over an extended temperature range. This ensures that the DAC maintains its 25°C performance very well at temperatures up to 125°C.

The AD7536 can be operated with or without the leakage reduction configuration. If V_{SS} (pin 27) is tied to AGND, then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to −0.3V as in Figures 5 and 6. The current taken by V_{SS} is very low (<10μA) allowing a simple resistor divider (R3, R4) to produce the required −300mV from −15V. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be 4.7μF or greater. Figure 8 is a plot of Offset Error versus temperature for both conditions. It clearly shows the improvement when the low leakage configuration is used.

OP-AMP SELECTION

In choosing an amplifier to be used with the AD7536, three parameters are of prime importance. These are:

1. Input Offset Voltage (V_{OS})
2. Input Bias Current (I_B)
3. Offset Voltage Drift (TC V_{OS}).

To maintain specified accuracy with V_{REF} at 10V, A1 and A2 of Figures 5 and 6 must have V_{OS} <100μV and I_B <10nA. It is important that the amplifier Open Loop Gain, A_{VOL}, be sufficiently large to keep V_{OS} <100μV for the full output voltage range. For a maximum output of 10V, A_{VOL} must be greater than 100,000.

In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A3, without any external adjustment for V_{OS}. In low frequency or fixed reference applications where fast output settling time is not required, the AD OP-07 is also recommended for A1 and A2. Because of its low V_{OS} no external potentiometers are needed. For faster settling time, one can use the AD544 series of op-amps.

Offset Voltage Drift and Bias Current drift are critical parameters for operation over a wide temperature range. The AD OP-07, AD OP-27 and AD OP-37 all exhibit very low offset drift while the AD544 has very low bias current drift. Table II summarizes the important specifications of the op-amps mentioned above.

Op-Amp	Input Offset Voltage (V_{OS})	Input Bias Current (I_B)	Offset Voltage Drift (TC V_{OS})	Settling Time to 0.003% FS
AD544L	500μV	25pA	5μV/°C	5μs
AD OP-07H	75μV	3nA	0.6μV/°C	50μs typ
AD OP-27CH	100μV	80nA	0.6μV/°C	6μs typ
AD OP-37CH	100μV	80nA	0.6μV/°C	1μs typ
HA-2620	4mV	35nA	20μV/°C	0.8μs typ

Table II. Guide to Op-Amp Selection

MICROPROCESSOR INTERFACING

AD7536 – 8086A INTERFACE

The versatility of the AD7536 loading sturcture allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this circuit the double buffering feature of the DAC is not used. AD0-AD13 of the 16-bit data bus are connected to the DAC data bus (DB0-DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III. In a multiple DAC system the double buffering of the AD7536 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., $\overline{\text{LDAC}}$) is brought low, updating all the DACs simultaneously.

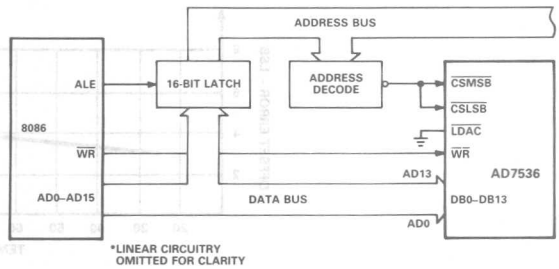


Figure 9. AD7536 – 8086 Interface Circuit

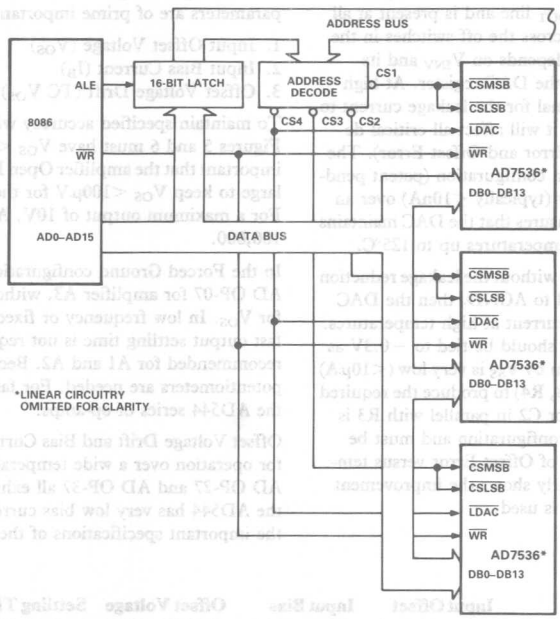


Figure 10. AD7536 – 8086 Interface: Multiple DAC System

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	:	DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	:	TO CODE SEGMENT REGISTER
04	BF00D0	MOV DI, # D000	:	LOAD DI WITH D000
07	C705"YZWX"	MOV MEM,# YZWX"	:	DAC LOADED WITH WXYZ
0B	EA0000		:	CONTROL IS RETURNED TO THE
0E	00FF			MONITOR PROGRAM

Table III. Sample Program for Loading AD7536 from 8086

AD7536 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7536 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
01000  MOVE.W   #W,D0      The desired DAC data, W, is
                           loaded into Data Register 0.
                           W may be any value between 0
                           and 16383 (decimal) or 0 and
                           3FFF (hexademical).
       MOVE.W   D0,$E000   The data W is transferred
                           between D0 and the DAC
                           Register.
       MOVE.B   #228,D7    Control is returned to the System
                           Monitor Program using these tow
       TRAP     #14        instructions.
```

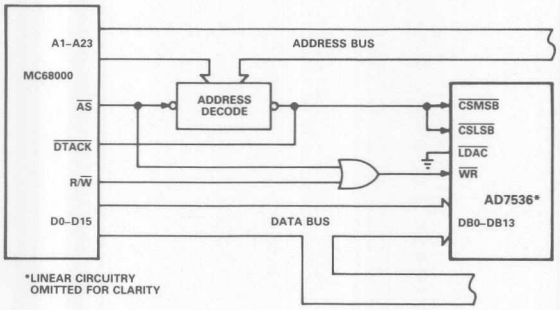


Figure 11. AD7536 – MC68000 Interface

AD7536 – Z80 INTERFACE

Though the AD7536 is ideally suited for use either with 16-bit microprocessors or in stand-alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the popular Z80 microprocessor.

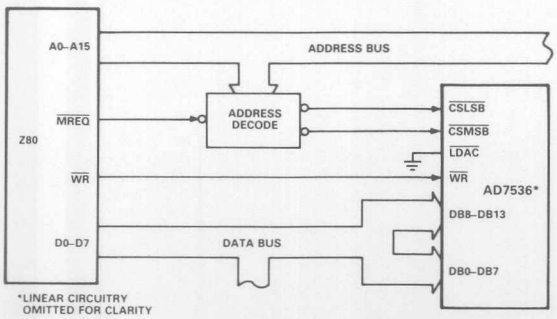


Figure 12. AD7536 – Z80 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7536 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

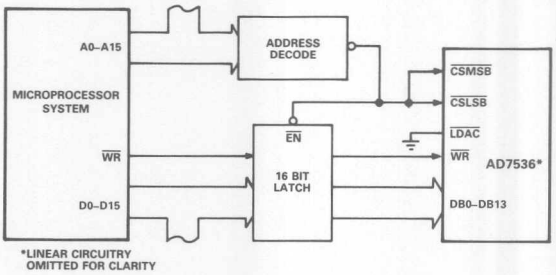


Figure 13. AD7536 Interface Circuit Using Latches to Minimize Digital Feedthrough

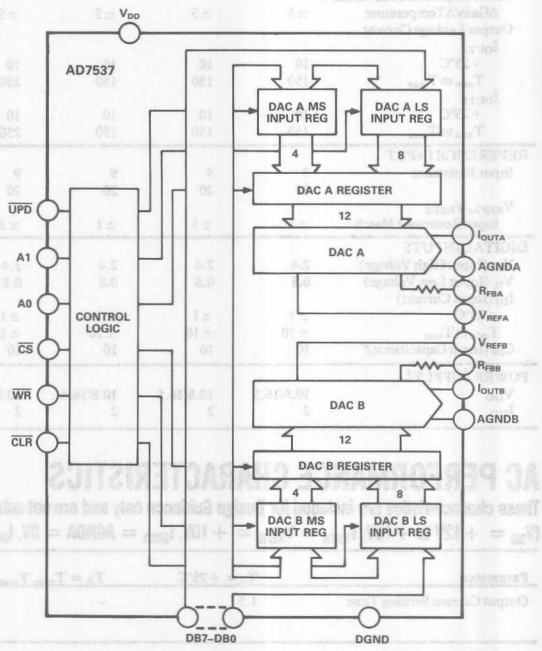
FEATURES

- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Byte Loading Structure
- Fast Interface Timing

APPLICATIONS

- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7537 contains two 12-bit current output DACs on one monolithic chip. A separate reference input is provided for each DAC. The dual DAC saves valuable board space, and the monolithic construction ensures excellent thermal tracking. Both DACs are guaranteed 12-bit monotonic over the full temperature range.

The AD7537 has a 2-byte (8LSBs, 4MSBs) loading structure. It is designed for right-justified data format. The control signals for register loading are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{UPD}$. Data is loaded to the input registers when $\overline{CS}$ and $\overline{WR}$ are low. To transfer this data to the DAC registers, $\overline{UPD}$ must be taken low with $\overline{WR}$.

Added features on the AD7537 include an asynchronous $\overline{CLR}$ line which is very useful in calibration routines. When this is taken low, all registers are cleared. The double buffering of the data inputs allows simultaneous update of both DACs. Also, each DAC has a separate AGND line. This increases the device versatility; for instance one DAC may be operated with AGND biased while the other is connected in the standard configuration.

The AD7537 is manufactured using the Linear Compatible CMOS (LC^2MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size:
   The AD7537 is packaged in small 24-pin, 0.3″ DIPs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance:
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

AD7537—SPECIFICATIONS (V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = AGND = 0V, I_{OUTB} = AGNDB = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0s
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0s
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB} Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−84	–	dB typ	V_{REFA} = 20V p-p 10kHz sine wave, V_{REFB} = 0V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	−84	–	dB typ	V_{REFB} = 20V p-p 10kHz sine wave, V_{REFA} = 0V. Both DACs loaded with all 1s.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF.
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	−82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: J, K, L Versions: −40°C to +85°C.
A, B, C Versions: −40°C to +85°C.
S, T, U Versions: −55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, $V_{REFA} = V_{REFB}$ = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V).

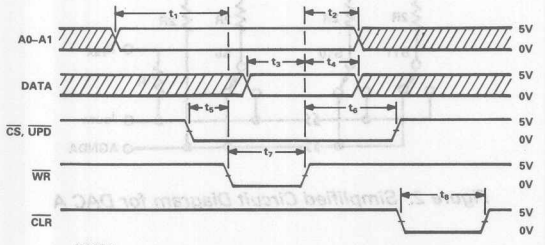
Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A −55°C to +125°C	Units	Test Conditions/Comments
t_1	15	15	30	ns min	Address Valid to Write Setup Time
t_2	15	15	25	ns min	Address Valid to Write Hold Time
t_3	60	80	80	ns min	Data Setup Time
t_4	25	25	25	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	80	80	100	ns min	Write Pulse Width
t_8	80	80	100	ns min	Clear Pulse Width

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGNDA, AGNDB . . . . . ±25V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, V_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGNDA, AGNDB to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C



NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f$ = 20ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Timing Diagram for AD7537

Operating Temperature Range
Commercial Plastic (J, K, L Versions) . . . . −40°C to +85°C
Industrial Hermetic (A, B, C Versions) . . . . −40°C to +85°C
Extended Hermetic (S, T, U Versions) . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7537JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7537KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7537LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7537JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7537KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7537LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7537AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7537BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7537CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7537SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7537TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7537UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7537SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7537TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7537UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

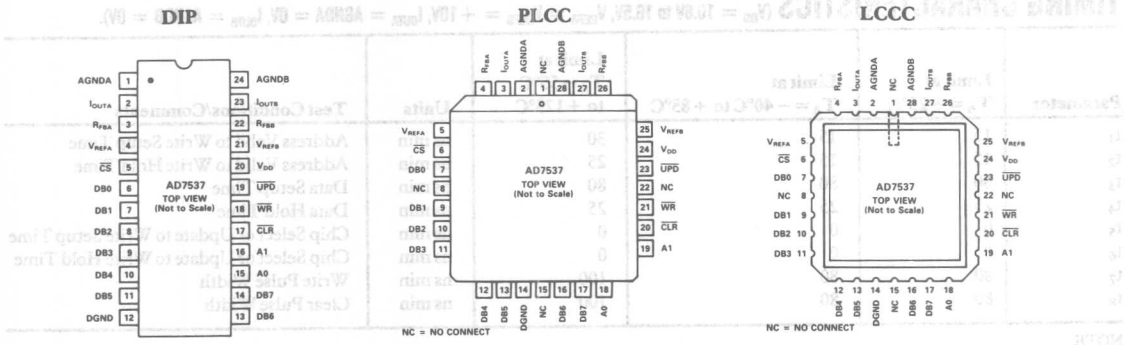
NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input. Active low.
6-14	DB0-DB7	Eight data inputs, DB0-DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally + 12V to + 15V, with ± 10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3(MSB)-DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3(MSB)-DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTE: X = Don't care

Table I. AD7537 Truth Table

CIRCUIT INFORMATION – D/A SECTION

The AD7537 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGNDA. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op amp (see Figures 4 and 5) to convert the current flowing in I_{OUTA} to a voltage output.

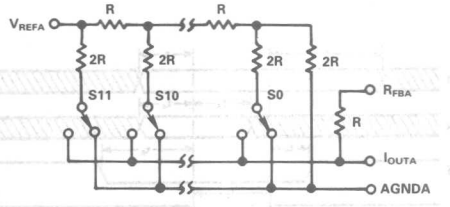


Figure 2. Simplified Circuit Diagram for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7537. A similar equivalent circuit can be drawn for DAC B.

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_0 is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA.

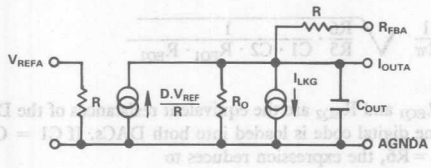


Figure 3. Equivalent Analog Circuit for DAC A

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (AD644, AD712) or separate packages (AD544, AD711, AD OP-27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7537, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 5 is given in Table III.

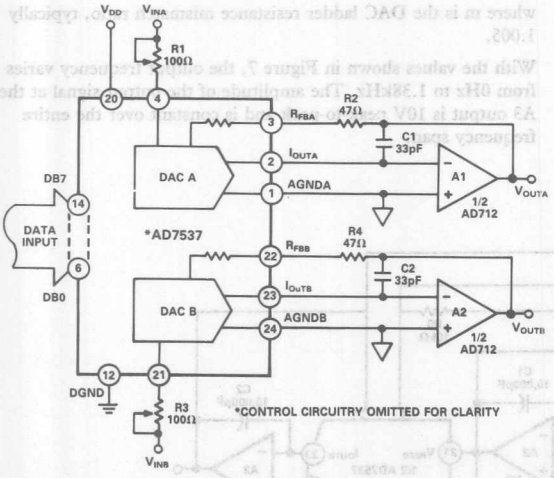


Figure 4. AD7537 Unipolar Binary Operation

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 4

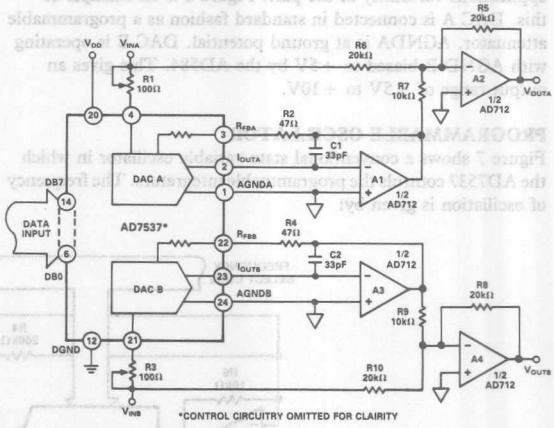


Figure 5. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

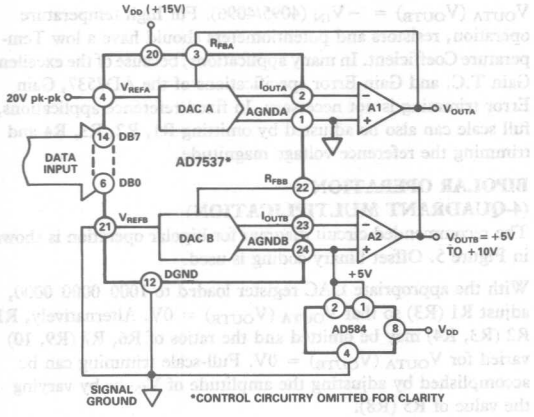


Figure 6. AD7537 DACs Used in Different Modes

SEPARATE AGND PINS

The DACs in the AD7537 have separate AGND lines taken to pins AGNDA and AGNDB on the package. This increases the applications versatility of the part. Figure 6 is an example of this. DAC A is connected in standard fashion as a programmable attenuator. AGNDA is at ground potential. DAC B is operating with AGND B biased to +5V by the AD584. This gives an output range of +5V to +10V.

PROGRAMMABLE OSCILLATOR

Figure 7 shows a conventional state-variable oscillator in which the AD7537 controls the programmable integrators. The frequency of oscillation is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}\cdot\frac{1}{C1\cdot C2\cdot R_{EQ1}\cdot R_{EQ2}}}$$

where R_{EQ1} and R_{EQ2} are the equivalent resistances of the DACs. The same digital code is loaded into both DACs. If C1 = C2 and R5 = R6, the expression reduces to

$$f = \frac{1}{2\pi}\cdot\frac{1}{C}\sqrt{\frac{1}{R_{EQ1}\cdot R_{EQ2}}}$$

Since $R_{EQ} = \frac{2^n\cdot R_{LAD}}{N}$, ($R_{LAD}$ = DAC ladder resistance).

$$f = \frac{1}{2\pi}\cdot\frac{1}{C}\sqrt{\frac{(N/2^n)^2}{R_{LAD1}\cdot R_{LAD2}}}$$

$$= \frac{1}{2\pi}\cdot\frac{D}{C}\cdot\frac{1}{\sqrt{R_{LAD1}\cdot R_{LAD2}}} \qquad D = \left(\frac{N}{2^n}\right)$$

$$= \frac{1}{2\pi}\cdot\frac{D}{C\cdot R_{LAD}\sqrt{m}}$$

where m is the DAC ladder resistance mismatch ratio, typically 1.005.

With the values shown in Figure 7, the output frequency varies from 0Hz to 1.38kHz. The amplitude of the output signal at the A3 output is 10V peak-to-peak and is constant over the entire frequency span.

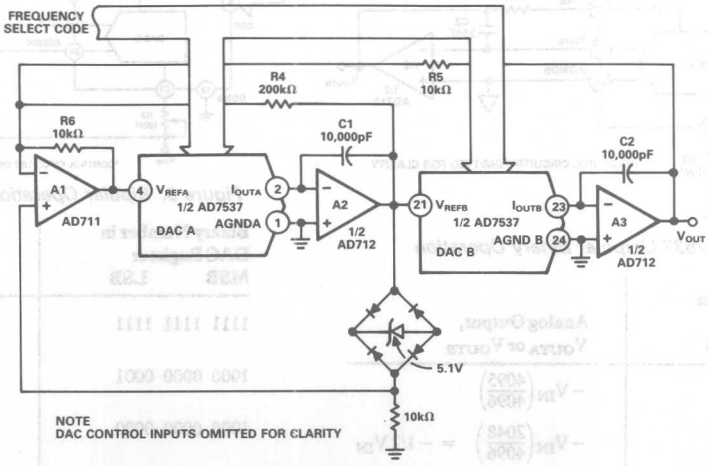


Figure 7. Programmable State Variable Oscillator

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are the AD711C and its dual version, the AD712C. These op amps have a wide bandwidth and high slew rate and are recommended for wide bandwidth ac applications. AD711/AD712 settling time to 0.01% is typically 3μs.

Temperature Coefficients: The gain temperature coefficient of the AD7537 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1 (R3) and R2 (R4) are used to adjust full scale range as in Figure 4, the temperature coefficient of R1 (R3) and R2 (R4) should also be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Application Note, Publication Number E630c-5-3/86 available from Analog Devices.

High Frequency Considerations: AD7537 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 and C2 in Figures 4 and 5.

Feedthrough: The dynamic performance of the AD7537 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 4 is shown in Figure 8 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

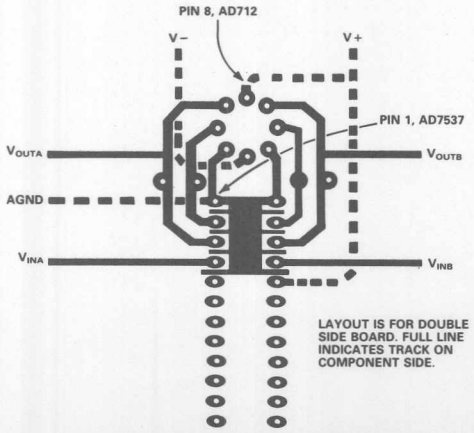


Figure 8. Suggested Layout for AD7537

MICROPROCESSOR INTERFACING

The byte loading structure of the AD7537 makes it very easy to interface the device to any 8-bit microprocessor system. Figures 9 and 10 show two interfaces: one for the MC6809 and the other for the MC68008. Figure 11 shows how an AD7537 system can be easily expanded by tying all the $\overline{UPD}$ lines together and using a single decoder output to control these. This expanded system is shown using a Z80 microprocessor but it is just as easily configured using any other 8-bit microprocessor system. Note how the system shown in Figure 11 produces 4 analog outputs with a minimum amount of hardware.

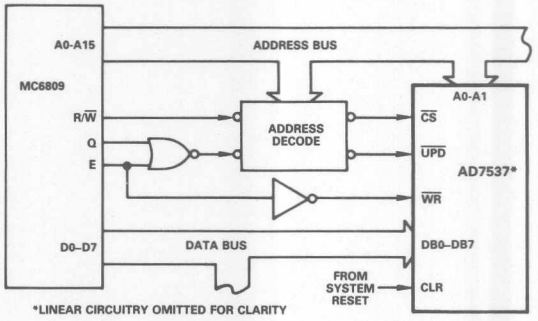


Figure 9. AD7537 – MC6809 Interface

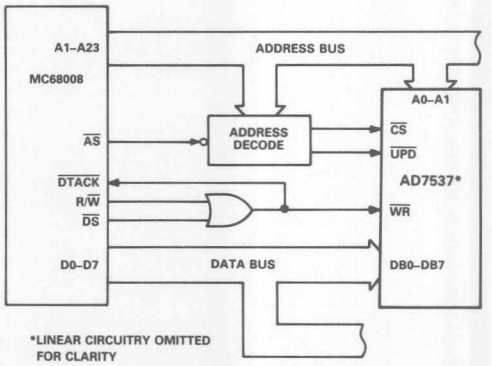


Figure 10. AD7537 – MC68008 Interface

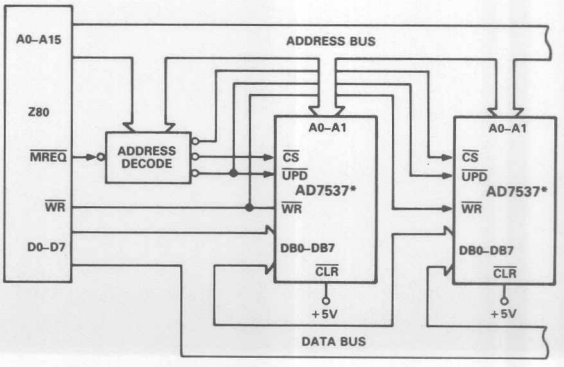


Figure 11. Expanded AD7537 System



LC²MOS
µP-Compatible 14-Bit DAC

AD7538

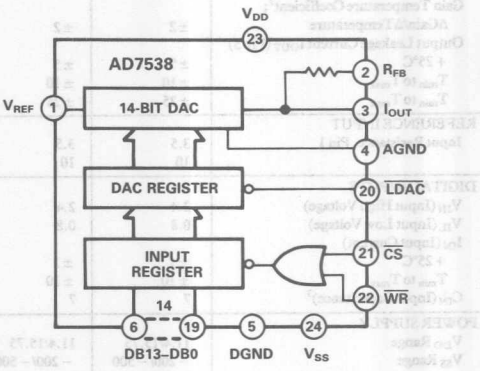
FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Cost 14-Bit Upgrade for 12-Bit Systems
- 14-Bit Parallel Load with Double Buffered Inputs
- Small 24-Pin, 0.3″ DIP and SOIC
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7538 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

The DAC is loaded by a single 14-bit wide word using standard Chip Select and Memory Write Logic. Double buffering, which is optional using $\overline{\text{LDAC}}$, allows simultaneous update in a system containing multiple AD7538s.

A novel low leakage configuration (U.S. Patent No. 4,590,456) enables the AD7538 to exhibit excellent output leakage current characteristics over the specified temperature range.

The AD7538 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7538 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Cost
   The AD7538, with its 14-bit dynamic range, affords a low cost solution for 12-bit system upgrades.
3. Small Package Size
   The AD7538 is packaged in a small 24-pin, 0.3″ DIP and a 24-pin SOIC.
4. Low Output Leakage
   By tying V_{SS} (Pin 24) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
5. Wide Power Supply Tolerance
   The device operates on a +12 to +15V V_{DD}, with a ±5% tolerance on this nominal figure. All specifications are guaranteed over this range.

Parameter	J Versions	K Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full-Scale Error						Measured using internal R_{FB}
+25°C	±4	±4	±4	±4	LSB max	DAC registers loaded with
T_{min}–T_{max}	±8	±5	±10	±6	LSB max	all 1s.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±2	±2	±2	±2	ppm/°C typ	
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD711 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	20	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.
Multiplying Feedthrough Error	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0s.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1s
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0s
Output Noise Voltage Density (10Hz – 100kHz)	15	–	nV$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Sample tested to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	$\overline{LDAC}$ Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} (Pin 23) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 24) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 6–22)
to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{PIN3} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

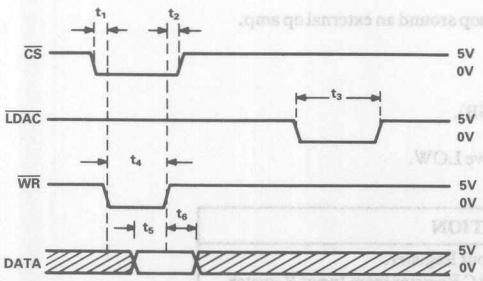
Operating Temperature Range
Commercial (J, K versions) . . . . . 0 to +70°C
Industrial (A, B versions) . . . . . −25°C to +85°C
Extended (S, T versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



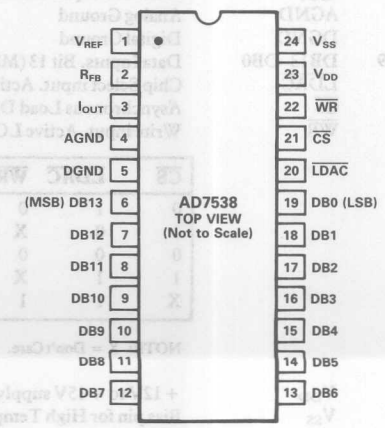


NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURES FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. If $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 or LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7538 Timing Diagram

PIN CONFIGURATION

DIP, SOIC



TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

DIGITAL-TO-ANALOG GLITCH IMPULSE
The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0s.

MULTIPLYING FEEDTHROUGH ERROR
This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option*
AD7538JN	0°C to +70°C	±2LSB	±8LSB	N-24
AD7538KN	0°C to +70°C	±1LSB	±4LSB	N-24
AD7538JR	0°C to +70°C	±2LSB	±8LSB	R-24
AD7538KR	0°C to +70°C	±1LSB	±4LSB	R-24
AD7538AQ	−25°C to +85°C	±2LSB	±8LSB	Q-24
AD7538BQ	−25°C to +85°C	±1LSB	±4LSB	Q-24
AD7538SQ	−55°C to +125°C	±2LSB	±8LSB	Q-24
AD7538TQ	−55°C to +125°C	±1LSB	±4LSB	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{REF}	Voltage Reference.
2	R_{FB}	Feedback resistor. Used to close the loop around an external op amp.
3	I_{OUT}	Current Output Terminal.
4	AGND	Analog Ground
5	DGND	Digital Ground
6–19	DB13–DB0	Data Inputs. Bit 13 (MSB) to Bit 0 (LSB).
20	$\overline{LDAC}$	Chip Select input. Active LOW.
21	$\overline{CS}$	Asynchronous Load DAC input. Active LOW.
22	$\overline{WR}$	Write input. Active LOW.

$\overline{CS}$	$\overline{LDAC}$	$\overline{WR}$	OPERATION
0	1	0	Load Input Register.
1	0	X	Load DAC Register from Input Register.
0	0	0	Input and DAC Registers are transparent
1	1	X	No operation.
X	1	1	No operation.

NOTE: X = Don't Care.

23	V_{DD}	+12V to +15V supply input.
24	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4 and 5 for recommended circuitry.

D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7538 D/A section. The three MSBs of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSBs of the Data Word consist of an R-2R ladder operated in a current steering configuration.

CIRCUIT INFORMATION

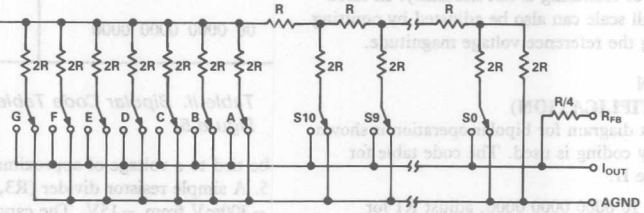


Figure 2. Simplified Circuit Diagram for the AD7538 D/A Section

The R-2R ladder current is 1/8 of the total reference input current. 7/8 I flows in the parallel ladder structure. Switches A-G steer equally weighted currents between I_{OUT} and AGND.

Since the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7538 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

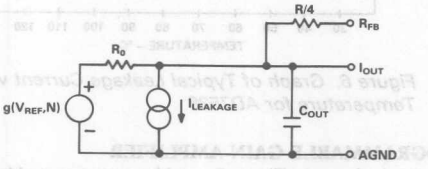


Figure 3. AD7538 Equivalent Analog Output Circuit

DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used.

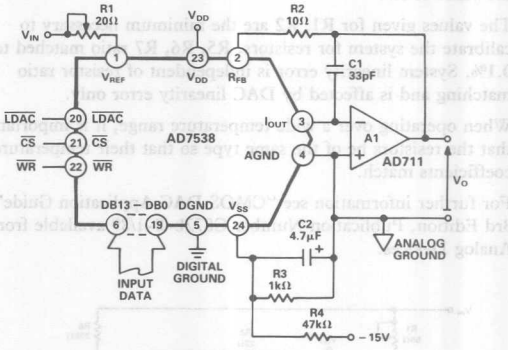


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB 11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7538

0s and amplifier offset (V_{OS}) adjusted so that V_{OUT} is 0V. Adjusting V_{OUT} to 0V is not necessary in many applications, but it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) to maintain specified DAC accuracy (see Applications Hints).

Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 so that $V_{OUTA} = -V_{IN}(16383/16384)$. For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7538, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used. The code table for Figure 5 is given in Table II.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0V$. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0V$. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

The values given for R1, R2 are the minimum necessary to calibrate the system for resistors, R5, R6, R7 ratio matched to 0.1%. System linearity error is independent of resistor ratio matching and is affected by DAC linearity error only.

When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

For further information see "CMOS DAC Application Guide", 3rd Edition, Publication Number G872b–8–1/89 available from Analog Devices.

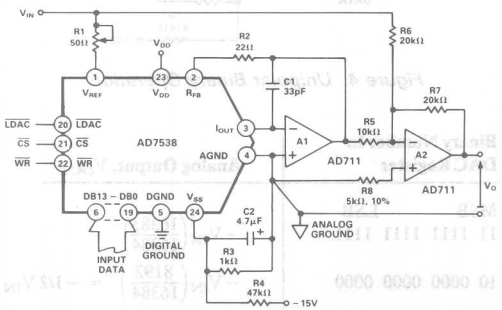


Figure 5. Bipolar Operation

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures, the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7538 features a leakage reduction configuration (U.S. Patent No. 4,590,456) to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (Pin 24) is tied to AGND then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should

DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

be tied to a voltage of approximately −0.3V as in Figures 4 and 5. A simple resistor divider (R3, R4) produces approximately −300mV from −15V. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be 4.7μF or greater. Figure 6 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

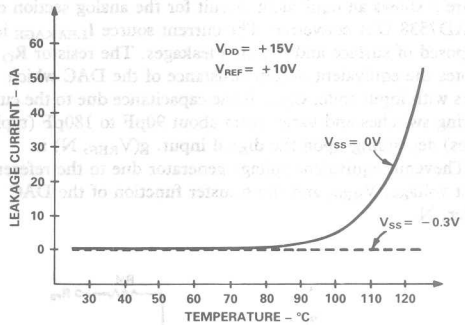


Figure 6. Graph of Typical Leakage Current vs. Temperature for AD7538

PROGRAMMABLE GAIN AMPLIFIER

The circuit shown in Figure 7 provides a programmable gain amplifier (PGA). In it the DAC behaves as a programmable resistance and thus allows the circuit gain to be digitally controlled.

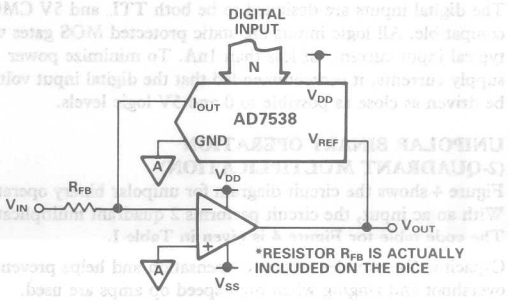


Figure 7. Programmable Gain Amplifier (PGA)

The transfer function of Figure 7 is:

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = -\frac{R_{EQ}}{R_{FB}} \quad (1)$$

R_{EQ} is the equivalent transfer impedance of the DAC from the V_{REF} pin to the I_{OUT} pin and can be expressed as

$$R_{EQ} = \frac{2^n R_{IN}}{N} \quad (2)$$

Where: n is the resolution of the DAC

N is the DAC input code in decimal

R_{IN} is the constant input impedance of the DAC ($R_{IN} = R_{LAD}$)

Substituting this expression into Equation 1 and assuming zero gain error for the DAC ($R_{IN} = R_{FB}$) the transfer function simplifies to

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{N} \quad (3)$$

The ratio $N/2^n$ is commonly represented by the term D and, as such, is the fractional representation of the digital input word.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{N} = \frac{-1}{D} \quad (4)$$

Equation 4 indicates that the gain of the circuit can be varied from 16,384 down to unity (actually 16,384/16,383) in 16,383 steps. The all 0s code is never applied. This avoids an open-loop condition thereby saturating the amplifier. With the all 0s code excluded there remains $2^n - 1$ possible input codes allowing a choice of $2^n - 1$ output levels. In dB terms the dynamic range is

$$20 \log_{10} \frac{V_{OUT}}{V_{IN}} = 20 \log_{10} (2^n - 1) = 84\text{dB}.$$

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10V, it is recommended that V_{OS} be no greater than 0.25mV, or (25×10^{-6}) (V_{REF}), over the temperature range of operation. The AD711 is a suitable op amp. The op amp has a wide bandwidth and high slew rate and is recommended for ac and other applications requiring fast settling.

General Ground Management: Since the AD7538 is specified for high accuracy, it is important to use a proper grounding technique. AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7538. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7538 AGND and DGND pins (1N914 or equivalent).

MICROPROCESSOR INTERFACING

The AD7538 is designed for easy interfacing to 16-bit microprocessors and can be treated as a memory mapped peripheral. This reduces the amount of external logic needed for interfacing to a minimal.

AD7538-8086 INTERFACE

Figure 8 shows the 8086 processor interface to a single device. In this setup the double buffering feature (using $\overline{\text{LDAC}}$) of the DAC is not used. The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately.

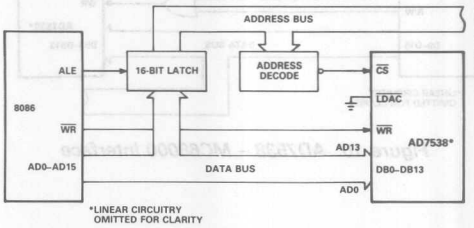


Figure 8. AD7538 – 8086 Interface Circuit

In a multiple DAC system the double buffering of the AD7538 allows the user to simulatenously update all DACs. In Figure 9, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., LDAC) is brought low, updating all the DACs simultaneoulsy.

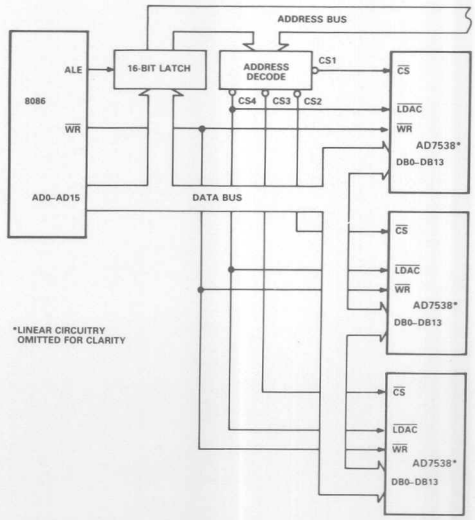


Figure 9. AD7538 – 8086 Interface: Multiple DAC System

AD7538-MC68000 INTERFACE

Figure 10 shows the MC68000 processor interface to a single device. In this setup the double buffering feature of the DAC is not used and the appropriate data is written into the DAC in one MOVE instruction.

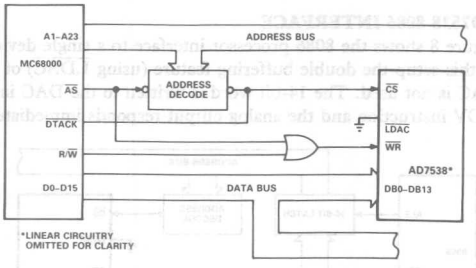


Figure 10. AD7538 – MC68000 Interface

DIGITAL FEEDTHROUGH

The digital inputs to the AD7538 are directly connected to the microprocessor bus in the preceding interface configurations. These inputs will be constantly changing even when the device is not selected. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 11 shows an interface circuit which uses this technique. All data inputs are latched from the bus by the $\overline{CS}$ signal. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

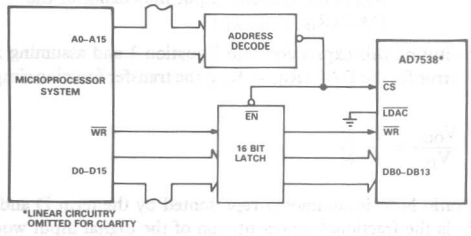
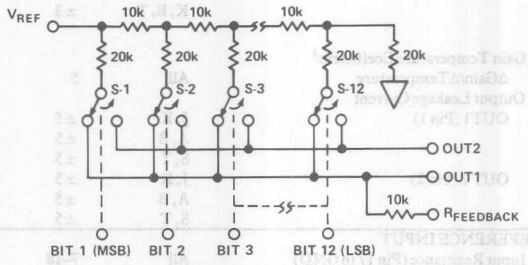


Figure 11. AD7538 Interface Circuit Using Latches to Minimize Digital Feedthrough

FEATURES

- Improved Version of AD7541
- Full Four Quadrant Multiplication
- 12-Bit Linearity (End-Point)
- All Parts Guaranteed Monotonic
- TTL/CMOS Compatible
- Low Cost
- Protection Schottky Not Required
- Low Logic Input Leakage

FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The Analog Devices' AD7541A is a low cost, high performance 12-bit monolithic multiplying digital to analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and is available in a standard 18-pin DIP and in 20-terminal surface mount packages.

The AD7541A is functionally and pin compatible with the industry standard AD7541 device and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output Schottky protection diodes are required.

This new device uses laser wafer trimming to provide full 12-bit end-point linearity with several new high performance grades.

PRODUCT HIGHLIGHTS

Compatability: The AD7541A can be used as a direct replacement for any AD7541–type device. As with the Analog Devices AD7541, the digital inputs are TTL/CMOS compatible and have been designed to have a ±1μA maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced with premium grade versions having a maximum gain error of ±3LSB.
2. Gain Error temperature coefficient has been reduced to 2ppm/°C typical and 5ppm/°C maximum.
3. Digital to analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.
5. Improvements in laser wafer trimming provides 1/2LSB max differential nonlinearity for top grade devices over the operating temperature range (vs. 1LSB on older 7541 types).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy T_{min} to T_{max}	Gain Error T_A = +25°C	Package Options[3]
AD7541AJN	0 to +70°C	±1LSB	±6LSB	N-18
AD7541AKN	0 to +70°C	±1/2LSB	±1LSB	N-18
AD7541AJP	0 to +70°C	±1LSB	±6LSB	P-20A
AD7541AKP	0 to +70°C	±1/2LSB	±1LSB	P-20A
AD7541AAQ	−25°C to +85°C	±1LSB	±6LSB	Q-18
AD7541ABQ	−25°C to +85°C	±1/2LSB	±1LSB	Q-18
AD7541ASQ	−55°C to +125°C	±1LSB	±6LSB	Q-18
AD7541ATQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-18
AD7541ASE	−55°C to +125°C	±1LSB	±6LSB	E-20A
AD7541ATE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-18) or cerdip (Q-18) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

AD7541A—SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V; OUT 1 = OUT 2 = GND = 0V unless otherwise specified)

Parameter	Version	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1LSB = ±0.024% of Full Scale
	K, B, T	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of Full Scale
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic
	K, B, T	±1/2	±1/2	LSB max	to 12 bits, T_{min} to T_{max}
Gain Error	J, A, S	±6	±8	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±3	±5	LSB max	effect of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	5	5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
OUT 2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical input resistance = 11kΩ.
					Typical input resistance temperature coefficient = −300ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates. I_{IN} typ (25°C) = 1nA.
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	%per% max	ΔV_{DD} = ±5%
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
		100	500	μA max	All digital inputs 0V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are Included for Design Guidance Only and are not Subject to Test.
V_{DD} = +15V, V_{IN} = +10V except where stated, OUT 1 = OUT 2 = GND = 0V, Output Amp is AD544 except where stated.

Parameter	Version[1]	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input					OUT 1 Load = 100Ω C_{EXT} = 13pF
Change to 90% of Final Analog Output)	All	100	–	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL TO ANALOG GLITCH IMPULSE					V_{REF} = 0V. All digital inputs 0V to V_{DD} or V_{DD} to 0V.
	All	1000	–	nV-sec typ	Measured using Model 50K as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR[3]					
(V_{REF} to OUT1)	All	1.0	–	mV p-p typ	V_{REF} = ± 10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	–	μs typ	To 0.01% of full scale range.
					OUT1 load = 100Ω, C_{EXT} = 13pF.
					Digital inputs = 0V to V_{DD} or V_{DD} to 0V
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	$= V_{IH}$
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	$= V_{IL}$

NOTES
[1]Temperature range as follows: J, K versions: 0 to +70°C
A, B versions: −25°C to +85°C
S, T versions: −55°C to +125°C.
[2]Guaranteed by design but not production tested.
[3]To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	+17V
V_{REF} to GND	±25V
V_{RFB} to GND	±25V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial (J, K versions)	0 to +70°C
Industrial (A, B versions)	−25°C to +85°C
Extended (S, T versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal maximum output is $-\left(\frac{4095}{4096}\right)(V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 4, 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

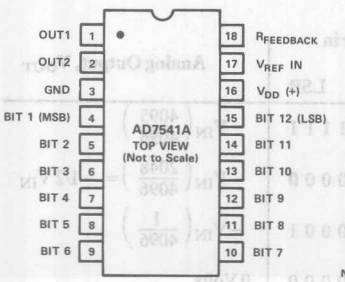
This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL-TO-ANALOG CHARGE INJECTION (QDA)

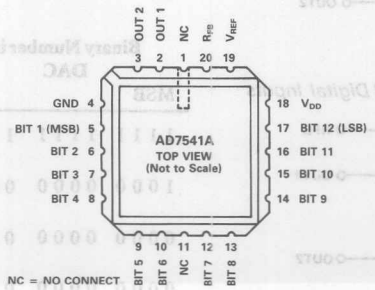
This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0pF.

PIN CONFIGURATIONS

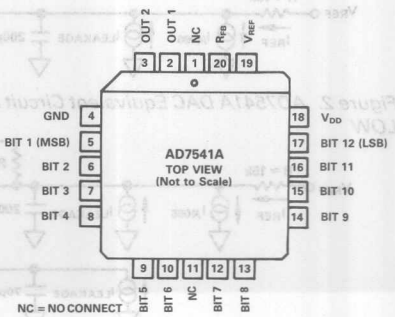
DIP



LCCC



PLCC



GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used–that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

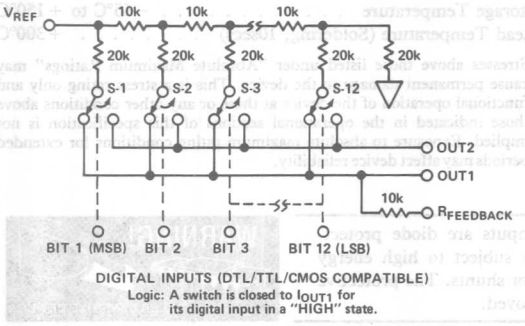


Figure 1. AD7541A Functional Diagram (Inputs "High")

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 2 and 3. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 70pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 3 is similar to Figure 2; however, the "ON" switches are now on terminal OUT1, hence the 200pF at that terminal.

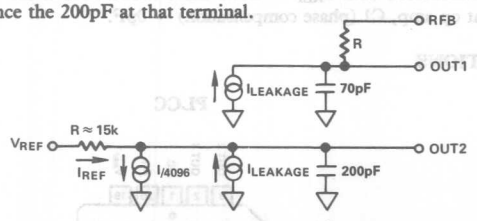


Figure 2. AD7541A DAC Equivalent Circuit All Digital Inputs LOW

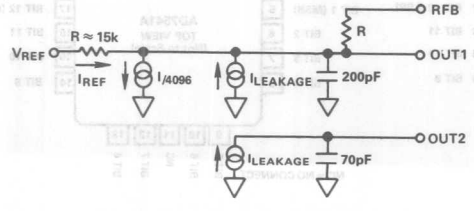


Figure 3. AD7541A DAC Equivalent Circuit All Digital Inputs HIGH

Applications

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.–load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq$ 10% of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 11kΩ). The AD544L is a high-speed implanted FET-input op amp with low factory-trimmed V_{OS}.

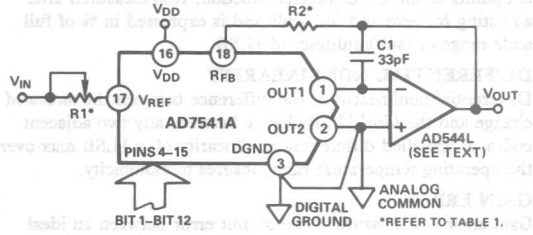


Figure 4. Unipolar Binary Operation

Trim Resistor	JN/AQ/SD	KN/BQ/TD
R1	100Ω	100Ω
R2	47Ω	33Ω

Table I. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
1111	1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000	0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000 0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference the circuit provides full 4-quadrant multiplication.

With the DAC loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 50pF) may be required for stability, depending on amplifier used.

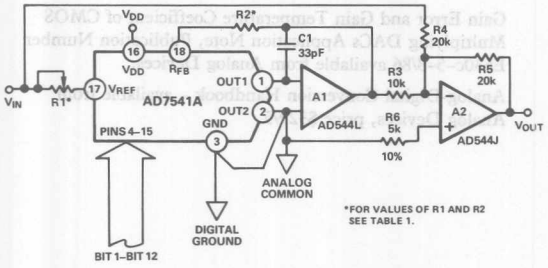


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
1111	1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

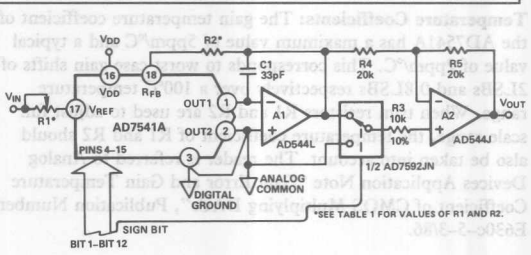


Figure 6. 12-Bit Plus Sign Magnitude Operation

Sign Bit	Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
0	1111	1111 1111	$+V_{IN} \cdot \left(\frac{4095}{4096}\right)$
0	0000	0000 0000	0 Volts
1	0000	0000 0000	0 Volts
1	1111	1111 1111	$-V_{IN} \cdot \left(\frac{4095}{4096}\right)$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Digital Glitches: One cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This should be minimized by screening the analog pins of the AD7541A (pins 1, 2, 17, 18) from the digital pins by a ground track run between pins 2 and 3 and between pins 16 and 17 of the AD7541A. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and GND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7541A, particularly in circuits with high currents and fast rise and fall times.

Temperature Coefficients: The gain temperature coefficient of the AD7541A has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630c–5–3/86.

SINGLE SUPPLY OPERATION

Figure 7 shows the AD7541A connected in a voltage switching mode. OUT1 is connected to the reference voltage and OUT2 is connected to GND. The D/A converter output voltage is available at the V_{REF} pin (pin 17) and has a constant output impedance equal to R_{LDR}. The feedback resistor R_{FB} is not used in this circuit.

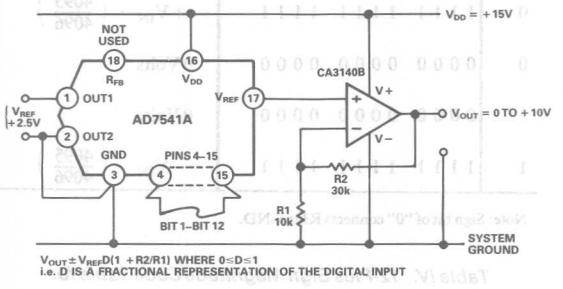


Figure 7. Single Supply Operation Using Voltage Switching Mode

The reference voltage must always be positive. If OUT1 goes more than 0.3V less than GND an internal diode will be turned on and a heavy current may flow causing device damage (the AD7541A is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices). Suitable references include the AD580 and AD584.

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltage at OUT1 should remain within 2.5V of GND, for a V_{DD} of 15V. If V_{DD} is reduced from 15V or the reference voltage at OUT1 increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

CMOS DAC Application Guide, Publication Number G872b–8–1/89 available from Analog Devices.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs Application Note, Publication Number E630c–5–3/86 available from Analog Devices.

Analog-Digital Conversion Handbook – available from Analog Devices, price $32.95.

CMOS 12-Bit Monolithic Multiplying CMOS D/A Converter

PM-7541A

FEATURES

- 7541 with Improved Accuracy and Ruggedness
- ±1/2 LSB Max Nonlinearity Over Full Temp. Range (12-Bit Linearity)
- ±1 LSB Max Gain Error – No User Adjustment Required
- Less Than 0.03 LSB Max Zero Scale Error (5nA)
- Low Gain Tempco ..... 5ppm/°C Max
- All Data Input Pins Designed with ESD Protective Circuitry
- Full Four-Quadrant Multiplication
- Low Power Consumption
- Low Feedthrough Error and Digital Charge Injection
- Superior Power Supply Rejection
  From +5V to +15V ..... .001%% Max
- Direct Replacement for AD7541 and AD7541A
- Both DIP Packages Suitable for Auto-Insertion, Surface Mount Packaging Available
- Available in Die Form

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generators
- Digitally-Controlled Attenuators
- Digitally-Controlled Power Supplies
- Digitally-Controlled Filters

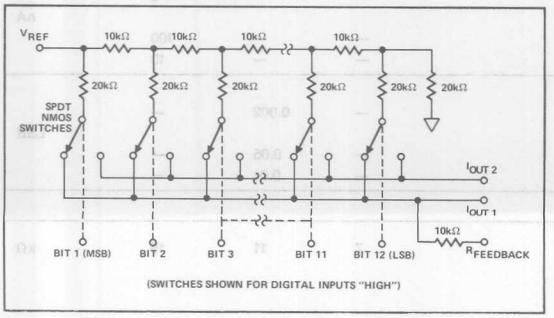
GENERAL DESCRIPTION

PMI's PM-7541A is a 12-bit resolution, current output, 4-quadrant multiplying digital-to-analog converter. Manufactured with advanced oxide-isolated, silicon-gate, monolithic CMOS technology, the PM-7541A features circuitry designed to protect data inputs against damage from electrostatic discharges.

Laser-trimmed thin-film resistors provide true 12-bit linearity with excellent absolute accuracy. The PM-7541A's low power dissipation, along with NMOS temperature compensating switches, insures high performance across the full temperature range.

The PM-7541A is a superior pin-compatible replacement for the industry standard 7541 and the AD7541A. Available in standard plastic and CerDIP packages, the PM-7541A is compatible with automatic insertion equipment. The improved performance of the PM-7541A permits upgrading existing designs with greater ruggedness and accuracy. Tighter linearity and gain error specifications may permit reduced system parts count by eliminating trimming circuitry.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

GAIN ERROR	NON-LINEARITY	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	±1/2 LSB	PM7541AAX	PM7541AEX	PM7541AGP
±2 LSB	±1/2 LSB	PM7541ABX	PM7541AFX	–
±2 LSB	±1/2 LSB	PM7541ABRC/883	PM7541AFP	–
±2 LSB	±1/2 LSB	–	PM7541AFPC	–
±2 LSB	±1/2 LSB	–	PM7541AFS	–

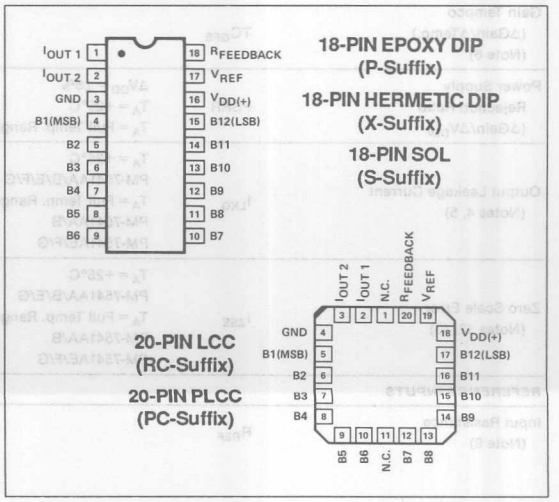
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7541AAX PM7541ABX	AD7541ATD AD7541ASD	MIL
PM7541AEX PM7541AFX	AD7541ABQ AD7541AAQ	IND
PM7541GP PM7541FPC PM7541AFP	AD7541AKN AD7541AKP AD7541AJN	COM

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) ..... ±17V
V_{REF} (to GND) ..... ±25V
V_{RFB} (to GND) ..... ±25V
Digital Input Voltage Range ..... V_{DD} to GND
Operating Temperature Range
AX/BX/ARC/BRC Versions ..... –55°C to +125°C
EX/FX/FP/FPC/FS Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W
18-Pin Plastic DIP (P)	70	30	°C/W
20-Contact LCC (RC)	88	33	°C/W
18-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +15V, V_{REF} = +10V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; T_A = –55°C to +125°C apply for PM-7541AAX/BX/ARC/BRC; T_A = –40°C to +85°C apply for PM-7541AEX/FX/FP/FPC/FS; and T_A = 0°C to +70°C apply for PM-7541AGP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	LSB
Nonlinearity (Note 1)	INL		—	—	±1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7541AA/E/G	—	—	±1/2	LSB
		PM-7541AB/F	—	—	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				LSB
		PM-7541AA/E/G	—	—	1	
		PM-7541AB/F	—	—	2	
		T_A = Full Temp. Range				
		PM-7541AA/E/G	—	—	2	
		PM-7541AB/F	—	—	3	
Gain Tempco (ΔGain/ΔTemp.) (Note 6)	TC_{GFS}		—	±2	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%				%/%
		T_A = +25°C	—	—	±0.001	
		T_A = Full Temp. Range	—	—	±0.002	
Output Leakage Current (Notes 4, 5)	I_{LKG}	T_A = +25°C				nA
		PM-7541AA/B/E/F/G	—	—	5	
		T_A = Full Temp. Range				
		PM-7541AA/B	—	—	100	
		PM-7541AE/F/G	—	—	10	
Zero Scale Error (Notes 12, 13)	I_{ZSE}	T_A = +25°C				LSB
		PM-7541AA/B/E/G	—	0.002	—	
		T_A = Full Temp. Range				
		PM-7541AA/B	—	0.05	—	
		PM-7541AE/F/G	—	0.01	—	
REFERENCE INPUTS						
Input Resistance (Note 9)	R_{REF}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; T_A = –55°C to +125°C apply for PM-7541AAX/BX/ARC/BRC; T_A = –40°C to +85°C apply for PM-7541AEX/FX/FP/FPC/FS; and T_A = 0°C to +70°C apply for PM-7541AGP, unless otherwise noted. *Continued*

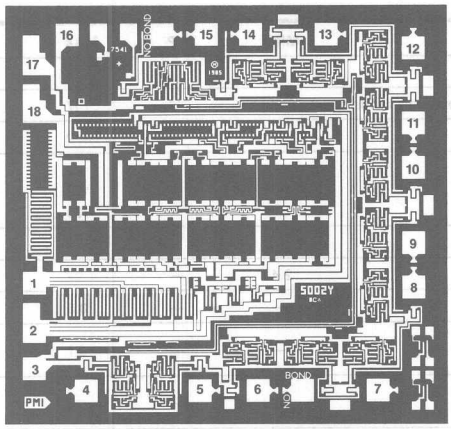
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Range	V_{DD}	Accuracy is not guaranteed over this range	+5	15	+17	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	—	—	2	mA
		Digital Inputs = 0V or V_{DD} T_A = +25°C	—	—	100	µA
		T_A = Full Temp. Range	—	—	100	
DIGITAL INPUTS						
Digital Input High	V_{IH}		2.4	—	—	V
Digital Input Low	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	V_{IN} = 0 to +15V	—	—	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	—	—	8	pF
DYNAMIC PERFORMANCE						
Propagation Delay (Notes 6, 7)	t_{PD}	From Digital Input Change to 90% of Final Analog Output T_A = +25°C	—	100	150	ns
Output Current Settling Time (Notes 6, 7, 8)	t_S	To ±1/2 LSB (±0.01% of Full Scale Range) T_A = +25°C	—	0.6	1	µs
Feedthrough Error (V_{REF} to I_{OUT}) (Note 6)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz All Digital Inputs Low T_A = +25°C	—	2	5	mV_{p-p}
Digital to Analog Glitch Energy (Notes 6, 11)	Q	T_A = +25°C	—	700	1000	nVs
ANALOG OUTPUTS						
Output Capacitance (Note 6)	$C_{OUT\,1}$	Digital Inputs = V_{IH}	—	85	120	pF
	$C_{OUT\,2}$		—	30	50	
	$C_{OUT\,1}$	Digital Inputs = V_{IL}	—	30	50	
	$C_{OUT\,2}$		—	85	120	

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to $I_{OUT\,1}$; digital inputs = V_{IL}.
5. Specification also applies for $I_{OUT\,2}$ with all digital inputs = V_{IH}.
6. Guaranteed by design and not tested.
7. I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital inputs = 0V to V_{DD} or V_{DD} to 0V.
8. Extrapolated to 1/2 LSB: t_s = Propagation Delay (t_{PD}) + 9τ, where τ = measured first time constant of the final RC decay.
9. Absolute temperature coefficient is approximately +50 ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. V_{REF} = +10V, all digital inputs = 0V.
13. Calculated from: $I_{ZSE}(\text{in LSBs}) = \frac{R_{REF}(4096)I_{LKG}}{V_{REF}}$

2

DICE CHARACTERISTICS



1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.59 × 2.54 mm, 6.58 sq. mm)

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, AGND = DGND = 0V, $V_{OUT\,1} = V_{OUT\,2} = 0V$, $T_A = +25°C$.

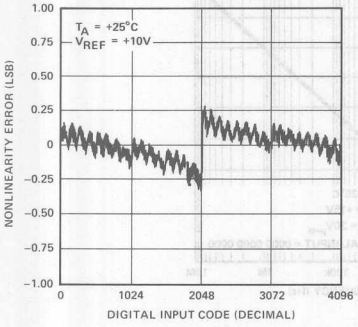
PARAMETER	SYMBOL	CONDITIONS	PM-7541AG LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error (Note 1)	G_{FSE}		±1	LSB MAX
Power Supply Rejection	PSRR	$\Delta V_{DD} = \pm 5\%$	±0.001	%/% MAX
Output Leakage Current ($I_{OUT\,1}$) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0 to 15V	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2 100	mA MAX μA MAX

NOTES:
1. Using internal feedback resistor.
2. Specification also applies for $I_{OUT\,2}$ but all Digital Inputs = V_{IH}.

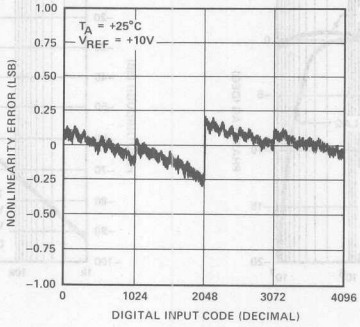
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

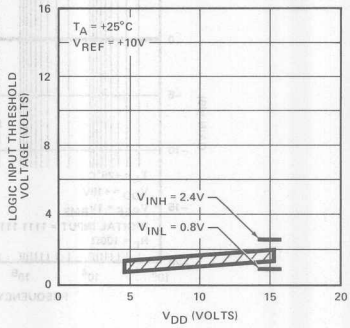
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +5V)



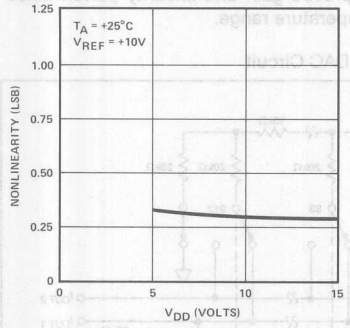
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +15V)



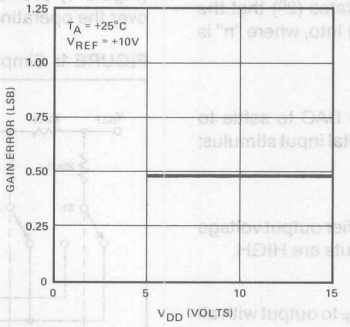
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



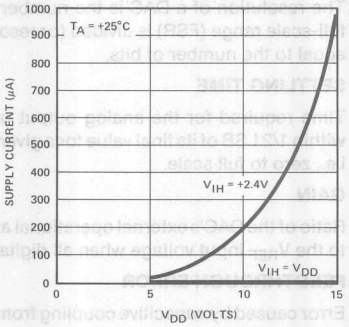
NONLINEARITY vs SUPPLY VOLTAGE



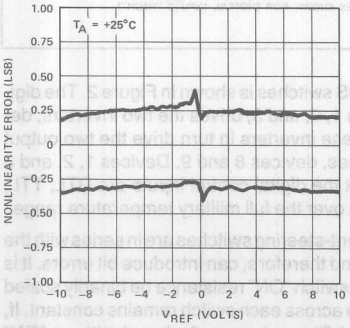
GAIN ERROR vs SUPPLY VOLTAGE



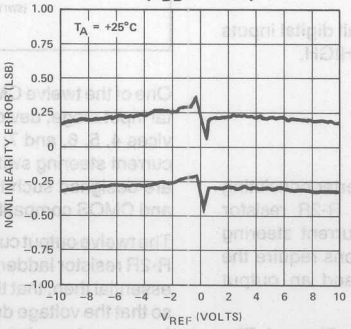
SUPPLY CURRENT vs SUPPLY VOLTAGE



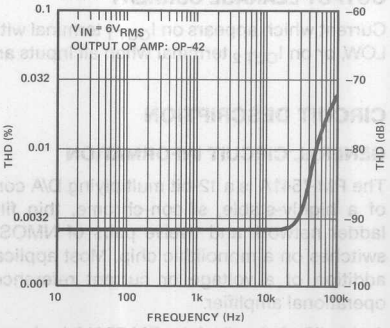
NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +5V)



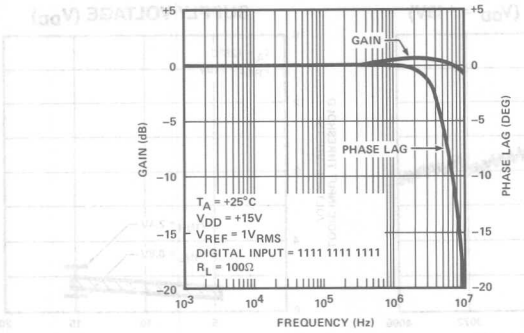
NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +15V)



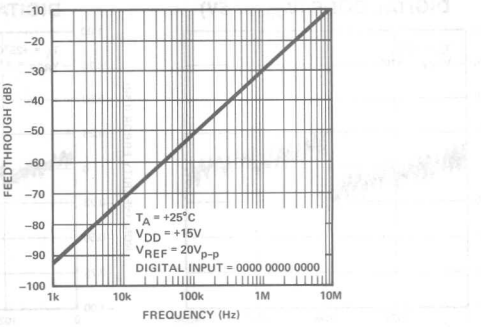
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



V_{REF} PHASE LAG AND FREQUENCY RESPONSE



FEEDTHROUGH vs FREQUENCY



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from $I_{OUT\,1}$ or $I_{OUT\,2}$ terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on $I_{OUT\,1}$ terminal with all digital inputs LOW, or on $I_{OUT\,2}$ terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

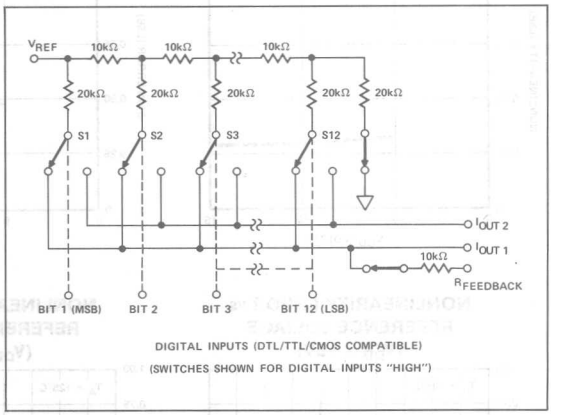
GENERAL CIRCUIT INFORMATION

The PM-7541A is a 12-bit multiplying D/A converter consisting of a highly-stable, silicon-chrome, thin film, R-2R resistor ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the PM-7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

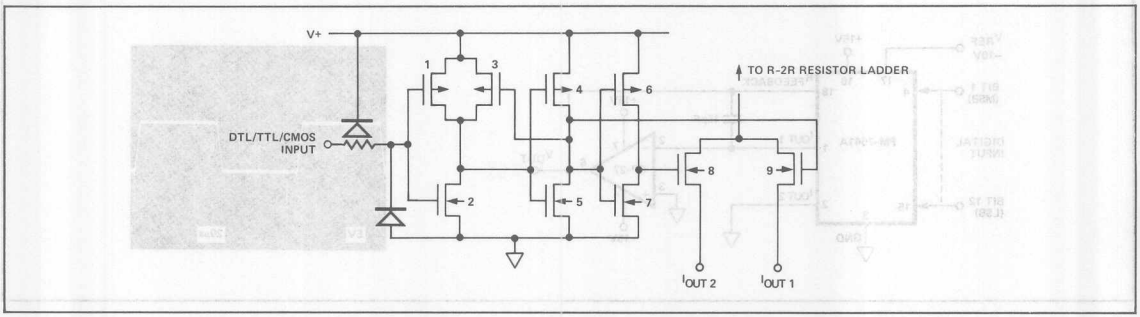
The design includes a matching switch in series with the feedback (R_{FB}) and terminating resistors. These switches (Figure 1) provide improved gain and linearity performance over the operating temperature range.

FIGURE 1: Simplified DAC Circuit



One of the twelve CMOS switches is shown in Figure 2. The digital input stage, devices 1, 2, and 3, drives the two inverters, devices 4, 5, 6, and 7; these inverters in turn drive the two output current steering switches, devices 8 and 9. Devices 1, 2, and 3 are designed such that the digital control inputs are DTL, TTL, and CMOS compatible over the full military temperature range.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 were designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.



To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

In the design of the PM-7541A's data inputs, ESD resistance has been incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes clamp the inputs well below dangerous levels during static discharge conditions.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT\ 2}$ when all inputs are LOW and $I_{OUT\ 1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore varied between the low and high values.

FIGURE 3: PM-7541A Equivalent Circuit (All Inputs LOW)

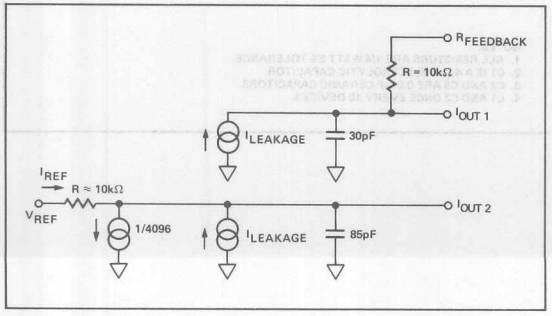
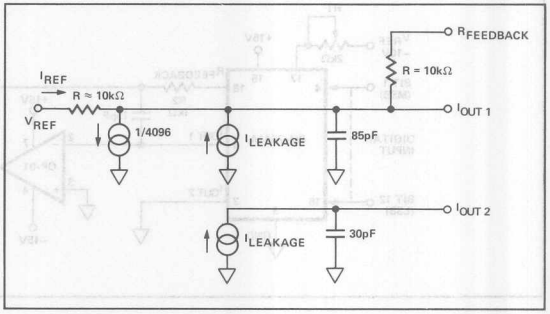


FIGURE 4: PM-7541A Equivalent Circuit (All Digital Inputs HIGH)



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the $I_{OUT\ 1}$ terminal, may be between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (See Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

FIGURE 5: Unipolar Binary Operation with High Accuracy Op Amp (2-Quadrant)

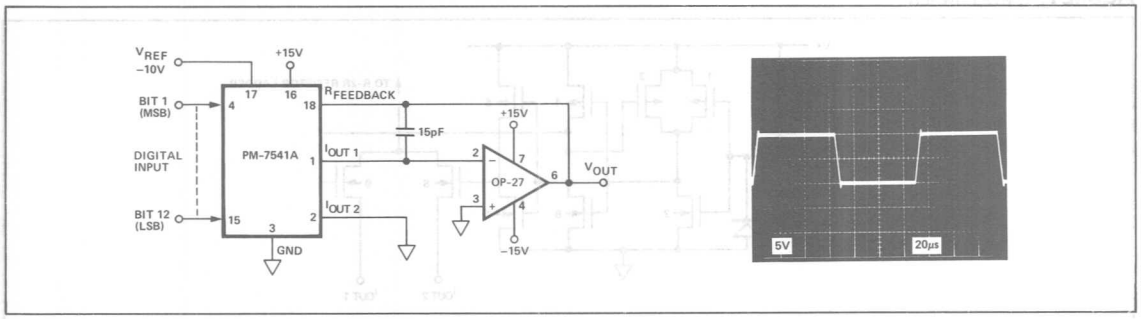
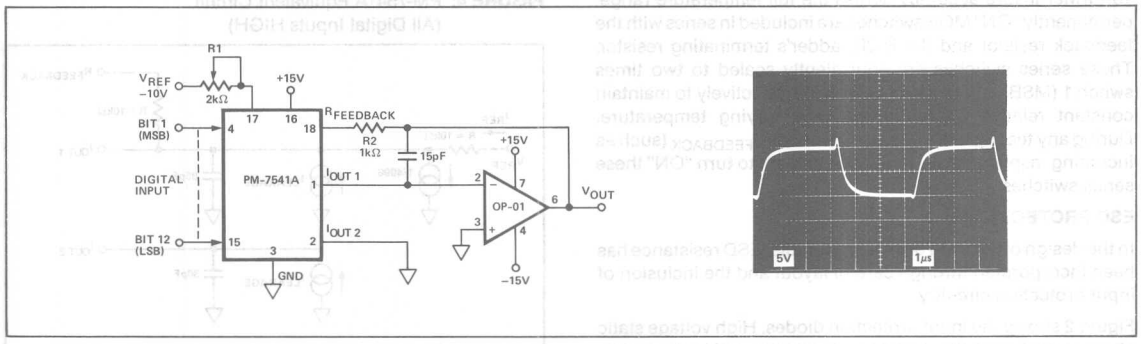
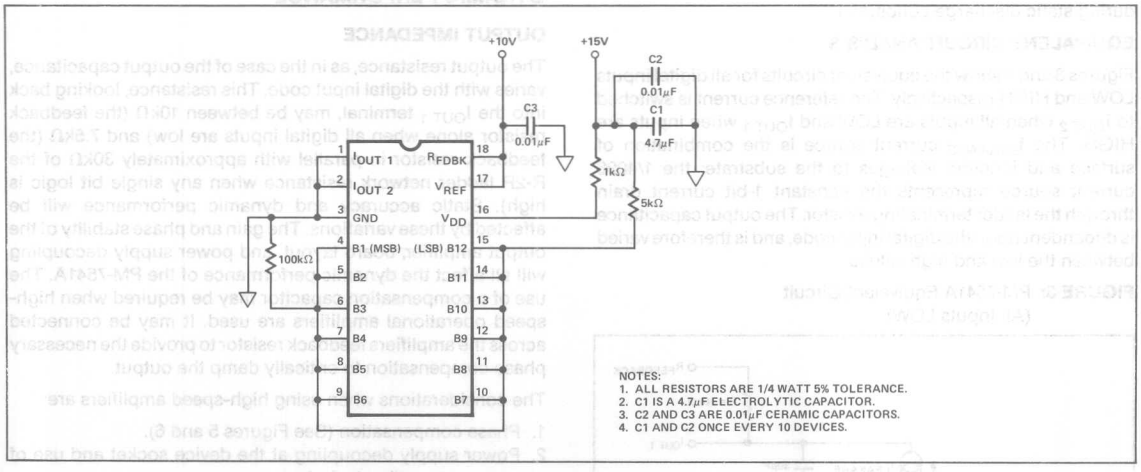


FIGURE 6: Unipolar Binary Operation with Fast Output Op Amp (2-Quadrant)



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of $I_{OUT\,1}$ and $I_{OUT\,2}$ (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e., rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 7 and the equation:

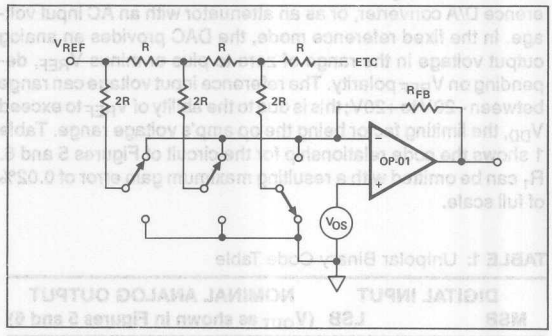
$$\text{Error Voltage} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:

$R_O \cong 10k\Omega$ for more than 4-bits of logic 1

$R_O \cong 30k\Omega$ for any single bit logic 1

FIGURE 7: Simplified Circuit



Therefore, the offset gain varies as follows:

$$\text{At code 0011 1111 1111: } V_{ERROR\,1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$$

$$\text{At code 0100 0000 0000: } V_{ERROR\,2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = \frac{4}{3}\,V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV for the PM-7541A DAC, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, and OP-27.

APPLICATIONS

Figures 5, 6, and 8 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541A and two types of PMI output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale. Low tempco (approximately 50ppm/°C) resistors or trimpots should be selected when gain adjustments are required.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can be used either as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF}, depending on V_{REF} polarity. The reference input voltage can range between –20V to +20V; this is due to the ability of V_{REF} to exceed V_{DD}, the limiting factor being the op amp's voltage range. Table 1 shows the code relationship for the circuit of Figures 5 and 6. R_1 can be omitted with a resulting maximum gain error of 0.02% of full scale.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 5 and 6)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111 1111 1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 5 and 6 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 5 and 6 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

Figure 8 shows a simple bipolar output circuit using the PM-7541A and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF}. Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF}. Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{IN} voltage or R_5. The zero-scale output voltage is adjusted while the digital inputs are set to 1000 0000 0000 by adjusting R_1 for a zero output voltage (less than 10% of 1 LSB). Resistors R_3, R_4, and R_5 must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors R_1 and R_2 temperature coefficients must be taken into account if they are used. C_1 phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

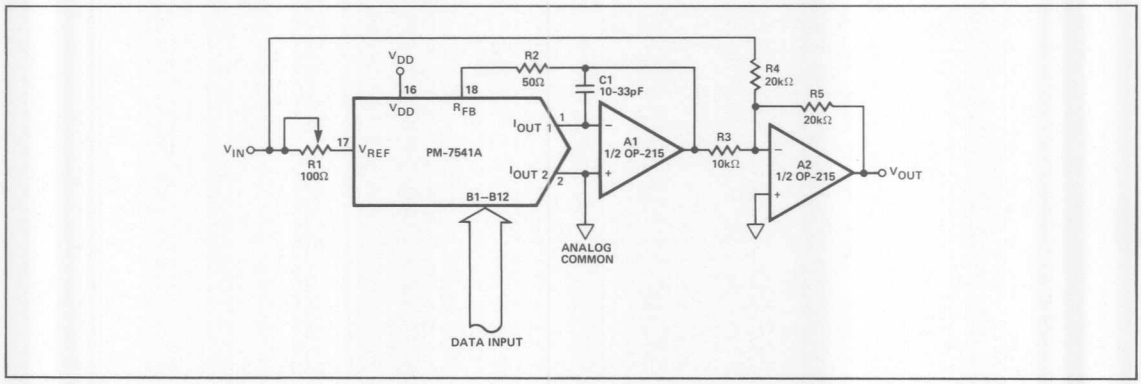
TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 8)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:

1. Nominal full scale for the circuit of Figure 8 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 8 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

FIGURE 8: Bipolar Operation (4-Quadrant Multiplication)



2

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7541A connected in the multiplying mode as shown in Figures 5 and 6 is:

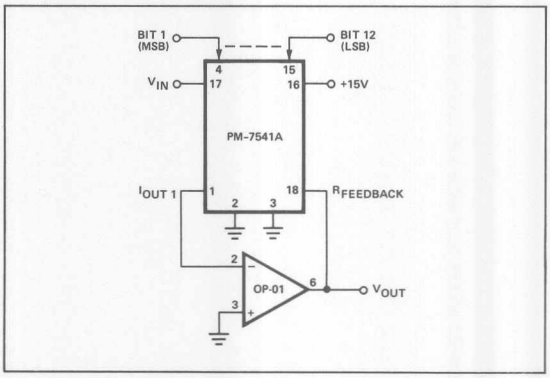
$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots\ldots\ldots \frac{A_{12}}{2^{12}}\right)$$

where A_x assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit. The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9. It now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots\ldots\ldots \frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON," the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON."

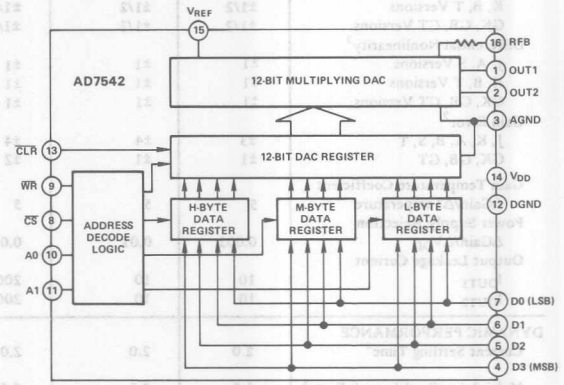
FIGURE 9: Analog/Digital Divider



FEATURES

- **Resolution: 12 Bits**
- **Nonlinearity: ±1/2LSB T_{min} to T_{max}**
- **Low Gain Drift: 2ppm/°C typ, 5ppm/°C max**
- **Microprocessor Compatible**
- **Full 4-Quadrant Multiplication**
- **Fast Interface Timing**
- **Low Power Dissipation: 40mW max**
- **Low Cost**
- **Small Size: 16-pin DIP and 20-Terminal Surface Mount Package**
- **Latch Free (Protection Schottky Not Required)**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP and 20 terminal surface mount packages) and easy μP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

AD7542—SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = −40°C to +85°C	Limit At[1] T_A = −55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
J, A, S Versions	±1	±1	±1	LSB max	
K, B, T Versions	±1/2	±1/2	±1/2	LSB max	
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
J, A, S Versions	±1	±1	±1	LSB max	All grades are guaranteed monotonic
K, B, T Versions	±1	±1	±1	LSB max	T_{min} to T_{max}
GK, GB, GT Versions	±1	±1	±1	LSB max	
Gain Error[2]					
J, K, A, B, S, T	±3	±4	±4	LSB max	Using internal R_{FB} only (gain error can be
GK, GB, GT	±1	±1	±2	LSB max	trimmed to zero using circuits of Figure 4 & 5)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1}	10	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2}	10	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB, OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+2.4	+2.4	+2.4	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (See Figures 4 and 5). Data is Loaded into Data Registers in 4-Bit Bytes.				
SWITCHING CHARACTERISTICS[5]	(See Figure 1)				
t_{WR}	80	120	160	ns min	t_{WR}: WRITE pulse width
t_{AWH}	0	10	10	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWH}	0	10	10	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{CLR}	200	200	250	ns min	t_{CLR}: Minimum CLEAR pulse width
t_{CWS}	10	20	20	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	40	40	40	ns min	t_{AWS}: Address valid-to-WRITE setup time
t_{DS}	60	100	100	ns min	t_{DS}: Data setup time
t_{DH}	10	10	10	ns min	t_{DH}: Data hold time
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1]Temperature Ranges as follows: J, K, GK Versions; −40°C to +85°C
A, B, GB Versions; −40°C to +85°C
S, T, GT Versions; −55°C to +125°C
[2]See definitions on next page.
[3]Guaranteed but not tested.
[4]Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
[5]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
V_{OUT1}, V_{OUT2} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation (Package)	
Plastic	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, GK Versions)	−40°C to +85°C
Industrial (A, B, GB Versions)	−40°C to +85°C
Extended (S, T, GT Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*COMMENTS: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Gain Error	Package Option[2]
AD7542JN	−40°C to +85°C	±1LSB	±3LSB	N-16
AD7542KN	−40°C to +85°C	±1/2LSB	±3LSB	N-16
AD7542GKN	−40°C to +85°C	±1/2LSB	±1LSB	N-16
AD7542JP	−40°C to +85°C	±1LSB	±3LSB	P-20A
AD7542KP	−40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7542GKP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7542AQ	−40°C to +85°C	±1LSB	±3LSB	Q-16
AD7542BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-16
AD7542GBQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-16
AD7542SQ	−55°C to +125°C	±1LSB	±3LSB	Q-16
AD7542TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-16
AD7542GTQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-16
AD7542SE	−55°C to +125°C	±1LSB	±3LSB	E-20A
AD7542TE	−55°C to +125°C	±1/2LSB	±3LSB	E-20A
AD7542GTE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

NOTES
[1]To order MIL-STD-883 Class B processed parts, add /883B to part number.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

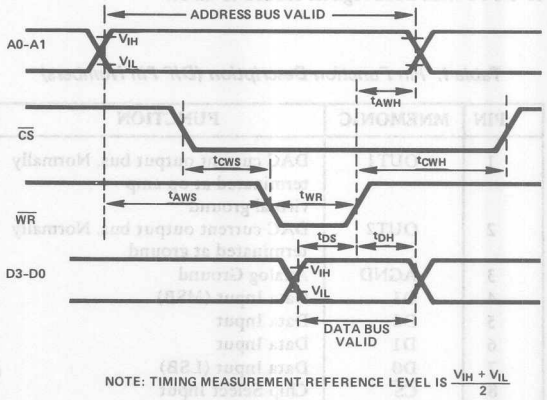
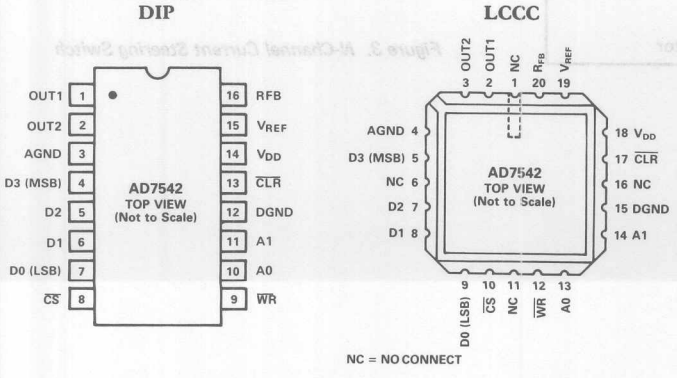


Figure 1. AD7542 Timing Diagram

PIN CONFIGURATIONS



RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

Table I. Pin Function Description (DIP Pin Numbers)

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at ground
3	AGND	Analog Ground
4	D3	Data Input (MSB)
5	D2	Data Input
6	D1	Data Input
7	D0	Data Input (LSB)
8	$\overline{CS}$	Chip Select Input
9	$\overline{WR}$	WRITE Input
10	A0	Address Bus Input
11	A1	Address Bus Input
12	DGND	Digital Ground
13	$\overline{CLR}$	Clear Input
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference Input
16	R_{FB}	DAC Feedback Resistor

GENERAL CIRCUIT INFORMATION
The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R–2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 2. An inverted R–2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

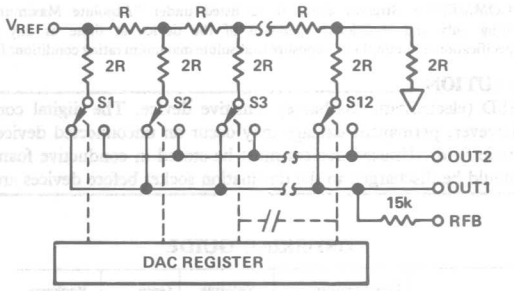


Figure 2. D/A Simplified Circuit Diagram

One of the current switches is shown in Figure 3. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient R_{FB} is recommended to define scale factor.)

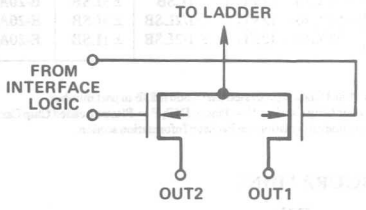


Figure 3. N-Channel Current Steering Switch

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at V_{REF}, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 33pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD711K is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

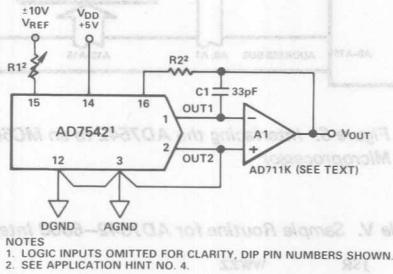


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Table II. Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the circuit provides full 4-quadrant multiplication.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

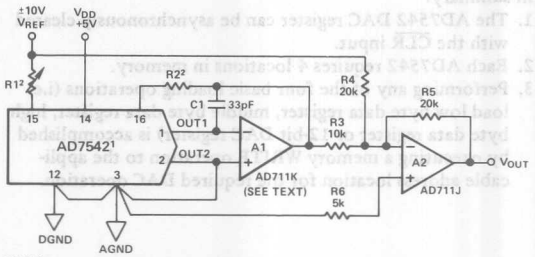


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

INTERFACE LOGIC

INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 6. $\overline{CS}$ is the decoded *device* address, and is derived by decoding the three higher order address bits. A0 and A1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e., load high byte, middle byte, low byte or DAC register). Table IV shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 1.

Additionally, the $\overline{CLR}$ input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 4), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 5), a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The AD7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

Table IV. AD7542 Truth Table

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	↓	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At $D_0 - D_3$
0	1	0	↓	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	↓	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⊓	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

NOTES:
[1] 1 indicates logic HIGH
[2] 0 indicates logic LOW
[3] X indicates don't care
[4] ↓ indicates LOW to HIGH transition
[5] MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB
[6] These control signals are level triggered.

AD7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 6. Since the AD7542 contains four registers each AD7542 is assigned four locations in memory. A0 and A1 provides the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the four addresses. Table V gives a sample loading subroutine written in re-entrant form.

Choosing an arbitrary start address of PPQQ, locations PPQQ, PPQQ+1 and PPQQ+2 select the low, middle and high byte registers respectively while address PPQQ+3 selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1.

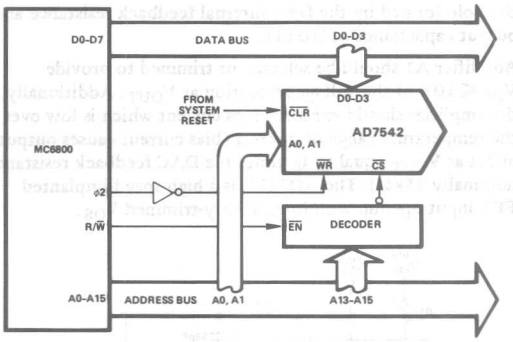


Figure 6. Interfacing the AD7542 to an MC6800 Microprocessor

Table V. Sample Routine for AD7542–6800 Interface

```
        JSR     WWZZ
WWZZ    PSH A                   PUSH ACC. A ONTO STACK
        TPA
        PSH A                   PUSH CCR ONTO STACK
        LDA A   XXYY
        STA A   PPQQ            LOAD LOW BYTE
        ROR A
        ROR A
        ROR A
        ROR A
        STA A   PPQQ+1          LOAD MIDDLE BYTE
        LDA A   XXYY+1
        STA A   PPQQ+2          LOAD HIGH BYTE
        STA A   PPQQ+3          LOAD DAC REGISTER
        PUL A
        TAP                     POP CCR FROM STACK
        PUL A                   POP ACC. A FROM STACK
        RTS                     RETURN TO MAIN PROGRAM
```

AD7542 INTERFACE TO 8085

A typical 8085 system configuration is shown in Figure 7. The AD7542 $\overline{CS}$ input is decoded from the three high order address lines A13–A15. The 8085 $\overline{WR}$ output is directly connected to the $\overline{WR}$ input of the AD7542. Table VI gives a sample loading subroutine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1. As before, arbitrary addresses PPQQ to PPQQ+3 select the low byte, middle byte, high byte and DAC registers respectively.

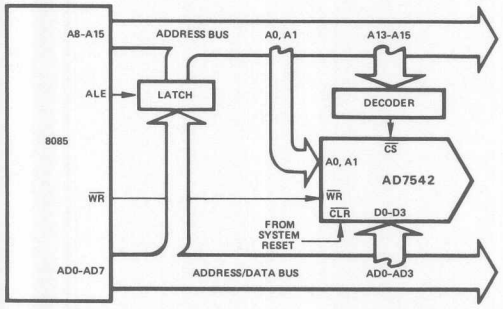


Figure 7. Interfacing the AD7542 to an 8085 Microprocessor

Table VI. Sample Routine for AD7542–8085 Interface

	CALL	7542	
7542	PUSH	PSW	PUSH REGISTER CONTENTS
	PUSH	B	ONTO STACK
	PUSH	H	
	LXI	H, XXYY	
	MOV	A, M	
	STA	PPQQ	LOAD LOW BYTE
	MVI	B, 04	
LOOP	RAR		
	DCR	B	
	JNZ	LOOP	
	STA	PPQQ+1	LOAD MIDDLE BYTE
	INX	H	
	MOV	A, M	
	STA	PPQQ+2	LOAD HIGH BYTE
	STA	PPQQ+3	LOAD DAC REGISTER
	POP	H	POP REGISTER CONTENTS
	POP	B	FROM STACK
	POP	PSW	
	RET		RETURN TO MAIN PROGRAM

APPLICATION HINTS

The AD7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7542 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7542. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7542 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a non-linearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This non-linearity term adds to the R/2R nonlinearity. To maintain specified operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = V_{REF} (2^{-n}) where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7542 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 4 and 5 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows: –

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7542 gain error specification of ±3LSBs it is recommended that R1 = 50Ω and R2 = 25Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.025}{8}(50 + 300) = 6\text{ppm/°C}$$

However, if the AD7542GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

5. For additional information on multiplying DACs refer to "CMOS DAC Application Guide," Publication Number G872a–15–4/86, available from Analog Devices.

12-Bit (4-Bit Nybble Input) Multiplying CMOS D/A Converter

PM-7542

FEATURES

- 4-Bit Bus Compatible 12-Bit Multiplying DAC
- Complete Microprocessor Interface with On-Chip Address Decoding and Asychronous CLEAR Input
- Fast Interface Timing
- Superior Accuracy: ±1/2 LSB INL Error Over Temperature and ±1 LSB Gain Error
- Excellent Power Supply Rejection ..... 0.002%% Max
- Reduced Digital Charge Injection
- Reduced Output Capacitance
- Small (16-Pin), Narrow (0.3") DIP Packages Suitable for Auto-Insertion and SO Surface Mount Package
- Improved ESD Resistance
- Superior Direct Replacement for AD7542
- Available in Die Form

APPLICATIONS

- Process Control and Industrial Automation
- Programmable Amplifiers
- Digitally-Controlled Power Supplies
- Digitally-Controlled Attenuators
- Digitally-Controlled Filters
- Instrumentation
- Avionics

ORDERING INFORMATION †

GAIN ERROR	NON-LINEARITY	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	±1/2 LSB	PM7542AQ	PM7542EQ	PM7542GP
±2 LSB	±1 LSB	PM7542BQ	PM7542FQ	–
±2 LSB	±1 LSB	PM7542BRC/883††	PM7542FP	–
±2 LSB	±1 LSB	–	PM7542FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7542AQ	AD7542GTD	MIL
PM7542AQ	AD7542TD	
PM7542BQ	AD7542SD	
PM7542EQ	AD7542GBD	IND
PM7542EQ	AD7542BD	
PM7542FQ	AD7542AD	
PM7542GP	AD7542GKN	COM
PM7542GP	AD7542KN	
PM7542FP	AD7542JN	

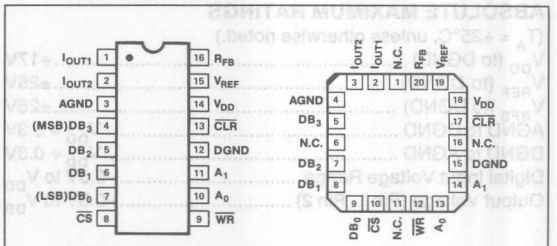
GENERAL DESCRIPTION

The PM-7542 is a 12-bit resolution, current output, multiplying CMOS DAC with a microprocessor interface to 4-bit busses. Improved analog accuracy, a fast digital interface, and input ESD protective circuitry make this a superior second-source to the industry standard 7542. This improved performance permits the easy upgrading of accuracy and ruggedness in existing designs.

Continued

2

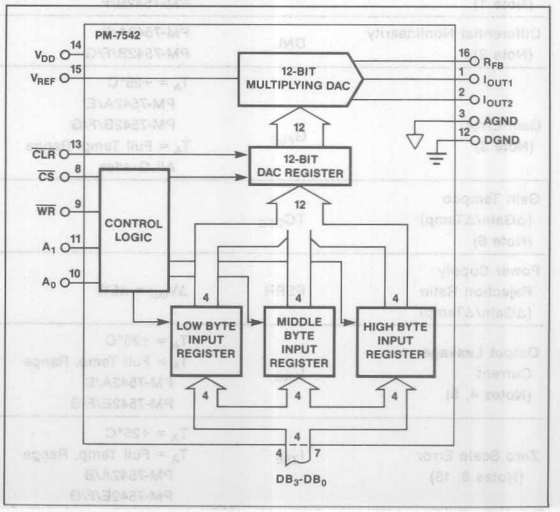
PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)
16-PIN EPOXY DIP (P-Suffix)
16-PIN SOL (S-Suffix)

20-PIN LCC (RC-Suffix)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION *Continued*

Under microprocessor control, 4-bit data bytes are loaded from a data bus into three 4-bit input registers. The resulting 12-bit data word can then be transferred to a DAC register, updating the analog output. Data input and transfer operations resemble the WRITE cycle of a static RAM. An asynchronous CLEAR input permits the immediate resetting of the DAC register to all zeros, without affecting the data resident in the input registers.

Improved linearity and gain error performance may permit a reduced circuit parts count through the elimination of trimming components. Fast interface timing reduces design considerations while minimizing microprocessor wait states. The PM-7542 is available in standard plastic and CerDIP packages that are compatible with auto-insertion equipment.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} (to DGND) ..... +17V
V_{REF} (to DGND) ..... ±25V
V_{RFB} (to DGND) ..... ±25V
AGND to DGND ..... V_{DD} + 0.3V
DGND to AGND ..... V_{DD} + 0.3V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}

Operating Temperature Range
A/B/BRC ..... –55°C to +125°C
E/F Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than AGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7542AQ/BQ; T_A = –40°C to +85°C for PM-7542EQ/FQ/FP/FS; and T_A = 0°C to +70°C for PM-7542GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	PM-7542 TYP	PM-7542 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Nonlinearity (Note 1)	INL	PM-7542A/E/G	—	—	±1/2	LSB
		PM-7542B/F	—	—	1	
Differential Nonlinearity (Note 2)	DNL	PM-7542A/E	—	—	±1/2	LSB
		PM-7542B/F/G	—	—	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				LSB
		PM-7542A/E	—	—	1	
		PM-7542B/F/G	—	—	2	
		T_A = Full Temp. Range				
		All Grades	—	—	2	
Gain Tempco (ΔGain/ΔTemp) (Note 6)	TC_{GFS}		—	—	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔTemp)	PSRR	ΔV_{DD} = ±5%	—	0.0006	±0.002	%/%
Output Leakage Current (Notes 4, 5)	I_{LKG}	T_A = +25°C	—	—	±5	nA
		T_A = Full Temp. Range				
		PM-7542A/B	—	—	±100	
		PM-7542E/F/G	—	—	±25	
Zero Scale Error (Notes 8, 13)	I_{ZSE}	T_A = +25°C	—	—	±0.02	LSB
		T_A = Full Temp. Range				
		PM-7542A/B	—	—	±0.5	
		PM-7542E/F/G	—	—	±0.1	
Input Resistance (Note 9)	R_{IN}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7542AQ/BQ; T_A = –40°C to +85°C for PM-7542EQ/FQ/FP/FS; and T_A = 0°C to +70°C for PM-7542GP, unless otherwise noted. *Continued*

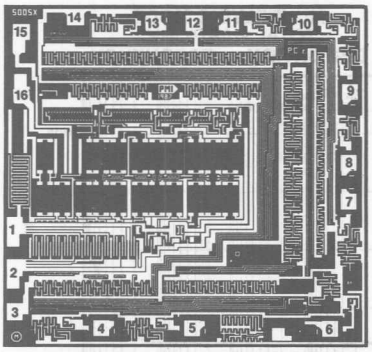
PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7)	t_s	T_A = +25°C	—	0.25	1	µs
Feedthrough Error (V_{REF} to I_{OUT1}) (Note 6)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz Digital Input = 0000 0000 0000 T_A = +25°C	—	0.45	1	mV_{p-p}
Digital to Analog Glitch Energy (Note 6)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	—	2	200	nVs
Total Harmonic Distortion (Note 6)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	—	—	–92	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz measured between R_{FB} and I_{OUT}	—	—	13	$nV/\sqrt{Hz}$
POWER SUPPLY						
Supply Voltage Range	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{IH} or V_{IL} All digital inputs = 0V or V_{DD}	— —	— —	2 0.1	mA
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	—	—	V
Digital Input LOW	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	V_{IN} = 0V to +5V	—	—	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	—	—	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IH}	— —	30 65	60 90	pF
	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IL}	— —	65 30	90 60	

for PM-7542AQ/BQ; T_A = −40°C to +85°C for PM-7542EQ/FQ/FTQ; and T_A = 0°C to 70°C for PM-7542JQ/KQ/KTQ.
Continued

PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Note 6)						
WRITE Pulse Width	t_{WR}	T_A = +25°C	90	—	—	ns
		T_A = Full Temp. Range	120	—	—	
CLEAR Pulse Width	t_{CLR}	T_A = +25°C	70	—	—	ns
		T_A = Full Temp. Range	90	—	—	
Address Valid to WRITE Hold Time	t_{AWH}	T_A = +25°C	10	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Chip Select to WRITE Hold Time	t_{CWH}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Chip Select to WRITE Set-up Time	t_{CWS}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Address Valid to WRITE Set-up Time	t_{AWS}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	
Data Set-up Time	t_{DS}	T_A = +25°C	40	—	—	ns
		T_A = Full Temp. Range	40	—	—	
Data Hold Time	t_{DH}	T_A = +25°C	40	—	—	ns
		T_A = Full Temp. Range	40	—	—	

NOTES:
1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT1}; all digital inputs = V_{IL}.
5. Specification also applies for I_{OUT2} when all digital inputs = V_{IH}.
6. Guaranteed by design and not tested.
7. I_{OUT1} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_s = Propagation Delay (t_{PD}) + 9τ. where τ = measured time constant of the final RC decay.
8. V_{REF} = +10V, all digital inputs = 0V.
9. Absolute temperature coefficient is less than +50 ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. All digital inputs = 0V.
13. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = ($R_{REF} \times I_{LKG} \times 4096$)/$V_{REF}$.
14. Calculations from $e_n = \sqrt{4K\ TRB}$ where:
    K = Boltzmann constant, J/°K R = resistance Ω
    T = resistor temperature, °K B = bandwidth, Hz

DICE CHARACTERISTICS



DIE SIZE 0.116 × 0.109 inch, 12,644 sq. mils
(2.95 × 2.77 mm, 8.17 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. DB_3 (MSB)
5. DB_2
6. DB_1
7. DB_0 (LSB)
8. $\overline{CS}$
9. $\overline{WR}$
10. A_0
11. A_1
12. DGND
13. $\overline{CLR}$
14. V_{DD} (Substrate)
15. V_{REF}
16. R_{FB}

2

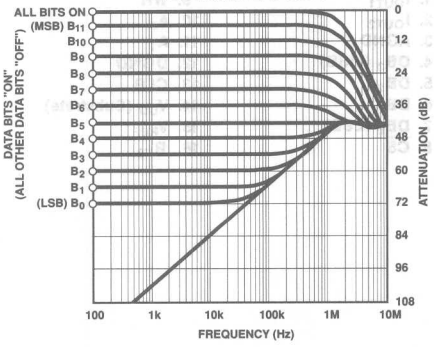
WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V, T_A = +25°C, unless otherwise noted.

			PM-7542GBC	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2 0.1	mA MAX

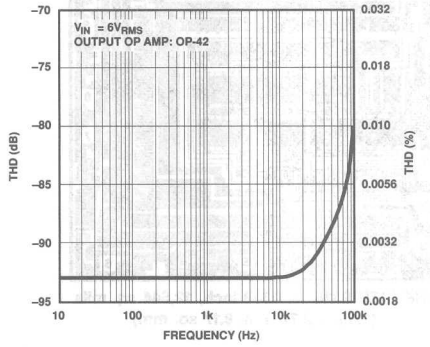
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

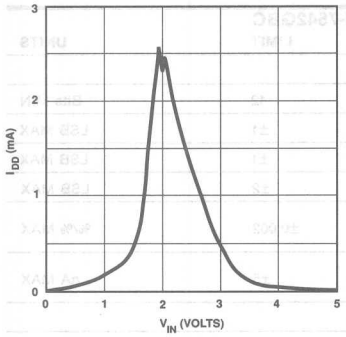
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



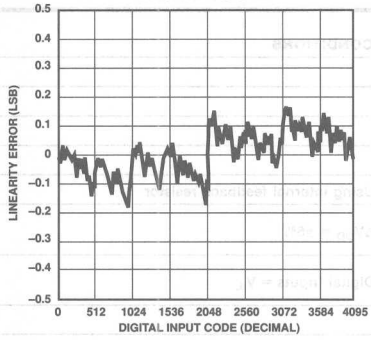
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



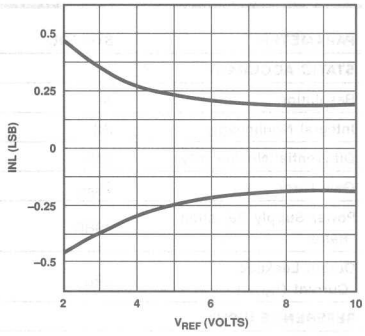
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



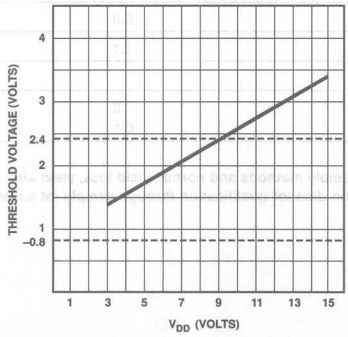
LINEARITY ERROR vs DIGITAL CODE



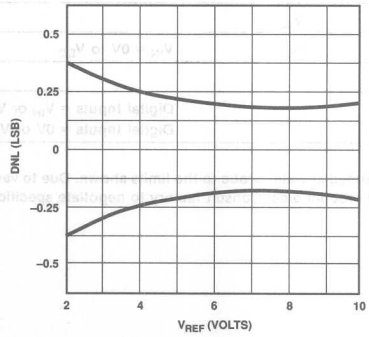
LINEARITY ERROR vs REFERENCE VOLTAGE



LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} terminal to ground with all digital inputs LOW, or from I_{OUT2} terminal to ground when all inputs are HIGH.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7542 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data input and control logic, and four data registers. The digital circuitry forms an interface between the 12-bit DAC and a four-bit data bus.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

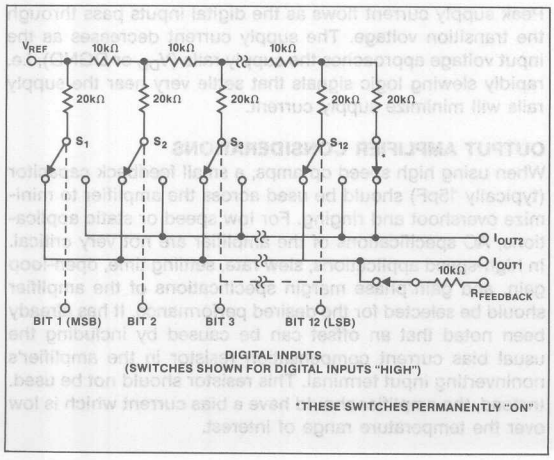


FIGURE 1: *Simplified DAC circuit*

A simplified circuit of the PM-7542 DAC is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistor, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7542 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

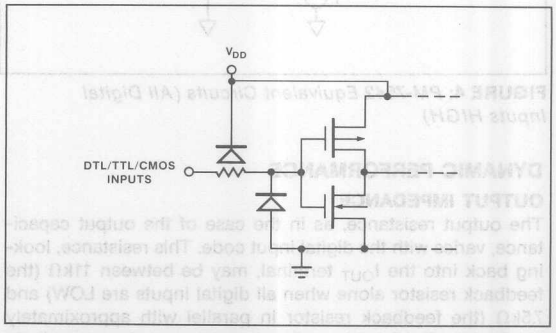


FIGURE 2: *Digital Input Protection*

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

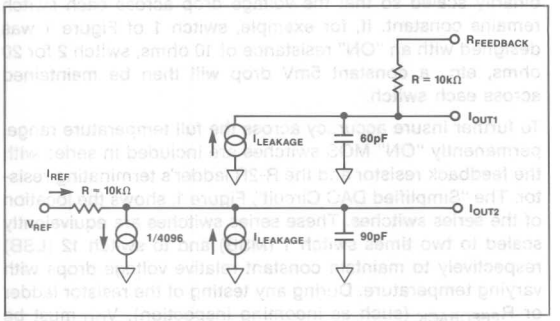


FIGURE 3: *PM-7542 Equivalent Circuit (All Inputs LOW)*

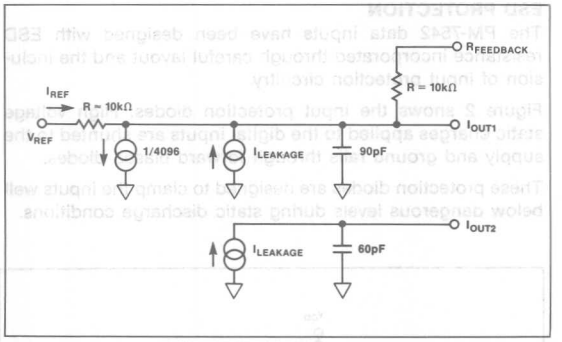


FIGURE 4: *PM-7542 Equivalent Circuits (All Digital Inputs HIGH)*

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 11kΩ (the feedback resistor alone when all digital inputs are LOW) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7542. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 8 and 9).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1}, I_{OUT2}, and AGND (pins 1, 2, and 3) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 8 and 9). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than ±200μV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital inputs resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 15pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

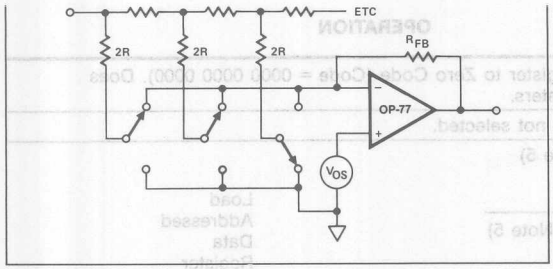


FIGURE 5: *Simplified Circuit*

Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:
$R_O = 10k\Omega$ for more than four bits of logic 1,
$R_O = 30k\Omega$ for any single bit of logic 1.

Therefore, the offset gain varies as follows:
at code 0011 1111 1111,

$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = +10V) of 2.4 mV for the PM-7542, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

INTERFACE LOGIC OPERATION

The PM-7542 has been designed to be interfaced as a memory mapped output device as shown in Figure 6.

As shown in the device truth table, Table 1, $\overline{CS}$ is an externally decoded **device** address, selecting the device when needed.

A_0 and A_1 are internally decoded **operation** addresses. Each of these four available operations requires a memory location. Data operations are performed by executing a memory WRITE to the address for that operation. This WRITE cycle is identical to that of a RAM. Updating the entire 12-bit data word requires four WRITE cycles (three data nybble loads and one data word transfer). Timing for a WRITE cycle is shown in Figure 7.

held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{REF}$.

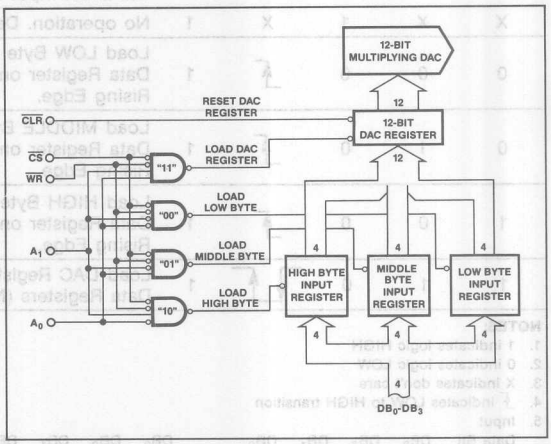


FIGURE 6: *Simplified Input Control Structure*

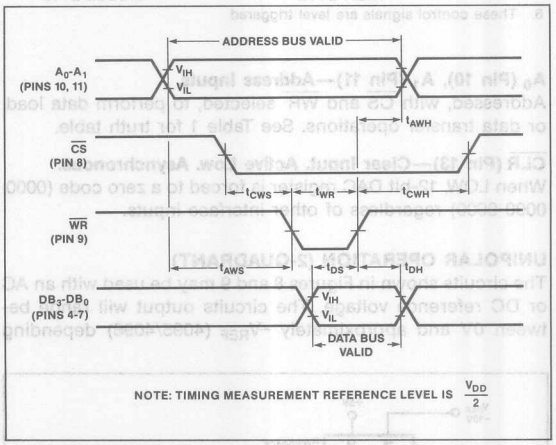


FIGURE 7: *PM-7542 Timing Diagram*

INTERFACE INPUT DESCRIPTION

$\overline{CS}$ (Pin 8)—Chip Select. Active Low.
Selected, with $\overline{WR}$, to load data into an input register or transfer data from input to DAC registers.

$\overline{WR}$ (Pin 9)—Write Input. Active Low.
Selected, with $\overline{CS}$ and appropriate address inputs, to load data into an input register or transfer data from input to DAC registers.

CONTROL INPUTS					OPERATION	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Reset 12-bit DAC Register to Zero Code (Code = 0000 0000 0000). Does not affect Input Registers.	
X	X	1	X	1	No operation. Device not selected.	
0	0	0	↓↑	1	Load LOW Byte (Note 5) Data Register on Rising Edge.	Load Addressed Data Register With Data at DB_0-DB_3.
0	1	0	↓↑	1	Load MIDDLE Byte (Note 5) Data Register on Rising Edge.	
1	0	0	↓↑	1	Load HIGH Byte (Note 5) Data Register on Rising Edge.	
1	1	0	↓↑	1	Load DAC Register with 12-Bit Data in LOW, MIDDLE, and HIGH Byte Data Registers (Note 6).	

NOTES:
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ↓↑ indicates LOW to HIGH transition
5. Input

Data Bit	DB_3	DB_2	DB_1	DB_0	DB_3	DB_2	DB_1	DB_0	DB_3	DB_2	DB_1	DB_0	
MSB→	X	X	X	X	X	X	X	X	X	X	X	X	←LSB
	HIGH BYTE				MIDDLE BYTE				LOW BYTE				

6. These control signals are level triggered

A_0 (Pin 10), A_1 (Pin 11)—Address Inputs. Addressed, with $\overline{CS}$ and $\overline{WR}$ selected, to perform data load or data transfer operations. See Table 1 for truth table.

$\overline{CLR}$ (Pin 13)—Clear Input. Active Low. Asynchronous. When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

UNIPOLAR OPERATION (2-QUADRANT)

The circuits shown in Figures 8 and 9 may be used with an AC or DC reference voltage. The circuits output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or ±25V, whichever is lowest.

Gain error may be trimmed by adjusting R_1 as shown in Figure 9. The DAC register must first be loaded with all 1s. R_1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

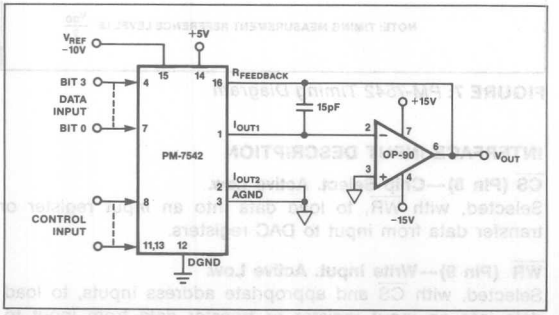


FIGURE 8: *Unipolar Operation with High Accuracy Micropower Op Amp (2-Quadrant)*

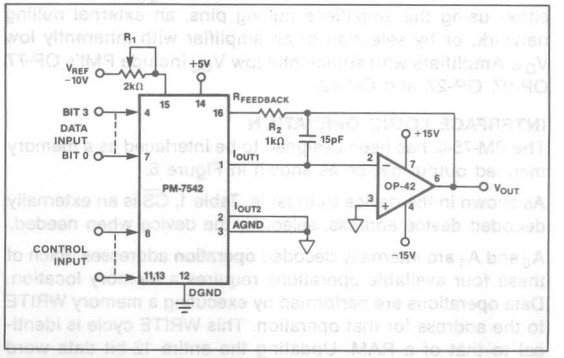


FIGURE 9: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

In many applications the PM-7542's negligible zero scale error and very low gain error permit the elimination of the trimming components (R_1 and the external $R_{FEEDBACK}$) without adverse effects on circuit performance.

TABLE 2: Unipolar Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 8 and 9)
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2049}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{2047}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:
1. Nominal full scale for the circuits of Figures 8 and 9 is given by $FS = V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 8 and 9 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$.

BIPOLAR OPERATION (4-QUADRANT)

Figure 10 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R_3 and R_4 causes offset and full scale errors while an R_5 to R_4 and R_3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted, adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 10)
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 10 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 10 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

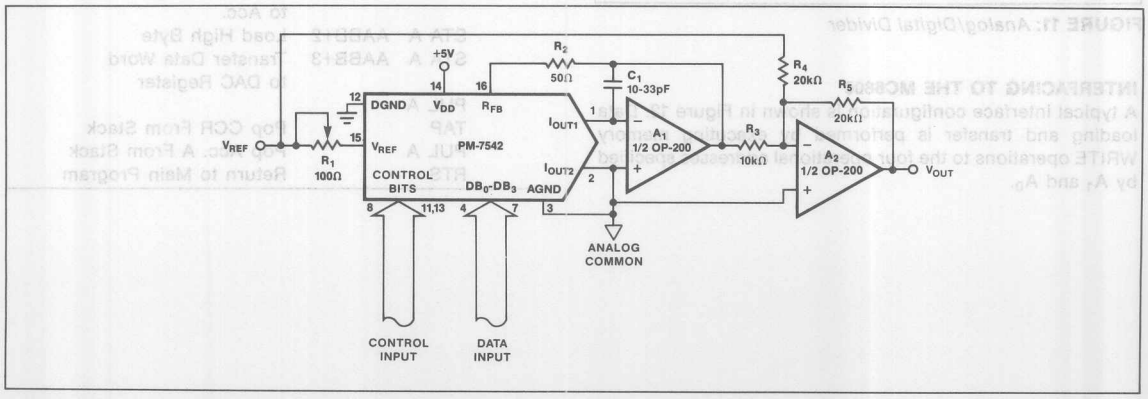


FIGURE 10: *Bipolar Operation (4-Quadrant, Offset Binary)*

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7542 connected in the multiplying mode as shown in Figures 8 and 9 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 11. It is now:

$$V_O = \frac{-V_{IN}}{\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}}$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

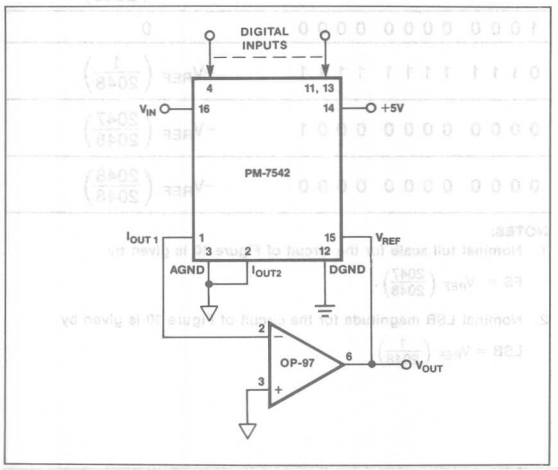


FIGURE 11: *Analog/Digital Divider*

INTERFACING TO THE MC6800

A typical interface configuration is shown in Figure 12. Data loading and transfer is performed by executing memory WRITE operations to the four operational addresses specified by A_1 and A_0.

Addresses AABB, AABB+1, and AABB+2 are assigned to load data into the low, middle, and high byte registers, respectively. Data transfer from input to DAC registers is assigned to address AABB+3. Eight bits of the full 12-bit data word are stored in memory location XXYY. The most significant data bits occupy the lower four bits of memory location XXYY+1.

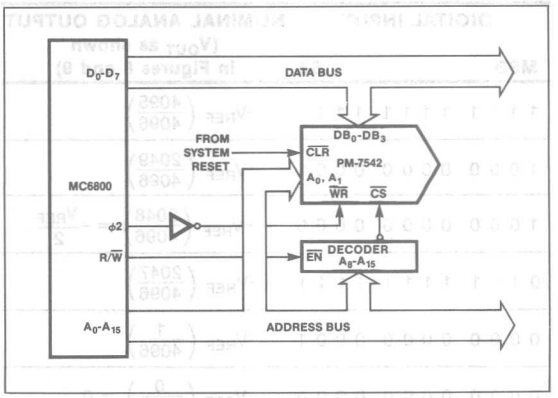


FIGURE 12: *Interfacing the PM-7542 to the MC6800*

DATA OPERATIONS SUBROUTINE

	JSR	WWZZ	Jump to Data Op Routine at WWZZ
WWZZ	PSH A		Push Acc. A Onto Stack
	TPA		
	PSH A		Push CCR Onto Stack
	LDA A	XXYY	Load Data to Acc.
	STA A	AABB	Load Low Byte
	ROR A		Rotate Right
	ROR A		
	ROR A		
	ROR A		
	STA A	AABB+1	Load Middle Byte
	LDA A	XXYY+1	Load Most Significant Byte to Acc.
	STA A	AABB+2	Load High Byte
	STA A	AABB+3	Transfer Data Word to DAC Register
	PUL A		
	TAP		Pop CCR From Stack
	PUL A		Pop Acc. A From Stack
	RTS		Return to Main Program

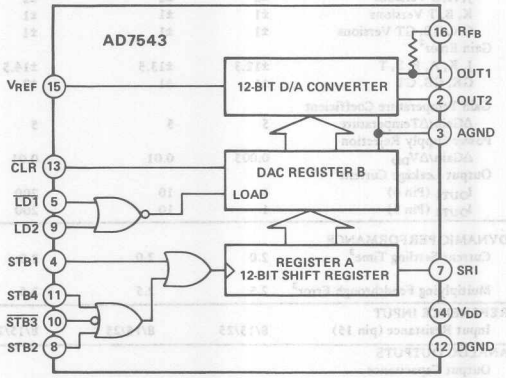
Serial Input 12-Bit DAC

AD7543

FEATURES

- Resolution: 12 Bits
- Nonlinearity: ±1/2LSB T_{min} to T_{max}
- Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
- Serial Load on Positive or Negative Strobe
- Asynchronous CLEAR Input for Initialization
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough: 1LSB max @ 10kHz
- Requires no Schottky Diode Output Protection
- Low Power Dissipation: 40mW max
- +5V Supply
- Small Size: 16-Pin DIP or 20-Terminal Surface Mount Package
- Low Cost

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

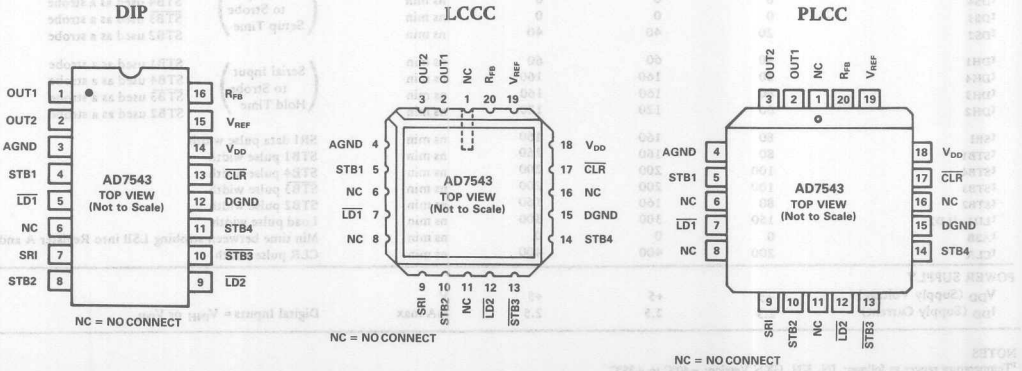
The AD7543 is a precision 12-bit monolithic CMOS multiplying DAC designed for serial interface applications.

The DAC's logic circuitry consists of a 12-bit serial-in parallel-out shift register (Register A) and a 12-bit DAC input register (Register B). Serial data at the AD7543 SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input. Once Register A is full its contents are loaded into Register B under control of the LOAD inputs.

Initialization is simplified by the use of the CLR input which provides an asynchronous reset of Register B.

Packaged in 16-pin DIP and 20-pin LCCC and PLCC, the AD7543 features excellent gain T.C. (2ppm/°C typ; 5ppm/°C max), +5V operation and latch-free operation. (No protection Schottky Diodes required.)

PIN CONFIGURATIONS



Parameter	T_A = +25°C	to +85°C	& +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
J, A, S Versions	±1	±1	±1	LSB max	
K, B, T Versions	±1/2	±1/2	±1/2	LSB max	
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
J, A, S Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
K, B, T Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GK, GB, GT Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
J, K, A, B, S, T	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GK, GB, GT	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 6 & 7)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$, see Figure 5.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is -300ppm/°C
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	Register B loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	Register B loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 6 and 7), serial load (MSB First)				
SWITCHING CHARACTERISTICS[5]					
t_{DS1}	50	100	100	ns min	(Serial Input to Strobe Setup Time) STB1 used as a strobe
t_{DS4}	0	0	0	ns min	STB4 used as a strobe
t_{DS3}	0	0	0	ns min	$\overline{STB3}$ used as a strobe
t_{DS2}	20	40	40	ns min	STB2 used as a strobe
t_{DH1}	30	60	60	ns min	(Serial Input to Strobe Hold Time) STB1 used as a strobe
t_{DH4}	80	160	160	ns min	STB4 used as a strobe
t_{DH3}	80	160	160	ns min	$\overline{STB3}$ used as a strobe
t_{DH2}	60	120	120	ns min	STB2 used as a strobe
t_{SRI}	80	160	160	ns min	SRI data pulse width
t_{STB1}	80	160	160	ns min	STB1 pulse width
t_{STB4}	100	200	200	ns min	STB4 pulse width
t_{STB3}	100	200	200	ns min	$\overline{STB3}$ pulse width
t_{STB2}	80	160	160	ns min	STB2 pulse width
t_{LD1}, t_{LD2}	150	300	300	ns min	Load pulse width
t_{ASB}	0	0	0	ns min	Min time between strobing LSB into Register A and loading Register B
t_{CLR}	200	400	400	ns min	CLR pulse width
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES

[1]Temperature ranges as follows: JN, KN, GKN Version; −40°C to +85°C
AQ, BQ, GBQ Versions: −40°C to +85°C
SQ, TQ, GTQ Versions: −55°C to +125°C

[2]See Terminology on following page.

[3]Guaranteed but not tested.

[4]Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[5]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . 0V, +7V
V_{DD} to DGND . . . . . 0V, +7V
AGND to DGND . . . . . V_{DD} +0.3V
DGND to AGND . . . . . V_{DD} +0.3V
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{OUT1}, V_{OUT2} to AGND . . . . . −0.3V, V_{DD} to +0.3V
V_{REF} to AGND . . . . . ±25V
V_{RFB} to AGND . . . . . ±25V
Power Dissipation (Package)
  Plastic
    To +70°C 670mW
    Derates above +70°C by . . . . . 8.3mW/°C
  Cerdip
    To +75°C 450mW
    Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
  Commercial (J, K, GK Versions) . . . . . −40°C to +85°C
  Industrial (A, B, GB Versions) . . . . . −40°C to +85°C
  Extended (S, T, GT Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Gain Error	Package Option*
AD7543JN	−40°C to +85°C	±1LSB	±12.3LSB	N-16
AD7543KN	−40°C to +85°C	±1/2LSB	±12.3LSB	N-16
AD7543GKN	−40°C to +85°C	±1/2LSB	±1LSB	N-16
AD7543JP	−40°C to +85°C	±1LSB	±12.3LSB	P-20A
AD7543KP	−40°C to +85°C	±1/2LSB	±12.3LSB	P-20A
AD7543GKP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7543JR	−40°C to +85°C	±1LSB	±12.3LSB	R-16
AD7543KR	−40°C to +85°C	±1/2LSB	±12.3LSB	R-16
AD7543GKR	−40°C to +85°C	±1/2LSB	±1LSB	R-16
AD7543AQ	−40°C to +85°C	±1LSB	±12.3LSB	Q-16
AD7543BQ	−40°C to +85°C	±1/2LSB	±12.3LSB	Q-16
AD7543GBQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-16
AD7543SQ	−55°C to +125°C	±1LSB	±12.3LSB	Q-16
AD7543TQ	−55°C to +125°C	±1/2LSB	±12.3LSB	Q-16
AD7543GTQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-16
AD7543SE	−55°C to +125°C	±1LSB	±12.3LSB	E-20A
AD7543TE	−55°C to +125°C	±1/2LSB	±12.3LSB	E-20A
AD7543GTE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

*E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table II
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table II
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
10	$\overline{STB3}$	Register A Strobe 3 input, see Table II
11	STB4	Register A Strobe 4 input, see Table II
12	DGND	Digital Ground
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R_{FB}	DAC Feedback Resistor

Table I. Pin Function Description, DIP Configuration

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 6 and 7.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

GENERAL CIRCUIT INFORMATION
The AD7543, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

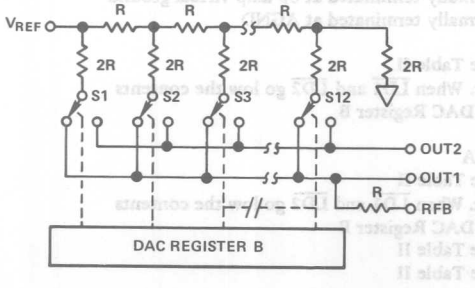


Figure 1. AD7543 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). The reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.

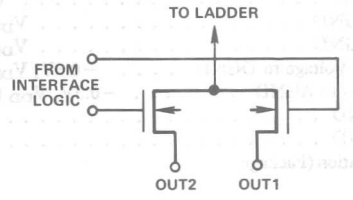


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS
The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the 1/4096 current source represents a constant 1 least significant bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

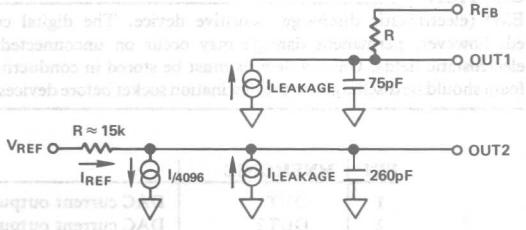


Figure 3. AD7543 DAC Equivalent Circuit All Digital Inputs LOW

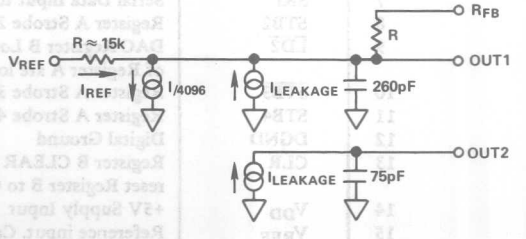


Figure 4. AD7543 DAC Equivalent Circuit All Digital Inputs HIGH

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↑	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↑	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↑	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown. ↑ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table II. AD7543 Truth Table

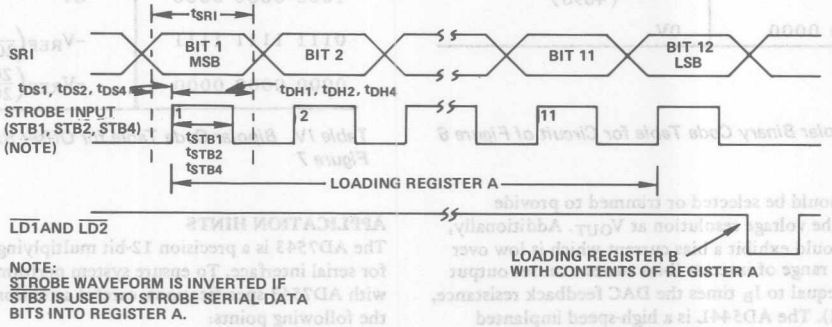


Figure 5. Timing Diagram

INTERFACE LOGIC INFORMATION

Shown in the AD8543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SR1 is clocked into the shift register on the leading (rising) edge of STB1, STB2 or STB4 or on the leading (falling) edge of $\overline{STB3}$. Table II defines the various logic states required on the Register A control inputs, while Figure 5 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing $\overline{LD1}$ and $\overline{LD2}$ momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing $\overline{CLR}$ momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit of Figure 6, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit of Figure 7, a CLEAR causes the DAC output to equal $-V_{REF}$.

APPLYING THE AD7543

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current (again of + or – polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table III.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10pF to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

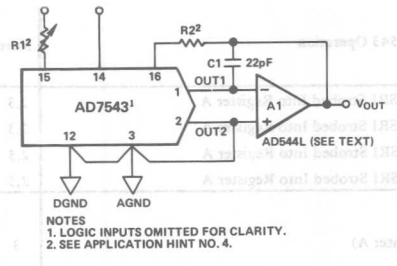


Figure 6. Unipolar Binary Operation (2-Quadrant Multiplication)

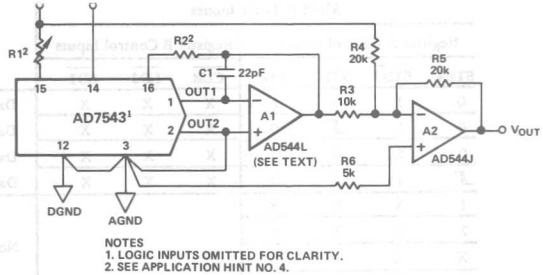


Figure 7. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table III. Unipolar Binary Code Table for Circuit of Figure 6

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table IV. Bipolar Code Table for Offset Binary Circuit of Figure 7

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table IV illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 to 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

APPLICATION HINTS

The AD7543 is a precision 12-bit multiplying DAC designed for serial interface. To ensure system performance consistent with AD7543 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7543. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7543 AGND and DGND pins to prevent possible device damage.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}\ 2^{-n}$ where n is the number of bits exercised].

3. HIGH FREQUENCY CONSIDERATIONS: AD7543 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7543 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 6 and 7 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7543 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm/°C}$$

However, if the AD7543GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630—10—6/81 available from Analog Devices.

5. For additional information on multiplying DACS refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479—15—8/78, available from Analog Devices.

AD7543 INTERFACE TO MC6800

In this example, it is assumed that the 12-bit data is contained in two memory locations (0000 and 0001). The four most significant bits are assumed to occupy the lower half of memory location 0000. The eight least significant bits occupy memory location 0001. The data is presented bit by bit on the D7 line and strobed into the AD7543 by executing memory write instructions. In this case the strobe signal (STB1) is supplied by decoding address 2000, R/$\overline{W}$ and ϕ_2. A memory write instruction to a different address (4000) loads the data from Register A to the DAC register.

Figure 8 shows the interface circuitry and Table V gives a listing of the procedure.

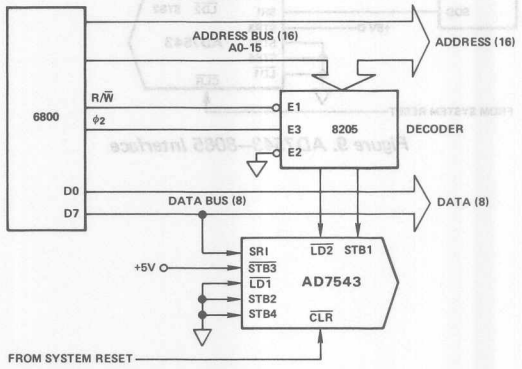


Figure 8. AD7543–MC6800 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
	LDA	B, 04	
	LDA	A, 0000	Load 4 Most Significant Bits
LOOP	ROL	A	Reposition in the Data
	DEC	B	in ACC A
	BNE	LOOP	
	LDA	B, 04	
	BSR	SHIFT	Output Data
	LDA	B, 08	
	LDA	A, 0001	Load 8 Least Significant Bits
	BSR	SHIFT	Output Data
	STA	A, 4000	Load DAC Register
	RTS		Return to Main Program
SHIFT	STA	A,2000	Strobe Data
	ROL	A	into AD7543
	DEC	B	
	BNE	SHIFT	
	RTS		

Table V. Sample Routine for AD7543–MC6800 Interface

AD7543 INTERFACE TO MCS-85

Figure 9 shows the AD7543 interfaced to the 8085. This system makes use of the serial output facility (SOD) on the 8085.

The data is presented serially on the SOD line and strobed into the AD7543 by executing memory write instructions. In this example the strobe signal (STB2) is supplied by decoding address 8000 and $\overline{WR}$. A memory write instruction to a different address (A000) loads the DAC Register with Register

A data. Table VI gives a listing of this procedure. Note, it is assumed that the required serial data is already present in right-justified format in Registers H and L when this procedure is implemented. Note that the sample routine of Table VI can be speeded up by replacing the SHIFT routine with a DAD H instruction.

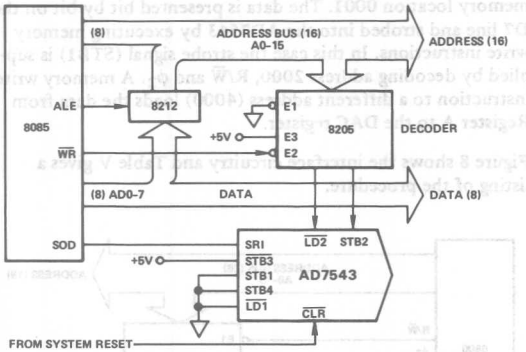


Figure 9. AD7543–8085 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
	MVI	B, 05	Shift Data Up to
LOOP	CALL	SHIFT	Most Significant
	DCR	B	Segment of HL with
	JNZ	LOOP	MSB as Carry
	MVI	B, OC	
LUP	MVI	A, 80	SOD Enable in ACC
	RAR		Shift in MSB of H
	SIM		Set Interrupt Mask
	STA	8000	Strobe Data into AD7543
	CALL	SHIFT	Get Next Bit into Carry
	DCR	B	
	JNZ	LUP	Go Back if Not Finished
	STA	A000	Load DAC Register of AD7543
	RET		Return to Main Program
SHIFT	MOV	A, L	Shift H and L Left
	RAL		One Place and
	MOV	L, A	Leave Uppermost Bit
	MOV	A, H	of H in Carry
	RAL		
	MOV	H, A	
	RET		

Table VI. Sample Routine for AD7543–8085 Interface

12-Bit Serial Input Multiplying CMOS D/A Converter

PM-7543

2

FEATURES

- Fast, Flexible Microprocessor Interface with Serial Data Input
- Superior Accuracy
  - ±1/2 LSB INL Max
  - ±1 LSB Gain Error Max
  - Low 5ppm/°C Max Tempco
- Improved ESD Resistance
- Auto-Insertable DIP Package
- Surface Mount SOL Package
- Superior Direct Replacement for AD7543
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available in Die Form

APPLICATIONS

- Process Control and Industrial Automation
- Programmable Amplifiers
- Digitally-Controlled Power Supplies, Attenuators, Filters
- Instrumentation
- Avionics
- Auto-Calibration Systems

ORDERING INFORMATION†

GAIN ERROR	NON-LINEARITY	TEMPERATURE RANGE MILITARY*	EXTENDED††† INDUSTRIAL	COMMERCIAL
±1LSB	±1/2LSB	PM7543AQ	PM7543EQ	–
±2LSB	±1/2LSB	–	–	PM7543GP
±2LSB	±1LSB	PM7543BQ	PM7543FQ	–
±2LSB	±1LSB	PM7543BRC/883	PM7543FP	–
±2LSB	±1LSB	–	PM7543FS	–
±2LSB	±1LSB	–	PM7543FPC	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

††† CerDIP and epoxy devices are available in the extended industrial temperature range of –40°C to +85°C.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7543AQ	AD7543GTD	MIL
PM7543AQ	AD7543TD	
PM7543BQ	AD7543SD	
PM7543EQ	AD7543GBD	IND
PM7543EQ	AD7543BD	
PM7543FQ	AD7543AD	
PM7543GP	AD7543GKN	COM
PM7543GP	AD7543KN	
PM7543FP	AD7543JN	
PM7543FPC	AD7543JP	

GENERAL DESCRIPTION

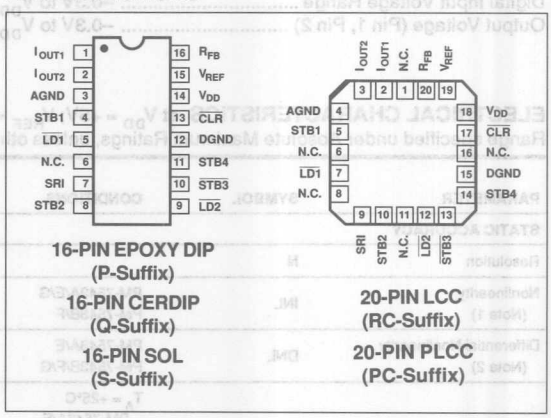
The PM-7543 is a 12-bit resolution, multiplying, CMOS D/A converter, which features serial data input and current output. Serial data input reduces pin count and allows the PM-7543 to be placed in a smaller package, saving PC board space. Improved analog parameters such as digital charge injection, power supply rejection, output capacitance, feedthrough error, fast microprocessor interface, and improved ESD protective circuitry make the PM-7543 a superior pin-compatible second-source to the industry standard AD7543.

The rising or falling edge (user selected) of the strobe inputs are used to clock serial data (present at the SRI pin) into the input shift register.

When the shift register's data has been updated, the new data word is transferred to the DAC register with use of the LOAD inputs.

Continued

PIN CONNECTIONS



16-PIN EPOXY DIP (P-Suffix)

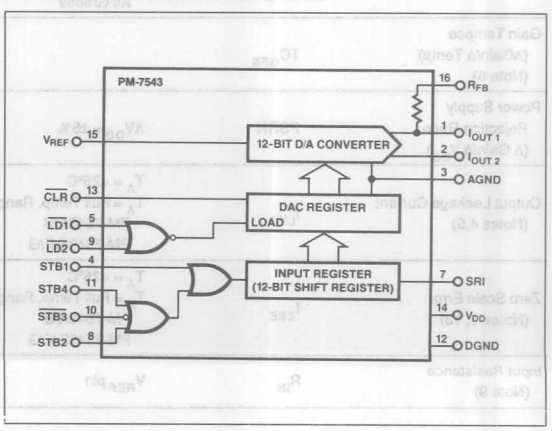
16-PIN CERDIP (Q-Suffix)

16-PIN SOL (S-Suffix)

20-PIN LCC (RC-Suffix)

20-PIN PLCC (PC-Suffix)

FUNCTIONAL BLOCK DIAGRAM



of multiple DACs. An asynchronous CLEAR input resets the DAC register without altering the data in the input register.

Improved linearity and gain error performance may permit reduced circuit parts count through the elimination of trimming components. Fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. The PM-7543 is available in standard plastic and CerDIP packages that are compatible with auto-insertion equipment. For an even smaller package, consider the DAC-8043, available in an 8-pin mini-DIP.

CerDIP and epoxy devices are available in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwide noted.)

V_{DD} to DGND ..... +17V
V_{REF} to DGND ..... ±25V
V_{RFB} to DGND ..... ±25V
DGND to AGND ..... V_{DD} + 0.3V
AGND to DGND ..... V_{DD} + 0.3V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}

EQ/FQ/FP/FPC/FS Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltage higher than V_{DD} or less than DGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control input are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7543 MIN	PM-7543 TYP	PM-7543 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	–	–	Bits
Nonlinearity (Note 1)	INL	PM-7543A/E/G	–	–	±1/2	LSB
		PM-7543B/F	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	PM-7543A/E	–	–	±1/2	LSB
		PM-7543B/F/G	–	–	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				
		PM-7543A/E	–	–	±1	LSB
		PM-7543B/F/G	–	–	±2	
		T_A = Full Temp. Range				
		All Grades	–	–	±2	
Gain Tempco (ΔGain/Δ Temp) (Note 6)	TC_{GFS}		–	–	±5	ppm/°C
Power Supply Rejection Ratio (Δ Gain/Δ V_{DD})	PSRR	ΔV_{DD} = ±5%	–	±0.0006	±0.002	%/%
Output Leakage Current (Notes 4,5)	I_{LKG}	T_A = +25°C	–	–	±1	nA
		T_A = Full Temp. Range				
		PM-7543A/B	–	–	±100	
		PM-7543E/F/G	–	–	±10	
Zero Scale Error (Notes 8, 13)	I_{ZSE}	T_A = +25°C	–	±0.002	±0.006	LSB
		T_A = Full Temp. Range				
		PM-7543A/B	–	±0.05	±0.61	
		PM-7543E/F/G	–	±0.01	±0.06	
Input Resistance (Note 9)	R_{IN}	V_{REF} pin	7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7543 MIN	PM-7543 TYP	PM-7543 MAX	UNITS
AC PERFORMANCE						
Output Current Setting Time (Notes 6,7)	t_s		–	0.380	1	µs
AC Feedthrough Error (V_{REF} to I_{OUT1}) (Note 6, 12)	FT	V_{REF} = 20Vp-p @ f = 10kHz T_A = +25°C	–	–	2.0	mV_{p-p}
Digital to Analog Glitch Energy (Note 6, 11)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	–	–	20	nVs
Total Harmonic Distortion (Note 6)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	–	–	–92	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz between R_{FB} and I_{OUT}	–	–	13	$nV/\sqrt{Hz}$
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 10)	I_{IN}	V_{IN} = 0V to +5V	–	–	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	–	–	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT1} C_{OUT2}	Digital Inputs = all 1s Digital Inputs = all 0s	– –	– –	90 90	pF
Output Capacitance (Note 6)	C_{OUT1} C_{OUT2}	Digital Inputs = all 0s Digital Inputs = all 1s	– –	– –	60 60	pF
TIMING CHARACTERISTICS						
Serial Input to Strobe Setup Times (t_{STB} = 80nS)	t_{DS1}	STB1 used as the strobe T_A = +25°C STB1 used as the strobe T_A = Full Temp. Range	50 50	– –	– –	ns
	t_{DS2}	STB2 used as the strobe T_A = +25°C STB2 used as the strobe T_A = Full Temp. Range	20 20	– –	– –	ns
	t_{DS3}	STB3 used as the strobe T_A = +25°C STB3 used as the strobe T_A = Full Temp. Range	10 20	– –	– –	ns
	t_{DS4}	STB4 used as the strobe T_A = +25°C STB4 used as the strobe T_A = Full Temp. Range	20 20	– –	– –	ns
Serial Input to Strobe Hold Times (t_{STB} = 80nS)	t_{DH1}	STB1 used as the strobe T_A = +25°C STB1 used as the strobe T_A = Full Temp. Range	40 50	– –	– –	ns
	t_{DH2}	STB2 used as the strobe T_A = +25°C STB2 used as the strobe T_A = Full Temp. Range	50 60	– –	– –	ns
	t_{DH3}	STB3 used as the strobe T_A = +25°C STB3 used as the strobe T_A = Full Temp. Range	80 80	– –	– –	ns
	t_{DH4}	STB4 used as the strobe T_A = +25°C STB4 used as the strobe T_A = Full Temp. Range	80 80	– –	– –	ns

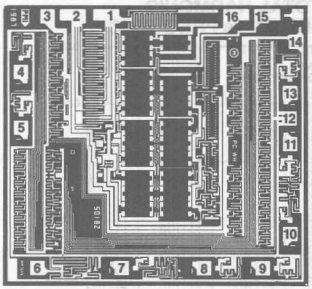
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7543 MIN	TYP	MAX	UNITS
SRI Data Pulse Width	t_{SRI}	T_A = Full Temp. Range	100	–	–	ns
STB1 Pulse Width ($\overline{STB1}$ = 80ns) (Note 15)	t_{STB1}	T_A = Full Temp. Range	80	–	–	ns
STB2 Pulse Width ($\overline{STB2}$ = 10ns) (Note 15)	t_{STB2}	T_A = Full Temp. Range	80	–	–	ns
STB3 Pulse Width ($\overline{STB3}$ = 80ns) (Note 15)	t_{STB3}	T_A = Full Temp. Range	80	–	–	ns
STB4 Pulse Width ($\overline{STB4}$ = 80ns) (Note 15)	t_{STB4}	T_A = Full Temp. Range	80	–	–	ns
Load Pulse Width	t_{LD1}, t_{LD2}	T_A = +25°C T_A = Full Temp. Range	140 180	– –	– –	ns
LSB Strobe into Input Register to Load DAC Register Time	t_{ASB}	T_A = Full. Temp. Range	0	–	–	ns
CLR Pulse Width	t_{CLR}	T_A = Full Temp. Range	80	–	–	ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All Digital Inputs = V_{IH} or V_{IL} All Digital Inputs = 0V or V_{DD}	– –	– –	2 0.1	mA

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT1}; all digital inputs = V_{IL}, V_{REF} = +10V.
5. Specification also applies for I_{OUT2} when all digital inputs = V_{IH}.
6. Guaranteed by design and not tested.
7. I_{OUT1} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_s = propagation delay (t_{PD}) + 9τ, where τ = measured time constant of the final RC decay.
8. V_{REF} = +10V, all digital inputs = 0V.
9. Absolute temperature coefficient is less than +300ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. All digital inputs = 0V.
13. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = $R_{REF} \times I_{LKG} \times 4096) / V_{REF}$.
14. Calculations from $e_n = \sqrt{4K\,TRB}$ where:
    K = Boltzmann constant, J/°K R = resistance Ω
    T = resistor temperature, °K B = bandwidth, Hz
15. Minimum low time pulse width for STB1, STB2, and STB4, and minimum high time pulse width for $\overline{STB3}$.

DICE CHARACTERISTICS



DIE SIZE 0.099 x 0.107 inch, 10,543 sq. mils (2.51 x 2.72 mm, 6.83 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. STB1
5. $\overline{LD1}$
6. N.C.
7. SRI
8. STB2
9. $\overline{LD2}$
10. $\overline{STB3}$
11. STB4
12. DGND
13. $\overline{CLR}$
14. V_{DD} (Substrate)
15. V_{REF}
16. R_{FB}

Substrate (die backside) is internally connected to V_{DD}.

2

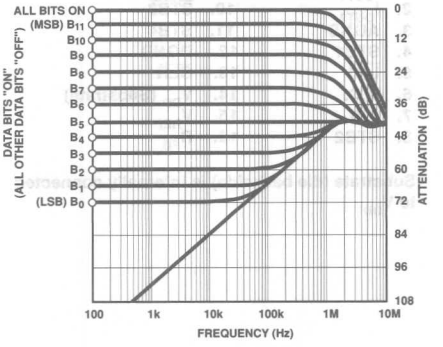
WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	PM-7543G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	±1	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}	V_{REF} pad	7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2.0 0.1	mA MAX

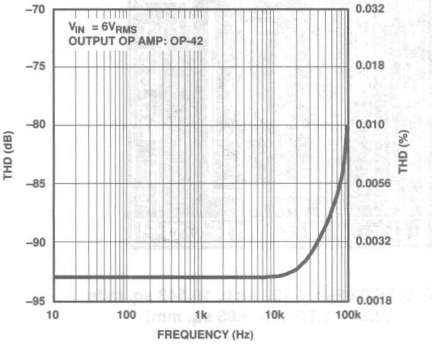
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

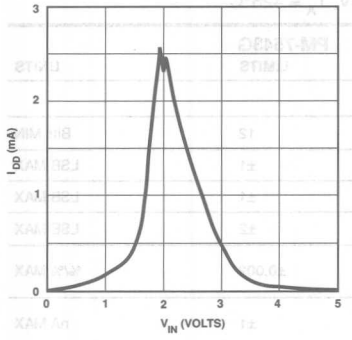
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



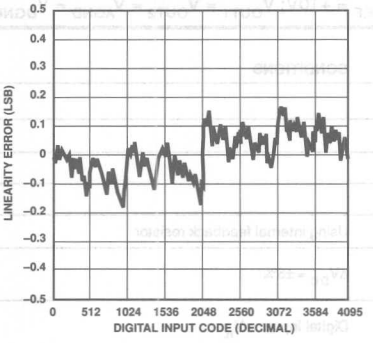
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



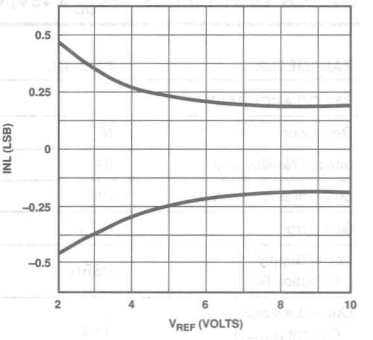
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



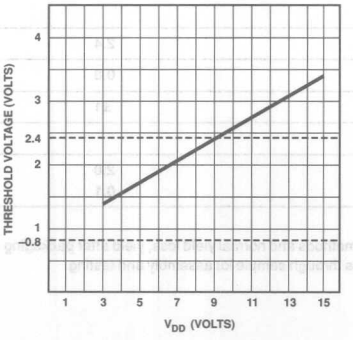
LINEARITY ERROR vs DIGITAL CODE



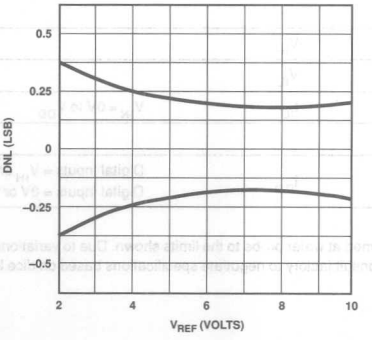
LINEARITY ERROR vs REFERENCE VOLTAGE



LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} to ground.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7543 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data input and control logic, and two data registers. The digital circuitry forms an interface in which serial data can be loaded, under microprocessor control, into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

A simplified circuit of the PM-7543 DAC is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches. These switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It was essential to design these switches such that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop would then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches were included in series with

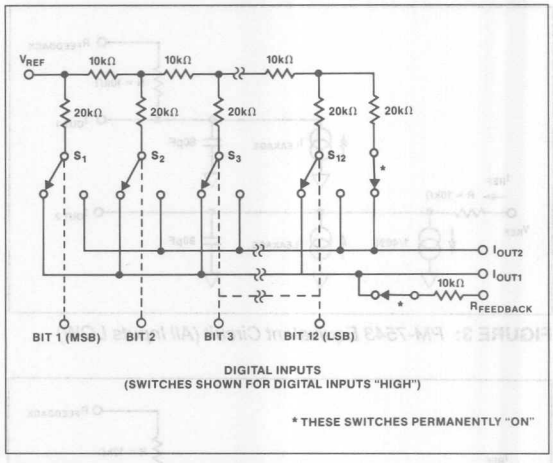


FIGURE 1: *Simplified DAC Circuit*

the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit," Figure 1, shows the location of these switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7543 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes were designed to clamp the inputs well below dangerous levels during static discharge conditions.

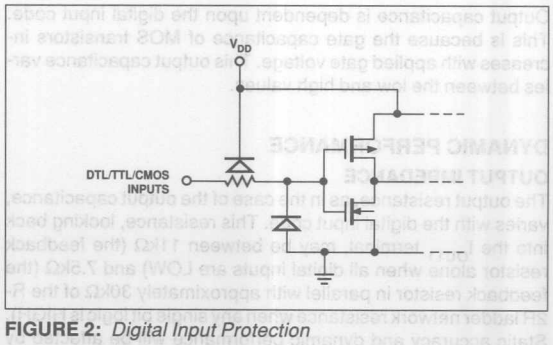


FIGURE 2: *Digital Input Protection*

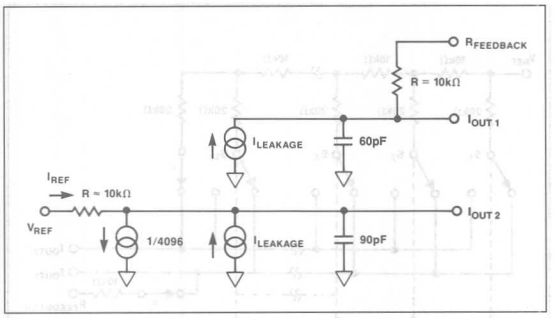


FIGURE 3: *PM-7543 Equivalent Circuit (All Inputs LOW)*

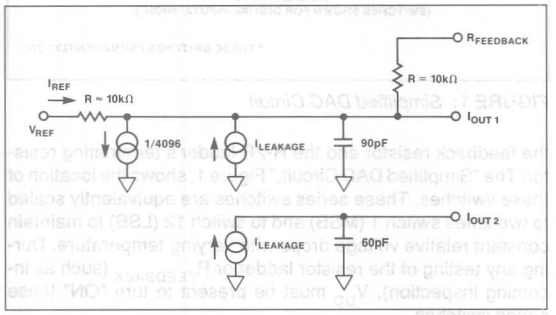


FIGURE 4: *PM-7543 Equivalent Circuit (All Digital Inputs HIGH)*

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the PM-7543's internal DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW, and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT1} terminal, may be between 11kΩ (the feedback resistor alone when all digital inputs are LOW) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations.

The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7543. The use of a small compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 7 and 8).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1}, I_{OUT2}, and AGND (pins 1, 2, and 3) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 7 and 8). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than ±200μV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

It is recommended that the digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition region (see the Supply Current vs Logic Input Voltage graph under the Typical Performance Characteristics). The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 5-30pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

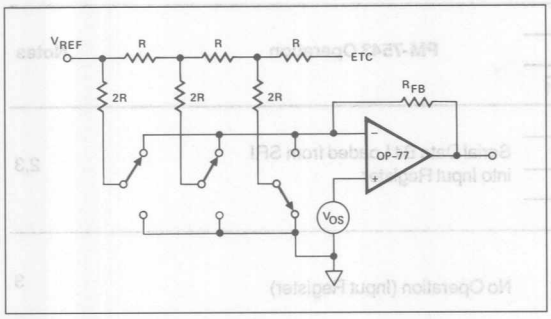


FIGURE 5: *Simplified Circuit*

Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:
$R_O = 10k\Omega$ for more than four bits of logic 1,
$R_O = 30k\Omega$ for any single bit of logic 1.

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{ERROR_1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3\,V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.4mV for the PM-7543, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-97, OP-07, OP-27 and OP-42.

INTERFACE LOGIC OPERATION

The microprocessor interface of the PM-7543 has been designed with multiple STROBE and LOAD inputs to maximize interfacing options. Control signals decoding may be done on-chip or with the use of external decoding circuitry (see Figure 11).

Serial data can be clocked into the input register with STB1, STB2, or STB4. The strobe inputs are active on the rising edge. $\overline{STB3}$ may be used with a falling edge to clock-in data.

Holding any STROBE input at its selected state (i.e. STB1, STB2 or STB4 at logic HIGH or $\overline{STB3}$ at logic LOW) will act to prevent any further data input.

When a new data word has been entered into the input register, it is transferred to the DAC register by asserting both LOAD inputs.

The $\overline{CLR}$ input allows asynchronous resetting of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{REF}$.

INTERFACE INPUT DESCRIPTION

STB1 (Pin 4), STB2 (Pin 8), STB4 (Pin 11) – Input Register Strobe. Inputs Active on Rising Edge. Selected to load serial data into input register. See Table 1 for details.

$\overline{STB3}$ (Pin 10) – Input Register Strobe Input. Active on Falling Edge. Selected to load serial data into input register. See Table 1 for details.

$\overline{LD1}$ (Pin 5), $\overline{LD2}$ (Pin 9) – Load DAC Register Inputs. Active Low. Selected together to load contents of Input Register into DAC register.

$\overline{CLR}$ (Pin 13) – Clear Input. Active Low. Asynchronous. When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

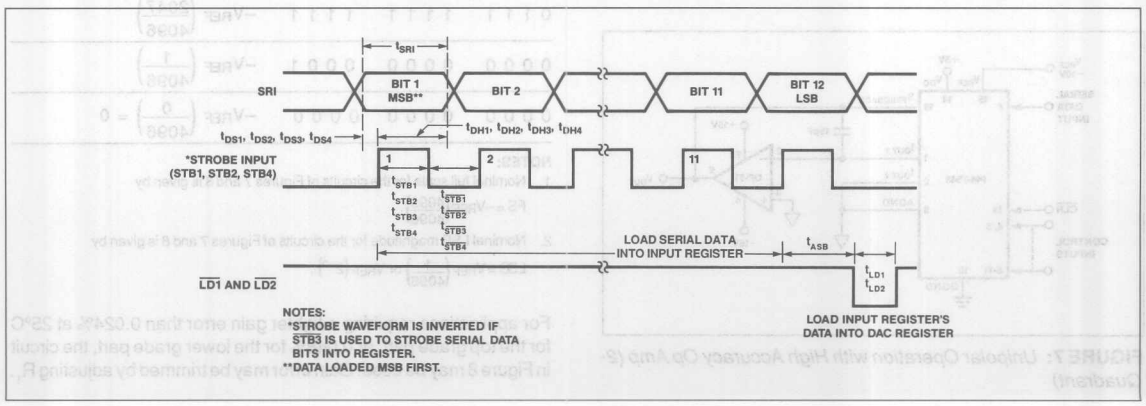


FIGURE 6: *Timing Diagram*

TABLE 1: PM-7543 Truth Table

PM-7543 Logic Inputs							PM-7543 Operation	Notes
Input Register		Control Inputs		DAC Register	Control Inputs			
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↓	X	X	X	Serial Data Bit Loaded from SRI into Input Register	2,3
0	1	↓	0	X	X	X		
0	↓	0	0	X	X	X		
↓	1	0	0	X	X	X		
1	X	X	X				No Operation (Input Register)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Reset DAC Register to Zero Code (Code: 0000 0000 0000) (Asynchronous Operation)	1,3
				1	1	X	No Operation (DAC Register)	3
				1	X	1		
				1	0	0	Load DAC Register with the Contents of Input Register	3

NOTES:
1. CLR = 0 Asynchronously resets DAC Register to 0000 0000 0000, but has no effect on Input Register.
2. Serial data is loaded into Input Register MSB first, on edges shown ↓ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

UNIPOLAR OPERATION (2-QUADRANT)

The circuit shown in Figures 7 and 8 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The V_{REF} voltage range is the maximum input voltage range of the op amp or ±25V, whichever is lowest.

In many applications the PM-7543's negligible zero scale error and very low gain error permit the elimination of the trimming of the components (R_1 and the external $R_{FEEDBACK}$) without adverse effects on circuit performance.

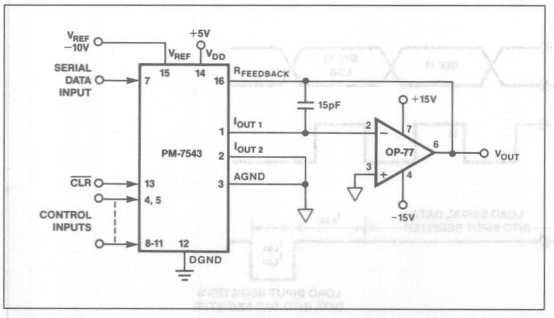


FIGURE 7: *Unipolar Operation with High Accuracy Op Amp (2-Quadrant)*

TABLE 2: Unipolar Code Table

DIGITAL INPUT			NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 7 and 8)
MSB		LSB	
1 1 1 1	1 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0	0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{2049}{4096}\right)$
1 0 0 0	0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{2047}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:
1. Nominal full scale for the circuits of Figures 7 and 8 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 7 and 8 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}\left(2^{-n}\right)$.

For applications requiring a tighter gain error than 0.024% at 25°C for the top grade part, or 0.048% for the lower grade part, the circuit in Figure 8 may be used. Gain error may be trimmed by adjusting R_1.

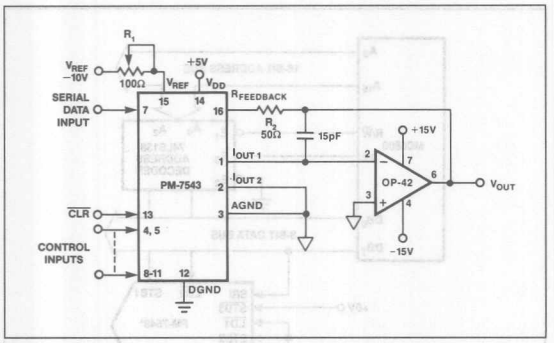


FIGURE 8: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

The DAC register must first be loaded with all 1s. R_1 is then adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

BIPOLAR OPERATION (4-QUADRANT)

Figure 9 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient match. Mismatching between R_3 and R_4 causes offset and full-scale errors while an R_5 to R_4 and R_3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted by adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB			LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 9)
1 1 1 1	1 1 1 1	1 1 1 1		$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0	0 0 0 0	0 0 0 1		$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0	0 0 0 0	0 0 0 0		0
0 1 1 1	1 1 1 1	1 1 1 1		$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0	0 0 0 0	0 0 0 1		$-V_{REF}\left(\frac{2047}{2048}\right)$
0 0 0 0	0 0 0 0	0 0 0 0		$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuits of Figure 9 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuits of Figure 9 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7543 connected in the multiplying mode as shown in Figures 7 and 8 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

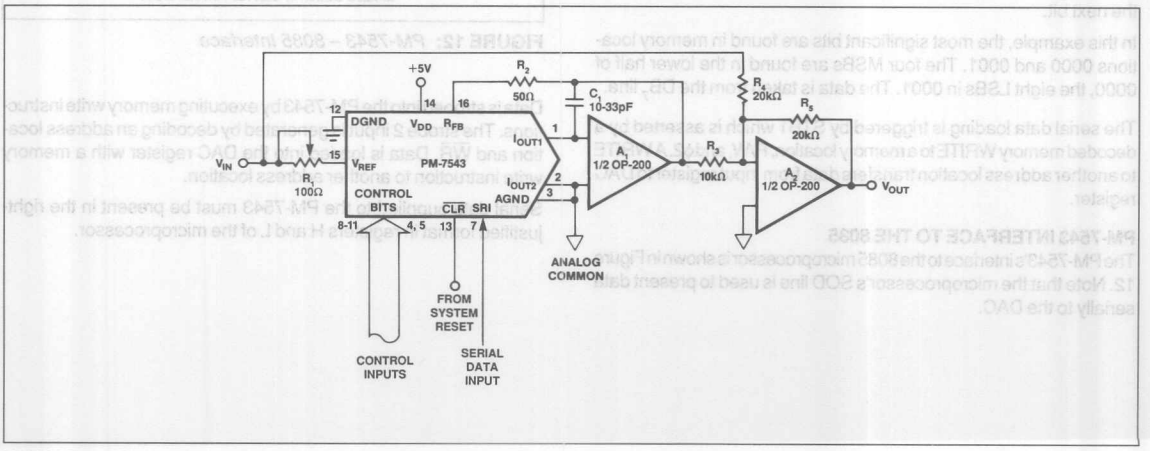


FIGURE 9: *Bipolar Operation (4-Quadrant, Offset Binary)*

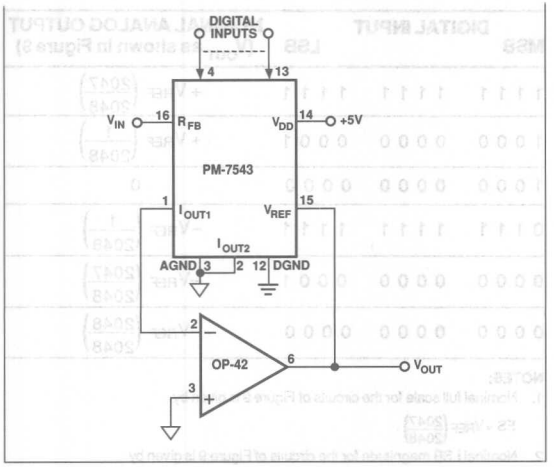


FIGURE 10: *Analog/Digital Divider*

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 10 and is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON," the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON."

INTERFACING TO THE MC6800

As shown in Figure 11, the PM-7543 may be interfaced to the 6800 by successively executing memory WRITE instructions while manipulating the data between WRITEs, so that each WRITE presents the next bit.

In this example, the most significant bits are found in memory locations 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the DB_7 line.

The serial data loading is triggered by STB1 which is asserted by a decoded memory WRITE to a memory location, R/W, and $\phi 2$. A WRITE to another address location transfers data from input register to DAC register.

PM-7543 INTERFACE TO THE 8085

The PM-7543's interface to the 8085 microprocessor is shown in Figure 12. Note that the microprocessor's SOD line is used to present data serially to the DAC.

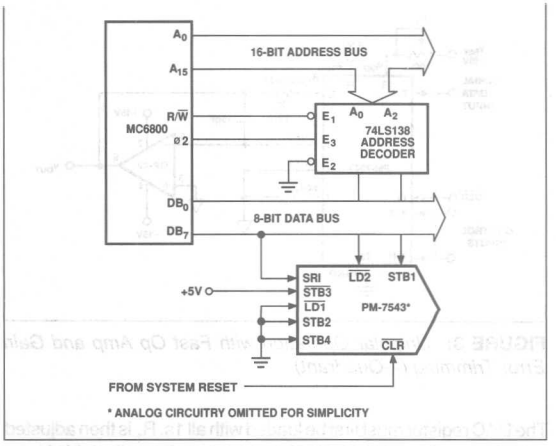


FIGURE 11: *PM-7543 – MC6800 Interface*

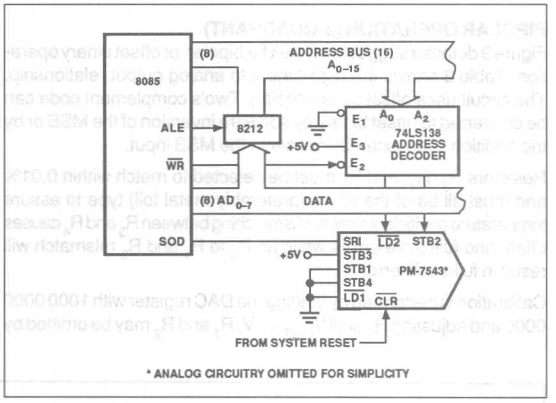


FIGURE 12: *PM-7543 – 8085 Interface*

Data is strobed into the PM-7543 by executing memory write instructions. The strobe 2 input is generated by decoding an address location and $\overline{WR}$. Data is loaded into the DAC register with a memory write instruction to another address location.

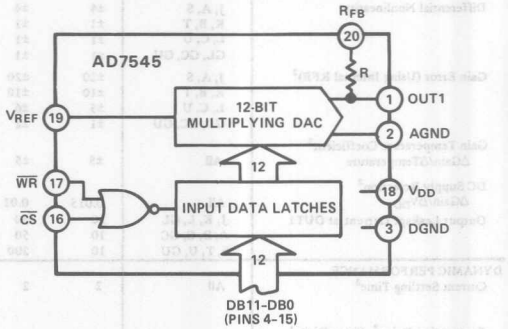
Serial data supplied to the PM-7543 must be present in the right-justified format in registers H and L of the microprocessor.

CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES
- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Small 20-Pin 0.3" DIP and 20-Terminal Surface Mount Packages
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

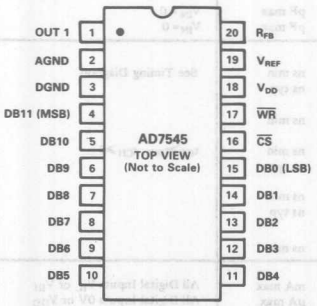
The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

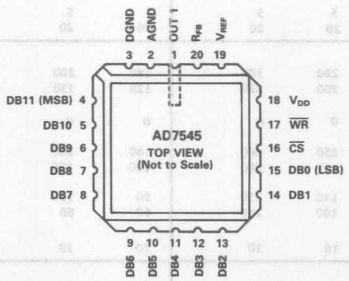
The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

PIN CONFIGURATIONS

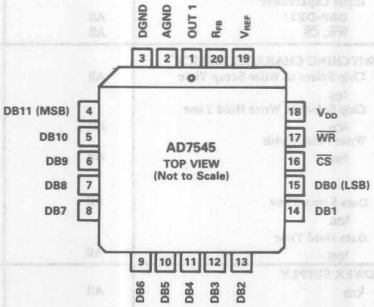
DIP



LCCC



PLCC



AD7545—SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}, T_{max}[1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}, T_{max}[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	µs max	To 1/2LSB. OUT 1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Digital to Analog Glitch Impulse	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At I_{OUT1}	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
Input Resistance	All	7	7	7	7	kΩ min	Input Resistance TC = –300ppm/°C typ
(Pin 19 to GND)		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3] C_{OUT1}	All	70	70	70	70	pF max	DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	µA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0–DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time	All	280	380	180	200	ns min	See Timing Diagram
t_{CS}		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time	All	140	210	90	120	ns min	
t_{DS}		100	150	60	80	ns typ	
Data Hold Time t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	µA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	µA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: J, K, L, GL versions: 0 to +70°C; A, B, C, GC versions: –25°C to +85°C; S, T, U, GU versions: –55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.

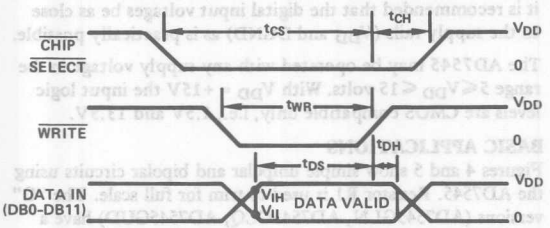
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $V_{IH} + V_{IL}/2$.

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (J, K, L, GL) Grades	0 to +70°C
Industrial (A, B, C, GC) Grades	−25°C to +85°C
Extended (S, T, U, GU) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RELATIVE ACCURACY: The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full scale points have been adjusted. This is an end point linearity measurement.

DIFFERENTIAL NONLINEARITY: The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1LSB then it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY: This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reached 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVsecs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33pF.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Maximum Gain Error T_A=+25°C V_{DD}=+5V	Package Option[3]
AD7545JN	0°C to +70°C	±2 LSB	±20 LSB	N-20
AD7545AQ	−25°C to +85°C	±2 LSB	±20 LSB	Q-20
AD7545SQ	−55°C to +125°C	±2 LSB	±20 LSB	Q-20
AD7545KN	0°C to +70°C	±1 LSB	±10 LSB	N-20
AD7545BQ	−25°C to +85°C	±1 LSB	±10 LSB	Q-20
AD7545TQ	−55°C to +125°C	±1 LSB	±10 LSB	Q-20
AD7545LN	0°C to +70°C	±1/2 LSB	±5 LSB	N-20
AD7545CQ	−25°C to +85°C	±1/2 LSB	±5 LSB	Q-20
AD7545UQ	−55°C to +125°C	±1/2 LSB	±5 LSB	Q-20
AD7545GLN	0°C to +70°C	±1/2 LSB	±1 LSB	N-20
AD7545GCQ	−25°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7545GUQ	−55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7545JP	0°C to +70°C	±2 LSB	±20 LSB	P-20A
AD7545SE	−55°C to +125°C	±2 LSB	±20 LSB	E-20A
AD7545KP	0°C to +70°C	±1 LSB	±10 LSB	P-20A
AD7545TE	−55°C to +125°C	±1 LSB	±10 LSB	E-20A
AD7545LP	0°C to +70°C	±1/2 LSB	±5 LSB	P-20A
AD7545UE	−55°C to +125°C	±1/2 LSB	±5 LSB	E-20A
AD7545GLP	0°C to +70°C	±1/2 LSB	±1 LSB	P-20A
AD7545GUE	−55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-20) in lieu of cerdip packages (Q-20).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military datasheets. For U.S. Standard Military Drawing (SMD) see DESC drawing 5962-87702.
[3]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

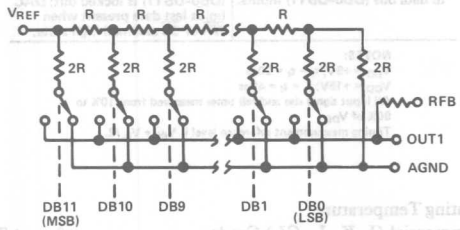


Figure 1. Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

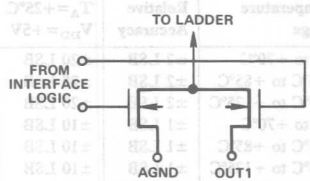


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION—DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

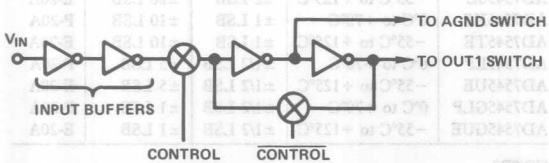


Figure 3. Digital Input Structure

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 1 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

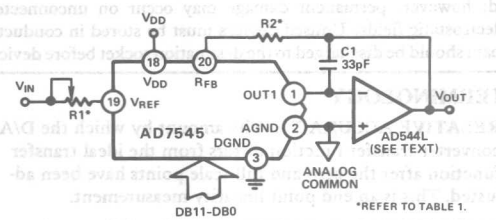


Figure 4. Unipolar Binary Operation

TRIM RESISTOR	J/A/S	K/B/T	L/C/U	GL/GC/GU
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades for V_{DD} = +5V

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive –OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 and R4 and R3 causes full scale error.

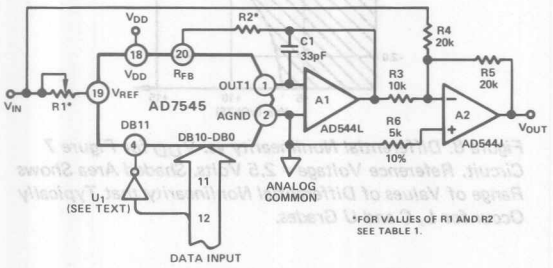


Figure 5. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table III. 2's Complement Code Table for Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

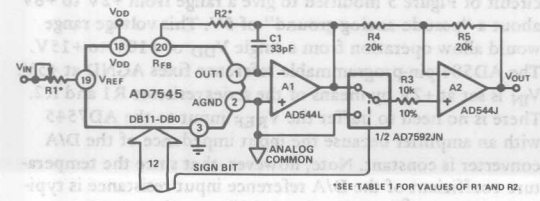


Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

Sign Bit	Binary Numbers in DAC Register			Analog Output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high cur-

rents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT 1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545 connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit.

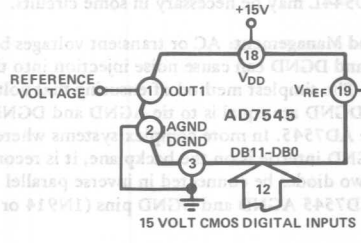


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions.

To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between OUT1 and AGND is increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

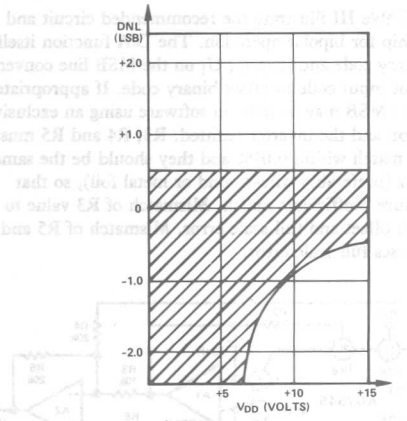


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

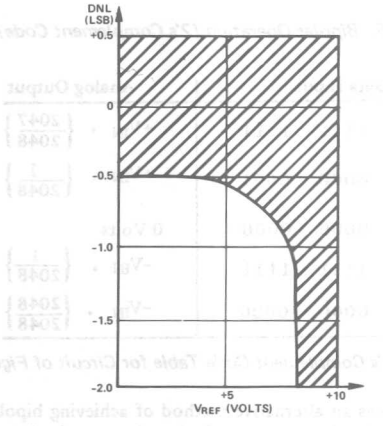


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2. There is no need to buffer the V_{REF} input to the AD7545 with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically –300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate

the +2.0V at the AD7545 V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

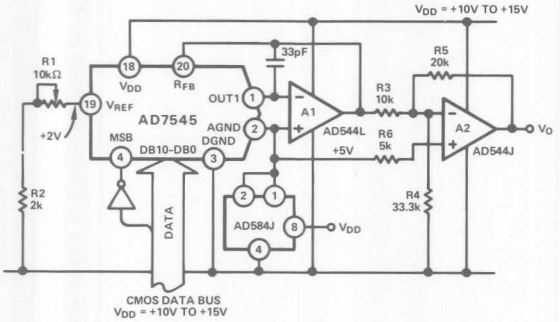


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545

The AD7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

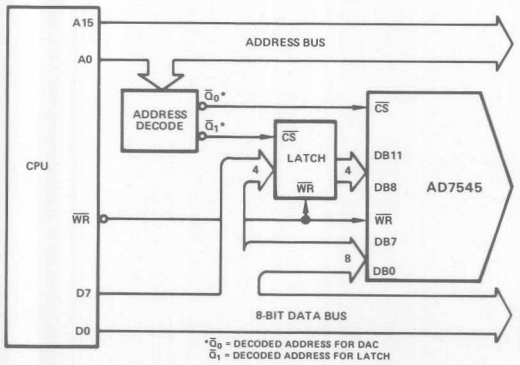


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each AD7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

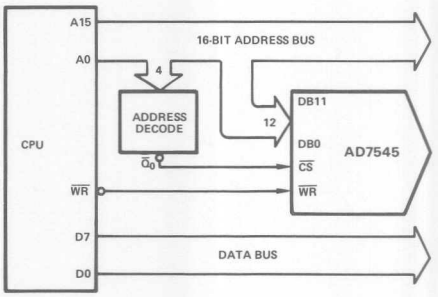


Figure 12. Connecting the AD7545 to 8-Bit Processors via the Address Bus

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A converters available from Analog Devices, Publication Number G479.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS – Application Note, Publication Number E630–10–6/81 available from Analog Devices.

PM-7545/PM-7645

FEATURES

- **Preadjusted Full Scale ..... ±1 LSB Maximum Gain Error**
- **Low Gain Temperature Coefficient ..... 2ppm/°C**
- **Small 20-Pin 0.3" Wide DIP**
- **PM-7545 TTL Compatible for V_{DD} = 5V**
- **PM-7645 TTL and 5V CMOS Compatible for V_{DD} = 15V**
- **High ESD Resistance**
- **Available in Die Form**

ORDERING INFORMATION †

	PACKAGE: 20-PIN		
MAXIMUM GAIN ERROR T_A = +25°C	MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	PM7545AR	PM7545ER	PM7545GP
±3 LSB	PM7545BR	PM7545FR	–
±3 LSB	PM7545BRC/883	PM7545FP	–
±3 LSB	–	PM7545FPC	–
±3 LSB	–	PM7545FS	–
±1 LSB	PM7645AR	PM7645ER	PM7645GP
±3 LSB	PM7645BR	PM7645FR	–
±3 LSB	–	PM7645FP	–
±3 LSB	–	PM7645FPC	–
±3 LSB	–	PM7645FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

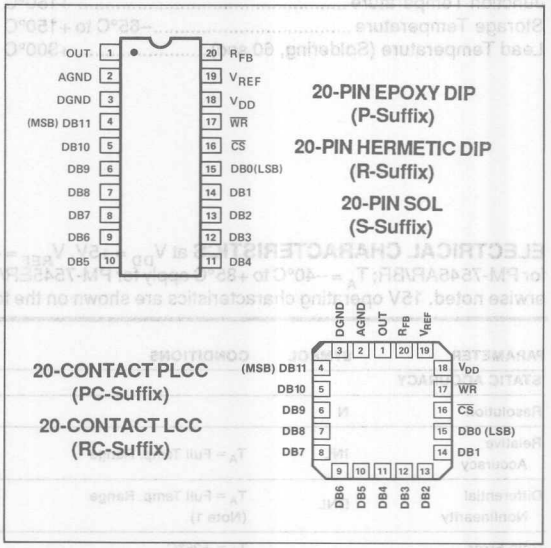
PMI	ADI	TEMPERATURE RANGE
PM7545AR	AD7545GUD	MILITARY
PM7545BR	AD7545UD	
PM7545BR	AD754TD	
PM7545BR	AD7545SD	
PM7545ER	AD7545GCQ	INDUSTRIAL
PM7545FR	AD7545CQ	
PM7545FR	AD7545BQ	
PM7545FR	AD7545AQ	
PM7545GP	AD7545GLN	COMMERCIAL
PM7545FP	AD7545LN	
PM7545FP	AD7545KN	
PM7545FP	AD7545JN	
PM7545FPC	AD7545KP	

GENERAL DESCRIPTION

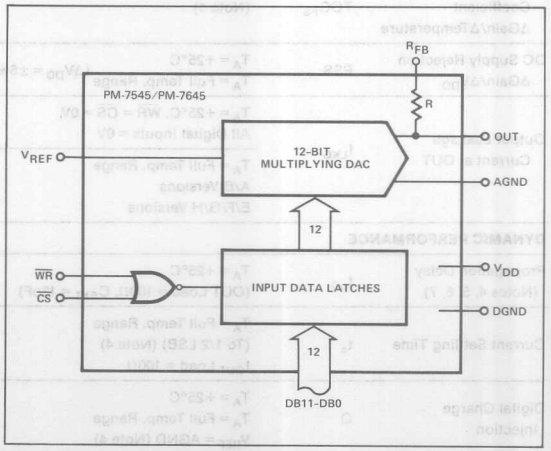
The PM-7545/PM-7645 are 12-bit CMOS multiplying DACs with internal data latches. Digital data is input in a 12-bit wide data format, while $\overline{CS}$ and $\overline{WR}$ control inputs are active low. During this time the latches are transparent allowing digital inputs direct connection to the DAC. When $\overline{WR}$ is returned to logic high, the current data word in the latch is saved.

The PM-7545 operates from 5 to 15 volt power supplies, offering TTL logic compatibility at V_{DD} of 5V and CMOS logic compatibility at V_{DD} of 15V. The PM-7645 is specified for operation at V_{DD} of 15V, offering TTL logic input compatibility.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



otherwise noted.)

V_{DD} to DGND ..... −0.3, +17V
Digital Input Voltage to DGND ..... −0.3, V_{DD}
AGND to DGND ..... −0.3, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0.3, V_{DD}
Operating Temperature Range
Military (AR, BR) Grades ..... −55°C to +125°C
Industrial (ER, FR, FP, FPC, FS) Grades .... −40°C to +85°C
Commercial (GP) Grade ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = −55°C to +125°C apply for PM-7545AR/BR; T_A = −40°C to +85°C apply for PM-7545ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages.

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G MIN	PM-7545A/E/G TYP	PM-7545A/E/G MAX	PM-7545B/F MIN	PM-7545B/F TYP	PM-7545B/F MAX	UNITS
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T_A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C	—	—	±1	—	—	±3	LSB
		T_A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}	PSS	T_A = +25°C (ΔV_{DD} = ±5%)	—	—	0.002	—	—	0.002	%/%
		T_A = Full Temp. Range (ΔV_{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I_{LKG}	T_A = +25°C, $\overline{WR}$ = $\overline{CS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range							
		A/B Versions	—	—	200	—	—	200	
		E/F/G/H Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t_{pD}	T_A = +25°C	—	—	300	—	—	300	ns
		(OUT Load = 100Ω, C_{EXT} = 13pF)	—	—	—	—	—	—	
Current Settling Time	t_s	T_A = Full Temp. Range (To 1/2 LSB) (Note 4) I_{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T_A = +25°C	—	—	300	—	—	300	nVs
		T_A = Full Temp. Range V_{REF} = AGND (Note 4)	—	—	400	—	—	400	
AC Feedthrough at I_{OUT}	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV_{p-p}

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545AR/BR; T_A = –40°C to +85°C apply for PM-7545ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G MIN	PM-7545A/E/G TYP	PM-7545A/E/G MAX	PM-7545B/F MIN	PM-7545B/F TYP	PM-7545B/F MAX	UNITS
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4)	C_{OUT}	T_A = Full Temp. Range DB0-DB11 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	70	—	—	70	pF
C_{OUT}		DB0-DB11 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	μA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0-DB11, $\overline{WR}$, $\overline{CS}$	C_{IN}	T_A = Full Temp. Range V_{IN} = 0 (Note 4)	—	—	8	—	—	8	pF
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram							
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	280	200	—	280	200	—	ns
		T_A = Full Temp. Range	380	270	—	380	270	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	250	175	—	250	175	—	ns
		T_A = Full Temp. Range	380	270	—	380	270	—	
Data Setup Time	t_{DS}	T_A = +25°C	140	100	—	140	100	—	ns
		T_A = Full Temp. Range	210	150	—	210	150	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = +25°C	—	2	100	—	2	100	μA
		T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	5	100	—	5	100	

NOTES:
1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}, DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED and NOT TESTED.
5. From digital input change to 90% of final analog output.
6. All digital inputs = 0V to V_{DD}, or V_{DD} to 0V.
7. Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA.
8. Sample tested at +25°C to ensure compliance.
9. Chip select $\overline{CS}$ must be coincident or present before and/or after write $\overline{WR}$; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.

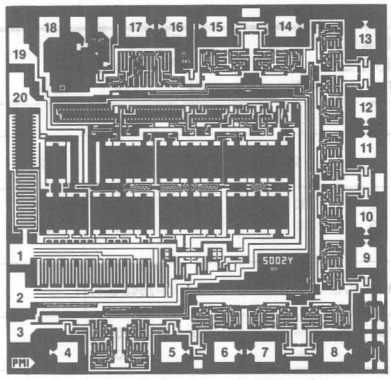
ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545/PM-7645AR/BR; T_A = –40°C to +85°C apply for PM-7545/PM-7645ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545/PM-7645GP, unless otherwise noted.

			PM-7545A/E/G PM-7645A/E/G			PM-7545B/F PM-7645B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T_A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C	—	—	±1	—	—	±3	LSB
		T_A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}	PSS	T_A = +25°C (ΔV_{DD} = ±5%)	—	—	0.002	—	—	0.002	%/%
		T_A = Full Temp. Range (ΔV_{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I_{LKG}	T_A = +25°C, $\overline{WR}$ = $\overline{CS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range							
		A/B Versions	—	—	200	—	—	200	
		E/F/G/H Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t_{pD}	T_A = +25°C (OUT Load = 100Ω, C_{EXT} = 13pF)	—	—	250	—	—	250	ns
Current Settling Time	t_s	T_A = Full Temp. Range (To 1/2 LSB) (Note 4) I_{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T_A = +25°C	—	—	250	—	—	250	nVs
		T_A = Full Temp. Range	—	—	300	—	—	300	
		V_{REF} = AGND (Note 4)							
AC Feedthrough at I_{OUT}	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV_{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4)	C_{OUT}	T_A = Full Temp. Range							
C_{OUT}		DB0-DB11 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	60	—	—	60	pF
		DB0-DB11 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	120	—	—	120	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range, PM-7545	13.5	—	—	13.5	—	—	V
Input Low Voltage	V_{INL}		—	—	1.5	—	—	1.5	
Input High Voltage	V_{INH}	T_A = Full Temp. Range, PM-7645	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	μA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0—DB11, $\overline{WR}$, $\overline{CS}$	C_{IN}	T_A = Full Temp. Range V_{IN} = 0 (Note 4)	—	—	8	—	—	8	pF

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545/PM-7645AR/BR; T_A = –40°C to +85°C apply for PM-7545/PM-7645ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545/PM-7645GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G PM-7645A/E/G MIN	TYP	MAX	PM-7545B/F PM-7645B/F MIN	TYP	MAX	UNITS
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = +25°C	—	2	100	—	2	100	µA
		T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	5	100	—	5	100	
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	PM-7545 A/E/G			PM-7545 B/F/H			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	180	120	—	180	120	—	ns
		T_A = Full Temp. Range	200	150	—	200	150	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	160	100	—	160	100	—	ns
		T_A = Full Temp. Range	240	170	—	240	170	—	
Data Setup Time	t_{DS}	T_A = +25°C	90	60	—	90	60	—	ns
		T_A = Full Temp. Range	120	80	—	120	80	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	PM-7645 A/E/G			PM-7645 B/F/H			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	150	—	—	150	—	—	ns
		T_A = Full Temp. Range	210	—	—	210	—	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	150	—	—	150	—	—	ns
		T_A = Full Temp. Range	210	—	—	210	—	—	
Data Setup Time	t_{DS}	T_A = +25°C	225	—	—	225	—	—	ns
		T_A = Full Temp. Range	300	—	—	300	—	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns

NOTES:
1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED and NOT TESTED.
5. From digital input change to 90% of final analog output.
6. All digital inputs = 0V to V_{DD}; or V_{DD} to 0V.
7. Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA.
8. Sample tested at +25°C to ensure compliance.
9. Chip select $\overline{CS}$ must be coincident or present before and/or after write $\overline{WR}$; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.59 × 2.54mm, 6.58 sq. mm)

1. OUT
2. AGND
3. DGND
4. DB11 (MSB)
5. DB10
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0 (LSB)
16. $\overline{CS}$
17. $\overline{WR}$
18. V_{DD}
19. V_{REF}
20. R_{FB}

WAFER TEST LIMITS at $T_A = 25°C$, $V_{DD} = +5$ or $+15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, AGND = DGND = 0V.

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1/2	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111 1111	±5	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R_{REF}	Pad 19	7/15	kΩ MIN/kΩ MAX
Digital Input High	V_{INH}	$V_{DD} = 5V$ PM-7545 only $V_{DD} = 15V$	2.4 13.5	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 5V$ PM-7545 only $V_{DD} = 15V$	0.8 1.5	V MAX
Digital Input High	V_{INH}	$V_{DD} = 15V$ PM-7645 only	2.4	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 15V$ PM-7645 only	0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSS	$\Delta V_{DD} = ±5\%$	0.002	%/% MAX

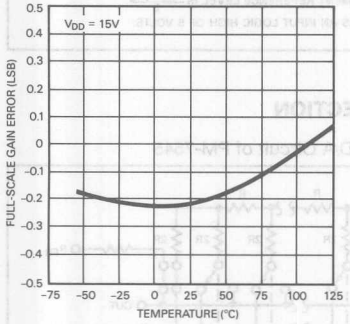
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		7	pF
Output Capacitance	C_{OUT}	DAC Latches Loaded with 0000 0000 0000	50	pF
		DAC Latches Loaded with 1111 1111 1111	110	
Propagation Delay (Notes 2, 3, 4)	t_{pD}	V_{DD} = 15V	140	ns
		V_{DD} = 5V PM-7545 only	230	

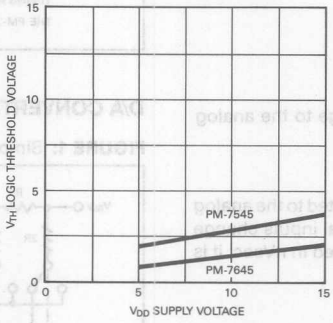
NOTES:
1. These characteristics are for design guidance only and are not subject to test.
2. From digital input change to 90% of final analog output.
3. OUT load = 100Ω, C_{EXT} = 13pF.
4. $\overline{CS}$ = $\overline{WR}$ = 0, DB0 to DB11 = 0V to V_{DD} or V_{DD} to 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

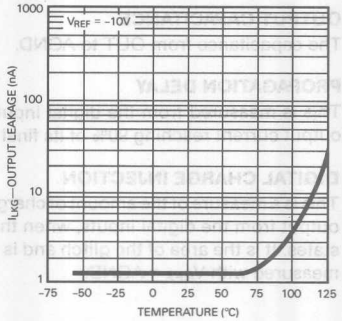
FULL-SCALE GAIN ERROR vs TEMPERATURE



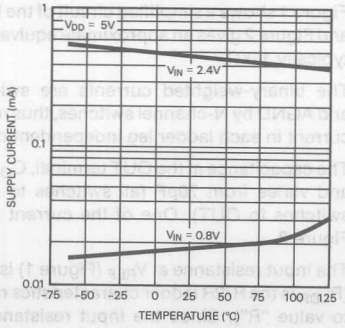
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



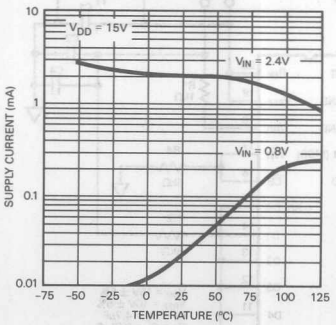
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE PM-7545



SUPPLY CURRENT vs TEMPERATURE PM-7645



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ±1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will increase for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT to AGND.

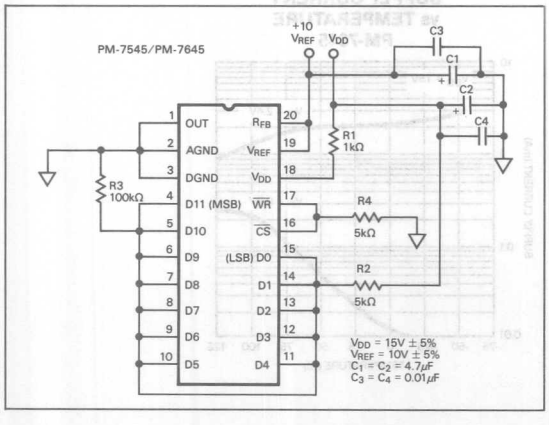
PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

DIGITAL CHARGE INJECTION

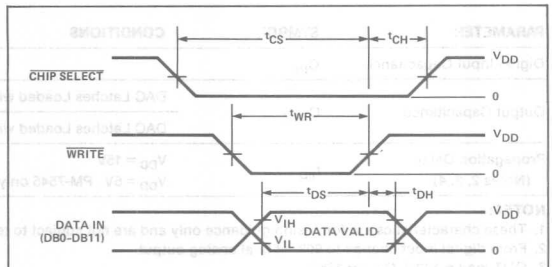
This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with V_{REF} = AGND.

BURN-IN CIRCUIT



LOGIC INFORMATION

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:
$\overline{CS}$ AND $\overline{WR}$ LOW, DAC RESPONDS TO DATA BUS (DB0-DB11) INPUTS.

HOLD MODE:
EITHER $\overline{CS}$ OR $\overline{WR}$ HIGH, DATA BUS (DB0-DB11) IS LOCKED OUT; DAC HOLDS LAST DATA PRESENT WHEN $\overline{WR}$ OR $\overline{CS}$ ASSUMED HIGH STATE.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
THE PM-7645 USES AN INPUT LOGIC HIGH OF 5 VOLTS.

D/A CONVERTER SECTION

FIGURE 1: Simplified D/A Circuit of PM-7545

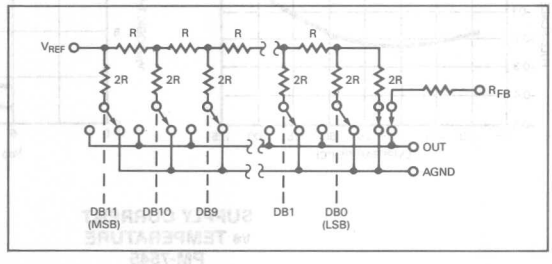


Figure 1 shows a simplified circuit of the D/A Converter section and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

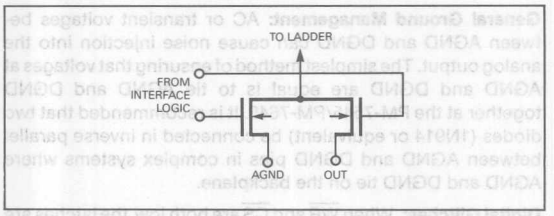
The binary-weighted currents are switched between OUT and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT terminal, C_{OUT}, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT). One of the current switches is shown in Figure 2.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

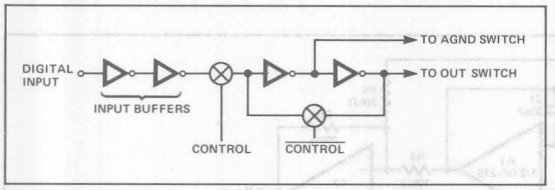
FIGURE 2: N-Channel Current Steering Switch



DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

FIGURE 3: Digital Input Structure



The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible. The PM-7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V. The PM-7645 operates with V_{DD} = 15V only; the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the PM-7545/PM-7645. Resistor R1 is used to trim for full scale. The following versions (PM-7545AR, PM-7545ER, PM-7545GP) have a guaranteed maximum gain error of ±1 LSB at +25°C and V_{DD} = +5V, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

FIGURE 4: Unipolar Binary Operation

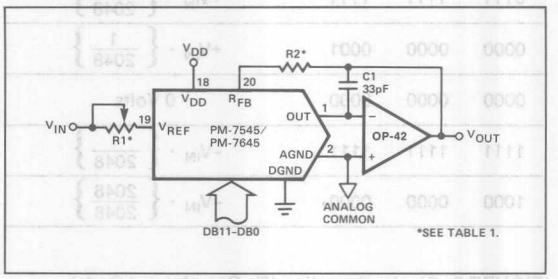


TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	CR	HP/FR/BR	GP/ER/AR
R1	200Ω	100Ω	20Ω
R2	68Ω	33Ω	6.8Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{4095}{4096} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{4096} \right\} = -1/2V_{IN}$
0000	0000	0001	$-V_{IN} \cdot \left\{ \frac{1}{4096} \right\}$
0000	0000	0000	0 Volts

uses offset binary code. The inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

TABLE III: 2's Complement Code Table for Circuit of Figure 5

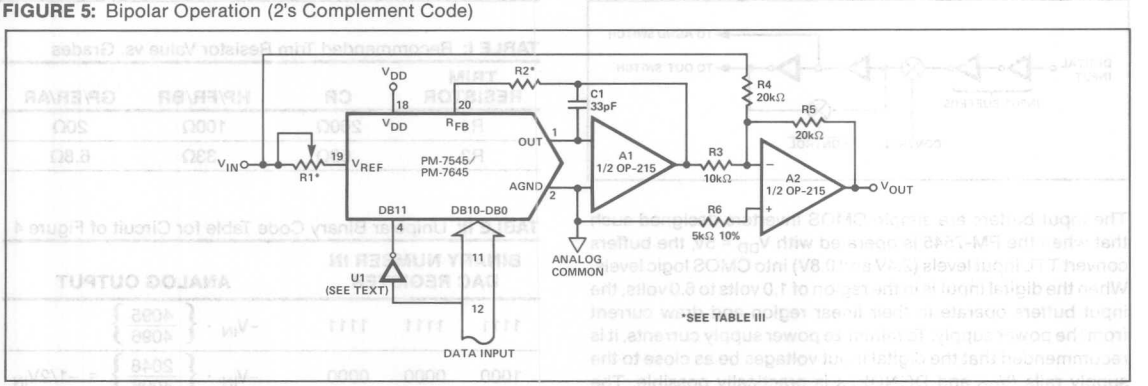
DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \cdot \left\{ \frac{2047}{2048} \right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{2048} \right\}$

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the PM-7545/PM-7645. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which $\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse $\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

FIGURE 5: Bipolar Operation (2's Complement Code)

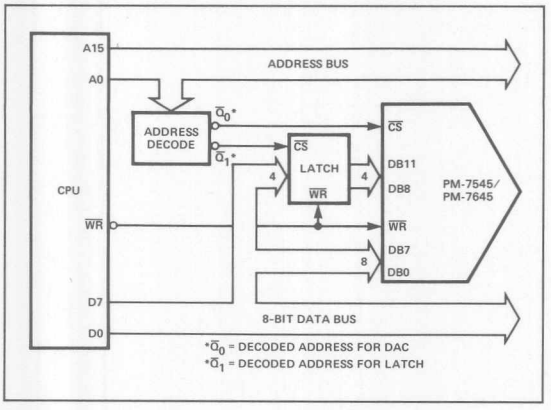


INTERFACING THE PM-7545/PM-7645 TO MICROPROCESSORS

The PM-7545 can be directly interfaced to either an 8 or 16-bit microprocessor via its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ control signals.

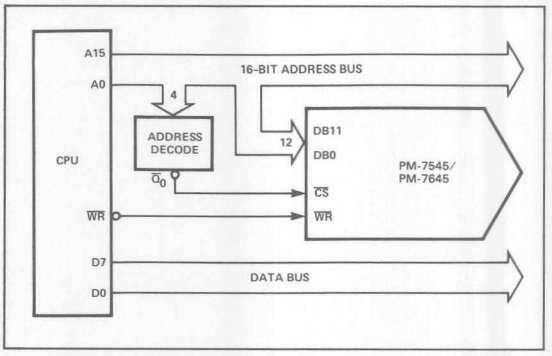
An 8-bit processor interface configuration is shown in Figure 6. It uses two memory addresses, one for the lower 8-bits and one for the upper 4-bits of data into the DAC via the latch.

FIGURE 6: 8-Bit Processor to PM-7545/7645 Interface



Connection to an 8-bit processor with a full 16-bit wide address bus (such as the 6800, 8080, Z80) is shown in Figure 7. The 12 lower address lines are fed directly to the PM-7545; this allows the PM-7545 to use 4k bytes for its address location. The address field of the instruction is organized so that the lower 12-bits contain the DAC data. Data is written into the DAC using a single write instruction.

FIGURE 7: Connecting the PM-7545/7645 to an 8-Bit Microprocessor via the Address Bus

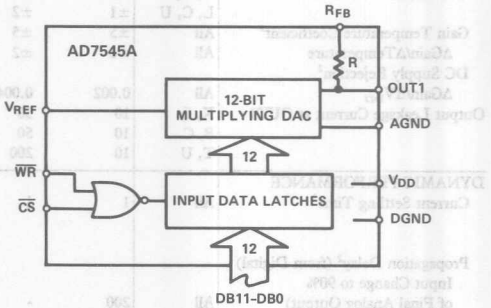


CMOS 12-Bit Buffered Multiplying DAC

AD7545A

FEATURES
Improved Version of AD7545
Fast Interface Timing
All Grades 12-Bit Accurate
Small 20-Pin 0.3" DIP
Low Cost

FUNCTIONAL BLOCK DIAGRAM

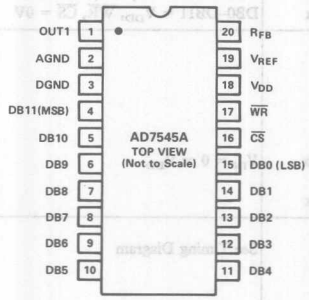


GENERAL DESCRIPTION

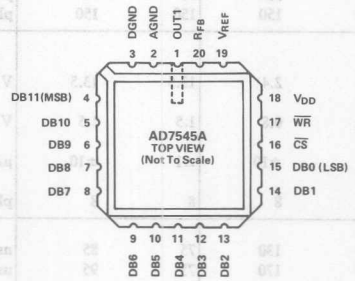
The AD7545A, a 12-bit CMOS multiplying DAC with internal data latches, is an improved version of the industry standard AD7545. This new design features a $\overline{WR}$ pulse width of 100 ns which allows interfacing to a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit-wide word under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing unbuffered operation of the DAC.

PIN CONFIGURATIONS

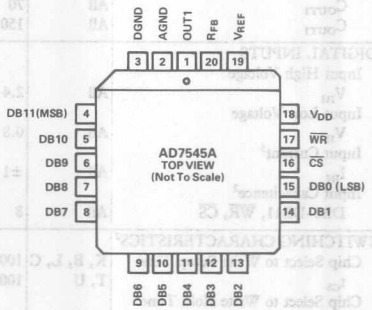
DIP



LCCC



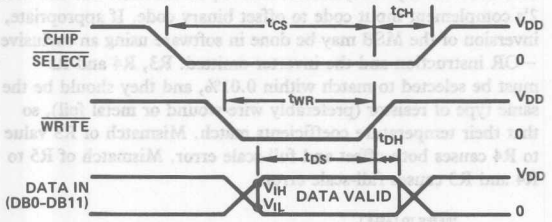
PLCC



Parameter	Version	Limits T_A = +25°C	Limits T_{min}–T_{max}[1]	Limits T_A = +25°C	Limits T_{min}–T_{max}[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	Endpoint Measurement
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed 12-Bit Monotonic Over Temperature
Gain Error	K, B, T	±3	±4	±3	±4	LSB max	Measured Using Internal R_{FB}.
	L, C, U	±1	±2	±1	±2	LSB max	DAC Register Loaded with All 1s.
Gain Temperature Coefficient[2]	All	±5	±5	±5	±5	ppm/°C max	
ΔGain/ΔTemperature	All	±2	±2	±2	±2	ppm/°C typ	
DC Supply Rejection[2]							
ΔGain/ΔV_{DD}	All	0.002	0.004	0.002	0.004	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	K, L	10	50	10	50	nA max	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	B, C	10	50	10	50	nA max	
	T, U	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[2]	All	1	1	1	1	μs max	To 1/2LSB. OUT1 Load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[2] (from Digital)							
Input Change to 90% of Final Analog Output)	All	200	-	150	-	ns max	OUT1 Load= 100Ω, C_{EXT} = 13pF[3]
Digital-to-Analog Glitch Inpulse[2]	All	5	-	5	-	nV sec typ	V_{REF} = AGND. OUT1 Load=100Ω, C_{EXT} = 13pF. DAC Register Alternately Loaded with All 0s and All 1s.
AC Feedthrough[2, 4]							
At OUT1	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
Input Resistance	All	10	10	10	10	kΩ min	Input Resistance TC = −300ppm/°C typ
(Pin 19 to GND)		20	20	20	20	kΩ max	Typical Input Resistance = 15kΩ
ANALOG OUTPUTS							
Output Capacitance[2]							
C_{OUT1}	All	70	70	70	70	pF max	DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	150	150	150	150	pF max	DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[5]							
I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[2]							
DB0–DB11, $\overline{WR}$, $\overline{CS}$	All	8	8	8	8	pF max	
SWITCHING CHARACTERISTICS[2]							
Chip Select to Write Setup Time	K, B, L, C	100	130	75	85	ns min	See Timing Diagram
t_{CS}	T, U	100	170	75	95	ns min	
Chip Select to Write Hold Time							
t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width	K, B, L, C	100	130	75	85	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
t_{WR}	T, U	100	170	75	95	ns min	
Data Setup Time							
t_{DS}	All	100	150	60	80	ns min	
Data Hold Time							
t_{DH}	All	5	5	5	5	ns min	
POWER SUPPLY							
V_{DD}	All	5	5	15	15	V	±5% for Specified Performance
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	100	100	100	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES
[1]Temperature Ranges as follows: K, L Versions = 0 to +70°C; B, C Versions = −25°C to +85°C; T, U Versions = −55°C to +125°C.
[2]Sample tested to ensure compliance.
[3]DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
[5]Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to 75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (KN, LN, KP, LP) Grades	0 to +70°C
Industrial (BQ, CQ, BE, CE) Grades	−25°C to +85°C
Extended (TQ, UQ, TE, UE) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



CIRCUIT INFORMATION – D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545A, and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 15kΩ.

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

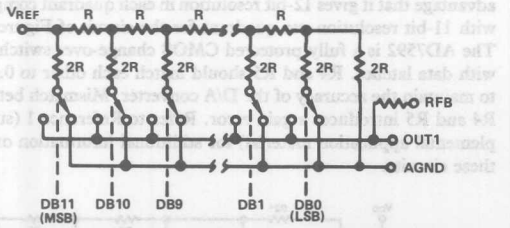


Figure 1. Simplified D/A Circuit of AD7545A

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R. Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

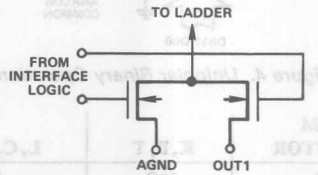


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION – DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

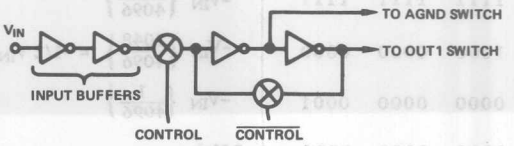


Figure 3. Digital Input Structure

The input buffers are simple CMOS inverters designed such that when the AD7545A is operated with $V_{DD} = 5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545A may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With $V_{DD} = +15V$ the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545A. Resistor R1 is used to trim for full scale. The L, C, U grades have a guaranteed maximum gain error of ±1LSB at +25°C, and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

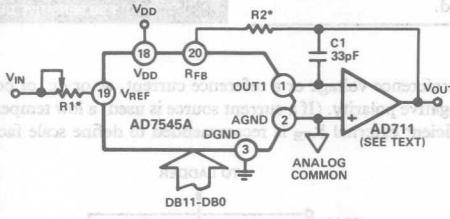


Figure 4. Unipolar Binary Operation

TRIM RESISTOR	K, B, T	L, C, U
R1	50Ω	20Ω
R2	27Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive −OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01%, and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full-scale error. Mismatch of R5 to R4 and R3 causes full-scale error.

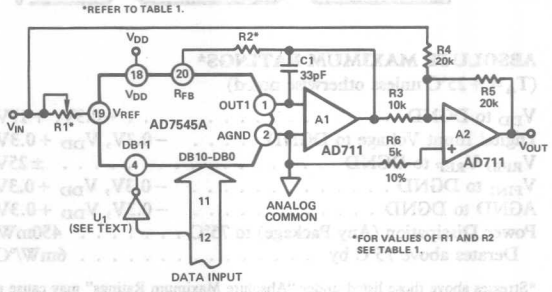


Figure 5. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table III. 2's Complement Code Table for Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error. Refer to Reference 1 (supplemental application material) for additional information on these circuits.

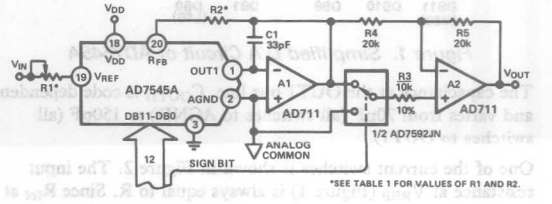


Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

Sign Bit	Binary Numbers in DAC Register			Analog Output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4, 5 and 6 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10V, it is recommended that V_{OS} be no greater than 0.25mV, or (25×10^{-6}) (V_{REF}), over the temperature range of operation. Suitable op amps are AD517 and AD711. The AD517 is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (150μV max for lowest grade) and in most applications will not require an offset trim. The AD711 has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD711 may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545A. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545A AGND and DGND pins (1N914 or equivalent).

Invalid Data: When $\overline{WR}$ and $\overline{CS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low, and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted signals or glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Digital Glitches: Digital glitches result due to capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545A (Pins 1, 2, 19, 20) from the digital pins by a ground track run between Pins 2 and 3 and between Pins 18 and 19 of the AD7545A. Note how the analog pins are at one end (DIP) or side (LCC and PLCC) of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the ditigal-to-analog sections of the AD7545A, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using $V_{DD} = +5$ volts. However, great care should be taken to ensure that the +5V used to power the AD7545A is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545A has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 (such as in Figure 4) are used to adjust full-scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient to CMOS Multiplying DACs", Publication Number E630c–5–3/86.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545A (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545A is, however, protected from the SCR latchup phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545A connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit and should be tied to OUT1 to minimize stray capacitance effects.

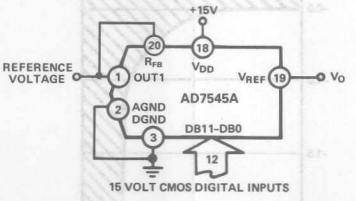


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between

OUT1 and AGND is increased to more than 2.5V, the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

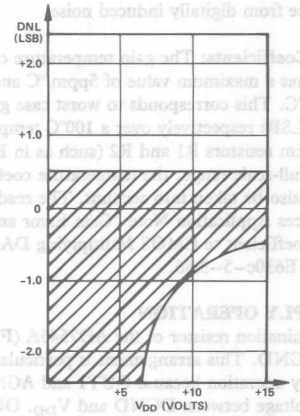


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for all Grades.

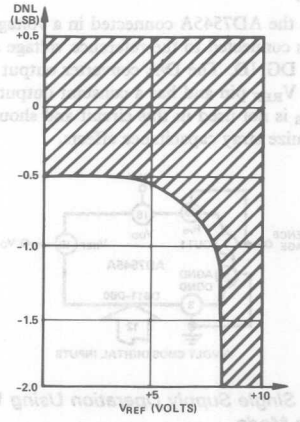


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for all Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2.

There is no need to buffer the V_{REF} input to the AD7545A with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically −300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate the +2.0V at the AD7545A V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

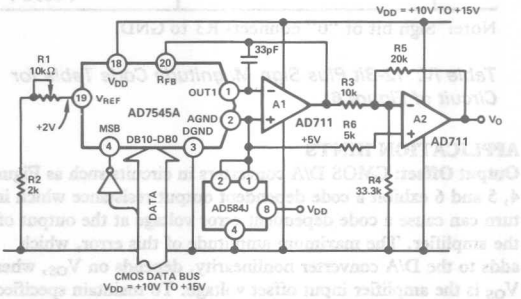


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545A

The AD7545A can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

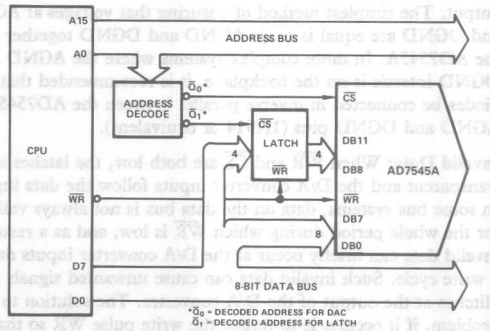


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each AD7545A connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

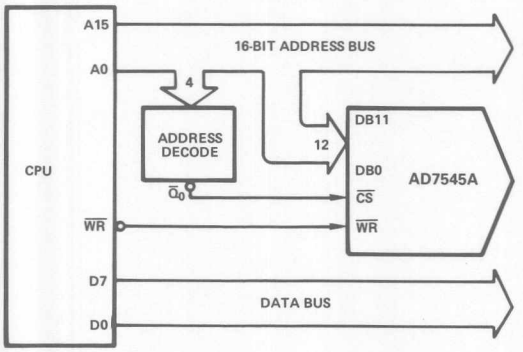


Figure 12. Connecting the AD7545A to 8-Bit Processors via the Address Bus

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Reference 1
CMOS DAC Application Guide available from Analog Devices, Publication Number G872a–15–4/86.

Reference 2
Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs – Application Note, Publication Number E630c–5–3/86.

Reference 3
Analog-Digital Conversion Handbook (Third Edition) available from Prentice-Hall.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy T_{min}–T_{max}	Gain Error T_{min}–T_{max}	Package Option[3]
AD7545AKN	0°C to +70°C	±1/2	±4	N-20
AD7545ALN	0°C to +70°C	±1/2	±2	N-20
AD7545AKP	0°C to +70°C	±1/2	±4	P-20A
AD7545ALP	0°C to +70°C	±1/2	±2	P-20A
AD7545ABQ	−25°C to +85°C	±1/2	±4	Q-20
AD7545ACQ	−25°C to +85°C	±1/2	±2	Q-20
AD7545ABE	−25°C to +85°C	±1/2	±4	E-20A
AD7545ACE	−25°C to +85°C	±1/2	±2	E-20A
AD7545ATQ	−55°C to +125°C	±1/2	±4	Q-20
AD7545AUQ	−55°C to +125°C	±1/2	±2	Q-20
AD7545ATE	−55°C to +125°C	±1/2	±4	E-20A
AD7545AUE	−55°C to +125°C	±1/2	±2	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.
[2]To order MIL-STD-883C, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

2

A15
A0
16-BIT ADDRESS BUS
A
ADDRESS DECODE
CS
RD
D7
D0
DATA BUS
DB11
DB0
CS
RD
AD7584A

ANALOG DEVICES

LC²MOS
Parallel Loading Dual 12-Bit DAC

AD7547

2

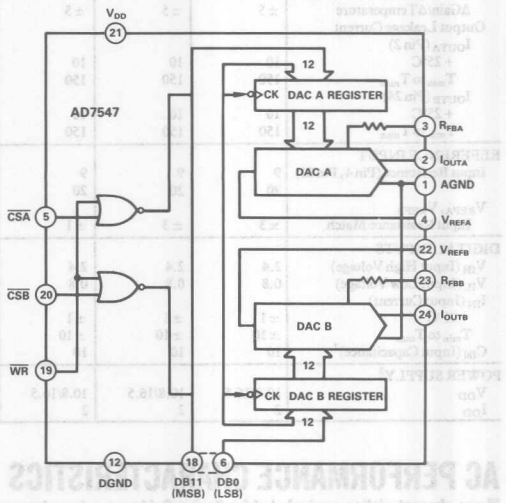
FEATURES

- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Fast Interface Timing

APPLICATIONS

- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

The AD7547 is manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size
   The AD7547 is available in 0.3" wide 24-pin DIPs and SOICs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

AD7547—SPECIFICATIONS[1] (V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current								
I_{OUTA} (Pin 2)								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded with all 0's.
T_{min} to T_{max}	150	150	150	250	250	250	nA max	
I_{OUTB} (Pin 24)								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded with all 0's.
T_{min} to T_{max}	150	150	150	250	250	250	nA max	
REFERENCE INPUT								
Input Resistance (Pin 4, Pin 22)	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14kΩ
	20	20	20	20	20	20	kΩmax	
V_{REFA}, V_{REFB} Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sinewave. DAC registers loaded with all 0's.
V_{REFB} to I_{OUTB}	−70	−65	dB max	
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−84	–	dB typ	V_{REFA} = 20V p-p 10kHz sinewave, V_{REFB} = 0V. Both DACs loaded with all 1's.
V_{REFB} to I_{OUTA}	−84	–	dB typ	V_{REFB} = 20V p-p 10kHz sinewave, V_{REFA} = 0V. Both DACs loaded with all 1's.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0's to all 1's. I_{OUTA}, I_{OUTB} Load = 100Ω, C_{EXT} = 13pF
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	−82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1's.

NOTES

[1]Temperature range as follows: J, K, L Versions: −40°C to +85°C.
A, B, C Versions: −40°C to +85°C.
S, T, U Versions: −55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V)

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	60	80	80	ns min	Data Setup Time
t_2	25	25	25	ns min	Data Hold Time
t_3	80	80	100	ns min	Chip Select to Write Setup Time
t_4	0	0	0	ns min	Chip Select to Write Hold Time
t_5	80	80	100	ns min	Write Pulse Width

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise stated)

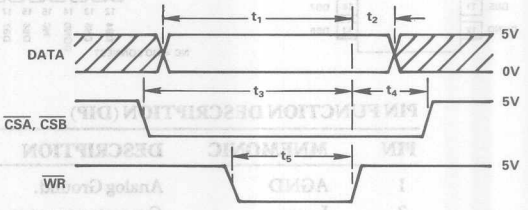
V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGND, ... ±25V
V_{RFBA}, V_{RFBB} to AGND, ... ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, I_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . −40°C to +85°C
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S, T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered

Table I. AD7547 Truth Table



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. t_r = t_f = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 1. Timing Diagram for AD7547

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7547JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7547KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7547LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7547JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7547KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7547LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7547JR	−40°C to +85°C	±1LSB	±6LSB	R-24
AD7547KR	−40°C to +85°C	±1/2LSB	±3LSB	R-24
AD7547LR	−40°C to +85°C	±1/2LSB	±1LSB	R-24
AD7547AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7547BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7547CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7547SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7547TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7547UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7547SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7547TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7547UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

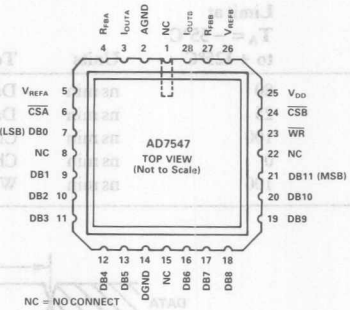


PIN CONFIGURATIONS

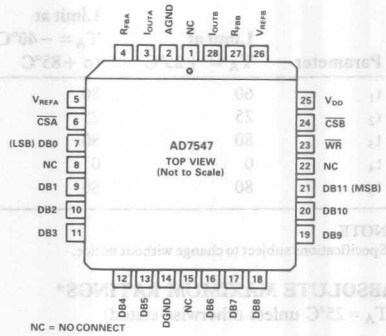
DIP, SOIC



LCCC



PLCC



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGND	Analog Ground.
2	I_{OUTA}	Current output terminal of DACA.
3	R_{FBA}	Feedback resistor for DACA.
4	V_{REFA}	Reference input to DACA.
5	$\overline{CSA}$	Chip Select Input for DAC A. Active low.
6-18	DB0-DB11	12 data inputs, DB0 (LSB) – DB11 (MSB).
12	DGND	Digital Ground.
19	$\overline{WR}$	Write Input. Data transfer occurs on rising edge of $\overline{WR}$. See Table I.
20	$\overline{CSB}$	Chip Select Input for DACB. Active low.
21	V_{DD}	Power supply input. Nominally + 12V to + 15V with ± 10% tolerance.
22	V_{REFB}	Reference input to DACB.
23	R_{FBB}	Feedback resistor of DACB.
24	I_{OUTB}	Current output terminal of DACB.

CIRCUIT INFORMATION

D/A SECTION

The AD7547 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGND. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op-amp (see Figures 4 and 5) to convert the current flowing in I_{OUTA} to a voltage output.

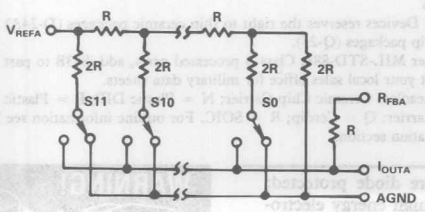


Figure 2. Simplified Circuit Diagram for DACA

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7547. A similar equivalent circuit can be drawn for DACB. Note that AGND is common to both DAC A and DAC B.

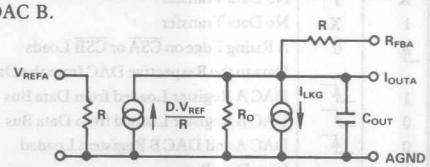


Figure 3. Equivalent Analog Circuit for DACA

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_O is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (AD644, AD712) or separate packages (AD544, AD711, AD OP-27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0's and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0V. Full-scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7547, Gain Error trimming is not necessary. In fixed reference applications, full-scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

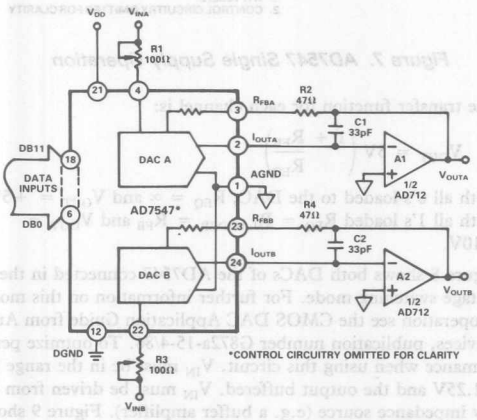


Figure 4. AD7547 Unipolar Binary Operation

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 5 is given in Table III.

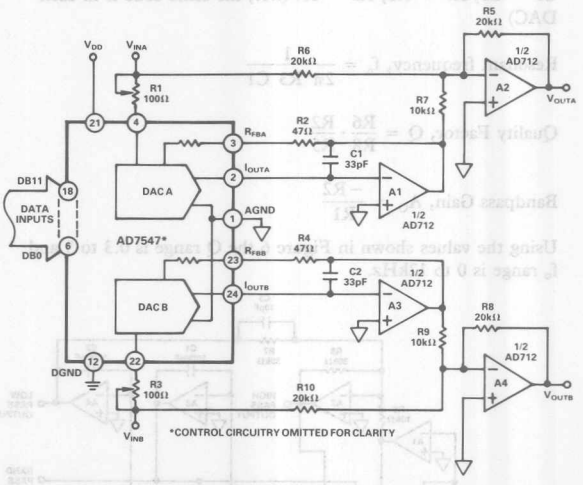


Figure 5. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5.

PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 6 provides three filter outputs: low pass, high pass and bandpass. It is called a State Variable Filter and the particular version shown in Figure 6 uses two AD7547s to control the critical parameters f_o, Q and A_0. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements. Thus, R1 in Figure 6 is controlled by the 12-bit digital word loaded to DAC A of the AD7547. This is also the case with R2, R3 and R4. The fixed resistor R5 is the feedback resistor, R_{FBB}.

$$\text{DAC Equivalent Resistance, Req} = \frac{4096 \times R_{LAD}}{N}$$

where R_{LAD} = DAC Ladder Resistance

N = DAC Digital Code in Decimal. (0<N<4095)

In the circuit of Figure 6:

C1 = C2, R7 = R8, R3 = R4 (i.e., the same code is in each DAC)

$$\text{Resonant frequency, } f_o = \frac{1}{2\pi\ R3\ C1}$$

$$\text{Quality Factor, } Q = \frac{R6}{R8} \cdot \frac{R2}{R5}$$

$$\text{Bandpass Gain, } A_O = \frac{-R2}{R1}$$

Using the values shown in Figure 6 the Q range is 0.3 to 5 and f_o range is 0 to 12kHz.

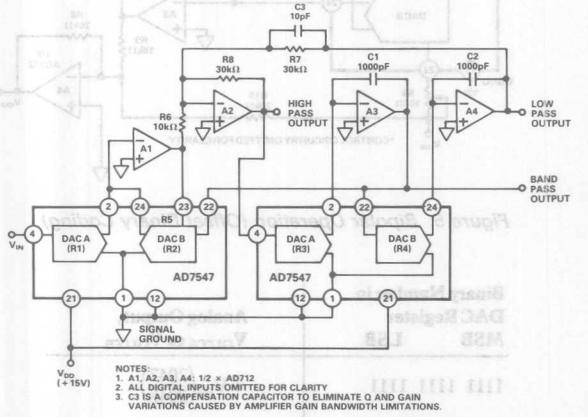


Figure 6. Programmable State Variable Filter

SINGLE SUPPLY APPLICATIONS

DAC A and DAC B of the AD7547 have termination resistors which are tied to the AGND line within the device. This arrangement is ideal for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 7 shows a circuit which provides two +5V to +10V analog outputs by biasing AGND to +5V with respect to DGND, which in this case is also the system ground. The two DAC reference inputs are also tied to system ground.

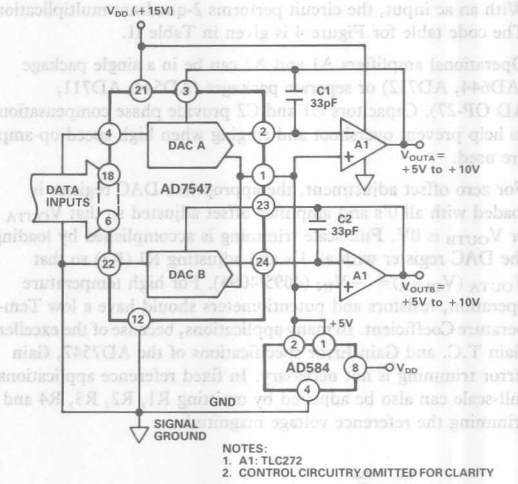


Figure 7. AD7547 Single Supply Operation

The transfer function for each channel is:

$$V_{OUT} = 5V\left(\frac{1 + R_{FB}}{R_{EQ}}\right)$$

With all 0's loaded to the DAC, $R_{EQ} = \infty$ and V_{OUT} = +5V. With all 1's loaded $R_{EQ} = R_{LADDER} = R_{FB}$ and V_{OUT} = +10V.

Figure 8 shows both DACs of the AD7547 connected in the voltage switching mode. For further information on this mode of operation see the CMOS DAC Application Guide from Analog Devices, publication number G872a-15-4/86. To optmize performance when using this circuit, V_{IN} must be in the range 0 to +1.25V and the output buffered. V_{IN} must be driven from a low impedance source (e.g. a buffer amplifier). Figure 9 shows how differential linearity degrades with increasing V_{IN}.

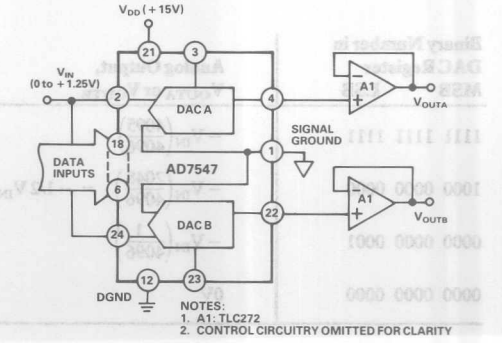


Figure 8. AD7547 Operated in Single Supply, Voltage Switching Mode

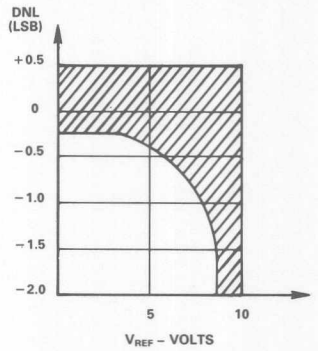


Figure 9. Differential Nonlinearity vs. Reference Voltage for Circuit of Figure 8. V_{DD} = 15V. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are the AD711C and its dual version, the AD712C. These op amps have a wide bandwidth and high slew rate and are recommended for wide bandwidth ac applications. AD711/AD712 settling time to 0.01% is typically 1μs.

Temperature Coefficients: The gain temperature coefficient of the AD7547 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full-scale range as in Figure 4, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Application Note, Publication Number E630c-5-3/86 available from Analog Devices.

High Frequency Considerations: AD7547 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 and C2 in Figures 4 and 5.

Feedthrough: The dynamic performance of the AD7547 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 4 is shown in Figure 10 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

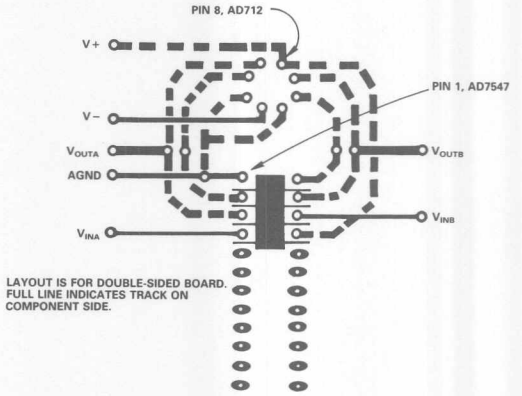


Figure 10. Suggested Layout for Circuit of Figure 4

MICROPROCESSOR INTERFACING

The AD7547 is designed for easy interfacing to 16-bit microprocessors. Figures 11 and 12 show the interface circuits for two of the most popular 16-bit microprocessors; the 8086 and the 68000. Note that the amount of external logic needed is minimal.

Since data is loaded into the DAC registers on the rising edge of WR, the possiblity of invalid data being loaded temporarily to the DAC is removed. This considerably eases the interface circuit design.

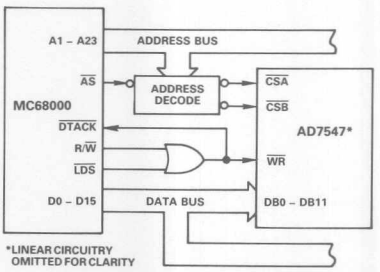


Figure 11. AD7547 – MC68000 Interface

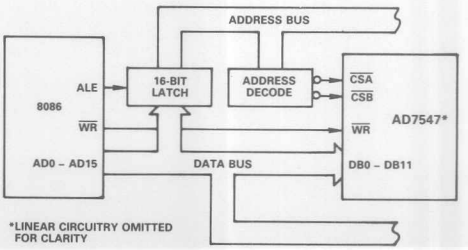


Figure 12. AD7547 – 8086 Interface

LC² MOS
8-Bit μP Compatible 12-Bit DAC

AD7548

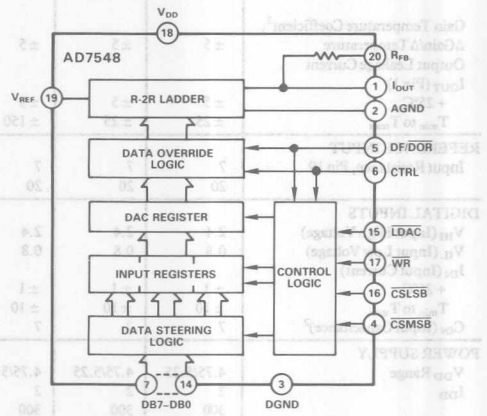
FEATURES

- 8-Bit Bus Compatible 12-Bit DAC
- All Grades 12-Bit Monotonic Over Full Temperature Ranges
- Operation Specified at +5V, +12V or +15V Power Supply
- Low Gain Drift of 5ppm/°C Maximum
- Full 4 Quadrant Multiplication
- Skinny DIP and Surface Mount Packages

APPLICATIONS

- 8-Bit Microprocessor Based Control Systems
- Programmable Amplifiers
- Function Generation
- Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7548 is a 12-bit monolithic CMOS D/A converter for use with 8-bit bus microprocessors. Data is loaded in two bytes to input holding registers as shown in the block diagram opposite. The AD7548 can be configured to accept either left- or right-justified data, least significant byte or most significant byte first, using standard TTL compatible control inputs.

A separate load DAC control input allows the user the choice of updating the analog output coincident with loading new data to the DAC input register or at any time after the data loading event. This feature is especially important in multi-DAC systems where simultaneous update of all DACs is required.

The new Linear Compatible CMOS (LC²MOS) process used in the manufacture of the AD7548 allows precision thin-film linear circuitry and high-speed low-power CMOS logic to be integrated on the same small chip. The high-speed logic allows direct interfacing to most of the popular 8-bit microprocessors.

PRODUCT HIGHLIGHTS

1. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allow direct interfacing to most of the popular 8-bit microprocessors.
2. Guaranteed Monotonicity
   The AD7548 is guaranteed monotonic to 12-bits over the full temperature range for all grades and at all specified supply voltages.
3. Selectable Data Input Format
   Left- or right-justified data, least significant or most significant byte first. This allows the AD7548 to be interfaced with microprocessors using either Motorola or Intel-type data formatting.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin DIP and 20-terminal surface mount packages.
5. Single Supply Operation – See Figure 8.
6. Low Gain Error and Gain Error T.C.

AD7548—SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	Specifications guaranteed over this range
I_{DD}	2	2	2	2	mA max	All digital inputs V_{IL} or V_{IH}
	300	300	300	300	μA max	All digital inputs 0V or V_{DD}

SPECIFICATIONS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over this range
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	1	1	1	1	mA max	All digital inputs 0V or V_{DD}

NOTES
[1]Temperature range as follows: J, K Versions: −40°C to +85°C
A, B Versions: −40°C to +85°C
S, T Versions: −55°C to +125°C
[2]Guaranteed by design but not production tested.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	240	240	290	ns min	Data Valid Setup Time
t_{DH}	50	50	70	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	250	280	320	ns min	Write Pulse Width

TIMING CHARACTERISTICS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	160	190	230	ns min	Data Valid Setup Time
t_{DH}	30	30	50	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	170	200	240	ns min	Write Pulse Width

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V, Output Amplifier is AD544 except where stated)

Parameter	Version	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_A = T_{MIN}, T_{MAX}	V_{DD} = +12V to +15V T_A = +25°C	V_{DD} = +12V to +15V T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time		1.5	–	1	–	µs typ	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Digital to Analog Glitch Impulse		400	–	330	–	nV-sec typ	Measured with V_{REF} = 0V, I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Multiplying Feedthrough Error[3]		3	5	3	5	mV p-p typ	V_{REF} = ±5V, 10kHz sine wave DAC register loaded with all 0s.
Total Harmonic Distortion		−85	–	−85	–	dB typ	V_{REF} = 6V rms @ 1kHz. DAC register loaded with all 1s.
Power Supply Rejection $\Delta GAIN/\Delta V_{DD}$		±0.015	±0.03	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance I_{OUT} (Pin 1)		200 100	200 100	200 100	200 100	pF max pF max	DAC register loaded with all 1s. DAC register loaded with all 0s.
Output Noise Voltage Density (10Hz–100kHz)		15	–	15	–	nV/√Hz typ	Measured between R_{FB} and I_{OUT}

NOTES
[1]Guaranteed by design but not production tested.
[2]Temperature range as follows: J, K Versions: −40°C to +85°C
A, B Versions: −40°C to +85°C
S, T Versions: −55°C to +125°C
[3]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (D-20) to DGND.
Specifications subject to change without notice.

(T_A = +25°C unless otherwise noted)

V_{DD} (pin 18) to DGND	+17V
V_{REF} (pin 19) to AGND	±25V
V_{RFB} (pin 20) to AGND	±25V
Digital Input Voltage (pins 4–17) to DGND	−0.3V, V_{DD}+0.3V
$V_{PIN\ 1}$ to DGND	−0.3V, V_{DD}+0.3V
AGND to DGND	−0.3V, V_{DD}+0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Commercial (J, K versions)	−40°C to +85°C
Industrial (A, B versions)	−40°C to +85°C
Extended (S, T versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

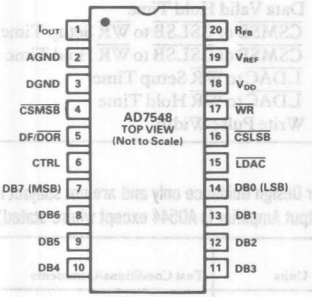
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

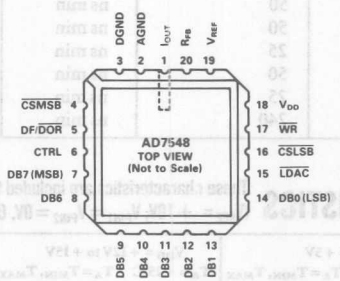


PIN CONFIGURATIONS

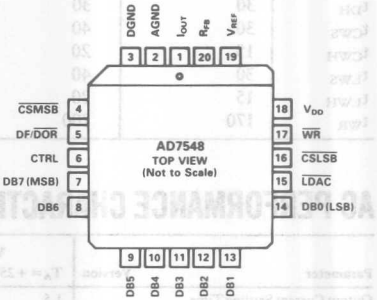
DIP, SOIC



LCCC



PLCC



ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option[3]
AD7548JN	−40°C to +85°C	±1LSB	±6LSB	N-20
AD7548KN	−40°C to +85°C	±1/2LSB	±3LSB	N-20
AD7548JP	−40°C to +85°C	±1LSB	±6LSB	P-20A
AD7548KP	−40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7548JR	−40°C to +85°C	±1LSB	±6LSB	R-20
AD7548KR	−40°C to +85°C	±1/2LSB	±3LSB	R-20
AD7548AQ	−40°C to +85°C	±1LSB	±6LSB	Q-20
AD7548BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-20
AD7548SQ	−55°C to +125°C	±1LSB	±6LSB	Q-20
AD7548TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-20
AD7548SE	−55°C to +125°C	±1LSB	±6LSB	E-20A
AD7548TE	−55°C to +125°C	±1/2LSB	±3LSB	E-20A

NOTE

[1]Analog Devices reserves the right to ship ceramic (package outline D-20) packages in lieu of cerdip (package outline Q-20) packages.

[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.

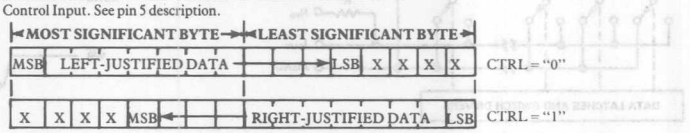
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	I_{OUT}	DAC current OUT bus. Normally terminated at virtual ground of output amplifier.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
5	DF/$\overline{DOR}$	Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held HIGH.

DF/$\overline{DOR}$	CTRL	FUNCTION
0	0	DAC register contents overridden by all 0's
0	1	DAC register contents overriden by all 1's
1	0	Left-justified input data selected
1	1	Right-justified input data selected

6	CTRL	Control Input. See pin 5 description.



X = Don't care states.

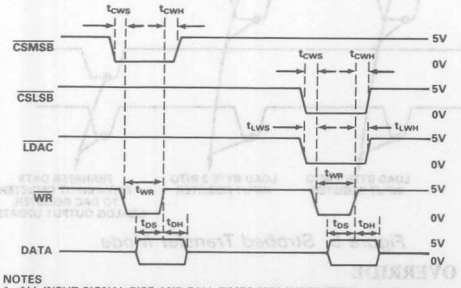
7	DB7	Data Bit 7. Most Significant Bit (MSB).
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	Data Bit 0. Least Significant Bit (LSB).
15	$\overline{LDAC}$	Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
16	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
17	$\overline{WR}$	WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register.

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	FUNCTION
0	1	0	1	Load LS Byte to Input Register.
0	1	0	0	Load LS Byte to Input Register and DAC Register.
0	0	1	1	Load MS Byte to Input Register.
0	0	1	0	Load MS Byte to Input Register and DAC Register.
0	1	1	0	Load Input Register to DAC Register.
1	X	X	X	No Data Transfer

18	V_{DD}	+5V to +15V Supply Input.
19	V_{REF}	Reference Voltage Input.
20	R_{FB}	Feedback Resistor. Used for normal D/A conversion.

CONTROL INPUT INFORMATION

Figure 1a shows the data load timing diagram for the AD7548. Figure 1b shows the simplified input control structure of the AD7548.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V.
   FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

Figure 1a. AD7548 Timing Diagram

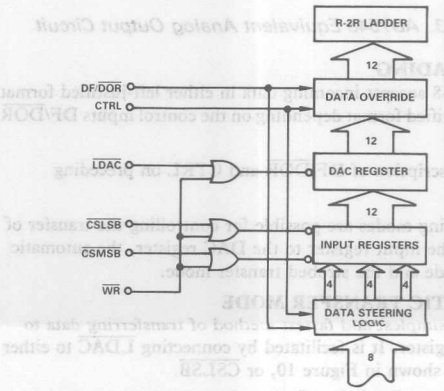


Figure 1b. Simplified AD7548 Input Control Structure

GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used, which steers binarily weighted currents between I_{OUT} and AGND, thus maintaining a constant current in each ladder leg independent of the switch state.

The input resistance at V_{REF} is constant and equal to the value "R" in Figure 2. Since the input resistance is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor).

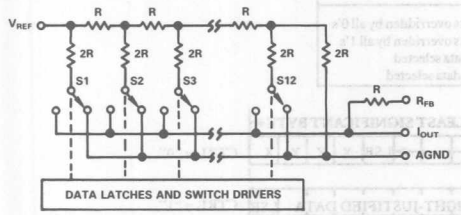


Figure 2. AD7548 Simplified Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7548 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O, denotes the equivalent output resistance of the DAC which varies with input code (excluding all 0's code) from 0.8R to 2R, where R is typically 11kΩ. C_{OUT} is the capacitance due to the current steering switches and varies from about 50pF to 120pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of R-2R ladder, N.

For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

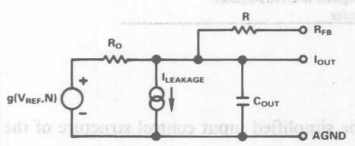


Figure 3. AD7548 Equivalent Analog Output Circuit

DATA LOADING

The AD7548 accepts incoming data in either left-justified format or right-justified format depending on the control inputs DF/$\overline{DOR}$ and CTRL.

(See pin description of DF/$\overline{DOR}$ and CTRL on preceding page).

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, the automatic transfer mode and the strobed transfer mode.

AUTOMATIC TRANSFER MODE

This is the simplest and fastest method of transferring data to the DAC register. It is facilitated by connecting $\overline{LDAC}$ to either $\overline{CSMSB}$, as shown in Figure 10, or $\overline{CSLSB}$.

Figure 4 shows the timing diagram for automatic transfer of 8 +4-bit data to the DAC register. The first write cycle loads the first byte of data to the input register. The second write cycle loads the second byte of data to the input register and automatically transfers both bytes to the DAC register.

Updating a single byte (High or Low) in the DAC register can be achieved in one write cycle using the automatic transfer mode.

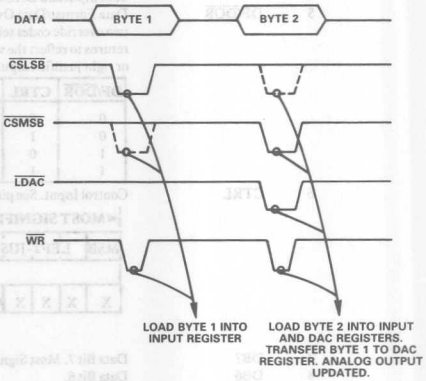


Figure 4. Automatic Transfer Mode

STROBED TRANSFER MODE

Figure 5 shows the timing diagram for the strobed transfer of 8 +4-bit data to the DAC register. Three write cycles are required for this transfer mode. The first two write cycles sequentially load bytes 1 and 2 into the input register. The third write cycle transfers data from the input register to the DAC register.

The strobed transfer mode allows the DAC registers of several AD7548's to be updated simultaneously, as shown in Figure 13, by means of a master strobe signal connected to the $\overline{LDAC}$ of each device.

A single byte of data (High or Low) can be transferred to the DAC register in two write cycles using the strobed transfer mode.

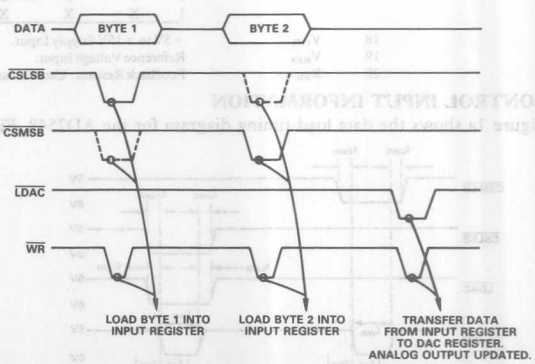


Figure 5. Strobed Transfer Mode

DATA OVERRIDE

The contents of the DAC register can be overridden by pulling DF/$\overline{DOR}$ (pin 5) LOW. The CTRL (pin 6) input then determines whether the DAC register data is overidden by all 0s (CTRL LOW) or all 1s (CTRL HIGH). This feature allows the user to calibrate the AD7548 in circuits such as Figure 6 without calling on the microprocessor to load calibration data.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary operation. With a dc input voltage or current (positive or negative polarity) applied at pin 19, the circuit is a unipolar D/A converter. With an ac input voltage the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

Table I shows the code relationship for the circuit of Figure 6.

For full scale trimming the DAC register is loaded with 1111 1111 1111. This is most easily accomplished by using the data override function. R1 is then adjusted for $V_{OUT} = -V_{IN}$ (4095/4096). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps.

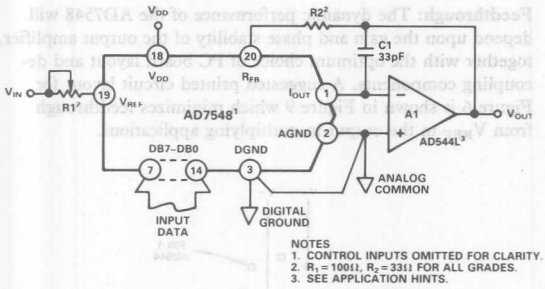


Figure 6. Unipolar Binary Operation

Table I. Unipolar Binary Code Table for Circuit of Figure 6

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The circuit uses offset binary input coding. However, 2's complement coding can be accommodated if the MSB is inverted (done in software) before data is loaded into the DAC.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively one can omit R1 and R2 and adjust the ratio of R3 and R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5.

R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably metal film) so that their temperature coefficients match. Mismatch of R3 to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

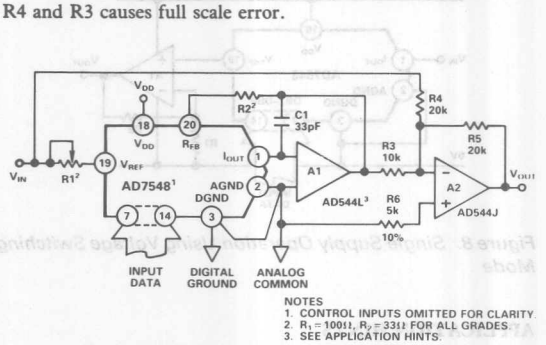


Figure 7. Bipolar Operation (Offset Binary Coding)

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 7

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

SINGLE SUPPLY OPERATION

Figure 8 shows the AD7548 connected in a voltage switching mode. The input voltage is connected to I_{OUT}. The D/A converter output voltage is taken from the V_{REF} pin and has a constant impedance equal to R. R_{FB} is not used in this circuit. The input voltage V_{IN} must always be positive with respect to AGND in order to prevent an internal diode from turning on. To maintain linearity the input voltage should remain within 2.5V of AGND with V_{DD} from +12V to +15V.

The output voltage V_{OUT} of Figure 8 is expressed as

$$V_{OUT} = (V_{IN})(D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

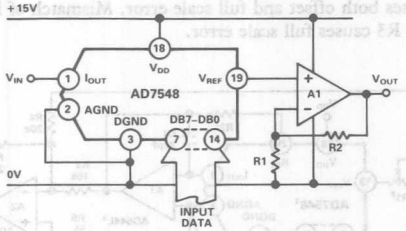


Figure 8. Single Supply Operation Using Voltage Switching Mode

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 6 and 7 exhibit a code dependent output resistance which in turn cause a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7548. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7548 AGND and DGND pins (1N914 or equivalent).

Temperature Coefficients: The gain temperature coefficient of the AD7548 has a maximum value of 5ppm/°C and typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

High Frequency Considerations: AD7548 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7548 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 6 is shown in Figure 9 which minimizes feedthrough from V_{REF} to the output in multiplying applications.

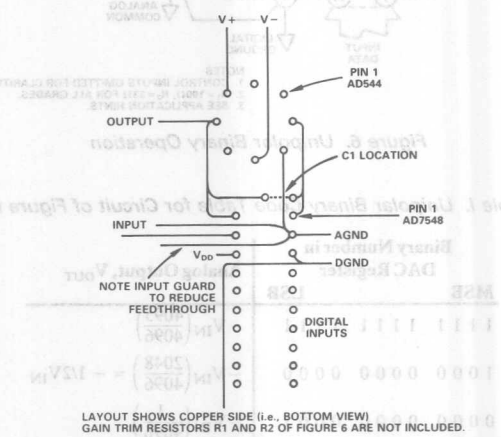


Figure 9. Suggested Layout for AD7548 and Op Amp

For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

MICROPROCESSOR INTERFACING

AD7548 – MC6800 INTERFACE

A typical 6800 configuration using the automatic transfer mode of the AD7548 is shown in Figure 10. Table III gives a sample loading routine written in re-entrant form. Data load and store instructions use extended addressing. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The data is considered right-justified with the four most significant bits occupying the lower half of XXYY + 1. The AD7548 is assigned a base address of PPQQ. This address selects the low byte register of the AD7548. Address PPQQ + 1 selects both the high byte register and the $\overline{\text{LDAC}}$ control input.

AD7548 – 8085A INTERFACE

Figure 11 shows a typical AD7548 to 8085A microprocessor interface configured for automatic transfer of 8 + 4-bit right-justified data. Table IV gives a sample loading routine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The four most significant data bits occupy the lower half of XXYY + 1. As before, addresses PPQQ and PPQQ + 1 select the $\overline{\text{CSLSB}}$ and $\overline{\text{CSMSB}}/\overline{\text{LDAC}}$ control inputs respectively. Since only two instructions (LHLD, SHLD) are required to both fetch and load the 12-bit data word to the AD7548, it may be more efficient to insert these instructions as required in the main program rather than use a subroutine such as illustrated here.

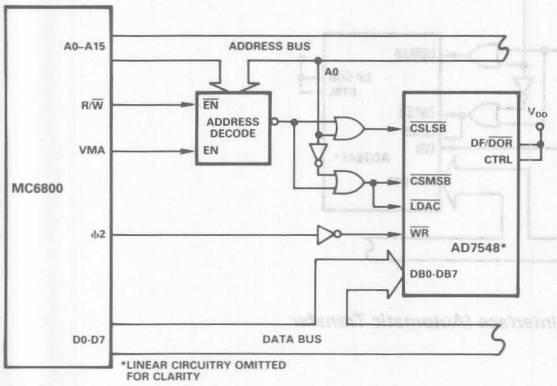


Figure 10. AD7548 – MC6800 Interface (Automatic Transfer Mode)

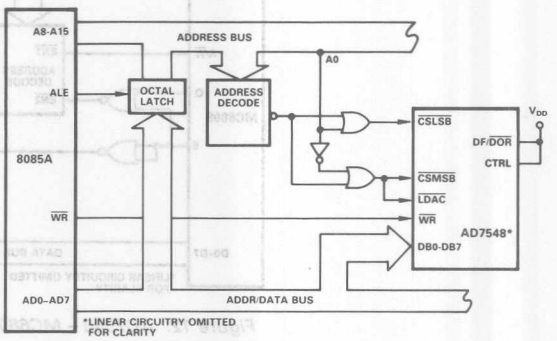


Figure 11. AD7548 – 8085A Interface (Automatic Transfer Mode)

Table III. Sample Routine for AD7548 – MC6800 Interface

	JSR	WWZZ	Jump to AD7548 subroutine
WWZZ	PSH A		Push A onto stack
	TPA		
	PSH A		Push CCR onto stack
	LDA A	$XXYY	
	STA A	$PPQQ	Load low byte to AD7548
	LDA A	$XXYY + 1	
	STA A	$PPQQ + 1	Load high byte to AD7548 and update analog output
	PUL A		
	TAP		Pull CCR from stack
	PUL A		Pull A from stack
	RTS		Return to main program

Table IV. Sample Routine for AD7548–8085A Interface

	CALL	7548	
7548	PUSH	PSW	Push register contents onto stack
	PUSH	H	
	LHLD	XXYY	Fetch 12-bit data
	SHLD	PPQQ	Load 12-bit data
	POP	H	Pop register contents from stack
	POP	PSW	
	RET		Return to main program

The AD7548 can be interfaced to the MC6809 microprocessor as shown in Figure 12 for automatic transfer of 8 + 4-bit data. Similar to the 8085A instructions LHLD and SHLD, the 6809 has two instructions to fetch and store 12-bit (16-bit) data to the AD7548, LDD and STD. However, in the 6809, the high byte of data is moved first, then the low byte (this is the opposite of the 8085A). This means that if the 12-bit data is assumed to reside at addresses XXYY and XXYY + 1 then XXYY must contain the high byte. It also means that the address decoding logic of Figure 11 must be slightly changed so that the even-order to load the high byte first. In this automatic transfer configuration $\overline{LDAC}$ is tied to the $\overline{CSLSB}$ input. The AD7548 analog output can thus be updated using only two instructions as follows:

```
LDD   $XXYY
STD   $PPQQ
```

The strobed transfer configuration is shown in Figure 13 with a dedicated decoder output assigned to each chip select input. The common $\overline{LDAC}$ signal allows simultaneous update of both AD7548 DAC registers.

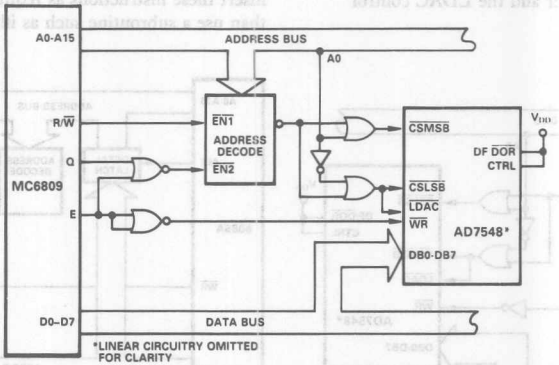


Figure 12. AD7548 – MC6809 Interface (Automatic Transfer Mode)

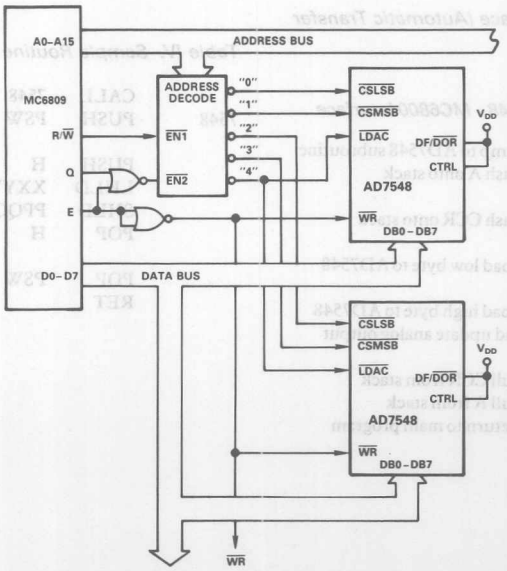


Figure 13. AD7548 – MC6809 Interface (Strobed Transfer Mode)

Figure 14 shows a typical AD7548 to 6502 microprocessor interface configured for automatic transfer of right-justified data. As a programming example, Figure 15 shows a flow chart for producing a 12-bit (4095-step-max) voltage ramp under 6502 control. Index registers X and Y of the 6502 form a 12-bit counter with the X-register holding the low byte of data and the Y-register the high byte. Table V shows the program listing. The X-register is compared with FF_H and the Y-register with 10_H to determine when the ramp voltage has reached its maximum value (FFF_H). By changing the comparison data in the program the maximum ramp output voltage can be varied from levels corresponding to FFF_H down to 000_H. In the program listing of Table V the AD7548 has been assigned contiguous addresses 0400 (low byte) and 0401 (high byte and DAC register).

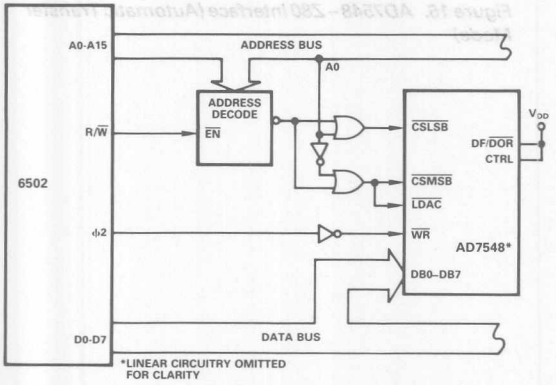


Figure 14. AD7548 – 6502 Interface (Automatic Transfer Mode)

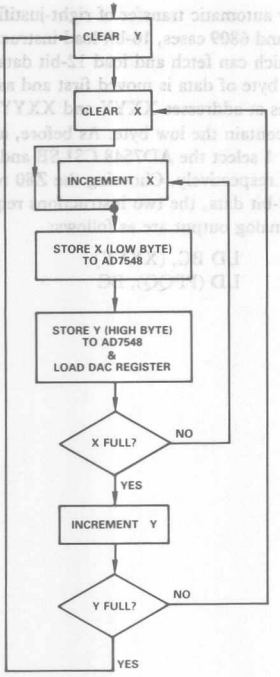


Figure 15. Flow Chart for Voltage Ramp Generation

Table V. Program Listing for Figure 15

ADDRESS	OP-CODE	MNEMONIC	OPERAND
0000	A0	LDY	# 00
01	00		
02	A2	LDX	# 00
03	00		
04	4C	JMP	0008
05	08		
06	00		
07	E8	INX	
08	8E	STX	0400
09	00		
0A	04		
0B	8C	STY	0401
0C	01		
0D	04		
0E	E0	CPX	# FF
0F	FF		
10	D0	BNE	0007
11	F5		
12	C8	INY	
13	C0	CPY	# 10
14	10		
15	D0	BNE	0002
16	EB		
17	FO	BEQ	0000
0018	E7		

AD7548 – Z80 INTERFACE

Figure 16 shows a typical AD7548 to Z80 microprocessor interface configured for automatic transfer of right-justified data. Similar to the 8085A and 6809 cases, 16-bit load instructions are available in the Z80 which can fetch and load 12-bit data to the AD7548. Since the low byte of data is moved first and assuming the 12-bit data resides at addresses XXYY and XXYY + 1, address XXYY must contain the low byte. As before, addresses PPQQ and PPQQ + 1 select the AD7548 $\overline{CSLSB}$ and $\overline{CSMSB}$/$\overline{LDAC}$ control inputs respectively. Choosing the Z80 register pair BC to hold the 12-bit data, the two instructions required to update the AD7548 analog output are as follows:

```
LD BC, (XXYY)
LD (PPQQ), BC
```

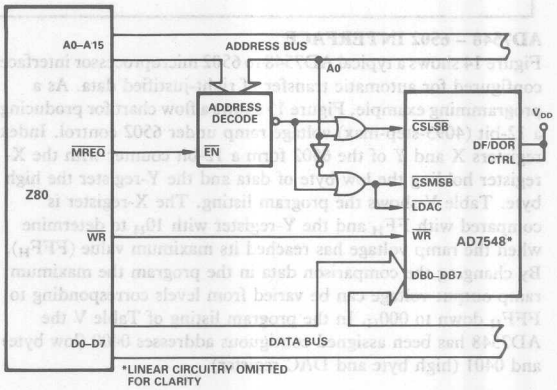


Figure 16. AD7548 – Z80 Interface (Automatic Transfer Mode)

CMOS 8-Bit μP Compatible 12-Bit D/A Converter

PM-7548

FEATURES

- 8-Bit Bus Compatible 12-Bit DAC
- Versatile Microprocessor Interface with Selectable Data Input Format and Data Override
- Faster Interface Timing
- High Accuracy: Low ±1/2 LSB INL Error Over Temperature and ±1 LSB Gain Error
- Superior Power Supply Rejection from +5V to +15V . . . . . 0.001%/% Max
- Low Feedthrough Error and Digital Charge Injection
- Data Inputs Designed with ESD Protective Circuitry
- Narrow (0.3") DIP Packages Suitable for Auto-Insertion
- Superior Direct Replacement for AD7548
- Full Four Quadrant Multiplication
- Available in Die Form

APPLICATIONS

- Process Control
- Programmable Amplifiers
- Digitally Controlled Power Supplies
- Digitally Controlled Attenuators
- Digitally Controlled Filters

ORDERING INFORMATION †

		PACKAGE: 20-PIN		
GAIN ERROR	NON-LINEARITY	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	±1/2 LSB	PM7548AR	PM7548ER	PM7548GP
±2 LSB	±1/2 LSB	PM7548BR	PM7548FR	—
±2 LSB	±1/2 LSB	PM7548BRC/883	PM7548FP	—
±2 LSB	±1/2 LSB	—	PM7548FPC	—
±2 LSB	±1/2 LSB	—	PM7548FS	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7548AR	AD7548TD	MIL
PM7548BR	AD7548SD	
PM7548ER	AD7548BQ	IND
PM7548FR	AD7548AQ	
PM7548GP	AD7548KN	COM
PM7548FP	AD7548JN	
PM7548FPC	AD7548JP	

GENERAL DESCRIPTION

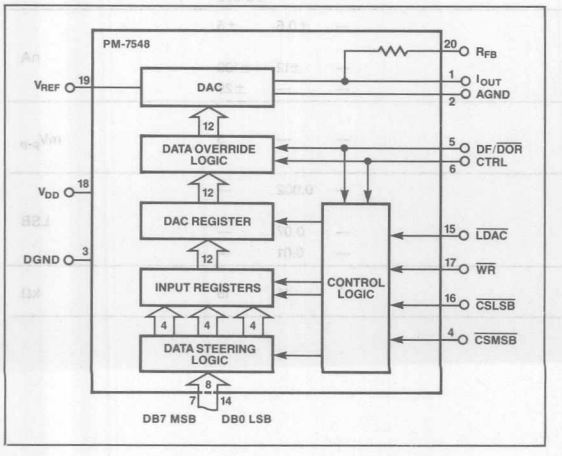
The PM-7548 is a 12-bit resolution, current output, CMOS D/A converter with a microprocessor interface for 8-bit busses. Its improved accuracy and inputs designed with ESD protection circuitry make it a superior pin-compatible replacement to the industry standard 7548. These performance improvements permit the upgrading of existing designs with greater accuracy and ruggedness. Tighter linearity and gain error specifications may permit a reduced circuit parts count through the elimination of trimming components. The PM-7548 is available in standard plastic and CERDIP packages that are compatible with auto-insertion equipment.

The PM-7548's versatile interface allows data to be loaded into an output register in two bytes. The PM-7548 can accept data right or left justified, least or most significant byte first, under microprocessor control. Faster interface timing minimizes microprocessor wait states.

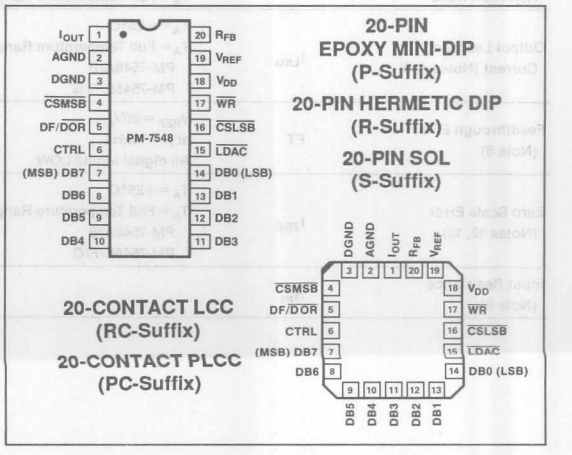
Analog output updating and the loading of new data into the input registers may be coincident or separated in time by use of the $\overline{\text{LDAC}}$ control input. This allows user control of data update and analog output update timing.

Data override control allows full-scale or zero-scale analog outputs without altering the contents of the DAC registers. This permits the user to perform circuit calibration without the need to load calibration data into the DAC registers.

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} (to GND) ..... +17V
V_{REF} (to GND) ..... ±25V
V_{RFB} (to GND) ..... ±25V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3 to V_{DD}
Operating Temperature Range
AR/BR/BRC Versions ..... –55°C to +125°C
ER/FR/FP/FPC/FS Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and dice. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{OUT} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7548AR/BR/BRC, T_A = –40°C to +85°C for PM-7548ER/FR/FP/FPC/FS, and T_A = 0°C to +70°C for PM-7548GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548 MIN	PM-7548 TYP	PM-7548 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Integral Nonlinearity (Note 1)	INL		—	—	1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7548A/E/G	—	—	1/2	LSB
		PM-7548B/F	—	—	1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				LSB
		PM-7548A/E/G	—	—	1	
		PM-7548B/F	—	—	2	
		T_A = Full Temperature Range				
		PM-7548A/E/G	—	—	2	
		PM-7548B/F	—	—	3	
Gain Temperature Coefficient (Note 6)	TCG_{FS}		—	±1	±5	ppm/°C
Power Supply Rejection Ratio	PSRR	T_A = +25°C	—	—	±0.001	%/%
		T_A = Full Temperature Range	—	—	±0.002	
Output Leakage Current (Notes 4, 5)	I_{LKG}	T_A = +25°C	—	±0.5	±5	nA
		T_A = Full Temperature Range				
		PM-7548A/B	—	±12	±100	
		PM-7548E/F/G	—	—	±25	
Feedthrough Error (Note 6)	FT	V_{REF} = $20V_{p-p}$ at f = 10kHz All digital inputs LOW	—	—	5	mV_{p-p}
Zero Scale Error (Notes 12, 13)	I_{ZSE}	T_A = +25°C	—	0.002	—	LSB
		T_A = Full Temperature Range				
		PM-7548A/B	—	0.07	—	
		PM-7548E/F/G	—	0.01	—	
Input Resistance (Note 9)	R_{IN}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{OUT} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7548AR/BR/BRC, T_A = –40°C to +85°C for PM-7548ER/FR/FP/FPC/FS, and T_A = -°C to +70°C for PM-7548GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7548 MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7, 8)	t_S	T_A = +25°C	–	–	1	µs
Digital-to-Analog Glitch Energy (Notes 6, 11)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC Register Loaded Alternately with All 0s and All 1s	–	–	200	nVs
Total Harmonic Distortion (Note 6)	THD	V_{REF} = 6V_{rms} @ 1kHz DAC Register Loaded with All 1s	–	–	–90	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz Measured Between R_{FB} and I_{OUT}	–	–	13	nV/√Hz
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 10)	I_{IL}	V_{IN} = 0V to +15V	–	–	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	–	–	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IH}	–	–	140	pF
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IL}	–	–	70	pF
TIMING CHARACTERISTICS (Note 6)						
Data Valid Setup Time	t_{DS}	T_A = +25°C T_A = Full Temperature Range	160 210	– –	– –	ns
Data Valid Hold Time	t_{DH}	T_A = +25°C T_A = Full Temperature Range	10 10	– –	– –	ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time	t_{CWS}	T_A = +25°C T_A = Full Temperature Range	0 0	– –	– –	ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time	t_{CWH}	T_A = +25°C T_A = Full Temperature Range	0 0	– –	– –	ns
$\overline{LDAC}$ to $\overline{WR}$ Setup Time	t_{LWS}	T_A = +25°C T_A = Full Temperature Range	0 0	– –	– –	ns
$\overline{LDAC}$ to $\overline{WR}$ Hold Time	t_{LWH}	T_A = +25°C T_A = Full Temperature Range	0 0	– –	– –	ns
Write Pulse Width	t_{WR}	T_A = +25°C T_A = Full Temperature Range	120 120	– –	– –	ns

NOTES:
1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT}; digital inputs = V_{IL}.
5. Specification also applies for AGND with all digital inputs = V_{IL}.
6. Guaranteed by design and not subject to test.
7. I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital inputs = 0V to V_{DD} or V_{DD} to 0V.
8. Extrapolated to 1/2 LSB: t_S = Propagation Delay (t_{PD}) + 9τ, where τ = measured first time constant of the final RC decay.
9. Absolute temperature coefficient is approximately +50ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. V_{REF} = +10V, all digital inputs = 0V.
13. Calculated from worst case R_{REF}: I_{ZSE} (in LSBs) = (R_{REF} x I_{LKG} x 4096)/V_{REF}.
14. Calculated from $e_N = \sqrt{4K\,TRB}$
    where: K = Boltzmann Constant, J/°K
    T = Resistor Temperature, °K
    R = Resistance, Ω
    B = Bandwidth, Hz.

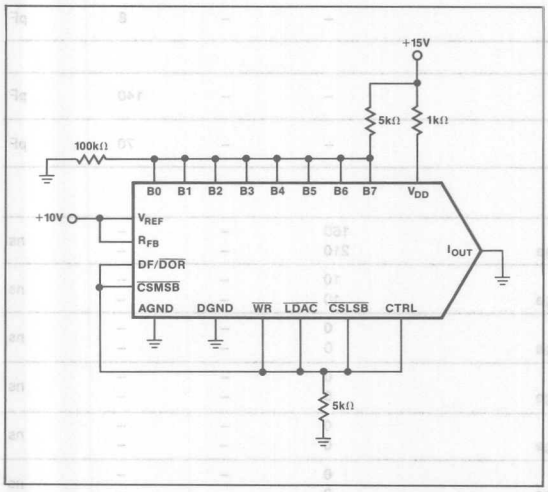
ELECTRICAL CHARACTERISTICS at V_{DD} = +12V or +15V; V_{REF} = +10V; V_{OUT} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7548AR/BR/BRC, T_A = –40°C to +85°C for PM-7548ER/FR/FP/FPC/FS, and T_A = 0°C to +70°C for PM-7548GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548 MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Range	V_{DD}		11.4	—	15.75	V
Supply Current	I_{DD}	All digital inputs = V_{INH} or V_{INL}	—	—	3	mA
		All digital input = 0V or V_{DD}	—	—	1	

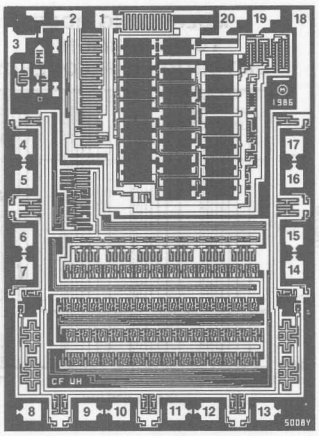
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7548AR/BR/BRC, T_A = –25°C to +85°C for PM-7548ER/FR, and T_A = 0°C to +70°C for PM-7548GP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548 MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Range	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{INH} or V_{INL}	—	—	2	mA
		All digital input = 0V or V_{DD}	—	120	300	μA

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.096 × 0.130 inch, 12,480 sq. mils
(2.46 × 3.33mm, 8.20 sq. mm)

1. I_{OUT}
2. AGND
3. DGND
4. $\overline{CSMSB}$
5. DF/$\overline{DOR}$
6. CTRL
7. DB7 (MSB)
8. DB6
9. DB5
10. DB4
11. DB3
12. DB2
13. DB1
14. DB0 (LSB)
15. $\overline{LDAC}$
16. $\overline{CSLSB}$
17. $\overline{WR}$
18. V_{DD}
19. V_{REF}
20. R_{FB}

2

WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT} = AGND = 0V, T_A = +25°C, unless otherwise noted.

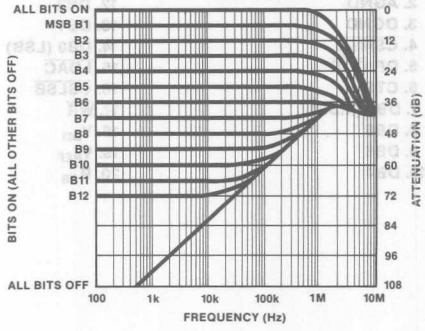
PARAMETER	SYMBOL	CONDITIONS	PM-7548GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1/2	LSB MAX
Gain Error (Note 1)	G_{FSE}		±1	LSB MAX
Power Supply Rejection	PSRR	ΔV_{DD} = ±5%	±0.001	%/% MAX
Output Leakage Current (I_{OUT})	I_{LKG}	V_{DD} = +15V Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{DD} = +15V V_{IN} = 0 to 15V	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	V_{DD} = +15V Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	3 1	mA MAX

NOTES:
1. Using internal feedback resistor.

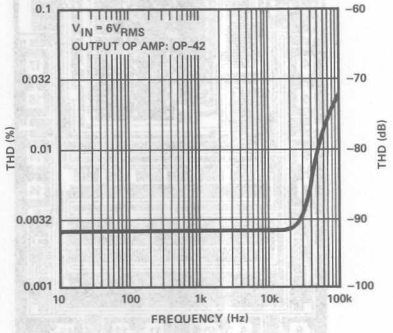
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

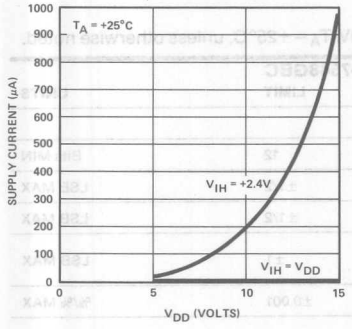
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



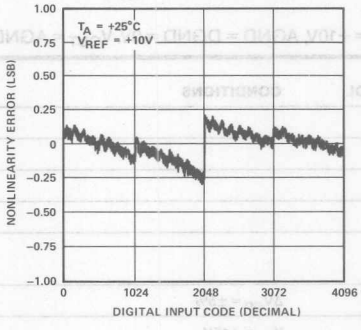
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



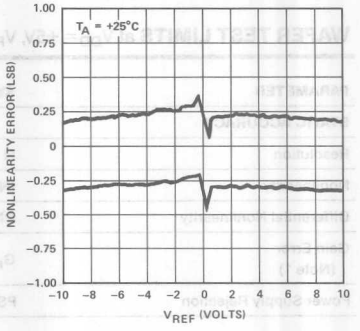
SUPPLY CURRENT vs SUPPLY VOLTAGE



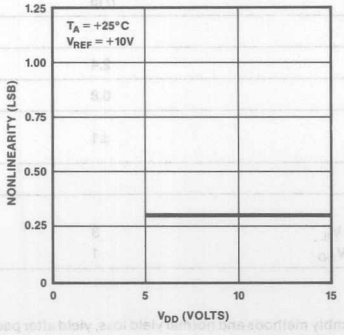
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +5V OR +15V)



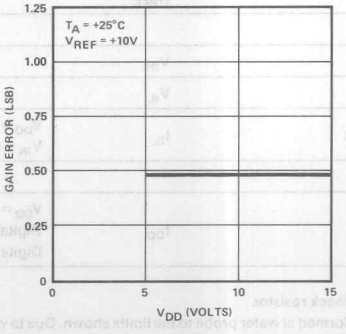
NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +5V OR +15V)



NONLINEARITY vs SUPPLY VOLTAGE



GAIN ERROR vs SUPPLY VOLTAGE



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT} terminal with all digital inputs LOW, or on AGND terminal when all inputs are HIGH.

OUTPUT LEAKAGE CURRENT

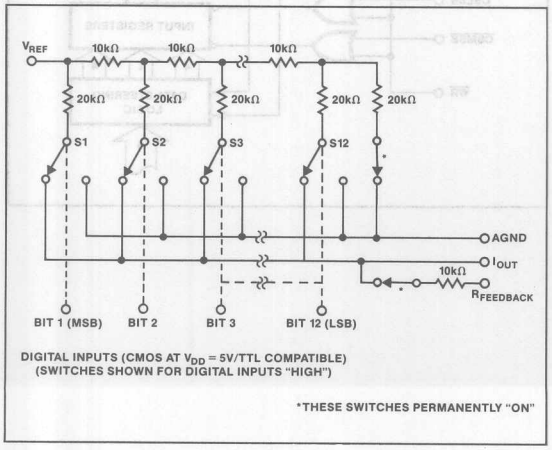
Current appearing at I_{OUT} when all digital inputs are LOW, or at AGND when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7548 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data-steering and control logic, and two data registers.

The digital circuitry forms a versatile interface between the 12-bit DAC and an 8-bit data bus. Several data formats can be accomodated, single or double buffering is available, and a data override function allows calibration data to be loaded into the DAC without altering data stored in the buffer registers.

FIGURE 1: Simplified DAC Circuit



A simplified circuit of the PM-7548 is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT} or AGND. Switching current to ground or I_{OUT} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings chart.

The PM-7548 design incorporates a regulator circuit which assures TTL compatibility at any V_{DD} from +5V to +15V across the full military temperature range. This regulator also contributes to the DAC's exceptional PSRR performance, and maintains timing performance independent of supply voltage.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

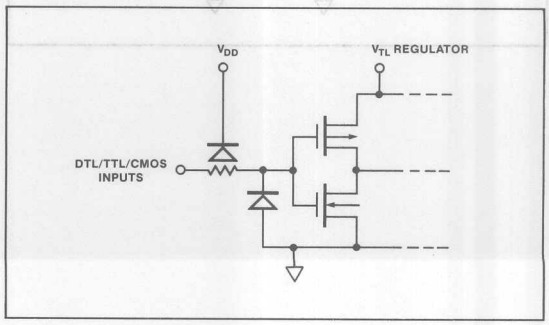
To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7548 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

FIGURE 2: Digital Input Protection



well below dangerous levels during static discharge conditions.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to AGND when all data bits are LOW and to I_{OUT} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

FIGURE 3: PM-7548 Equivalent Circuit (All Inputs LOW)

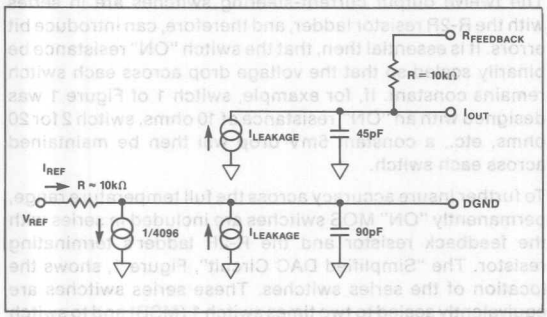


FIGURE 4: PM-7548 Equivalent Circuit (All Digital Inputs HIGH)

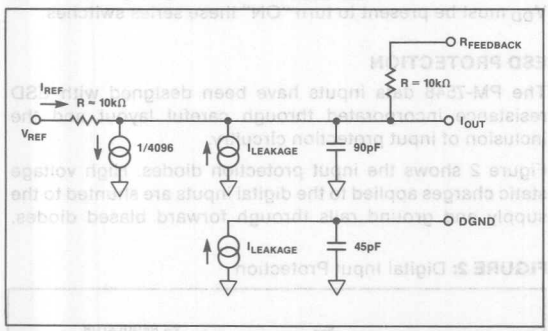
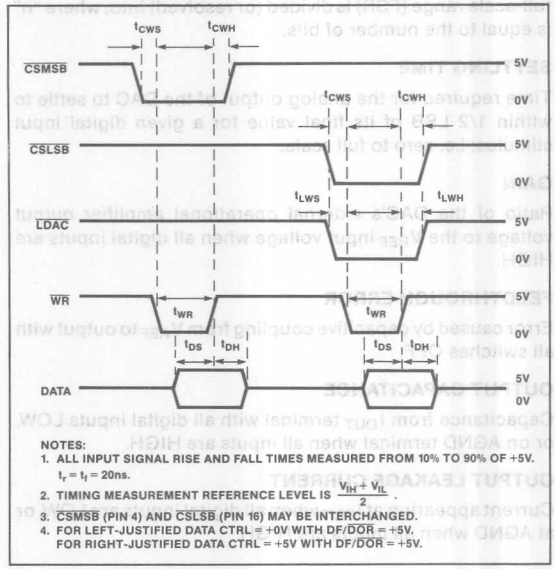
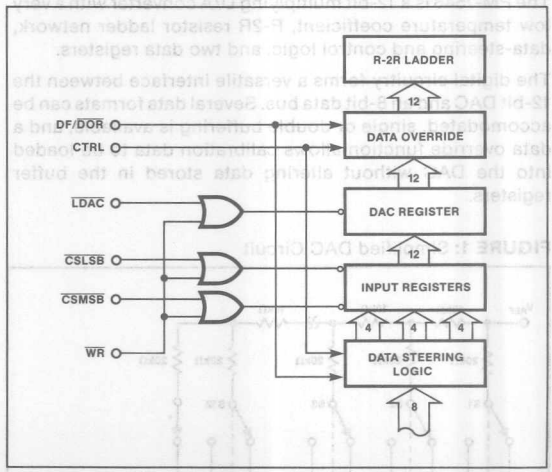


FIGURE 5: PM-7548 Data Input and Control Timing Diagram



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V.
   FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

FIGURE 6: Simplified PM-7548 Input Control Structure



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 11kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7548. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers' feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 9 and 10).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

INTERFACE INPUT DESCRIPTION

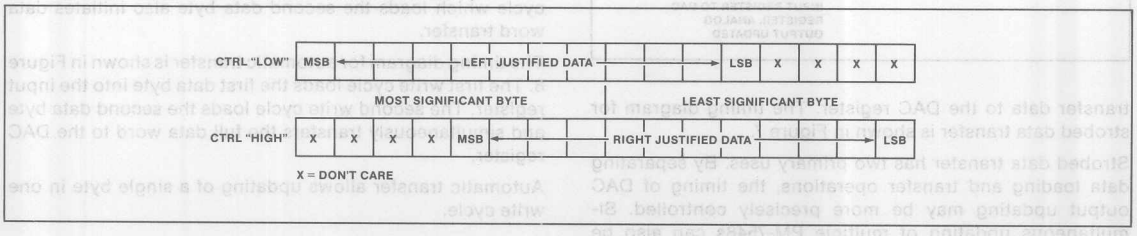
$\overline{\text{CSMSB}}$ (Pin 4) - Chip Select Most Significant Byte. Active Low. Selected either with $\overline{\text{WR}}$, to load most significant byte data into the input register, or with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ to load data into both input and DAC registers.

$\overline{\text{CSLSB}}$ (Pin 16) - Chip Select Least Significant Byte. Active Low. Selected either with $\overline{\text{WR}}$ to load least significant byte data into the input register, or with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ to load data into both input and DAC registers.

DF/$\overline{\text{DOR}}$ (Pin 5) - Data Format/Data Override. When LOW, DAC is forced to full-scale or zero-scale output as selected by CTRL. Use of Data Override does not affect data held in DAC register. When DF/$\overline{\text{DOR}}$ is HIGH, CTRL selects either right or left data input format. DF/$\overline{\text{DOR}}$ is normally held HIGH.

DF/$\overline{\text{DOR}}$	CTRL	Function
0	0	DAC forced to zero-scale (all zeros)
0	1	DAC forced to full-scale (all ones)
1	0	Left-justified data format selected
1	1	Right-justified data format selected

CTRL (Pin 6) - Control Input (Refer also to DF/$\overline{\text{DOR}}$)



$\overline{\text{LDAC}}$ (Pin 15) - Load DAC Input. Active Low. Selected, with other interface inputs, to load DAC register from input register or external data bus.

$\overline{\text{WR}}$ (Pin 17) - Write Input. Active Low. Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

$\overline{\text{WR}}$	$\overline{\text{CSMSB}}$	$\overline{\text{CSLSB}}$	$\overline{\text{LDAC}}$	Function
0	1	0	1	Load LSByte to Input Register
0	1	0	0	Load LSByte to Input and DAC Registers
0	0	1	1	Load MSByte to Input Register
0	0	1	0	Load MSByte to Input and DAC Registers
0	1	1	0	Load Input Register to DAC Register
1	X	X	X	No Data Transfer

DATA LOADING AND TRANSFER

DATA INPUT AND TRANSFER

Data may be loaded into the input register in either a left- or right-justified format. The data format is selected through the DF/$\overline{\text{DOR}}$ and CTRL inputs (refer to Interface Input Description).

Data transfer, from the input register to the DAC register, can be automatic upon loading of the second data byte into the input register or can occur at a later time through a strobed transfer.

STROBED DATA TRANSFER MODE

Strobed data transfer allows the full 12-bit digital word to be loaded into the input register and transferred to the DAC register at some later time. This transfer mode requires three write cycles: two to load the new digital word, and a third to

FIGURE 7: Strobed Data Transfer Mode

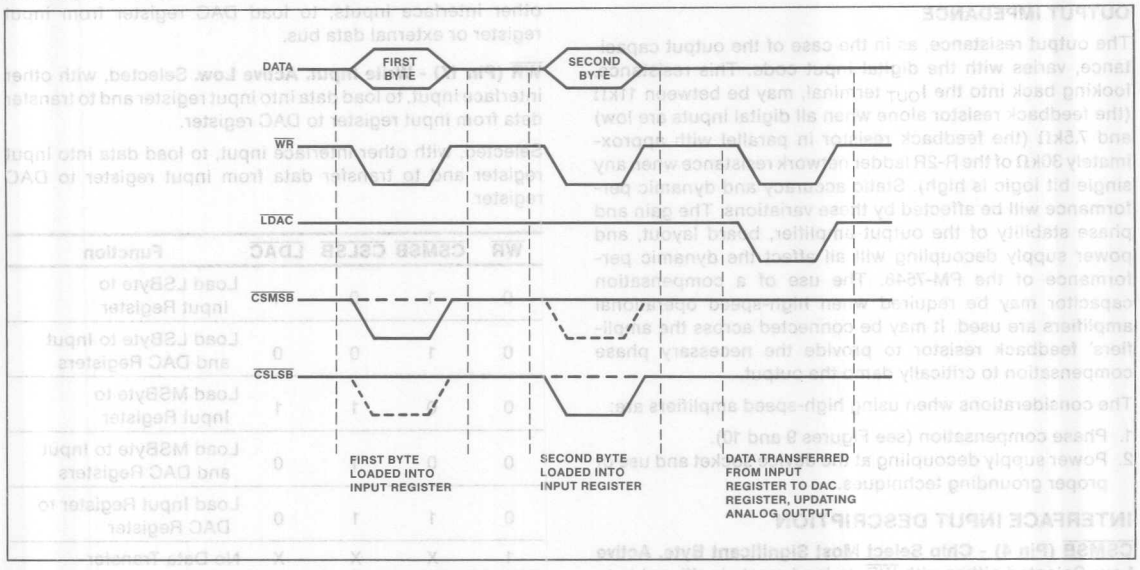
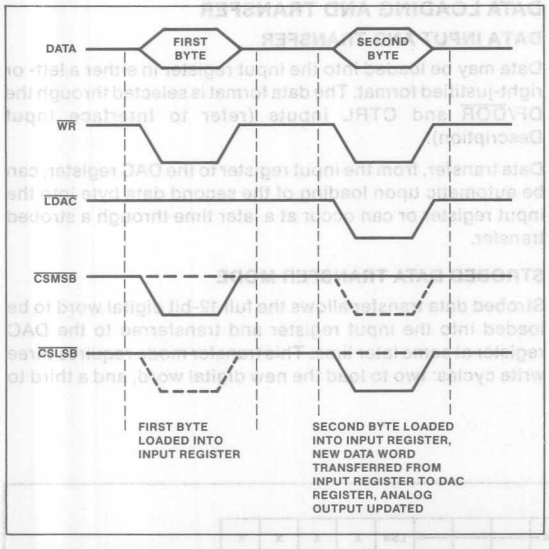


FIGURE 8: Automatic Data Transfer Mode



transfer data to the DAC register. The timing diagram for strobed data transfer is shown in Figure 7.

Strobed data transfer has two primary uses. By separating data loading and transfer operations, the timing of DAC output updating may be more precisely controlled. Simultaneous updating of multiple PM-7548s can also be accomplished by the use of a master strobe signal applied to the $\overline{\text{LDAC}}$ pins of the DACs.

A single data byte can be updated in two write cycles with the strobed transfer mode.

DATA OVERRIDE

System calibration typically requires full-scale and zero-scale DAC outputs (digital words all 1s and 0s respectively). The PM-7548's data override ability allows full-scale and zero-scale outputs without altering the contents of the DAC and input registers, or requiring the controlling microprocessor to load calibration data.

Data override is accessed by setting the DF/$\overline{\text{DOR}}$ pin LOW. The CTRL pin then selects the override code: CTRL LOW yields all 0s, CRTL HIGH yields all 1s.

AUTOMATIC DATA TRANSFER MODE

Data may be transferred automatically from the input register to the DAC register while loading the second (High or Low) byte. This is the simplest and fastest transfer mode, requiring only two write cycles to load and transfer a complete new digital word. This operation can be simplified by connecting $\overline{\text{LDAC}}$ directly to either $\overline{\text{CSMSB}}$ or $\overline{\text{CSLSB}}$ so that the write cycle which loads the second data byte also initiates data word transfer.

The timing diagram for automatic transfer is shown in Figure 8. The first write cycle loads the first data byte into the input register. The second write cycle loads the second data byte and simultaneously transfers the full data word to the DAC register.

Automatic transfer allows updating of a single byte in one write cycle.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT} and AGND (pins 1 and 2) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, (see Figures 9 and 10). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 15pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

2

FIGURE 9: Unipolar Binary Operation with High Accuracy Op Amp (2-Quadrant)

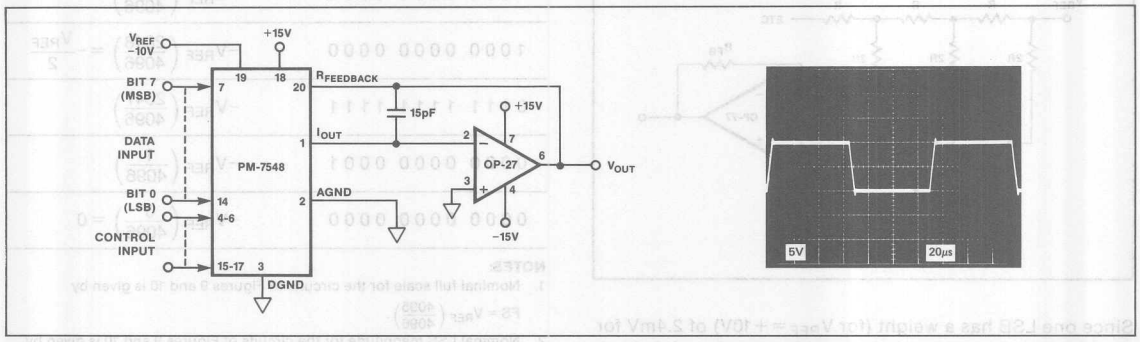
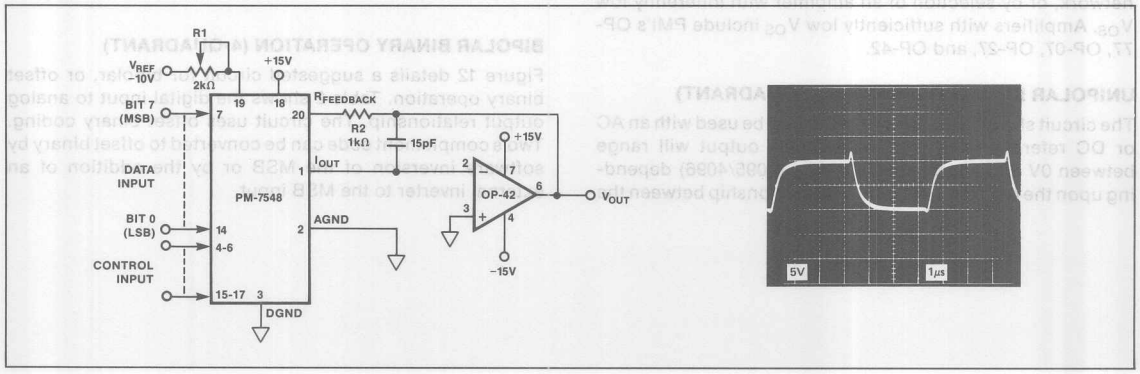


FIGURE 10: Unipolar Binary Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)



the circuit of Figure 11 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:

$R_O = 10k\Omega$ for more than 4-bits of logic 1

$R_O = 30k\Omega$ for any single bit logic 1

Therefore, the offset gain varies as follows:

At code 0011 1111 1111,

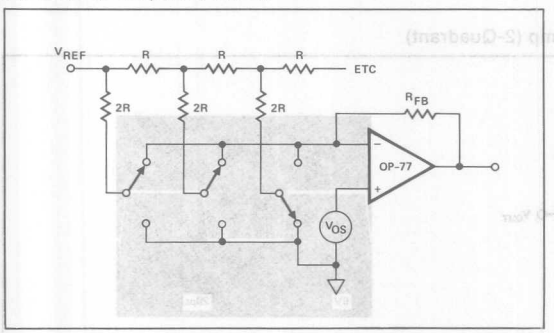
$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2V_{OS}$$

At code 0100 0000 0000,

$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3V_{OS}$$

The error difference is 2/3 V_{OS}.

FIGURE 11: Simplified Circuit



Since one LSB has a weight (for $V_{REF} = +10V$) of 2.4mV for the PM-7548, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuit shown in Figures 9 and 10 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the parameters for the V_{REF} range are the maximum input voltage range for the op amp or ±25V, whichever is lowest.

Gain error may be trimmed by adjusting R1 as shown in Figure 10. The DAC register must first be loaded with all 1s. This is most easily accomplished by asserting Data Override HIGH (DF/$\overline{DOR}$ LOW and CTRL HIGH). R1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In many applications the PM-7548's negligible zero scale error and very low gain error permit the elimination of the trimming components (R1 and the external $R_{FEEDBACK}$) without adverse effects on circuit performance.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB — LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 9 and 10)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111 1111 1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 9 and 10 is given by $FS = V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 9 and 10 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

Figure 12 details a suggested circuit for bipolar, or offset binary operation. Table 2 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

TABLE 2: Bipolar (Offset Binary) Code Table

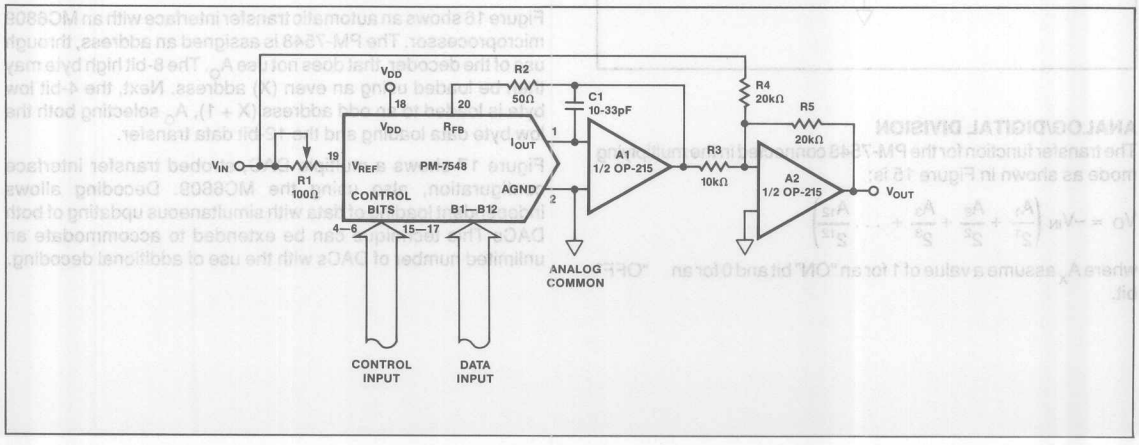
DIGITAL INPUT MSB		LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 12)
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0
1111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 7 is given by
   $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 7 is given by
   $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

Resistors R3, R4, and R5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R3 and R4 causes offset and full scale errors while an R5 to R4 and R3 mismatch will result in full scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R1 until $V_{OUT} = 0V$. R1 and R2 may be omitted, adjusting the ratio of R3 to R4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R5 until the desired V_{OUT} is achieved.

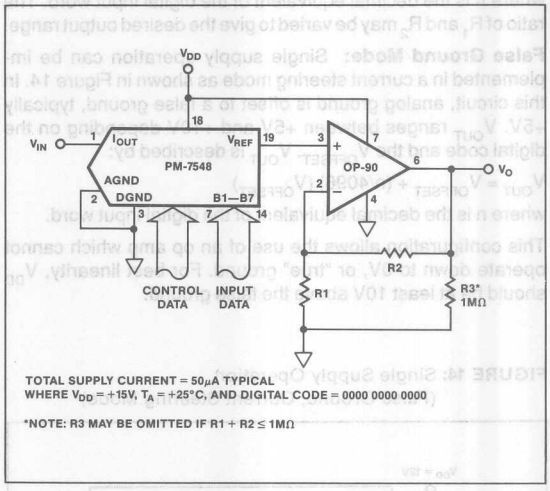
FIGURE 12: Bipolar Operation (4-Quadrant)



SINGLE SUPPLY OPERATION

Voltage Switching Mode: Figure 13 shows the PM-7548 in a single supply voltage switching mode. This circuit uses the micropower OP-90 to minimize supply current requirements. This op amp allows the circuit output to swing to ground provided that the op amp sees a resistance to ground of less than 1MΩ.

FIGURE 13: Ultra Low Power Single Supply Operation (Voltage Switching Mode)



As shown, a reference voltage is applied to I_{OUT} and the buffer op amp is tied, in a noninverting orientation, to the V_{REF} pin. The DAC's R-2R ladder acts as a voltage divider, its output voltage at the V_{REF} pin having an impedance of R (typically 11kΩ).

The applied reference voltage must always be positive with respect to AGND. This will avoid the forward biasing of an internal diode found between I_{OUT} and AGND. The reference voltage must also be maintained within +2.5V of AGND (with V_{DD} between +12V and +15V) to maintain linearity.

The output voltage of this circuit can be described as:

$$V_{OUT} = V_{REF}\ (n/4096)\left(\frac{R_1 + R_2}{R_1}\right)$$

where n is the decimal equivalent of the digital input word. The ratio of R_1 and R_2 may be varied to give the desired output range.

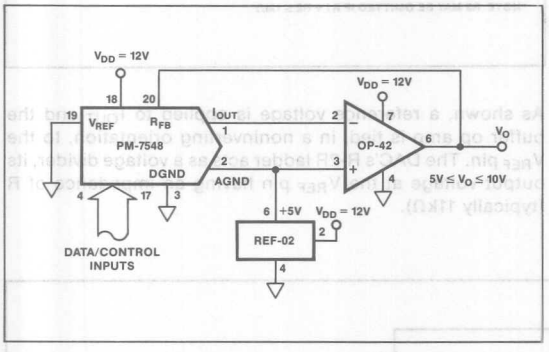
False Ground Mode: Single supply operation can be implemented in a current steering mode as shown in Figure 14. In this circuit, analog ground is offset to a false ground, typically +5V. V_{OUT} ranges between +5V and +10V depending on the digital code and the V_{OFFSET}. V_{OUT} is described by:

$$V_{OUT} = V_{OFFSET} + (n/4096)\ (V_{OFFSET})$$

where n is the decimal equivalent of the digital input word.

This configuration allows the use of an op amp which cannot operate down to 0V, or "true" ground. For best linearity, V_{DD} should be at least 10V above the false ground.

FIGURE 14: Single Supply Operation (False Ground, Current Steering Mode)



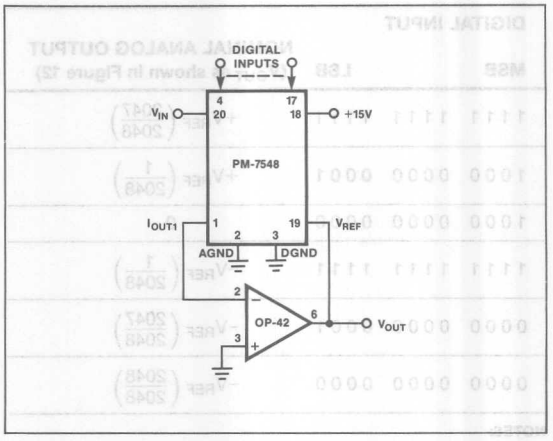
ANALOG/DIGITAL DIVISION

The transfer function for the PM-7548 connected in the multiplying mode as shown in Figure 15 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}\right)$$

where A_X assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

FIGURE 15: Analog/Digital Divider



The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 15. It is now:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} \ldots + \frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

MICROPROCESSOR INTERFACE

The PM-7548 can be directly interfaced to an 8-bit microprocessor's bus. Two such interfaces are shown in Figures 16 and 17.

Figure 16 shows an automatic transfer interface with an MC6809 microprocessor. The PM-7548 is assigned an address, through use of the decoder, that does not use A_0. The 8-bit high byte may then be loaded using an even (X) address. Next, the 4-bit low byte is loaded to an odd address (X + 1), A_0 selecting both the low byte data loading and the 12-bit data transfer.

Figure 17 shows a multiple DAC, strobed transfer interface configuration, also using the MC6809. Decoding allows independent loading of data with simultaneous updating of both DACs This technique can be extended to accommodate an unlimited number of DACs with the use of additional decoding.

FIGURE 16: PM-7548/MC6809 Interface Automatic Transfer Mode

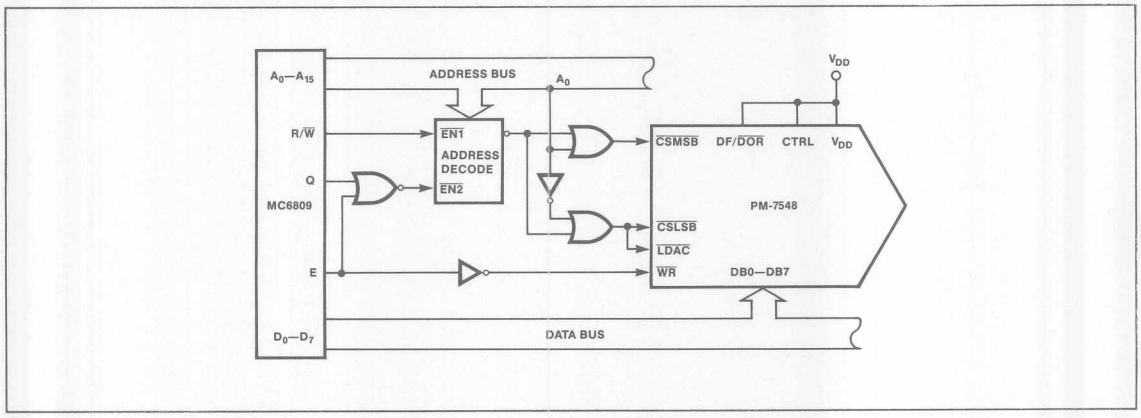
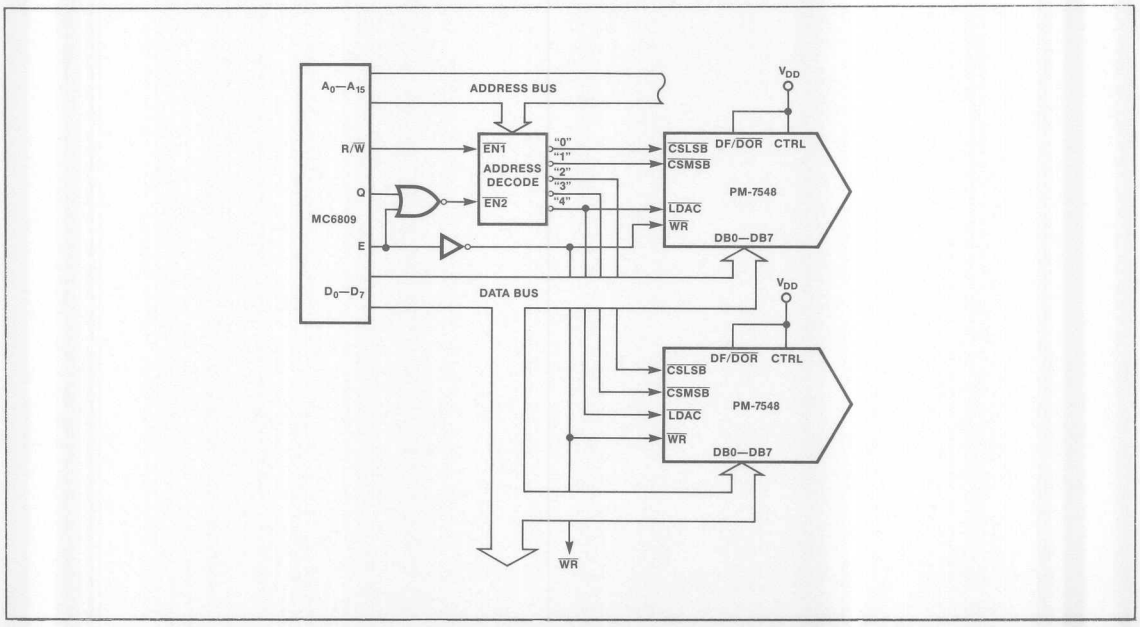


FIGURE 17: PM-7548/MC6809 Interface Multiple DAC, Strobed Transfer Mode



ANALOG DEVICES

LC²MOS
Dual 12-Bit µP-Compatible DAC
AD7549

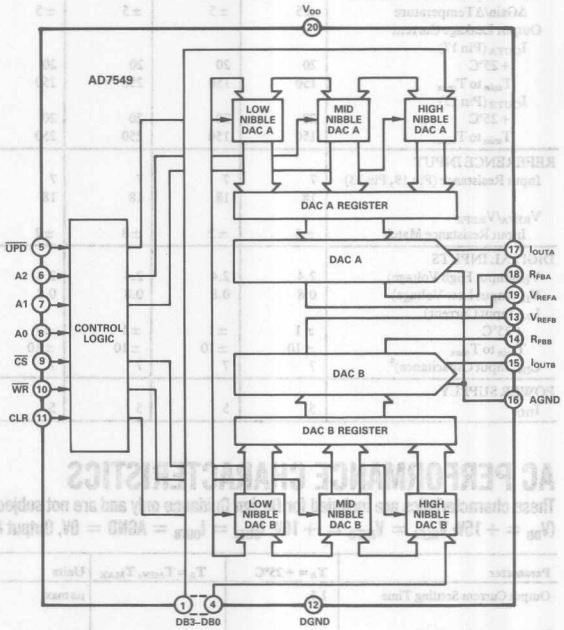
FEATURES

- Two Doubled Buffered 12-Bit DACs
- 4-Quadrant Multiplication
- Low Gain Error (3LSBs max)
- DAC Ladder Resistance Matching: 1%
- Space Saving Skinny DIP and Surface Mount Packages
- Latch-Up Proof
- Extended Temperature Range Operation

APPLICATIONS

- Programmable Filters
- Automatic Test Equipment
- Microcomputer Based Process Control
- Audio Systems
- Programmable Power Supplies
- Synchro Applications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7549 is a monolithic dual, 12-bit, current output D/A converter. It is packaged in both 0.3″ wide 20-pin DIPs and in 20-terminal surface mount packages. Both DACs provide four quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The monolithic construction ensures excellent thermal tracking and gain error tracking between the two DACs.

The DACs in the AD7549 are each loaded in three 4-bit nibbles. The control logic is designed for easy processor interfacing. Input and DAC register loading is accomplished using address lines A0, A1, A2 and $\overline{CS}$, $\overline{WR}$ lines. A logic high level on the CLR input clears all registers. Both DACs may be simultaneously updated using the $\overline{UPD}$ input.

The AD7549 is manufactured using the Linear Compatible CMOS(LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC or 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Small package size: the loading structure adopted for the AD7549 enables two 12-Bit DACs to be packaged in either a small 20-pin 0.3″ DIP or in 20-terminal surface mount packages.
2. DAC to DAC matching: since both DACs are fabricated on the same chip, precise matching and tracking is inherent. This opens up applications which otherwise would not be considered, i.e., Programmable Filters, Audio Systems, etc.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Full Scale Error	Package Option[2]
AD7549JN	−40°C to +85°C	±1LSB	±6LSB	N-20
AD7549KN	−40°C to +85°C	±1/2LSB	±3LSB	N-20
AD7549JP	−40°C to +85°C	±1LSB	±6LSB	P-20A
AD7549KP	−40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7549AQ	−40°C to +85°C	±1LSB	±6LSB	Q-20
AD7549BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-20
AD7549SQ	−55°C to +125°C	±1LSB	±6LSB	Q-20
AD7549TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-20
AD7549SE	−55°C to +125°C	±1LSB	±6LSB	E-20A
AD7549TE	−55°C to +125°C	±1/2LSB	±3LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

AD7549—SPECIFICATIONS[1]

(V_{DD} = +15V ±5%[2], V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC.
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current						
I_{OUTA} (Pin 17)						
+25°C	20	20	20	20	nA max	DAC A Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
I_{OUTB} (Pin 15)						
+25°C	20	20	20	20	nA max	DAC B Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
REFERENCE INPUT						
Input Resistance (Pin 19, Pin 13)	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	18	18	18	18	kΩ max	
V_{REFA}/V_{REFB} Input Resistance Match	±3	±2	±3	±2	% max	Typically ±1%
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
I_{DD}	5	5	5	5	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V, Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	10	–	nV-sec typ	Measured with V_{REFA} = V_{RFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20V p-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUTA}	80	80	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	80	80	pF max	
C_{OUTA}	160	160	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	160	160	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−62	–	dB typ	V_{REFA} = 20V p-p 100kHz sine wave, V_{REFB} = 0V
V_{REFB} to I_{OUTA}	−62	–	dB typ	V_{REFB} = 20V p-p 100kHz sine wave, V_{REFA} = 0V
Digital Crosstalk	10	–	nV-sec typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}
Harmonic Distortion	−90	–	dB typ	V_{IN} = 6V rms 1kHz

NOTES

[1]Temperature range as follows: J, K, Versions: −40°C to +85°C
A, B, Versions: −40°C to +85°C
S, T, Versions: −55°C to +125°C

[2]At V_{DD} = 5V, the device is fully functional with degraded performance.

[3]Guaranteed by Product Assurance testing.

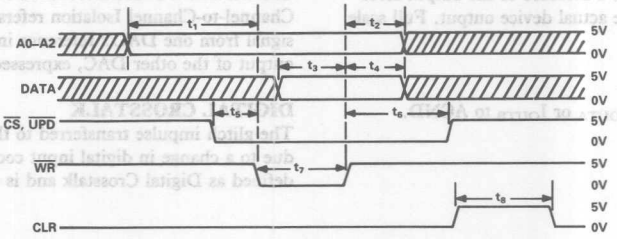
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +15V, V_{REFA} = V_{RFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	50	80	110	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	180	200	240	ns min	Data Setup Time
t_4	0	0	0	ns min	Data Hold Time
t_5	20	20	20	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	170	200	250	ns min	Write Pulse Width
t_8	170	200	250	ns min	Clear Pulse Width

Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (Pin 20) to DGND	−0.3V, +17V
V_{REFA}, V_{REFB} (Pins 19, 13) to AGND	±25V
V_{RFBA}, V_{RFBB} (Pins 18, 14) to AGND	±25V
Digital Input Voltage (Pins 1–11) to DGND	−0.3V, V_{DD} +0.3V
V_{PIN15}, V_{PIN17}, to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial (J, K Versions)	−40°C to +85°C
Industrial (A, B Versions)	−40°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB max over the operating temperature range ensures montonicity.

FULL-SCALE ERROR
Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUTA} or I_{OUTB} to AGND.

This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REFA} and V_{REFB} equal to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUTA} or I_{OUTB} with the DAC registers loaded to all zeros.

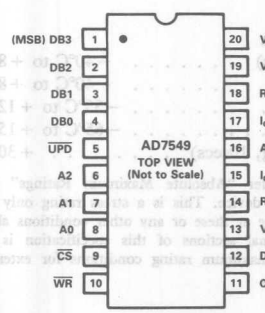
MULTIPLYING FEEDTHROUGH ERROR
This is the error due to capacitive feedthrough from V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB} with the DAC registers loaded to all zeros.

CHANNEL-TO-CHANNEL ISOLATION
Channel-to-Channel Isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

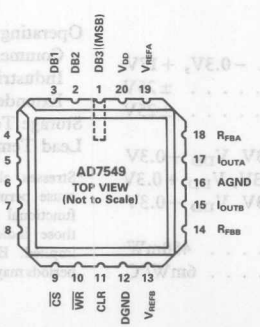
DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as Digital Crosstalk and is specified in nV-secs.

PIN CONFIGURATIONS

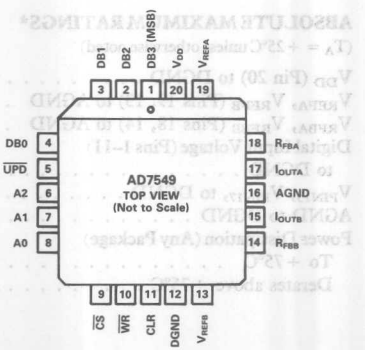
DIP



LCCC



PLCC



PIN	FUNCTION	DESCRIPTION
1	DB3	Data Bit 3, Data Bit 7 or Data Bit 11 (MSB)
2	DB2	Data Bit 2, Data Bit 6 or Data Bit 10.
3	DB1	Data Bit 1, Data Bit 5 or Data Bit 9.
4	DB0	Data Bit 0, Data Bit 4 or Data Bit 8.
5	$\overline{UPD}$	Updates DAC Registers from 4-bit input registers. DAC A and DAC B both updated simultaneously.
6	A2	Address line 2.
7	A1	Address line 1.
8	A0	Address line 0.
9	$\overline{CS}$	Chip Select Input. Active low.
10	$\overline{WR}$	Write Input. Active low.
11	CLR	Clear Input. Active High. Clears all registers.
12	DGND	Digital Ground.
13	V_{REFB}	Voltage reference input to DAC B.
14	R_{FBB}	Feedback resistor of DAC B.
15	I_{OUTB}	Current output terminal of DAC B.
16	AGND	Analog ground.
17	I_{OUTA}	Current output terminal of DAC A.
18	R_{FBA}	Feedback resistor of DAC A.
19	V_{REFA}	Voltage reference input to DAC A.
20	V_{DD}	+15V supply input.

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	⊓	0	0	0	DAC A LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	0	1	DAC A MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	0	DAC A HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	1	DAC A Register loaded from Input Registers.
0	1	0	⊓	1	0	0	DAC B LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	0	1	DAC B MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	0	DAC B HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	1	DAC B Register loaded from Input Registers.
0	0	1	⊓	X	X	X	DAC A, DAC B Registers updated simultaneously from Input Registers.

NOTE: X = Don't Care

Table I. AD7549 Truth Table

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (i.e. AD644) or separate packages (AD544). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all O's and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is at a minimum (i.e. ≤120μV). Full scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

Resistors R5, R6, R7 (R8, R9, R10) must be ratio matched to 0.01%. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table III.

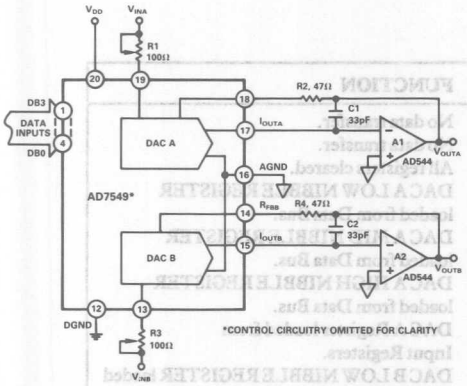


Figure 2. AD7549 Unipolar Binary Operation

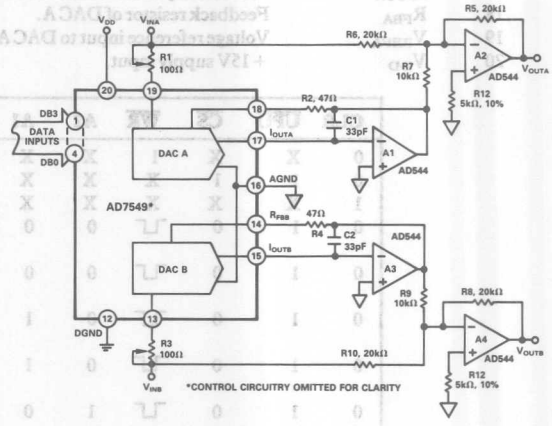


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 3

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 2 and 3 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD644L, AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Temperature Coefficients: The gain temperature coefficient of the AD7549 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full scale range, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account.

High Frequency Considerations: AD7549 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7549 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 2 is shown in Figure 4 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

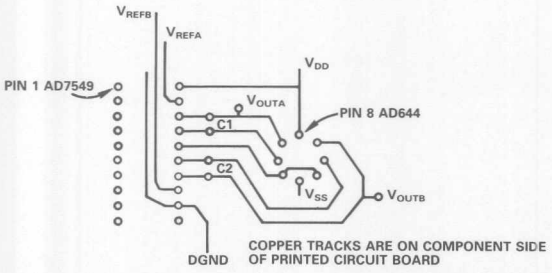


Figure 4. Suggested Layout for AD7549 with AD644 (Dual Op Amp)

AD7549 – 8085A INTERFACE

A typical interface circuit for the AD7549 and the 8085A microprocessor is given in Figure 5. Only the bottom 4 bits of the microprocessor data bus are used. The address decoder provides both the $\overline{CS}$ and $\overline{UPD}$ signals for the DAC. Address lines A0, A1, A2 select one of six DAC Input Registers for accepting data. In applications where simultaneous loading of the DACs is required then the $\overline{UPD}$ pin must be used to strobe both DAC registers. Otherwise, $\overline{UPD}$ may be tied high and address lines A0-A2, in conjunction with $\overline{CS}$ and $\overline{WR}$ signals, will select each DAC register separately (see Pin Function Description).

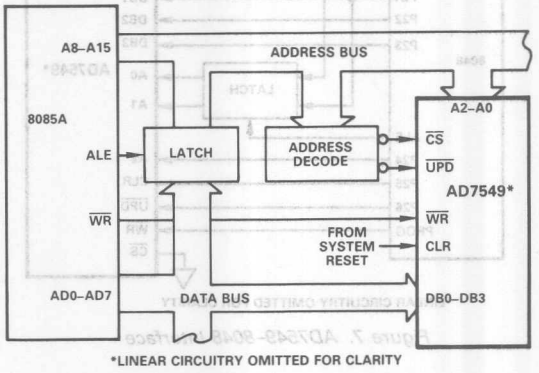


Figure 5. AD7549–8085A Interface

AD7549 – Z80 INTERFACE

Figure 6 shows the AD7549 connected to the Z80 microprocessor. The interface structure is similar to that for the 8085A.

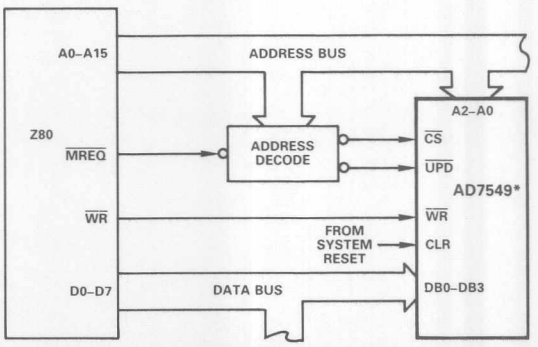


Figure 6. AD7549–Z80 Interface

AD7549 – 8048 INTERFACE

The AD7549 can be interfaced to the 8048 single component microcomputer using the circuit of Figure 7. A minimum number of I/O lines are needed. The system is easily expanded by using extra port lines to provide Chip Selects for more AD7549's. The advantage of this interface lies in its simplicity. In either single or multiple DAC applications both the software and chip select decoding are simplified over what would be required if the devices were memory mapped in a conventional manner.

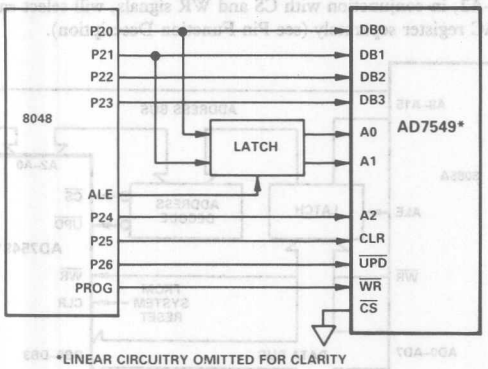


Figure 7. AD7549–8048 Interface

The combination of 8048 system and AD7549 is particularly suitable for dedicated control applications. By adding reference and output circuitry a complete control system can be configured with a minimum number of components.

AD7549 – MC6809 INTERFACE

Figure 8 is the interface circuit for the popular MC6809 8-bit microprocessor. $\overline{CS}$ and $\overline{UPD}$ signals are decoded from the address for the simultaneous update facility while the $\overline{WR}$ pulse is provided by inverting the microprocessor clock, E.

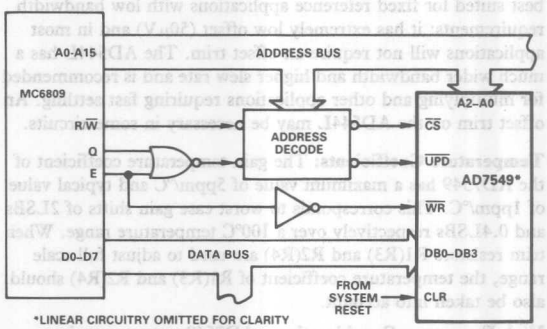


Figure 8. AD7549–MC6809 Interface

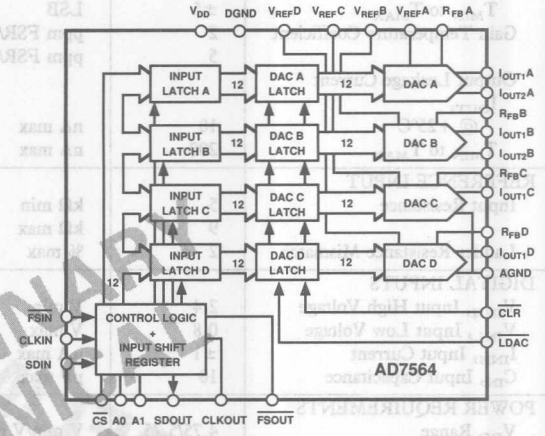
LC²MOS Quad 12-Bit DAC

AD7564

FEATURES
- Four 12-Bit DACs in One Package
- 4-Quadrant Multiplication
- Separate References
- Single +5 V Supply
- Low Power
- Versatile Serial Interface
- Simultaneous Update Capability
- Reset Function
- 28-Pin SOIC

APPLICATIONS
- Process Control
- Portable Instrumentation
- General Purpose Test Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7564 contains four 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT} and R_{FB} terminals. The I_{OUT2} terminals of DAC A and DAC B are pinned out separately, whereas I_{OUT2} of DAC C and DAC D are tied together at AGND.

The AD7564 is a serial input device. When it is selected by bringing $\overline{CS}$ low, data is loaded using $\overline{FSIN}$, CLKIN and SDIN. Two address pins, A0 and A1, set up a device address and this feature may be used to simplify device loading in a multi-DAC environment. Alternatively, A0 and A1 can be ignored and the serial out capability used to configure a daisy chained system.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

The device is packaged in a 28-pin SOIC package.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	AD7564B	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSB	
T_{MIN} to T_{MAX}	±5	LSB	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Rejection			
$\Delta Gain/\Delta V_{DD}$	−75	dB min	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for design guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7564B	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital-to-Analog Glitch Impulse	40	nV-s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	−66	dB max	V_{REF} = 20 V pk–pk, 10 kHz Sine Wave. DAC Latch Loaded with all 0s.
Channel-to-Channel Isolation	−76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk–pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV-s typ	Effect of all 0s to All 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV-s typ	Feedthrough to Any DAC Output with $\overline{CS}$ High for All 0s to All 1s Code Transition on the Data Bus.
Total Harmonic Distortion	−83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			All 1s loaded to the DAC. V_{REF} = 0 V,
@ 1 kHz	20	nV/$\sqrt{Hz}$	Output Op Amp is AD OP-07.

NOTES
[1]Temperature range as follows: B Version −40°C to +85°C.
Specifications subject to change without notice.

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TIMING SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; I_{OUT1} = I_{OUT2} = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN Low Time
t_3	40	40	ns min	CLKIN High Time
t_4	30	30	ns min	$\overline{FSIN}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	50	50	ns max	Delay between CLKIN Rising Edge and CLKOUT Rising Edge
t_9[2]	40	40	ns min	$\overline{FSOUT}$ Valid After CLKOUT Rising Edge
t_{10}[2]	70	70	ns max	SDOUT Valid After CLKOUT Rising Edge
t_{11}[2]	10	10	ns max	$\overline{FSOUT}$ High After CLKOUT Rising Edge
t_{12}	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width
t_{13}	0	0	ns min	$\overline{CS}$ to $\overline{FSIN}$ Setup Time
t_{14}	0	0	ns min	$\overline{CS}$ to $\overline{FSIN}$ Hold Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_8, t_9, t_{10}, t_{11} are measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V.

PRELIMINARY TECHNICAL DATA

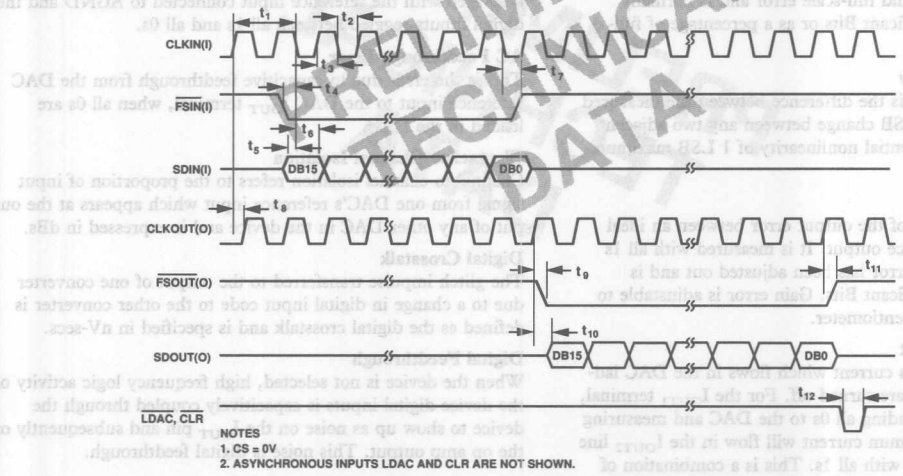


Figure 1. Mode 1 Timing Diagram

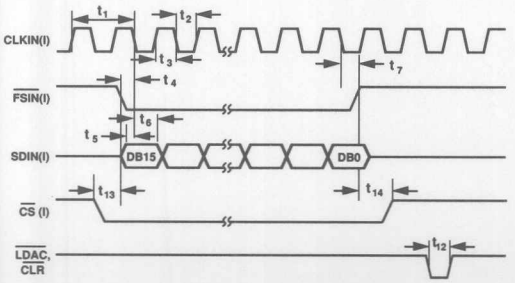


Figure 2. Mode 2 Timing Diagram

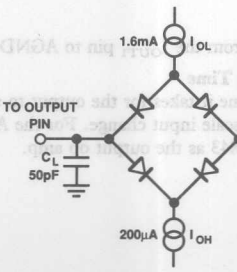


Figure 3. Output Load Circuit

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ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3 V to +6 V
I_{OUT1} to DGND	−0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND	±15 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial Plastic (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	250 mW
Derates Above +75°C by	10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

Relative Accuracy

Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error

Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current

Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance

This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7568, it is specified with the AD843 as the output op amp.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measure as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error

This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation

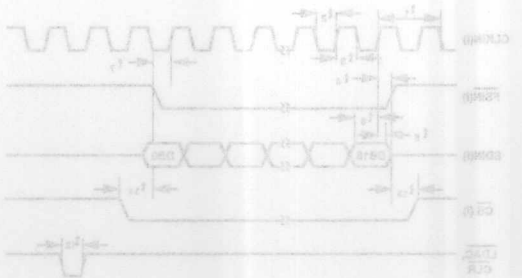
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the digital crosstalk and is specified in nV-secs.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.



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PIN DESCRIPTION

Pin	Description
V_{DD}	Positive Power Supply. This is +5 V ± 5%.
DGND	Digital Ground.
$V_{REF}A$–$V_{REF}D$	DAC Reference Inputs.
$R_{FB}A$–$R_{FB}D$	DAC Feedback Resistor Pins.
$I_{OUT1}A$–$I_{OUT1}D$	DAC I_{OUT1} Terminals.
$I_{OUT2}A$–$I_{OUT2}B$	DAC I_{OUT2} Terminals for DAC A and DAC B. These should normally connected to the signal ground of the system.
AGND	This is the common point to which the I_{OUT2} terminals for DAC C and DAC D are connected. It should be connected to the signal ground of the system.
CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN.
$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register, and data is transferred on the falling edges of CLKIN. If the address bits are valid, the 12-bit DAC data is transferred to the appropriate input latch on the sixteenth falling edge after $\overline{FSIN}$ goes low.
SDIN	Serial Data Input. The device accepts a 16-bit word. The first two bits are device address bits and these are followed by two DAC select bits. The remaining 12 bits are data.
CLKOUT	Clock Output; this is used to latch the serial data output.
$\overline{FSOUT}$	This is the frame synchronization output signal for the serial data output.
SDOUT	This shift register output allows multiple devices to be connected in a daisy chain configuration.
$\overline{CS}$	Active Low Chip Select Input.
A0, A1	Device Address Pins. These inputs give the device an address. If the first two bits of the serial input stream do not correspond to this address, the data which follows is ignored and not loaded to any input latch. However, it will appear at SDOUT irrespective of this.
$\overline{LDAC}$	Asynchronous $\overline{LDAC}$ Input. When this input is taken low, all DAC latches are simultaneously updated with the contents of the input latches.
$\overline{CLR}$	Asynchronous $\overline{CLR}$ Input. When this input is taken low, all DAC latches are loaded with all 0s.

Table I. AD7564 Loading Sequence

DB15															DB0
A1	A0	DS1	DS0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table II. DAC Selection

DS1	DS0	Function
0	0	DAC A Selected
0	1	DAC B Selected
1	0	DAC C Selected
1	1	DAC D Selected

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

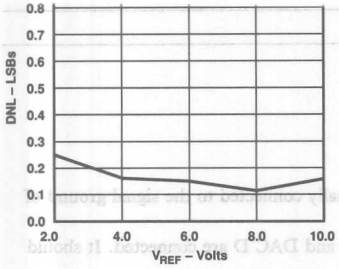


Figure 4. Differential Nonlinearity Error vs. V_{REF}

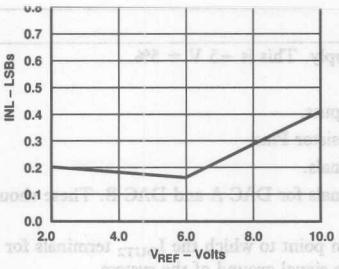


Figure 5. Integral Nonlinearity Error vs. V_{REF}

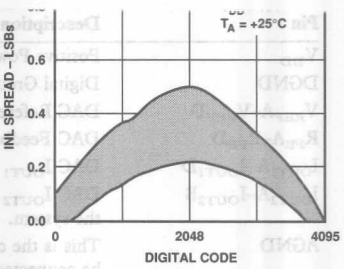


Figure 6. Typical DAC-to-DAC Linearity Matching

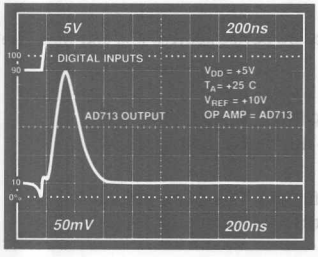


Figure 7. Digital-to-Analog Glitch Impulse

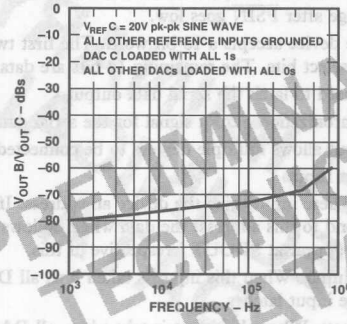


Figure 8. Channel-to-Channel Isolation (1 DAC to 1 DAC)

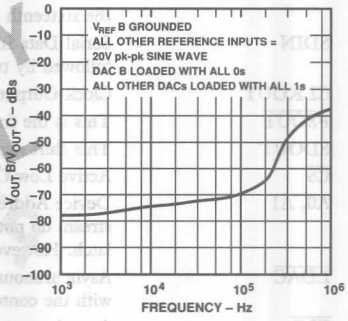


Figure 9. Channel-to-Channel Isolation (1 DAC to All Other DACs)

PRELIMINARY TECHNICAL DATA

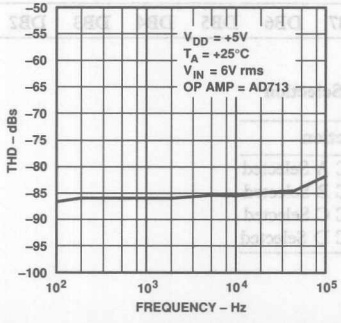


Figure 10. Total Harmonic Distortion vs. Frequency

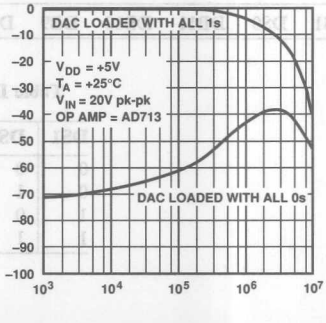


Figure 11. Multiplying Frequency Response vs. Digital Code

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

D/A SECTION

The AD7564 contains four 12-bit current output D/A converters. A simplified circuit diagram for one of the D/A converters is shown in Figure 12.

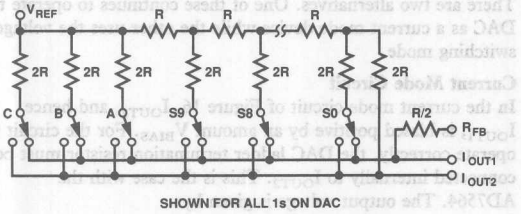


Figure 12. Simplified D/A Circuit Diagram

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A, B and C. The remaining 10 bits of the data word drive the switches S0 to S9 in a standard R-2R ladder configuration.

Each of the switches A to C steers 1/4 of the total reference current with the remaining current passing through the R-2R section.

DAC A and DAC B have separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} pins. DAC C and DAC D have their I_{OUT2} pins connected to the device AGND pin.

When an output amplifier is connected in the standard configuration of Figure 14, the output voltage is given by:

$$V_{OUT} = -D \cdot V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC. Thus, in the AD7568, D can be set from 0 to 4095/4096.

INTERFACE SECTION

The AD7564 is a serial input device. Three input signals control the serial interface. These are $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

When the $\overline{FSIN}$ input goes low, data appearing on the SDIN line is clocked into the input shift register on each falling edge of CLKIN. When sixteen bits have been received, the register loading is automatically disabled until the next falling edge of $\overline{FSIN}$ is detected. Also, there are three output signals which allow several AD7564s to be easily connected together. These are FSOUT, CLKOUT and SDOUT. The operation of these is shown in the timing diagram of Figure 1.

When the sixteen bits have been received in the input shift register, DB15 and DB14 (A1 and A0) are checked to see if they correspond to the state of pin A1 and A0. If they do, then the word is accepted. Otherwise, it is disregarded. This allows the user to address one of four AD7564s in a very simple fashion. DB13 and DB12 of the 16-bit word determine which of the four DAC input latches is to be loaded. When the $\overline{LDAC}$ line goes low, all four DAC latches in the device are simultaneously loaded with the contents of their respective input latches and the outputs change accordingly.

Bringing the $\overline{CLR}$ line low resets the DAC latches to all 0s. The input latches are not affected, so that the user can revert to the previous analog output, if desired.

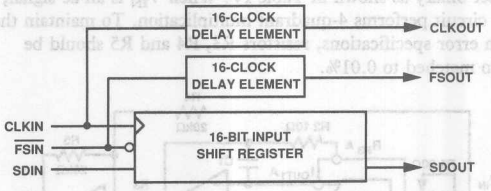


Figure 13. Input Logic

UNIPOLAR BINARY OPERATION

(2-Quadrant Multiplication)

Figure 14 shows the standard unipolar binary connection diagram for one of the DACs in the AD7568. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. Resistors R1 and R2 allow the user to adjust the DAC gain error. Offset can be removed by adjusting the output amplifier offset voltage.

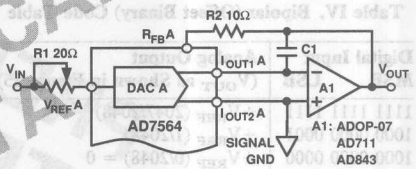


Figure 14. Unipolar Binary Operation

A1 should be chosen to suit the application. For example, the ADOP-07 is ideal for very low bandwidth applications while the AD843 and AD845 offer very fast settling time in wide bandwidth applications. Appropriate multiple versions of these amplifiers can be used with the AD7564 to reduce board space requirements.

The code table for Figure 14 is shown in Table III.

Table III. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output (V_{OUT} as Shown in Figure 14)
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0001	$-V_{REF}$ (2049/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0111 1111 1111	$-V_{REF}$ (2047/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	$-V_{REF}$ (0/4096) = 0

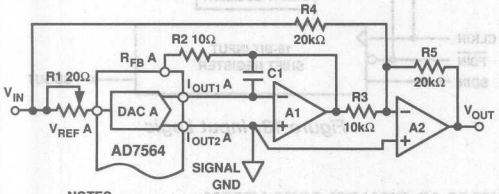
NOTE
Nominal LSB size for the circuit of Figure 14 is given by: V_{REF} (1/4096).

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 15 shows the standard connection diagram for bipolar operation of any one of the DACs in the AD7564. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R3, R4 and R5 should be ratio matched to 0.01%.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER, A1.

Figure 15. Bipolar Operation (4-Quadrant Multiplication)

Table IV. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output (V_{OUT} as Shown in Figure 15)
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	$+V_{REF}$ (0/2048) = 0
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0001	$-V_{REF}$ (2047/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

NOTE
Nominal LSB size for the circuit of Figure 15 is given by: V_{REF} (1/2048)

SINGLE SUPPLY CIRCUITS

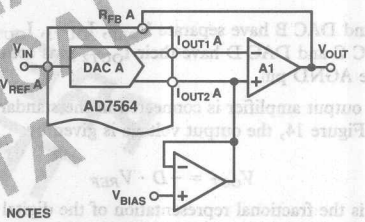
The AD7564 operates from a single +5 V supply and this makes it ideal for single supply systems. When operating in such a system, it is not possible to use the standard circuits of Figures 14 and 15 since these invert the analog input, V_{IN}. There are two alternatives. One of these continues to operate the DAC as a current mode device while the other uses the voltage switching mode.

Current Mode Circuit

In the current mode circuit of Figure 16, I_{OUT2}, and hence I_{OUT1}, is biased positive by an amount V_{BIAS}. For the circuit to operate correctly, the DAC ladder termination resistor must be connected internally to I_{OUT2}. This is the case with the AD7564. The output voltage is given by:

$$V_{OUT} = \left(D \cdot \frac{R_{FB}}{R_{DAC}} \cdot (V_{BIAS} - V_{IN})\right) + V_{BIAS}$$

As D varies from 0 to 4095/4096, the output voltage varies from $V_{OUT} = V_{BIAS}$ to $V_{OUT} = 2\ V_{BIAS} - V_{IN}$. V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the I_{OUT2} terminal without any problems.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER, A1.

Figure 16. Single Supply Current-Mode Operation

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

LC²MOS Octal 12-Bit DAC

AD7568

2

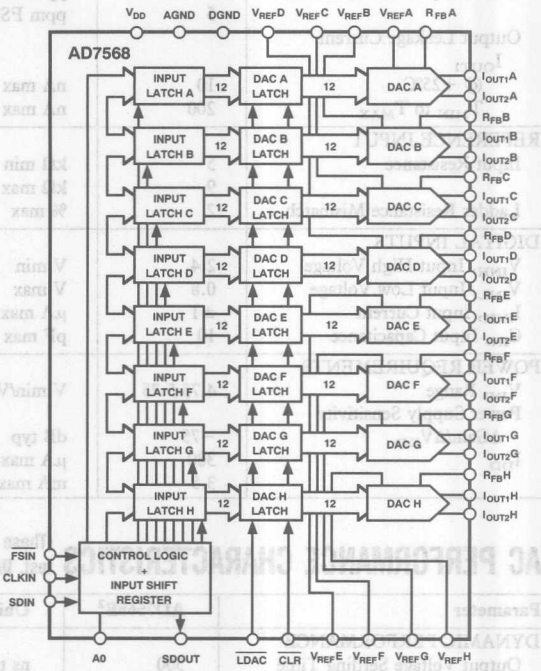
FEATURES

- 8 12-Bit DACs in One Package
- 4-Quadrant Multiplication
- Separate References
- Single +5 V Supply
- Low Power: 1 mW
- Versatile Serial Interface
- Simultaneous Update Capability
- Reset Function
- 44-Pin PQFP

APPLICATIONS

- Process Control
- Automatic Test Equipment
- General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7568 contains eight 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals.

The AD7568 is a serial input device. Data is loaded using FSIN, CLKIN and SDIN. One address pin, A0, sets up a device address, and this feature may be used to simplify device loading in a multi-DAC environment.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

The AD7568 is housed in a space-saving 44-pin Plastic Quad Flat Pack.

Parameter	AD7568B	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity			
$\Delta Gain/\Delta V_{DD}$	−75	dB typ	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

AC PERFORMANCE CHARACTERISTICS

(These characteristics are included for Design Guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital to Analog Glitch Impulse	40	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	−66	dB max	V_{REF} = 20 V pk–pk, 10 kHz Sine Wave. DAC Latch Loaded with All 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC.
	30	pF max	All 0s Loaded to DAC.
Channel-to-Channel Isolation	−76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk–pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV–s typ	Effect of all 0s to all 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV–s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK.
Total Harmonic Distortion	−83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			
@ 1 kHz	20	nV/$\sqrt{Hz}$	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp is AD OP-07.

NOTES
[1]Temperature range as follows: B Version: −40°C to +85°C.
[2]All specifications also apply for V_{REF} = +10 V, except relative accuracy which degrades to ±1 LSB.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V ± 5%; I_{OUT1} = I_{OUT2} = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN High Time
t_3	40	40	ns min	CLKIN Low Time
t_4	30	30	ns min	$\overline{FSIN}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	70	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

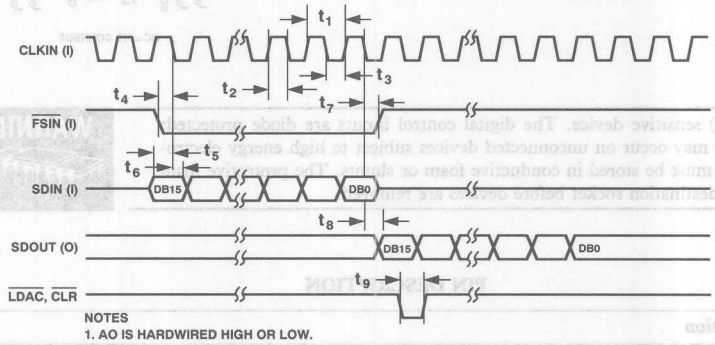


Figure 1. Timing Diagram

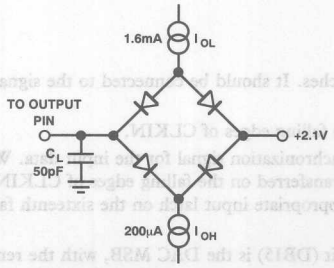


Figure 2. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Package Option*
AD7568BS	−40°C to +85°C	±0.5	S-44

*S = Plastic Quad Flat Pack (PQFP). For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

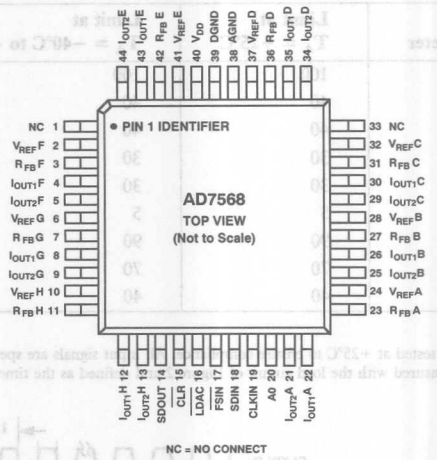
V_{DD} to DGND . . . . . −0.3 V to +6 V
I_{OUT1} to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND . . . . . ±15 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (B Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 250 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PIN CONFIGURATIONS



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN DESCRIPTION

Pin	Description
V_{DD}	Positive power supply. This is +5 V ± 5%.
DGND	Digital Ground.
AGND	Analog Ground.
$V_{REF}A$ – $V_{REF}H$	DAC reference inputs.
$R_{FB}A$ – $R_{FB}H$	DAC feedback resistor pins.
$I_{OUT}A$ – $I_{OUT}H$	DAC current output terminals.
AGND	This pin connects to the back gates of the current steering switches. It should be connected to the signal ground of the system.
CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN.
$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register, and data is transferred on the falling edges of CLKIN. If the address bit is valid, the 12-bit DAC data is transferred to the appropriate input latch on the sixteenth falling edge after $\overline{FSIN}$ goes low.
SDIN	Serial data input. The device accepts a 16-bit word. The first bit (DB15) is the DAC MSB, with the remaining bits following. Next comes the device address bit, A0. If this does not correspond to the logic level on pin A0, the data is ignored. Finally come the three DAC select bits. These determine which DAC in the device is selected for loading.
SDOUT	This shift register output allows multiple devices to be connected in a daisy chain configuration.
A0	Device address pin. This input gives the device an address. If DB3 of the serial input stream does not correspond to this, the data which follows is ignored and not loaded to any input latch. However it will appear at SDOUT irrespective of this.
$\overline{LDAC}$	Asynchronous $\overline{LDAC}$ input. When this input is taken low, all DAC latches are simultaneously updated with the contents of the input latches.
$\overline{CLR}$	Asynchronous $\overline{CLR}$ input. When this input is taken low, all DAC latch outputs go to zero.

TERMINOLOGY

Relative Accuracy
Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage or full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7568, it is specified with the AD843 as the output op amp.

Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.

Table I. AD7568 Loading Sequence

DB15											DB0				
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A0	DS2	DS1	DS0

Table II. DAC Selection

DS2	DS1	DS0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Selected
1	0	1	DAC F Selected
1	1	0	DAC G Selected
1	1	1	DAC H Selected

AD7568—Typical Performance Curves

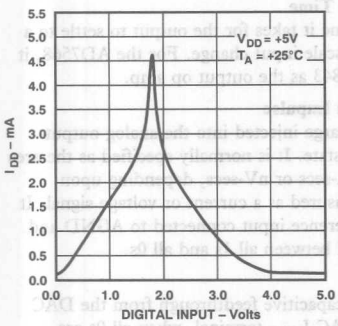


Figure 3. Supply Current vs. Logic Input Voltage

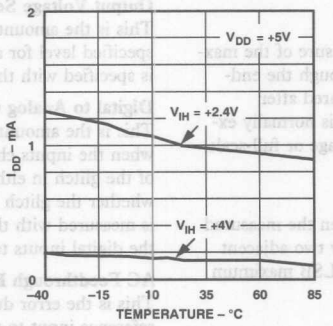


Figure 4. Supply Current vs. Temperature

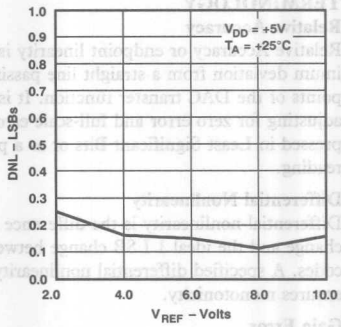


Figure 5. Differential Nonlinearity Error vs. V_{REF}

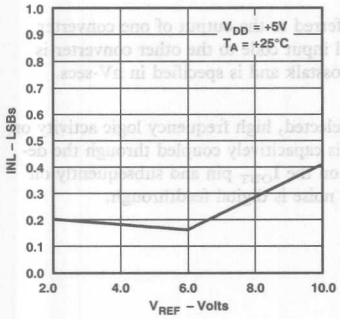


Figure 6. Integral Nonlinearity Error vs. V_{REF}

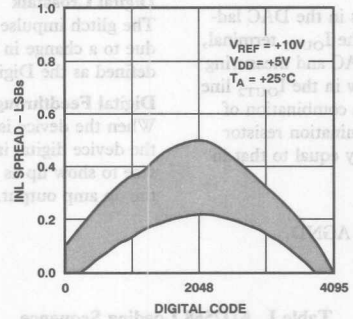


Figure 7. Typical DAC to DAC Linearity Matching

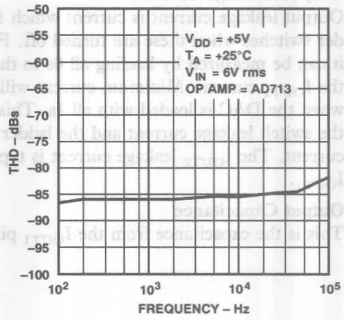


Figure 8. Total Harmonic Distortion vs. Frequency

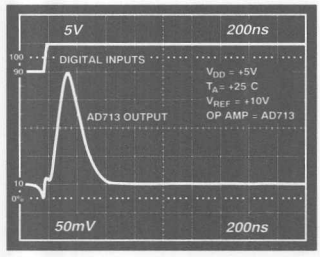


Figure 9. Digital-to-Analog Glitch Impulse

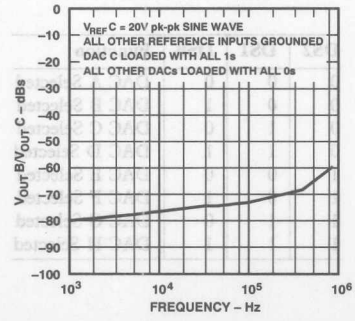


Figure 10. Channel-to-Channel Isolation (1 DAC to 1 DAC)

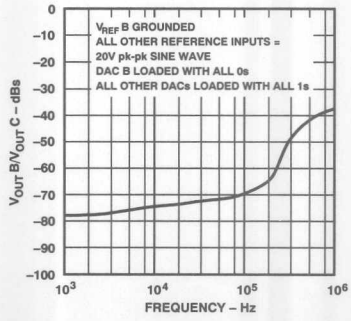


Figure 11. Channel-to-Channel Isolation (1 DAC to All Other DACs)

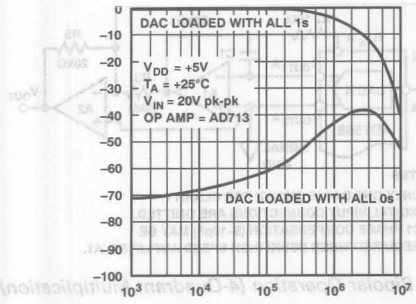


Figure 12. Multiplying Frequency Response vs. Digital Code

GENERAL DESCRIPTION

D/A Section

The AD7568 contains eight 12-bit current-output D/A converters. A simplified circuit diagram for one of the D/A converters is shown in Figure 13.

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A, B and C. The remaining 10 bits of the data word drive the switches S0 to S9 in a standard R–2R ladder configuration.

Each of the switches A to C steers 1/4 of the total reference current with the remaining current passing through the R–2R section.

Each DAC in the device has separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} pins. This makes the device extremely versatile and allows DACs in the same device to be configured differently.

When an output amplifier is connected in the standard configuration of Figure 15, the output voltage is given by:

$$V_{OUT} = -D \cdot V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC. Thus, in the AD7568, D can be set from 0 to 4095/4096.

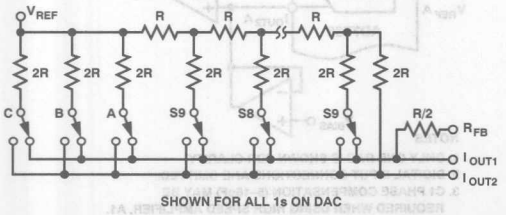


Figure 13. Simplified D/A Circuit Diagram

The AD7568 is a serial input device. Three lines control the serial interface, $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

When the $\overline{FSIN}$ input goes low, data appearing on the SDIN line is clocked into the input shift register on each falling edge of CLKIN. When sixteen bits have been received, the register loading is automatically disabled until the next falling edge of $\overline{FSIN}$ detected. Also, the received data is clocked out on the next rising edge of CLKIN and appears on the SDOUT pin. This feature allows several devices to be connected together in a daisy chain fashion.

When the sixteen bits have been received in the input shift register, DB3 (A0) is checked to see if it corresponds to the state of pin A0. If it does, then the word is accepted. Otherwise, it is disregarded. This allows the user to address one of two AD7568s in a very simple fashion. DB0 to DB2 of the 16-bit word determine which of the eight DAC input latches is to be loaded. When the $\overline{LDAC}$ line goes low, all eight DAC latches in the device are simultaneously loaded with the contents of their respective input latches, and the outputs change accordingly.

Bringing the $\overline{CLR}$ line low resets the DAC latches to all 0s. The input latches are not affected, so that the user can revert to the previous analog output if desired.

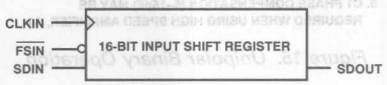


Figure 14. Input Logic

(2-Quadrant Multiplication)

Figure 15 shows the standard unipolar binary connection diagram for one of the DACs in the AD7568. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. Resistors R1 and R2 allow the user to adjust the DAC gain error. Offset can be removed by adjusting the output amplifier offset voltage.

A1 should be chosen to suit the application. For example, the ADOP-07 or OP-177 are ideal for very low bandwidth applications while the AD843 and AD845 offer very fast settling time in wide bandwidth applications. Appropriate multiple versions of these amplifiers can be used with the AD7568 to reduce board space requirements.

The code table for Figure 15 is shown in Table III.

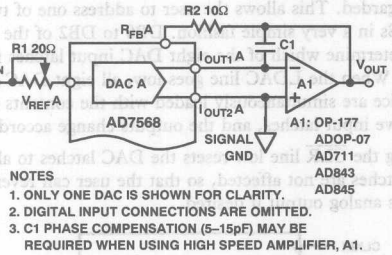


Figure 15. Unipolar Binary Operation

Table III. Unipolar Binary Code Table

Digital Input MSB . . . . . LSB	Analog Output (V_{OUT} As Shown in Figure 15)
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0001	$-V_{REF}$ (2049/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0111 1111 1111	$-V_{REF}$ (2047/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	$-V_{REF}$ (0/4096) = 0

NOTE
Nominal LSB size for the circuit of Figure 15 is given by: V_{REF} (1/4096).

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 16 shows the standard connection diagram for bipolar operation of any one of the DACs in the AD7568. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R3, R4 and R5 should be ratio matched to 0.01%.

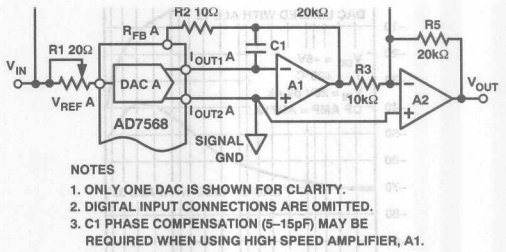


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

Table IV. Bipolar (Offset Binary) Code Table

Digital Input MSB . . . . . LSB	Analog Output (V_{OUT} As Shown in Figure 16)
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	$+V_{REF}$ (0/2048) = 0
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0001	$-V_{REF}$ (2047/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

NOTE
Nominal LSB size for the circuit of Figure 16 is given by: V_{REF} (1/2048).

SINGLE SUPPLY CIRCUITS

The AD7568 operates from a single +5 V supply, and this makes it ideal for single supply systems. When operating in such a system, it is not possible to use the standard circuits of Figures 15 and 16 since these invert the analog input, V_{IN}. There are two alternatives. One of these continues to operate the DAC as a current-mode device, while the other uses the voltage switching mode.

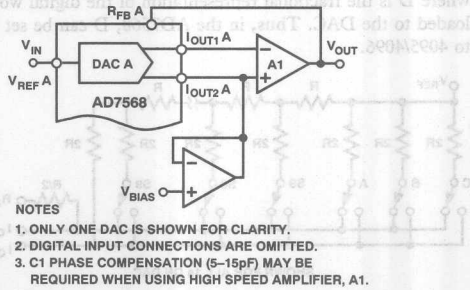


Figure 17. Single Supply Current-Mode Operation

Current Mode Circuit

In the current mode circuit of Figure 17, I_{OUT2}, and hence I_{OUT1}, is biased positive by an amount V_{BIAS}. For the circuit to operate correctly, the DAC ladder termination resistor must be connected internally to I_{OUT2}. This is the case with the AD7568. The output voltage is given by:

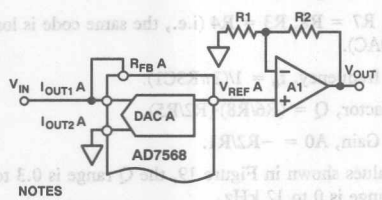
$$V_{OUT} = \left\{ D\frac{R_{FB}}{R_{DAC}} (V_{BIAS} - V_{IN}) \right\} + V_{BIAS}$$

As D varies from 0 to 4095/4096, the output voltage varies from $V_{OUT} = V_{BIAS}$ to $V_{OUT} = 2\ V_{BIAS} - V_{IN}$. V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the I_{OUT2} terminal without any problems.

Voltage Mode Circuit

Figure 18 shows DAC A of the AD7568 operating in the voltage-switching mode. The reference voltage, V_{IN} is applied to the I_{OUT1} pin, I_{OUT2} is connected to AGND and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage making single supply operation possible. The output from the DAC is a voltage at a constant impedance (the DAC ladder resistance). Thus, an op amp is necessary to buffer the output voltage. The reference voltage input no longer sees a constant input impedance, but one which varies with code. So, the voltage input should be driven from a low impedance source.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC no longer have the same source-drain voltage. As a result, their on-resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 volts or an internal diode will turn on, causing possible damage to the device. This means that the full-range multiplying capability of the DAC is lost.



NOTES
1) ONLY ONE DAC IS SHOWN FOR CLARITY.
2) DIGITAL INPUT CONNECTIONS ARE OMITTED.
3) C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER, A1.

Figure 18. Single Supply Voltage Switching Mode Operation

APPLICATIONS

Programmable State Variable Filter

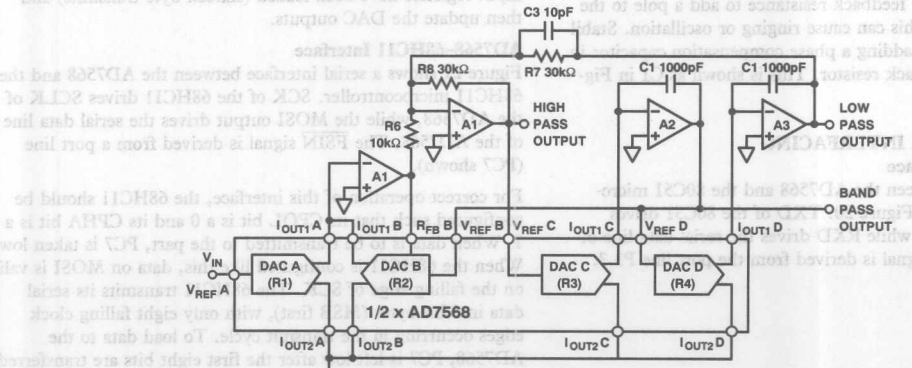
The AD7568 with its multiplying capability and fast settling time is ideal for many types of signal conditioning applications. The circuit of Figure 19 shows its use in a state variable filter design. This type of filter has three outputs: low pass, high pass and bandpass. The particular version shown in Figure 19 uses one half of an AD7568 to control the critical parameters f_0, Q and A_0. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements. Thus, R1 in Figure 19 is controlled by the 12-bit digital word loaded to DAC A of the AD7568. This is also the case with R2, R3 and R4. The fixed resistor R5 is the feedback resistor, $R_{FB}B$.

DAC Equivalent Resistance, $R_{EQ} = (R_{LADDER} \times 4096)/N$

where:

R_{LADDER} is the DAC ladder resistance.

N is the DAC Digital Code in Decimal ($0 < N < 4096$).



NOTES
1. A1, A2, A3, A4: 1/4 x AD713
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN BANDWIDTH LIMITATIONS.

Figure 19. Programmable 2nd Order State Variable Filter

In the circuit of Figure 19:

C1 = C2, R7 = R8, R3 = R4 (i.e., the same code is loaded to each DAC).

Resonant frequency, $f_0 = 1/(2\pi R3C1)$.

Quality Factor, $Q = (R6/R8)\cdot(R2/R5)$.

Bandpass Gain, $A0 = -R2/R1$.

Using the values shown in Figure 19, the Q range is 0.3 to 5, and the f_0 range is 0 to 12 kHz.

APPLICATION HINTS

Output Offset

CMOS D/A converters in circuits such as Figures 15, 16 and 17 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. For the AD7568 to maintain specified accuracy with V_{REF} at 10 V, it is recommended that V_{OS} be no greater than 500 μV, or $(50 \times 10^{-6})\cdot(V_{REF})$, over the temperature range of operation. Suitable amplifiers include the AD OP-07, AD OP-27, OP-177, AD711, AD845 or multiple versions of these.

Temperature Coefficients

The gain temperature coefficient of the AD7568 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full-scale in Figures 15 and 16, their temperature coefficients should be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Application Note, Publication Number E630c–5–3/86, available from Analog Devices.

High Frequency Considerations

The output capacitances of the AD7568 DACs work in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 in Figures 15, 16 and 17.

MICROPROCESSOR INTERFACING

AD7568–80C51 Interface

A serial interface between the AD7568 and the 80C51 microcontroller is shown in Figure 20. TXD of the 80C51 drives SCLK of the AD7568 while RXD drives the serial data line of the part. The $\overline{FSIN}$ signal is derived from the port line P3.3.

The 80C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the data word transmitted to the AD7568 corresponds to the loading sequence shown in Table I. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 80C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7568, P3.3 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7568. When the second serial transfer is complete, the P3.3 line is taken high. Note that the 80C51 outputs the serial data byte in a format which has the LSB first. The AD7568 expects the MSB first. The 80C51 transmit routine should take this into account.

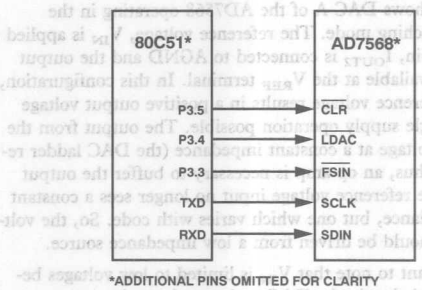


Figure 20. AD7568 to 80C51 Interface

$\overline{LDAC}$ and $\overline{CLR}$ on the AD7568 are also controlled by 80C51 port outputs. The user can bring $\overline{LDAC}$ low after every two bytes have been transmitted to update the DAC which has been programmed. Alternatively, it is possible to wait until all the input registers have been loaded (sixteen byte transmits) and then update the DAC outputs.

AD7568–68HC11 Interface

Figure 21 shows a serial interface between the AD7568 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7568, while the MOSI output drives the serial data line of the AD7568. The $\overline{FSIN}$ signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7568, PC7 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7568. When the second serial transfer is complete, the PC7 line is taken high.

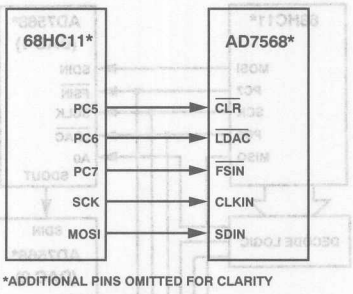


Figure 21. AD7568 to 68HC11 Interface

In Figure 21, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are controlled by the PC6 and PC5 port outputs. As with the 80C51, each DAC of the AD7568 can be updated after each two-byte transfer, or else all DACs can be simultaneously updated.

AD7568–ADSP-2101 Interface

Figure 22 shows a serial interface between the AD7568 and the ADSP-2101 digital signal processor. The ADSP-2101 may be set up to operate in the SPORT Transmit Normal Internal Framing Mode. The following ADSP-2101 conditions are recommended: Internal SCLK; Active High Framing Signal; 16-bit word length. Transmission is initiated by writing a word to the TX register after the SPORT has been enabled. The data is then clocked out on every rising edge of SCLK after TFS goes low. TFS stays low until the next data transfer.

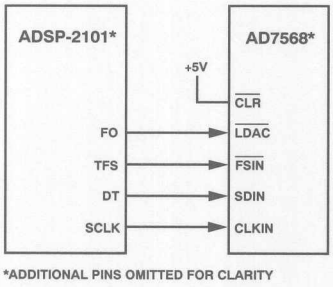


Figure 22. AD7568 to ADSP-2101 Interface

AD7568–TMS320C25 Interface

Figure 23 shows an interface circuit for the TMS320C25 digital signal processor. The data on the DX pin is clocked out of the processor's Transmit Shift Register by the CLKX signal. 16-bit transmit format should be chosen by setting the FO bit in the ST1 register to 0. The transmit operation begins when data is written into the data transmit register of the TMS320C25. This data will be transmitted when the FSX line goes low while

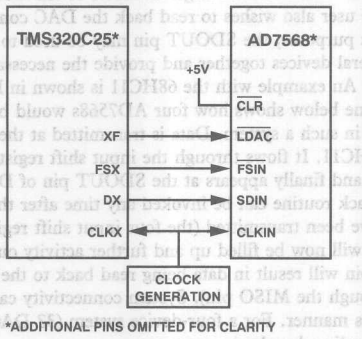


Figure 23. AD7568 to TMS320C25 Interface

CLKX is high or going high. The data, starting with the MSB, is then shifted out to the DX pin on the rising edge of CLKX. When all bits have been transmitted, the user can update the DAC outputs by bringing the XF output flag low.

Multiple DAC Systems

If there are only two AD7568s in a system, there is a simple way of programming each. This is shown in Figure 24. If the user wishes to program one of the DACs in the first AD7568, then DB3 of the serial bit stream should be set to 0, to correspond to the state of the A0 pin on that device. If the user wishes to program a DAC in the second AD7568, then DB3 should be set to 1, to correspond to A0 on that device.

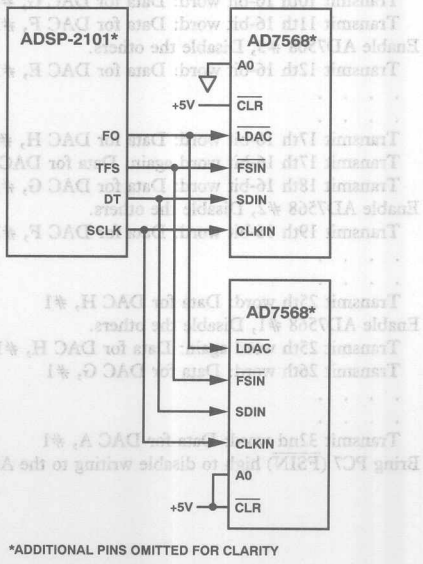


Figure 24. Interfacing ADSP-2101 to Two AD7568s

For systems which contain larger numbers of AD7568s and where the user also wishes to read back the DAC contents for diagnostic purposes, the SDOUT pin may be used to daisy chain several devices together and provide the necessary serial readback. An example with the 68HC11 is shown in Figure 25. The routine below shows how four AD7568s would be programmed in such a system. Data is transmitted at the MOSI pin of the 68HC11. It flows through the input shift registers of the AD7568s and finally appears at the SDOUT pin of DAC N. So, the readback routine can be invoked any time after the first four words have been transmitted (the four input shift registers in the chain will now be filled up and further activity on the CLKIN pin will result in data being read back to the microcomputer through the MISO pin). System connectivity can be verified in this manner. For a four-device system (32 DACs) a two-line to four-line decoder is necessary.

Note that to program the 32 DACs, 35 transmit operations are needed. In the routine, three words must be retransmitted. The first word for DACs #3, #2 and #1 must be transmitted twice in order to synchronize their arrival at the SDIN pin with A0 going low.

Table V. Routine for Loading 4 AD7568s Connected As in Figure 25

Bring PC7 ($\overline{FSIN}$) low to allow writing to the AD7568s.
Enable AD7568 #4 (Bring A0 low). Disable the others.
  Transmit 1st 16-bit word: Data for DAC H, #4
  . . .
  . . .
  Transmit 9th 16-bit word: Data for DAC H, #3
  Transmit 9th 16-bit word again: Data for DAC H, #3
  Transmit 10th 16-bit word: Data for DAC G, #3
  Transmit 11th 16-bit word: Data for DAC F, #3
Enable AD7568 #3, Disable the others.
  Transmit 12th 16-bit word: Data for DAC E, #3
  . . . .
  . . . .
  Transmit 17th 16-bit word: Data for DAC H, #2
  Transmit 17th 16-bit word again: Data for DAC H, #2
  Transmit 18th 16-bit word: Data for DAC G, #2
Enable AD7568 #2, Disable the others.
  Transmit 19th 16-bit word: Data for DAC F, #2
  . . . .
  . . . .
  Transmit 25th word: Data for DAC H, #1
Enable AD7568 #1, Disable the others.
  Transmit 25th word again: Data for DAC H, #1
  Transmit 26th word: Data for DAC G, #1
  . . . .
  . . . .
  Transmit 32nd word: Data for DAC A, #1
Bring PC7 ($\overline{FSIN}$) high to disable writing to the AD7568s.

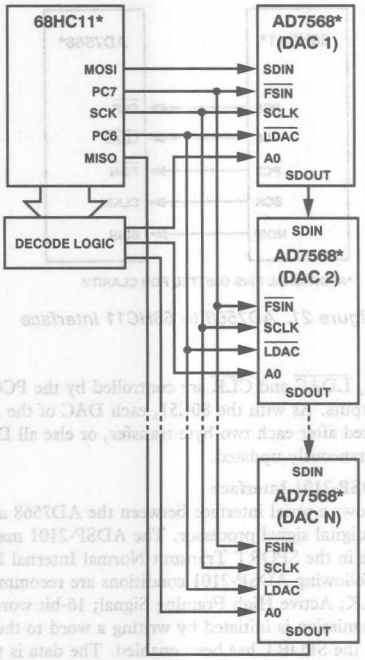


Figure 25. Multi-DAC System

Buffered Multiplying DAC

AD7628

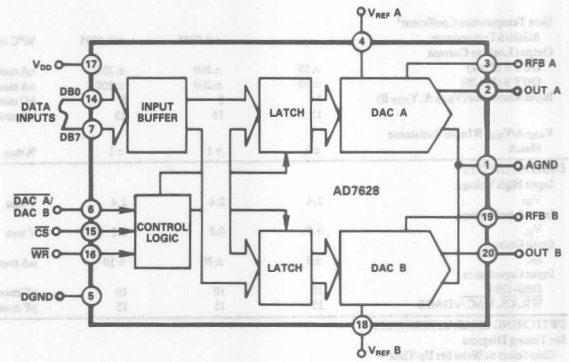
FEATURES

On-Chip Latches for Both DACs
+12V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible from +12V to +15V
Latch Free (Protection Schottkys not Required)

APPLICATIONS

Disk Drives
Programmable Filters
X-Y Graphics
Gain/Attenuation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7628 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in small 0.3"-wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC}}$ A/DAC B determines which DAC is to be loaded. The AD7628's load cycle is similar to the write cycle of a random access memory, and the device is bus compatible with most 8-bit microprocessors, including 6502, 6809, 8085, Z80.

The device operates from a +12V to +15V power supply and is TTL-compatible over this range. Power dissipation is a low 20mW.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7628 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7628's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC}}$ A/DAC B select line has allowed the AD7628 to be packaged in a small 20-pin 0.3" wide DIP, 20-pin SOIC, 20-terminal PLCC and 20-terminal LCC.
3. TTL-Compatibility: All digital inputs are TTL-compatible over a +12V to +15V power supply range.

AD7628—SPECIFICATIONS

V_{DD} = +10.8V to +15.75V, (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	T_A = +25°C[1]	T_A = −40°C to +85°C	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	8	8	8	Bits	
Relative Accuracy	±1/2	±1/2	±1/2	LSB max	This is an Endpoint Linearity Specification
Differential Nonlinearity	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	±2	±3	±3	LSB max	Measured Using Internal RFB A and RFB B. Both DAC Latches Loaded with 11111111. Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	–	±0.0035	±0.0035	%/°C max	
Output Leakage Current					
OUT A (Pin 2)	±50	±200	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	±50	±200	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	±1	±1	±1	% max	
DIGITAL INPUTS[4]					
Input High Voltage V_{IH}	2.4	2.4	2.4	V min	
Input Low Voltage V_{IL}	0.8	0.8	0.8	V max	
Input Current I_{IN}	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance					
DB0–DB7	10	10	10	pF max	
WR, CS, DAC A/DAC B	15	15	15	pF max	
SWITCHING CHARACTERISTICS[3] See Timing Diagram					
Chip Select to Write Set Up Time t_{CS}	160	160	210	ns min	
Chip Select to Write Hold Time t_{CH}	10	10	10	ns min	
DAC Select to Write Set Up Time t_{AS}	160	160	210	ns min	
DAC Select to Write Hold Time t_{AH}	10	10	10	ns min	
Data Valid to Write Set Up Time t_{DS}	160	160	210	ns min	
Data Valid to Write Hold Time t_{DH}	10	10	10	ns min	
Write Pulse Width t_{WR}	150	170	210	ns min	
POWER SUPPLY					See Figure 3
I_{DD}, K Grade	2	2	–	mA	All Digital Inputs V_{IL} or V_{IH}
B, T Grades	2	2.5	2.5	mA	All Digital Inputs V_{IL} or V_{IH}
All Grades	100	500	500	μA	All Digital Inputs 0V or V_{DD}

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

V_{DD} = +10.8V to +15.75V. (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	T_A = +25°C[1]	T_A = −40°C to +85°C[1]	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	0.01	0.02	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME	350	400	400	ns max	To 1/2LSB. Out A/Out B load = 100Ω. WR = CS = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL-TO-ANALOG GLITCH IMPULSE	330	–	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE					
C_{OUT} A	25	25	25	pF max	DAC Latches Loaded with 00000000
C_{OUT} B	25	25	25	pF max	
C_{OUT} A	60	60	60	pF max	DAC Latches Loaded with 11111111
C_{OUT} B	60	60	60	pF max	
AC FEEDTHROUGH					
V_{REF} A to OUT A	−70	−65	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B	−70	−65	−65	dB max	@ 10kHz
CHANNEL-TO-CHANNEL ISOLATION					Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	−80	–	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 10kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A	−80	–	–	dB typ	V_{REF} B = 20V p-p Sine Wave @ 10kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	60	–	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	−85	–	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are K Version; −40°C to +85°C
B Version; −40°C to +85°C
T Version; −55°C to +125°C
[2]Specification applies to both DACs in AD7628.
[3]Guaranteed by design but not production tested.
[4]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (K) Grades	−40°C to +85°C
Industrial (B) Grades	−40°C to +85°C
Extended (T) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Gain Error	Package Option[2]
AD7628KN	−40°C to +85°C	±1/2LSB	±2LSB	N-20
AD7628KP	−40°C to +85°C	±1/2LSB	±2LSB	P-20A
AD7628KR	−40°C to +85°C	±1/2LSB	±2LSB	R-20
AD7628BQ	−40°C to +85°C	±1/2LSB	±2LSB	Q-20
AD7628TQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-20
AD7628TE	−55°C to +125°C	±1/2LSB	±2LSB	E-20A

NOTES

[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full-scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC latches after offset error has been adjusted out. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

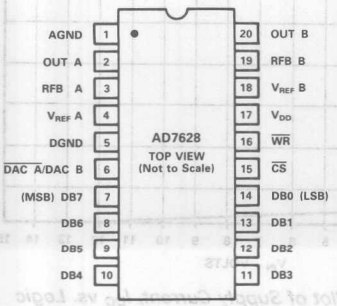
Digital-to-Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

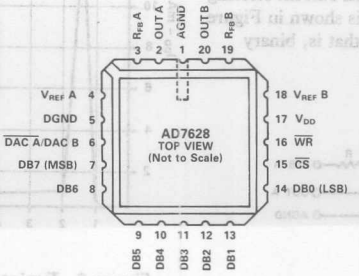
Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS

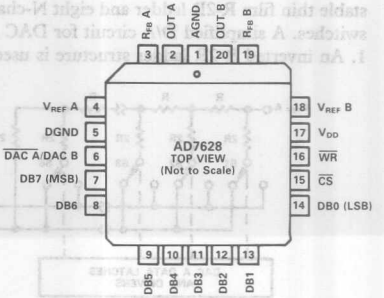
DIP, SOIC



LCCC



PLCC



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

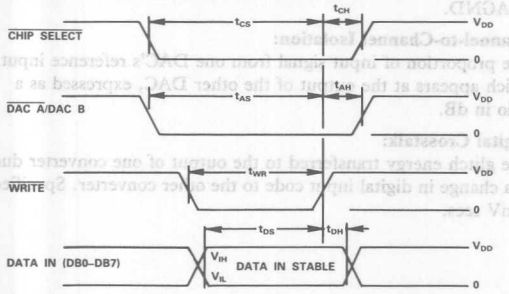
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. V_{DD} = +10.8V TO +15.75V, $t_R = t_F$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION – D/A SECTION

The AD7628 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

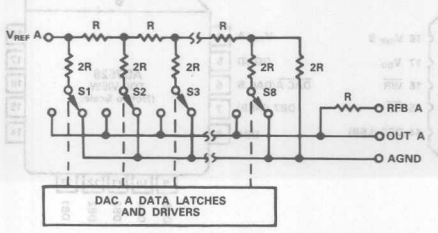


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7628's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. $g(V_{REF} A, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

For further information on CMOS multiplying D/A converters refer to "CMOS DAC Application Guide, 2ND Edition" available from Analog Devices, Publication Number G872a–15–4/86.

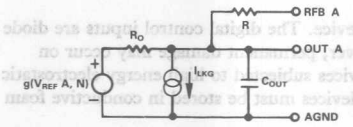


Figure 2. Equivalent Analog Output Circuit of DAC A

CIRCUIT INFORMATION – DIGITAL SECTION

The input buffers are simple CMOS level-shifters designed such that when the AD7628 is operated with V_{DD} from 10.8V to 15.75V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 1.0 volt to 2.0 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7628 may be operated with any supply voltage in the range $10.8 \leq V_{DD} \leq 15.75$ volts.

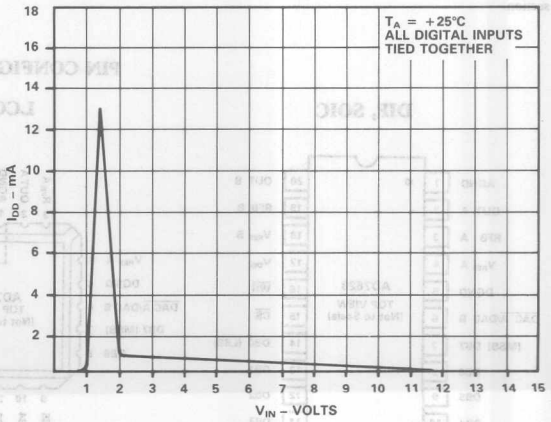


Figure 3. Typical Plot of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN} for V_{DD} = +15V.

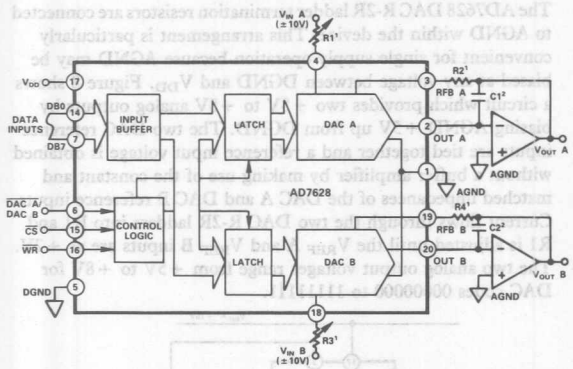


Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.

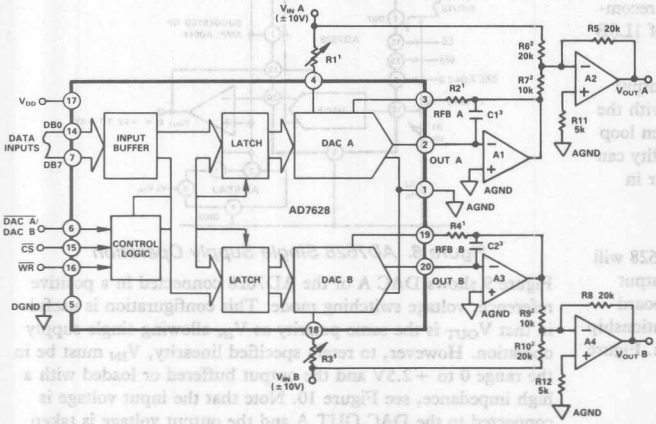


Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	K/B/T
R1; R3	500
R2; R4	150

Table III. Recommended Trim Resistor Values

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7628 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7628 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7628. In more complex systems where the AGND–DGND intertie is on the back-plane, it is recommended that diodes be connected in inverse parallel between the AD7628 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7628 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7628 and the AD644 dual op-amp which minimizes feedthrough and crosstalk.

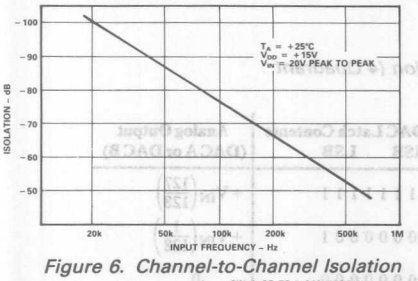


Figure 6. Channel-to-Channel Isolation

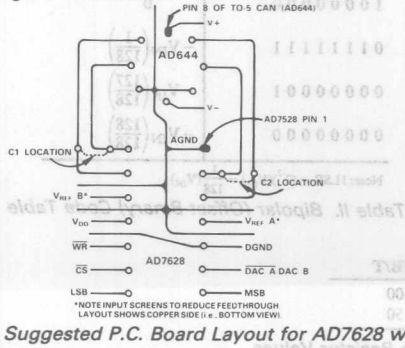


Figure 7. Suggested P.C. Board Layout for AD7628 with AD644 Dual Op-Amp

SINGLE SUPPLY APPLICATIONS

The AD7628 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit which provides two +5V to +8V analog outputs by biasing AGND +5V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2V. The two analog output voltages range from +5V to +8V for DAC codes 00000000 to 11111111.

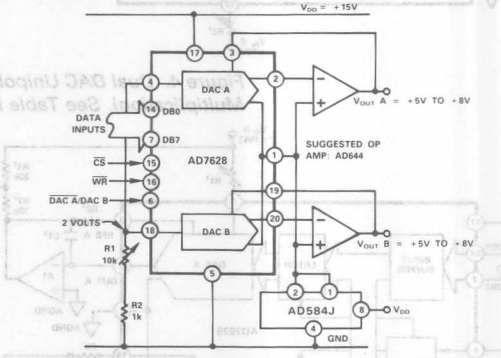


Figure 8. AD7628 Single Supply Operation

Figure 9 shows DAC A of the AD7628 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 to +2.5V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC V_{REF} A pin.

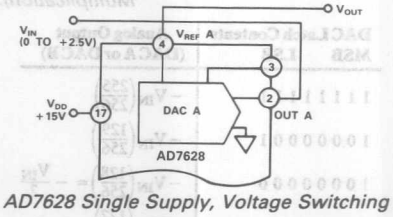


Figure 9. AD7628 Single Supply, Voltage Switching Mode

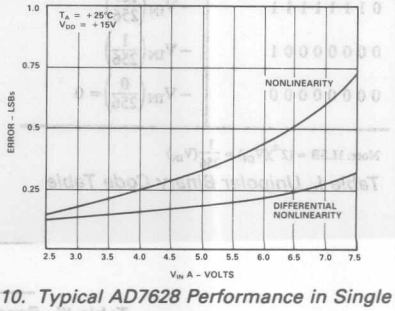


Figure 10. Typical AD7628 Performance in Single Supply Voltage Switching Mode

MICROPROCESSOR INTERFACE

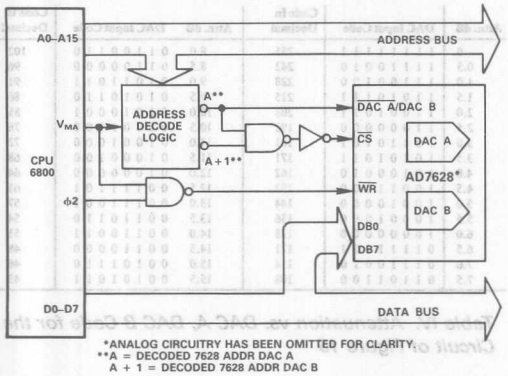


Figure 11. AD7628 Dual DAC to 6800 CPU Interface

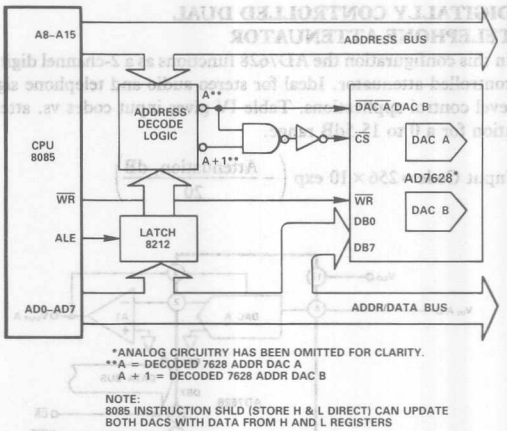


Figure 12. AD7628 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

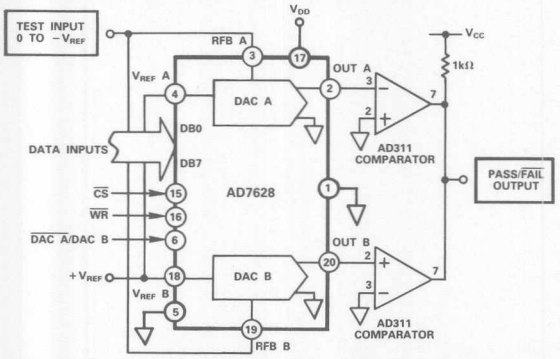


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7628 is used to implement a programmable window comparator. DACS A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

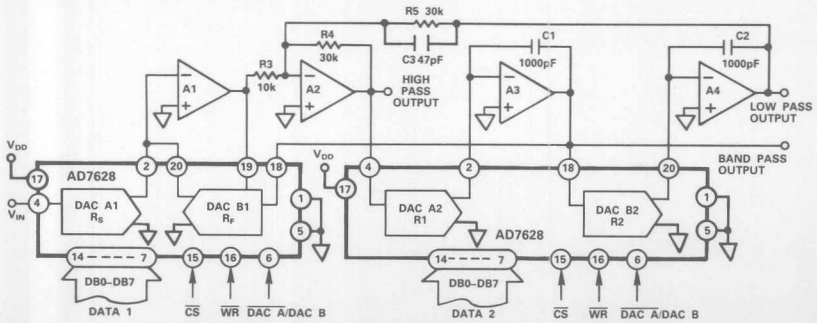


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$f_C = \frac{1}{2\pi\ R_1\ C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals
$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7628. Op amps are 2×AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is fc = 0 to 15kHz and Q = 0.3 to 4.5.

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

In this configuration the AD7628 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 to 15.5dB range.

$$\text{Input Code} = 256 \times 10 \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

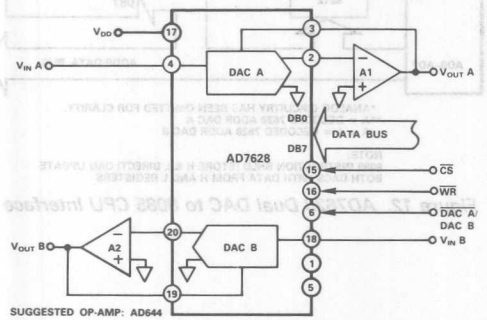


Figure 15. Digitally Controlled Dual Telephone Attenuator

Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

Dual 8-Bit Buffered Multiplying CMOS D/A Converter

PM-7628

FEATURES

- On-Chip Latches for Both DACs
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible from +5V To +15V
- 8-Bit Endpoint Linearity (±1/2 LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible (60ns Write Time)
- Improved ESD and Latch-Up Resistance
- Automatically Insertable CerDIP and Plastic Packages
- Available in Surface Mount SO, PLCC, and LCC Packages
- Improved AD7628
- Available in Die Form

APPLICATIONS

- Disk Drives
- Digital Gain/Attenuation Control
- Digitally-Controlled Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

		PACKAGE: 20-Pin DIP	
RELATIVE ACCURACY	GAIN ERROR T_A = +25°C	MILITARY* TEMPERATURE –55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C TO +85°C
±1/2LSB	±2LSB	PM7628AR	PM7628ER
±1/2LSB	±2LSB	PM7628ARC/883	PM7628FP
±1/2LSB	±2LSB	–	PM-7628FPC††
±1/2LSB	±2LSB	–	PM7628FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7628 is an improved version of the AD7628 offering TTL compatibility from +5 to +15 volts and faster AC timing. It contains two 8-bit multiplying CMOS digital-to-analog converters that are fabricated in a single chip. This monolithic construction offers excellent DAC-to-DAC matching and tracking over temperature.

The PM-7628 consists of two thin-film R-2R resistor-ladder networks, two tracking span resistors, two data latches, one input buffer, and control logic circuitry.

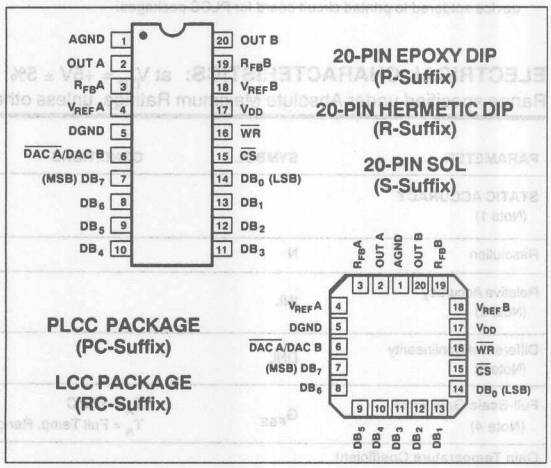
The PM-7628's digital inputs are bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. Data loading is similar to that of a RAM's write cycle. Digital input data is directed into one of the DAC data latches determined by the DAC selection control line DAC A/DAC B.

Operating from a single +5V to +15V power supply, the PM-7628 dissipates only 12mW of power in a space saving 20-pin 0.3" DIP, and 20-terminal surface mount packages. The PM-7628 features circuitry designed to protect against damage from electrostatic discharges.

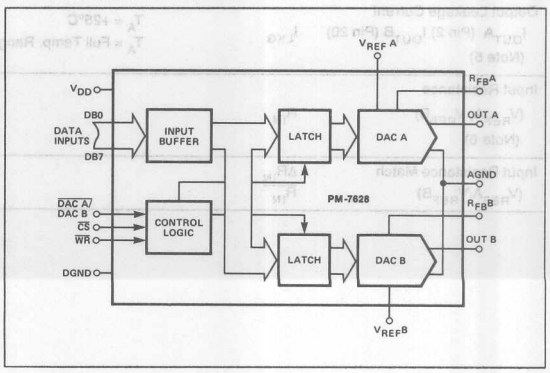
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7628AR	AD7628TQ	MIL
PM7628ARC/883	AD7628TE	
PM7628ER	AD7628BQ	IND
PM7628FP	AD7628KN	COM
PM7628FPC	AD7628KP	

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V to +17V
AGND to DGND ..... 0V, V_{DD} + 0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} + 0.3V
V_{PIN2}, V_{PIN20} to AGND ..... –0.3V, V_{DD}
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V
Operating Temperature Range
AR, ARC Versions ..... –55°C to +125°C
ER, FP, FPC, FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	80	15	°C/W
20-Pin Plastic DIP (P)	74	32	°C/W
20-Contact LCC (RC)	89	27	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damag- may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready for use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS:

at V_{DD} = +5V ± 5%; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full-Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	– –	±0.5 ±1.0	±2 ±3	LSB
Gain Temperature Coefficient (Δ Gain / Δ Temperature) (Notes 4, 10)	TCG_{FS}		–	–	±0.007	%/°C
Output Leakage Current $I_{OUT}A$ (Pin 2) $I_{OUT}B$ (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	– –	±5 –	±50 ±200	nA
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	–	15	kΩ
Input Resistance Match ($V_{REF}A$/$V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%

ELECTRICAL CHARACTERISTICS: at V_{DD} = +5V ± 5%; $V_{REF}A = V_{REF}B$ = +10V; $I_{OUT}A = I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}		2.4	–	–	V
Digital Input Low (Note 8)	V_{INL}		–	–	0.8	V
Input Current (Note 7)	I_{IN}	T_A = +25°C	–	±.001	±1	µA
		T_A = Full Temp. Range	–	–	±10	
Input Capacitance (Note 10)	C_{IN}	DB0-DB7	–	–	10	pF
		$\overline{WR}$, $\overline{CS}$, DAC A /DAC B	–	–	15	
SWITCHING CHARACTERISITCS (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}		100	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		100	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		100	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		90	–	–	ns
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Input = V_{INH} or V_{INL}	–	–	1	mA
		All Digital Input = 0V or V_{DD}				
		T_A = +25°C	–	–	0.5	mA
		T_A = Full Temp. Range	–	–	1.0	

2

ELECTRICAL CHARACTERISTICS: at V_{DD} = +5V ± 5%; $V_{REF}A = V_{REF}B$ = +10V; $I_{OUT}A = I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
AC PERFORMANCE CHARACTERISTIC (Note 12)						
DC Supply Rejection Ratio (Δ Gain / ΔV_{DD}) (Note 13)	PSRR	T_A = +25°C	–	–	0.02	%/%
		T_A = Full Temp. Range	–	–	0.04	
Current Settling Time (Notes 10, 15, 16, 20)	t_S	T_A = Full Temp. Range	–	–	300	ns
Digital Charge Injection (Note 17)	Q	T_A = +25°C	–	100	–	nVs
Output Capacitance	$C_{OUT}A$	DAC Latches Loaded	–	–	25	pF
	$C_{OUT}B$	with 0000 0000	–	–	25	
	$C_{OUT}A$	DAC Latches Loaded	–	–	60	
	$C_{OUT}B$	with 1111 1111	–	–	60	
AC Feedthrough (Note 18)	FT_A	$V_{REF}A$ to $I_{OUT}A$:				dB
		T_A = +25°C	–	–	–70	
		T_A = Full Temp. Range	–	–	–65	
	FT_B	$V_{REF}B$ to $I_{OUT}B$:				
		T_A = +25°C	–	–	–70	
		T_A = Full Temp. Range	–	–	–65	
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	$V_{REF}A$ to $I_{OUT}B$: $V_{REF}A = 20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}B$ = 0V; T_A = +25°C	–	–80	–	dB
	CCI_{AB}	$V_{REF}B$ to $I_{OUT}A$; $V_{REF}B = 20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}A$ = 0V; T_A = +25°C	–	–80	–	
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25°C	–	30	–	nVs
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz T_A = +25°C	–	–85	–	dB

ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	– –	±0.5 ±1	±2 ±3	LSB
Gain Temperature Coefficient (Δ Gain / Δ Temperature) (Notes 4, 10)	TCG_{FS}		–	–	±0.0035	%/°C
Output Leakage Current $I_{OUT}A$ (Pin 2) $I_{OUT}B$ (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	– –	±5 –	±50 ±200	nA
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}		2.4	–	–	V
Digital Input Low (Note 8)	V_{INL}		–	–	0.8	V
Input Current (Note 7)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	– –	±.001 –	±1 ±10	µA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, DAC A /$\overline{DAC\ B}$	– –	– –	10 15	pF

ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

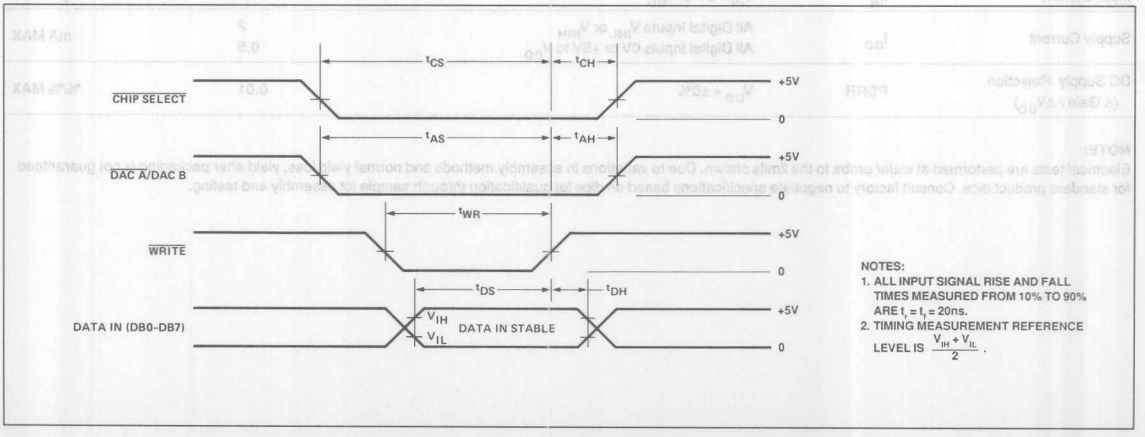
PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
SWITCHING CHARACTERISITCS (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		70	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		60	–	–	ns
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Input = V_{INH} or V_{INL}				
		T_A = +25°C	–	–	2	mA
		T_A = Full Temp. Range	–	–	2.5	mA
		All Digital Input = 0V or +5V to V_{DD}				
		T_A = +25°C	–	–	0.5	mA
		T_A = Full Temp. Range	–	–	1.0	mA
AC PERFORMANCE CHARACTERISTIC (Note 12)						
DC Supply Rejection Ratio (Δ Gain / ΔV_{DD}) (Note 13)	PSRR	T_A = +25°C	–	–	0.01	%/%
		T_A = Full Temp. Range	–	–	0.02	%/%
Current Settling Time (Notes 10, 15, 16, 20)	t_S	T_A = Full Temp. Range	–	–	200	ns
Digital Charge Injection (Note 17)	Q	T_A = +25°C	–	160	–	nVs
Output Capacitance	$C_{OUT}A$	DAC Latches Loaded	–	–	25	pF
	$C_{OUT}B$	with 0000 0000	–	–	25	pF
	$C_{OUT}A$	DAC Latches Loaded	–	–	60	pF
	$C_{OUT}B$	with 1111 1111	–	–	60	pF

ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V, $V_{REF}A$ = $V_{REF}B$ = +10V, I_{OUT} = I_{OUT} = 0 A
Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7628 TYP	MAX	UNITS
AC Feedthrough (Note 18)	FT_A	$V_{REF}A$ to $I_{OUT}A$: T_A = +25°C	–	–	–70	dB
		T_A = Full Temp. Range	–	–	–65	
	FT_B	$V_{REF}B$ to $I_{OUT}B$: T_A = +25°C	–	–	–70	
		T_A = Full Temp. Range	–	–	–65	
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	$V_{REF}A$ to $I_{OUT}B$: $V_{REF}A$ = 20V_{p-p} Sinewave @ f = 10kHz $V_{REF}B$ = 0V; T_A = +25°C	–	–80	–	dB
	CCI_{AB}	$V_{REF}B$ to $I_{OUT}A$; $V_{REF}B$ = 20V_{p-p} Sinewave @ f = 10kHz $V_{REF}A$ = 0V; T_A = +25°C	–	–80	–	
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25°C	–	50	–	nVs
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz T_A = +25°C	–	–85	–	dB

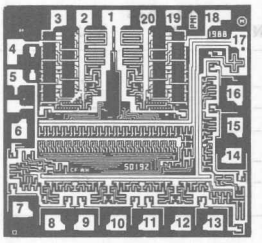
NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All grades guaranteed to be monotonic over the full operating temperature range.
4. Measured using internal $R_{FB}A$ and $R_{FB}B$. Both DAC latches loaded with 1111 1111.
5. DAC loaded with 0000 0000.
6. Input resistance TC = 300 ppm/°C.
7. V_{IN} = 0V or V_{DD}.
8. For all data bits DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$ /DAC B.
9. Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
10. Guaranteed and not tested.
11. See timing diagram.
12. These characteristics are for design guidance only and are not subject to test.
13. ΔV_{DD} = ±5%.
14. From digital input to 90% of final analog-output current.
15. $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$, $I_{OUT}B$ load = 100Ω, C_{EXT} = 13pF.
16. $\overline{WR}$, $\overline{CS}$ = 0V, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
17. For code transition 0000 0000 to 1111 1111.
18. $V_{REF}A$, $V_{REF}B$ = 20V_{p-p} Sinewave @ f = 10kHz.
19. Both DAC latches loaded with 1111 1111.
20. Extrapolated: t_S (1/2 LSB) = t_{PD} + 6.2τ, where τ = the measured first time constant of the final RC decay.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE t_r = t_f = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

DICE CHARACTERISTICS



DIE SIZE 0.082 x 0.078 inch, 6,396 sq. mils
(2.08 x 1.98 mm, 4.126 sq. mm)

1. ANALOG GROUND (AGND)
2. OUTPUT A (OUT A)
3. DAC A FEEDBACK RESISTOR ($R_{FB}A$)
4. DAC A REFEREMCE INPUT ($V_{REF}A$)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC}$ A/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. DAC B FEEDBACK RESISTOR ($R_{FB}B$)
20. OUTPUT B (OUT B)

Substrate (die Backside) is internally connected to V_{DD}.

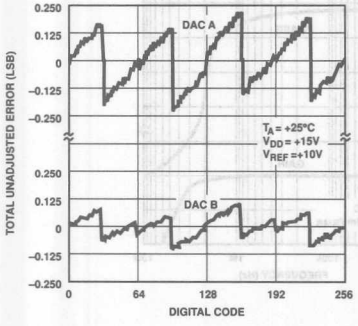
WAFER TEST LIMITS at V_{DD} = +5V, +10.8V or +15.75V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted.

			PM-7628G	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 Pad 2 and 20	±50	nA MAX
Input Resistance	R_{IN}	Pad 4 and 18	8/15	kΩ MIN/ kΩ MAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\Delta V_{REF}A, B$		±1	% MAX
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or +5V to V_{DD}	2 0.5	mA MAX
DC Supply Rejection (Δ Gain / ΔV_{DD})	PSRR	V_{DD} = ±5%	0.01	%/% MAX

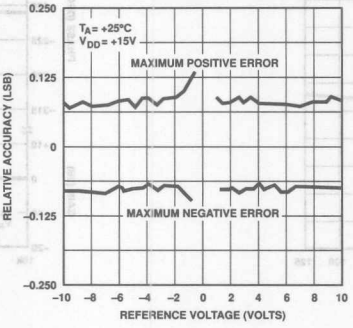
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

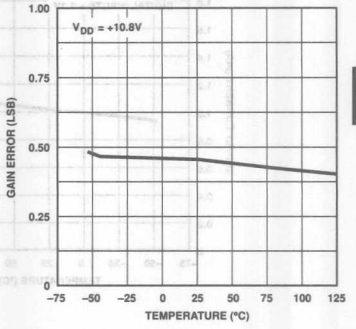
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT



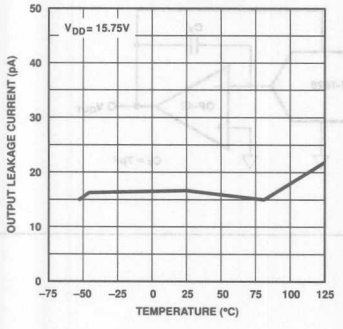
RELATIVE ACCURACY vs REFERENCE VOLTAGE



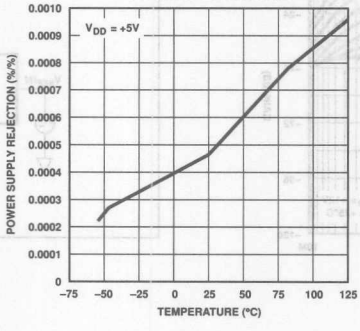
FULL-SCALE GAIN ERROR vs TEMPERATURE



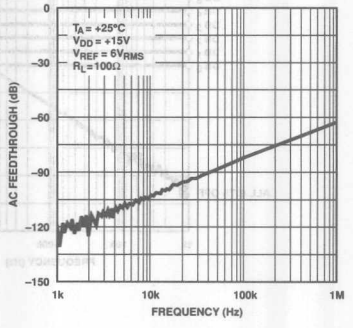
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



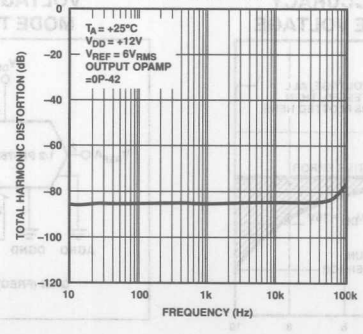
POWER SUPPLY REJECTION vs TEMPERATURE



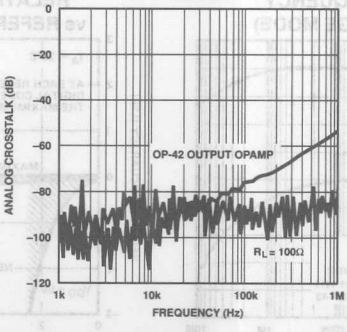
AC FEEDTHROUGH vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

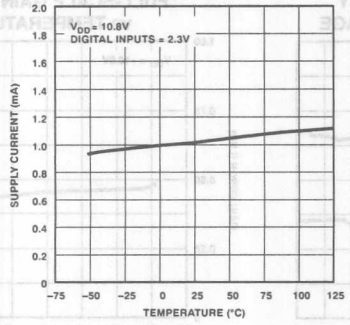


ANALOG CROSSTALK vs FREQUENCY

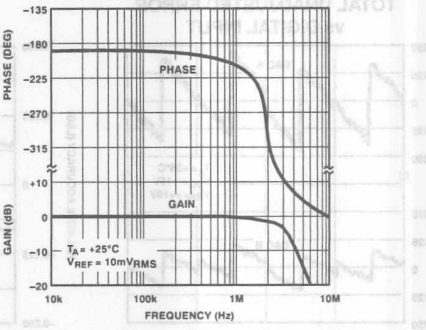


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

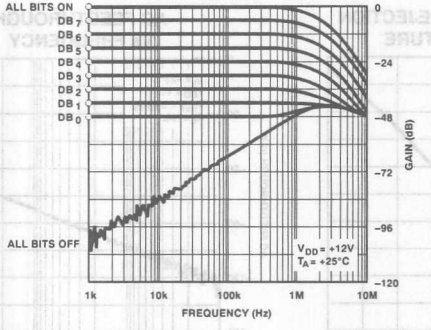
SUPPLY CURRENT (I_{DD}) vs TEMPERATURE



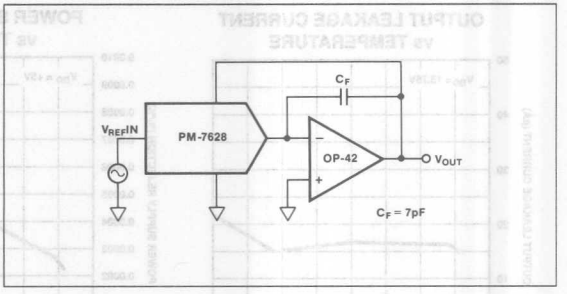
GAIN AND PHASE SHIFT vs FREQUENCY WITH OP-42 OUTPUT AMPLIPHIER



GAIN (V_{OUT}/V_{REF}) vs FREQUENCY

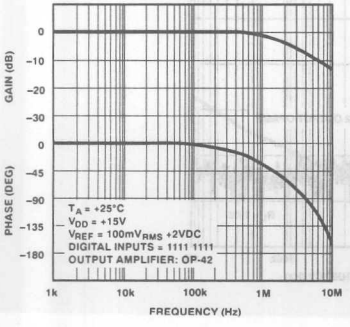


TEST CIRCUIT FOR GAIN vs FREQUENCY

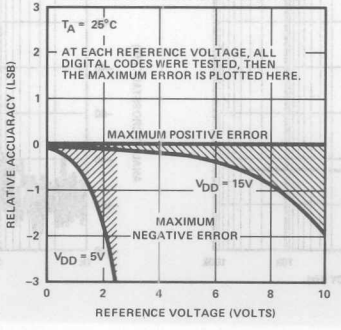


VOLTAGE SWITCHING MODE CHARACTERISTICS

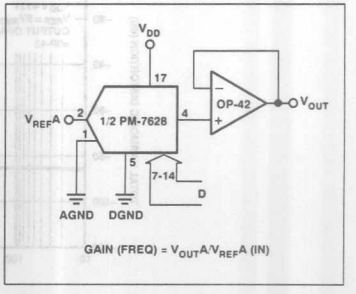
GAIN AND PHASE vs FREQUENCY (VOLTAGE MODE)



RELATIVE ACCURACY vs REFERENCE VOLTAGE



VOLTAGE SWITCHING MODE TEST CIRCUIT



RELATIVE ACCURACY OR INTEGRAL NONLINEARITY (INL)

This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs.

Refer to PMI 1988 Data Book, Section 11, for additional digital-to-analog converter definitions.

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

MODE SELECTION

The inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit line DB0-DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

D/A SECTION

There is a normally closed switch in series with the internal feedback resistor (R_{FB}) as shown in Figure 1. This switch improves linearity performance over temperature and power supply rejection; however, when the circuit is not powered up, the switch assumes an open state.

See the PM-7528 data sheet for additional circuit information and applications.

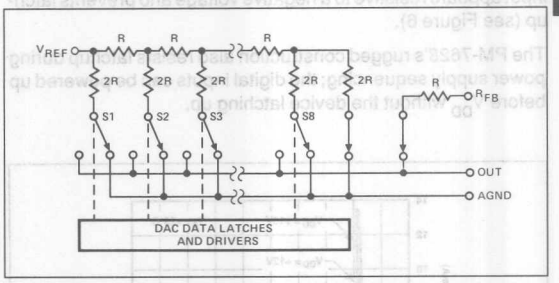


FIGURE 1: *Simplified Functional Circuit for DAC A or DAC B*

DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed such that TTL input levels are converted into internal CMOS logic levels; they are used to drive the internal circuitry. A simple 5V regulator is used to ensure TTL compatibility at V_{DD} = 12V to 15V (see Figure 2).

The PM-7628's digital inputs are TTL compatible between the V_{DD} range of +5V to +16.5V. The digital inputs affect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition region. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption.

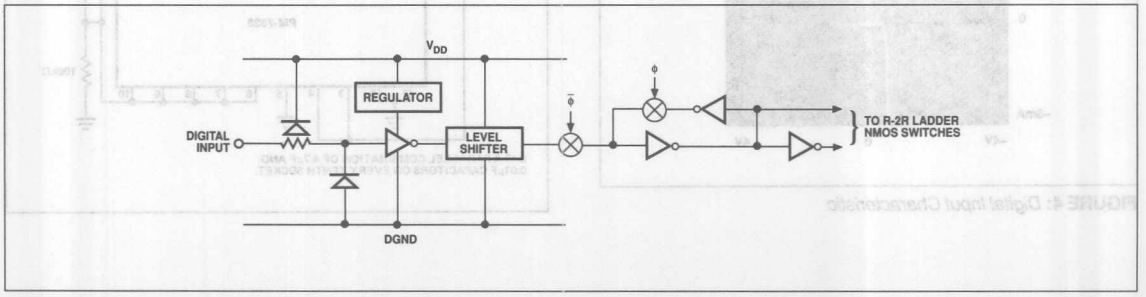


FIGURE 2: *Simplified Schematic of Digital Inputs*

There are several fast logic families that are used to buffer the DAC's digital inputs. These buffers, if not properly terminated, will cause reflections that can exhibit 1.5 to 3V of negative overshoot. This overshoot, when applied to the digital inputs, will cause an internal diode to become forward biased as shown in Figure 4. If sufficient current is generated, most CMOS devices will latchup resulting in a catastrophic failure. The PM-7628 features circuitry designed to reduce the susceptibility of electrostatic discharges and latchup (see Figure 5). As shown, a series resistor has been incorporated into each digital input so that the input appears resistive to a negative voltage and prevents latchup (see Figure 6).

The PM-7628's rugged construction also resists latchup during power supply sequencing; the digital inputs can be powered up before V_{DD} without the device latching up.

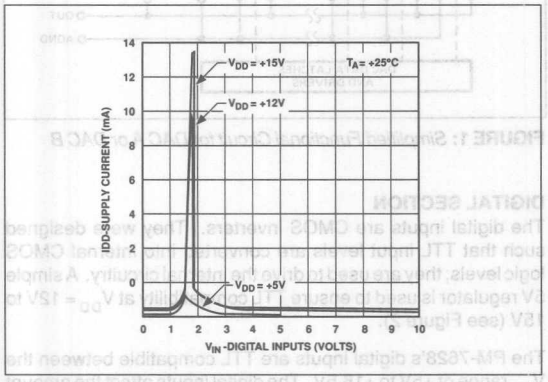


FIGURE 3: *Digital Inputs vs. I_{DD}*

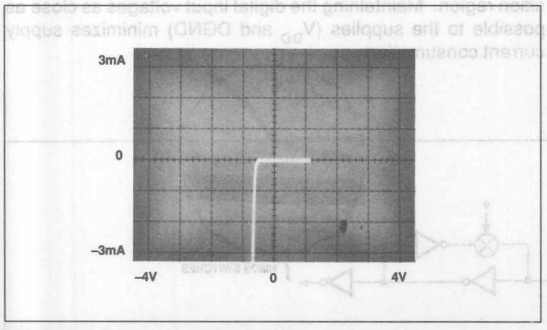


FIGURE 4: *Digital Input Characteristic*

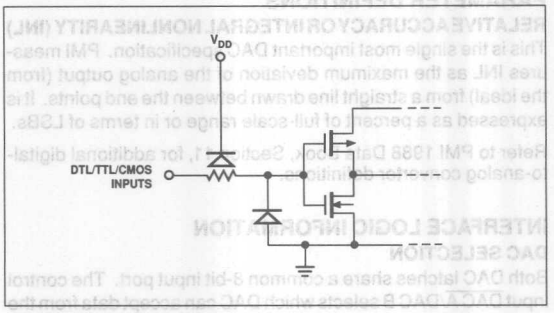


FIGURE 5: *Digital Input Protection*

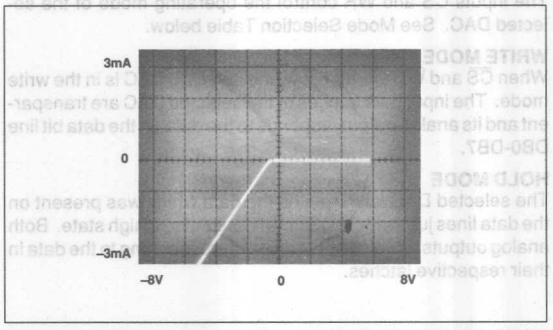
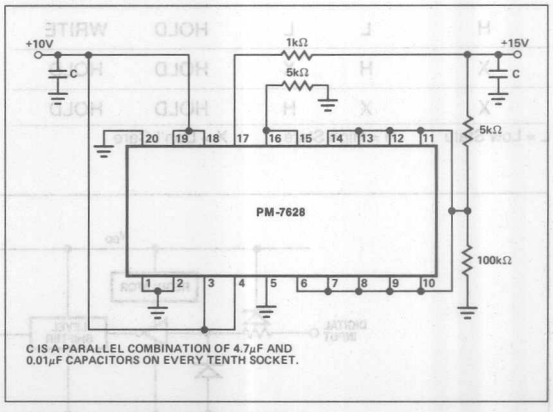


FIGURE 6: *PM-7628 Digital Input Characteristic*

BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The most common application of the PM-7628 is in the voltage output mode. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 7. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB_0 thru DB_7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of ±25 volts for both DC or AC signals. The circuit in Figure 7 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation, connect the PM-7628 as shown in Figure 8. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB_0 thru DB_7. This circuit provides full four-quadrant multiplication, able to accept ± polarities on both inputs as well as the circuit output.

2

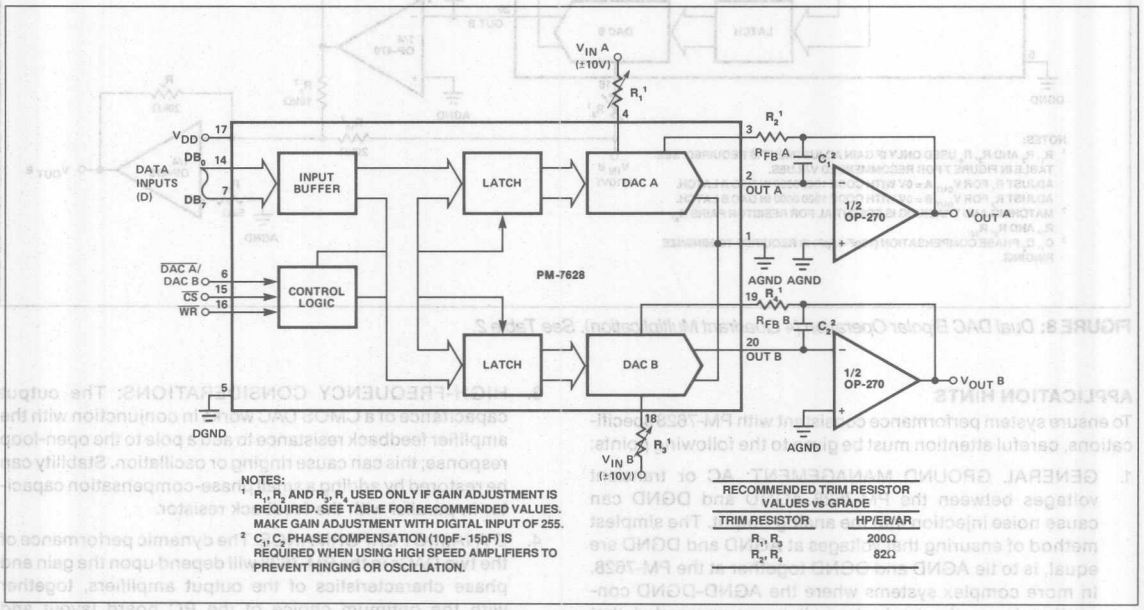


FIGURE 7: *Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.*

TABLE 1: Unipolar Binary Code Table. See Figure 7.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1111 1111	$-V_{IN}\left(\frac{255}{256}\right)$
1000 0001	$-V_{IN}\left(\frac{129}{256}\right)$
1000 0000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0111 1111	$-V_{IN}\left(\frac{127}{256}\right)$
0000 0001	$-V_{IN}\left(\frac{1}{256}\right)$
0000 0000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

NOTE: 1 LSB = (2^{-8}) (V_{IN}) = $\frac{1}{256}(V_{IN})$

TABLE 2: Bipolar (Offset Binary) Code Table. See Figure 8.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1111 1111	$+V_{IN}\left(\frac{127}{128}\right)$
1000 0001	$+V_{IN}\left(\frac{1}{128}\right)$
1000 0000	0
0111 1111	$-V_{IN}\left(\frac{1}{128}\right)$
0000 0001	$-V_{IN}\left(\frac{127}{128}\right)$
0000 0000	$-V_{IN}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = (2^{-7}) (V_{IN}) = $\frac{1}{128}$ (V_{IN})

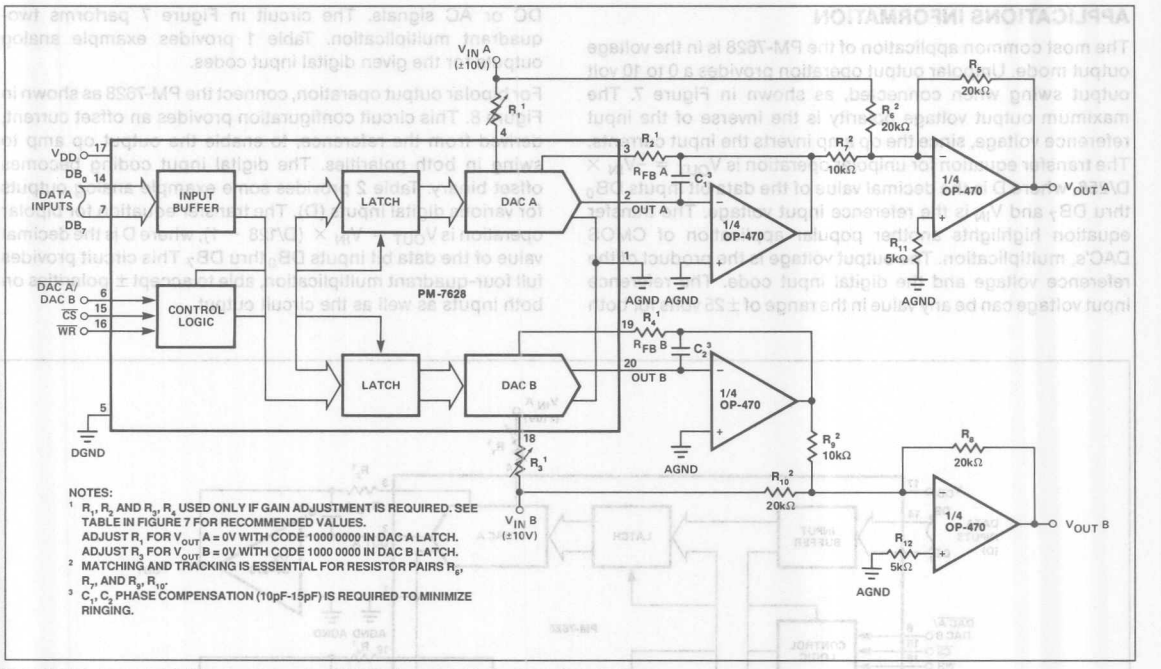


FIGURE 8: *Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.*

APPLICATION HINTS

To ensure system performance consistent with PM-7628 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the PM-7628 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7628. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that Schottky diodes (HP5082-2835 or equivalent) be connected in inverse parallel between the PM-7628 AGND and DGND pins.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of 0.67 V_{OS} (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH-FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a small phase-compensation capacitor in parallel with the feedback resistor.
4. DYNAMIC PERFORMANCE: The dynamic performance of the two DACs in the PM-7628 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
5. CIRCUIT LAYOUT SUGGESTIONS: Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1μF in parallel with a 1μF or 10μF) is recommended across V_{DD} to DGND.

SINGLE SUPPLY OPERATION, VOLTAGE SWITCHING

With the PM-7628 connected in the voltage switching mode of operation (Figure 9) only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, relative accuracy versus input reference voltage, shows that to maintain a ±1/2 LSB maximum linearity error, V_{REF} should be less than 1.5 volts for V_{DD} = 5 volts or less than 6 volts for V_{DD} = 15 volts. The gain-phase response graph shows dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when V_{DD} = 5 volts. Additionally, settling time measures 400 to 500 nanoseconds for a digital input change of 255 to 0 when V_{DD} = 5V.

The output terminal in the voltage switching mode has a constant output resistance (≈11kΩ) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.

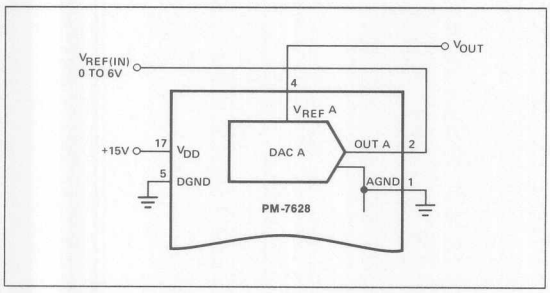


FIGURE 9: *PM-7628 in Single Supply, Voltage-Switching Mode*

SINGLE SUPPLY, CURRENT SWITCHING

An alternate single-supply operating mode for the PM-7628 results when offsetting the analog ground. Figure 10 shows the circuit. The advantage of this configuration is the ability to set the output voltage level in the center of the supply voltage. This allows use of lower cost op amps that would not work in single-supply voltage-switching applications.

The transfer equation in this mode of operation is:

$$V_{OUT}(D) = D/256\ (AGND - V_{REF}) + AGND;$$

where D is the whole number binary input.

A popular connection in the current-steering single-supply mode consists of a 2.5 volt reference connected to AGND, the V_{REF} input grounded, V_{DD} connected to +12 volts, and the external (V+) op amp tied to +12 volts. This hookup results in the following transfer equation:

$$V_{OUT}(D) = 2.5\ (1 + D/256);$$

where $V_{OUT}(255) = 2.5\ (1 + 255/256) = 5V$
$V_{OUT}(0) = 2.5V.$

To maintain best linearity keep AGND equal to or less than 7 volts when V_{DD} is +12 volts.

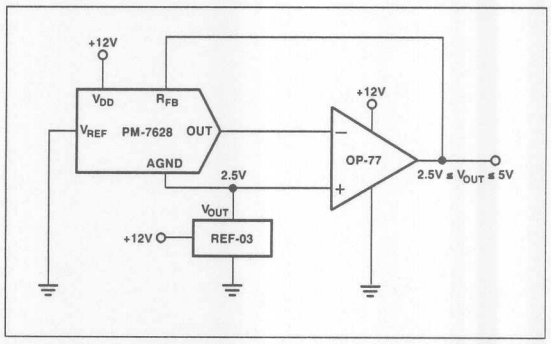


FIGURE 10: *PM-7628 in Single Supply, Current-Steering Mode*

SINGLE SUPPLY, CURRENT SWITCHING

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$V_{OUT}(0) = 2.5V.$

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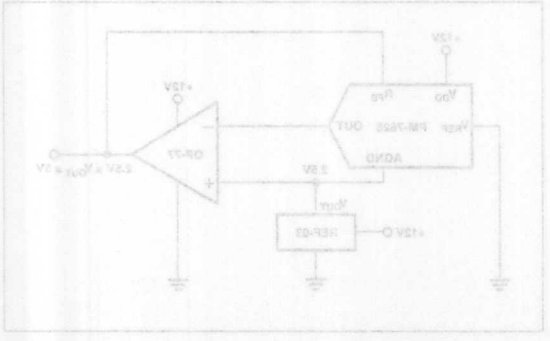


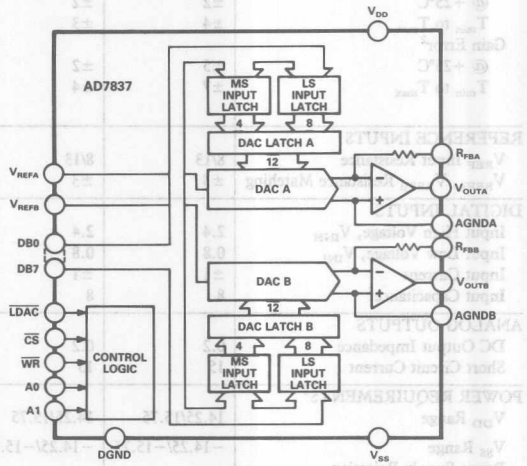
FIGURE 10: PM-7528 in Single Supply, Current-Steering Mode

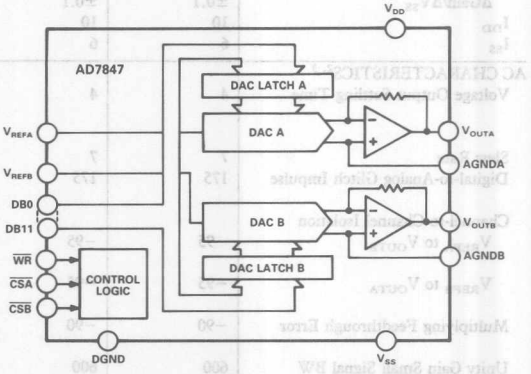
LC²MOS
Complete, Dual 12-Bit MDACs
AD7837/AD7847

FEATURES
- Two 12-Bit MDACS with Output Amplifiers
- 4-Quadrant Multiplication
- Space-Saving 0.3", 24-Pin DIP and 24-Terminal SOIC Package
- Parallel Loading Structure: AD7847
- (8 + 4) Loading Structure: AD7837

APPLICATIONS
- Automatic Test Equipment
- Function Generation
- Waveform Reconstruction
- Programmable Power Supplies
- Synchro Applications

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7837/AD7847 is a complete, dual, 12-bit multiplying digital-to-analog converter with output amplifiers on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7847 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7837 has a double-buffered 8-bit bus interface structure with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7837 updates the DAC latches and analog outputs.

The output amplifiers are capable of developing ±10 V across a 2 kΩ load. They are internally compensated with low input offset voltage due to laser trimming at wafer level.

The amplifier feedback resistors are internally connected to V_{OUT} on the AD7847.

The AD7837/AD7847 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

A novel low leakage configuration (U.S. Patent No. 4,590,456) ensures low offset errors over the specified temperature range.

PRODUCT HIGHLIGHTS

1. The AD7837/AD7847 is a dual, 12-bit, voltage-out MDAC on a single chip. This single chip design offers considerable space saving and increased reliability over multichip designs.
2. The AD7837 and the AD7847 provide a fast versatile interface to 8-bit or 16-bit data bus structures.

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	Guaranteed Monotonic
Zero Code Offset Error[2]					
@ +25°C	±2	±2	±2	mV max	DAC Latch Loaded with All 0s
T_{min} to T_{max}	±4	±3	±5	mV max	Temperature Coefficient = ±5 μV/°C typ
Gain Error[2]					
@ +25°C	±5	±2	±5	LSB max	DAC Latch Loaded with All 1s
T_{min} to T_{max}	±7	±4	±7	LSB max	Temperature Coefficient = ±2 ppm of FSR/°C typ
REFERENCE INPUTS					
V_{REF} Input Resistance	8/13	8/13	8/13	kΩ min/max	Typical Input Resistance = 10 kΩ
V_{REFA}, V_{REFB} Resistance Matching	±3	±3	±3	% max	Typically ±0.5%
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current	±1	±1	±1	μA max	Digital Inputs at 0 V and V_{DD}
Input Capacitance[3]	8	8	8	pF max	
ANALOG OUTPUTS					
DC Output Impedance	0.2	0.2	0.2	Ω typ	
Short Circuit Current	15	15	15	mA typ	V_{OUT} Connected to AGND
POWER REQUIREMENTS[4]					
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	V min/max	
V_{SS} Range	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	V min/max	
Power Supply Rejection					
$\Delta Gain/\Delta V_{DD}$	±0.1	±0.1	±0.1	%per %max	V_{DD} = 15 V ± 5%, V_{REF} = −10 V
$\Delta Gain/\Delta V_{SS}$	±0.1	±0.1	±0.1	%per %max	V_{SS} = −15 V ± 5%, V_{REF} = +10 V
I_{DD}	10	10	10	mA max	Output Unloaded. Typically 5 mA
I_{SS}	6	6	6	mA max	Output Unloaded. Typically 4 mA
AC CHARACTERISTICS[2, 3]					
Voltage Output Settling Time	4	4	4	μs typ	Settling Time to Within ±1/2 LSB of Final Value. DAC Latch Alternately Loaded with All 0s and All 1s
Slew Rate	7	7	7	V/μs typ	
Digital-to-Analog Glitch Impulse	175	175	175	nV secs typ	DAC Latch Alternately Loaded with 01 . . . 11 and 10 . . . 00
Channel-to-Channel Isolation					
V_{REFA} to V_{OUTB}	−95	−95	−95	dB typ	V_{REFA} = 20 V p–p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
V_{REFB} to V_{OUTA}	−95	−95	−95	dB typ	V_{REFB} = 20 V p–p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
Multiplying Feedthrough Error	−90	−90	−90	dB typ	V_{REF} = 20 V p–p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Unity Gain Small Signal BW	600	600	600	kHz typ	V_{REF} = 100 mV p–p Sine Wave. DAC Latch Loaded with All 1s
Full Power BW	110	110	90	kHz typ	V_{REF} = 20 V p–p Sine Wave. DAC Latch Loaded with All 1s
Total Harmonic Distortion	−88	−88	−88	dB typ	V_{REF} = 6 V rms, 1 kHz. DAC Latch Loaded with All 1s
Digital Crosstalk	10	10	10	nV secs typ	Code Transition from All 0s to All 1s
Output Noise Voltage @ +25°C					See Typical Performance Graphs
(0.1 Hz to 10 Hz)	2	2	2	μV rms typ	Amplifier Noise and Johnson Noise of R_{FB}

NOTES
[1]Temperature Ranges are as follows: A, B Versions, −40°C to +85°C; S Version, −55°C to +125°C.
[2]See Terminology.
[3]Sample tested @ +25°C to ensure compliance.
[4]The Devices are functional with V_{DD}/V_{SS} = ±12 V (See typical performance graphs.)
Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +15 V ± 5%, V_{SS} = −15 V ± 5%, AGNDA = AGNDB = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	80	100	ns min	$\overline{WR}$ Pulse Width
t_4	80	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[3]	15	15	ns min	Address to $\overline{WR}$ Setup Time
t_7[3]	15	15	ns min	Address to $\overline{WR}$ Hold Time
t_8[3]	80	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested @ +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 3 and 5.
[3]AD7837 only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND, AGNDA, AGNDB . . . . . −0.3 V to +17 V
V_{SS}[1] to DGND, AGNDA, AGNDB . . . . . +0.3 V to −17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
AGNDA, AGNDB to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{OUTA}[2], V_{OUTB}[2] to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
R_{FBA}[3], R_{FBB}[3] to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial/Industrial (A, B Versions) . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode connected between V_{SS} and AGND (cathode to AGND) ensures the Maximum Ratings will be observed.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
[3]AD7837 only.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7837AN	−40°C to +85°C	±1 LSB	N-24
AD7837BN	−40°C to +85°C	±1/2 LSB	N-24
AD7837AR	−40°C to +85°C	±1 LSB	R-24
AD7837BR	−40°C to +85°C	±1/2 LSB	R-24
AD7837AQ	−40°C to +85°C	±1 LSB	Q-24
AD7837BQ	−40°C to +85°C	±1/2 LSB	Q-24
AD7837SQ	−55°C to +125°C	±1 LSB	Q-24
AD7847AN	−40°C to +85°C	±1 LSB	N-24
AD7847BN	−40°C to +85°C	±1/2 LSB	N-24
AD7847AR	−40°C to +85°C	±1 LSB	R-24
AD7847BR	−40°C to +85°C	±1/2 LSB	R-24
AD7847AQ	−40°C to +85°C	±1 LSB	Q-24
AD7847BQ	−40°C to +85°C	±1/2 LSB	Q-24
AD7847SQ	−55°C to +125°C	±1 LSB	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TERMINOLOGY

Relative Accuray (Linearity)
Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Zero Code Offset Error
Zero code offset error is the error in output voltage from V_{OUTA} or V_{OUTB} with all 0s loaded into the DAC latches. It is due to a combination of the DAC leakage current and offset errors in the output amplifier.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded. It does not include offset error.

Total Harmonic Distortion
This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from the V_{REF} input to V_{OUT} of the same DAC when the DAC latch is loaded with all 0s.

Channel-to-Channel Isolation
This is an ac error due to capacitive feedthrough from the V_{REF} input on one DAC to V_{OUT} on the other DAC. It is measured with the DAC latches loaded with all 0s.

Digital Feedthrough
Digital feedthrough is the glitch impulse injected from the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

For the AD7837, it is measured with $\overline{LDAC}$ held high. For the AD7847, it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code on the DAC latch of the other converter. It is specified in nV secs.

Digital-to-Analog Glitch Impulse
This is the voltage spike that appears at the output of the DAC when the digital code changes, before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).

Unity Gain Small Signal Bandwidth
This is the frequency at which the small signal voltage output from the output amplifier is 3 dB below its dc level. It is measured with the DAC latch loaded with all 1s.

Full Power Bandwidth
This is the maximum frequency for which a sinusoidal input signal will produce full output at rated load with a distortion less than 3%. It is measured with the DAC latch loaded with all 1s.

AD7837 PIN FUNCTION DESCRIPTION (DIP & SOIC PIN NUMBERS)

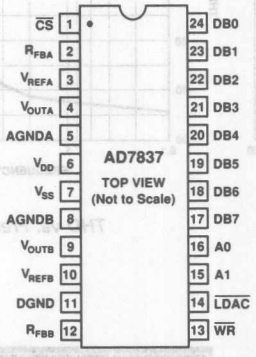
Pin	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
2	R_{FBA}	Amplifier Feedback Resistor for DAC A.
3	V_{REFA}	Reference Input Voltage for DAC A. This may be an ac or dc signal.
4	V_{OUTA}	Analog Output Voltage from DAC A.
5	AGNDA	Analog Ground for DAC A.
6	V_{DD}	Positive Power Supply.
7	V_{SS}	Negative Power Supply.
8	AGNDB	Analog Ground for DAC B.
9	V_{OUTB}	Analog Output Voltage from DAC B.
10	V_{REFB}	Reference Input Voltage for DAC B. This may be an ac or dc signal.
11	DGND	Digital Ground. Ground reference for digital circuitry.
12	R_{FBB}	Amplifier Feedback Resistor for DAC B.
13	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
14	$\overline{LDAC}$	DAC Update Logic Input. Data is transferred from the input latches to the DAC latches when $\overline{LDAC}$ is taken low.
15	A1	Address Input. Most significant address input for input latches (see Table II).
16	A0	Address Input. Least significant address input for input latches (see Table II).
17–20	DB7–DB4	Data Bit 7 to Data Bit 4.
21–24	DB3–DB0	Data Bit 3 to Data Bit 0 (LSB) or Data Bit 11 (MSB) to Data Bit 8.

AD7847 PIN FUNCTION DESCRIPTION (DIP & SOIC PIN NUMBERS)

Pin	Mnemonic	Description
1	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is low.
2	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is low.
3	V_{REFA}	Reference Input Voltage for DAC A. This may be an ac or dc signal.
4	V_{OUTA}	Analog Output Voltage from DAC A.
5	AGNDA	Analog Ground for DAC A.
6	V_{DD}	Positive Power Supply.
7	V_{SS}	Negative Power Supply.
8	AGNDB	Analog Ground for DAC B.
9	V_{OUTB}	Analog Output Voltage from DAC B.
10	V_{REFB}	Reference Input Voltage for DAC B. This may be an ac or dc signal.
11	DGND	Digital Ground.
12	DB11	Data Bit 11 (MSB).
13	$\overline{WR}$	Write Input. $\overline{WR}$ is a positive edge triggered input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
14-24	DB10–DB0	Data Bit 10 to Data Bit 0 (LSB).

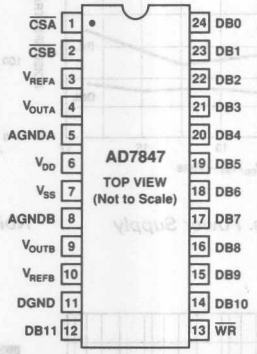
AD7837 PIN CONFIGURATION

DIP & SOIC

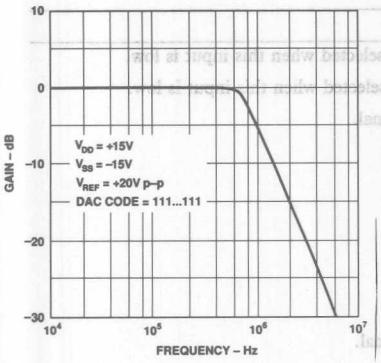


AD7847 PIN CONFIGURATION

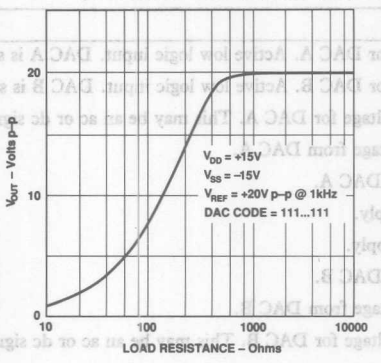
DIP & SOIC



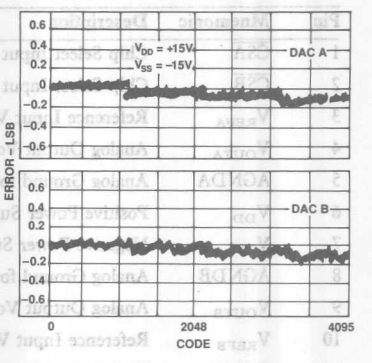
AD7837/AD7847—Typical Performance Graphs



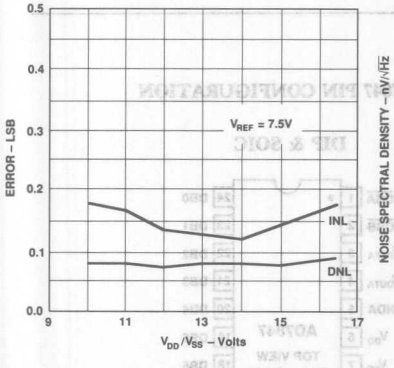
Frequency Response



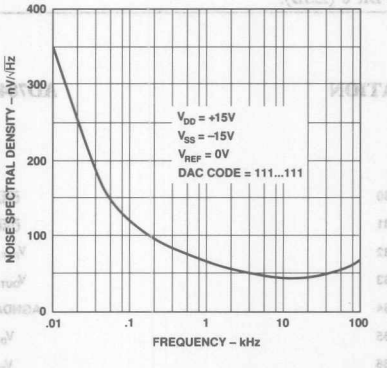
Output Voltage Swing vs. Resistive Load



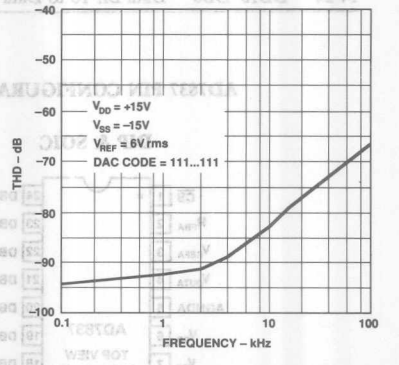
DAC to DAC Linearity Matching



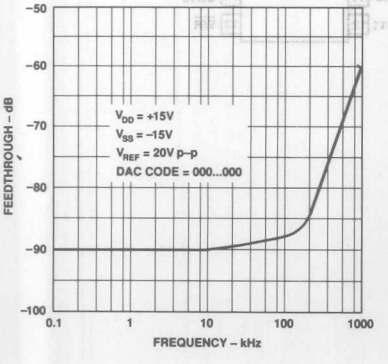
Linearity vs. Power Supply



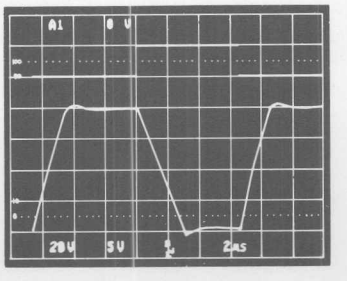
Noise Spectral Density vs. Frequency



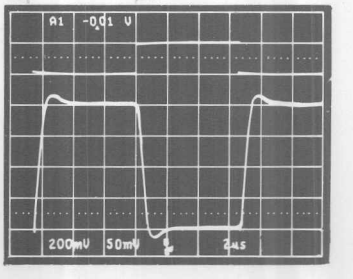
THD vs. Frequency



Multipling Feedthrough Error vs. Frequency



Large Signal Pulse Response



Small Signal Pulse Response

CIRCUIT INFORMATION

D/A Section

A simplified circuit diagram for one of the D/A converters and output amplifier is shown in Figure 1.

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A–C. The remaining 10 bits drive the switches (S0–S9) in a standard R-2R ladder configuration.

Each of the switches A–C steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

The output amplifier and feedback resistor perform the current to voltage conversion giving

$$V_{OUT} = -D \cdot V_{REF}$$

where D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

The output amplifier can maintain ±10 V across a 2 kΩ load. It is internally compensated and settles to 0.01% FSR (1/2 LSB) in less than 5 μs. Note that on the AD7837, V_{OUT} must be connected externally to R_{FB}.

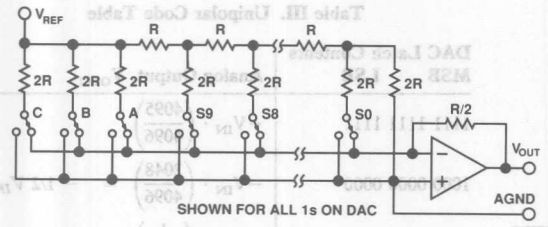


Figure 1. D/A Simplified Circuit Diagram

INTERFACE LOGIC INFORMATION – AD7847

The input control logic for the AD7847 is shown in Figure 2. The part contains a 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch, while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. The latches are edge triggered so that input data is latched to the respective latch on the rising edge of $\overline{WR}$. If $\overline{CSA}$ and $\overline{CSB}$ are both low and $\overline{WR}$ is taken high, the same data will be latched to both DAC latches. The control logic truth table is shown in Table I, while the write cycle timing diagram for the part is shown in Figure 3.

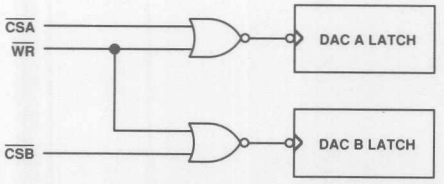


Figure 2. AD7847 Input Control Logic

Table I. AD7847 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	↓	Data Latched to DAC A
1	0	↓	Data Latched to DAC B
0	0	↓	Data Latched to Both DACs
↓	1	0	Data Latched to DAC A
1	↓	0	Data Latched to DAC B
↓	↓	0	Data Latched to Both DACs

X = Don't Care. ↓ = Rising Edge Triggered.

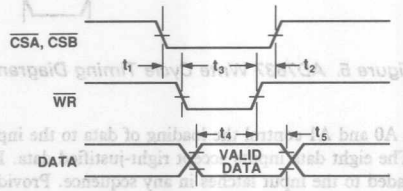


Figure 3. AD7847 Write Cycle Timing Diagram

INTERFACE LOGIC INFORMATION – AD7837

The input loading structure on the AD7837 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC – an input latch and a DAC latch. Each input latch is further subdivided into a least-significant 8-bit latch and a most-significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7837 is shown in Figure 4, while the write cycle timing diagram is shown in Figure 5.

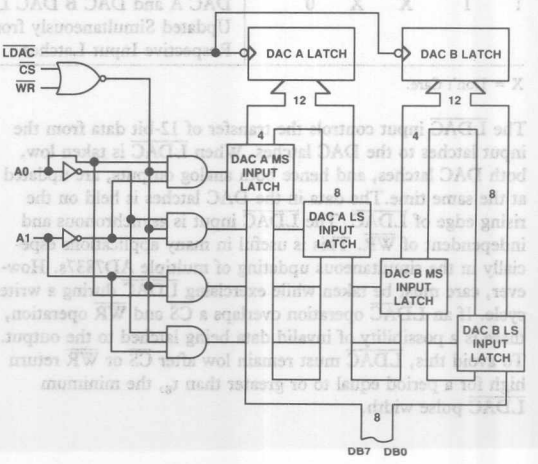


Figure 4. AD7837 Input Control Logic

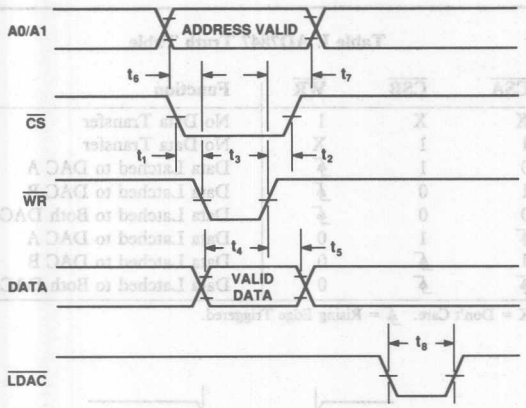


Figure 5. AD7837 Write Cycle Timing Diagram

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The control logic truth table for the part is shown in Table II.

Table II. AD7837 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DAC A and DAC B DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. When $\overline{LDAC}$ is taken low, both DAC latches, and hence both analog outputs, are updated at the same time.The data in the DAC latches is held on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7837s. However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

UNIPOLAR BINARY OPERATION

Figure 6 shows DAC A on the AD7837/AD7847 connected for unipolar binary operation. Similar connections apply for DAC B. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. The code table for this circuit is shown in Table III. Note that on the AD7847 the feedback resistor R_{FB} is internally connected to V_{OUT}.

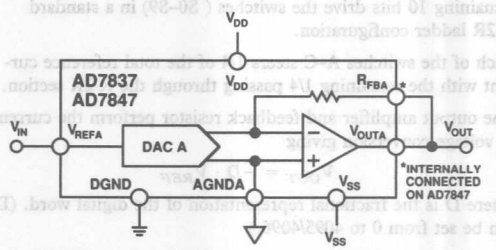


Figure 6. Unipolar Binary Operation

Table III. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

Note 1 LSB = $\frac{V_{IN}}{4096}$.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 shows the AD7837/AD7847 connected for bipolar operation. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R1, R2 and R3 should be ratio matched to 0.01%. Note that on the AD7847 the feedback resistor R_{FB} is internally connected to V_{OUT}.

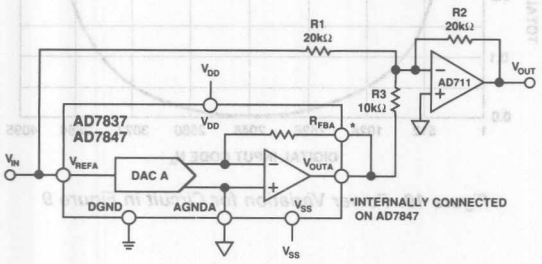


Figure 7. Bipolar Offset Binary Operation

Table IV. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN} \cdot \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{IN} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{2048}\right) = -V_{IN}$

Note 1 LSB = $\frac{V_{IN}}{2048}$.

APPLICATIONS

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The dual DAC/amplifier combination along with access to R_{FB} make the AD7837 ideal as a programmable gain amplifier. In this application, the DAC functions as a programmable resistor in the amplifier feedback loop. This type of configuration is shown in Figure 8 and is suitable for ac gain control. The circuit consists of two PGAs in series. Use of a dual configuration provides greater accuracy over a wider dynamic range than a single PGA solution. The overall system gain is the product of the individual gain stages. The effective gains for each stage are controlled by the DAC codes. As the code decreases, the effective DAC resistance increases, and so the gain also increases.

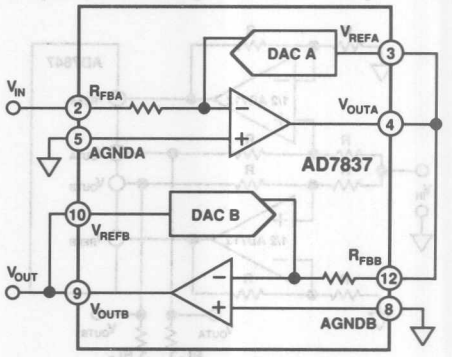


Figure 8. Dual PGA Circuit

The transfer function is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_{EQA}}{R_{FBA}} \cdot \frac{R_{EQB}}{R_{FBB}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where R_{EQA}, R_{EQB} are the effective DAC resistances controlled by the digital input code:

$$R_{EQ} = \frac{2^{12} R_{IN}}{N} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where R_{IN} is the DAC input resistance and is equal to R_{FB} and N= DAC input code in decimal.

The transfer function in (1) thus simplifies to

$$\frac{V_{OUT}}{V_{IN}} = \frac{2^{12}}{N_A} \cdot \frac{2^{12}}{N_B} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where N_A = DAC A input code in decimal

and N_B = DAC B input code in decimal.

N_A, N_B may be programmed between 1 and $(2^{12}-1)$. The zero code is not allowed as it results in an open loop amplifier response. To minimize errors, the digital codes N_A and N_B should be chosen to be equal to or as close as possible to each other to achieve the required gain.

ANALOG PANNING CIRCUIT

In audio applications it is often necessary to digitally "pan" or split a single signal source into a two-channel signal while maintaining the total power delivered to both channels constant. This may be done very simply by feeding the signal into the V_{REF} input of both DACs . The digital codes are chosen such that the code applied to DAC B is the 2s complement of that applied to DAC A. In this way the signal may be panned between both channels as the digital code is changed. The total power variation with this arrangement is 3 dB.

For applications which require more precise power control the circuit shown in Figure 9 may be used.This circuit requires the AD7837/AD7847, an AD712 dual op amp and 8 equal value resistors.

Again both channels are driven with 2s complementary data. The maximum power variation using this circuit is only 0.5 dBs.

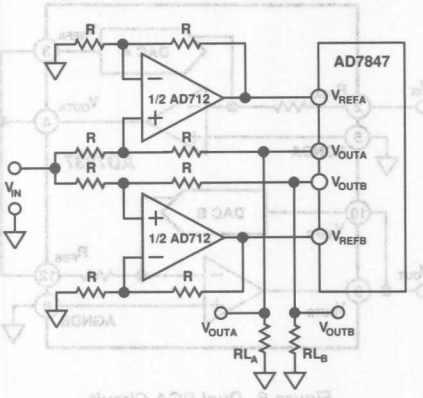


Figure 9. Analog Panning Circuit

The voltage output expressions for the two channels are as follows:

$$V_{OUTA} = -V_{IN}\left(\frac{N_A}{2^{12} + N_A}\right)$$

$$V_{OUTB} = -V_{IN}\left(\frac{N_B}{2^{12} + N_B}\right)$$

where N_A = DAC A input code in decimal ($1 \leq N_A \leq 4095$)

and N_B = DAC B input code in decimal ($1 \leq N_B \leq 4095$)

with N_B= 2s complement of N_A.

The 2s complement relationship between N_A and N_B causes N_B to increase as N_A decreases and vice versa.

Hence $N_A + N_B = 4096$.

With $N_A = 2048$, then $N_B = 2048$ also; this gives the balanced condition where the power is split equally between both channels. The total power variation as the signal is fully panned from channel B to channel A is shown in Figure 10.

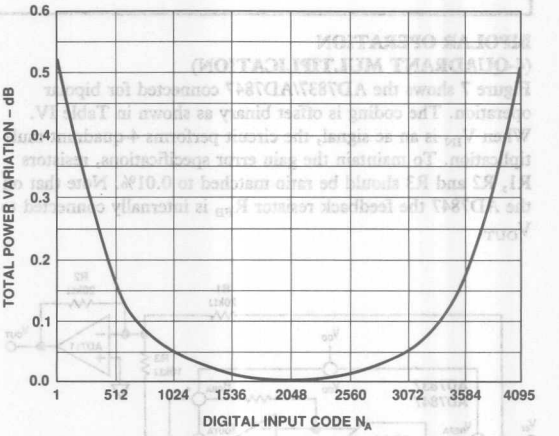


Figure 10. Power Variation for Circuit in Figure 9

APPLYING THE AD7837/AD7847

General Ground Management

AC or transient voltages between the analog and digital grounds i.e., between AGNDA/AGNDB and DGND can cause noise injection into the analog output. The best method of ensuring that both AGNDs and DGND are equal is to connect them together at the AD7837/AD7847 on the circuit board. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AGND and DGND pins (1N914 or equivalent).

Power Supply Decoupling

In order to minimize noise it is recommended that the V_{DD} and the V_{SS} lines on the AD7837/AD7847 be decoupled to DGND using a 10 μF in parallel with a 0.1 μF ceramic capacitor.

Operation with Reduced Power Supply Voltages

The AD7837/AD7847 is specified for operation with V_{DD}/V_{SS} = ±15 V ±5%. The part may be operated down to V_{DD}/V_{SS} = ±10 V without significant linearity degradation. See typical performance graphs. The output amplifier however requires approximately 3 V of headroom so the V_{REF} input should not approach within 3 V of either power supply voltages in order to maintain accuracy.

MICROPROCESSOR INTERFACING–AD7847

Figures 11 to 13 show interfaces between the AD7847 and three popular 16-bit microprocessor systems, the 8086, MC68000 and the TMS320C10. In all interfaces, the AD7847 is memory-mapped with a separate memory address for each DAC latch.

AD7847–8086 Interface

Figure 11 shows an interface between the AD7847 and the 8086 microprocessor. A single MOV instruction loads the 12-bit word into the selected DAC latch and the output responds on the rising edge of $\overline{WR}$.

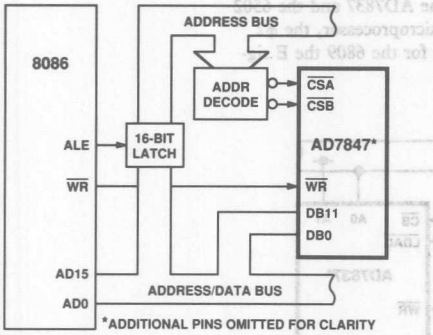


Figure 11. AD7847 to 8086 Interface

AD7847–MC68000 Interface

Figure 12 shows an interface between the AD7847 and the MC68000. Once again a single MOVE instruction loads the 12-bit word into the selected DAC latch. $\overline{CSA}$ and $\overline{CSB}$ are AND-gated to provide a $\overline{DTACK}$ signal when either DAC latch is selected.

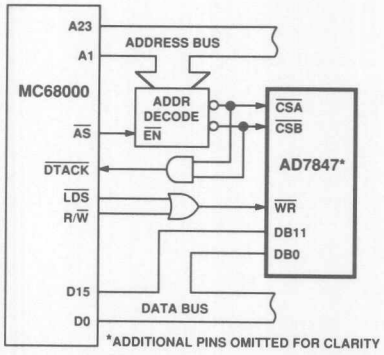


Figure 12. AD7847 to MC68000 Interface

AD7847–TMS320C10 Interface

Figure 13 shows an interface between the AD7847 and the TMS320C10 DSP processor. A single OUT instruction loads the 12-bit word into the selected DAC latch.

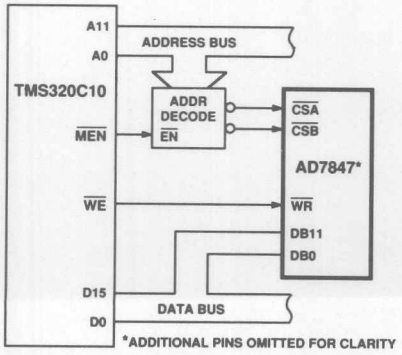


Figure 13. AD7847 to TMS320C10 Interface

MICROPROCESSOR INTERFACING–AD7837

Figures 14 to 16 show the AD7837 configured for interfacing to microprocessors with 8-bit data bus systems. In all cases, data is right-justified and the AD7837 is memory-mapped with the two lowest address lines of the microprocessor address bus driving the A0 and A1 inputs of the AD7837. Five separate memory addresses are required, one for the each MS latch and one for each LS latch and one for the common $\overline{LDAC}$ input. Data is written to the respective input latch in two write operations. Either high byte or low byte data can be be written first to the input latch. A write to the AD7837 $\overline{LDAC}$ address transfers the data from the input latches to the respective DAC latches and updates both analog outputs. Alternatively, the $\overline{LDAC}$ input can be asynchronous and can be common to a several AD7837s for simultaneous updating of a number of voltage channels.

AD7837–8051/8088 Interface

Figure 14 shows the connection diagram for interfacing the AD7837 to both the 8051 and the 8088. On the 8051, the signal $\overline{PSEN}$ is used to enable the address decoder while $\overline{DEN}$ is used on the 8088.

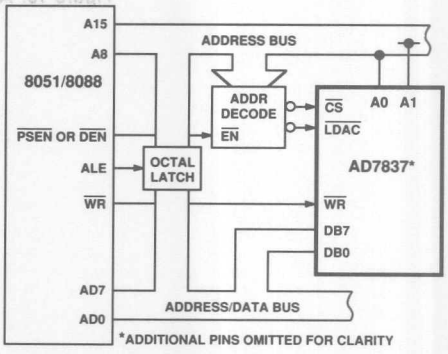


Figure 14. AD7837 to 8051/8088 Interface

AD7837–68008 Interface

An interface between the AD7837 and the MC68008 is shown in Figure 15. In the diagram shown, the $\overline{LDAC}$ signal is derived from an asynchronous timer but this can be derived from the address decoder as in the previous interface diagram.

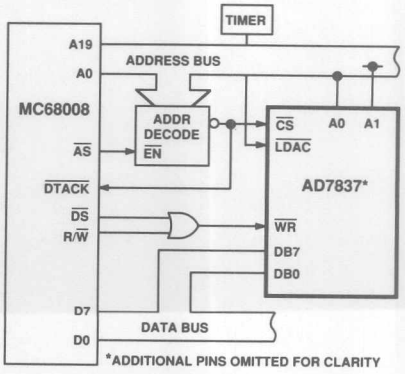


Figure 15. AD7837 to 68008 Interface

AD7837–6502/6809 Interface

Figure 16 shows an interface between the AD7837 and the 6502 or 6809 microprocessor. For the 6502 microprocessor, the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

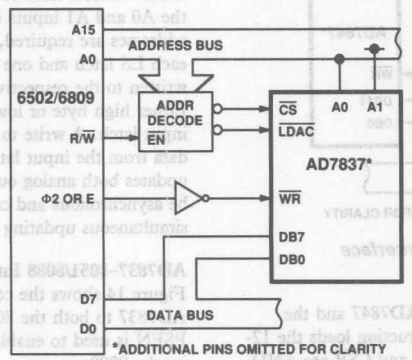


Figure 16. AD7837 to 6502/6809 Interface

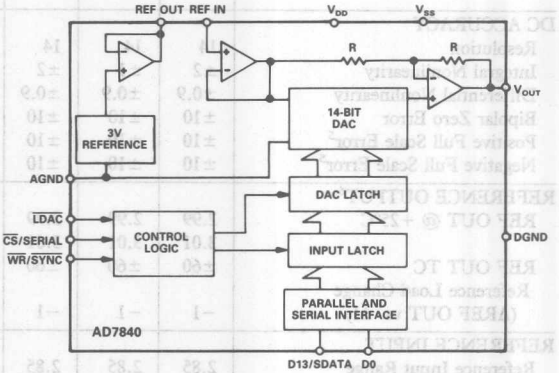
LC²MOS Complete 14-Bit DAC

AD7840

FEATURES

- Complete 14-Bit Voltage Output DAC
- Parallel and Serial Interface Capability
- 80dB Signal-to-Noise Ratio
- Interfaces to High Speed DSP Processors e.g., ADSP-2100, TMS32010, TMS32020
- 45ns min $\overline{WR}$ Pulse Width
- Low Power – 70mW typ.
- Operates from ±5V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3V buried Zener reference, DAC output amplifier and high speed control logic.

The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6MHz.

The analog output from the AD7840 provides a bipolar output range of ±3V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20kHz can be created.

The AD7840 is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 14-Bit D/A Function
   The AD7840 provides the complete function for creating ac signals and dc voltages to 14-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 14-bit D/A converter.
2. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7840 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Fast, Versatile Microprocessor Interface
   The AD7840 is capable of 14-bit parallel and serial interfacing. In the parallel mode, data setup times of 21ns and write pulse widths of 45ns make the AD7840 compatible with modern 16-bit microprocessors and digital signal processors. In the serial mode, the part features a high data transfer rate of 6MHz.

AD7840—SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V, REF IN = +3V, R_L = 2kΩ, C_L = 100pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	S[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR)	76	78	76	dB min	V_{OUT}=1kHz Sine Wave, f_{SAMPLE} =100kHz Typically 82dB at +25°C for 0 <V_{OUT}<20kHz[4]
Total Harmonic Distortion (THD)	−78	−80	−78	dB max	V_{OUT}=1kHz Sine Wave, f_{SAMPLE}= 100kHz Typically −84dB at +25°C for 0 <V_{OUT}<20kHz[4]
Peak Harmonic or Spurious Noise	−78	−80	−78	dB max	V_{OUT}=1kHz Sine Wave, f_{SAMPLE}=100kHz Typically −84dB at +25°C for 0 <V_{OUT}<20kHz[4]
DC ACCURACY					
Resolution	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT TC	±60	±60	±60	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0-500μA)
REFERENCE INPUT					
Reference Input Range	2.85	2.85	2.85	V min	3V ±5%
	3.15	3.15	3.15	V max	
Input Current	50	50	50	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD}=5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD}=5V ±5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0V to V_{DD}
Input Current ($\overline{CS}$ Input Only)	±10	±10	±10	μA max	V_{IN} =V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V Nom	
dc Output Impedance	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling Time					Settling Time to within ±1/2LSB of Final Value
Positive Full-Scale Change	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change	4	4	4	μs max	Typically 2.5μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	14	14	15	mA max	Output Unloaded, SCLK=+5V. Typically 10mA
I_{SS}	6	6	7	mA max	Output Unloaded, SCLK=+5V. Typically 4mA
Power Dissipation	100	100	110	mW max	Typically 70mW

NOTES

[1]Temperature ranges are as follows: J, K Versions, 0 to +70°C; A, B Versions, −25°C to +85°C; S Version, −55°C to +125°C.

[2]V_{OUT} (pk-pk)= ±3V.

[3]SNR calculation includes distortion and noise components.

[4]Using external sample-and-hold (see Testing the AD7840).

[5]Measured with respect to REF IN and includes bipolar offset error.

[6]For capacitive loads greater than 50pF, a series resistor is required (see Internal Reference section).

[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V.)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	45	50	ns min	$\overline{WR}$ Pulse Width
t_4	21	28	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width
t_7	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge
t_8[3]	150	200	ns min	SCLK Cycle Time
t_9	30	40	ns min	Data Valid to SCLK Setup Time
t_{10}	75	100	ns min	Data Valid to SCLK Hold Time
t_{11}	75	100	ns min	$\overline{SYNC}$ to SCLK Hold Time

NOTE
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
[2]See Figures 6 and 8.
[3]SCLK mark/space ratio is 40/60 to 60/40.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{SS} to AGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . 0V to V_{DD}
REF IN to AGND . . . . . −0.3V to V_{DD} +0.3V
Digital Inputs to DGND . . . . . −0.3V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1]	Temperature Range	SNR (dB)	Integral Nonlinearity (LSB)	Package Option[2]
AD7840JN	0 to +70°C	78 min	±2 max	N-24
AD7840KN	0 to +70°C	80 min	±1 max	N-24
AD7840JP	0 to +70°C	78 min	±2 max	P-28A
AD7840KP	0 to +70°C	80 min	±1 max	P-28A
AD7840AQ	−25°C to +85°C	78 min	±2 max	Q-24
AD7840BQ	−25°C to +85°C	80 min	±1 max	Q-24
AD7840SQ[3]	−55°C to +125°C	78 min	±2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$/SERIAL	Chip Select/Serial Input. When driven with normal logic levels, it is an active low logic input which is used in conjunction with $\overline{WR}$ to load parallel data to the input latch. For applications where $\overline{CS}$ is permanently low, an R, C is required for correct power-up (see $\overline{LDAC}$ input). If this input is tied to V_{SS}, it defines the AD7840 for serial mode operation.
2	$\overline{WR}$/$\overline{SYNC}$	Write/Frame Synchronization Input. In the parallel data mode, it is used in conjunction with $\overline{CS}$ to load parallel data. In the serial mode of operation, this pin functions as a Frame Synchronization pulse with serial data expected after the falling edge of this signal.
3	D13/SDATA	Data Bit 13(MSB)/Serial Data. When parallel data is selected, this pin is the D13 input. In serial mode, SDATA is the serial data input which is used in conjunction with $\overline{SYNC}$ and SCLK to transfer serial data to the AD7840 input latch.
4	D12/SCLK	Data Bit 12/Serial Clock. When parallel data is selected, this pin is the D12 input. In the serial mode, it is the serial clock input. Serial data bits are latched on the falling edge of SCLK when $\overline{SYNC}$ is low.
5	D11/FORMAT	Data Bit 11/Data Format. When parallel data is selected, this pin is the D11 input. In serial mode, a logic 1 on this input indicates that the MSB is the first valid bit in the serial data stream. A logic 0 indicates that the LSB is the first valid bit (see Table I).
6	D10/JUSTIFY	Data Bit 10/Data Justification. When parallel data is selected, this pin is the D10 input. In serial mode, this input controls the serial data justification (see Table I).
7–11	D9—D5	Data Bit 9 to Data Bit 5. Parallel data inputs.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	D4—D1	Data Bit 4 to Data Bit 1. Parallel data inputs.
17	D0	Data Bit 0 (LSB). Parallel data input.
18	V_{DD}	Positive Supply, +5V± 5%.
19	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
20	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3V with REF IN = +3V).
21	V_{SS}	Negative Supply Voltage, −5V ±5%.
22	REF OUT	Voltage Reference Output. The internal 3V analog reference is provided at this pin. To operate the AD7840 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500μA.
23	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7840 is 3V.
24	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal (see Interface Logic Information section). The AD7840 should be powered-up with $\overline{LDAC}$ high. For applications where $\overline{LDAC}$ is permanently low, an R, C is required for correct power-up (see Figure 19).

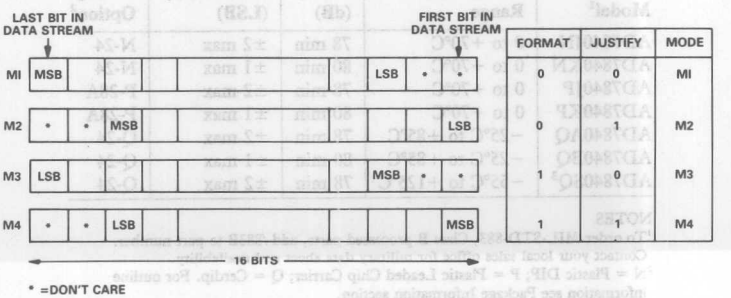


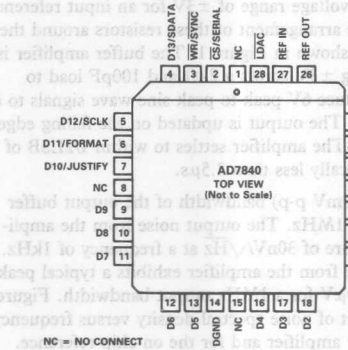
Table I. Serial Data Modes

PIN CONFIGURATIONS

DIP



PLCC



2

D/A SECTION

The AD7840 contains a 14-bit voltage mode D/A converter consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 1. The three MSBs of the data word are decoded to drive the seven switches A—G. The 11LSBs switch an 11-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3V reference and the device is tested with 3V applied to REF IN. Operating the AD7840 at reference voltages outside the ± 5% tolerance range may result in degraded performance from the part.

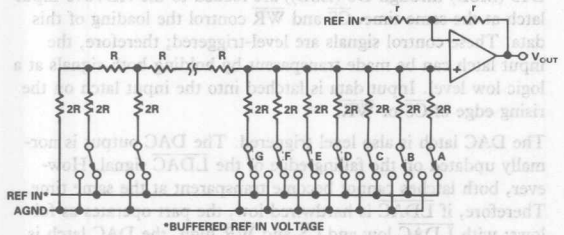


Figure 1. DAC Ladder Structure

INTERNAL REFERENCE

The AD7840 has an on-chip temperature compensated buried Zener reference (see Figure 2) which is factory trimmed to 3V ±10mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

The reference voltage can also be used as a reference for other components and is capable of providing up to 500μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50pF. If the reference is required for external use, it should be decoupled to AGND with a 200Ω resistor in series with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor.

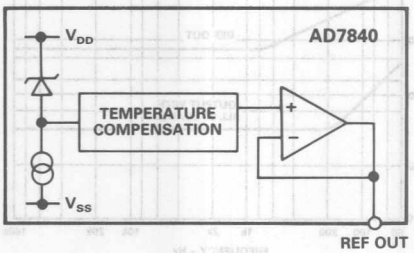


Figure 2. Internal Reference

EXTERNAL REFERENCE

In some applications, the user may require a system reference or some other external reference to drive the AD7840 reference input. Figure 3 shows how the AD586 5V reference can be conditioned to provide the 3V reference required by the AD7840 REF IN. An alternate source of reference voltage for the AD7840 in systems which use both a DAC and an ADC is to use the REF OUT voltage of ADCs such as the AD7870 and AD7871. A circuit showing this arrangement is shown in Figure 20.

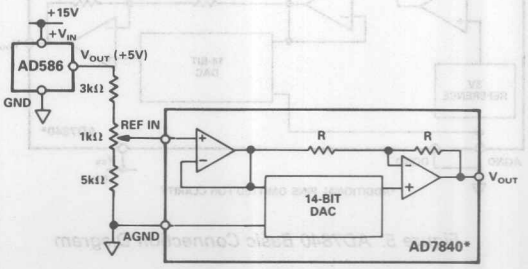


Figure 3. AD586 Driving AD7840 REF IN

OP AMP SECTION

The output from the voltage mode DAC is buffered by a non-inverting amplifier. Internal scaling resistors on the AD7840 configure an output voltage range of ±3V for an input reference voltage of +3V. The arrangement of these resistors around the output op amp is as shown in Figure 1. The buffer amplifier is capable of developing ±3V across a 2kΩ and 100pF load to ground and can produce 6V peak-to-peak sine wave signals to a frequency of 20kHz. The output is updated on the falling edge of the $\overline{\text{LDAC}}$ input. The amplifier settles to within 1/2LSB of its final value in typically less than 2.5μs.

The small signal (200mV p-p) bandwidth of the output buffer amplifier is typically 1MHz. The output noise from the amplifier is low with a figure of 30nV/$\sqrt{\text{Hz}}$ at a frequency of 1kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150μV for a 1MHz output bandwidth. Figure 4 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for the on-chip reference.

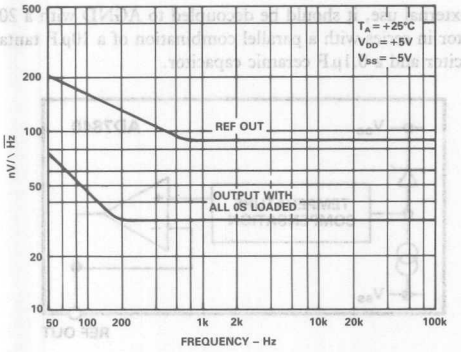


Figure 4. Noise Spectral Density vs. Frequency

TRANSFER FUNCTION

The basic circuit configuration for the AD7840 is shown in Figure 5. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1LSB = FS/16,384 = 6V/16,384 = 366μV.

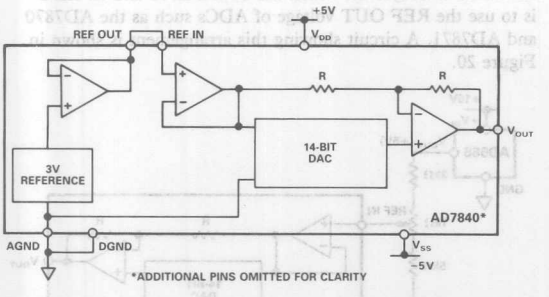


Figure 5. AD7840 Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+2.999634V
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	+2.999268V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+0.000366V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0V
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	−0.000366V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	−2.999634V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	−3V

*Assuming REF IN = +3V.

Table II. Ideal Input/Output Code Table

The output voltage can be expressed in terms of the input code, N, using the following expression:

$$V_{OUT} = \frac{2 \times N \times REFIN}{16384} \quad -8192 \leq N \leq +8191$$

INTERFACE LOGIC INFORMATION

The AD7840 contains two 14-bit latches, an input latch and a DAC latch. Data can be loaded to the input latch in one of two basic interface formats. The first is a parallel 14-bit wide data word; the second is a serial interface where 16 bits of data are serially clocked into the input latch. In the parallel mode, $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of data. When the serial data format is selected, data is loaded using the SCLK, $\overline{\text{SYNC}}$ and SDATA serial inputs. Data is transferred from the input latch to the DAC latch under control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7840.

Parallel Data Format

Table III shows the truth table for AD7840 parallel mode operation. The AD7840 normally operates with a parallel input data format. In this case, all 14 bits of data (appearing on data inputs D13 (MSB) through D0 (LSB)) are loaded to the AD7840 input latch at the same time. $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of this data. These control signals are level-triggered; therefore, the input latch can be made transparent by holding both signals at a logic low level. Input data is latched into the input latch on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{WR}}$.

The DAC latch is also level triggered. The DAC output is normally updated on the falling edge of the $\overline{\text{LDAC}}$ signal. However, both latches cannot become transparent at the same time. Therefore, if $\overline{\text{LDAC}}$ is hardwired low, the part operates as follows; with $\overline{\text{LDAC}}$ low and $\overline{\text{CS}}$ and $\overline{\text{WR}}$ high, the DAC latch is transparent. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ go low (with $\overline{\text{LDAC}}$ still low), the input latch becomes transparent but the DAC latch is disabled. When $\overline{\text{CS}}$ or $\overline{\text{WR}}$ return high, the input latch is locked out and the DAC latch becomes transparent again and the DAC output is updated. The write cycle timing diagram for parallel data is shown in Figure 6. Figure 7 shows the simplified parallel input control logic for the AD7840.

$\overline{CS}$	$\overline{WR}$	$\overline{LDAC}$	Function
H	X	H	Both Latches Latched
X	H	H	
L	L	H	Input Latch Transparent
H	H	L	Input Latch Latched
H	X	L	DAC Latch Transparent
X	H	L	Analog Output Updated
↓	↓	L	Input Latch Transparent DAC Latch Data Transfer Inhibited
L	↑	L	Input Latch Is Latched
↑	L	L	DAC Latch Data Transfer Occurs

X = Don't Care

Table III. Parallel Mode Truth Table

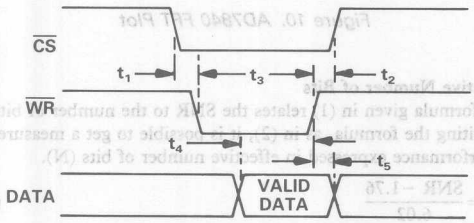


Figure 6. Parallel Mode Timing Diagram

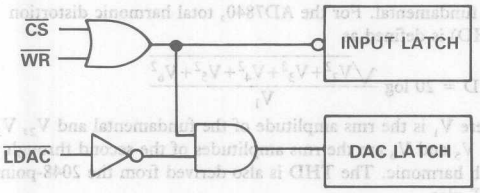


Figure 7. AD7840 Simplified Parallel Input Control Logic

Serial Data Format

The serial data format is selected for the AD7840 by connecting the $\overline{CS}$/SERIAL line to −5V. In this case, the $\overline{WR}$/SYNC, D13/SDATA, D12/SCLK, D11/FORMAT and D10/JUSTIFY pins all assume their serial functions. The unused parallel inputs should not be left unconnected to avoid noise pickup. Serial data is loaded to the input latch under control of SCLK, $\overline{SYNC}$ and SDATA. The AD7840 expects a 16-bit stream of serial data on its SDATA input. Serial data must be valid on the falling edge of SCLK. The $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7840 that valid serial data will be available for the next 16 falling edges of SCLK. Figure 8 shows the timing diagram for serial data format.

Although 16 bits of data are clocked into the AD7840, only 14 bits go into the input latch. Therefore, two bits in the stream are don't cares since their value does not affect the input latch data. The order and position in which the AD7840 accepts the 14 bits of input data depends upon the FORMAT and JUSTIFY inputs. There are four different input data modes which can be chosen (see Table I in the Pin Function Description section).

The first mode (M1) assumes that the first two bits of the input data stream are don't cares, the third bit is the LSB and the last (or 16th bit) is the MSB. This mode is chosen by tying both the FORMAT and JUSTIFY pins to a logic 0. The second mode (M2; FORMAT = 0, JUSTIFY = 1) assumes that the first bit in the data stream is the LSB, the fourteenth bit is the MSB and the last two bits are don't cares. The third mode (M3; FORMAT = 1, JUSTIFY = 0) assumes that the first two bits in the stream are again don't cares, the third bit is now the MSB and the sixteenth bit is the LSB. The final mode (M4; FORMAT = 1, JUSTIFY = 1) assumes that the first bit is the MSB, the fourteenth bit is the LSB and the last two bits of the stream are don't cares.

As in the parallel mode, the $\overline{LDAC}$ signal controls the loading of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{LDAC}$. However, if $\overline{LDAC}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of SCLK. If $\overline{LDAC}$ goes low during the transfer of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{LDAC}$. If $\overline{LDAC}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of SCLK. If $\overline{LDAC}$ returns high before the serial data transfer is completed, no DAC latch update takes place. Figure 9 shows the simplified serial input control logic for the AD7840.

2

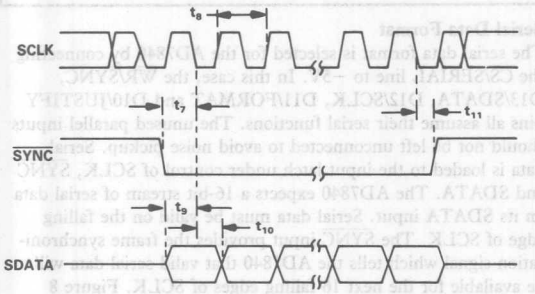


Figure 8. Serial Mode Timing Diagram

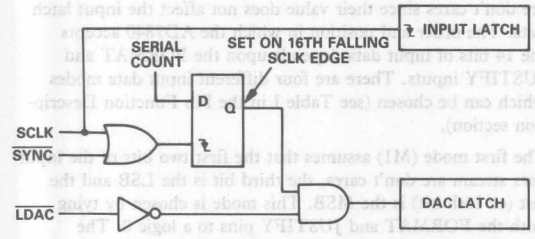


Figure 9. AD7840 Simplified Serial Input Control Logic

AD7840 DYNAMIC SPECIFICATIONS

The AD7840 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as speech synthesis, servo control and high speed modems. These applications require information on the DAC's effect on the spectral content of the signal it is creating. Hence, the parameters for which the AD7840 is specified include signal-to-noise ratio, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave output is given by

$$SNR = (6.02N + 1.76)dB \quad (1)$$

where N is the number of bits. Thus for an ideal 14-bit converter, SNR = 86dB.

Figure 10 shows a typical 2048 point Fast Fourier Transform (FFT) plot of the AD7840KN with an output frequency of 1kHz and an update rate of 100kHz. The SNR obtained from this graph is 81.8dB. It should be noted that the harmonics are taken into account when calculating the SNR.

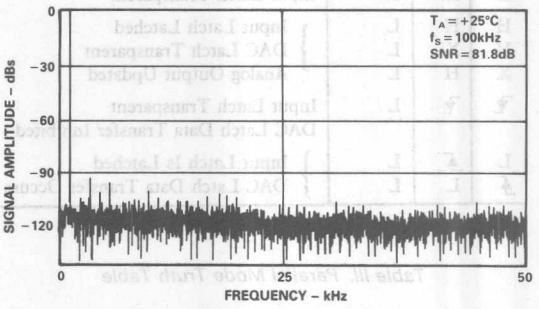


Figure 10. AD7840 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7840, total harmonic distortion (THD) is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2+V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the 2048-point FFT plot.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the DAC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

Testing the AD7840

A simplified diagram of the method used to test the dynamic performance specifications is outlined in Figure 11. Data is loaded to the AD7840 under control of the microcontroller and associated logic at a 100kHz update rate. The output of the AD7840 is applied to a ninth order, 50kHz, low-pass filter. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7840 can be evaluated.

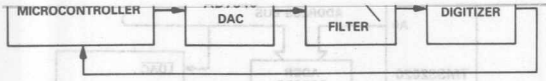


Figure 11. AD7840 Dynamic Performance Test Circuit

The digitizer sampling is synchronized with the AD7840 update rate to ease FFT calculations. The digitizer samples the AD7840 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7840 would not be measured correctly. Using the digitizer directly on the AD7840 output would give better results than the actual performance of the AD7840. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7840 is measured.

Some applications will require improved performance versus frequency from the AD7840. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 12 will extend the very good performance of the AD7840 to 20kHz.

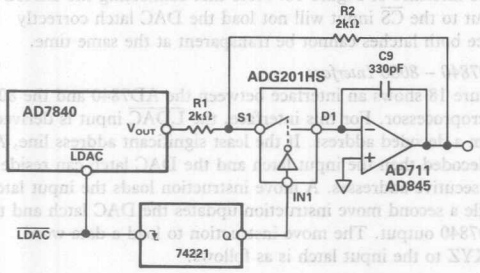


Figure 12. Sample-and-Hold Circuit

Other applications will already have an inherent sample-and-hold function following the AD7840. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance of the AD7840.

AD7840's performance over a wide range of input frequencies at an update rate of 100kHz. The plot of Figure 13 is without a sample-and-hold on the AD7840 output while the plot of Figure 14 is generated with the sample-and-hold circuit of Figure 12 on the output.

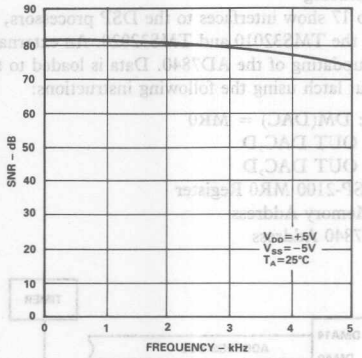


Figure 13. Performance vs. Frequency (No Sample-and-Hold)

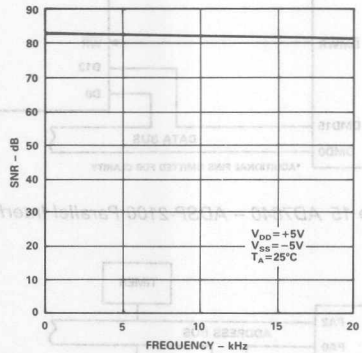


Figure 14. Performance vs. Frequency (with Sample-and-Hold)

MICROPROCESSOR INTERFACING

The AD7840 logic architecture allows two interfacing options for interfacing the part to microprocessor systems. It offers a 14-bit wide parallel format and a serial format. Fast pulse widths and data setup times allow the AD7840 to interface directly to most microprocessors including the DSP processors. Suitable interfaces to various microprocessors are shown in Figures 15 to 23.

Parallel Interfacing

Figures 15 to 17 show interfaces to the DSP processors, the ADSP-2100, the TMS32010 and TMS32020. An external timer controls the updating of the AD7840. Data is loaded to the AD7840 input latch using the following instructions:

ADSP-2100 : DM(DAC) = MR0
TMS32010 : OUT DAC,D
TMS32020 : OUT DAC,D
MR0 = ADSP-2100 MR0 Register
D = Data Memory Address
DAC = AD7840 Address

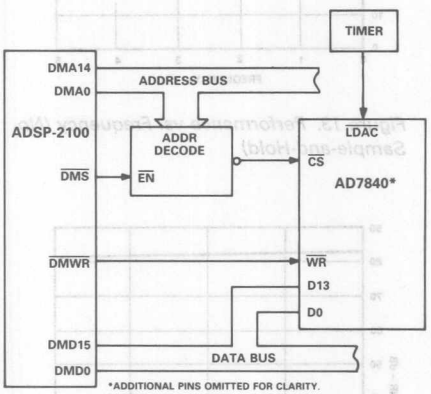


Figure 15 AD7840 – ADSP-2100 Parallel Interface

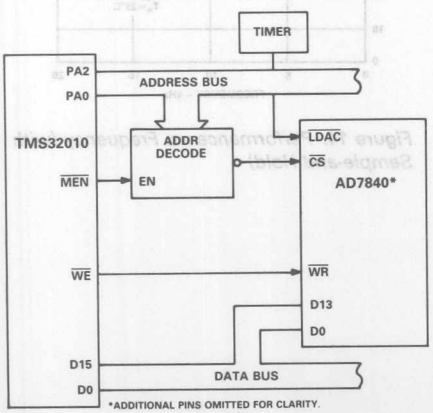


Figure 16. AD7840 – TM32010 Parallel Interface

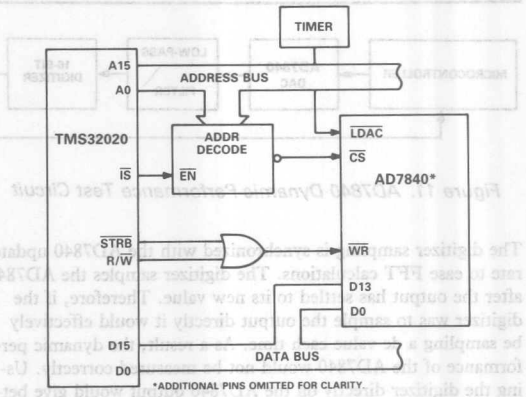


Figure 17. AD7840 – TMS32020 Parallel Interface

Some applications may require that the updating of the AD7840 DAC latch be controlled by the microprocessor rather than the external timer. One option (for double-buffered interfacing) is to decode the AD7840 $\overline{LDAC}$ from the address bus so that a write operation to the DAC latch (at a separate address than the input latch) updates the output. An example of this is shown in the 8086 interface of Figure 18. Note that connecting the $\overline{LDAC}$ input to the $\overline{CS}$ input will not load the DAC latch correctly since both latches cannot be transparent at the same time.

AD7840 – 8086 Interface

Figure 18 shows an interface between the AD7840 and the 8086 microprocessor. For this interface, the $\overline{LDAC}$ input is derived from a decoded address. If the least significant address line, A0, is decoded then the input latch and the DAC latch can reside at consecutive addresses. A move instruction loads the input latch while a second move instruction updates the DAC latch and the AD7840 output. The move instruction to load a data word WXYZ to the input latch is as follows:

MOV DAC,#YZWX
DAC = AD7840 Address

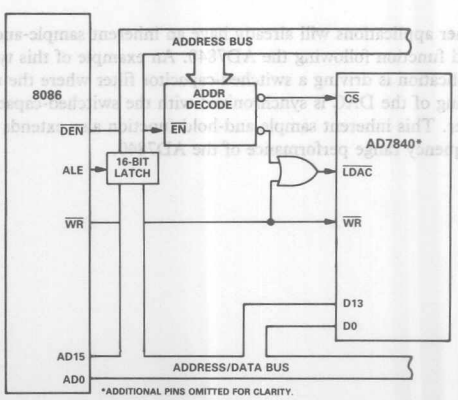


Figure 18. AD7840 – 8086 Parallel Interface

AD7840 – 68000 Interface

An interface between the AD7840 and the 68000 microprocessor is shown in Figure 19. In this interface example, the $\overline{LDAC}$ input is hardwired low. As a result the DAC latch and analog output are updated on the rising edge of $\overline{WR}$. A single move instruction, therefore, loads the input latch and updates the output.

MOVE.W D0,$DAC
D0 = 68000 D0 Register
DAC = AD7840 Address

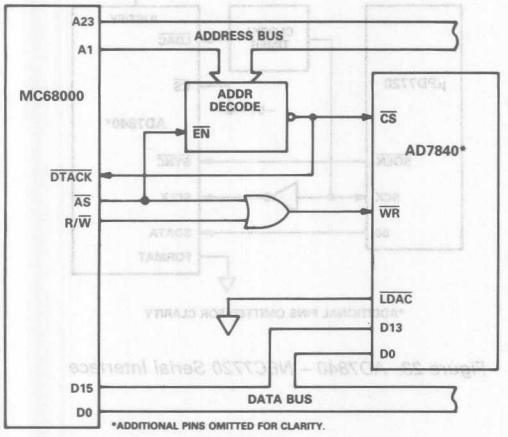


Figure 19. AD7840 – MC68000 Parallel Interface

Serial Interfacing

Figures 20 to 23 show the AD7840 configured for serial interfacing with the $\overline{CS}$ input hardwired to −5V. The parallel bus is not activated during serial communication with the AD7840.

AD7840 – ADSP-2101/ADSP-2102 Serial Interface

Figure 20 shows a serial interface between the AD7840 and the ADSP-2101/ADSP-2102 DSP processor. Also included in the interface is the AD7870, a 12-bit A/D converter. An interface such as this is suitable for modem and other applications which have a DAC and an ADC in serial communication with a microprocessor.

The interface uses just one of the two serial ports of the ADSP-2101/ADSP-2102. Conversion is initiated on the AD7870 at a fixed sample rate (e.g., 9.6kHz) which is provided by a timer or clock recovery circuitry. While communication takes place between the ADC and the ADSP-2101/ADSP-2102, the AD7870 $\overline{SSTRB}$ line is low. This $\overline{SSTRB}$ line is used to provide a frame synchronization pulse for the AD7840 $\overline{SYNC}$ and ADSP-2101/ADSP-2102 TFS lines. This means that communication between the processor and the AD7840 can only take place while the AD7870 is communicating with the processor. This arrangement is desirable in systems such as modems where the DAC and ADC communication should be synchronous.

The use of the AD7870 SCLK for the AD7840 SCLK and ADSP-2101/ADSP-2102 SCLK means that only one serial port of the processor is used. The serial clock for the AD7870 must be set for continuous clock for correct operation of this interface.

Data from the ADSP-2101/ADSP-2102 is valid on the falling edge of SCLK. The $\overline{LDAC}$ input of the AD7840 is permanently low so the update of the DAC latch and analog output takes place on the sixteenth falling edge of SCLK (with $\overline{SYNC}$ low). The FORMAT pin of the AD7840 must be tied to +5V and the JUSTIFY pin tied to DGND for this interface to operate correctly.

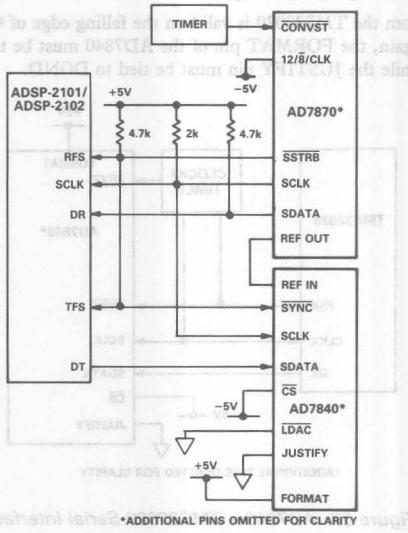


Figure 20. Complete DAC/ADC Serial Interface

AD7840 – DSP56000 Serial Interface

A serial interface between the AD7840 and the DSP56000 is shown in Figure 21. The DSP56000 is configured for normal mode synchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to the AD7840 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{SYNC}$ input of the AD7840.

The $\overline{LDAC}$ input of the AD7840 is connected to DGND so the update of the DAC latch takes place on the sixteenth falling edge of SCLK. As with the previous interface, the FORMAT pin of the AD7840 must be tied to +5V and the JUSTIFY pin tied to DGND.

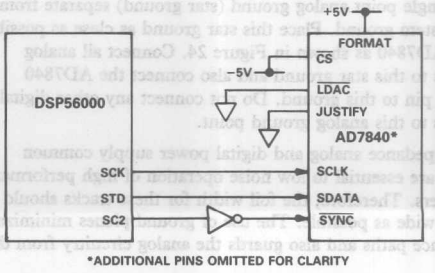


Figure 21. AD7840 – DSP56000 Serial Interface

AD7840 – TMS32020 Serial Interface

Figure 22 shows a serial interface between the AD7840 and the TMS32020 DSP processor. In this interface, the CLKX and FSX pin of the TMS32020 are generated from the clock/timer circuitry. The same clock/timer circuitry generates the $\overline{LDAC}$ signal of the AD7840 to synchronize the update of the output with the serial transmission. The FSX pin of the TMS32020 must be configured as an input.

Data from the TMS32020 is valid on the falling edge of CLKX. Once again, the FORMAT pin of the AD7840 must be tied to +5V while the JUSTIFY pin must be tied to DGND.

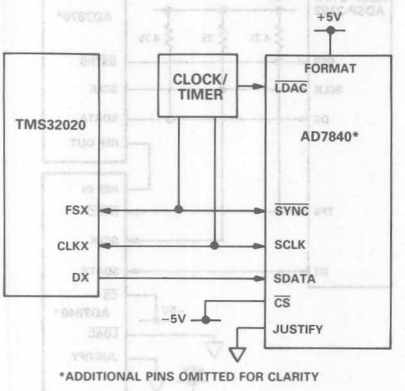


Figure 22. AD7840 – TMS32020 Serial Interface

AD7840 – NEC7720 Serial Interface

A serial interface between the AD7840 and the NEC7720 is shown in Figure 23. The serial clock must be inverted before being applied to the AD7840 SCLK input because data from the processor is valid on the rising edge of SCK.

The NEC7720 is programmed for the LSB to be the first bit in the serial data stream. Therefore, the AD7840 is set up with the FORMAT pin tied to DGND and the JUSTIFY pin tied to +5V.

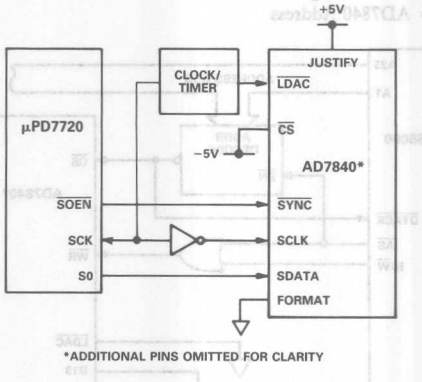


Figure 23. AD7840 – NEC7720 Serial Interface

APPLYING THE AD7840

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7840 works on an LSB size of 366μV. Therefore, the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feed through to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7840 as shown in Figure 24. Connect all analog grounds to this star ground and also connect the AD7840 DGND pin to this ground. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layouts of Figures 27 and 28 have both analog and digital ground planes which are kept separated and only joined at the star ground close to the AD7840.

NOISE

Keep the signal leads on the V_{OUT} signal and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC output and its destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

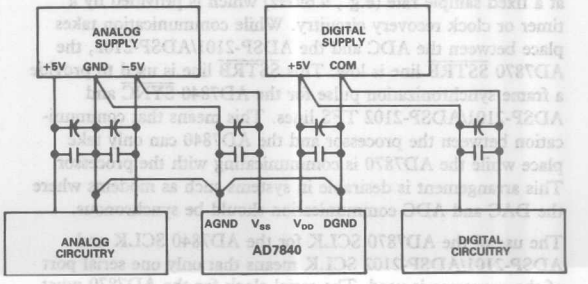


Figure 24. Power Supply Grounding Practice

DATA ACQUISITION BOARD

Figure 25 shows the AD7840 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 26 to 28. The board layout has three interface ports: one serial and two parallel. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

Some systems will require the addition of a re-construction filter on the output of the AD7840 to complete the data acquisition system. There is a component grid provided near the analog output on the PCB which may be used for such a filter or any other output conditioning circuitry. To facilitate this option, there is a shorting plug (labeled LK1 on the PCB) on the analog output track. If this shorting plug is used, the analog output connects to the output of the AD7840; otherwise this shorting plug can be omitted and a wire link used to connect the analog output to the PCB component grid.

The board also contains a simple sample-and-hold circuit which can be used on the output of the AD7840 to extend the very good performance of the AD7840 over a wider frequency range. A second wire link (labelled LK2 on the PCB) connects V_{OUT} (SKT1) to either the output of this sample-and-hold circuit or directly to the output of the AD7840.

INTERFACE CONNECTIONS

There are two parallel connectors, labeled SKT4 and SKT6, and one serial connector, labeled SKT5. A shorting plug option (LK8 in Figure 25) on the AD7840 $\overline{CS}$/SERIAL input configures the DAC for the appropriate interface (see Pin Function Description).

SKT6 is a 96-contact (3-row) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to drive the AD7840 $\overline{CS}$ input on the data acquisition board. To avoid selecting on-board sockets at the same time, LK6 on the ADSP-2100 board must be removed. The AD7840 and ADSP-2100 data lines are aligned for left justified data transfer.

SKT4 is a 26-way (2-row) IDC connector. This connector contains the same signal contacts as SKT6 and in addition contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing. This decoded $\overline{WR}$ can be selected via LK4. The pinout for this connector is shown in Figure 29.

SKT5 is a nine-way D-type connector which is meant for serial interfacing only. The evaluation board has the facility to invert $\overline{SYNC}$ line via LK7. This is necessary for serial interfacing between the AD7840 and DSP processors such as the DSP56000. The SKT5 pinout is shown in Figure 30.

SKT1, SKT2 and SKT3 are three BNC connectors which provide connections for the analog output, the $\overline{LDAC}$ input and an external reference input. The use of an external reference is optional; the shorting plug (LK3) connects the REF IN pin to either this external reference or to the AD7840's own internal reference.

Wire links LK5 and LK6 connect the D11 and D10 inputs to the data lines for parallel operation. In the serial mode, these links allow the user to select the required format and justification for serial data (see Table I).

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silkscreen in Figure 26. The connections are labelled V+ and V− and the range for both of these supplies is 12V to 15V. Connection to the 5V digital supply is made through any of the connectors (SKT4 to SKT6). The −5V analog supply required by the AD7840 is generated from a voltage regulator on the V− power supply input (IC5 in Figure 25).

SHORTING PLUG OPTIONS

There are eight shorting plug options which must be set before using the board. These are outlined below:

LK1	Connects the analog output to SKT1. The analog output may also be connected to a component grid for signal conditioning.
LK2	Selects either the AD7840 V_{OUT} or the sample-and-hold output.
LK3	Selects either the internal or external reference.
LK4	Selects the decoded R/$\overline{W}$ and $\overline{STRB}$ inputs for TMS32020 interfacing.
LK5	Configures the D11/FORMAT input.
LK6	Configures the D10/JUSTIFY input.
LK7	Selects either the inverted or noninverted $\overline{SYNC}$.
LK8	Selects either parallel or serial interfacing.

COMPONENT LIST

IC1	AD7840 Digital-to-Analog Converter
IC2	AD711 Op Amp
IC3	ADG201HS High Speed Switch
IC4	74HC221 Monostable
IC5	79L05 Voltage Regulator
IC6	74HC02
C1, C3, C5, C7, C11, C13, C15, C17	10μF Capacitors
C2, C4, C6, C8, C12, C14, C16, C18	0.1μF Capacitors
C9	330pF Capacitor
C10	68pF Capacitor
R1, R2	2.2kΩ Resistors
R3	15kΩ Resistor
RP1, RP2	100kΩ Resistor Packs
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8	Shorting Plugs
SKT1, SKT2, SKT3	BNC Sockets
SKT4	26-Contact (2-Row) IDC Connector
SKT5	9-Contact D-Type Connector
SKT6	96-Contact (3-Row) Eurocard Connector

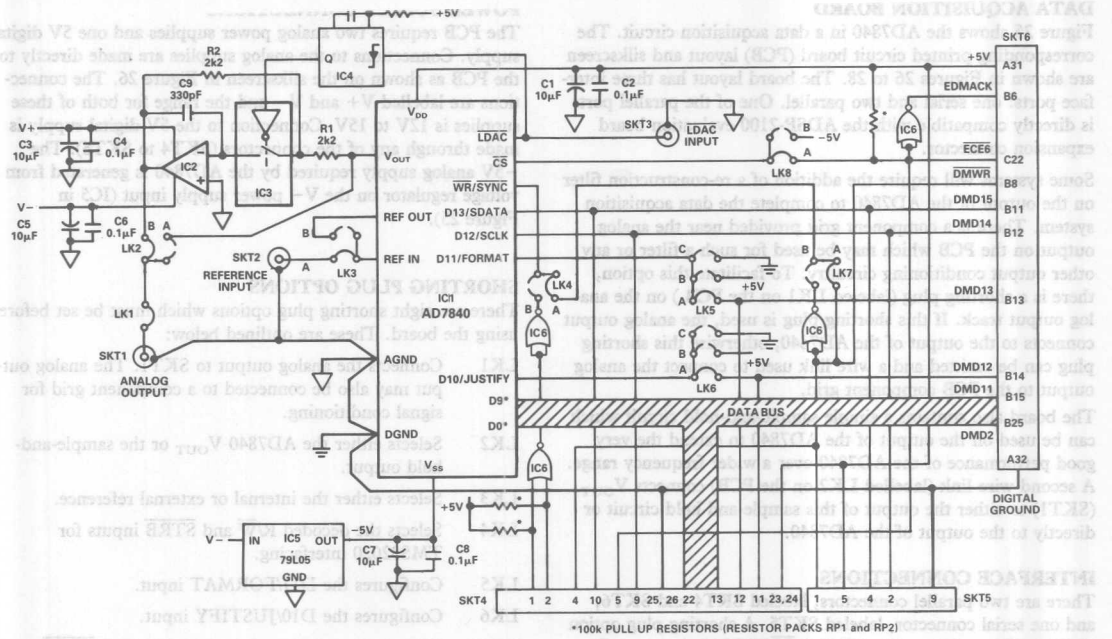
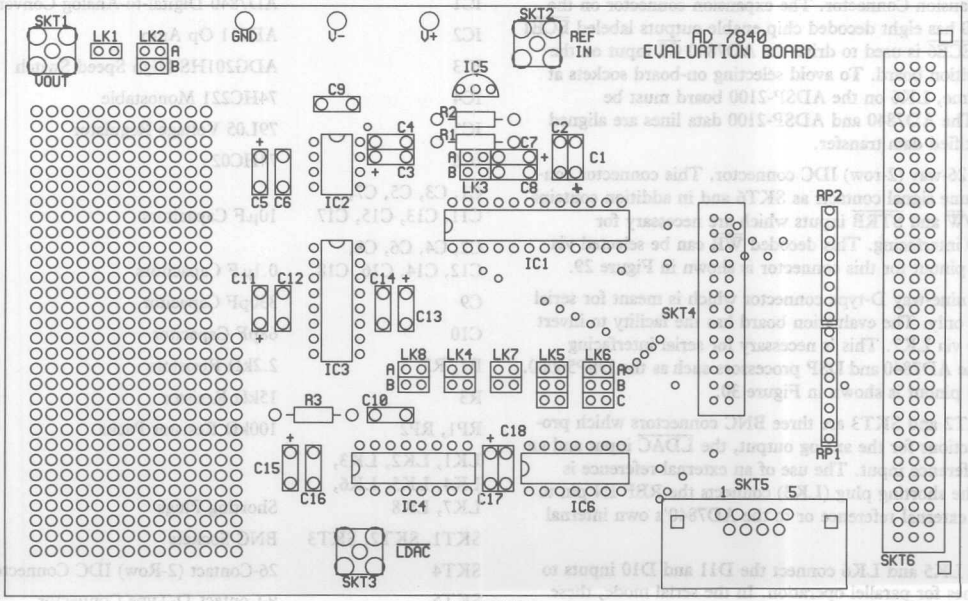
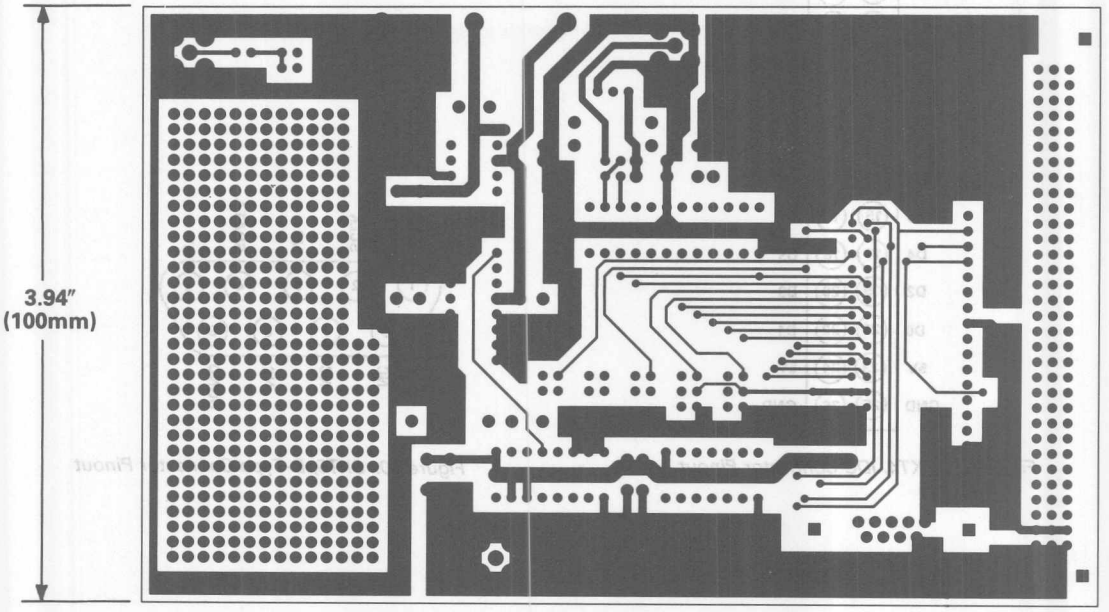


Figure 25. Data Acquisition Circuit Using the AD7840



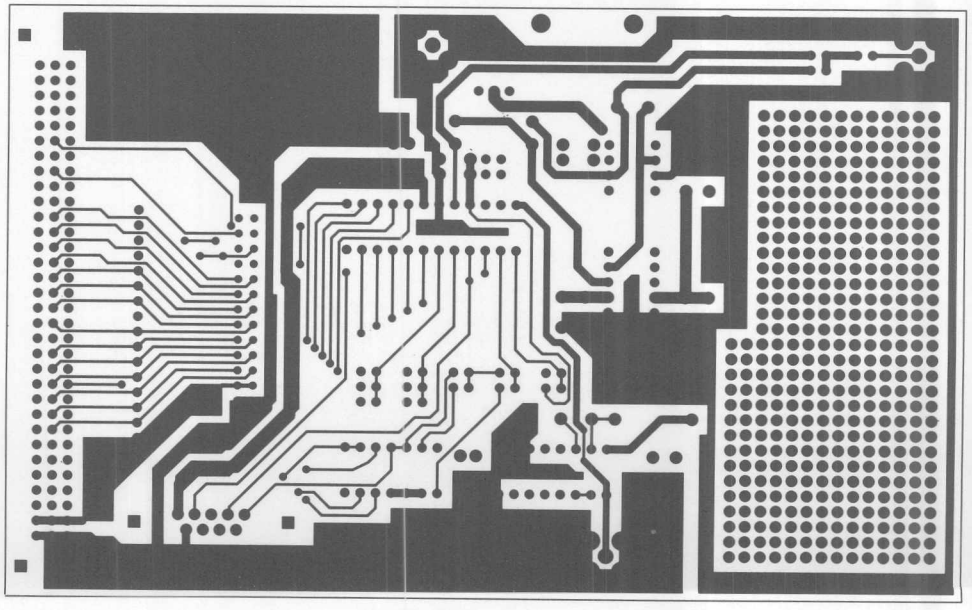
SILKSCREEN

Figure 26. PCB Silkscreen for Figure 25



COMPONENT SIDE

Figure 27. PCB Component Side Layout for Figure 25



SOLDER SIDE

Figure 28. PCB Solder Side Layout for Figure 25

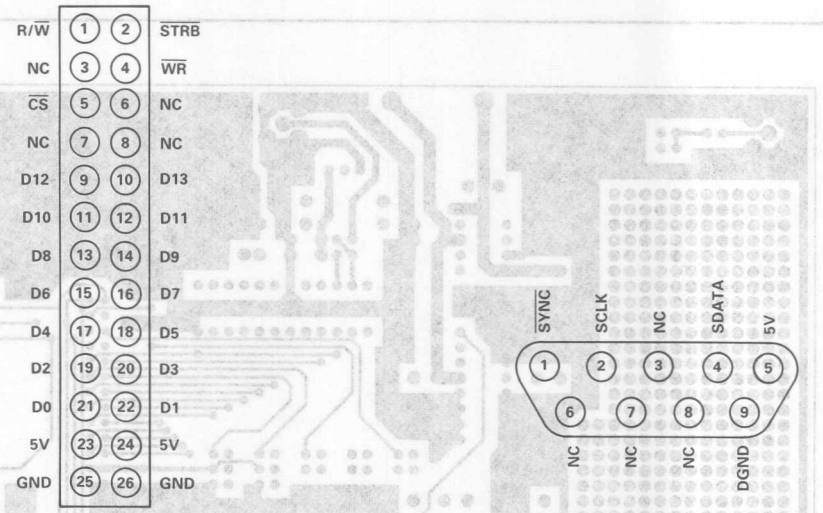
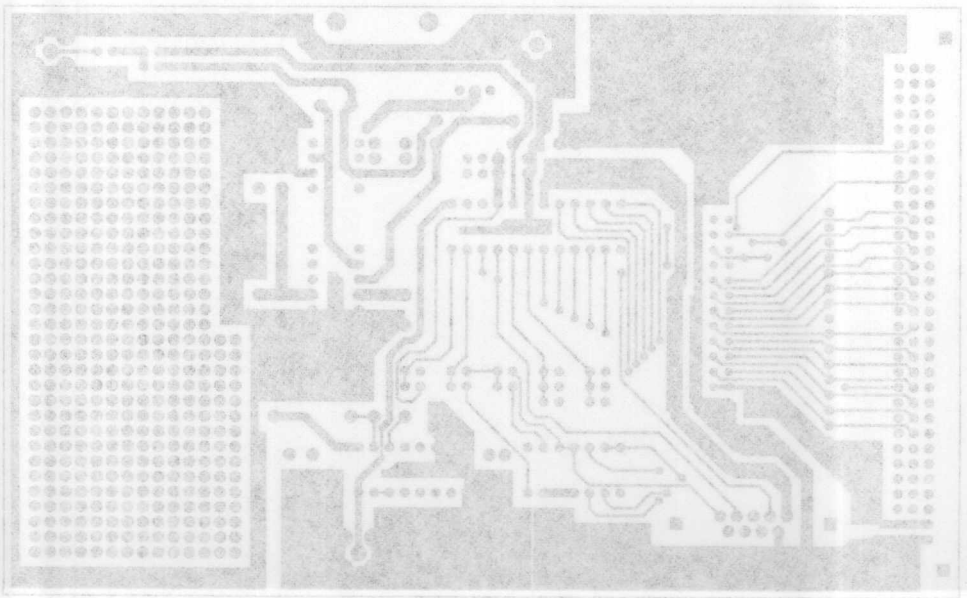


Figure 29. SKT4, IDC Connector Pinout

Figure 30. SKT5, D-Type Connector Pinout

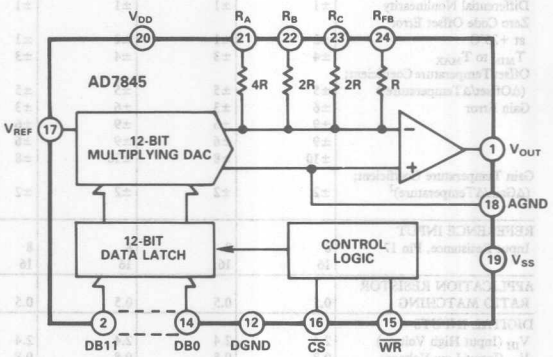


LC²MOS
Complete 12-Bit Multiplying DAC
AD7845

FEATURES
- 12-Bit CMOS MDAC with Output Amplifier
- 4-Quadrant Multiplication
- Guaranteed Monotonic (T_{MIN} to T_{MAX})
- Space-Saving 0.3″ DIPs and 24- or 28-Terminal Surface Mount Packages
- Application Resistors On Chip for Gain Ranging, etc.
- Low Power LC²MOS

APPLICATIONS
- Automatic Test Equipment
- Digital Attenuators
- Programmable Power Supplies
- Programmable Gain Amplifiers
- Digital-to-4–20 mA Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7845 is the industry's first 4-quadrant multiplying D/A converter with an on-chip amplifier. It is fabricated on the LC²MOS process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The 12 data inputs drive latches which are controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, making microprocessor interfacing simple. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5 V CMOS compatible.

The output amplifier can supply ±10 V into a 2 kΩ load. It is internally compensated, and its input offset voltage is low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT}, but the user may alternatively choose R_A, R_B or R_C to scale the output voltage range.

PRODUCT HIGHLIGHTS

1. Voltage Output Multiplying DAC
   The AD7845 is the first DAC which has a full 4-quadrant multiplying capability and an output amplifier on chip. All specifications include amplifier performance.
2. Matched Application Resistors
   Three application resistors provide an easy facility for gain ranging, voltage offsetting, etc.
3. Space Saving
   The AD7845 saves space in two ways. The integration of the output amplifier on chip means that chip count is reduced. The part is housed in skinny 24-pin, 0.3″ DIP, 28-terminal LCC and PLCC and 24-terminal SOIC packages.

ACCURACY								
Resolution	12	12	12	12	12	12	Bits	1 LSB = $\frac{V_{REF}}{2^{12}}$ = 2.4 mV
Relative Accuracy								
at +25°C	±1	±1/2	±1	±1/2	±1	±1/2	LSB max	All Grades Are Guaranteed
T_{MIN} to T_{MAX}	±1	±3/4	±3/2	±1	±2	±1	LSB max	Monotonic over Temperature
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	DAC Register Loaded with All 0s.
Zero Code Offset Error								
at +25°C	±2	±1	±2	±1	±2	±1	mV max	
T_{MIN} to T_{MAX}	±4	±3	±4	±3	±5	±4	mV max	
Offset Temperature Coefficient; (ΔOffset/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	µV/°C typ	
Gain Error	±6	±3	±6	±3	±6	±3	LSB max	R_{FB}, V_{OUT} Connected
	±9	±6	±9	±6	±9	±6	LSB max	R_C, V_{OUT} Connected, V_{REF} = +5 V
	±9	±6	±9	±6	±9	±6	LSB max	R_B, V_{OUT} Connected, V_{REF} = +5 V
	±10	±8	±10	±8	±10	±8	LSB max	R_A, V_{OUT} Connected, V_{REF} = +2.5 V
Gain Temperature Coefficient; (ΔGain/ΔTemperature)[2]	±2	±2	±2	±2	±2	±2	ppm of FSR/°C typ	R_{FB}, V_{OUT} Connected
REFERENCE INPUT								
Input Resistance, Pin 17	8	8	8	8	8	8	kΩ min	Typical Input Resistance = 12 kΩ
	16	16	16	16	16	16	kΩ max	
APPLICATION RESISTOR RATIO MATCHING	0.5	0.5	0.5	0.5	0.5	0.5	% max	Matching Between R_A, R_B, R_C
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±1	±1	±1	±1	±1	±1	µA max	Digital Inputs at 0 V and V_{DD}
C_{IN} (Input Capacitance)[2]	7	7	7	7	7	7	pF max	
POWER SUPPLY[4]								
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V min/V max	
V_{SS} Range	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	V min/V max	
Power Supply Rejection								
ΔGain/ΔV_{DD}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{DD} = +15 V ± 5%, V_{REF} = −10 V
ΔGain/ΔV_{SS}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{SS} = −15 V ± 5%.
I_{DD}	10	10	10	10	10	10	mA max	V_{OUT} Unloaded
I_{SS}	4	4	4	4	4	4	mA max	V_{OUT} Unloaded

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance and are not subject to test.

DYNAMIC PERFORMANCE								
Output Voltage Settling Time	5	5	5	5	5	5	µs max	To 0.01% of Full-Scale Range. V_{OUT} Load = 2 kΩ, 100 pF. DAC Register Alternately Loaded with All 0s and All 1s. Typically 2.5 µs at 25°C.
Slew Rate	7	7	7	7	7	7	V/µs typ	V_{OUT} Load = 2 kΩ, 100 pF.
Digital-to-Analog Glitch Impulse	450	450	450	450	450	450	nV-s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error[3]	5	5	5	5	5	5	mV p–p typ	V_{REF} = ±10 V, 10 kHz Sine Wave DAC Register Loaded with All 0s.
Unity Gain Small Signal Bandwidth	600	600	600	600	600	600	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s. V_{REF} = 100 mV p–p Sine Wave.
Full Power Bandwidth	250	250	250	250	250	250	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s. V_{REF} = 20 V p–p Sine Wave. R_L = 2 kΩ.
Total Harmonic Distortion	−90	−90	−90	−90	−90	−90	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
OUTPUT CHARACTERISTICS[5]								
Open Loop Gain	85	85	85	85	85	85	dB min	V_{OUT}, R_{FB} Not Connected
Output Voltage Swing	±10	±10	±10	±10	±10	±10	V min	V_{OUT} = ±10 V, R_L = 2 kΩ
Output Resistance	0.2	0.2	0.2	0.2	0.2	0.2	Ω typ	R_L = 2 kΩ, C_L = 100 pF
Short Circuit Current @ +25°C	15	15	15	15	15	15	mA typ	R_{FB}, V_{OUT} Connected, V_{OUT} Shorted to AGND
Output Noise Voltage (0.1Hz to 10Hz) @ +25°C	2	2	2	2	2	2	µV rms typ	Includes Noise Due to Output Amplifier and Johnson Noise of R_{FB}
f = 10 Hz	250	250	250	250	250	250	nV/√Hz typ	
f = 100 Hz	100	100	100	100	100	100	nV/√Hz typ	
f = 1 kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 10 kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 100 kHz	50	50	50	50	50	50	nV/√Hz typ	

NOTES
[1]Temperature Ranges are as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S, T Versions: −55°C to +125°C.
[2]Sample tested to ensure compliance.
[3]The metal lid on the ceramic D-24A package is connected to Pin 12 (DGND).
[4]The device is functional with a power supply of ±12 V.
[5]Minimum specified load resistance is 2 kΩ.

Specifications subject to change without notice.

Parameter	Limit at T_A = +25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{CS}	100	135	140	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	100	135	140	ns min	Write Pulse Width
t_{DS}	100	100	120	ns min	Data Setup Time
t_{DH}	20	20	20	ns min	Data Hold Time

Specifications subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3 V to +17 V
V_{SS} to DGND . . . . . +0.3 V to −17 V
V_{REF} to AGND . . . . . ±25 V
V_{RFB} to AGND . . . . . ±25 V
V_{RA} to AGND . . . . . ±25 V
V_{RB} to AGND . . . . . ±25 V
V_{RC} to AGND . . . . . ±25 V
V_{OUT} to AGND[1] . . . . . V_{DD} +0.3 V, V_{SS} −0.3 V
AGND to DGND . . . . . −0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
Power Dissipation (Any Package)
To +75°C . . . . . 650 mW
Derates above +75°C . . . . . 10 mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

NOTE
[1]V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

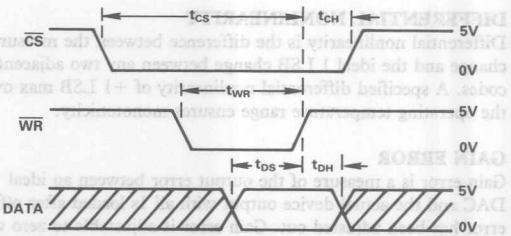
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Package Option[3]
AD7845JN	0°C to +70°C	±1 LSB	N-24
AD7845KN	0°C to +70°C	±1/2 LSB	N-24
AD7845JP	0°C to +70°C	±1 LSB	P-24A
AD7845KP	0°C to +70°C	±1/2 LSB	P-24A
AD7845JR	0°C to +70°C	±1 LSB	R-24
AD7845KR	0°C to +70°C	±1/2 LSB	R-24
AD7845AQ	−25°C to +85°C	±1 LSB	Q-24
AD7845BQ	−25°C to +85°C	±1/2 LSB	Q-24
AD7845SQ/883B	−55°C to +125°C	±1 LSB	Q-24
AD7845TQ/883B	−55°C to +125°C	±1/2 LSB	Q-24
AD7845SE/883B	−55°C to +125°C	±1 LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

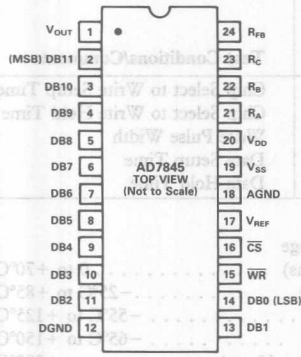


NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_R = t_F = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

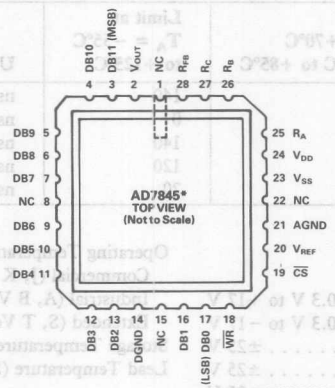
Figure 1. AD7845 Timing Diagram

PIN CONFIGURATIONS

DIP, SOIC

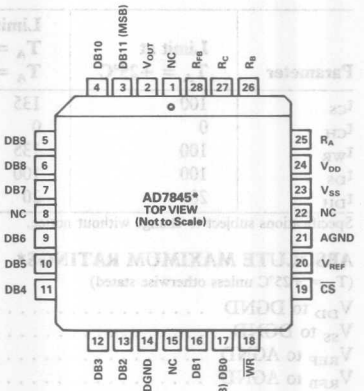


LCC



*NC = NO CONNECT

PLCC



*NC = NO CONNECT

TERMINOLOGY

LEAST SIGNIFICANT BIT

This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7845, 1LSB = $\frac{V_{REF}}{2^{12}}$.

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain error are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of +1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer. See Figure 13.

ZERO CODE OFFSET ERROR

This is the error present at the device output with all 0s loaded in the DAC. It is due to the op amp input offset voltage and bias current and the DAC leakage current.

TOTAL HARMONIC DISTORTION

This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

OUTPUT NOISE

This is the noise due to the white noise of the DAC and the input noise of the amplifier.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

DIGITAL FEEDTHROUGH

When the DAC is not selected (i.e., $\overline{CS}$ is high) high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

MULTIPLYING FEEDTHROUGH ERROR

This is ac error due to capacitive feedthrough from the V_{REF} terminal to V_{OUT} when the DAC is loaded with all 0s.

OPEN-LOOP GAIN

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied at the V_{REF} pin with all 1s loaded in the DAC. It is specified at dc.

UNITY GAIN SMALL SIGNAL BANDWIDTH

This is the frequency at which the magnitude of the small signal voltage gain of the output amplifier is 3 dB below unity. The device is operated as a closed-loop unity gain inverter (i.e., DAC is loaded with all 1s).

OUTPUT RESISTANCE

This is the effective output source resistance.

FULL POWER BANDWIDTH

Full power bandwidth is specified as the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a distortion level of 3%.

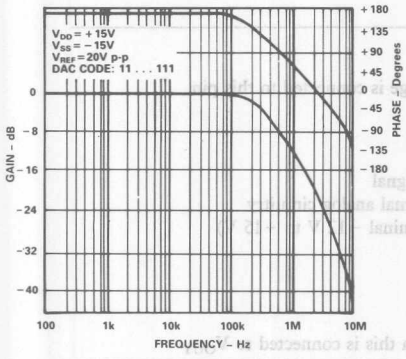


Figure 2. Frequency Response, G = −1

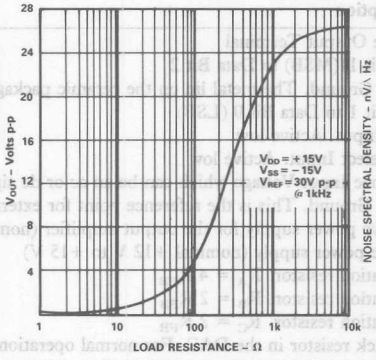


Figure 3. Output Voltage Swing vs. Resistive Load

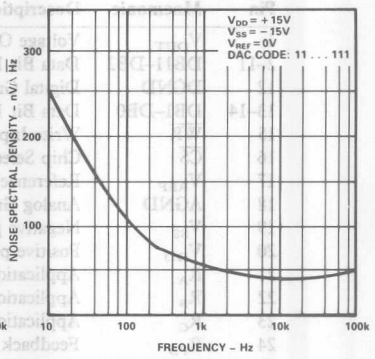


Figure 4. Noise Spectral Density

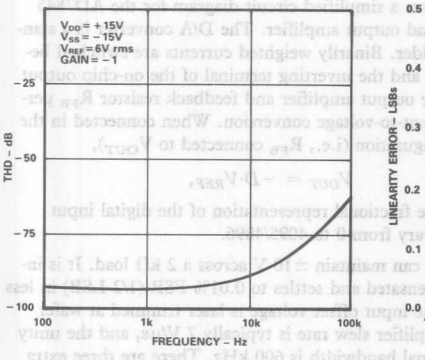


Figure 5. THD vs. Frequency

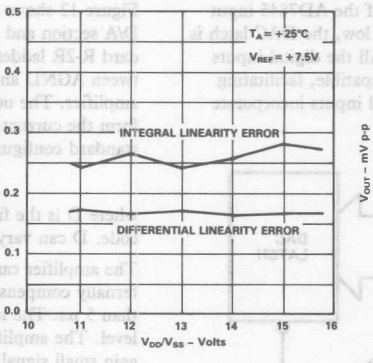


Figure 6. Typical AD7845 Linearity vs. Power Supply

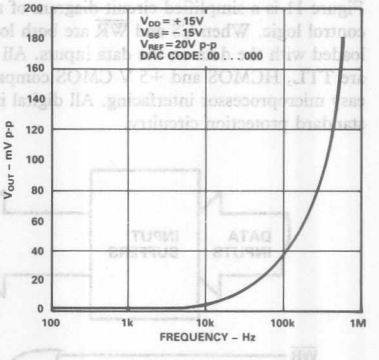


Figure 7. Multiplying Feedthrough Error vs. Frequency

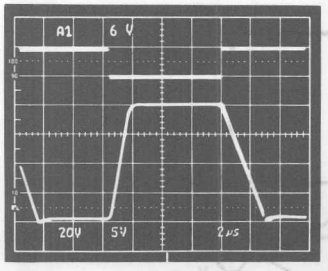


Figure 8. Unity Gain Inverter Pulse Response (Large Signal)

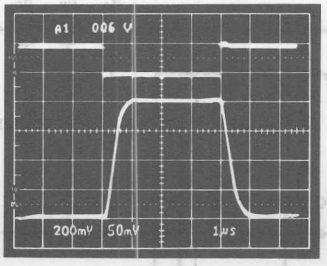


Figure 9. Unity Gain Inverter Pulse Response (Small Signal)

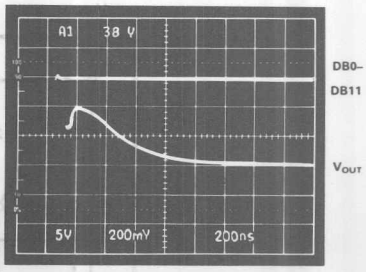


Figure 10. Digital-to-Analog Glitch Impulse (All 1s to All 0s Transition)

Pin	Mnemonic	Description
1	V_{OUT}	Voltage Output Terminal
2–11	DB11–DB2	Data Bit 11(MSB) to Data Bit 2
12	DGND	Digital Ground. The metal lid on the ceramic package is connected to this pin
13–14	DB1–DB0	Data Bit 1 to Data Bit 0 (LSB)
15	$\overline{WR}$	Write Input. Active low
16	$\overline{CS}$	Chip Select Input. Active low
17	V_{REF}	Reference Input Voltage which can be an ac or dc signal
18	AGND	Analog Ground. This is the reference point for external analog circuitry
19	V_{SS}	Negative power supply for the output amplifier (nominal −12 V to +15 V)
20	V_{DD}	Positive power supply (nominal +12 V to +15 V)
21	R_A	Application resistor. $R_A = 4\ R_{FB}$
22	R_B	Application resistor. $R_B = 2\ R_{FB}$
23	R_C	Application resistor. $R_C = 2\ R_{FB}$
24	R_{FB}	Feedback resistor in the DAC. For normal operation this is connected to V_{OUT}

CIRCUIT INFORMATION

Digital Section

Figure 11 is a simplified circuit diagram of the AD7845 input control logic. When $\overline{CS}$ and $\overline{WR}$ are both low, the DAC latch is loaded with the data on the data inputs. All the digital inputs are TTL, HCMOS and +5 V CMOS compatible, facilitating easy microprocessor interfacing. All digital inputs incorporate standard protection circuitry.

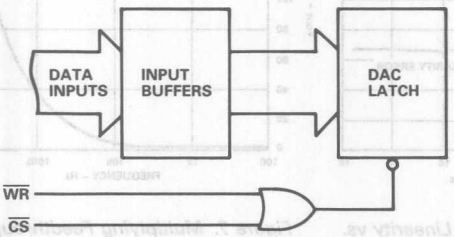


Figure 11. AD7845 Input Control Logic

D/A Section

Figure 12 shows a simplified circuit diagram for the AD7845 D/A section and output amplifier. The D/A converter is a standard R-2R ladder. Binarily weighted currents are switched between AGND and the inverting terminal of the on-chip output amplifier. The output amplifier and feedback resistor R_{FB} perform the current-to-voltage conversion. When connected in the standard configuration (i.e., R_{FB} connected to V_{OUT}),

$$V_{OUT} = -D \cdot V_{REF},$$

where D is the fractional representation of the digital input code. D can vary from 0 to 4095/4096.

The amplifier can maintain ±10 V across a 2 kΩ load. It is internally compensated and settles to 0.01% FSR (1/2 LSB) in less than 5 μs. The input offset voltage is laser trimmed at wafer level. The amplifier slew rate is typically 7 V/μs, and the unity gain small signal bandwidth is 600 kHz. There are three extra on-chip resistors (R_A, R_B, R_C) connected to the amplifier inverting terminal. These are useful in a number of applications including offset adjustment and gain ranging.

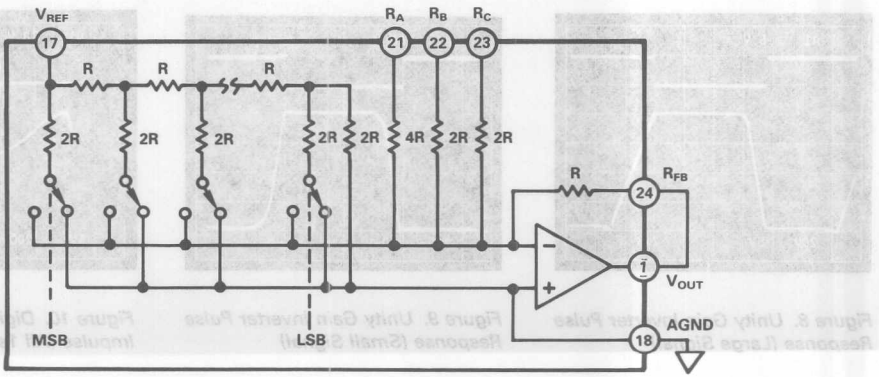


Figure 12. Simplified Circuit Diagram for the AD7845 D/A Section and Output Amplifier

UNIPOLAR BINARY OPERATION

Figure 13 shows the AD7845 connected for unipolar binary operation. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. The code table for Figure 13 is given in Table I.

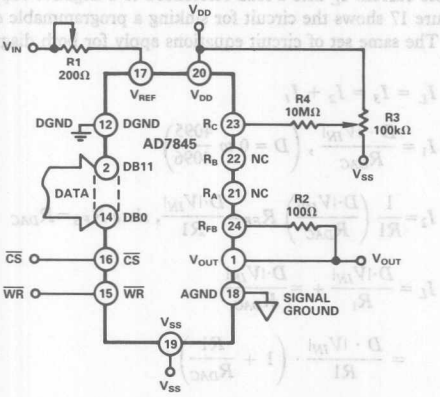


Figure 13. Unipolar Binary Operation

Table I. Unipolar Binary Code Table for AD7845

Binary Number In DAC Register			Analog Output, V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right)=-1/2V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 V

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 13

Zero Offset Adjustment

1. Load DAC with all 0s.
2. Trim R3 until V_{OUT} = 0 V.

Gain Adjustment

1. Load DAC with all 1s.
2. Trim R1 so that $V_{OUT} = -V_{IN}\frac{4095}{4096}$.

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude. For high temperature applications, resistors and potentiometers should have a low temperature coefficient.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit for bipolar operation is shown in Figure 14. Offset binary coding is used.

The offset specification of this circuit is determined by the matching of internal resistors R_B and R_C and by the zero code offset error of the device. Gain error may be adjusted by varying the ratio of R1 and R2.

To use this circuit without trimming and keep within the gain error specifications, resistors R1 and R2 should be ratio matched to 0.01%.

The code table for Figure 14 is given in Table II.

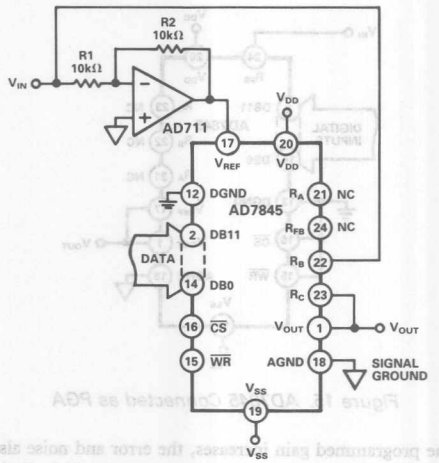


Figure 14. Bipolar Offset Binary Operation

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 14

Binary Number In DAC Register			Analog Output, V_{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0 V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)=-V_{IN}$

APPLICATIONS CIRCUITS

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The AD7845 performs a PGA function when connected as in Figure 15. In this configuration, the R-2R ladder is connected in the amplifier feedback loop. R_{FB} is the amplifier input resistor. As the code decreases, the R-2R ladder resistance increases and so the gain increases.

$$V_{OUT} = -V_{IN} \cdot \frac{R_{DAC}}{D} \cdot \frac{1}{R_{FB}}, \left(D = 0 \text{ to } \frac{4095}{4096}\right)$$

$$= -V_{IN} \cdot \frac{R_{DAC}}{D} \cdot \frac{1}{R_{DAC}} = \frac{-V_{IN}}{D}, \text{ since } R_{FB} = R_{DAC}$$

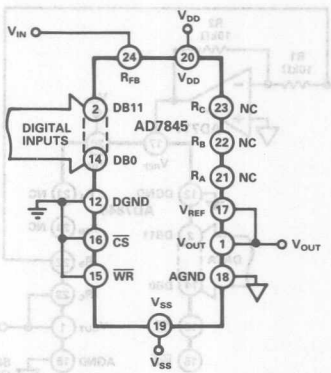


Figure 15. AD7845 Connected as PGA

As the programmed gain increases, the error and noise also increase. For this reason, the maximum gain should be limited to 256. Table III shows gain versus code.

Note that instead of using R_{FB} as the input resistor, it is also possible to use combinations of the other application resistors, R_A, R_B and R_C. For instance, if R_B is used instead of R_{FB}, the gain range for the same codes of Table II now goes from 1/2 to 128.

Table III. Gain and Error vs. Input Code for Figure 15

Digital Inputs			Gain	Error (%)
1111	1111	1111	4096/4095 ≈ 1	0.04
1000	0000	0000	2	0.07
0100	0000	0000	4	0.13
0010	0000	0000	8	0.26
0001	0000	0000	16	0.51
0000	1000	0000	32	1.02
0000	0100	0000	64	2.0
0000	0010	0000	128	4.0
0000	0001	0000	256	8.0

PROGRAMMABLE CURRENT SOURCES

The AD7845 is ideal for designing programmable current sources using a minimum of external components. Figures 16 and 17 are examples. The circuit of Figure 16 drives a programmable current I_L into a load referenced to a negative supply. Figure 17 shows the circuit for sinking a programmable current, I_L. The same set of circuit equations apply for both diagrams.

$$I_L = I_3 = I_2 + I_1$$

$$I_1 = \frac{D \cdot |V_{IN}|}{R_{DAC}}, \left(D = 0 \text{ to } \frac{4095}{4096}\right)$$

$$I_2 = \frac{1}{R1}\left(\frac{D \cdot |V_{IN}|}{R_{DAC}}\right) R_{FB} = \frac{D \cdot |V_{IN}|}{R1}, \text{ since } R_{FB} = R_{DAC}$$

$$I_L = \frac{D \cdot |V_{IN}|}{R_1} + = \frac{D \cdot |V_{IN}|}{R_{DAC}}$$

$$= \frac{D \cdot |V_{IN}|}{R1} \cdot \left(1 + \frac{R1}{R_{DAC}}\right)$$

Note that by making R1 much smaller than R_{DAC}, the circuit becomes insensitive to both the absolute value of R_{DAC} and its temperature variations. Now, the only resistor determining load current I_L is the sense resistor R1.

If R1 = 100 Ω, then the programming range is 0 to 100 mA, and the resolution is 0.024 mA.

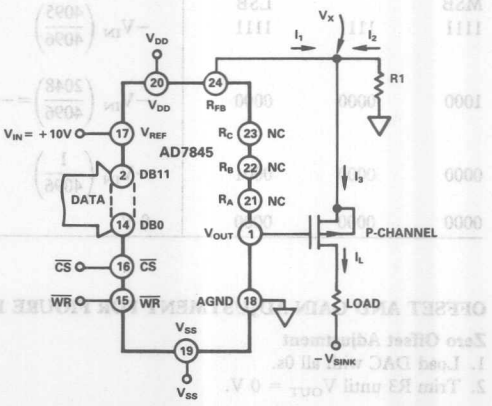


Figure 16. Programmable Current Source

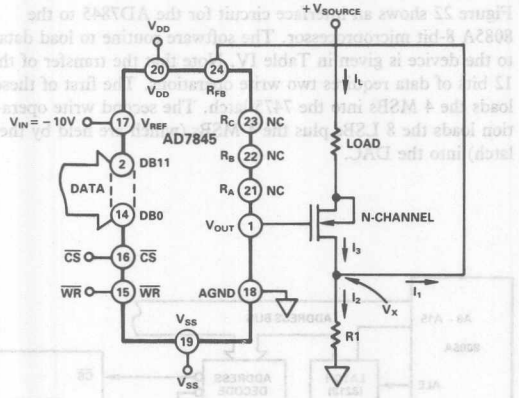


Figure 17. Programmable Current Sink

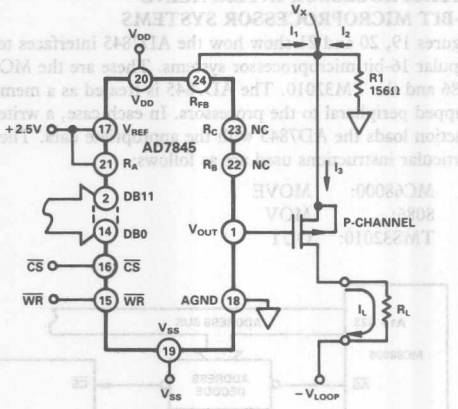


Figure 18. 4–20 mA Current Loop

4–20 mA CURRENT LOOP

The AD7845 provides an excellent way of making a 4–20 mA current loop circuit. This is basically a variation of the circuits in Figures 16 and 17 and is shown in Figure 18. The application resistor R_A (Value 4R) produces the effective 4 mA offset.

$I_L = I_3 = I_2 + I_1$

Since $I_2 > I_1$,

$$I_L = -\frac{V_X}{156} = \left(\frac{2.5}{4R} \times R_{FB} + \frac{2.5}{R_{DAC}} \times D \times R_{FB}\right) \times \frac{1}{156}$$

and since $R_{DAC} = R_{FB} = R$

$$I_L = \left(\frac{2.5}{4} + D \times 2.5\right) \times \frac{1000}{156}\ mA$$

$= [4 + (16 \times D)]mA$, where D goes from 0 to 1 with Digital Code

When D = 0 (Code of all 0s):
I_L = 4 mA

When D = 1 (Code of all 1s):
I_L = 20 mA

The above circuit succeeds in significantly reducing the circuit component count. Both the on-chip output amplifier and the application resistor R_A contribute to this.

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7845. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7845 AGND and DGND pins (IN914 or equivalent).

Digital Glitches: When a new digital word is written into the DAC, it results in a change of voltage applied to some of the DAC switch gates. This voltage change is coupled across the switch stray capacitance and appears as an impulse on the current output bus of the DAC. In the AD7845, impulses on this bus are converted to a voltage by R_{FB} and the output amplifier. The output voltage glitch energy is specified as the area of the resulting spike in nV-seconds. It is measured with V_{REF} connected to analog ground and for a zero to full-scale input code transition. Since mircoprocessor based systems generally have noisy grounds which couple into the power supplies, the AD7845 V_{DD} and V_{SS} terminals should be decoupled to signal ground.

Temperature Coefficients: The gain temperature coefficient of the AD7845 has a maximum value of 5 ppm/°C. This corresponds to wrost case gain shift of 2 LSBs over a 100°C temperature range. When trim resistors R1 and R2 in Figure 13 are used to adjust full-scale range, the temperature coefficient of R1 and R2 must be taken into account. The offset temperature coefficient is 5 ppm of FSR/°C maximum. This correponds to a worst case offset shift of 2 LSBs over a 100°C temperature range.

The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS," Publication Number E630C-5-3/86.

MICROPROCESSOR INTERFACING

16-BIT MICROPROCESSOR SYSTEMS

Figures 19, 20 and 21 show how the AD7845 interfaces to three popular 16-bit microprocessor systems. These are the MC68000, 8086 and the TM32010. The AD7845 is treated as a memory-mapped peripheral to the processors. In each case, a write instruction loads the AD7845 with the appropriate data. The particular instructions used are as follows:

MC68000: MOVE
8086: MOV
TMS32010: OUT

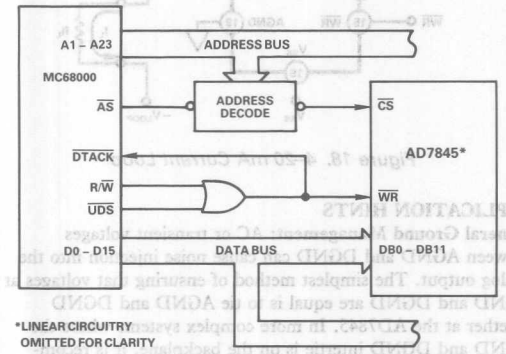


Figure 19. AD7845 to MC68000 Interface

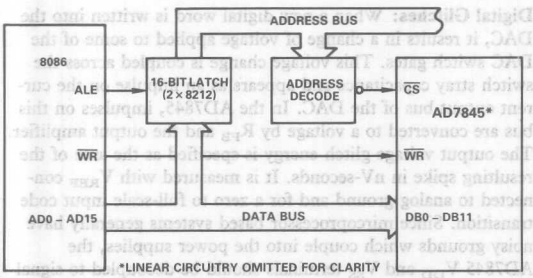


Figure 20. AD7845 to 8086 Interface

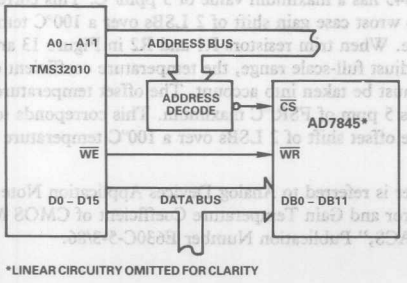


Figure 21. TMS32010

8-BIT MICROPROCESSOR SYSTEMS

Figure 22 shows an interface circuit for the AD7845 to the 8085A 8-bit microprocessor. The software routine to load data to the device is given in Table IV. Note that the transfer of the 12 bits of data requires two write operations. The first of these loads the 4 MSBs into the 7475 latch. The second write operation loads the 8 LSBs plus the 4 MSBs (which are held by the latch) into the DAC.

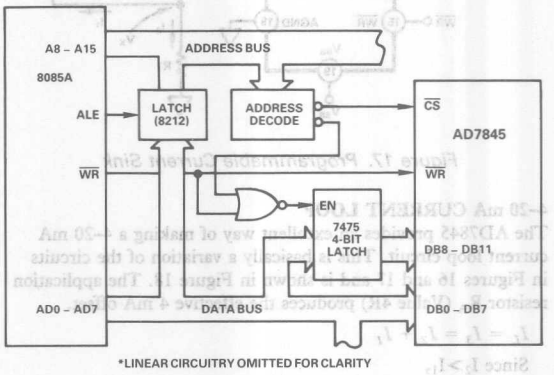
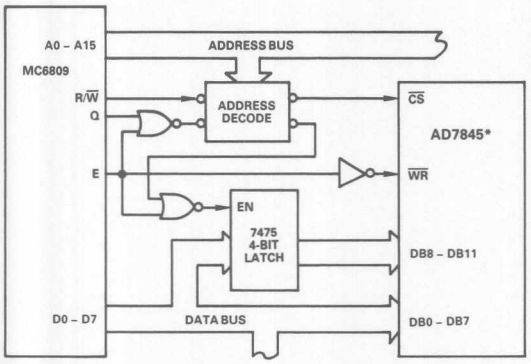


Figure 22. 8085A Interface

Table IV. Subroutine Listing for Figure 22

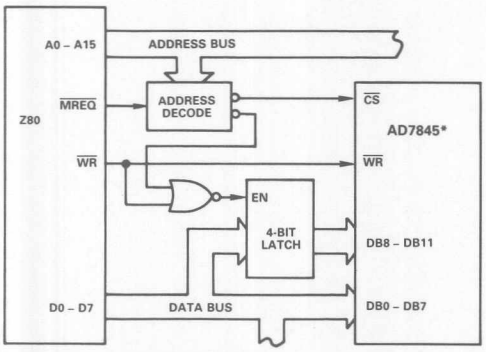
2000	LOAD DAC : LXI	H,#3000	The H,L register pair are loaded with latch address 3000.
	MVI	A,#"MS"	Load the 4 MSBs of data into accumulator.
	MOV	M,A	Transfer data from accumulator to latch.
	INR	L	Increment H,L pair to AD7845 address.
	MVI	A,#"LS"	Load the 8 LSBs of data into accumulator.
	MOV	M,A	Transfer data from accumulator to DAC.
	RET		End of routine.

Figure 23 and 24 are the interface circuits for the Z80 and MC6809 microprocessors. Again, these use the same basic format as the 8085A interface.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 23. AD7845 to Z80 Interface

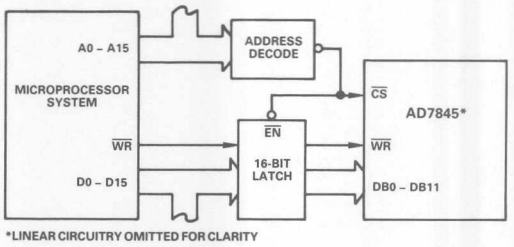


*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 24. MC6809 Interface

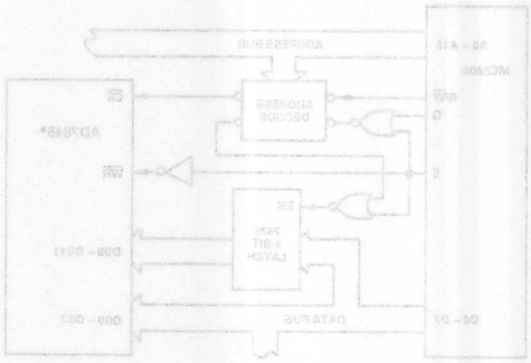
DIGITAL FEEDTHROUGH

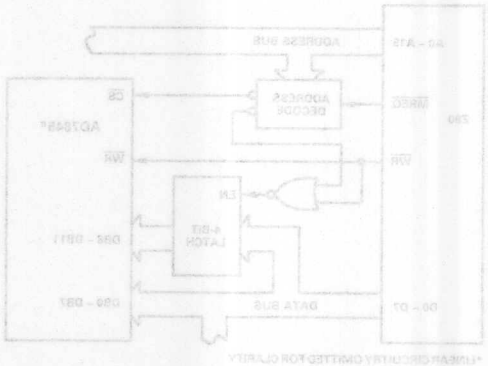
In the preceding interface configurations, most digital inputs to the AD7845 are directly connected to the microprocess bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 25 shows an interface circuit which uses this technique. All data inputs are latched from the busy by the $\overline{CS}$ signal. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 25. AD7845 Interface Circuit Using Latches to Minimize Digital Feedthrough


ADDRESS BUS
A0 – A15
MC6809
E
R/W
ADDRESS DECODE
CS
ADC7845*
WR
EN
74LS 4-BIT LATCH
DB8 – DB11
DB0 – DB7
DATA BUS
D0 – D7
*LINEAR CIRCUITRY OMITTED FOR CLARITY


ADDRESS BUS
A0 – A15
MREQ
Z80
ADDRESS DECODE
CS
ADC7845*
WR
EN
4-BIT LATCH
DB8 – DB11
DB0 – DB7
DATA BUS
D0 – D7
*LINEAR CIRCUITRY OMITTED FOR CLARITY

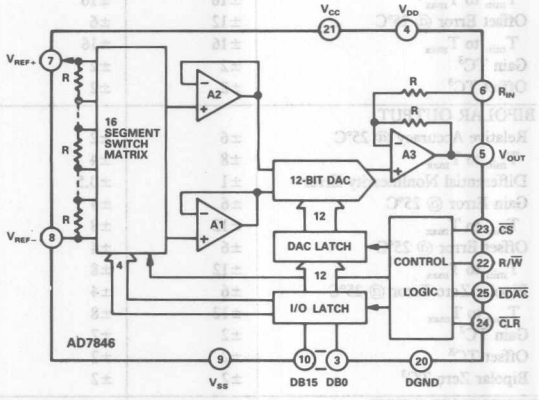
LC²MOS 16-Bit Voltage Output DAC

AD7846

FEATURES

16-Bit Monotonicity over Temperature
±2LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power (100mW typical)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with Analog Devices' LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipolar output range (0 to +5V, 0 to +10V) or bipolar output ranges (±5V, ±10V).

The DAC uses a segmented architecture. The 4MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents of the DAC latch to 00 . . . 000 or 10 . . . 000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-pin plastic, ceramic, LCCC and PLCC packages.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100mW makes the AD7846 the lowest power, high accuracy DAC on the market.

AD7846—SPECIFICATIONS[1]

(V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V. V_{OUT} loaded with 2kΩ, 1000pF to 0V. V_{REF+} = +5V, R_{IN} connected to 0V. All specifications T_{MIN} to T_{MAX} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version[2]	Units	Test Conditions/Comments
Resolution	16	16	16	Bits	
UNIPOLAR OUTPUT					V_{REF-}=0V, V_{OUT}=0V to +10V
Relative Accuracy @ 25°C	±12	±4	±12	LSB typ	1LSB=153μV
T_{min} to T_{max}	±16	±8	±16	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±12	±6	±12	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±16	±24	LSB max	
Offset Error @ 25°C	±12	±6	±12	LSB typ	
T_{min} to T_{max}	±16	±16	±24	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-}=−5V, V_{OUT}=−10V to +10V
Relative Accuracy @ 25°C	±6	±2	±6	LSB typ	1LSB=305μV
T_{min} to T_{max}	±8	±4	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±12	±8	±16	LSB max	
Offset Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±12	±8	±16	LSB max	
Bipolar Zero Error @ 25°C	±6	±4	±6	LSB typ	
T_{min} to T_{max}	±12	±8	±16	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20	20	20	kΩ min	Resistance from V_{REF-} to V_{REF+}
	40	40	40	kΩ max	Typically 30kΩ
V_{REF+} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
V_{REF-} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V max	
Resistive Load	2	2	3	kΩ min	To 0V
Capacitive Load	1000	1000	1000	pF max	To 0V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0V or Any Power Supply
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK}=1.6mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE}=400μA
Floating State Leakage Current	±10	±10	±10	μA max	DB0-DB15=0 to V_{CC}
Floating State Output Capacitance[3]	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+11.4/+15.75	+11.4/+15.75	+11.4/+15.75	Vmin/Vmax	
V_{SS}	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	Vmin/Vmax	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	Vmin/Vmax	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[5]	1.5	1.5	2	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES

[1]Temperature Ranges as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S Version: −55°C to +125°C.

[2]Minimum load for S version is 3kΩ.

[3]Sample tested to ensure compliance.

[4]AD7846 is functional with power supplies of ±12V. See Typical Performance Curves.

[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. (V_{REF+} = +5V, V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V, R_{IN} connected to 0V.)

Parameter	T_A = 25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
Output Settling Time	7	7	µs max	To 0.006% FSR. V_{OUT} loaded. V_{REF-} = 0V.
	9	9	µs max	To 0.003% FSR. V_{OUT} loaded. V_{REF-} = −5V.
Digital-to-Analog Glitch Impulse	400	400	nV-secs typ	DAC alternately loaded with 10 . . . 0000 and 01 . . . 1111. V_{OUT} unloaded.
AC Feedthrough	0.5	0.5	mV pk-pk typ	V_{REF-} = 0V, V_{REF+} = 1V rms, 10kHz sine wave. DAC loaded with all 0s.
Digital Feedthrough	10	10	nV-secs typ	DAC alternately loaded with all 1s and all 0s. $\overline{CS}$ High.
Output Noise Voltage Density (1kHz–100kHz)	50	50	nV/$\sqrt{Hz}$ typ	Measured at V_{OUT}. DAC loaded with 0111011 . . . 11. V_{REF+} = V_{REF-} = 0V.

TIMING CHARACTERISTICS (V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C, T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Setup Time
t_2	150	160	190	ns min	$\overline{CS}$ Pulse Width (Write Cycle)
t_3	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Hold Time
t_4	110	110	120	ns min	Data Setup Time
t_5	0	0	0	ns min	Data Hold Time
t_6	230	270	320	ns max	Data Access Time
t_7	10	10	10	ns min	Bus Relinquish Time
	80	90	90	ns max	
t_8	20	20	20	ns min	$\overline{CLR}$ Setup Time
t_9	150	150	150	ns min	$\overline{CLR}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CLR}$ Hold Time
t_{11}	80	100	100	ns min	$\overline{LDAC}$ Pulse Width
t_{12}	240	280	330	ns min	$\overline{CS}$ Pulse Width (Read Cycle)

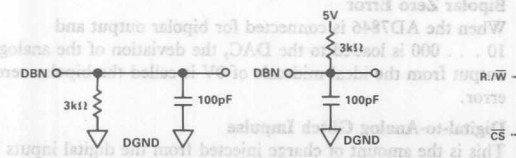
NOTES

[1]Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

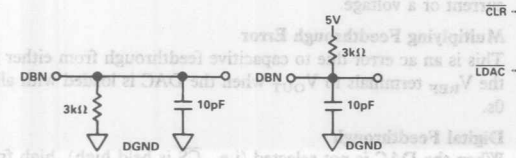
[3]t_7 is defined as the time required for an output to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High Z to V_{OH} b. High Z to V_{OL}

Figure 1. Load Circuits for Access Time (t_6)



a. V_{OH} to High Z b. V_{OL} to High Z

Figure 2. Load Circuits for Bus Relinquish Time (t_7)

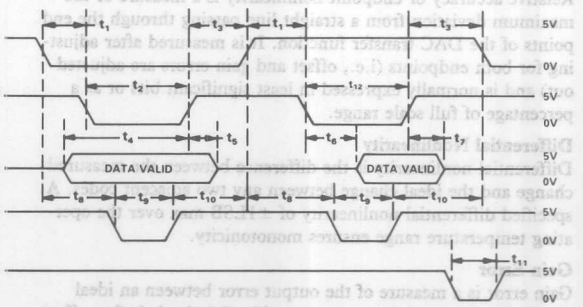
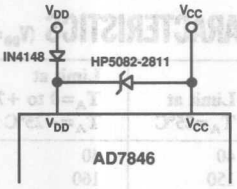


Figure 3. AD7846 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND . . . . . −0.3V or +17V
V_{CC} to DGND[2] . . . . . −0.3V, V_{DD} +0.3V or +7V (Whichever Is Lower)
V_{SS} to DGND . . . . . +0.3V to −17V
V_{REF+} to DGND . . . . . ±25V
V_{REF-} to DGND . . . . . ±25V
V_{OUT} to DGND[3] . . . . . ±25V
R_{IN} to DGND . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C
Operating Temperature Range
J, K Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.
[2]V_{CC} must not exceed V_{DD} by more than 0.3V. If it is possible for this to happen during power supply sequencing, the following diode protection scheme will ensure protection.



[3]V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceeded.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7846JN	0°C to +70°C	±16 LSB	N-28
AD7846KN	0°C to +70°C	±8 LSB	N-28
AD7846JP	0°C to +70°C	±16 LSB	P-28A
AD7846KP	0°C to +70°C	±8 LSB	P-28A
AD7846AD	−25°C to +85°C	±16 LSB	D-28
AD7846BD	−25°C to +85°C	±8 LSB	D-28
AD7846SD/883B	−55°C to +125°C	±16 LSB	D-28
AD7846SE/883B	−55°C to +125°C	±16 LSB	E-28A

*D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

Least Significant Bit
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7846, 1LSB = $(V_{REF+} - V_{REF-})/2^{16}$.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain errors are adjusted out) and is normally expressed in least significant bits or as a percentage of full scale range.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

Offset Error
This is the error present at the device output with all 0s loaded in the DAC. It is due to op amp input offset voltage and bias current and the DAC leakage current.

Bipolar Zero Error
When the AD7846 is connected for bipolar output and 10 . . . 000 is loaded to the DAC, the deviation of the analog output from the ideal midscale of 0V is called the bipolar zero error.

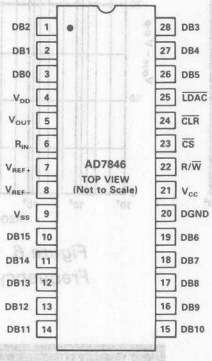
Digital-to-Analog Glitch Impulse
This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or a voltage.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from either of the V_{REF} terminals to V_{OUT} when the DAC is loaded with all 0s.

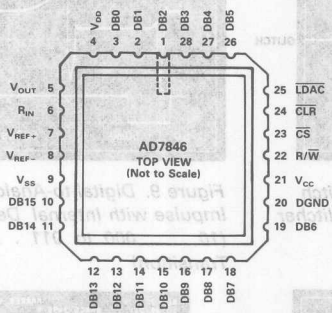
Digital Feedthrough
When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs in capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

PIN CONFIGURATIONS

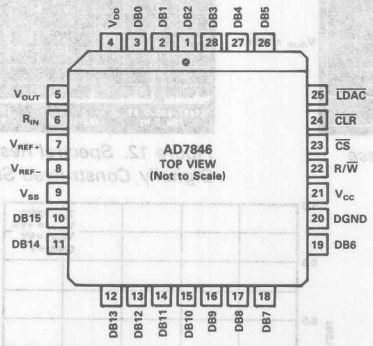
DIP



LCCC



PLCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1–3	DB2–DB0	Data I/O pins. DB0 is LSB.
4	V_{DD}	Positive supply for analog circuitry. This is +15V nominal.
5	V_{OUT}	DAC output voltage pin.
6	R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Table I.
7	V_{REF+}	V_{REF+} input. The DAC is specified for V_{REF+} = +5V.
8	V_{REF-}	V_{REF-} input. For unipolar operation connect V_{REF-} to 0V and for bipolar operation connect it to −5V. The device is specified for both conditions.
9	V_{SS}	Negative supply for analog circuitry. This is −15V nominal.
10–19	DB15–DB6	Data I/O pins. DB15 is MSB.
20	DGND	Ground pin for digital circuitry.
21	V_{CC}	Positive supply for digital circuitry. This is +5V nominal.
22	R/$\overline{W}$	R/$\overline{W}$ input. This can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Chip select input. This selects the device.
24	$\overline{CLR}$	Clear input. The DAC can be cleared to 000 . . . 000 or 100 . . . 000. See Table II.
25	$\overline{LDAC}$	Asynchronous load input to DAC.
26–28	DB5–DB3	Data I/O pins.

Output Range	V_{REF+}	V_{REF-}	R_{IN}
0V to +5V	+5V	0V	V_{OUT}
0V to +10V	+5V	0V	0V
+5V to −5V	+5V	−5V	V_{OUT}
+5V to −5V	+5V	0V	+5V
+10V to −10V	+5V	−5V	0V

Table I. AD7846 Output Voltage Ranges

AD7846—Typical Performance Curves

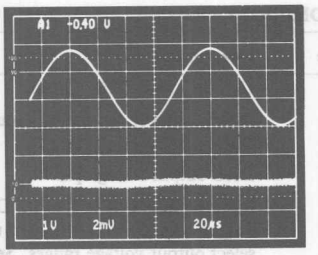


Figure 4. AC Feedthrough. V_{REF+} = 1V rms, 10kHz Sine Wave.

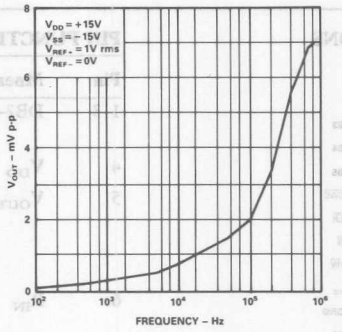


Figure 5. AC Feedthrough vs. Frequency

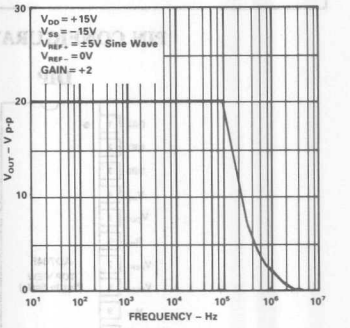


Figure 6. Large Signal Frequency Response

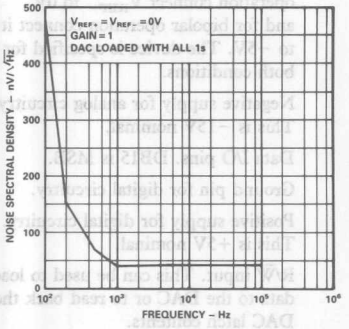


Figure 7. Noise Spectral Density

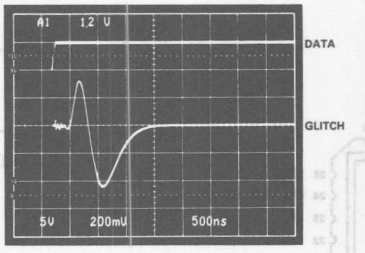


Figure 8. Digital-to-Analog Glitch Impulse without Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

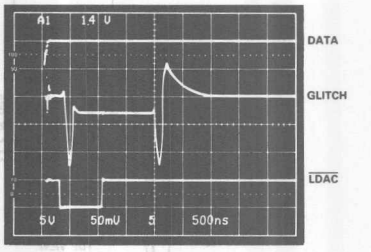


Figure 9. Digital-to-Analog Glitch Impulse with Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

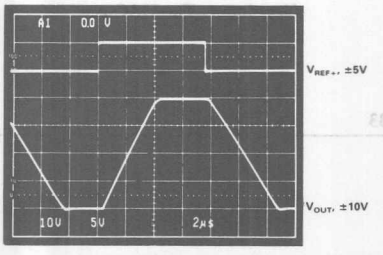


Figure 10. Pulse Response (Large Signal)

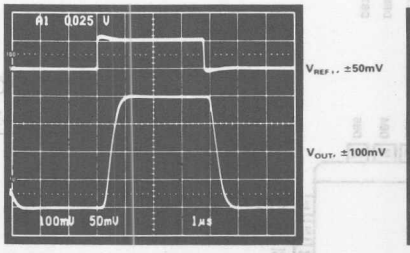


Figure 11. Pulse Response (Small Signal)

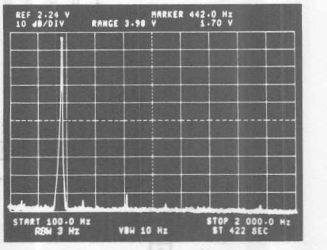


Figure 12. Spectral Response of Digitally Constructed Sine Wave

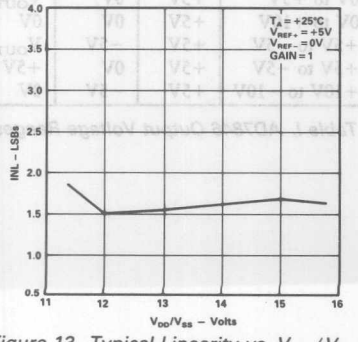


Figure 13. Typical Linearity vs. V_{DD}/V_{SS}

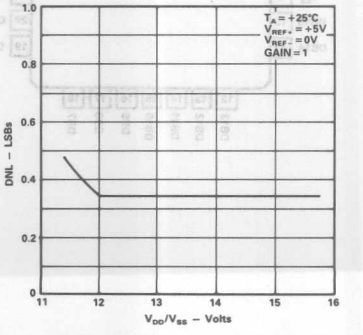


Figure 14. Typical Monotonicity vs. V_{DD}/V_{SS}

CIRCUIT DESCRIPTION

Digital Section

Figure 15 shows the digital control logic and on-chip data latches in the AD7846. Table II is the associated truth table. The D/A converter had two latches which are controlled by four signals: $\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$. The input latch is connected to the data bus (DB15–DB0). A word is written to the input latch by bringing $\overline{CS}$ low and R/$\overline{W}$ low. The contents of the input latch may be read back by bringing $\overline{CS}$ low and R/$\overline{W}$ high. This feature is called "readback" and is used in system diagnostic and calibration routines.

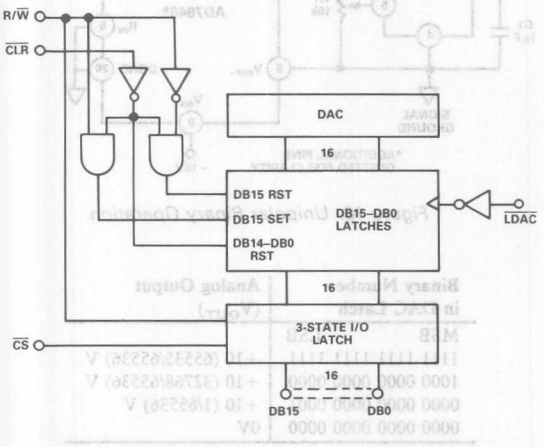


Figure 15. AD7846 Input Control Logic

CS	R/W	LDAC	CLR	Function
1	X	X	X	3-State DAC I/O Latch in High Z State
0	0	X	X	DAC I/O Latch Loaded with DB15–DB0
0	1	X	X	Contents of DAC I/O Latch Available on DB15–DB0
X	X	0	1	Contents of DAC I/O Latch Transferred to DAC Latch
X	0	X	0	DAC Latch Loaded with 000 . . . 000
X	1	X	0	DAC Latch Loaded with 100 . . . 000

Table II. AD7846 Control Logic Truth Table

Data is transferred from the input latch to the DAC latch with the $\overline{LDAC}$ strobe. The equivalent analog value of the DAC latch contents appears at the DAC output. The $\overline{CLR}$ pin resets the DAC latch contents to 000 . . . 000 or 100 . . . 000, depending on the state of R/$\overline{W}$. Writing a $\overline{CLR}$ loads 000 . . . 000 and reading a $\overline{CLR}$ loads 100 . . . 000. To reset a DAC to 0V in a unipolar system the user should exercise $\overline{CLR}$ while R/$\overline{W}$ is low; to reset to 0V in a bipolar system exercise the $\overline{CLR}$ while R/$\overline{W}$ is high.

D/A Conversion

Figure 16 shows the D/A section of the AD7846. There are three DACs, each of which have their own buffer amplifiers. DAC1 and DAC2 are 4-bit DACs. They share a 16-resistor string but have their own analog multiplexers. The voltage reference is applied to the resistor string. DAC3 is a 12-bit voltage mode DAC with its own output stage.

The 4MSBs of the 16-bit digital code drive DAC1 and DAC2 while the 12LSBs control DAC3. Using DAC1 and DAC2, the MSBs select a pair of adjacent nodes on the resistor string and present that voltage to the positive and negative inputs of DAC3. This DAC interpolates between these two voltages to produce the analog output voltage.

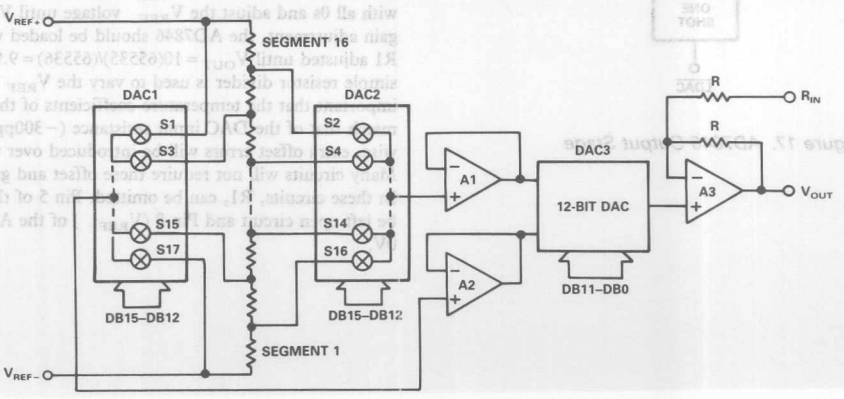


Figure 16. AD7846 D/A Conversion

DAC1 switches from the bottom of Segment 1 to the top of Segment 2 while DAC2 stays connected to the top of Segment 1. The code driving DAC3 is automatically complemented to compensate for the inversion of its inputs. This means that any linearity effects due to amplifier offset voltages remain unchanged when switching from one segment to the next and 16-bit monotonicity is ensured if DAC3 is monotonic. So, 12-bit resistor matching in DAC3 guarantees overall 16-bit monotonicity. This is much more acheivable than the 16-bit matching which a conventional R-2R structure would have needed.

Output Stage

The output stage of the AD7846 is shown in Figure 17. It is capable of driving a 2kΩ/1000pF load. It also has a resistor feedback network which allows the user to configure it for gains of one or two. Table I shows the different output ranges that are possible.

An additional feature is that the output buffer is configured as a track-and-hold amplifier. Although normally tracking its input, this amplifier is placed in a hold mode for approximately 1μs after the leading edge of $\overline{LDAC}$. This short state keeps the DAC output at its previous value while the AD7846 is internally changing to its new value. So, any glitches that occur in the transition are not seen at the output. In systems where the $\overline{LDAC}$ is tied permanently low, the deglitching will not be in operation. Figures 8 and 9 show the outputs of the AD7846 with and without the deglitcher.

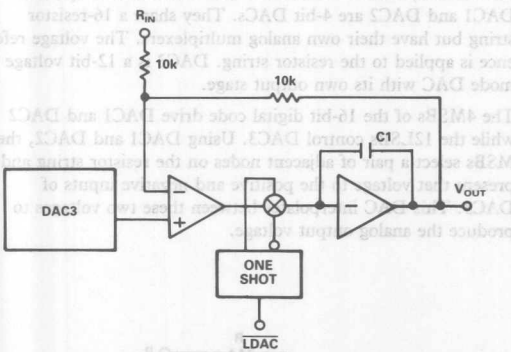


Figure 17. AD7846 Output Stage

Since R_{IN} is tied to 0V, the output amplifier has a gain of 2 and the output range is 0 to +10V. If a 0 to +5V range is required, R_{IN} should be tied to V_{OUT}, configuring the output stage for a gain of 1. Table III gives the code table for the circuit of Figure 18.

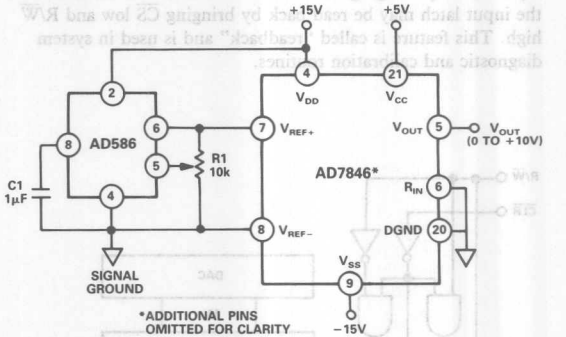


Figure 18. Unipolar Binary Operation

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	+10 (65535/65536) V
1000 0000 0000 0000	+10 (32768/65536) V
0000 0000 0000 0001	+10 (1/65536) V
0000 0000 0000 0000	0V

NOTE
1LSB = 10V/2^{16} = 10V/65536 = 152μV.

Table III. Code Table for Figure 18

Offset and gain may be adjusted in Figure 18 as follows : To adjust offset, disconnect the V_{REF-} input from 0V, load the DAC with all 0s and adjust the V_{REF-} voltage until V_{OUT} = 0V. For gain adjustment, the AD7846 should be loaded with all 1s and R1 adjusted until V_{OUT} = 10(65535)/(65536) = 9.999847V. If a simple resistor divider is used to vary the V_{REF-} voltage, it is important that the temperature coefficients of these resistors match that of the DAC input resistance (−300ppm/°C). Otherwise, extra offset errors will be introduced over temperature. Many circuits will not require these offset and gain adjustments. In these circuits, R1, can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 8 (V_{REF-}) of the AD7846 tied to 0V.

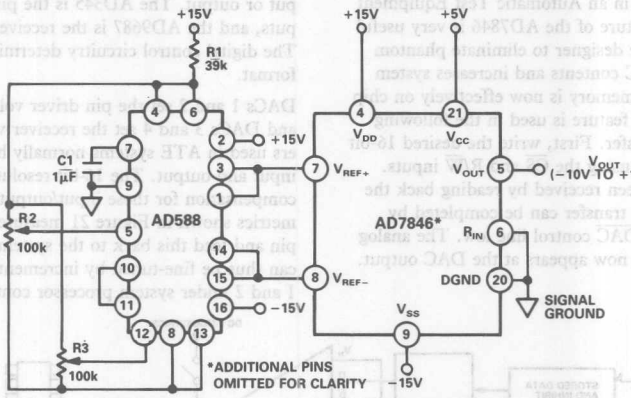


Figure 19. Bipolar ±10V Operation

BIPOLAR OPERATION

Figure 19 shows the AD7846 set up for ±10V bipolar operation. The AD588 provides precision ±5V tracking outputs which are fed to the V_{REF+} and V_{REF-} inputs of the AD7846. The code table for Figure 19 is shown in Table IV.

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	+10 (32767/32768) V
1000 0000 0000 0001	+10 (1/32768) V
1000 0000 0000 0000	0V
0111 1111 1111 1111	−10 (1/32768) V
0000 0000 0000 0000	−10 (32768/32768) V

NOTE
1LSB = 10V/2^{15} = 10V/32768 = 305μV.

Table IV. Offset Binary Code Table for Figure 19

Full scale and bipolar zero adjustment are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the +5V and −5V outputs together with respect to ground.

For bipolar zero adjustment on the AD7846, load the DAC with 100 . . . 000 and adjust R3 until V_{OUT} = 0V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 9.999694V.

When bipolar zero and full scale adjustment are not needed, R2 and R3 can be omitted, Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating. If a user wants a ±5V output range, there are two choices. By tying Pin 6 (R_{IN}) of the AD7846 to V_{OUT} (Pin 5), the output stage gain is reduced to unity and the output range is ±5V. If only a positive +5V reference is available, bipolar ±5V operation is still possible. Tie V_{REF-} to 0V and connect R_{IN} to V_{REF+}. This will also give a ±5V output range. However, the linearity, gain, and offset error specifications will be the same as the unipolar 0 to +5V range.

Other Output Voltage Ranges

In some cases, users may require output voltage ranges other than those already mentioned. One example is systems which need the output voltage to be a whole number of millivolts (i.e. 1mV, 2mV, etc.). If the AD689 (8.192V reference) is used with the AD7846 as in Figure 20, then the LSB size is 125μV. This makes it possible to program whole millivolt values at the output. Table V shows the code table for Figure 20.

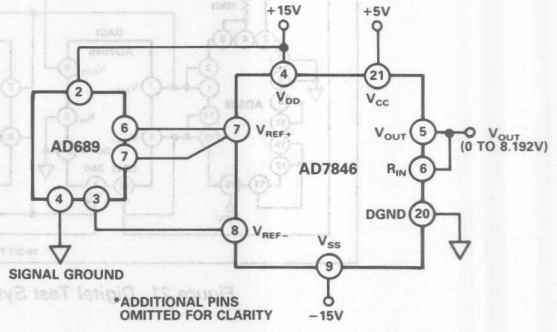


Figure 20. Unipolar Output with AD689

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	8.192V (65535/65536) = 8.1919V
1000 0000 0000 0000	8.192V (32768/65536) = 4.096V
0000 0000 0000 1000	8.192V (8/65536) = 0.001V
0000 0000 0000 0100	8.192V (4/65536) = 0.0005V
0000 0000 0000 0010	8.192V (2/65536) = 0.00025V
0000 0000 0000 0001	8.192V (1/65536) = 0.000125V

NOTE
1LSB = 8.192V/2^{16} = 125μV.

Table V. Code Table for Figure 20

Multiplying Operation

The AD7846 is a full multiplying DAC. To get four-quadrant multiplication, tie V_{REF} to 0V, apply the ac input to V_{REF-} and tie R_{IN} to V_{REF-}. Figure 6 shows the Large Signal Frequency Response when the DAC is used in this fashion.

TEST APPLICATION

Figure 21 shows the AD7846 in an Automatic Test Equipment application. The readback feature of the AD7846 is very useful in these systems. It allows the designer to eliminate phantom memory used for storing DAC contents and increases system reliability since the phantom memory is now effectively on chip with the DAC. The readback feature is used in the following manner to control a data transfer. First, write the desired 16-bit word to the DAC input latch using the $\overline{CS}$ and R/$\overline{W}$ inputs. Verify that correct data has been received by reading back the latch contents. Now, the data transfer can be completed by bringing the asynchronous $\overline{LDAC}$ control line low. The analog equivalent of the digital word now appears at the DAC output.

In Figure 21, each pin on the Device Under Test can be an input or output. The AD345 is the pin driver for the digital inputs, and the AD9687 is the receiver for the digital outputs. The digital control circuitry determines the signal timing and format.

DACs 1 and 2 set the pin driver voltage levels (V_H and V_L), and DACs 3 and 4 set the receiver voltage levels. The pin drivers used in ATE systems normally have a nonlinearity between input and output. The 16-bit resolution of the AD7846 allows compensation for these input/output nonlinearities. The dc parametrics shown in Figure 21 measure the voltage at the device pin and feed this back to the system processor. The pin voltage can thus be fine-tuned by incrementing or decrementing DACs 1 and 2 under system processor control.

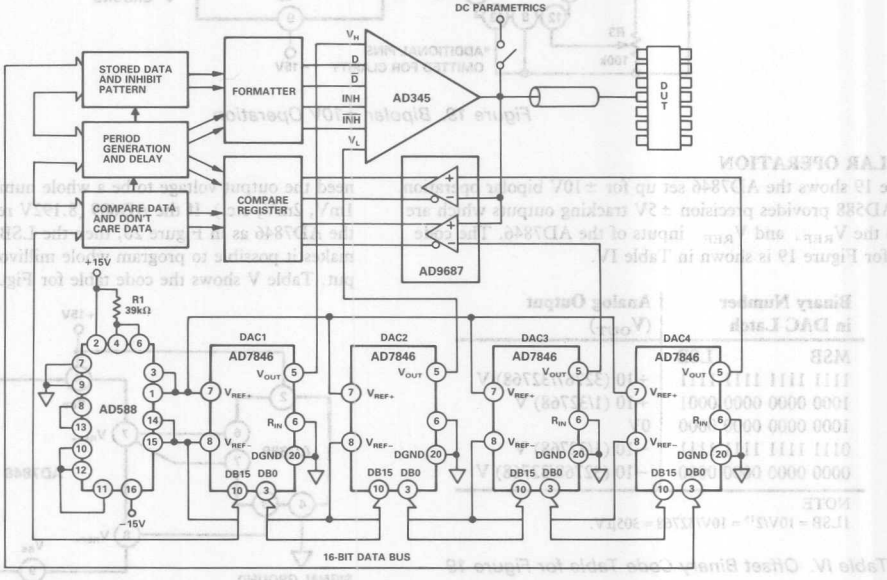


Figure 21. Digital Test System with 16-Bit Performance

POSITION MEASUREMENT APPLICATION

Figure 22 shows the AD7846 in a position measurement application using an LVDT (Linear Variable Displacement Transducer), an AD630 synchronous demodulator and a comparator to make a 16-bit LVDT-to-Digital Convertor. The LVDT is excited with a fixed frequency and fixed amplitude sine wave (usually 2.5kHz, 2V pk-pk). The outputs of the secondary coil are in anti-phase and their relative amplitudes depend on the position of the core in the LVDT. The AD7846 output interpolates between these two inputs in response to the DAC input code. The AD630 is set up so that it rectifies the DAC output signal. Thus, if the output of the DAC is in phase with the V_{REF+} input, the inverting input to the comparator will be positive, and if it is in phase with V_{REF-}, the output will be negative. By turning on each bit of the DAC in succession starting with the MSB, and deciding to leave it on or turn it off based on the comparator output, a 16-bit measurement of the core position is obtained.

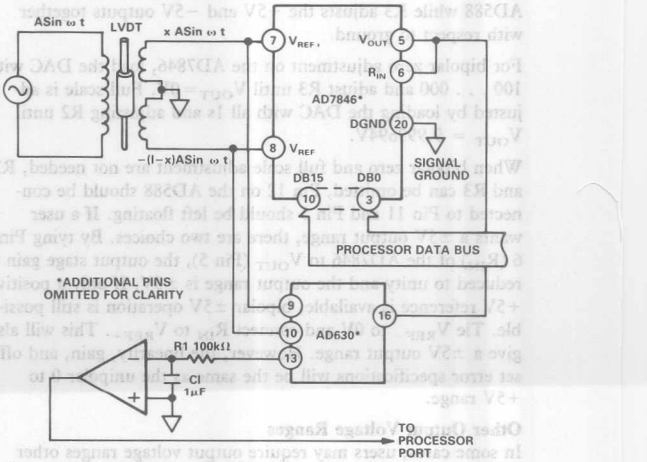


Figure 22. AD7846 in Position Measurement Application

AD7846–8086 Interface

Figure 23 shows the 8086 16-bit processor interfacing to the AD7846. The double buffering feature of the DAC is not used in this circuit since $\overline{LDAC}$ is permanently tied to 0V. AD0–AD15 (the 16-bit data bus) are connected to the DAC data bus (DB0–DB15). The 16-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example, the DAC address is D000H.

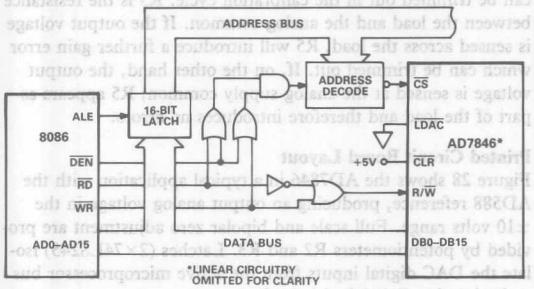


Figure 23. AD7846 to 8086 Interface Circuit

In a multiple DAC system, the double buffering of the AD7846 allows the user to simultaneously update all DACs. In Figure 24, a 16-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

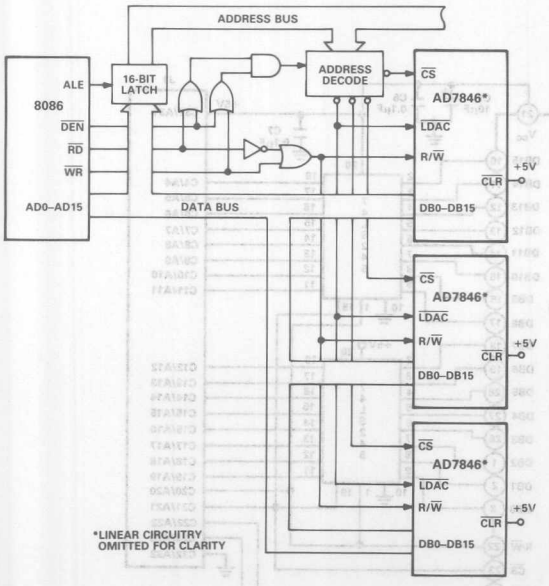


Figure 24. AD7846 to 8086 Interface: Multiple DAC System

Interfacing between the AD7846 and MC68000 is accomplished using the circuit of Figure 25. The following routine writes data to the DAC latches and then outputs the data via the DAC latch.

1000	MOVE.W #W, D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 65535 (decimal) or 0 and FFFF (hexadecimal).
	MOVE.W D0, $E000	The data, W, is transferred between D0 and the DAC register.
	MOVE.W #228, D7	Control is returned to the System Monitor using these two instructions.
	TRAP #14	

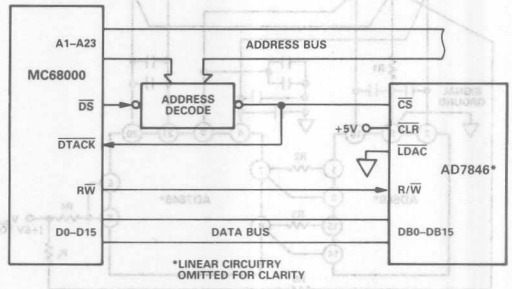


Figure 25. AD7846 to MC68000 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7846 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus

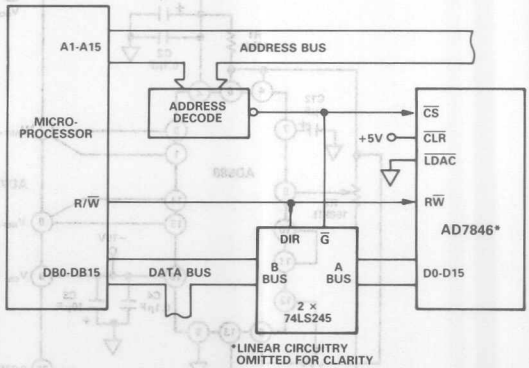


Figure 26. AD7846 Interface Circuit Using Latches to Minimize Digital Feedthrough

noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 26 shows an interface circuit which isolates the DAC from the bus. Note that to make use of the AD7846 readback feature using the isolation technique of Figure 26, the latch needs to be bidirectional.

APPLICATION HINTS

Noise

In high resolution systems, noise is often the limiting factor. With a 10 volt span, a 16-bit LSB is 152μV (−96dB). Thus, the noise floor must stay below −96dB in the frequency range of interest. Figure 7 shows the noise spectral density for the AD7846.

Grounding

As well as noise, the other prime consideration in high resolution DAC systems is grounding. With an LSB size of 152μV and a load current of 5mA, 1LSB of error can be introduced by series resistance of only 0.03Ω.

Figure 27 below shows recommended grounding for the AD7846 in a typical application.

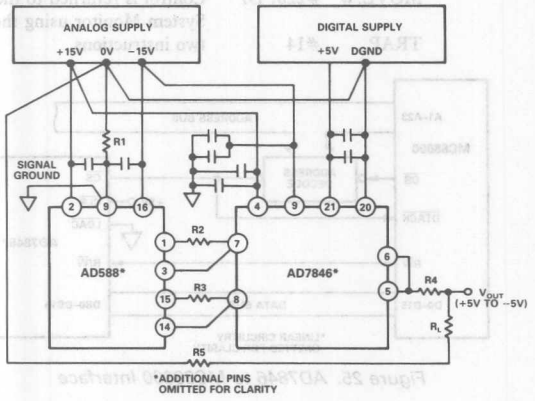


Figure 27. AD7846 Grounding

R1 to R5 represent lead and track resistances on the printed circuit board. R1 is the resistance between the Analog Power Supply ground and the Signal Ground. Since current flowing in R1 is very low (bias current of AD588 sense amplifier), the effect of R1 is negligible. R2 and R3 represent track resistance between the AD588 outputs and the AD7846 reference inputs. Because of the Force and Sense outputs on the AD588, these resistances will also have a negligible effect on accuracy.

R4 is the resistance between the DAC output and the load. If R_L is constant, then R4 will introduce a gain error only which can be trimmed out in the calibration cycle. R5 is the resistance between the load and the analog common. If the output voltage is sensed across the load, R5 will introduce a further gain error which can be trimmed out. If, on the other hand, the output voltage is sensed at the analog supply common, R5 appears as part of the load and therefore introduces no errors.

Printed Circuit Board Layout

Figure 28 shows the AD7846 in a typical application with the AD588 reference, producing an output analog voltage in the ±10 volts range. Full scale and bipolar zero adjustment are provided by potentiometers R2 and R3. Latches (2×74LS245) isolate the DAC digital inputs from the active microprocessor bus and minimize digital feedthrough.

The printed circuit board layout for Figure 28 is shown in Figures 29 and 30. Figure 29 is the component side layout while Figure 30 is the solder side layout. The component overlay is shown in Figure 31.

In the layout, the general grounding guidelines given in Figure 27 are followed. The AD588 and AD7846 are as close as possible, and the decoupling capacitors for these are also kept as close to the device pins as possible.

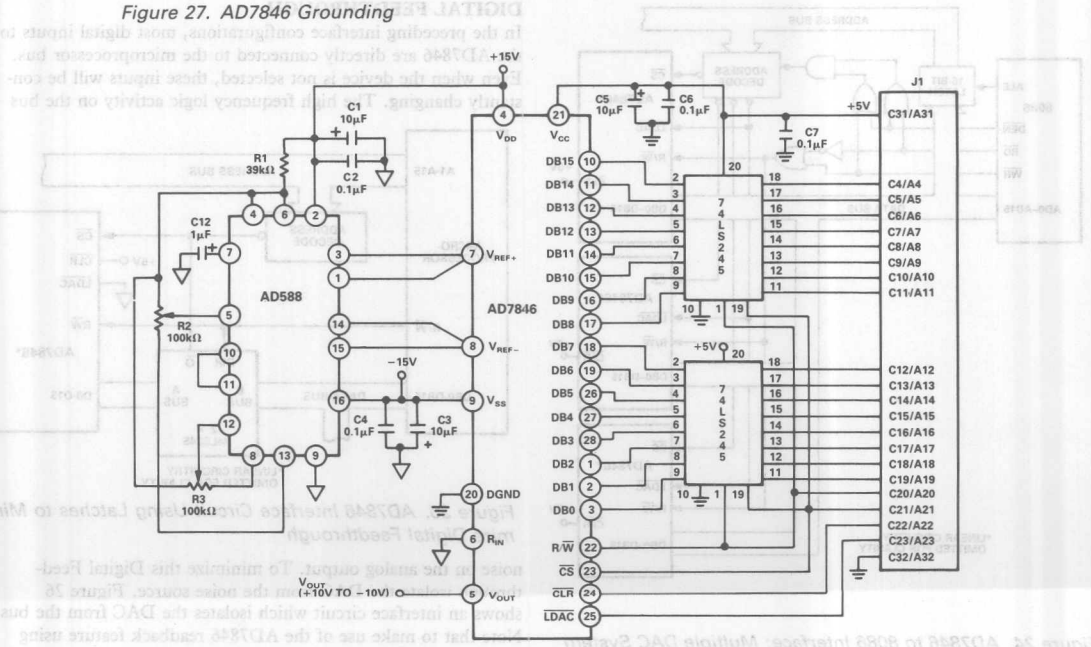


Figure 28. Schematic for AD7846 Board

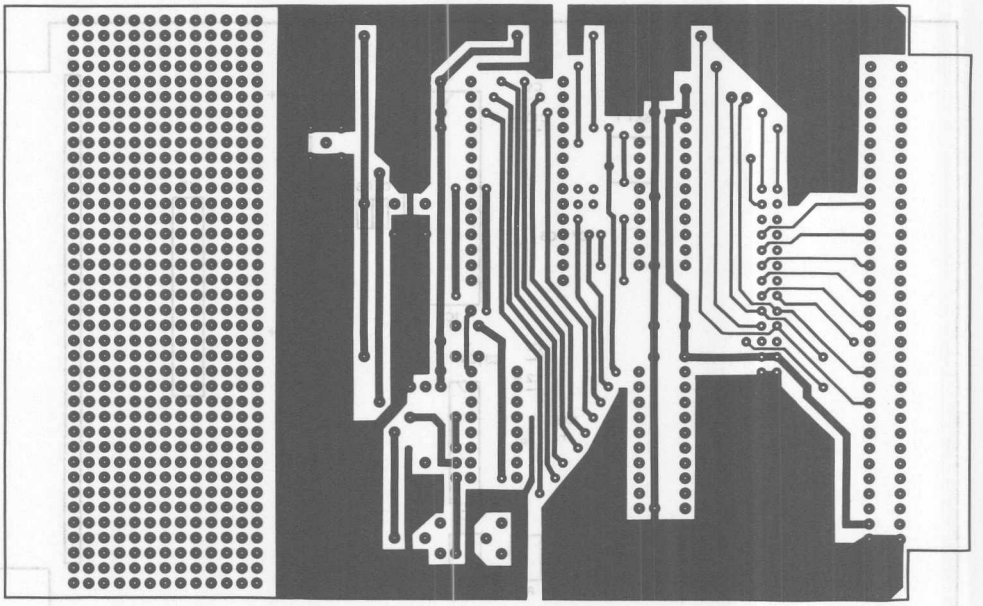


Figure 29. PCB Component Side Layout for Figure 28

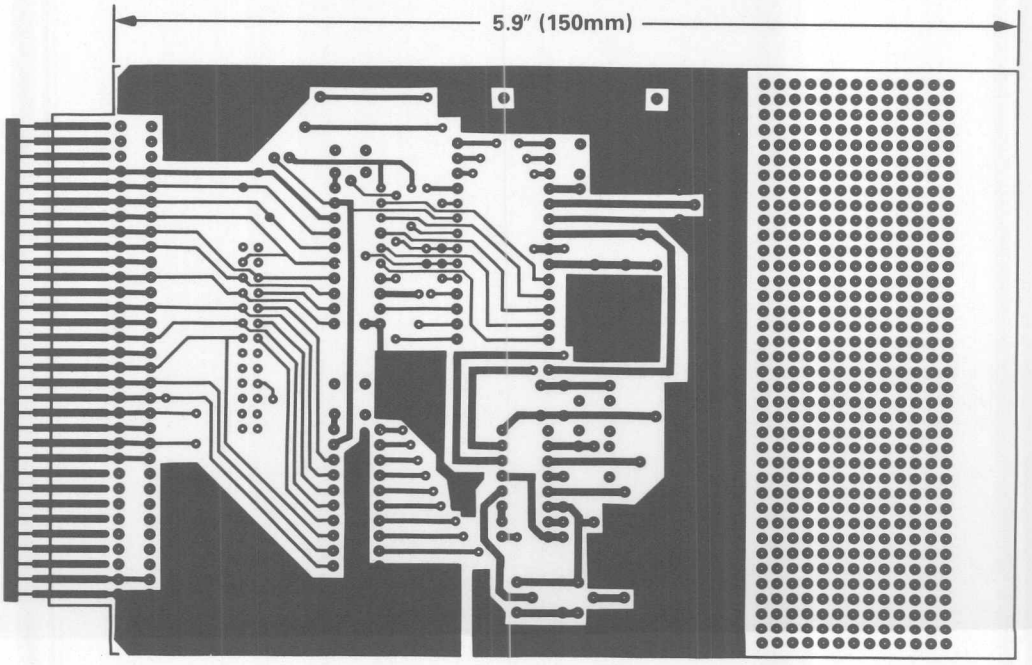


Figure 30. PCB Solder Side Layout for Figure 28

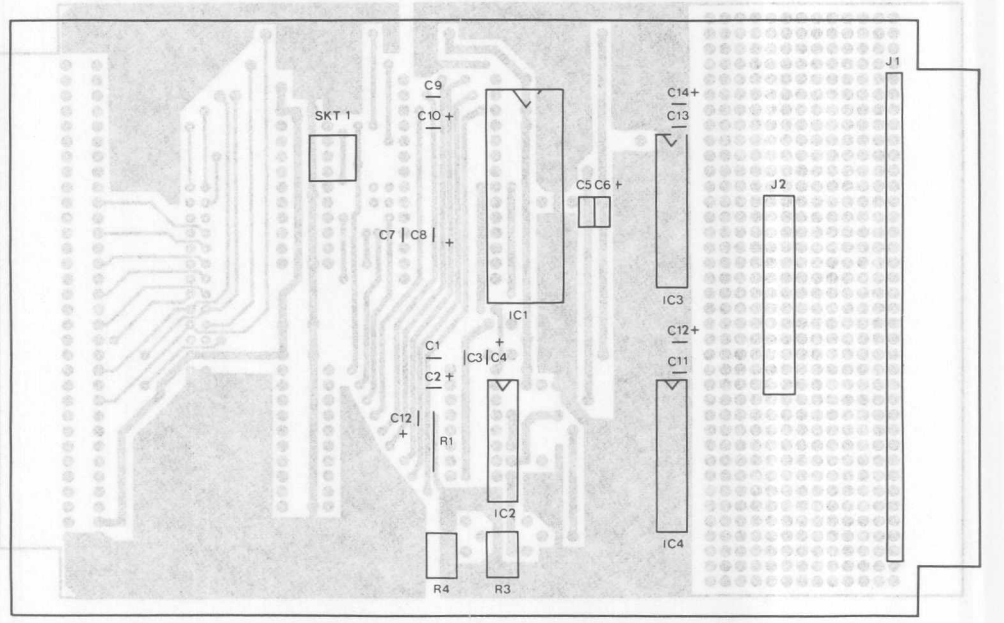


Figure 31. Component Overlay for Circuit of Figure 28

FEATURES

Complete DAC with DSP Interface, Comprising:
- **12-Bit Voltage Mode DAC**
- **3 V Zener Reference**
- **Output Buffer Amplifier with 4 μs Settling Time**
- **8 Word FIFO and Interface Logic**

72 dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS320C25, TMS32010
42 ns min $\overline{WR}$ Pulse Width
Low Power −60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Synthesis
High Speed Modems
DSP Servo Control When Used with AD7878

GENERAL DESCRIPTION

The AD7848 is a fast, complete, 12-bit, voltage output D/A converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

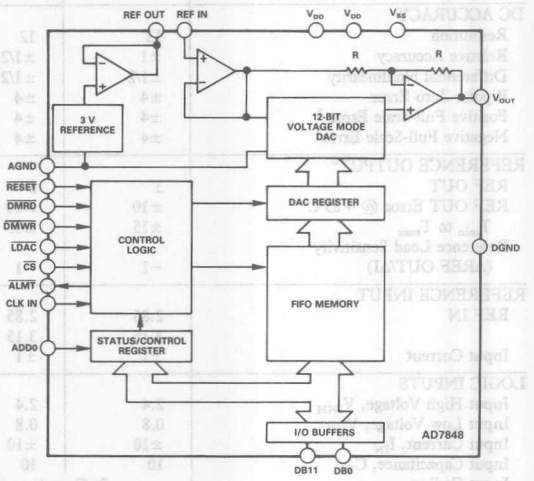
The FIFO memory allows up to eight samples to be loaded to the AD7848 at full microprocessor speed. The samples are then loaded to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 20 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains FIFO empty, FIFO full and FIFO word count information.

The analog output from the AD7848 provides a bipolar output range of ±3 V. Full power output signals up to 20 kHz can be created and the AD7848 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion.

The AD7848 is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology, process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic and hermetic dual-in-line package (DIP) and in a 28-terminal plastic leaded chip carrier (PLCC).

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Complete D/A Function with DSP Interface
   The AD7848 provides the complete function for creating ac signals to 12-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 12-bit D/A converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing peripherals in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7848 is fully specified and tested for ac parameters, including signal-to-noise ratio and harmonic distortion.
3. Fast Microprocessor Interface
   Data setup times of 20 ns and write pulse widths of 42 ns make the AD7848 compatible with all modern 16-bit microprocessors and digital signal processors. Key digital timing parameters are also tested and specified over the full operating temperature range.

AD7848—SPECIFICATIONS

(V_{DD} = 5 V±5%, V_{SS} = −5 V±5%, AGND = DGND = 0V, REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF, f_{CLK} = 10 MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions[1]	K, B Versions	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to Noise Ratio[3] (SNR) @ +25°C	70	72	dB min	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	70	dB min	Typically 72 dB at +25°C for 0<f_{OUT}<20 kHz[4]
Total Harmonic Distortion (THD)	−80	−80	dB typ	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −80 dB at +25°C for 0<f_{OUT}<20 kHz[4]
Peak Harmonic or Spurious Noise	−80	−80	dB typ	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −80 dB at +25°C for 0<f_{OUT}<20 kHz[4]
DC ACCURACY				
Resolution	12	12	Bits	
Relative Accuracy	±1	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	LSB typ	Guaranteed Monotonic
Bipolar Zero Error	±4	±4	LSB max	
Positive Full-Scale Error[5]	±4	±4	LSB max	
Negative Full-Scale Error[5]	±4	±4	LSB max	
REFERENCE OUTPUT[6]				
REF OUT	3	3	V nom	
REF OUT Error @ +25°C	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT				
REF IN	2.85	2.85	V min	
	3.15	3.15	V max	
Input Current	±1	±1	μA max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V±5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V±5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	pF max	
Input Coding	2s Complement			
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	2.7	2.7	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating State Leakage Current	10	10	μA max	
Floating State Output Capacitance[7]	15	15	pF max	
ANALOG OUTPUT				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.2	0.2	Ω typ	
Short Circuit Current	25	25	mA typ	
AC CHARACTERISTICS[7]				
Voltage Output Settling Time[8]				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	
Negative Full-Scale Change	4	4	μs max	
Digital-to-Analog Glitch Impulse[8]	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough[8]	2	2	nV secs typ	
CLK IN Feedthrough	2	2	mV typ	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	mA max	CS = DMWR = DMRD = Data Inputs = 5 V; Output Unloaded
I_{SS}	6	6	mA max	CS = DMWR = DMRD = Data Inputs = 5 V; Output Unloaded
Power Dissipation	95	95	mW max	Typically 60 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions, 0 to +70°C; A, B Versions, −25°C to +85°C.
[2]V_{OUT} = ±3 V.
[3]SNR includes distortion and noise components.
[4]Using external sample-and-hold (see Testing the AD7848).
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Sample tested @ +25°C to ensure compliance.
[8]Measured with CLK IN stopped.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V±5%, V_{SS} = −5 V±5%, AGND=DGND=0 V)

Parameter	Limit at T_{min}, T_{max} (J, A, Versions)	Limit at T_{min}, T_{max} (K, B Versions)	Units	Conditions/Comments
t_1	42	42	ns min	INTERNAL WRITE Pulse Width
t_2	5	5	ns min	ADD0 to INTERNAL WRITE Setup Time
t_3	0	0	ns min	ADD0 to INTERNAL WRITE Hold Time
t_4	t_1–12 or 50[2]	t_1–22 or 50[2]	ns min	Data Valid to INTERNAL WRITE Setup Time
t_5	10	10	ns min	Data Valid to INTERNAL WRITE Hold Time
t_6	1.5 CLK IN Cycles	1.5 CLK IN Cycles	min	$\overline{LDAC}$ Pulse Width
t_7	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Setup Time
t_8	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Hold Time
t_9	60	45	ns min	$\overline{DMRD}$ Pulse Width
t_{10}[3]	57	41	ns max	Data Access Time after $\overline{DMRD}$
t_{11}[4]	5	5	ns min	Bus Relinquish Time
	45	45	ns max	

NOTES
[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]The smaller number of these two is the required data setup time, i.e., for narrower write pulses a shorter setup time is required.
[3] t_{10} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_{11} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

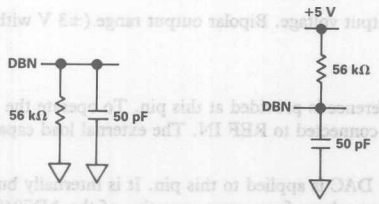
V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND . . . . . V_{SS}−0.3 V to V_{DD}+0.3 V
REF IN to AGND . . . . . −0.3 V to V_{DD}+0.3 V
REF OUT to AGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

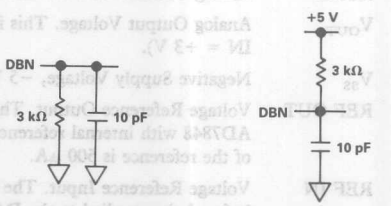
Model	Temperature Range	SNR (dBs)	Package Option*
AD7848JN	0°C to +70°C	70 min	N-28
AD7848KN	0°C to +70°C	72 min	N-28
AD7848JP	0°C to +70°C	70 min	P-28A
AD7848KP	0°C to +70°C	72 min	P-28A
AD7848AQ	−25°C to +85°C	70 min	Q-28
AD7848BQ	−25°C to +85°C	72 min	Q-28

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information, see Package Information section.



a. High-Z to V_{OH} b. V_{OL} to High-Z

Figure 1. Load Circuits for Access Time



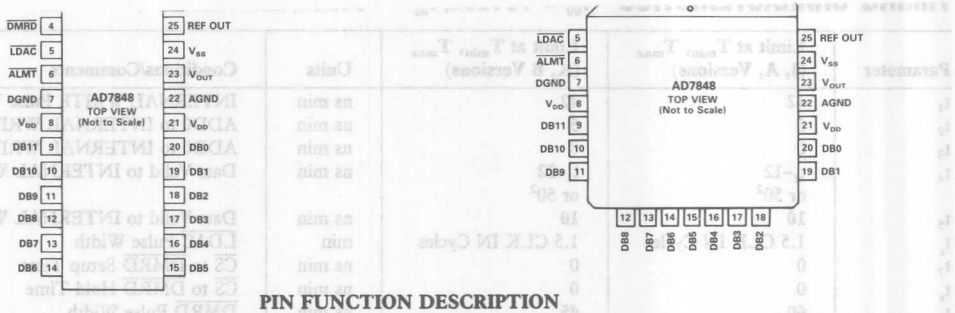
a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.





PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	ADD0	Address Input. This input determines whether the word on the data bus during a write operation is loaded to the FIFO RAM or to the status/control register. A logic low selects the FIFO memory, while a logic high selects the status/control register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ to write data to either the FIFO memory or the status/control register. Corresponds directly to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS320C25), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory Read. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to access data from the status/control register. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded to the DAC register from FIFO memory Location 0 on the falling edge of this signal. The $\overline{LDAC}$ input is asynchronous to CLK IN and is independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$. A software $\overline{LDAC}$ can be performed by writing to the control register (see STATUS/ CONTROL REGISTER section).
6	$\overline{ALMT}$	FIFO Almost Empty. A logic low indicates that the word count (i.e., number of data words in the FIFO) has reached the programmed almost empty word count in the status/control register. $\overline{ALMT}$ is updated after every $\overline{LDAC}$ operation. The $\overline{ALMT}$ output can be disabled (i.e., set to a logic high) by writing a Logic 1 to DB7 ($\overline{ENAL}$) of the status/control register. The $\overline{ALMT}$ status can also be obtained by reading the status register (see STATUS/CONTROL REGISTER section).
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{DD}	Positive Supply Voltage, +5 V±5%.
9–20	DB11–DB0	Data Bit 11 (MSB) to DB0 (LSB). Three-state TTL input/outputs. Coding for data words is 2s complement.
21	V_{DD}	Positive Supply Voltage, +5 V±5%. Same as Pin 8; both pins must be tied together at the package.
22	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
23	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3 V with REF IN = +3 V).
24	V_{SS}	Negative Supply Voltage, −5 V±5%.
25	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. To operate the AD7848 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500 μA.
26	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7848 is 3 V.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low clears the words in the FIFO memory and the contents of the DAC register to 0000 0000 0000 and resets the status/control register and control logic.
28	CLK IN	Clock Input. TTL compatible logic input. Used as the clock source for all internal dynamic logic and provides synchronization during bus transactions. The mark/space ratio of this clock can vary from 35/65 to 65/35 provided the INTERNAL WRITE timing is obeyed (see READ/WRITE Operations section).

Table I. Status/Control Bit Function Description

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{\text{ALMT}}$	AEC2	AEC1	AEC0	$\overline{\text{ENAL}}$	$\overline{\text{FFUL}}$	0	FEMP	FUND	FC2	FC1	FC0
CONTROL FUNCTION (WRITE)	X	AEC2	AEC1	AEC0	$\overline{\text{ENAL}}$	RESET	$\overline{\text{LDAC}}$	X	X	X	X	X
RESET STATUS	0	0	0	0	0	1	0	1	0	0	0	0

X = DON'T CARE

STATUS/ CONTROL REGISTER

The AD7848 contains two on-chip registers – a status register for monitoring the status of the FIFO memory and a control register to provide control for the FIFO memory functions. Because both registers reside at the same address and much of the information is common to both they are treated here as a common status/control register. Read operations from the status/control register access data from the status register, while write operations are to the control register.

The register is directly accessible through the data bus (DB11–DB0) with a read or a write operation when ADD0 is high. A write operation provides control for the $\overline{\text{ALMT}}$ output, DAC register updates and FIFO word count reset. This is normally done on power-up initialization. The FIFO memory address pointer is decremented after every DAC register update and this pointer is compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{\text{ALMT}}$ output is asserted if the $\overline{\text{ENAL}}$ control bit is set to 0. This $\overline{\text{ALMT}}$ can be used to interrupt the microprocessor after any predetermined number of DAC register updates (between 1 and 8). The status of the address pointer, along with FIFO underflow, FIFO empty and $\overline{\text{ALMT}}$ status can be accessed at any time by reading the status/control register. Note, reading from the status/control register does not cause any internal movement in the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 (ALMT)

Almost Empty Flag. Read only. This is the same as the Pin 6 ($\overline{\text{ALMT}}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed word count in bit locations DB10–DB8. $\overline{\text{ALMT}}$ is updated at the end of an $\overline{\text{LDAC}}$ operation. $\overline{\text{ALMT}}$ is active following a device reset because both the FIFO word count and the almost empty word count are 000.

DB10–DB8 (AEC2–AEC0)

Almost Empty Word Count. Read/Write. The count value determines the number of words in the FIFO memory which will cause $\overline{\text{ALMT}}$ to be set. When the FIFO word count equals the programmed count in these three bits, then both the $\overline{\text{ALMT}}$ output and DB11 of the status/control register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{\text{ALMT}}$ is set when only Location 0 through Location 3 of the FIFO memory contain valid data. AEC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{\text{ENAL}}$)

Enable Almost Empty. Read/Write. Writing a 1 to this bit disables the $\overline{\text{ALMT}}$ output and status/control register bit DB11.

DB6 (FFUL/RESET)

FIFO Full/Reset. Read/Write. Reading a 0 from this bit indicates that there are 8 words in the FIFO memory (i.e. the FIFO is full). Writing a 1 to this bit location will cause a system reset as per the $\overline{\text{RESET}}$ input (Pin 27).

DB5 ($\overline{\text{LDAC}}$)

Load DAC. Write only. Writing a 0 to this location causes the sample in Location 0 of the FIFO to be loaded into the DAC register. The function of this bit is the same as the $\overline{\text{LDAC}}$ input (Pin 5).

DB4 (FEMP)

FIFO Empty. Read only. Reading a 1 indicates that there are no words in FIFO memory. When the FIFO is empty, any further $\overline{\text{LDAC}}$ operations will continue to update the DAC register with the contents of Location 0 of the FIFO.

DB3 (FUND)

FIFO Underflow. Read only. If the FIFO memory is empty and further DAC register updates occur, then this bit is set to a 1. It will remain set until an $\overline{\text{LDAC}}$ operation occurs with valid data in FIFO Location 0.

DB2–DB0 (FC2–FC0)

FIFO Word Count. Read only. The value read from these bits indicates the number of words in FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contain valid data. Note, reading all 0s indicates that there is either one word or no word in the FIFO memory; in this case, the FIFO Empty determines if there is no word in memory. FC2 is the most significant bit.

D/A SECTION

The AD7848 contains a 12-bit voltage output D/A converter consisting of highly stable thin film resistors and high speed NMOS single pole, double throw switches. The simplified circuit diagram for the DAC section is shown in Figure 3. The three MSBs of the data word are decoded to drive the seven switches A-G. The 9 LSBs switch a 9-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

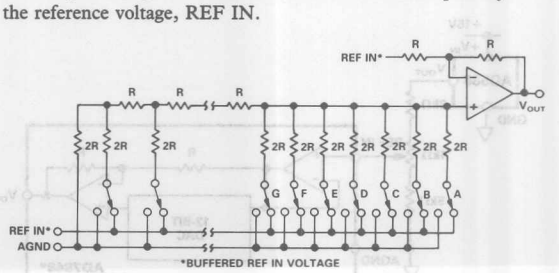


Figure 3. DAC Ladder Structure

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3 V reference and the device is tested with 3 V applied to REF IN. Operating the AD7848 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

INTERNAL REFERENCE

The AD7848 has an on-chip temperature compensated buried Zener reference (see Figure 4) which is factory trimmed to 3 V± 10 mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

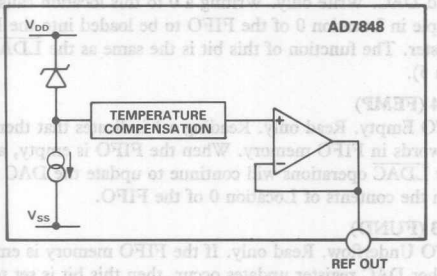


Figure 4. Internal Reference

The reference voltage can also be used as a reference for other components in the system and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

EXTERNAL REFERENCE

In some applications the user may require a system reference or some other external reference to drive the AD7848 reference input. Figure 5 shows how the AD586 5 V reference can be conditioned to provide the 3 V reference required by the AD7848 REF IN. An alternate source of reference voltage for the AD7848 in systems which use both a DAC and an ADC is to use the REF OUT voltage of an ADC such as the AD7878. A circuit showing this arrangement is outlined in Figure 16.

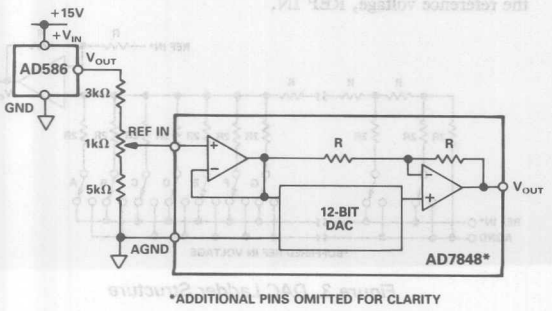


Figure 5. AD586 Driving AD7848 REF IN

OP AMP SECTION

The output from the converter is buffered by a noninverting amplifier. Internal scaling resistors on the AD7848 configure the output voltage for ±3 V from an input reference voltage of +3 V. Figure 5 shows the arrangement of these resistors around the output op amp. The buffer amplifier is capable of developing ±3 V across a 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals up to a frequency of 20 kHz.

The output is updated on the falling edge of the $\overline{LDAC}$ input. For a software DAC update, the output is updated on the next rising clock edge after receiving a software $\overline{LDAC}$. The amplifier settles to within 1/2 LSB of its final value in typically less than 2 μs for a full-scale output change.

TRANSFER FUNCTION

The basic circuit configuration for the AD7848 is shown in Figure 6. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1 LSB = FS/4096 = 6 V/4096 = 1.465 mV. The output voltage, V_{OUT}, can be expressed in terms of the input code, N, using the following relationship:

$$V_{OUT} = \frac{2 \cdot N \cdot REF\ IN}{4096} \quad -2048 \leq N \leq +2047$$

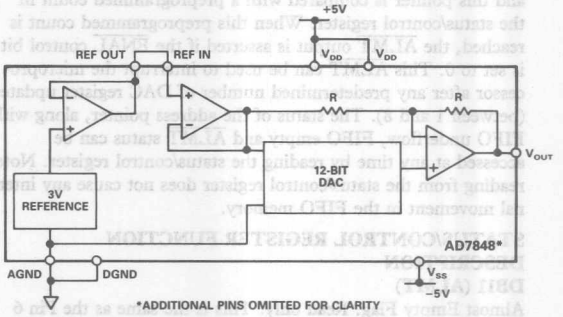


Figure 6. Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0111 1111 1111	+2.998535 V
0111 1111 1110	+2.99707 V
0000 0000 0001	+0.001465 V
0000 0000 0000	0 V
1111 1111 1111	−0.001465 V
1000 0000 0001	−2.998535 V
1000 0000 0000	−3 V

*Assuming REF IN = +3 V.

Table II. Ideal Input/Output Code Table

INTERNAL FIFO MEMORY

The internal FIFO memory of the AD7848 consists of eight memory locations, each memory location 12 bits wide. A block diagram of the AD7848 FIFO architecture is shown in Figure 7.

Data is loaded to the FIFO under control of $\overline{CS}$ and $\overline{DMWR}$. The FIFO Address Pointer always points to the top of memory i.e., the uppermost location which contains valid data. This pointer is incremented when a new word is loaded to the FIFO

from the data bus. Data is loaded from the FIFO to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. When $\overline{LDAC}$ is asserted, the data contained in the bottom location of the FIFO (Location 0) is transferred to the DAC register. On completion of this transfer operation, each word in the FIFO moves down one location and the Address Pointer is decremented by one. Therefore, each data word enters at the top of memory, propagates down with successive $\overline{LDAC}$ operations until it reaches Location 0 from where it can be transferred to the DAC register.

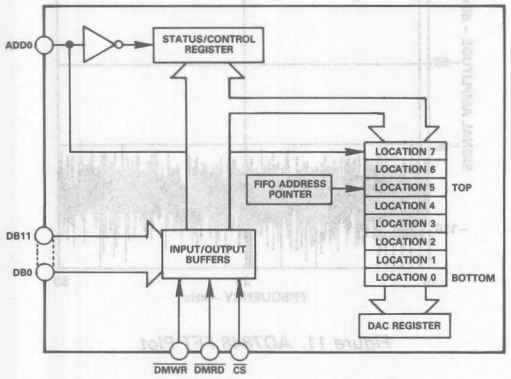


Figure 7. Internal FIFO Architecuture

The propagation of data words down the FIFO occurs in synchronization with the AD7848 input clock (CLK IN). As a result, a write operation to the FIFO memory must also be synchronous with CLK IN. If the write operation is not synchronous with a CLK IN cycle or if the $\overline{DMWR}$ line goes low within 20 ns prior to a rising edge of CLK IN, the AD7848 logic will stop operating correctly. This means that in systems where the AD7848 CLK IN is not derived from the microprocessor clock, the CLK IN and $\overline{DMWR}$ signals will have to be synchronized externally.

The updating of the status register following data movements in the FIFO also occurs in synchronization with CLK IN. The status register is updated on the next rising CLK IN edge after $\overline{DMWR}$ goes low. A setup time of 70 ns is required between the falling edge of $\overline{DMWR}$ and the rising edge of CLK IN to ensure that the status register update takes place on that rising edge; otherwise the update will slip to the next rising edge of CLK IN. If the AD7848 is operated with a $\overline{DMWR}$ to CLK IN setup time of less than 70 ns, the updating of the status register does not take place on the same clock cycle but data is written correctly to the FIFO. This means that in these situations the status register should not be read during the CLK IN cycle following the write operation. To get the correct information, the user will have to allow one clock cycle between the write and read operations.

READ/WRITE OPERATIONS

The AD7848 read/write operations consist of writing to the FIFO memory and status/control register and reading from the status/control register. These operations are controlled by the $\overline{CS}$, $\overline{DMWR}$, $\overline{DMRD}$ and *ADD0* logic inputs.

Write Operation

A write operation to the AD7848 FIFO memory consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 low. Internally, these signals are gated with CLK IN to provide an INTERNAL WRITE signal (see Figure 8). The pulse width of this INTERNAL WRITE signal is effectively the overlap between the CLK IN low time and the $\overline{CS}$ and $\overline{DMWR}$ pulses. This may result in shorter write pulse widths, setup times and data hold times than those given by a microprocessor. The timing on the AD7848 timing diagram of Figure 9 is therefore given with respect to the INTERNAL WRITE signal rather than the $\overline{DMWR}$ signal. A similar situation exists for writing information to the AD7848 status/control register. A write operation to the status/control register consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 high.

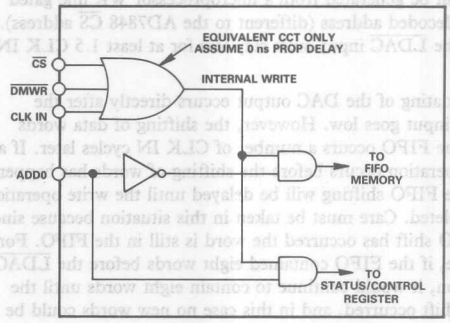


Figure 8. $\overline{DMWR}$ Internal Logic

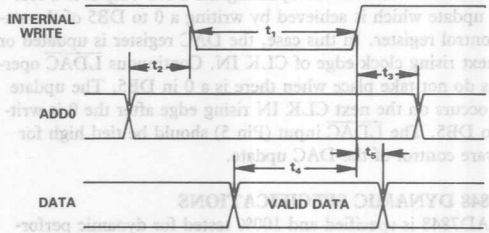


Figure 9. AD7848 Write Operation

Data is internally latched to the FIFO memory on the rising edge of CLK IN after $\overline{DMWR}$ goes low. Keeping $\overline{DMWR}$ low for numerous CLK IN cycles does not result in numerous FIFO write operations. Data is written on the first rising CLK IN edge after $\overline{DMWR}$ goes low.

Read Operation

Figure 10 shows the timing diagram for a read operation from the status/control register of the AD7848. $\overline{CS}$ and $\overline{DMRD}$ going low accesses data from the status/control register. The ADD0 line can either be high or low for a read from the status/control register.

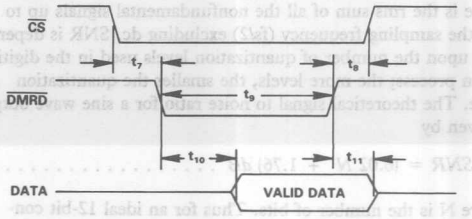


Figure 10. AD7848 Read Operation

UPDATING THE DAC OUTPUT

The DAC output on the AD7848 can be updated under software or hardware control. For hardware control, the output is updated by asserting the $\overline{LDAC}$ input; for software control, writing a 0 to DB5 of the status/control register updates the output.

The $\overline{LDAC}$ input is an asynchronous input which is independent of CLK IN. This is essential for applications where precise sampling in time is important. In these applications, the signal update must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases, the $\overline{LDAC}$ input is driven from a timer or some precise clock source.

In applications where precise sampling is not critical, the $\overline{LDAC}$ pulse can be generated from a microprocessor $\overline{WR}$ line gated with a decoded address (different to the AD7848 $\overline{CS}$ address). Note, the $\overline{LDAC}$ input must stay low for at least 1.5 CLK IN cycles.

The updating of the DAC output occurs directly after the $\overline{LDAC}$ input goes low. However, the shifting of data words down the FIFO occurs a number of CLK IN cycles later. If a write operation occurs before the shifting of words has happened then the FIFO shifting will be delayed until the write operation is completed. Care must be taken in this situation because since no FIFO shift has occurred the word is still in the FIFO. For example, if the FIFO contained eight words before the $\overline{LDAC}$ operation, it would continue to contain eight words until the FIFO shift occurred, and in this case no new words could be written to the FIFO.

The alternative method for updating the DAC output is a software update which is achieved by writing a 0 to DB5 of the status/control register. In this case, the DAC register is updated on the next rising clock edge of CLK IN. Continuous $\overline{LDAC}$ operations do not take place when there is a 0 in DB5. The update only occurs on the next CLK IN rising edge after the 0 is written to DB5. The $\overline{LDAC}$ input (Pin 5) should be tied high for software control of the DAC update.

AD7848 DYNAMIC SPECIFICATIONS

The AD7848 is specified and 100% tested for dynamic performance specifications rather than traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as Speech Synthesis, Servo Control and High Speed Modems. These applications require information on the DAC's effect on the spectral content of the signal it is creating. Hence, the parameters for which the AD7848 is specified include Signal-to-Noise Ratio, Harmonic Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave output is given by

$$SNR = (6.02\,N + 1.76)\,dB \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

Figure 11 shows a typical 2048 point Fast Fourier Transform (FFT) plot of the AD7848KN with an output frequency of 1 kHz and an update rate of 100 kHz. The SNR obtained from this graph is 73.3 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

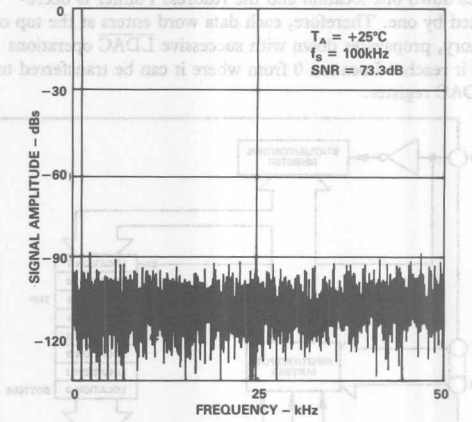


Figure 11. AD7848 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N_{EFF}).

$$N_{EFF} = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7848, THD is defined as

$$THD = 20\,Log\,\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the 2048-point FFT plot.

Peak Harmonic or Spurious Noise

Peak Harmonic or Spurious Noise is defined as the ratio of the rms value of the next largest component in the DAC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

Testing the AD7848

The method used to test the dynamic performance specifications is outlined in Figure 12. Data is loaded to the AD7848 under control of the microcontroller and associated logic. The output of the AD7848 is applied to a 9th order low-pass filter. The output of the filter is in turn applied to a 14-bit accurate digitizer. The digitizer samples the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7848 can be evaluated.

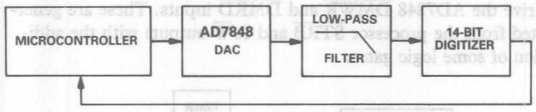


Figure 12. AD7848 Dynamic Performance Test Circuit

The digitizer's sampling is synchronized with the AD7848 update rate to ease FFT calculations. The digitizer samples the AD7848 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly; it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7848 would not be measured correctly, giving better results than the actual performance of the AD7848. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7848 is measured.

Some applications will require improved performance versus frequency from the AD7848. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 13 will extend the very good performance of the AD7848 to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7848. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance of the AD7848.

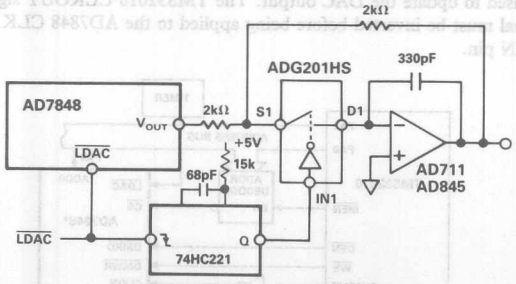


Figure 13. Sample-and-Hold Circuit

Performance versus Frequency

The typical performance plots of Figures 14 and 15 show the performance of the AD7848 over a wide range of input frequencies. The plot of Figure 14 is without a sample-and-hold on the output while the plot of Figure 15 is generated with the sample-and-hold circuit of Figure 13 on the output.

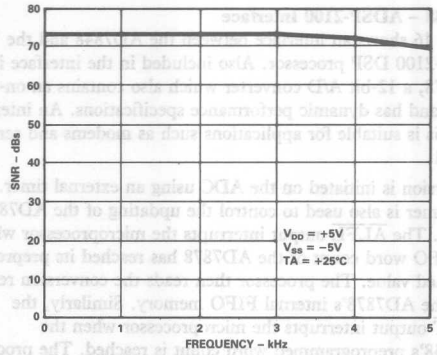


Figure 14. Performance vs. Frequency (No Sample-and-Hold)

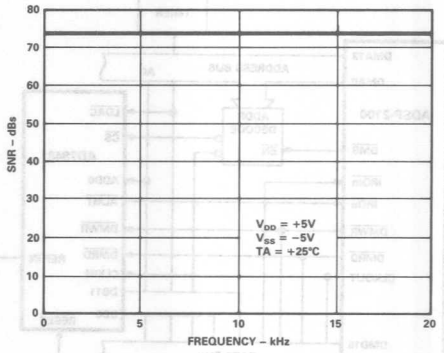


Figure 15. Performance vs. Frequency (with Sample-and-Hold)

MICROPROCESSOR INTERFACING

The AD7848 high speed bus timing allows direct interfacing to DSP processors. Due to the complexity of the AD7848 internal logic, only synchronous interfacing is allowed. This means that the AD7848 CLK IN must be the same as or a derivative of the processor clock. In applications where this is not possible, the CLK IN and $\overline{DMWR}$ signals must be externally gated. Suitable processor interfaces are shown in Figures 16 to 19.

AD7848 – ADSP-2100 Interface

Figure 16 shows an interface between the AD7848 and the ADSP-2100 DSP processor. Also included in the interface is the AD7878, a 12-bit A/D converter which also contains an on-chip FIFO and has dynamic performance specifications. An interface like this is suitable for applications such as modems and servo control.

Conversion is initiated on the ADC using an external timer. This timer is also used to control the updating of the AD7848 output. The $\overline{ALFL}$ output interrupts the microprocessor when the FIFO word count of the AD7878 has reached its preprogrammed value. The processor then reads the conversion results from the AD7878's internal FIFO memory. Similarly, the $\overline{ALMT}$ output interrupts the microprocessor when the AD7848's preprogrammed word count is reached. The processor then loads another batch of samples to the AD7848's internal FIFO memory.

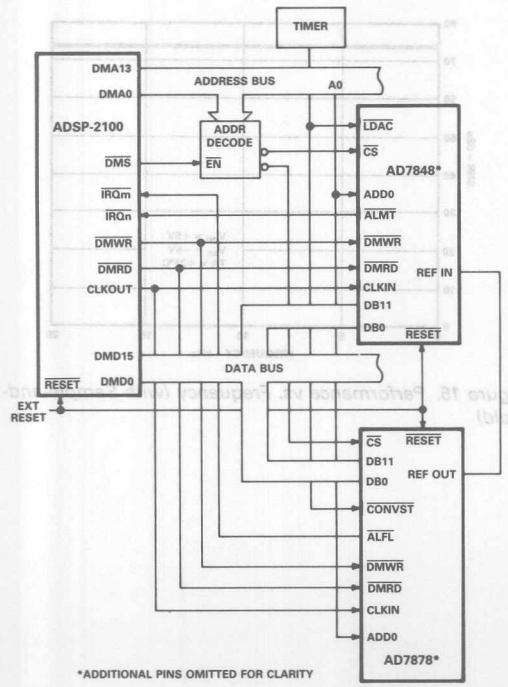


Figure 16. AD7848/AD7878 – ADSP-2100 Interface

AD7848 – TMS320C25 Interface

An interface between the AD7848 and the TMS320C25 DSP processor is shown in Figure 17. As in the previous interface, the updating of the AD7848 output is controlled by an external timer. The $\overline{ALMT}$ output of the AD7848 provides an interrupt signal to the TMS320C25. The TMS320C25 CLKOUT2 signal must be inverted before being applied to the AD7848 CLK IN pin. A single WAIT state is inserted in a read cycle to the AD7848 status/control register via the TMS320C25 READY input.

The TMS320C25 does not have separate $\overline{RD}$ and $\overline{WR}$ outputs to drive the AD7848 $\overline{DMWR}$ and $\overline{DMRD}$ inputs. These are generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

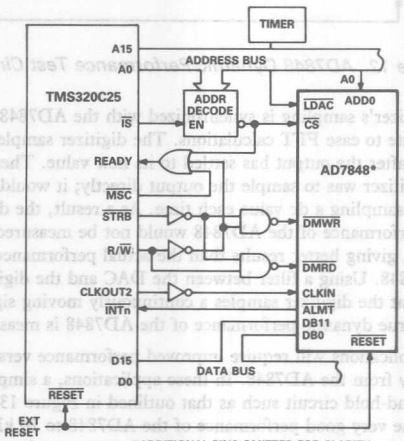


Figure 17. AD7848 – TMS320C25 Interface

AD7848 – TMS32010 Interface

Figure 18 shows an interface between the AD7848 and the TMS32010 DSP processor. Once again, an external timer is used to update the DAC output. The TMS32010 CLKOUT signal must be inverted before being applied to the AD7848 CLK IN pin.

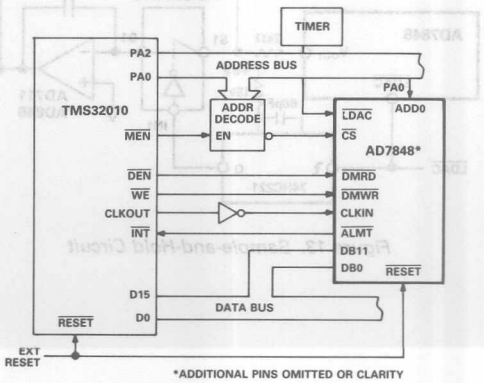


Figure 18. AD7848 – TMS32010 Interface

AD7848 – MC68000 Interface

This interface also uses an external timer for updating the analog output as described in the previous three interfaces. It differs from the other interfaces because it needs extra logic due to the nature of its interrupts. The MC 68000 has eight levels of external interrupt. When interrupting this processor one of these levels (0 to 7) has to be encoded onto the IPL2–IPL0 inputs. This is achieved with a 74148 encoder in Figure 19, (interrupt level 1 is taken for example purposes only). The $\overline{ALMT}$ output drives the appropriate input of the 74148 for the required interrupt level. The MC68000 places this interrupt level on address bits A3 to A1 at the start of the interrupt service routine. Additional logic is used to decode this interrupt level on the address bus and the FC2–FC0 outputs to generate a VPA signal for the MC68000. This results in an autovectored interrupt; the start address for the service routine must be loaded into the appropriate auto vector location during initialization. For further information on the 68000 interrupts consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate separate $\overline{DMWR}$ and $\overline{DMRD}$ inputs for the the AD7848. Since the $\overline{UDS}$ line is used to decode the $\overline{DMWR}$ and $\overline{DMRD}$ signals, the AD7848 is memory-mapped at an even address.

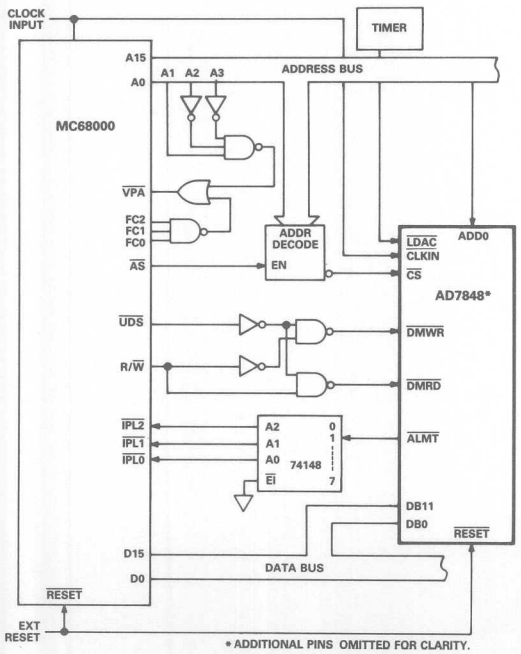


Figure 19. AD7848 – MC68000 Interface

APPLYING THE AD7848

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7848 works on an LSB size of 1.465 mV. Therefore, the designer has to be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feedthrough to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7848 as shown in Figure 20. Connect all analog grounds to this star ground and also connect the AD7848 DGND pin to this ground. Do not connect any other digital grounds to this analog ground point.

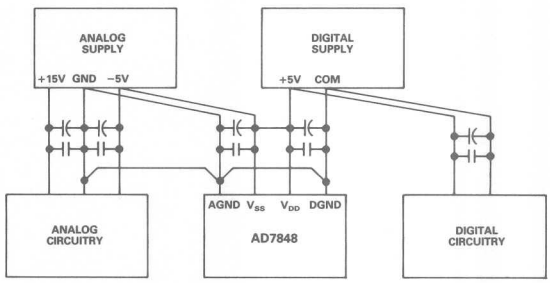


Figure 20. Power Supply Grounding Practice

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the signal leads on the V_{OUT} signal and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC output and its destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

FEEDTHROUGH

The CLK IN feedthrough to the analog output is 2 mV typical. This occurs at 10 MHz and since almost all applications will have a low pass filter on the output to remove the update frequency, the CLK IN feedthrough should not be a problem.

Figure 19. ADI7845 – MC68000 Interface

Figure 20. Power Supply Grounding Practice

250MSPS Video Digital-to-Analog Converter

AD9701

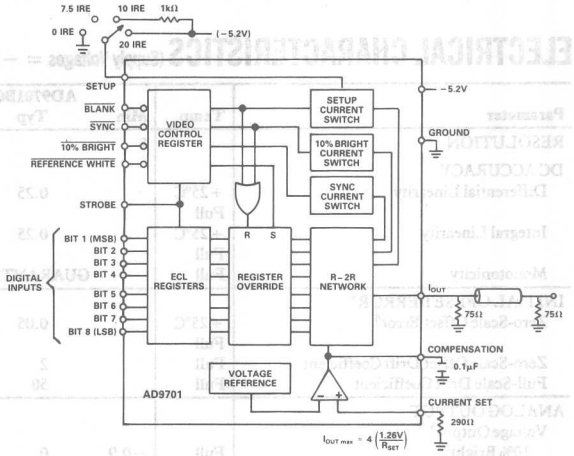
FEATURES

- 250MSPS Update Rate
- Low Glitch Impulse
- Complete Composite Functions
- Internal Voltage Reference
- Single −5.2V Supply

APPLICATIONS

- Raster Scan Displays
- Color Graphics
- Automated Test Equipment
- TV Video Reconstruction

FUNCTIONAL BLOCK DIAGRAM



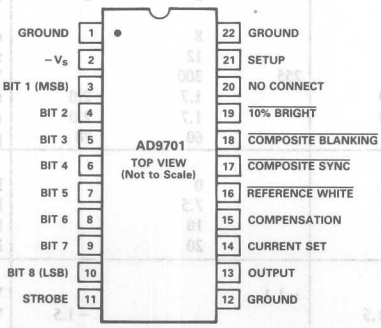
GENERAL DESCRIPTION

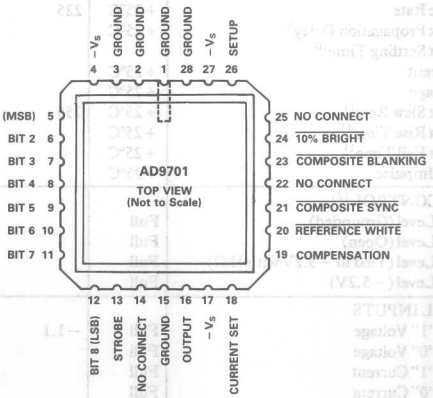
The AD9701 is a high-speed, 8-bit digital-to-analog converter with fully integrated composite video functions. High-speed ECL input registers provide synchronous operation of data and control functions up to 250MSPS.

The AD9701 incorporates on-board control functions including horizontal sync, blanking, reference white level, and a 10% bright signal for highlighting. The setup level is also adjustable from 0 IRE units to 20 IRE units, through the control pin. An internal voltage reference allows the AD9701 to operate as a stand-alone video reconstruction DAC.

The AD9701 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades of the AD9701 are packaged in a 22-pin ceramic DIP, with the extended temperature device also available in a 28-pin LCC package.

PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −7V
Digital Input Voltages (including STROBE, SYNC, BLANKING, 10% BRIGHT, and REFERENCE WHITE) . . . . . 0V to $-V_S$
Analog Output Current 37mA
Power Dissipation (+25°C Free Air)[2] 780mW
Operating Temperature Range
AD9701BQ . . . . . −25°C to +85°C
AD9701SQ/SE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V; R_L = 37.5Ω; Setup = 0V, unless otherwise stated)

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
RESOLUTION		8			8			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Monotonicity	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR[3]								
Zero-Scale Offset Error[4]	+25°C		0.05	0.9		0.05	0.9	mV
	Full			0.9			0.9	mV
Zero-Scale Offset Drift Coefficient	Full		2			2		µV/°C
Full-Scale Drift Coefficient	Full		50			50		µV/°C
ANALOG OUTPUT								
Voltage Output[5]								
10% Bright[6]	Full	−0.9	0		−0.9	0		mV
Reference White	Full	−67.45	−71	−74.55	−67.45	−71	−74.55	mV
Blanking (Setup = 0 IRE)[7]	Full	−698.55	−708.5	−718.45	−698.55	−708.5	−718.45	mV
Sync (Setup = 0 IRE)[8]	Full	−979.25	−993.5	−1007.75	−979.25	−993.5	−1007.75	mV
Current Output[5]								
10% Bright[6]	Full	−0.024	0		−0.024	0		mA
Reference White	Full	−1.805	−1.9	−1.996	−1.805	−1.9	−1.995	mA
Blanking (Setup = 0 IRE)[7]	Full	−18.63	−18.9	−19.16	−18.63	−18.9	−19.16	mA
Sync (Setup = 0 IRE)[8]	Full	−26.11	−26.5	−26.87	−26.11	−26.5	−26.87	mA
Output Compliance Range	Full		−1.6; +0.1			−1.6; +0.1		V
Output Resistance	+25°C	640	800		640	800		Ω
DYNAMIC PERFORMANCE								
Update Rate	+25°C	225	250		225	250		MSPS
Output Propagation Delay[9]	+25°C		5	6		5	6	ns
Output Settling Time[10]								
Current	+25°C		8			8		ns
Voltage	+25°C		12			12		ns
Output Slew Rate[11]	+25°C	255	300		255	300		V/µs
Output Rise Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Output Fall Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Glitch Impulse	+25°C		60	70		60	70	pV-s
SETUP CONTROL[12]								
Setup Level (Grounded)	Full		0			0		IRE
Setup Level (Open)	Full		7.5			7.5		IRE
Setup Level (Tied to −5.2V with 1kΩ)	Full		10			10		IRE
Setup Level (−5.2V)	Full		20			20		IRE
DIGITAL INPUTS								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			15			15	µA
Input Capacitance	+25°C		4	5.5		4	5.5	pF
Data Setup Time	+25°C	0.1			0.1			ns
Data Hold Time	+25°C	1.4			1.4			ns
POWER SUPPLY[13]								
Supply Current (−5.2V)	+25°C		140	160		140	160	mA
	Full			160			160	mA
Nominal Power Dissipation	+25°C		728			728		mW
Power Supply Rejection Ratio[14]	Full		3	6		3	6	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance . . .

22-Pin Ceramic $\theta_{ja} = 64°C/W; \theta_{jc} = 16°C/W$

28-Pin Ceramic LCC $\theta_{ja} = 70°C/W; \theta_{jc} = 21°C/W$

[3]SYNC, BLANKING, and REFERENCE WHITE are inactive (Logic "1"). $I_{SET} \approx 1.26V/R_{SET}$.

[4]All bits at logic HIGH.

[5]All values are relative to full-scale output, after being normalized to nominal value. Typical variation in full-scale output from device to device can reach ±10%, for a fixed R_{SET} resistor.

[6]The effect of 10% BRIGHT algebraically adds to the output waveform.

[7]The output level with BLANKING active (Logic "0"), is determined by the setup control level.

[8]In normal operation, the BLANKING input is activated (Logic "0") prior to or in conjunction with the SYNC input. The effect of the SYNC output is relative to the setup level.

[9]Measured from edge of STROBE to 50% transition point of the output signal.

[10]Measured with full-scale change in output level, from the 10% transition level to within ±0.2% of the final output value.

[11]Measured from 10% to 90% transition point for full-scale step output.

[12]An IRE unit is 1% of the Grey Scale (GS range) with a 0 IRE setup level.

[13]Supply Voltage should remain stable within ±5% for normal operation.

[14]Measured at ±5% of $-V_S$.

Specifications subject to change without notice.

2

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES

1. Setup (Pin 21) grounded (0 IRE units).
2. Setup (Pin 21) open (7.5 IRE units).
3. Setup (Pin 21) to −5.2V through 1k (0 IRE units).
4. Setup (Pin 21) to −5.2V (20 IRE units).

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9701BQ	−25°C to +85°C	22-Pin DIP, Industrial Temperature	Q-22
AD9701SE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9701SQ	−55°C to +125°C	22-Pin DIP, Extended Temperature	Q-22

*E = Leadless Ceramic Chip Carrier; Q = Cerdip. For outline information see Package Information section.

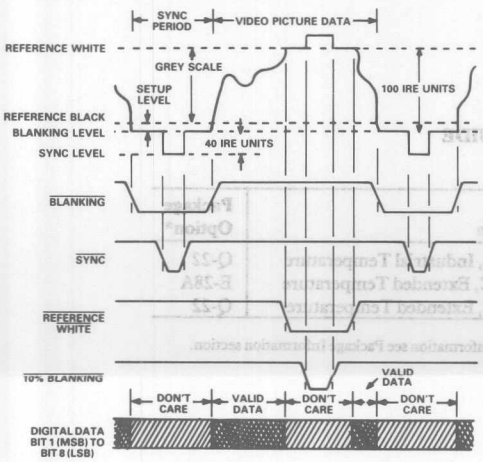
FUNCTIONAL DESCRIPTION

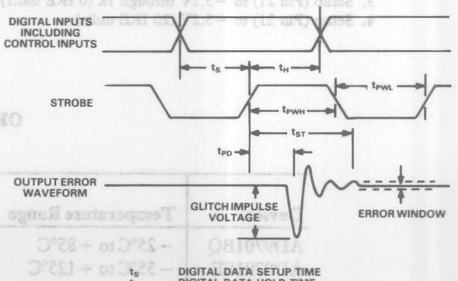
PIN NAME	DESCRIPTION
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.
$-V_S$	– Negative supply pin, nominally $-5.2V$.
BIT 1 (MSB)	– One of eight digital input bits. BIT 1 (MSB) is the most-significant-bit of the digital input word.
BIT 2 – BIT 7	– One of eight digital input bits.
BIT 8 (LSB)	– One of eight digital input bits. BIT 8 (LSB) is the least-significant-bit of the digital input word.
STROBE	– Data and control register strobe input. STROBE is leading edge triggered.
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.
SETUP	– The SETUP input determines the position of the blanking level relative to the "reference black" level (all data bits at logic "0"). The setup level is adjustable from 0 IRE units to 20 IRE units below the reference black level (an IRE unit is 1% of the "grey scale" range).

SETUP LEVEL	CONFIGURATION (PIN 21)
0 IRE Units	Ground
7.5 IRE Units	Open
10 IRE Units	Connection to $-5.2V$ through $1k\Omega$
20 IRE Units	Connection to $-5.2V$

$\overline{\text{10\% BRIGHT}}$	– $\overline{\text{10\% BRIGHT}}$ adds an additional current to the output level, equal to roughly 10% of the "grey scale" range. The $\overline{\text{10\% BRIGHT}}$ is active logic LOW, and operates independently of all other inputs.
$\overline{\text{COMPOSITE BLANKING}}$	– The $\overline{\text{COMPOSITE BLANKING}}$ input, active logic LOW, forces output to the blanking level set with the SETUP input.
$\overline{\text{COMPOSITE SYNC}}$	– The $\overline{\text{COMPOSITE SYNC}}$ input, active LOW, creates a negative going horizontal synchronization pulse relative to the blanking level. Under normal operating conditions the $\overline{\text{COMPOSITE BLANKING}}$ signal should precede and extend past the $\overline{\text{COMPOSITE SYNC}}$ signal. See SETUP for additional information.
$\overline{\text{REFERENCE WHITE}}$	– The $\overline{\text{REFERENCE WHITE}}$ input, active LOW, overrides the data inputs, and forces the output to the maximum "grey scale" level.
COMPENSATION	– The COMPENSATION input insures adequate gain stability for the internal reference amplifier. Under normal operating conditions, the COMPENSATION input is decoupled to ground through a $0.1\mu F$ capacitor.
CURRENT SET	– The CURRENT SET input determines the full-scale or "grey scale" range. The effects of the video control functions are in addition to the "grey scale" range. ($168\Omega \leq R_{SET} \leq 600\Omega$). $I_{OUTmax} \approx 4I_{SET} = 4(1.26V/R_{SET})$
OUTPUT	– Analog output.
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.

SYSTEM TIMING DIAGRAMS

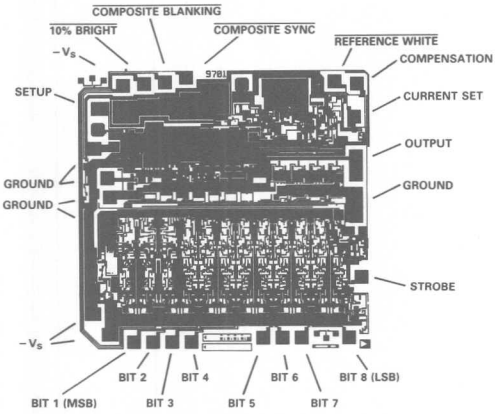




t_S DIGITAL DATA SETUP TIME
t_H DIGITAL DATA HOLD TIME
t_{PWH} STROBE PULSE WIDTH HIGH
t_{PWL} STROBE PULSE WIDTH LOW
t_{ST} SETTLING TIME
t_{PD} MINIMUM PROPAGATION DELAY

NOTES
1. ALL INPUTS, INCLUDING THE VIDEO CONTROL FUNCTIONS, ARE SYNCHRONIZED TO THE STROBE INPUT.
2. THE 10% BRIGHT CONTROL WILL INCREASE THE OUTPUT LEVEL BY APPROXIMATELY 10 IRE UNITS OVER THE PRESENT OUTPUT LEVEL.
3. AN IRE UNIT IS IDEALLY 7.14mV.

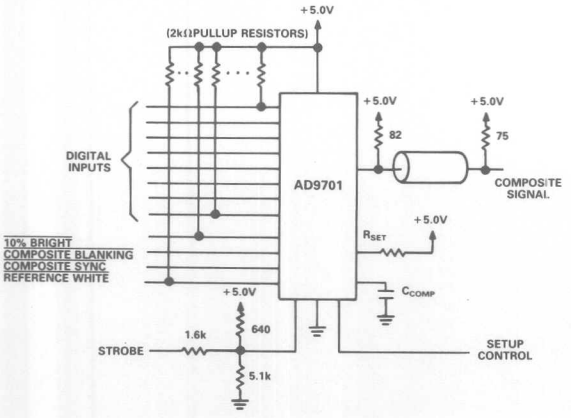
DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	107 × 104 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

APPLICATIONS INFORMATION

Raster scan video displays image data on a line by line basis, with timing and control signals inserted between the lines. The control signals include the horizontal synchronization pulses which are used to align the display circuitry at the beginning of each line. After the complete video image is displayed on the monitor, the process begins again with the next image. The vertical reset pulse(s) that initiate this timing sequence are located between each video image.



Raster Graphics Configuration for TTL Systems

The image data is distinguished from the timing information by its location relative to the blanking level. The blanking reference level is at the blackest extreme of the image data, and all timing signals are designed to fall below the blanking level so as not to be seen on the monitor. The actual image data is located above the blanking level, and it may be further separated from the timing signal by the setup level. The setup level is simply a buffer zone between the timing and image data.

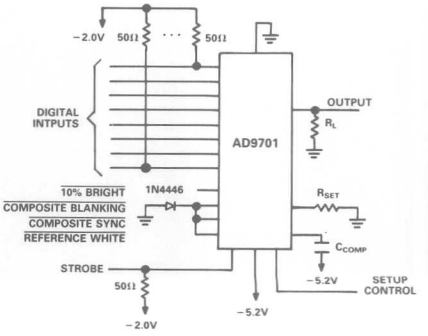
Generation of the timing signals for the AD9701 is controlled by the COMPOSITE BLANKING and the COMPOSITE SYNC inputs. In normal operation the output level of the AD9701 is forced to the blanking level (black) with the COMPOSITE BLANKING control so that when the synchronization occurs, it will not interfere (be seen) with the monitor image. The COMPOSITE SYNC control forces the output level below the blanking level, generating the synchronization pulse.

The "grey scale" is the image intensity range, located above the blanking level by the amount of the setup level. The setup level is "reference black," the darkest displayable picture intensity. The top of the "grey scale" is "reference white," or the brightest picture intensity. As an 8-bit device, the AD9701 divides the "grey scale" into 256 individual levels.

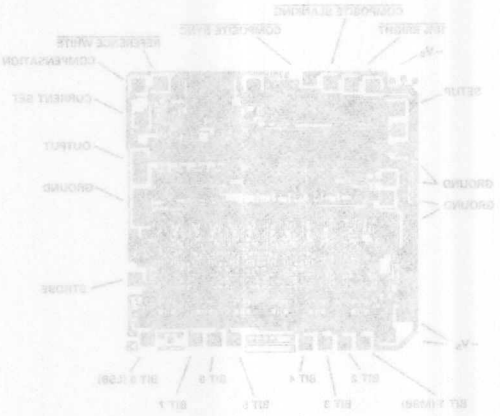
Normal raster scan waveforms divide the region between the blanking level and reference white into 100 IRE units (International Radio Engineers). The setup level can range from 0 to 20 IRE units, but typically is around 10 IRE units, and the synchronization pulse level typically falls 40 IRE units below the blanking level. For the AD9701, the reference white level is 10 IRE units below the full-scale output range ($0mA_{OUT}$).

In terms of priority, the REFERENCE WHITE control overrides the data inputs, but both COMPOSITE SYNC and COMPOSITE BLANKING override the data inputs and the REFERENCE WHITE control. A fourth control is active at all times, 10% BRIGHT, which adds approximately 10 IRE units to the output level no matter what the input state of the AD9701. The 10% BRIGHT control is primarily used to highlight areas of the video image.

As with any high-speed device, the AD9701 requires a substantial low impedance ground plane and high quality ground connections to achieve the best performance. Performance can also be improved with adequate power supply decoupling near the supply pins of the AD9701. In ECL mode, the output of the AD9701 is designed to drive 75Ω cable directly, with 75Ω terminations to ground at both ends of the cable. For TTL configurations the output should be terminated to +5.0V through an 82Ω resistor (see circuit below).



Standard Reconstruction Configuration



Die Dimensions	107 × 104 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	–V$_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

Raster Graphics Configuration for TTL Systems

Standard Reconstruction Configuration

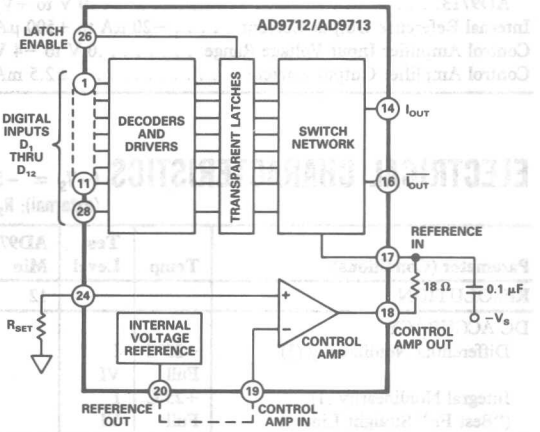
12-Bit, 100 MSPS D/A Converters

AD9712/AD9713

FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
Low Glitch Impulse: 100 pV–s
Fast Settling: 30 ns to ±1 LSB
Low Power: 700 mW

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

FUNCTIONAL BLOCK DIAGRAM

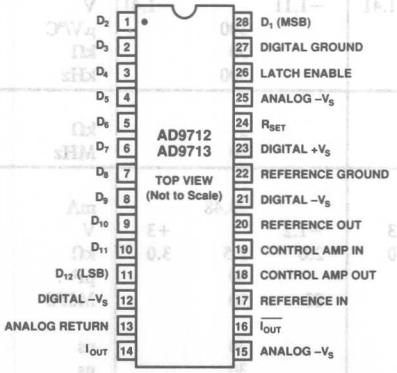


GENERAL DESCRIPTION

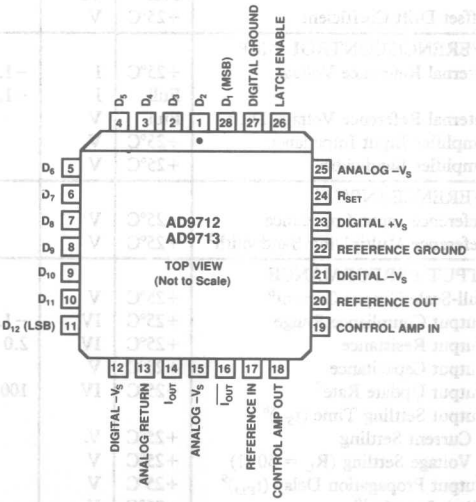
The AD9712 and AD9713 are 12-bit, high speed digital-to-analog converters constructed in an advanced oxide isolated bipolar process. The AD9712 is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713 will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 100 pV-s; and fast settling times of 30 ns to ±1 LSB. Both units are characterized for dynamic performance, and have excellent harmonic suppression.

The AD9712 and AD9713 are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of 0 to +70°C. Contact the factory for availability of military-grade devices.



Plastic DIP Pinout Designations (Top View)



PLCC Pinout Designations

AD9712/AD9713—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713 Only) . . . . . +6 V
Negative Supply Voltage ($-V_S$)
(AD9712 and AD9713) . . . . . −7 V
DAC Outputs to ANALOG RETURN . . . . . +0.5 V to −2 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
AD9712. . . . . .0 V to $-V_S$
AD9713. . . . . .0 V to $+V_S$
Internal Reference Output Current . . . . . −20 μA to +500 μA
Control Amplifier Input Voltage Range . . . . . .0 V to −4 V
Control Amplifier Output Current . . . . . ±2.5 mA
REFERENCE IN Voltage Range . . . . . −3.7 V to $-V_S$
Analog Output Current (I_{OUT} or $\overline{I_{OUT}}$) . . . . . .30 mA
Operating Temperature Range
AD9712JN/JP . . . . . .0 to +70°C
AD9713JN/JP . . . . . .0 to +70°C
Maximum Junction Temperature[2] . . . . . +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S$ = −5.2 V; $+V_S$ = +5 V (AD9713 Only); CONTROL AMP IN = −1.2 V (external); R_{SET} = 7.5 kΩ, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9712JN/JP Min	AD9712JN/JP Typ	AD9712JN/JP Max	AD9713JN/JP Min	AD9713JN/JP Typ	AD9713JN/JP Max	Units
RESOLUTION			12			12			Bits
DC ACCURACY									
Differential Nonlinearity (J)	+25°C	I		1.2	2.0		1.2	2.0	LSB
	Full	VI			4.0			4.0	LSB
Integral Nonlinearity (J)	+25°C	I			3.0			3.0	LSB
("Best Fit" Straight Line)	Full	VI			4.0			4.0	LSB
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	1.5		0.5	1.5	μA
	Full	VI			5.0			5.0	μA
Full-Scale Gain Error[3]	+25°C	I		4.0	8.5		4.0	8.5	%
	Full	VI			11.0			11.0	%
Offset Drift Coefficient	+25°C	V		0.03			0.03		μA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	−1.13	−1.26	−1.39	−1.13	−1.26	−1.39	V
	Full	I	−1.11		−1.41	−1.11		−1.41	V
Internal Reference Voltage Drift	Full	V		300			300		μV/°C
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[4]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[5]	+25°C	V		40			40		MHz
OUTPUT PERFORMANCE									
Full-Scale Output Current[6]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+3	−1.2		+3	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		30			30		pF
Output Update Rate[7]	+25°C	IV	100	110		80	90		MSPS
Output Settling Time (t_{ST})[8]									
Current Settling	+25°C	V		30			30		ns
Voltage Settling (R_L = 50 Ω)	+25°C	V		30			30		ns
Output Propagation Delay (t_{PD})[9]	+25°C	V		8			11		ns
Glitch Impulse[10]	+25°C	V		100			100		pV-s
Output Slew Rate[11]	+25°C	V		400			400		V/μs
Output Rise Time[11]	+25°C	V		3			3		ns
Output Fall Time[11]	+25°C	V		2			2		ns

Parameter (Conditions)	Temp	Level	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	−1.0	−0.8		2.0			V
Logic "0" Voltage	Full	VI		−1.7	−1.5			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			10			600	μA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[12]	+25°C	V		3			3		ns
Input Hold Time (t_H)[13]	+25°C	V		3			3		ns
Latch Pulse Width (t_{LPW}) (Transparent)	+25°C	V		2.5			4		ns
AC LINEARITY[14]									
Spurious-Free Dynamic Range	+25°C	V		−60			−55		dBc
POWER SUPPLY[15]									
Positive Supply Current (+5.0 V)	+25°C	I					10	20	mA
	Full	VI						23	mA
Negative Supply Current (−5.2 V)	+25°C	I		130	160		135	165	mA
	Full	VI			170			175	mA
Nominal Power Dissipation	+25°C	V		676			726		mW
Power Supply Rejection Ratio (PSRR)[16]	+25°C	I		50	350		50	350	μA/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 28-pin plastic DIP θ_{JA} = 42°C/W; θ_{JC} = 7°C/W; 28-pin PLCC θ_{JA} = 48°C/W; θ_{JC} = 10°C/W.

[3]Measured as error of the ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.

[4]Full-scale variations among devices are more severe when driving REFERENCE IN directly.

[5]Frequency at which a 3 dB reduction in output of DAC is observed; R_L = 50 Ω; 50% modulation at midscale.

[6]Based on I_{FS} = 128 (V_{REF}/R_{SET}) when using internal amplifier.

[7]Output settling to 0.1%.

[8]Measured at midscale transition, to ±0.024%.

[9]Measured from falling edge of LATCH ENABLE signal to 50% point of full-scale transition.

[10]Glitch impulse combines the absolute value of positive and negative transitions operating in latched mode.

[11]Measured with R_L = 50 Ω and DAC operating in latched mode.

[12]Data must remain stable prior to falling edge of LATCH ENABLE signal for specified time.

[13]Data must remain stable after rising edge of LATCH ENABLE signal for specified time.

[14]Update rate ≤50 MSPS; output frequency = 5 MHz.

[15]Supply voltages should remain stable within ±5% for normal operation.

[16]Measured at ±5% of $+V_S$ (AD9713 only) and $-V_S$ (AD9712 or AD9713) using external reference.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

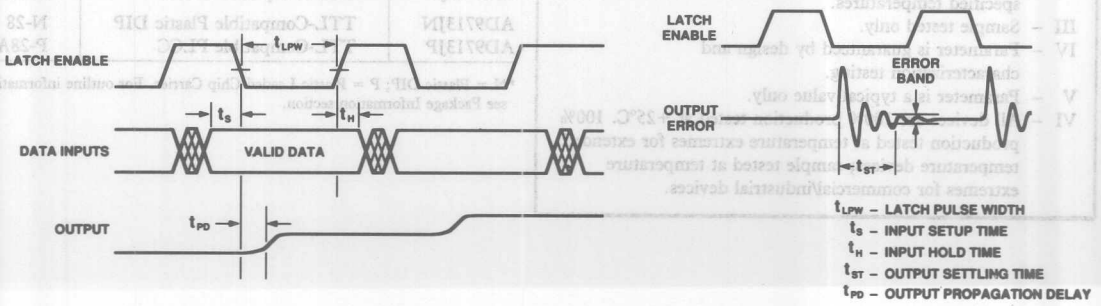
ORDERING GUIDE

Model	Description	Package Option*
AD9712JN	ECL-Compatible Plastic DIP	N-28
AD9712JP	ECL-Compatible PLCC	P-28A
AD9713JN	TTL-Compatible Plastic DIP	N-28
AD9713JP	TTL-Compatible PLCC	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

AD9712/AD9713 PIN DESCRIPTIONS

Pin No.	Name	Function
1–10	D_2–D_{11}	Ten of twelve digital input bits.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current switch network. Voltage changes at this point have a direct effect on the full-scale output. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE IN (Pin 17). Output of internal control amplifier, which provides a temperature compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally −1.26 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin; used only on the AD9713; nominally +5 V.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
26	LATCH ENABLE	Transparent latch control line.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.



AD9712/AD9713 Timing Diagram

THEORY AND APPLICATIONS

The AD9712 and AD9713 high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Transparent Latches, the Switch Network and the Control Amplifier. An internal band-gap reference is also included to allow operation with a minimum of external components.

Digital Inputs

The AD9712 employs single-ended ECL-compatible inputs for data inputs D_1–D_{12} and LATCH ENABLE. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9713, a TTL translator is added at each input; with this exception, the AD9712 and AD9713 are identical.

In the Decoder/Driver section, the four MSBs (D_1–D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the eight Least Significant Bits (LSBs) and LATCH ENABLE. This delay minimizes data skew, and data setup and hold times at the latch inputs; this is important when operating the latches in the transparent mode. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

The latches operate in their transparent mode when LATCH ENABLE (Pin 26) is at logic level "0." The latches can be used to synchronize data to the current switches by applying a narrow LATCH ENABLE pulse with proper data setup and hold times as shown in the timing diagram. With an external transparent latch at each data input clocked out of phase with the DAC, the AD9712/AD9713 operates in a master slave (edge-triggered) mode.

Although the AD9712/AD9713 chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9713. Digital feedthrough can be reduced by forming a low-pass filter using a resistor in series with the capacitance of each digital input.

References

As shown in the functional block diagram, the internal band-gap reference, control amplifier and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 20) should be connected to CONTROL AMP IN (Pin 19). CONTROL AMP OUT (Pin 18) should be connected to REFERENCE IN (Pin 17) through an 18 Ω resistor. A 0.1 μF ceramic capacitor from Pin 17 to $-V_S$ (Pin 15) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 24).

Full-scale output current is determined by the voltage at CONTROL AMP IN (V_{REF}) and R_{SET} according to the equation:

$$I_{OUT}\,(FS) = V_{REF}/R_{SET} \times 128.$$

The internal reference is nominally −1.26 V with a tolerance of ±10% and typical drift over temperature of 300 μV/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference shown in Figure 1 features ±10 ppm/°C drift over temperatures from 0 to +70°C.

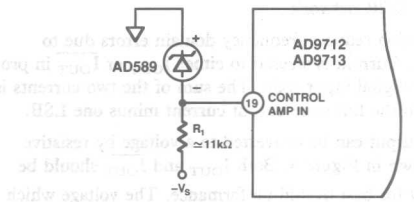


Figure 1. Use of AD589 as External Reference

Two modes of multiplying operation are possible with the AD9712/AD9713. Signals with bandwidths up to 400 kHz and input swings from −0.1 V to −1.2 V can be applied to the CONTROL AMP input as shown in Figure 2. Because the control amplifier is internally compensated, the 0.1 μF capacitor at Pin 17 can be eliminated to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

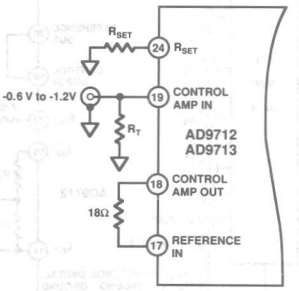


Figure 2. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of −4 V to −5.2 V. This can be implemented by capacitively coupling into REFERENCE IN an ac signal and establishing a dc bias of −4.0 V to −5.2 V, as shown in Figure 3; or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

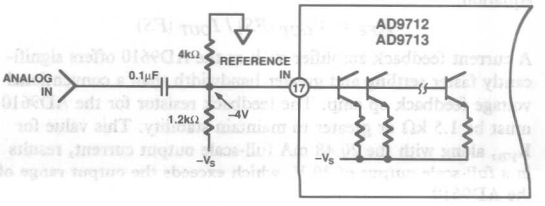


Figure 3. Wideband Multiplying Circuit

Outputs

The Switch Network controls complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. As indicated earlier, D_1–D_4 are decoded into 15 "thermometer code" lines which drive matched current sources. D_5 and D_6 control weighted current sources; and D_7–D_{12} are applied to the R-2R network.

This segmentation reduces frequency domain errors due to glitch impulse. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figure 4. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

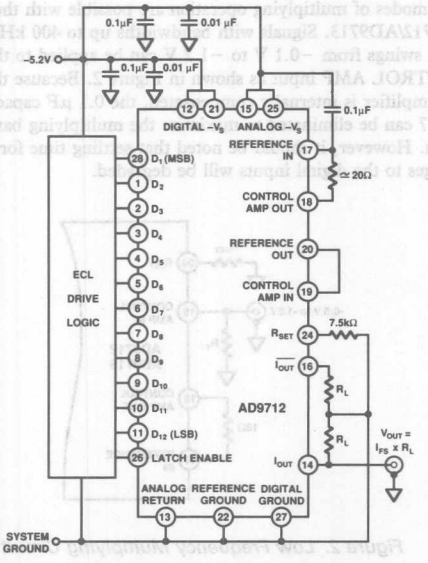


Figure 4. Typical Resistive Load Connection

When operating at the nominal full-scale current of 20.48 mA, the voltage swing will be from 0 to −1.024 V across 50 Ω resistors. Bipolar outputs are possible by sourcing a current equal to half the DAC full-scale current into the load resistor.

An alternate method of converting the current output to voltage is by driving the summing node of an operational amplifier directly with a feedback resistor selected according to the equation:

$$R_{FB} = V_{OUT}\,(FS) / I_{OUT}\,(FS)$$

A current feedback amplifier such as the AD9610 offers significantly faster settling and greater bandwidth than a conventional voltage feedback op amp. The feedback resistor for the AD9610 must be 1.5 kΩ or greater to maintain stability. This value for R_{FB}, along with the 20.48 mA full-scale output current, results in a full-scale output of 30 V, which exceeds the output range of the AD9610.

Full-scale output voltage can be reduced by either reducing the DAC's full-scale output current, or by using a current divider at the DAC output as shown in Figure 5. Reducing DAC full-scale output current degrades both linearity and settling time; therefore, the current divider method is preferable.

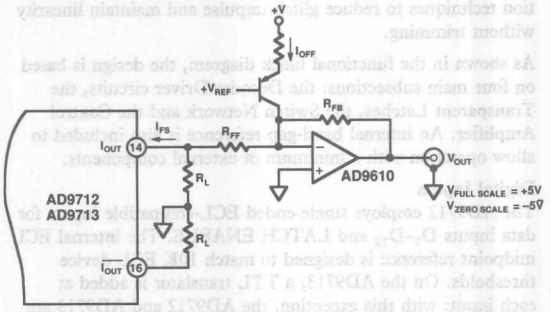


Figure 5. I/V Conversion Using Current Feedback Amp

The DAC output is not clamped at virtual ground in this configuration because of the series resistance R_{FF}. The value of R_{FF} is selected according to the equation:

$$R_{FF} = \frac{R_L I_{FS} - \left(\frac{V_{Full\ Scale}}{R_{FB}} + I_{OFF}\right) R_L}{\frac{V_{Full\ Scale}}{R_{FB}} + I_{OFF}}$$

As an example, assume the following conditions:

$R_L = 50\ \Omega$

$R_{FB} = 1.5\ k\Omega$

$I_{FS} = 20.48\ mA$

$$I_{OFF} = \frac{-V_{Zero\ Scale}}{R_{FB}} = 3.3\ mA$$

Given these conditions, $R_{FF} = 103.6\ \Omega$

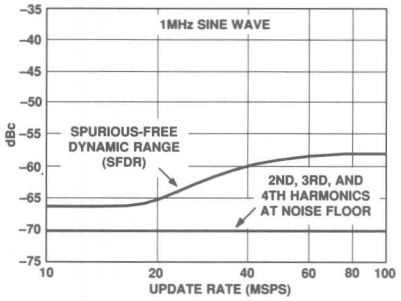
Power and Grounding

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the AD9712 or AD9713. DACs are most often used in circuits which are predominantly digital. To preserve 12-bit performance, especially at conversion speeds up to 100 MSPS, special precautions are necessary for power supplies and grounding.

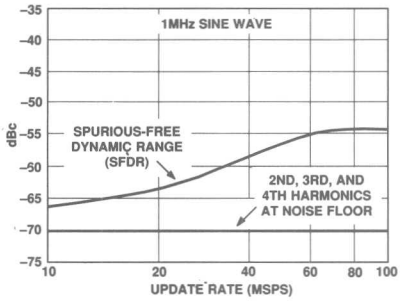
Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads, along with high frequency, low inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

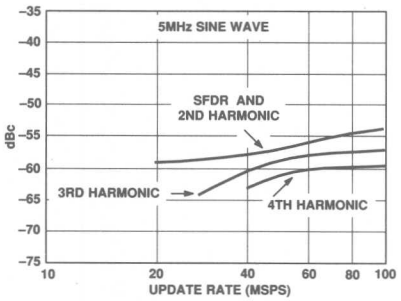
Molded socket assemblies should be avoided even when prototyping circuits with the AD9712 or AD9713. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out end), or #60330808-3 (open end) should be used. These have much less effect on interlead capacitance than do molded assemblies.



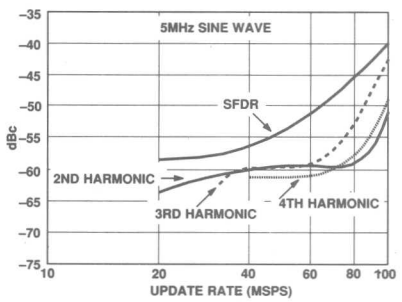
AD9712 Harmonic Distortion vs. Update Rate



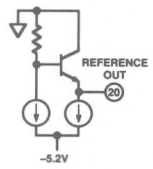
AD9713 Harmonic Distortion vs. Update Rate



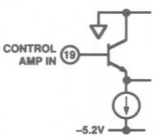
AD9712 Harmonic Distortion vs. Update Rate



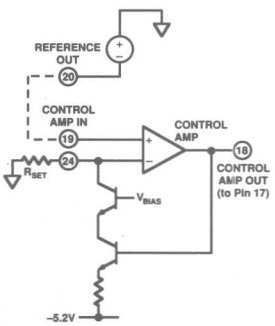
AD9713 Harmonic Distortion vs. Update Rate



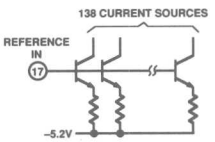
Reference Output



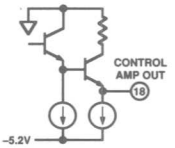
Control Amplifier Input



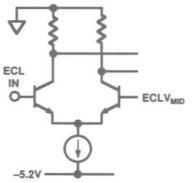
Full-Scale Current Control Loop



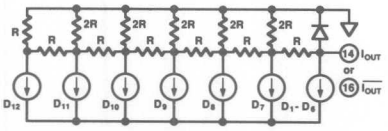
Reference Input



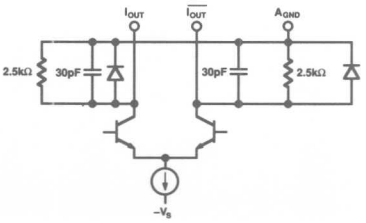
Control Amplifier Output



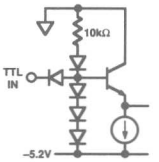
ECL Input Buffer



R-2R DAC
(for 6 LSBs)



Output Circut



TTL Input Buffer

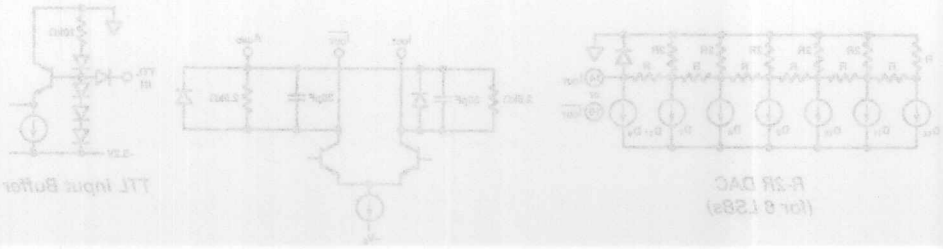
AD9712/AD9713 Equivalent Circuits

AD9713 Harmonic Distortion vs. Update Rate

AD9712 Harmonic Distortion vs. Update Rate

AD9713 Harmonic Distortion vs. Update Rate

AD9712 Harmonic Distortion vs. Update Rate



AD9712/AD9713 Equivalent Circuits

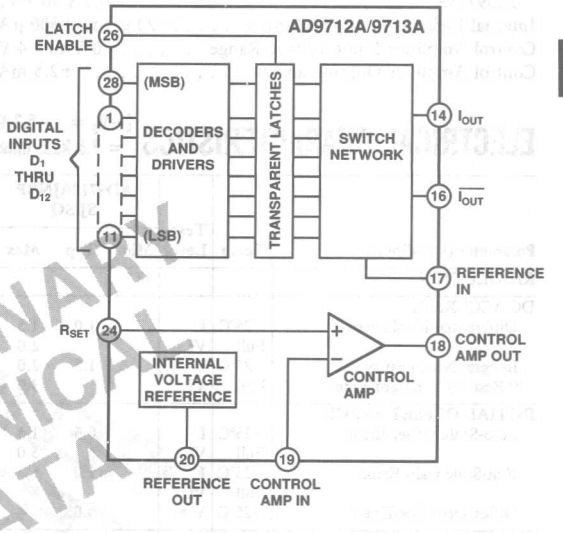
12-Bit, 100 MSPS D/A Converters

AD9712A/AD9713A

FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
SFDR @ 1 MHz: 70 dBc
Low Glitch Impulse: 35 pV-s
Fast Settling: 25 ns
Low Power: 750 mW
3/4 LSB DNL (K and T Grades)

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD9712A and AD9713A D/A converters are replacements for the AD9712 and AD9713 units which offer improved ac and dc performance. Like their predecessors, they are 12-bit, high speed digital-to-analog converters fabricated in an advanced oxide isolated bipolar process. The AD9712A is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713A will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 50 pV-s and fast settling times of 25 ns for the AD9712A, and 30 ns for the AD9713A. Both units are characterized for dynamic performance and have excellent harmonic suppression. The K and T grades have guaranteed limits on spurious-free dynamic range (SFDR).

The AD9712A and AD9713A are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of 0°C to +70°C. Both are also available for extended temperature ranges of −55°C to +125°C in cerdips and 28-pin J-leaded ceramic packages.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Negative Supply Voltage ($-V_S$) . . . . . −7 V
(AD9712A and AD9713A)
Analog-to-Digital Ground Voltage Differential . . . . . 0.5 V
Digital Input Voltages (D1–D12, LATCH ENABLE)
AD9712A . . . . . 0 V to $-V_S$
AD9713A . . . . . −0.5 V to $+V_S$
Internal Reference Output Current . . . . . −20 μA to +500 μA
Control Amplifier Input Voltage Range . . . . . 0 V to −4 V
Control Amplifier Output Current . . . . . ±2.5 mA

Operating Temperature Range
AD9712A/AD9713AJN/JP/KN/KP . . . . . 0°C to +70°C
AD9712A/AD9713ASJ/SQ/TJ/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature[2]
AD9712A/AD9713AJN/JP/KN/KP . . . . . +150°C
AD9712A/AD9713ASJ/SQ/TJ/TQ . . . . . +175°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS

[$-V_S$ = −5.2 V; $+V_S$ = +5 V (AD9713A only); Reference Voltage = −1.2 V; R_{SET} = 7.5 kΩ, unless otherwise noted]

Parameter (Conditions)	Temp	Test Level	AD9712AJN/JP SJ/SQ			AD9712AKN/KP TJ/TQ			AD9713AJN/JP SJ/SQ			AD9713AKN/KP TJ/TQ			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			12			12			12			12			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		1.0	1.5		0.5	0.75		1.0	1.5		0.5	0.75	LSB
	Full	VI			2.0			1.5			2.0			1.5	LSB
Integral Nonlinearity	+25°C	I		1.5	2.0		0.75	1.0		1.5	2.0		0.75	1.0	LSB
("Best Fit" Straight Line)	Full	VI			3.0			1.75			3.0			1.75	LSB
INITIAL OFFSET ERROR															
Zero-Scale Offset Error	+25°C	I		0.5	1.5		0.5	1.5		0.5	1.5		0.5	1.5	μA
	Full	VI			5.0			5.0			5.0			5.0	μA
Full-Scale Gain Error[3]	+25°C	I		1.0	5		1.0	5		1.0	5		1.0	5	%
	Full	VI			8			8			8			8	%
Offset Drift Coefficient	+25°C	V		0.03			0.03			0.03			0.03		μA/°C
REFERENCE/CONTROL															
Internal Reference Voltage	+25°C	I	−1.17	−1.21	−1.25	−1.17	−1.21	−1.25	−1.17	−1.21	−1.25	−1.17	−1.21	−1.25	V
	Full	VI	−1.14		−1.28	−1.14		−1.28	−1.14		−1.28	−1.14		−1.28	V
Internal Reference Voltage Drift	Full	V		50			50			50			50		ppm/°C
Amplifier Input Impedance	+25°C	V		50			50			50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300			300			300		kHz
REFERENCE INPUT[4]															
Reference Input Impedance	+25°C	V		3			3			3			3		kΩ
Ref. Multiplying Bandwidth[5]	+25°C	V		40			40			40			40		MHz
OUTPUT PERFORMANCE															
Full-Scale Output Current[6]	+25°C	V		20.48			20.48			20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+2	−1.2		+2	−1.2		+2	−1.2		+2	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		16			16			16			16		pF
Output Update Rate[7]	+25°C	IV	100	110		100	110		80	90		80	90		MSPS
Output Settling Time (t_{ST})[8]	+25°C	V		22			22			27			27		ns
Output Propagation Delay (t_{PD})[9]	+25°C	V		8			8			10			10		ns
Glitch Impulse[10]	+25°C	V		50			50			50			50		pV-s
Output Slew Rate[11]	+25°C	V		750			750			750			750		V/μs
Output Rise Time[11]	+25°C	V		2			2			2			2		ns
Output Fall Time[11]	+25°C	V		2			2			2			2		ns
DIGITAL INPUTS															
Logic "1" Voltage	Full	VI	−1.0	−0.8		−1.0	−0.8		2.0			2.0			V
Logic "0" Voltage	Full	VI		−1.7	−1.5		−1.7	−1.5			0.8			0.8	V
Logic "1" Current	Full	VI			20			20			20			20	μA
Logic "0" Current	Full	VI			10			10			600			600	μA
Input Capacitance	+25°C	V		3			3			3			3		pF
Input Setup Time (t_S)[12]	+25°C	IV	1	0		1	0		1	0		1	0		ns
	Full	IV	2			2			2			2			ns
Input Hold Time (t_H)[13]	+25°C	IV	2.5	1		2.5	1		2.5	1		2.5	1		ns
	Full	IV	3.5			3.5			3.5			3.5			ns
Latch Pulse Width (t_{LPW})	+25°C	IV	3	2		3	2		3	2		3	2		ns
(LOW) (Transparent)	Full		4			4			4			4			ns

PRELIMINARY TECHNICAL DATA

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Parameter (Conditions)	Temp.	Test Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
AC LINEARITY[14]															
Spurious-Free Dynamic Range (SFDR)															
1 MHz Output @ 12.5 MSPS	+25°C	V		68			68			68			68		dBc
5 MHz Output @ 25 MSPS	+25°C	V		64			64			64			64		dBc
10 MHz Output @ 50 MSPS	+25°C	V		58			58			58			58		dBc
POWER SUPPLY[15]															
Positive Supply Current	+25°C	I								5	10		5	10	mA
(+5.0 V)	Full	VI									13			13	mA
Negative Supply Current	+25°C	I		138	165		138	165		142	170		142	170	mA
(−5.2 V)	Full	VI			175			175			180			180	mA
Nominal Power Dissipation	+25°C	V		676			676			726			726		mW
Power Supply Rejection Ratio (PSRR)[16]	+25°C	I		50	280		50	280		50	280		50	280	μA/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 28-pin plastic DIP θ_{JA} = 42°C/W; θ_{JC} = 7°C/W; 28-pin PLCC θ_{JA} = 48°C/W; θ_{JC} = 10°C/W; 28-pin J-Leaded package: θ_{JA} = 80°C/W; θ_{JC} = 30°C/W; Cerdip: θ_{JA} = 75°C/W; θ_{JC} = 25°C/W.

[3]Measured as error in ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.

[4]Full-scale variations among devices are higher when driving REFERENCE INPUT directly.

[5]Frequency at which a 3 dB change in output of DAC is observed; R_L = 50 Ω; 50% modulation at midscale.

[6]Based on $I_{FS} = 128 (V_{REF}/R_{SET})$ when using internal amplifier.

[7]Output settling to 0.1%.

[8]Measured as voltage settling at midscale transition to ±0.024%; R_L = 50 Ω.

[9]Measured from falling edge of LATCH ENABLE signal to 50% transition point of output signal.

[10]Glitch impulse combines the absolute value of positive and negative transitions.

[11]Measured with R_L = 75 Ω and DAC operating in latched mode.

[12]Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.

[13]Data must remain stable for specified time after rising edge of LATCH ENABLE signal.

[14]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum from dc to one-half the clock rate, excluding dc.

[15]Supply voltages should remain stable within ±5% for normal operation.

[16]Measured at ±5% of $+V_S$ (AD9713A only) and $-V_S$ (AD9712A or AD9713A) using external reference.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

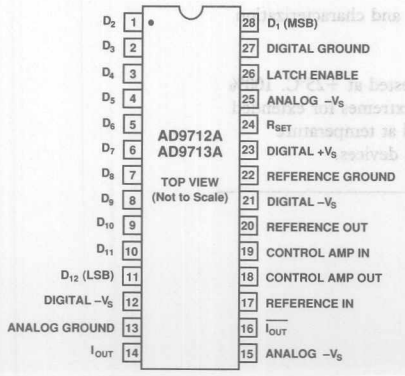
PIN DESCRIPTIONS

Pin No.	Name	Function
1–10	D_2–D_{11}	Ten of 12 digital input bits.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
	Input Coding vs. Current Output	
	Input Code $D_1 - D_{12}$	*I_{OUT} (mA)* *I_{OUT} (mA)*
	111111111111	−20.475 0
	000000000000	0 −20.475
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
16	I_{OUT}	Complementary analog current output; zero-scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current source network. Voltage changes at this point have a direct effect on the full-scale output value of unit. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 17). Output of internal control amplifier, which provides a temperature-compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally −1.26 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin, used only on the AD9713A; nominally +5 V.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
26	LATCH ENABLE	Transparent latch control line. Register is transparent when LATCH ENABLE is LOW.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.

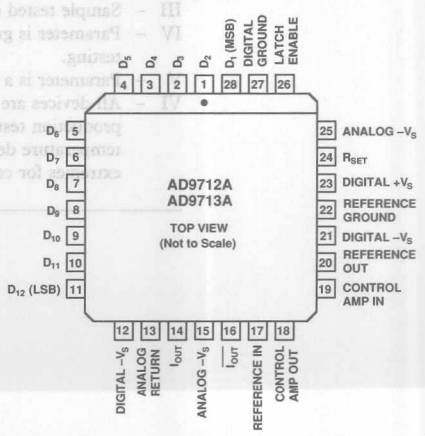
PRELIMINARY TECHNICAL DATA

PIN CONFIGURATIONS

DIP



PLCC



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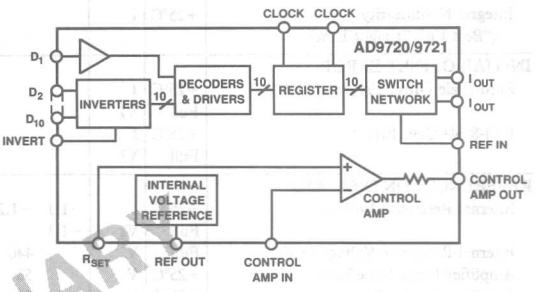
10-Bit, 300 MSPS D/A Converters

AD9720/AD9721

FEATURES
300 MSPS (ECL)/100 MSPS (TTL) Update Rate
Low Glitch Impulse: 15 pV-s
Fast Settling: 10 ns to 1/2 LSB
Low Power: 1.1 W
On-Board Quadrature Logic for DDS Applications
Differential Clock (ECL)

APPLICATIONS
Direct Digital Synthesis
Arbitrary Waveform Synthesis
Waveform Reconstruction
High Speed Imaging

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD9720 and AD9721 D/A converters are 10-bit, high speed digital-to-analog converters constructed in an oxide isolated bipolar process. The AD9720 is ECL compatible, and will update up to 300 MSPS; the AD9721 is TTL compatible and will update up to 100 MSPS.

Designed for direct digital synthesis (DDS), waveform reconstruction, and high resolution video applications, both devices feature low glitch impulse of 15 pV-s; and fast settling times of 10 ns to 1/2 LSB.

On-board logic minimizes external components in DDS applications. All that is needed for 300 MHz DDS is the AD9720, the AD9950 Phase Accumulator, and 1k × 9 of memory.

Both converters are characterized for dynamic performance, and have excellent harmonic suppression and spectral purity in waveform generation applications.

The units are available in 28-pin DIPs, 28-terminal PLCCs and J-leaded quad packs. Commercial devices are packaged in plastic for operation from 0°C to +70°C; extended temperature range devices for operation from −55°C to +125°C are in hermetic ceramic packages. Contact the factory for information about the availability of MIL STD 883 devices.

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ELECTRICAL CHARACTERISTICS unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9720KN/KP Min	AD9720KN/KP Typ	AD9720KN/KP Max	AD9720TJ/TQ Min	AD9720TJ/TQ Typ	AD9720TJ/TQ Max	AD9721KN/KP Min	AD9721KN/KP Typ	AD9721KN/KP Max	AD9721TJ/TQ Min	AD9721TJ/TQ Typ	AD9721TJ/TQ Max	Units
RESOLUTION			10			10			10			10			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.25	0.5		0.25	0.5		0.25	0.5		0.25	0.5	LSB
	Full	VI			0.75			0.75			0.75			0.75	LSB
Integral Nonlinearity ("Best Fit" Straight Line)	+25°C	I			1			1			1			1	LSB
INITIAL OFFSET ERROR															
Zero-Scale Offset Error	+25°C	I			0.5			0.5							µA
	Full	VI			1.0			1.0							µA
Full-Scale Gain Error[1]	+25°C	I			20			20							%
	Full	VI			20			20							%
REFERENCE/CONTROL AMP															
Internal Reference Voltage	+25°C	I	−1.1	−1.25	−1.3	−1.1	−1.25	−1.3							V
	Full	VI	−1.1		−1.3	−1.1		−1.3							V
Internal Reference Voltage Drift	Full	V		440			440								µV/°C
Amplifier Input Impedance	+25°C	V		50			50								kΩ
Amplifier Bandwidth	+25°C	V		300			300			300			300		kHz
REFERENCE INPUT[2]															
Reference Input Impedance	+25°C	V		50			50			50			50		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V								70			70		MHz
OUTPUT PERFORMANCE															
Full-Scale Output Current[4]	+25°C	V		20.48			20.48			20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+3	−1.2		+3	−1.2		+3	−1.2		+3	V
Output Resistance	+25°C	IV		240			240								kΩ
Output Capacitance	+25°C	V		12			12			15			15		pF
Output Update Rate[5]	+25°C	IV	300			300			100			100			MSPS
	Full	V		300			300			100			100		MSPS
Current Settling Time (1/2 LSB)[6]	+25°C	V		5	10		5	10		5	10		5	10	ns
Voltage Settling Time (1/2 LSB)[6]	+25°C	V		5	10		5	10		5	10		5	10	ns
Propagation Delay (t_{PD})[7]	+25°C	V		2.5			2.5								ns
Glitch Impulse[8]	+25°C	V		15			15			15			15		pV-s
Output Slew Rate[9]	+25°C	V		500			500								V/µs
Output Rise Time[9]	+25°C	V		1.5			1.5								ns
Output Fall Time[9]	+25°C	V		1.5			1.5								ns
DIGITAL INPUTS															
Logic "1" Voltage	Full	VI	−1.0			−1.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			0.8			0.8	V
Input Capacitance	+25°C	V		3			3								pF
Input Setup Time (t_S)[10]	+25°C	IV					1								ns
	Full	IV	1.75			1.75									ns
Input Hold Time (t_H)[11]	+25°C	IV					1								ns
	Full	IV	0.75			1.75									ns
Clock Pulse Width (Low)	+25°C	IV		1.25			1.25								ns
Clock Pulse Width (High)	+25°C	IV		1.25			1.25								ns
DYNAMIC PERFORMANCE															
Spurious-Free Dynamic Range (SFDR)[12]															
1.2 MHz Output @ 50 MSPS	+25°C	I	65	70		65	70		65	70		65	70		dBc
10 MHz Output @ 100 MSPS	+25°C	I	65			65			65			65			dBc
POWER SUPPLY[13]															
Nominal Power Dissipation	+25°C	V		1			1			1			1		W

PRELIMINARY TECHNICAL DATA

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NOTES
[1]Measured as error in ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 32.
[2]Full-scale variations among devices are higher when driving REFERENCE IN directly.
[3]Frequency at which a 3 dB change in output of DAC is observed; R_L = 50 Ω; 50% modulation at midscale.
[4]Based on I_{FS} = 32 (CONTROL AMP IN/R_{SET}) when using internal amplifier.
[5]Output settling to 0.1%.
[6]Measured as voltage settling at midscale transition to ±0.024%; R_L = 50 Ω.
[7]Measured from rising edge of CLOCK signal to 50% transition point of output signal.
[8]Glitch impulse combines the absolute value of positive and negative transitions.
[9]Measured with R_L = 50 Ω and DAC operating in latched mode.
[10]Data must remain stable for specified time prior to rising edge of CLOCK.
[11]Data must remain stable for specified time after rising edge of CLOCK.
[12]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum from dc to one-half the clock rate, excluding dc.
[13]Supply voltages should remain stable within ±5% for normal operation.
Specifications subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS[1]

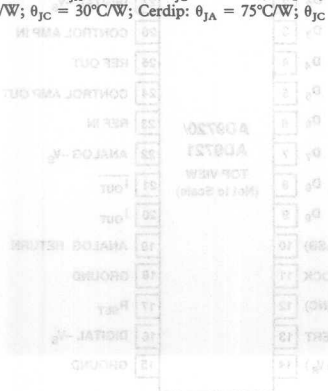
Positive Supply Voltage (+V_S) (AD9721 only) . . . . . +6 V
Negative Supply Voltage (−V_S) . . . . . −7 V
(AD9720 and AD9721) Analog Output Current . . . . . 30 mA
Digital Input Voltages (D_1–D_{10}, CLOCK, $\overline{CLOCK}$)
AD9720 . . . . . 0 V to −V_S
AD9721 . . . . . −0.5 V to +V_S
Internal Reference Output Current . . . . . 500 μA
Control Amplifier Input Voltage Range . . . . . 0 V to −4 V
Control Amplifier Output Current . . . . . 2.5 mA
Reference Input Voltage . . . . . −3.7 V to −V_S
Range (V_{REF})
Operating Temperature Range
AD9720/AD9721KN/KP . . . . . 0°C to +70°C
AD9720/AD9721TJ/TQ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[2]
AD9720/AD9721KN/KP . . . . . +150°C
AD9720/AD9721TJ/TQ/883 . . . . . +175°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 28-pin plastic DIP θ_{JA} = 42°C/W; θ_{JC} = 7°C/W; 28-pin PLCC θ_{JA} = 48°C/W; θ_{JC} = 10°C/W; 28-pin J-Leaded package: θ_{JA} = 80°C/W; θ_{JC} = 30°C/W; Cerdip: θ_{JA} = 75°C/W; θ_{JC} = 25°C/W.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PRELIMINARY TECHNICAL DATA



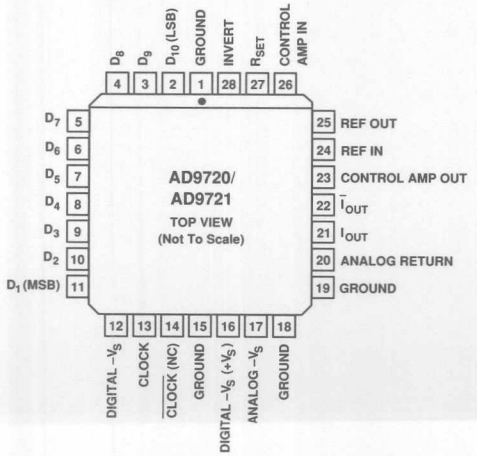
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PIN DESCRIPTIONS

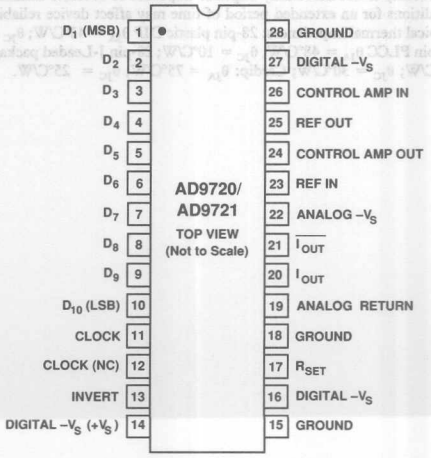
DIP Pin #	Name	Function
1	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.
2–9	D_2–D_9	Eight of 10 digital input bits. Digital inputs are ECL compatible for AD9720; TTL compatible for AD9721. See coding table elsewhere.
10	D_{10} (LSB)	Least Significant Bit (LSB) of digital input word. **Input Coding vs. Current Output** Input Code D_1–D_{10} I_{OUT} (mA) $I_{\overline{OUT}}$ (mA) 1111111111 −20.48 0 0000000000 0 −20.48
11	CLOCK	Edge-triggered latch enable signal for on-board registers. ECL compatible for AD9720; TTL compatible for AD9721. Register loads data on rising edge of CLOCK signal; must be driven in conjunction with $\overline{CLOCK}$.
12	$\overline{CLOCK}$/NC	Complementary edge-triggered latch enable signal for on-board registers. ECL compatible for AD9720; TTL compatible for AD9721.
13	INVERT	Normally connected to logic LOW. Control signal for on-board quad logic.
14	DIGITAL $-V_S/+V_S$	One of three negative digital supply pins; nominally −5.2 V.
15	GROUND	Converter ground return.
16	DIGITAL $-V_S$	One of three negative digital supply pins; nominally −5.2 V.
17	R_{SET}	Connection for external resistance reference; nominally 1,960 Ω. Full-scale current out = 32 (CONTROL AMP IN/R_{SET}) when using internal amplifier.
18	GROUND	Converter ground return.
19	ANALOG RETURN	Analog current return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
20	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1." With external load resistor, output voltage = I_{OUT} ($R_{LOAD} \parallel R_{INTERNAL}$). $R_{INTERNAL}$ is nominally 200 Ω.
21	$I_{\overline{OUT}}$	Complementary analog current output; zero-scale output occurs with digital inputs at all "1."
22	ANALOG $-V_S$	Negative analog supply; nominally −5.2 V.
23	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 22). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of DAC. Full-scale current output = 32 (CONTROL AMP IN/R_{SET}) when using internal amplifier.
24	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 23). Output of internal control amplifier, which provides a reference for the current switch network.
25	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 25). Internal voltage reference, nominally −1.27 V.
26	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 24) if not connected to external reference.
27	DIGITAL $-V_S$	One of three negative digital supply pins; nominally −5.2 V.
28	GROUND	Converter ground return.

PIN CONFIGURATIONS

PLCC



DIP



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Ultrahigh Speed IC D/A Converter

AD9768

FEATURES
5ns Settling Time
100MSPS Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MSPS. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

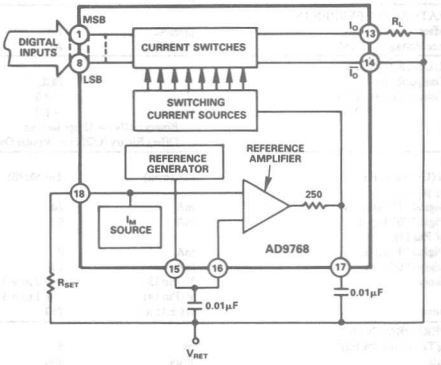
An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

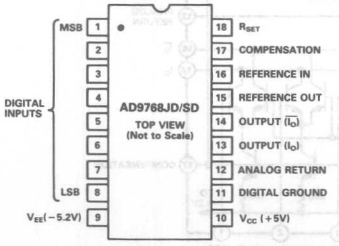
FUNCTIONAL BLOCK DIAGRAM



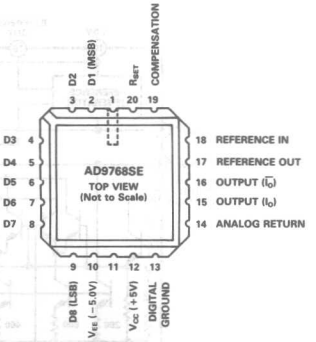
The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

AD9768JD/SD PIN CONNECTIONS



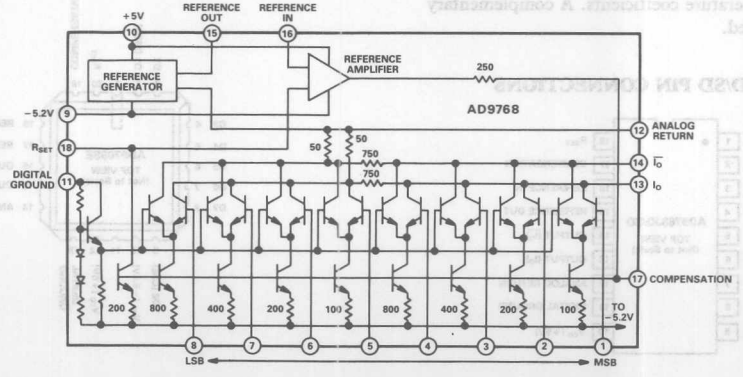
AD9768SE PIN CONNECTIONS



RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	μA	78
ACCURACY[1]		
Differential Nonlinearity	± % FS	0.2
Integral Nonlinearity	± % FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	μA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (−1.26V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	−0.9
"0" =	V	−1.7
Coding		Binary (BIN) = Unipolar Out Offset Binary (OBN) = Bipolar Out
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
$\overline{I_{OUT}}$ (@ Pin 14)		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V (Pin 13)	−0.7 to +3.0
	V (Pin 14)	−1.1 to +3.0
Impedance	Ω (±15%)	750
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/μs	400
Update Rate	MSPS	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	−1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to −1.1 (−2)
Current-Multiplying Mode	mA (max)	0 to −5 (−7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	−0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –		Measured at Pin 13; Digital "0" Applied to Bits 1-8: $-0.1\ V_M$ Input = 0mA I_{OUT} $-1.1\ V_M$ Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: $-0.1\ V_M$ Input = 1mA I_{OUT} $-1.1\ V_M$ Input = 20mA I_{OUT}
Large Signal Bandwidth (−3dB Point)	kHz	250
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –		Measured at Pin 13; Digital "0" Applied to Bits 1-8: 1mA I_M Input = 0mA I_{OUT} 5mA I_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: 1mA I_M Input = 4mA I_{OUT} 5mA I_M Input = 20mA I_{OUT}
Large Signal Bandwidth (−3dB Point)	MHz	40
POWER REQUIREMENTS		
−5.2V ±0.25	mA (max)	66 (70)
+5.0V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating		
AD9768JD	°C	0 to +70
AD9768SD/SE	°C	−55 to +125
Storage	°C	−55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θ_{JA} (Free Air)	°C/W	90
Junction to Case, θ_{JA}	°C/W	20
PACKAGE OPTION[8]		
Ceramic (D-18)		AD9768JD AD9768SD
LCC (E-20A)		AD9768SE

NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{SET} = 0V.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6]Case temperature.
[7]Maximum junction temperature 125°C.
[8]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

Specifications subject to change without notice.



AD9768SD D/A Schematic

THEORY OF OPERATION

Refer to the AD9768SD schematic.

The transistors pictured on the bottom of the diagram, connected to paired transistors in the middle of the schematic, are current sources which are always "on". The paired transistors are differential current switches, designed to steer current from the current sources to either pin 13 (I_O) or pin 14 ($\overline{I_O}$).

Digital inputs applied to pins 1-8 determine which transistors will be operating in each pair and establish what current will flow at pins 13 and 14.

The transistor on the extreme left of the schematic is a base reference for the paired current switches and is used to assure the switches will be centered around an ECL voltage swing. The diodes connected to the base of this transistor are temperature compensation devices for the base reference circuit.

There are three different current sources in the AD9768 D/A. The eight transistors shown on the bottom of the schematic are structured as two identical groups of four current sources, each of which is binarily weighted. The MSB group, comprised of the four on the right, is connected to the LSB group through a 15:1 current divider made up of two 50Ω and two 750Ω resistor networks. The geometry of the AD9768 guarantees the binary weighing ratios among the 100, 200, 400 and 800 resistors in each emitter circuit are correct.

The resistor values which are shown indicate the ratios among the resistors, and not their nominal values.

The third current source is a single transistor, pictured in the lower left portion of the schematic with its collector connected to pin 18 R_{SET}. Its function is to help establish the base voltage on the eight current sources; it works in conjunction with the external R_{SET} resistor selected by the user of the AD9768, and the reference amplifier. Current flowing through this transistor is referred to as I_M in the figures and text.

When the AD9768 is operating as a conventional current-output D/A converter, I_M develops a voltage across R_{SET} which is one of the inputs to the on-board reference amplifier shown in the schematic. The other input to this amplifier is the on-chip reference voltage of -1.26 volts.

The output of the reference amplifier adjusts the current-source base reference voltage at pin 17; this, in turn, adjusts the value of I_M in the single-transistor current source and causes it to develop a voltage across R_{SET} which maintains pin 18 at the -1.26 volts of the on-chip reference supply.

To maintain good stability in the internal loop reference amplifier, a ceramic chip capacitor with a nominal value of 0.01μF should be connected to pin 17 COMPENSATION; minimum recommended value for this capacitor is 3900pF.

The temperature coefficient of the load resistor (R_L) can affect the performance of the AD9768 D/A converter, as it can with any current-output converter. The design and use of the AD9768 and its dependence on an external R_{SET} resistor, however, make it sensitive also to the tempco of R_{SET}. The user is cautioned to select R_L and R_{SET} resistors which have low temperature coefficients.

DIGITAL GROUND (pin 11) and ANALOG RETURN (pin 12) are normally connected together; this connection should be made as close as possible to the device case to minimize possible noise problems. The AD9768 D/A is similar to any other high-speed, high performance device: optimum use requires careful attention to all design details, including the layout of the circuit in which the converter is used.

CONVENTIONAL AD9768

Refer to Figure 1, Conventional AD9768SD.

The output current of the AD9768 appears at pin 13 (I_O) and develops a voltage across the load resistor R_L which is based on:

A. I_M (the current flowing through the single-transistor source discussed above)
B. Value of R_L

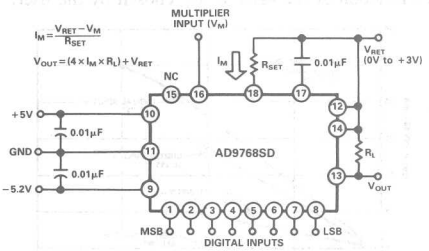


Figure 1. Conventional AD9768SD

I_M is a function of the return voltage (V_{RET}), the reference voltage (V_{REF}), and the value of R_{SET}; all of these are selected by the user for his application. The necessary equations for calculating precise values for each are part of Figure 1. As indicated, the voltage drop across R_L is added to the return voltage; the resulting voltage is the total V_{OUT} of the converter.

VOLTAGE MULTIPLYING MODE

In addition to its use as an ultra-high speed current output D/A converter, the AD9768 can also be used as a two-quadrant multiplying D/A in either a voltage mode or a current mode.

Refer to Figure 2, Multiplying AD9768 (Voltage Mode).

When operating in this mode, the analog output of the AD9768 is influenced by the digital inputs and an external multiplying voltage (V_M) applied to pin 16 REFERENCE IN, which takes the place of the internal reference used when the D/A is operating in a conventional manner.

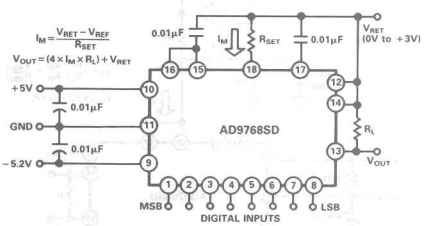


Figure 2. Multiplying AD9768 (Voltage Mode)

The value of I_M flowing through R_{SET} is set by the voltage of V_{RET} minus the multiplying voltage (V_M), divided by R_{SET}; the amount of this current is part of the equation which establishes the analog output (V_{OUT}) of the AD9768 and is chosen by the user for his application. As it is when operating the D/A in a conventional fashion, V_{RET} can be any value between 0 volts and +3 volts. V_M (for purposes of discussion here) is some negative voltage and can be varied over a range which is approximately 1 volt peak-to-peak.

If the load resistor (R_L) has a value of 50 ohms, if R_{SET} has a value of 220 ohms, and if V_{RET} is 0V, the center of the V_M voltage will be −0.6V; and it can vary from −0.1V to −1.1V. Typically, the frequency of these variations has an upper limit of 250kHz when operating in the voltage multiplying mode; that frequency is the 3dB point of the bandwidth of the internal reference amplifier.

The combined effects of variations in V_M and changes in digital input values are shown in Figure 3, I_{OUT} vs. Multiplying Voltage. In this illustration, the ordinate of the graph is expressed in terms of milliamps of I_{OUT} current at pin 13. V_{OUT}, of course, will be a function of the value of R_L chosen by the user.

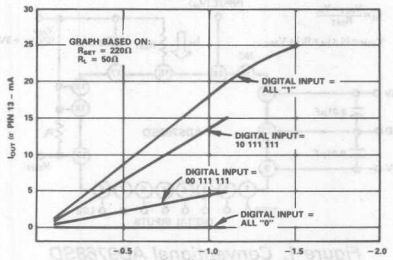


Figure 3. I_{OUT} vs. Multiplying Voltage

The negative value of V_M on the horizontal axis is shown starting at approximately −0.1V, rather than 0V, because the AD9768 must have some small value of voltage applied to perform a multiplying function. For the conditions shown in the figure, output current starts to become nonlinear at approximately 20mA because of the maximum 30mA output drive capabilities of the device. Different values for R_{SET} and R_L would alter the point where limiting first appears.

CURRENT MULTIPLYING MODE

The AD9768 D/A converter can be operated at markedly higher multiplying rates when operated in a current-multiplying mode, as contrasted with the voltage-multiplying mode. Refer to Figure 4, Multiplying AD9768SD (Current Mode).

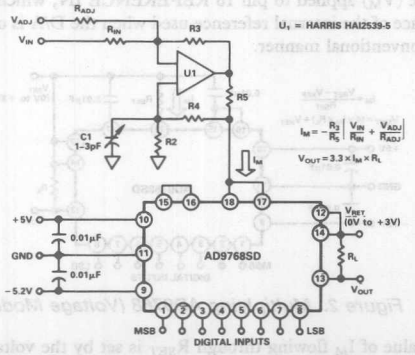


Figure 4. Multiplying AD9768SD (Current Mode)

In this mode, the internal reference amplifier and its inherent frequency limitations are replaced by a current source comprised of U1 and associated circuits. These circuits supply a unipolar current I_M which is one-fourth the full-scale output current (with digital "1" applied to all inputs) and set current flow through the load resistor.

V_{IN} is some voltage chosen by the user for his particular application; the value of this voltage is based in part on the size of the load resistor and the 0mA to 5mA range of I_M. V_{IN} can have frequency components as high as 40MHz. V_{ADJ} and R_{ADJ} provide an offset adjustment to compensate for the dc component of V_{IN} to assure I_M is always a unipolar current between 0mA and 5mA. The values of the required voltages and resistors can be calculated using the equations which are part of Figure 4.

Refer to Figure 5, I_{OUT} vs. Multiplying Current.

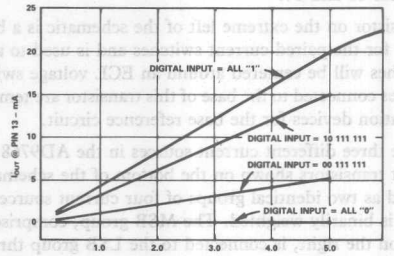


Figure 5. I_{OUT} vs. Multiplying Current

As shown, I_M can vary over the range of 0mA to 5mA; a value of approximately 0.3mA may be the practical lower limit because of nonlinearities at extremely small current levels. These changes in I_M are combined with variations in digital inputs, producing complex changes in the output current (at pin 13) and in V_{OUT}. The "rounding" of the current curve in the graph is the result of I_{OUT} approaching the 30mA maximum drive capabilities of the AD9768 and needs to be taken into account to assure optimum performance in the selected application.

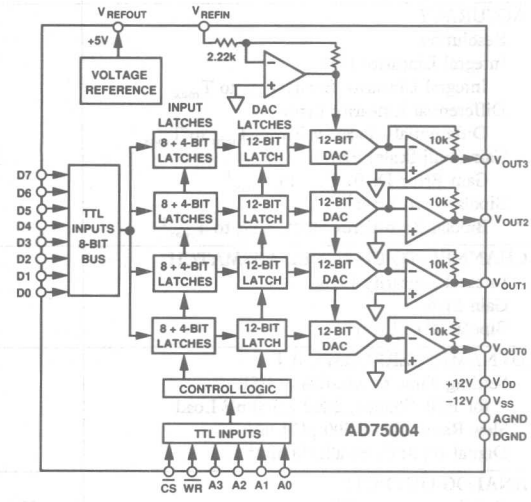
Quad 12-Bit D/A Converter

AD75004

FEATURES

4 Complete 12-Bit D/A Functions
Double-Buffered Latches
Simultaneous Update of All DACs Possible
±5 V Output Range
High Stability Bandgap Reference
Monolithic BiMOS Construction
Guaranteed Monotonic over Temperature
3/4 LSB Linearity Guaranteed over Temperature
4 μs max Settling Time to 0.01%
Operates with ±12 V Supplies
Low Power: 720 mW max Including Reference
TTL/5 V CMOS Compatible Logic Inputs
8-Bit Microprocessor Interface
24-Pin PDIP or 28-Lead PLCC Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75004 contains four complete, voltage output, 12-bit digital-to-analog converters, a high stability bandgap reference, and double-buffered input latches on a single chip. The converters use 12 precision high speed bipolar current steering switches and laser-trimmed thin-film resistor networks to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latches. The design of the input latches allows direct interface to 8-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 50 ns, allowing use with fast microprocessors.

The functional completeness and high performance of the AD75004 results from a combination of advanced switch design, the BiMOS II fabrication process, and proven laser trimming technology. BiMOSII is an epitaxial BiCMOS process optimized for analog and converter functions. The AD75004 is trimmed at the wafer level and is specified to ±1/2 LSB maximum linearity error at 25°C and ±3/4 LSB over the full operating temperature range. The on-chip output amplifiers provide an output range of ±5 V, with 1 LSB equal to 2.44 mV.

The bandgap reference on the chip has low noise, long term stability and temperature drift characteristics comparable to discrete reference diodes. The absolute value of the reference is laser trimmed to +5.00 V with 0.6% maximum error. Its temperature coefficient is also laser trimmed.

Typical full-scale gain TC is 15 ppm/°C. With guaranteed monotonicity over the full temperature range, the AD75004 is well suited for wide temperature range performance.

DIGITAL INPUTS (D0–D7, A0–A3, $\overline{CS}$, $\overline{WR}$)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	**2.0**		**5.5**	V
Input Voltage, Logic "0"	V_{IL}	**0**		**0.8**	V
Input Current, V_{IH} = 5.5 V	I_{IH}			**10**	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			**10**	μA
Input Capacitance	C_{IN}			10	pF
ACCURACY					
Resolution				12	Bits
Integral Linearity Error			±1/4	**±1/2**	LSB
Integral Linearity Error, T_{min} to T_{max}			±1/2	±3/4	LSB
Differential Linearity Error			±1/2	**±3/4**	LSB
Differential Linearity Error, T_{min} to T_{max}			Guaranteed Monotonic		
Gain (Full-Scale) Error[1]			±2	**±10**	LSB
Gain Error Drift, T_{min} to T_{max}[1]			±15	±30	ppm/°C
Bipolar Zero Error[1]			±1	**±2**	LSB
Bipolar Zero Error Drift, T_{min} to T_{max}[1]			±3	±7	ppm/°C
CHANNEL-TO-CHANNEL MISMATCH					
Integral Linearity Error			±1/2	**±1**	LSB
Gain Error[1]			±1	**±4**	LSB
Bipolar Zero Error[1]			±1	**±2**	LSB
DYNAMIC PERFORMANCE					
Settling Time to ±0.01% of FSR					
for FSR Change, 2 kΩ || 500 pF Load			2	4	μs
Slew Rate, 2 kΩ || 500 pF Load		5			V/μs
Digital Input Crosstalk (Static)[2]				–50	dB
ANALOG OUTPUTS					
Full-Scale Range (FSR)	V_{OUT}		±5		V
Output Current	I_{OUT}	±5			mA
Short Circuit Limit Current				**40**	mA
VOLTAGE REFERENCE					
Reference Output Voltage	V_{REFOUT}	**4.97**	5.00	**5.03**	V
Temperature Coefficient			±15	±25	ppm/°C
Reference Output Current[3]		3.0	5.0		mA
Reference Input Voltage	V_{REFIN}	4.5	5.0	5.5	V
Reference Input Current @ 5.0 V	I_{REFIN}			3.0	mA
POWER SUPPLY GAIN SENSITIVITY					
$\Delta Gain/\Delta V_{DD}$, V_{DD} = +10.8 to +13.2 V dc[1]			±15	**±25**	ppm of FSR/%
$\Delta Gain/\Delta V_{SS}$, V_{SS} = −10.8 to −13.2 V dc[1]			±15	**±25**	ppm of FSR/%
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{SS}	**±10.8**	±12	**±13.2**	V
Supply Currents	I_{DD}, I_{SS}		±25	**±30**	mA
TEMPERATURE RANGE					
Specification	T_{min}, T_{max}	0		+70	°C
Storage		−65		+150	°C

NOTES

[1]Gain and bipolar zero errors are measured using internal voltage reference and include its errors.

[2]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2 kΩ || 500 pF load by means of varying the digital input code.

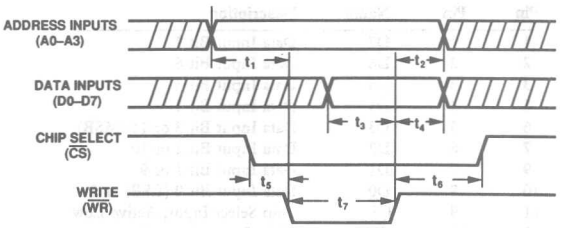
[3]The internal voltage reference is intended to drive on-chip only; buffer it if using it externally.

[4]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

Parameter	Symbol	Min	Units
Address Setup Time	t_1	30	ns
Address Hold Time	t_2	10	ns
Data Setup Time	t_3	10	ns
Data Hold Time	t_4	45	ns
Chip Select to Write Setup Time	t_5	0	ns
Write to Chip Select Hold Time	t_6	0	ns
Write Pulse Width	t_7	50	ns



NOTES
[1]Timing measurement reference level is 1.5 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

	Min	Max	Units	Conditions
V_{DD} to DGND	−0.3	+18	V	
V_{SS} to DGND	−18	+0.3	V	
V_{DD} to V_{SS}	−0.3	+26.4	V	
V_{REFIN} to AGND	−0.3	V_{DD}	V	
Digital Inputs to DGND	−0.3	V_{DD}	V	
AGND to DGND	−0.3	+0.3	V	
Short to AGND on Analog Outputs		Indefinite	sec	
Power Dissipation		1.0	W	$T_A \leq 75°C$
Specification Temperature Range	0	+70	°C	
Storage Temperature	−65	+150	°C	
Lead Temperature		+300	°C	Soldering, 10 seconds

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

Control and Address Lines						
$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No operation
X	1	X	X	X	X	No operation
0	0	0	0	A1*	A0*	8 LSBs → one input latch
0	0	0	1	A1*	A0*	4 MSBs → one input latch
0	0	1	0	A1*	A0*	Update one DAC latch
0	0	1	1	X	X	Update all 4 DAC latches

NOTE
*The A1 and A0 inputs specify the relevant channel.

A1	A0	Channel
0	0	0
0	1	1
1	0	2
1	1	3

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN DESCRIPTION

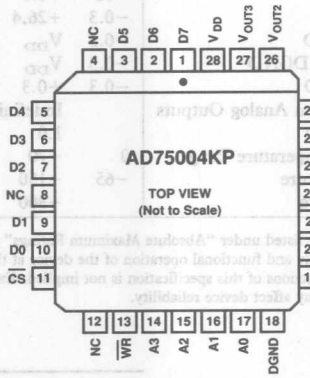
PLCC Pin	Plastic DIP Pin	Name	Description
1	1	D7	Data Input Bit 7
2	2	D6	Data Input Bit 6
3	3	D5	Data Input Bit 5
5	4	D4	Data Input Bit 4
6	5	D3	Data Input Bit 3 or 11 (MSB)
7	6	D2	Data Input Bit 2 or 10
9	7	D1	Data Input Bit 1 or 9
10	8	D0	Data Input Bit 0 (LSB) or 8
11	9	$\overline{CS}$	Chip Select Input; Active Low
13	10	$\overline{WR}$	Write Input; Active Low
14	11	A3	Address Input Bit 3 (MSB)
15	12	A2	Address Input Bit 2
16	13	A1	Address Input Bit 1
17	14	A0	Address Input Bit 0 (LSB)
18	15	DGND	Digital Ground
19	16	AGND	Analog Ground
20	17	V_{SS}	−12 V Power Supply
21	18	V_{REFOUT}	+5 V Reference Output
22	19	V_{REFIN}	Reference Input
23	20	V_{OUT0}	Analog Output 0
24	21	V_{OUT1}	Analog Output 1
26	22	V_{OUT2}	Analog Output 2
27	23	V_{OUT3}	Analog Output 3
28	24	V_{DD}	+12 V Power Supply
4	–	NC	No Internal Connection
8	–	NC	No Internal Connection
12	–	NC	No Internal Connection
25	–	NC	No Internal Connection

PIN CONFIGURATIONS

24-Pin Plastic DIP



28-Pin PLCC



BINARY CODE TABLE

Twos Complement Value in DAC Latch			Analog Output Voltage
MSB		LSB	
0111	1111	1111	(2047/2048) * V_{REFIN}
0000	0000	0001	(1/2048) * V_{REFIN}
0000	0000	0000	0 V
1111	1111	1111	− (1/2048) * V_{REFIN}
1000	0000	0000	$-V_{REFIN}$

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD75004KN	0°C to +70°C	N-24A
AD75004KP	0°C to +70°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

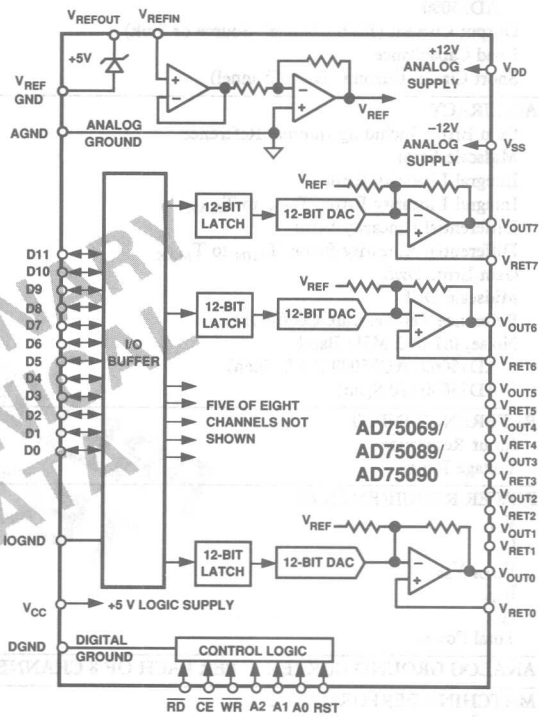
Monolithic Octal 12-Bit DACPORTs

AD75069/AD75089/AD75090

FEATURES
- Eight Complete Voltage Output DACs
- On-Chip Voltage Reference
- On-Chip Data Latches with Readback Feature
- Variety of Output Voltage Ranges: +7.5 V/−2.5 V, ± 5 V, ±10 V
- Compact 44-Pin PLCC and Ceramic JLCC Packages

APPLICATIONS
- Automatic Test Equipment
- Instrumentation
- Avionics
- Robotics
- Process Control

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75069/AD75089/AD75090 DACPORTs™ contain eight complete 12-bit, voltage output digital-to-analog converters in one monolithic IC. They thus offer the highest density 12-bit D/A functions available. The three models differ in their output voltage ranges: the AD75069 outputs −2.5 V to +7.5 V, the AD75089 outputs ±5 V, and the AD75090 outputs ±10 V.

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors that are laser-trimmed to achieve guaranteed monotonicity over the full operating temperature range. DAC-to-DAC matching performance is specified.

The output amplifier combines the best features of bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10 μs, and each output can drive a 2 mA, 500 pF load. Short circuit protection allows indefinite shorts to V_{CC}, V_{DD}, V_{SS}, and GND.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows these DACPORTs to interface with most microprocessors through a single 12-bit wide bus. A readback feature allows the internal DAC registers to be read back through the digital port, as 12-bit words. When disabled, the readback drivers are placed in a high impedance mode.

A RESET control pin is provided to allow simultaneous asynchronous reset of all DAC data latches, causing the DAC outputs to go to the negative extreme of their range.

The analog portion of these DACPORTs consists of eight DAC cells, eight output amplifiers, a voltage reference, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-chip application resistors and output amplifier. The chip may be operated from the internal reference or an external reference.

The high performance and functional completeness of these DACPORTs result from their fabrication in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features bipolar transistors for precise analog circuitry, CMOS transistors for dense logic and analog switches, laser-trimmed thin-film resistors and double-level metal interconnects.

PRELIMINARY TECHNICAL DATA

DACPORT is a trademark of Analog Devices, Inc.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD75069/AD75089/AD75090—SPECIFICATIONS

(V_{CC} = +5 V, V_{DD} = +12 V, V_{SS} = −12 V, V_{REF} = +5 V, T_A = +25°C unless otherwise noted.)

Parameter	Min	Typ	Max	Units
RESOLUTION		12		Bits
ANALOG OUTPUT				
Voltage Range, V_{OUT} max to V_{OUT} min				
AD75069		−2.5/+7.5		Volts
AD75089		±5		Volts
AD75090		±10		Volts
Output Current (Each Channel, Source or Sink)	2			mA
Load Capacitance			500	pF
Short Circuit Current (Each Channel)		25	40	mA
ACCURACY				
Gain Error, Including Internal Reference	−10	±5	10	LSB
Midscale Error	−4	±1/2	4	LSB
Integral Linearity Error	−1/2	±1/4	1/2	LSB
Integral Linearity Error, T_{MIN} to T_{MAX}	−1.5	±1/2	+1.5	LSB
Differential Linearity Error	−1/2	±1/4	1/2	LSB
Differential Linearity Error, T_{MIN} to T_{MAX}	−3/4	±1/2	+3/4	LSB
Gain Error Drift	−10	±5	10	ppm of FSR/°C
Midscale Drift	−10	±5	10	ppm of FSR/°C
Reference Temperature Coefficient	−25	±15	25	ppm/°C
Noise, 0.1 to 2 MHz Band				
AD75069, AD75089 (10 V Span)			300	μV rms
AD75090 (20 Span)			600	μV rms
REFERENCE INPUT				
Input Resistance	2.0	10		MΩ
Voltage Range	−3.0		+5.5	Volts
POWER REQUIREMENTS				
V_{CC}	4.5	5.0	5.5	Volts
I_{CC}		0.1	1	mA
V_{DD}, V_{SS}	±11.4	±12.0	±13.2	Volts
I_{DD}		15	20	mA
I_{SS}		−14	−16	mA
Total Power		350	432	mW
ANALOG GROUND CURRENT[1] PER EACH OF 8 CHANNELS	−600		+600	μA
MATCHING PERFORMANCE				
Gain[2]	−5	±2.5	5	LSB
Midscale[3]	−4	±2	4	LSB
Linearity[4]	−1	±1/2	1	LSB
CROSSTALK				
Analog (DC)			−90	dB
Digital (Transient)			−60	dB
DYNAMIC PERFORMANCE (R_L = 5 kΩ, C_L = 500 pF)				
Slew Rate	2.0	2.5		V/μs
Settling Time to ±1/2 LSB				
V_{OUT} max to V_{OUT} min or V_{OUT} min to V_{OUT} max				
AD75069, AD75089 (10 V Span)		6	8	μs
AD75090 (20 V Span)		8	10	μs
POWER SUPPLY GAIN SENSITIVITY				
11.4 V ≤ V_{DD} ≤ 13.2 V		±6	±10	ppm/%
−13.2 V ≤ V_{SS} ≤ −11.4 V		±1	±2	ppm/%

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0			Volts
V_{IL}	0		0.8	Volts
I_{IH} @ V_{IN} = V_{LL}	**−10**	±1	**10**	µA
I_{IL} @ V_{IN} = DGND	**−10**	±1	**10**	µA
DIGITAL OUTPUTS				
V_{OL} @ I_{SINK} = 1.6 mA			0.4	Volts
V_{OH} @ I_{SOURCE} = 0.5 mA	2.4			Volts
DIGITAL TIMING[5]				
Data Write Mode (Figure 1)				
Data Setup Time, t_{DSU}	30			ns
Address Setup Time, t_{ASU}	30			ns
Chip Enable-Write Time, t_{CEW}	10			ns
Write Pulse Width, T_W	80			ns
Write-Chip Enable Time, t_{WCE}	0			ns
Address Hold Time, t_{AH}	20			ns
Data Hold Time, t_{DH}	50			ns
Data Readback Mode (Figure 2)				
Address Setup Time , t_{ASU}	30			ns
Chip Enable-Read Time, t_{CER}	0			ns
Read Pulse Width, t_R	70			ns
Access Time from Read, t_{RD}			75	ns
Access Time from Chip Enable, t_{CED}			85	ns
Access Time from Address Change, t_{AD}			120	ns
Data Bus Release Time, t_{REL}			30	ns
Read-Chip Enable Time, t_{RCE}	0			ns
Address Hold Time, t_{AH}	20			ns
Asynchronous Reset				
Reset Pulse Width, t_{RST}	80			ns
TEMPERATURE RANGE (T_{MIN}, T_{MAX})				
A Versions	−40		+85	°C
J Versions	0		+70	°C

PRELIMINARY TECHNICAL DATA

NOTES
[1]Analog ground current is input code dependent.
[2]Gain matching error is the largest difference in gain error between any two DACs in one package.
[3]Midscale matching error is the largest difference in midscale values between any two DACs in one package.
[4]Linearity matching error is the difference in the worst case integral linearity error between any two DACs in one package.
[5]Reference level for timing measurements = 1.5 V.

See definitions of specifications later on in this data sheet.
Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

TIMING DIAGRAMS

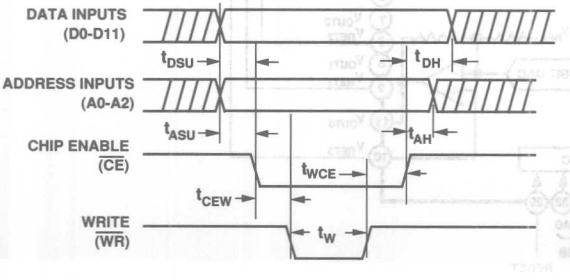


Figure 1. Write Timing Diagram

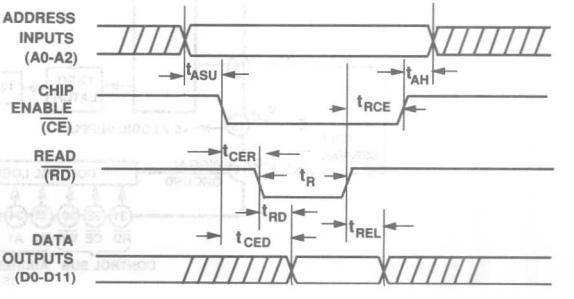


Figure 2. Readback Timing Diagram

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

V_{DD} to AGND . . . . . 0 V to +18 V
V_{SS} to AGND . . . . . −18 V to 0 V
AGND to DGND . . . . . −1 V to +1 V
AGND to VREFGND . . . . . ±13.2 V
AGND to VRET0–7 . . . . . ±13.2 V
V_{REFIN} Input . . . . . V_{DD} to V_{SS}
V_{DD} to V_{SS} . . . . . 0 V to +26.4 V
Digital Inputs . . . . . −0.3 V to +7 V
Analog Outputs
. . . . . Indefinite Shorts to V_{CC},V_{DD},V_{SS}, and AGND
Soldering Temperature . . . . . +300°C, 10 sec
Power Dissipation . . . . . 1000 mW

ll the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Output Voltage Range	Temperature Range	Package Option*
AD75069JP	−2.5 V/+7.5 V	0°C to +70°C	P-44A
AD75069AJ	−2.5 V/+7.5 V	−40°C to +85°C	J-44A
AD75089JP	± 5 V	0°C to +70°C	P-44A
AD75089AJ	± 5 V	−40°C to +85°C	J-44A
AD75090JP	±10 V	0°C to +70°C	P-44A
AD75090AJ	±10 V	−40°C to +85°C	J-44A

*J = J-Leaded Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier (PLCC) package. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PRELIMINARY TECHNICAL DATA

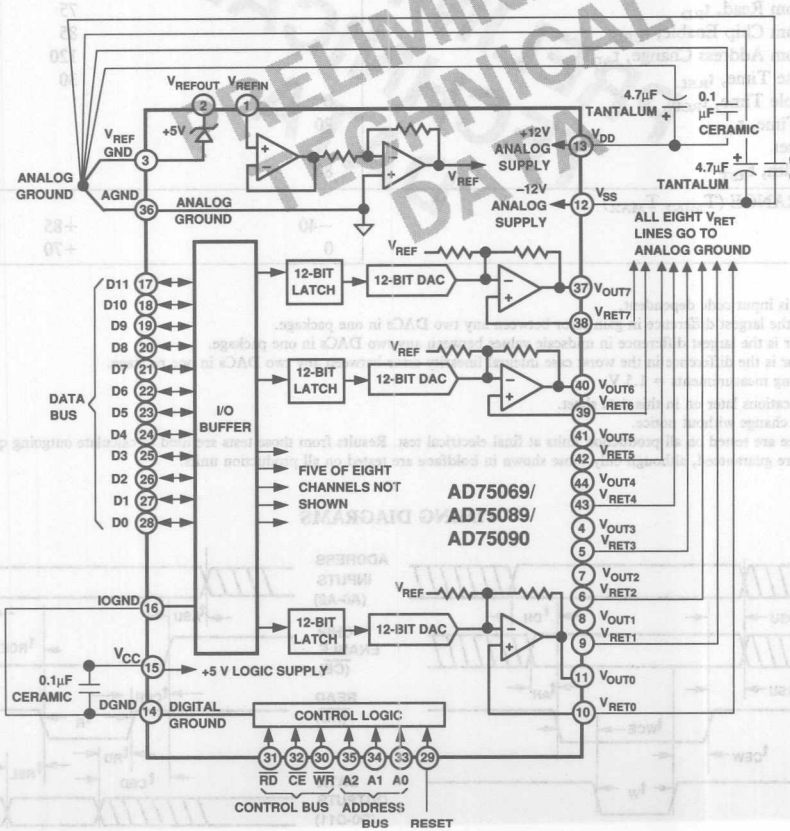
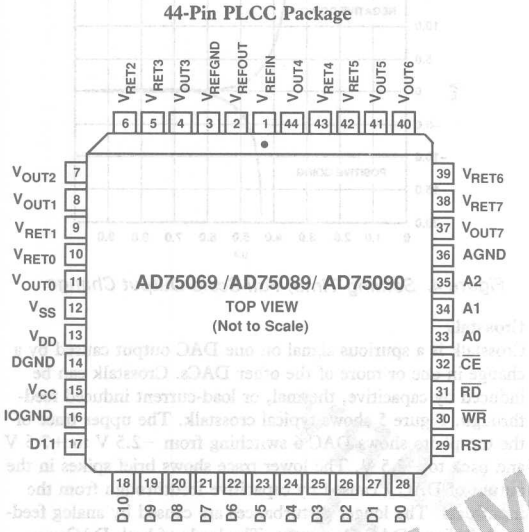


Figure 3. Recommended Circuit Schematic

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PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Name	Description
1	V_{REFIN}	Reference Input
2	V_{REFOUT}	5 V Reference Output
3	V_{REFGND}	Reference Ground
4	V_{OUT3}	Analog Output 3
5	V_{RET3}	Analog Return 3
6	V_{RET2}	Analog Return 2
7	V_{OUT2}	Analog Output 2
8	V_{OUT1}	Analog Output 1
9	V_{RET1}	Analog Return 1
10	V_{RET0}	Analog Return 0
11	V_{OUT0}	Analog Output 0
12	V_{SS}	−12 V Analog Power Supply
13	V_{DD}	+12 V Analog Power Supply
14	DGND	Digital Ground
15	V_{CC}	+5 V Digital Power Supply
16	IOGND	Bus Interface Ground
17	D11	Data Input Bit 11 (MSB)
18	D10	Data Input Bit 10
19	D9	Data Input Bit 9
20	D8	Data Input Bit 8
21	D7	Data Input Bit 7
22	D6	Data Input Bit 6
23	D5	Data Input Bit 5
24	D4	Data Input Bit 4
25	D3	Data Input Bit 3
26	D2	Data Input Bit 2
27	D1	Data Input Bit 1
28	D0	Data Input Bit 0 (LSB)
29	RST	Reset Input; Active High
30	$\overline{WR}$	Write Input; Active Low
31	$\overline{RD}$	Read Input; Active Low
32	$\overline{CE}$	Chip Enable Input; Active Low
33	A0	Address Input Bit 0 (LSB)
34	A1	Address Input Bit 1
35	A2	Address Input Bit 2 (MSB)
36	AGND	Analog Ground
37	V_{OUT7}	Analog Output 7
38	V_{RET7}	Analog Return 7
39	V_{RET6}	Analog Return 6
40	V_{OUT6}	Analog Output 6
41	V_{OUT5}	Analog Output 5
42	V_{RET5}	Analog Return 5
43	V_{RET4}	Analog Return 4
44	V_{OUT4}	Analog Output 4

DEFINITIONS OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR: Integral linearity error is the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from −full scale to +full scale) for any digital input code.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD75069/AD75089/AD75090 are monotonic over their full operating temperature range.

DIFFERENTIAL LINEARITY ERROR: Monotonic behavior requires that the differential linearity error be less than 1 LSB over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 V output span, a change of 1 LSB in digital input code should result in a 2.44 mV change in the analog output (1 LSB = 10 V/4096 = 2.44 mV). If in actual use, however, a 1 LSB change in the input code results in a change of only 0.61 mV (1/4 LSB) in analog output, the differential nonlinearity error would be −1.83 mV, or −3/4 LSB.

GAIN ERROR: DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

MIDSCALE ERROR: Midscale error is the difference between the ideal midscale output and the actual output of a DAC when the input code is loaded with the MSB = "1" and the rest of the bits = "0."

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

CROSSTALK: Crosstalk is the change in an output caused by a change in one or more of the other inputs or outputs. It is due to capacitive and thermal coupling between channels.

FULL-SCALE RANGE: FSR is 20 V for ±10 V range and 10 V for ±5 V and −2.5/+7.5 V ranges.

TRANSISTOR COUNT

The AD75069/AD75089/AD75090 contains 5,225 transistors.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

BINARY CODE TABLE

Offset Binary Value in DAC Latch	Analog Output Voltage
MSB LSB	
1111 1111 1111	V_{OUT} max
1000 0000 0000	Midscale = (V_{OUT} max + 1 LSB − V_{OUT} min)/2
0000 0000 0000	V_{OUT} min

ANALOG CIRCUIT CONSIDERATIONS

Grounding Recommendations

The AD75069/AD75089/AD75090 have twelve pins for analog and digital grounds, designated AGND, V_{RET0}–V_{RET7}, V_{REFGND}, IOGND, and DGND. The AGND pin is the ground reference point for the device. V_{REFGND} is the ground reference point for the on-chip voltage reference. V_{RET0} through V_{RET7} are the 8 ground return pins for the 8 DACs and their output amplifiers. The 10 analog ground pins should be connected radially to the analog ground point in the system. The external reference and any external loads should also be returned to the analog ground point. To minimize crosstalk, all paths to the single analog ground point must be short and direct.

The IOGND and DGND pins should be connected to the digital ground point in the circuit. These pins return current from the bus interface and logic portions, respectively, of the AD75069/AD75089/AD75090 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection may be broken or otherwise disconnected, then two diodes should be connected in inverse parallel between the analog and digital ground pins of the AD75069/AD75089/AD75090 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD75069/AD75089/AD75090 require three power supplies for proper operation. V_{CC} powers the logic portions of the device and requires +5 volts. V_{DD} and V_{SS} power the remaining portions of the circuitry and require ±12 V.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. Recommended values are 4.7 μF tantalum and 0.1 μF ceramic from V_{DD} and V_{SS} to analog ground, and 0.1 μF from V_{CC} to digital ground.

Voltage Reference

The AD75069/AD75089/AD75090 are designed to operate from a reference voltage of 5 V. The internal reference can serve the entire chip. If superior tolerance, PSRR, or temperature performance are needed, external devices, such as the AD586, may be used.

Output Considerations

Each DAC output can source or sink ±2 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 500 pF can be accommodated with no effect on stability.

AD75069/AD75089/AD75090 output voltage settling time is 10 μs maximum. Figure 4 shows the output voltage settling time of the AD75069 with a fixed 5 V reference and all bits switched from 1 to 0 and from 0 to 1.

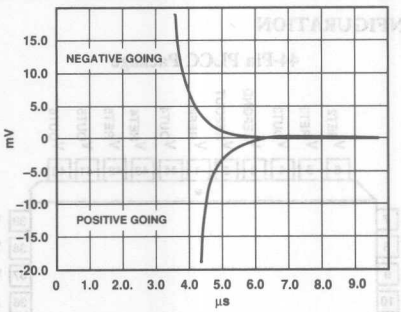


Figure 4. Settling Time; Full-Scale Output Change

Crosstalk

Crosstalk is a spurious signal on one DAC output caused by a change in one or more of the other DACs. Crosstalk can be induced by capacitive, thermal, or load-current induced feedthrough. Figure 5 shows typical crosstalk. The upper trace of the top photo shows DAC 6 switching from −2.5 V to +7.5 V and back to −2.5 V. The lower trace shows brief spikes in the output of DAC 7 caused by capacitive feedthrough from the input data. The longer disturbances are caused by analog feedthrough from DAC 6's output. The loads of both DACs are 5 kΩ in parallel with 500 pF. The lower photo shows the detail of the falling edge of DAC 6 (large trace) and the effect on DAC 7 (middle trace) under the same conditions.

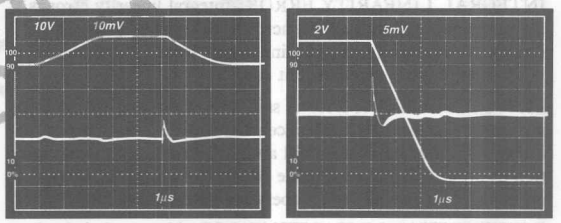


Figure 5. Output Crosstalk

DIGITAL INTERFACING

To write to the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Write ($\overline{WR}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{WR}$ connects to the system write strobe.

If the data is changed while $\overline{CE}$ and $\overline{WR}$ are low, the DAC register is transparent, and it will follow the input data.

Readback

To read data back from the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Read ($\overline{RD}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{RD}$ connects to the system read strobe.

If the address is changed while $\overline{CE}$ and $\overline{RD}$ are low, the data output will follow the selected address after a delay of t_{AD}.

Data Reset

To reset all data latches asynchronously, take Reset (RST) high. This clears all data latches and causes the DAC outputs to go to the negative end of their output range, i.e., −2.5 V for the AD75069, −5 V for the AD75089, and −10 V for the AD75090.

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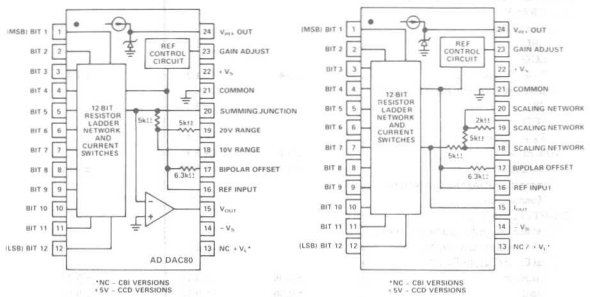
Complete Low Cost 12-Bit D/A Converters

AD DAC80/AD DAC85/AD DAC87

FEATURES

- Single Chip Construction
- On-Board Output Amplifier
- Low Power Dissipation: 300mW
- Monotonicity Guaranteed over Temperature
- Guaranteed for Operation with ±12V Supplies
- Improved Replacement for Standard DAC80, DAC800 HI-5680
- High Stability, High Current Output Buried Zener Reference
- Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity
- Low Cost Plastic Packaging

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD DAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The AD DAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300mW which not only improves reliability but also improves long term stability.

The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The AD DAC80 Series is available in three performance grades and two package types. The AD DAC80 is specified for use over the 0 to +70°C temperature range and is available in both plastic and ceramic DIP packages. The AD DAC85 and AD DAC87 are available in hermetically sealed ceramic packages and are specified for the −25°C to +85°C and −55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The AD DAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs, when properly compensated.
4. The precision buried Zener reference can supply up to 2.5mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

PRODUCT OFFERING

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions are delineated in this data sheet.

	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250			250			250	μA
I_{IL} (V_{IL} = 0.8V)			100			100			100	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD										LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C										
CBI			±3/4			±3/4			±3/4	LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±3/4			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05	±0.1		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	−25		+85	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V_S)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ||500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ± 10%, 5V supply when applicable			±0.002			±0.002			±0.002	% of FSR/%V_S
±12V ± 5%			±0.002			±0.002			±0.002	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies	±11.4[7]		±16.5	±11.4[7]		±16.5	±11.4[7]		±16.5	V
Logic Supplies									V	
Supply Drain										
+12, +15V		5	10		5	10		5	10	mA
−12, −15V		14	20		14	20		14	20	mA
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+125	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_P = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TECHNOLOGY	Hybrid			Hybrid			Hybrid			
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD			3			3			3	Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI		±1/4	±1/2			±1/2			±1/2	LSB[1]
CCD		±1/8	±1/4			±1/4			±1/4	LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±1/2	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2	±3/4		±1/2			±1/2		LSB
CCD		±1/4	±1/2		±1/2			±1/2		LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1			±0.1		% FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05			±0.05		%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	0		+70	−25		+85	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20							ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15							% of FSR
Bipolar		±0.06	±0.10							% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±5	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3		±1			±1		ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ||500pF load)										
with 10kΩ Feedback		5			5			5		μs
with 5kΩ Feedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate	10	15			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR										
for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD		±10			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2			3.2		kΩ
– Unipolar		6.6			6.6			6.6		kΩ
Compliance		−1.5, +10			−2.5, +10			−2.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20		±10	±20	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14		±16	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	+4.5		+16	+4.5		+15.5	+4.5		+15.5	V
Supply Drain[7]										
+15V		10	20		15	20		15	20	mA
−15V		20	35		25	30		25	30	mA
+5V[8]		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating	−25		+85	−25		+85	−55		+125	°C
Storage	−55		+130	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
[8]+5V supply required only for CCD versions.
Specifications subject to change without notice.

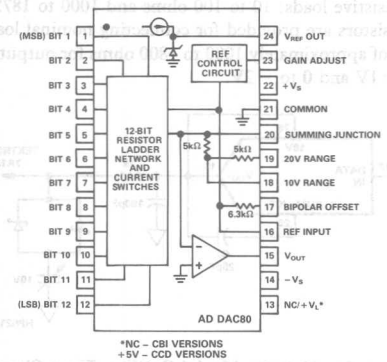
AD DAC80/AD DAC85/AD DAC87 — SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC85LD Min	AD DAC85LD Typ	AD DAC85LD Max	AD DAC85MIL Min	AD DAC85MIL Typ	AD DAC85MIL Max	AD DAC87 Min	AD DAC87 Typ	AD DAC87 Max	Units
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2		±1/4	±1/2	LSB[1]
CCD		–			–			–		LSB
T_A @ T_{min} to T_{max}			±1/2			±3/4			±3/4	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2			±1/2			±1/2		LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1			±0.1			±0.1	±0.2	% FSR[3]
Offset Error[2]		±0.05			±0.05			±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	−25		+85	−55		+125	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		–			–			±15	±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		–			–			±0.13	±0.30	% of FSR
Bipolar		–			–			±0.12	±0.24	% of FSR
Gain										
Including Internal Reference			±10			±20		±10	±25	ppm of FSR/°C
Excluding Internal Reference								±5	±10	ppm of FSR/°C
Unipolar Offset		±1			±2			±1	±3	ppm of FSR/°C
Bipolar Offset			±5			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ|500pF load)										
with 10kΩFeedback		5			5			5		μs
with 5kΩFeedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate		20			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2		2.5	3.2	4.1	kΩ
– Unipolar		6.6			6.6		5.0	6.6	8.2	kΩ
Compliance		−2.5, +10			−2.5, +10			−1.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	20		10	20		±5	10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002	±0.003	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		+15.5	+4.5		+15.5	+4.5		+16.5	V
Supply Drain[7]										
+15V		15	20		15	20		10	20	mA
−15V		25	30		25	30		20	35	mA
+5V[8]		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	−25		+85	−55		+125	−55		+125	°C
Operating	−55		+125	−55		+125	−55		+125	°C
Storage	−55		+125	−55		+120	−65		+150	°C

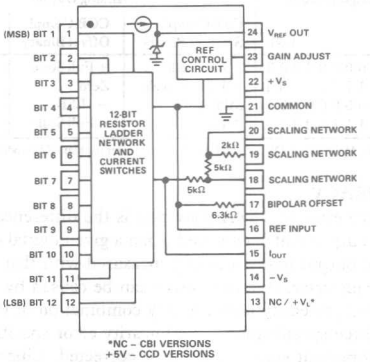
NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_P = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
[8]+5V supply required only for CCD versions.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground . . . . . 0V to +18V
$-V_S$ to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 1 to 12) to Power Ground . . . −1.0V to +7V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite short to power ground or $+V_S$



Voltage Model Functional Diagram and Pin Configuration



Current Model Functional Diagram and Pin Configuration

ORDERING GUIDE

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Option*
AD DAC80N-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	N-24
AD DAC80D-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	D-24
AD DAC85D-CBI-V	Binary	Voltage	Monolithic	−25°C to +85°C	±1/2LSB	D-24
AD DAC87D-CBI-V	Binary	Voltage	Monolithic	−55°C to +125°C	±1/2LSB	D-24
AD DAC80-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CBI-V**	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CBI-I**	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CCD-V**	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CCD-I**	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85C-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC85-CCD-I	Binary Coded Decimal	Current	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC87-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC87-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A

*For outline information see Package Information section.
**Z-Suffix devices guarantee performance of 0 to +5V and ±5V spans with minimum supply voltages of ±11.4V.

DIGITAL INPUT CODES

The AD DAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

Table I. Digital Input Codes

Digital Input		Analog Output		
MSB	LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
0 0 0 0 0 0 0 0 0 0 0 0		+ Full Scale	+ Full Scale	− 1LSB
0 1 1 1 1 1 1 1 1 1 1 1		+ 1/2 Full Scale	Zero	− Full Scale
1 0 0 0 0 0 0 0 0 0 0 0		Mid-Scale	− 1LSB	+ Full Scale
1 1 1 1 1 1 1 1 1 1 1 1		Zero	− Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2LSB means that the output voltage step sizes can range from 1/2LSB to 1 1/2LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models. Three settling times are specified to ± 0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25pF as shown in Figure 1a.

Current Output Models. Two settling times are specified to ± 0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage ranges of ± 1V and 0 to −2V.

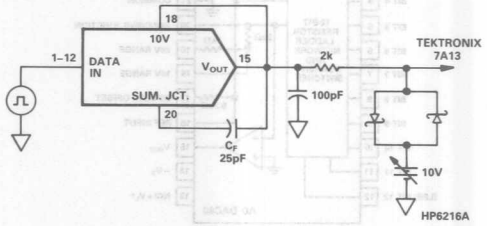


Figure 1a. Voltage Model Settling Time Circuit

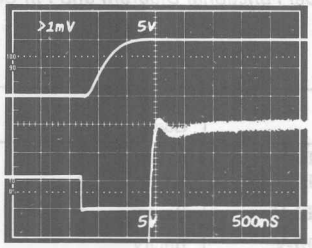


Figure 1b. Voltage Model Settling Time C_F = 25pF

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ± 1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 2. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input codes, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

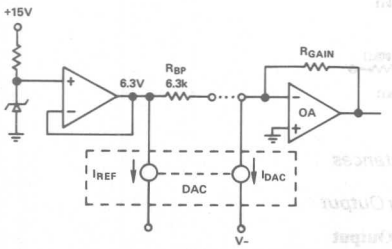


Figure 2. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ± 1/2LSB max and the differential linearity error of ± 3/4LSB max guarantee monotonic performance over the specified range. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 3. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 2) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 3. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 10ppm/°C max.

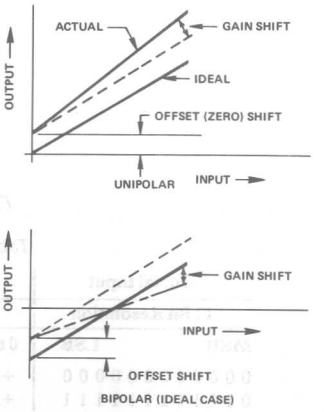


Figure 3. Unipolar and Bipolar Drifts

Using the AD DAC80 Series

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the AD DAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 6 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

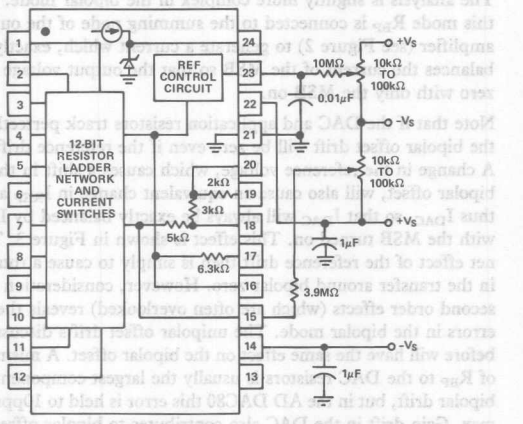


Figure 4. External Adjustment and Voltage Supply Connection Diagram, Current Model

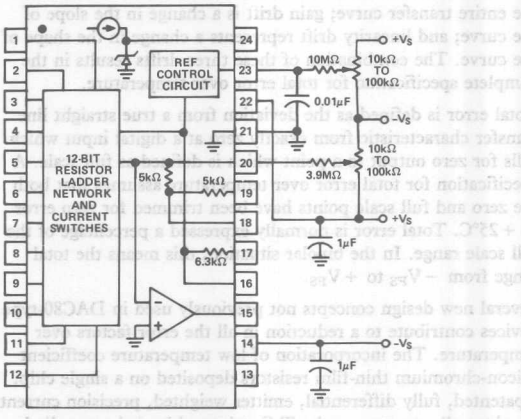


Figure 5. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

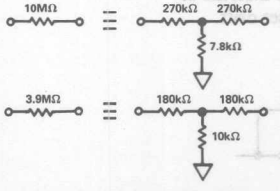


Figure 6. Equivalent Resistances

Table II. Digital Input/Analog Output

Digital Input		Analog Output			
12 Bit Resolution		Voltage*		Current	
MSB	LSB	0 to +10V	±10V	0 to −2mA	±1mA
0 0 0 0 0 0 0 0 0 0 0 0		+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
0 1 1 1 1 1 1 1 1 1 1 1		+5.0000V	0.0000V	−1.0000mA	0.0000mA
1 0 0 0 0 0 0 0 0 0 0 0		+4.9976V	4.88mV	−0.9995mA	+0.0005mA
1 1 1 1 1 1 1 1 1 1 1 1		0.0000V	−10.0000V	0.0000mA	−1.00mA
1LSB		2.44mV	−0.0049V	0.488μA	0.488μA

*To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 7).

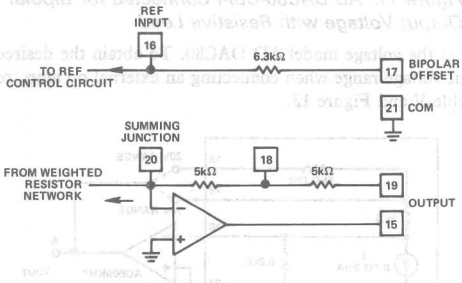


Figure 7. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10kΩ feedback resistor; 3 microseconds for a 5kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 8 and 9. External R_{LS} resistors are required to produce exactly 0 to −2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

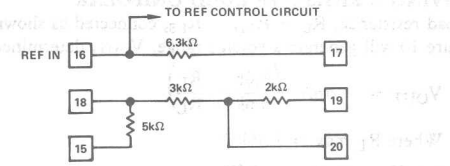


Figure 8. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to −2V. These resistors (R_{LI}: TCR = 20ppm/°C) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

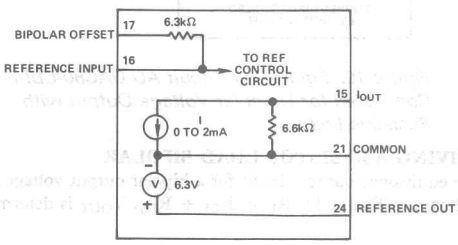


Figure 9. AD DAC80 Current Model Equivalent Output Circuit

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table IV. Current Model/Resistive Load Connections

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LI} Connections			Reference	Bipolar Offset	
				Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to −2V	0.968kΩ	210Ω	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)
COB or CTC	±1V	1.2kΩ	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)
CCD	0 to ±2V	3kΩ	N/A	N.C.	21	N.C.	24	N.C.	N/A

Figure 10 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = −2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to −2V. With R_{LS} = 0, V_{OUT} = −1.69V.

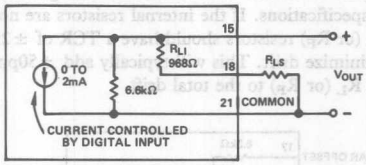


Figure 10. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

and V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 12,

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the



Figure 11. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 12.

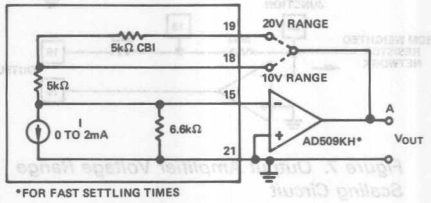


Figure 12. External Op Amp–Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

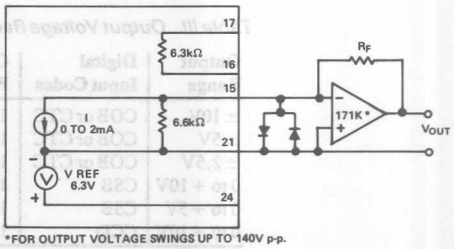


Figure 13. External Op Amp–Using External Feedback Resistors

Table V. External Op Amp Voltage Mode Connections

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24

ANALOG DEVICES

CMOS 80 MHz, Triple 8-Bit Video DAC

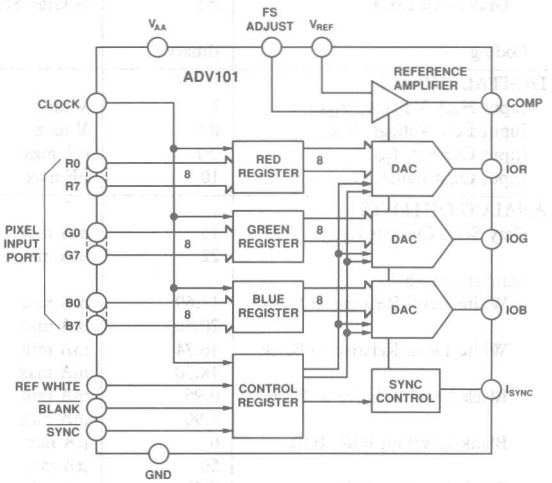
ADV101

FEATURES
- 80 MHz Pipelined Operation
- Triple 8-Bit D/A Converters
- RS-343A/RS-170 Compatible Outputs
- TTL Compatible Inputs
- +5 V CMOS Monolithic Construction
- 40-Pin DIP or 44-Pin PLCC Package
- Plug-In Replacement for BT101
- Power Dissipation: 400 mW

APPLICATIONS
- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Video Signal Reconstruction
- Desktop Publishing

SPEED GRADES
- 80 MHz
- 50 MHz
- 30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV101 (ADV®) is a digital-to-analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV101 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV101 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV101 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6″, 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential non-linearity of ±05 LSB. Integral nonlinearity is guaranteed to be a maximum of ± 1 LSB.

ADV is a registered trademark of Analog Devices Inc.

ADV101—SPECIFICATIONS

(V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±0.5	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}* 12,082/R_{SET}) mA IOR, IOB = (V_{REF}* 8,627/R_{SET}) mA
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	9.5	mA max	
Sync Level on IOG	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	2	% typ	
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	+10	μA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	
Analog Output Skew	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[2]Sample tested at +25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

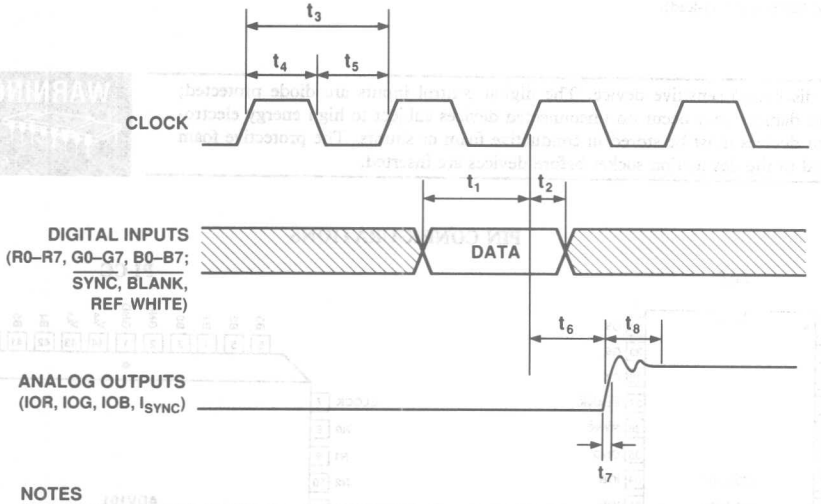
[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{max}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ORDERING GUIDE

Model	Speed	Temperature Range	Package Option[1]
ADV101KN80	80 MHz	0°C to +70°C	N-40A
ADV101KN50	50 MHz	0°C to +70°C	N-40A
ADV101KN30	30 MHz	0°C to +70°C	N-40A
ADV101KP80[2]	80 MHz	0°C to +70°C	P-44A
ADV101KP50[2]	50 MHz	0°C to +70°C	P-44A
ADV101KP30[2]	30 MHz	0°C to +70°C	P-44A

NOTES
[1]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC).
[2]PLCC: Plastic Leaded Chip Carrier (J-lead).

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG, I_{SYNC} to GND[1] . . . . . 0 V to V_{AA}

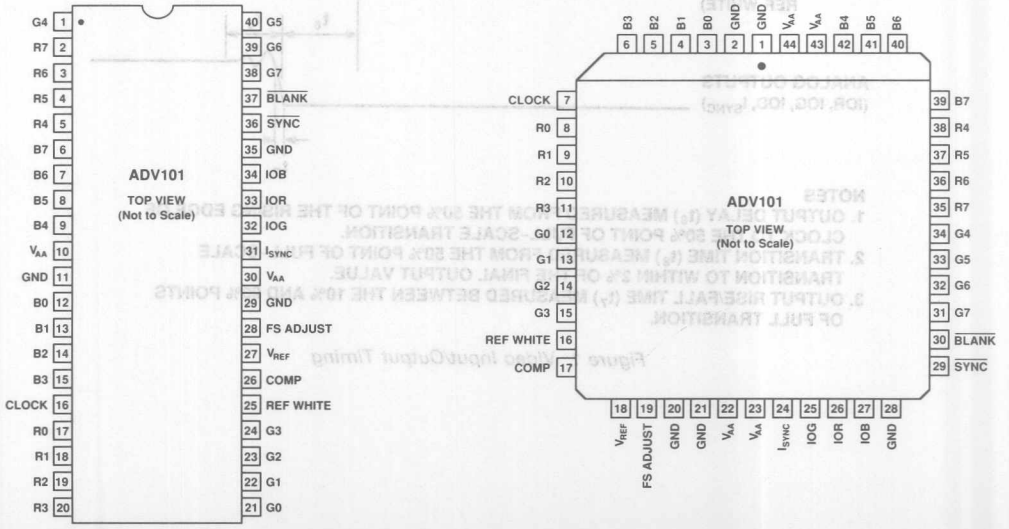
NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R7, G0–G7, R0–R7 and REF WHITE pixel and control inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input; switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and REF WHITE pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the pixel input data (R0–R7, G0–G7 and B0–B7). REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output. This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: $$I_{SYNC}\,(mA) = 3{,}455 \times V_{REF}\,(V)/\,R_{SET}\,(\Omega)$$ If sync information is not required on the green channel, I_{SYNC} should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $$R_{SET}\,(\Omega) = 12{,}082 \times V_{REF}\,(V)/IOG\,(mA)$$ The relationship between R_{SET} and the full-scale output current on IOR and IOB is given by: $$IOR,\ IOB\,(mA) = 8{,}628 \times V_{REF}\,(V)/\,R_{SET}\,(\Omega)$$
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.2 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV101 must be connected.
GND	Ground. All GND pins must be connected.

FEATURES

66MHz Pipelined Operation
Triple 8-Bit D/A Converters
256×24 Color Palette RAM
3×24 Overlay Registers
RS-343A/RS-170 Compatible Outputs
+5V CMOS Monolithic Construction
40-Pin DIP or Small 44-Pin PLCC Package
Power Dissipation: 1000mW

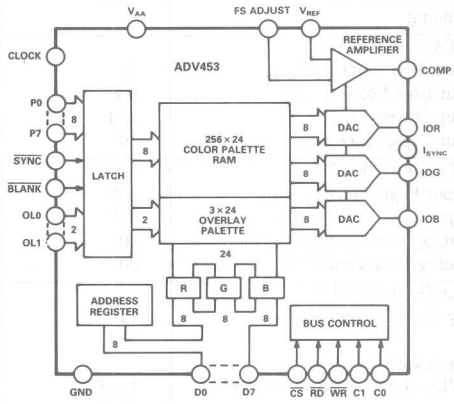
APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

66MHz
40MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV453 (ADV®) is a complete analog video output RAM-DAC on a single monolithic chip. It is specifically designed for high resolution color graphics systems. The part contains a 256×24 color lookup table, a 3×24 overlay palette as well as triple 8-bit video D/A converters. The ADV453 is capable of simultaneously displaying up to 259 colors, 256 from the lookup table and three from the overlay registers, out of a total color palette of 16.8 million addressable colors.

The three overlay registers allow for the implementation of overlaying cursors, pull down menus and grids. There is an independent, asynchronous MPU bus which allows access to the color lookup table without affecting the input of video data via the pixel port. The ADV453 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV453 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6″, 40-pin DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 66MHz.
2. Compatible with a wide variety of high resolution color graphics systems including VGA* and Macintosh II**.
3. Three overlay registers allow for implementation of overlaying cursors, pull down menus and grids.
4. Guaranteed monotonic. Integral and differential nonlinearities guaranteed to be a maximum of ±1LSB.
5. Low glitch energy, 50pV secs.

ADV is a registered trademark of Analog Devices, Inc.
*VGA is a trademark of International Business Machines Corp.
**Macintosh II is a registered trademark of Apple Computer Inc.

ADV453—SPECIFICATIONS (V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5%	Gray Scale max	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	± 1	μA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	10	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating State Leakage Current	20	μA max	
Floating State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level on IOG	0	μA min	Typically 5μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF typ	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	−5	mA typ	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	
Supply Current, I_{AA}	275	mA max	Typically 220mA, 66MHz Parts
	250	mA max	Typically 190mA, 40MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%, f = 1kHz, COMP = 0.1μF
Power Dissipation	1375	mW max	Typically 1000mW, 66MHz Parts
	1250	mW max	Typically 900mW, 40MHz Parts
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[2,3]	−30	dB typ	
Glitch Impulse[2,3]	50	pV secs typ	
DAC to DAC Crosstalk	−23	dB typ	

NOTE

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C

[2]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. *Analog output load* ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2]).

Parameter	66MHz Version	40MHz Version	Units	Conditions/Comments
f_{max}	66	40	MHz max	Clock Rate
t_1	35	35	ns min	$\overline{CS}$, C0, C1 Setup Time
t_2	35	35	ns min	$\overline{CS}$, C0, C1 Hold Time
t_3	25	25	ns min	$\overline{RD}$, $\overline{WR}$ High Time
t_4	10	10	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_5	100	100	ns max	$\overline{RD}$ Asserted to Data Valid
t_6	15	15	ns max	$\overline{RD}$ Negated to Data Bus Three Stated
t_7	50	50	ns min	$\overline{WR}$ Low Time
t_8	35	35	ns min	Write Data Setup Time
t_9	0	0	ns min	Write Data Hold Time
t_{10}	5	7	ns min	Pixel & Control Setup Time
t_{11}	2	3	ns min	Pixel & Control Hold Time
t_{12}	15	25	ns min	Clock Cycle Time
t_{13}	5	7	ns min	Clock Pulse Width High Time
t_{14}	5	7	ns min	Clock Pulse Width Low Time
t_{15}	20	20	ns typ	Analog Output Delay
	30	30	ns max	
t_{16}	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[3]	25	25	ns typ	Analog Output Settling Time
t_{PD}	$2\times t_{12}$	$2\times t_{12}$	ns max	Pipeline Delay
t_{SK}	1	1	ns typ	Analog Output Skew
	2	2	ns max	

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by HC logic.

Specifications subject to change without notice.

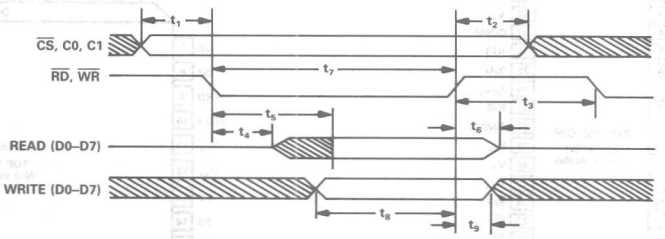


Figure 1. MPU Read/Write Timing

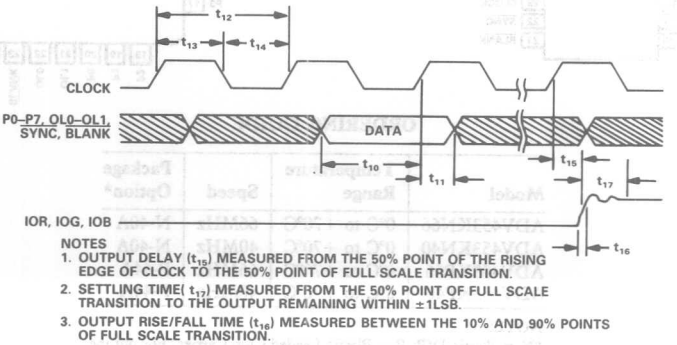


Figure 2. Video Input/Output Timing

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



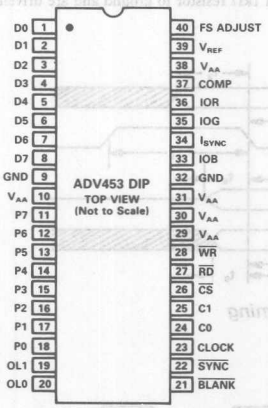
ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . . . GND −0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
IOR, IOB, IOG to GND[1] . . . . . 0V to V_{AA}

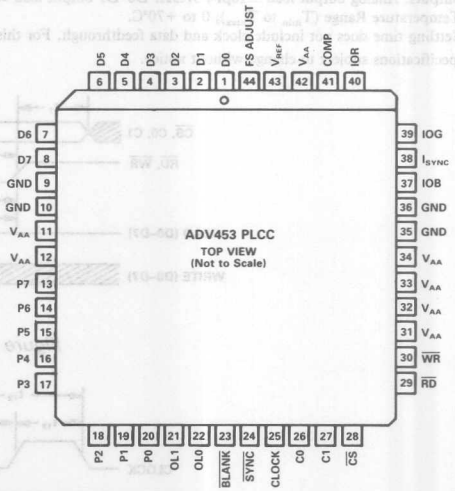
NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING GUIDE

Model	Temperature Range	Speed	Package Option*
ADV453KN66	0°C to +70°C	66MHz	N-40A
ADV453KN40	0°C to +70°C	40MHz	N-40A
ADV453KP66	0°C to +70°C	66MHz	P-44A
ADV453KP40	0°C to +70°C	40MHz	P-44A

NOTES
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is at logical zero, the pixel and overlay inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output (see Figure 5). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table V; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7 and OL0–OL1 data inputs as well as the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of CLOCK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
OL0–OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information (see Table IV), i.e., the 256×24 color palette or the 3×24 overlay palette. When accessing the overlay palette, the P0–P7 inputs are ignored. OL0–OL1 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output (see Figure 3). This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: I_{SYNC} (mA) = 1,728 * V_{REF}(V)/ R_{SET} (Ω). If sync information is not required on the green channel, I_{SYNC} should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and GND (see Figure 6) controls the magnitude of the full scale video signal. Note that the IRE relationships in Figure 5 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: IOG (mA) = (K + 326 + 1,728) * V_{REF}(V)/R_{SET} (Ω) The relationship between R_{SET} and the full scale output current on IOR and IOB is given by: IOR, IOB (mA) = (K + 326)* V_{REF}(V)/R_{SET}(Ω) where K = 3,993
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1μF ceramic capacitor must be connected between COMP and V_{AA} (Figure 6).
V_{REF}	Voltage reference input. An external 1.235V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA} (Figure 6.)
V_{AA}	Analog power supply (5V±5%). All V_{AA} pins on the ADV453 must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{\text{CS}}$	Chip select control input (TTL compatible). $\overline{\text{CS}}$ must be at logical zero to enable the reading and writing of data to and from the device. The IOR, IOG and IOB outputs are forced to the black level while $\overline{\text{CS}}$ is at logical zero. Note that the ADV453 will not operate properly if $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are simultaneously at logical zero.
$\overline{\text{WR}}$	Write control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{WR}}$ must both be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$ or $\overline{\text{CS}}$. See Figure 1.
$\overline{\text{RD}}$	Read control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being carried out, i.e., address register, color palette RAM or overlay registers read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register, the color palette RAM and the overlay registers over this 8-bit bidirectional data bus. D0 is the least significant bit.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{BLANK}$ signal is latched on the rising edge of CLOCK. While $\overline{BLANK}$ is at logical zero, the pixel and overlay inputs are ignored.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{SYNC}$ input switches off a 40 IRE current source on the I_{SYNC} output (see Figure 5). $\overline{SYNC}$ does not override any other control or data input, as shown in Table V; therefore, it should only be asserted during the blanking interval. $\overline{SYNC}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7 and OL0–OL1 data inputs as well as the $\overline{SYNC}$ and $\overline{BLANK}$ control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of CLOCK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
OL0–OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information (see Table IV), i.e., the 256×24 color palette or the 3×24 overlay palette. When accessing the overlay palette, the P0–P7 inputs are ignored. OL0–OL1 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output (see Figure 3). This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{SYNC}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{SYNC}$ is at logical one is given by: I_{SYNC} (mA) = 1.725 * V_{REF}(V)/ R_{SET} (Ω). If sync information is not required on the green channel, I_{SYNC} should be connected to GND.
PS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and GND (see Figure 6) controls the magnitude of the full scale video signal. Note that the IRE relationships in Figure 5 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: IOG (mA) = (K + 326 + 1.725) * V_{REF}(V)/R_{SET} (Ω) The relationship between R_{SET} and the full scale output current on IOR and IOB is given by: IOR, IOB (mA) = (K + 326)* V_{REF}(V)/R_{SET}(Ω) where K = 3,993
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1μF ceramic capacitor must be connected between COMP and V_{AA} (Figure 6).
V_{REF}	Voltage reference input. An external 1.235V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA} (Figure 6.)
V_{AA}	Analog power supply (5V ± 5%). All V_{AA} pins on the ADV453 must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{CS}$	Chip select control input (TTL compatible). $\overline{CS}$ must be at logical zero to enable the reading and writing of data to and from the device. The IOR, IOG and IOB outputs are forced to the black level while $\overline{CS}$ is at logical zero. Note that the ADV453 will not operate properly if $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are simultaneously at logical zero.
$\overline{WR}$	Write control input (TTL compatible). $\overline{CS}$ and $\overline{WR}$ must both be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. See Figure 1.
$\overline{RD}$	Read control input (TTL compatible). $\overline{CS}$ and $\overline{RD}$ must both be at logical zero when reading data from the device. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being carried out, i.e., address register, color palette RAM or overlay registers read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register, the color palette RAM and the overlay registers over this 8-bit bidirectional data bus. D0 is the least significant bit.

CMOS 100 MHz True-Color Graphics Triple 8-Bit Video RAM-DAC

ADV473*

2

FEATURES

ADV478/ADV471 (ADV®) Register Level Compatible
IBM PS/2*, VGA*/XGA* Compatible
100 MHz Pipelined Operation
Triple 8-Bit D/A Converters
Triple 256 × 8 (256 × 24) Color Palette RAM
Three 15 × 8 Overlay Registers
On-Board Voltage Reference
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs and Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
Standard MPU I/O Interface
+5 V CMOS Monolithic Construction
68-Pin PLCC

APPLICATIONS

High Resolution Color Graphics
True-Color Visualization
CAE/CAD/CAM
Image Processing
Desktop Publishing

MODES	SPEED GRADES
24-Bit True Color	100 MHz
8-Bit Pseudo Color	80 MHz
15-Bit True Color	66 MHz
8-Bit True Color	50 MHz, 35 MHz

GENERAL DESCRIPTION

The ADV473 is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for true-color computer graphics systems.

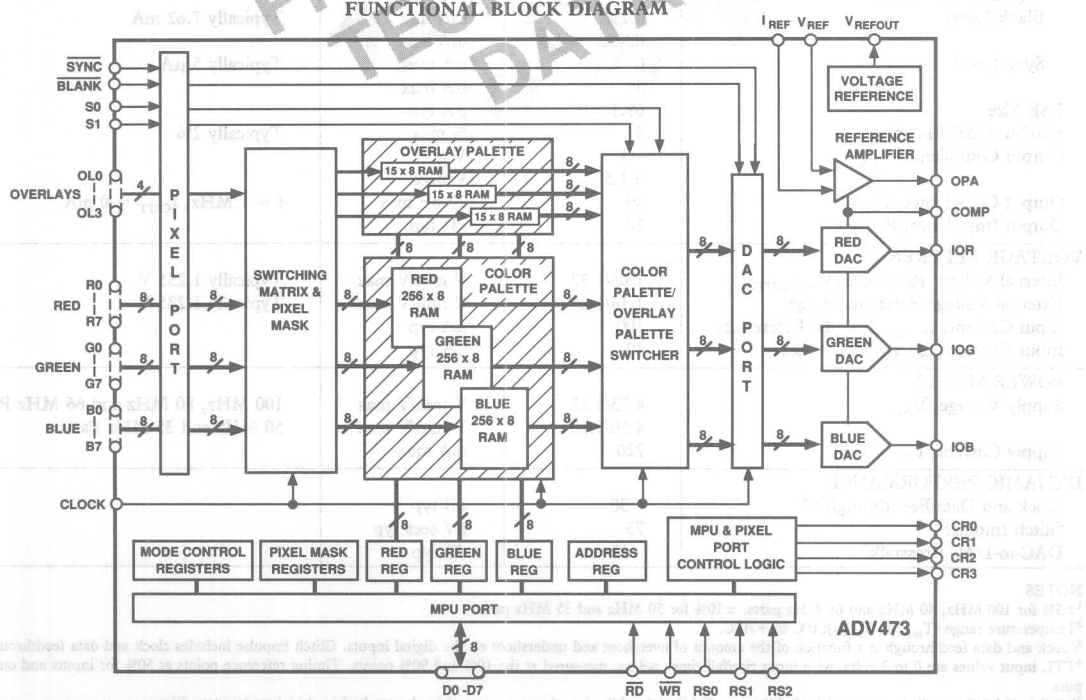
The ADV473 integrates a number of graphic functions onto one device allowing 24-bit direct true-color operation at the maximum screen update rate of 100 MHz. It can also be used in other modes, including 15-bit true color and 8-bit pseudo or indexed color. The ADV473 is fully PS/2 and VGA register level compatible. It is also capable of implementing IBM's XGA standard.

The device consists of three, high speed, 8-bit, video D/A converters (RGB), a 256 × 24 RAM which can be configured as a

(Continued on page 2–808)

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



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*Personal System/2 and VGA are trademarks of International Business Machines Corp.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	μA max	
Floating-State Leakage Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
(Pedestal = 7.5 IRE)	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5 μA
(Pedestal = 0 IRE)	50	μA max	
Blank Level	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC-to-DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.5	V max	
Output Capacitance, C_{OUT}	30	30 pF max	f = 1 MHz, I_{OUT} = 0 mA
Output Impedance, R_{OUT}	10	kΩ typ	
VOLTAGE REFERENCE			
Internal Voltage Reference (V_{REFOUT})	1.08/1.32	V min/V max	Typically 1.235 V
External Voltage Reference Range	1.14/1.26	V min/V max	Typically 1.235 V
Input Current, I_{VREF} (Internal Reference)	100	μA typ	
Input Current (External Reference)	10	μA typ	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	100 MHz, 80 MHz and 66 MHz Parts
	4.50/5.50	V min/V max	50 MHz and 35 MHz Parts
Supply Current, I_{AA}	220	mA max	
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−30	dB typ	
Glitch Impulse[3, 4]	75	pV secs typ	
DAC-to-DAC Crosstalk[5]	−23	dB typ	

NOTES

[1]±5% for 100 MHz, 80 MHz and 66 MHz parts. ±10% for 50 MHz and 35 MHz parts.

[2]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

[4]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured at the 10% and 90% points. Timing reference points at 50% for inputs and outputs.

[5]DAC to DAC Crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING CHARACTERISTICS[1] (V_{AA}[1] = 5 V; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 140 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	100 MHz Version	80 MHz Version	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
fmax	100	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	10	ns min	RS0–RS2 Setup Time
t_2	10	10	10	10	10	ns min	RS0–RS2 Hold Time
t_3[4]	3	3	3	3	3	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	5	5	ns min	Read Data Hold Time
t_7	10	10	10	10	10	ns min	Write Data Setup Time
t_8	10	10	10	10	10	ns min	Write Data Hold Time
t_9	100	100	100	100	100	ns max	CR0-CR3 Delay Time
t_{10}	50	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{11}	40	40	40	40	40	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{12}	3	3	3	3	3	ns min	Pixel & Control Setup Time
t_{13}	3	3	3	3	3	ns min	Pixel & Control Hold Time
t_{14}	10	12.5	15.15	20	28	ns min	Clock Cycle Time
t_{15}	3	4	5	6	7	ns min	Clock Pulse Width High Time
t_{16}	3	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{17}	30	30	30	30	30	ns max	Analog Output Delay
t_{18}	3	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{19}[6]	13	13	13	13	13	ns max	Analog Output Settling Time
t_{SK}	2	2	2	2	2	ns max	Analog Output Skew
t_{PD}	4 × t_{14}	4 × t_{14}	4 × t_{14}	4 × t_{14}	4 × t_{14}	ns	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 2.
[2]±5% for 100 MHz, 80 MHz and 66 MHz parts. ±10% for 50 MHz and 35 MHz parts.
[3]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.
[4]t_3 and t_4 are measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.4 V or 2.4 V.
[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and, as such, are independent of external bus loading capacitances.
[6]Settling time does not include clock and data feedthrough.

Specifications subject to change without notice.

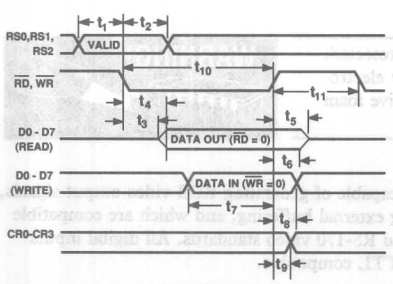


Figure 1. MPU Read/Write Timing

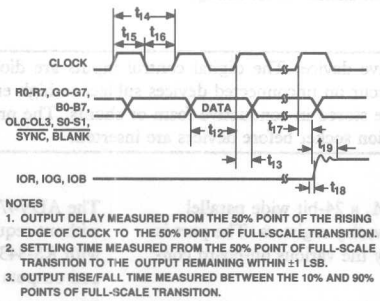


Figure 2. Video Input/Output Timing

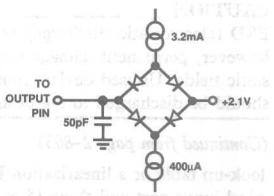


Figure 3. Load Circuit for Bus Access and Relinquish Time

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
100 MHz, 80 MHz, 66 MHz Parts		4.75	5.00	5.25	Volts
50 MHz, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
I_{REF} Current	I_{REF}				
Standard RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Pin . . . . . GND−0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[2] . . . . . 0 V to V_{AA}

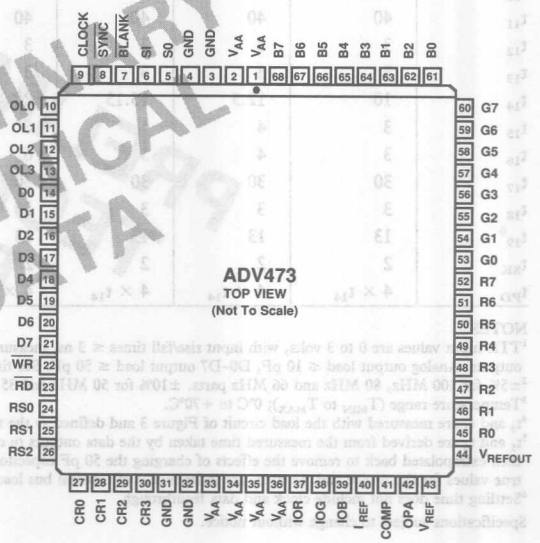
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

Model	Speed	Temperature Range	No. of Pins	Package Option[1, 2]
ADV473KP100	100 MHz	0°C to +70°C	68	P-68A
ADV473KP80	80 MHZ	0°C to +70°C	68	P-68A
ADV473KP66	66 MHZ	0°C to +70°C	68	P-68A
ADV473KP50	50 MHz	0°C to +70°C	68	P-68A
ADV473KP35	35 MHz	0°C to +70°C	68	P-68A

[1]All devices are packaged in a 68-pin plastic leaded (J-lead) chip carrier.
[2]P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATION
68-Pin PLCC



PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



(Continued from page 2–805)

look-up table or a linearization RAM, a 24-bit wide parallel pixel input port and three 15 × 8 overlay registers. The part is controlled through the MPU port by the various on-board control/command registers.

The individual red, green and blue pixel input ports allow true-color, image rendition. True-color image rendition, at speeds of up to 100 MHz, is achieved through the 24-bit pixel input port. The ADV473 is also capable of implementing 8-bit true-color, 8-bit pseudo color and 15-bit true color.

The ADV473 is capable of generating RGB video output signals, without requiring external buffering, and which are compatible with RS-343A and RS-170 video standards. All digital inputs and outputs are TTL compatible.

The part can be driven by the on-board voltage reference or an external voltage/current reference.

The part is packaged in a 68-pin Plastic Leaded Chip Carrier (PLCC).

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PIN FUNCTION DESCRIPTION

$\overline{\text{BLANK}}$	Composite Blank Control Input (TTL Compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
$\overline{\text{SYNC}}$	Composite SYNC Control Input (TTL Compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the analog outputs, $\overline{\text{SYNC}}$ should be connected to ground.
CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, S0, S1, OL0–OL3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
R0–R7 B0–B7 G0–G7	Red, Green and Blue Select Inputs (TTL Compatible). These inputs specify, on a pixel basis, the color value to be written to the DACs. They are latched on the rising edge of CLOCK. R0, G0 and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color Mode Select Inputs (TTL Compatible). These inputs specify the mode of operation as shown in Table III. They are latched on the rising edge of CLOCK.
OL0–OL3	Overlay Select Inputs (TTL Compatible). These inputs specify which palette is to be used to provide color information. When accessing the overlay palette, the R0–R7, G0–G7, B0–B7, S0 and S1 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, Green, and Blue Current Outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: R_{SET} (Ω) = 3,195 × V_{REF} (V)/I_{OUT} (mA) SETUP = 7.5 IRE) R_{SET} (Ω) = 3,025 × V_{REF} (V)/I_{OUT} (mA) SETUP = 0 IRE) When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is: I_{REF} (mA) = I_{OUT} (mA)/3.195 (SETUP = 7.5 IRE) I_{REF} (mA) = I_{OUT} (mA)/3.025 (SETUP = 0 IRE)
COMP	Compensation Pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage Reference Input. If an external voltage reference is used, it must supply this input with a 1.2 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA}.
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating.
V_{REFOUT}	Voltage Reference Output. This output provides a 1.2 V reference and may be connected directly to the V_{REF} pin. If it is preferred to use an external voltage reference, this pin may be left floating. Up to four ADV473s can be driven from V_{REFOUT}.
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog Ground. All GND pins must be connected.
$\overline{\text{WR}}$	Write Control Input (TTL Compatible). D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0–RS2 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be asserted simultaneously.
$\overline{\text{RD}}$	Read Control Input (TTL Compatible). To read data from the device, $\overline{\text{RD}}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{\text{RD}}$ during MPU read operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be asserted simultaneously.
RS0, RS1, RS2	Register Select Inputs (TTL Compatible). RS0–RS2 specify the type of read or write operation being performed.
D0–D7	Data Bus (TTL Compatible). Data is transferred into and out of the device over this eight-bit bidirectional data bus. D0 is the least significant bit.
CR0–CR7	Control Outputs (TTL Compatible). These outputs are used to control application specific features. The output values are determined by the contents of the command register (CR).

PRELIMINARY TECHNICAL DATA

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TERMINOLOGY

BLANKING LEVEL
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

COMPOSITE $\overline{\text{SYNC}}$ SIGNAL ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite $\overline{\text{SYNC}}$ signal.

GRAY SCALE
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and to display images.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the reference black level and the blanking level.

$\overline{\text{SYNC}}$ LEVEL
The peak level of the composite $\overline{\text{SYNC}}$ signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface
The ADV473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

Three address decode lines, RS0–RS2, specify whether the MPU is accessing the address register, the color palette RAM, the overlay registers, or read mask register. These controls also determine whether this access is a read or write function. Table I illustrates this decoding. The 8-bit address register is used to address the contents of the color palette RAM and overlay registers.

Table I. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Command Register

Color Palette Writes
The MPU writes to the address register (selecting RAM write mode, RS2 = 0, RS1 = 0 and RS0 = 0) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the BLUE write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the palette by initially writing the start address and then performing a sequence of RED, GREEN and BLUE writes. The address automatically increments to the next highest location after a BLUE write.

Color Palette Reads
The MPU writes to the address register (selecting RAM read mode, RS2 = 0, RS1 = 1 and RS0 = 1) with the address of the color palette RAM location to be read back. The contents of the palette RAM are copied to the RED, GREEN and BLUE registers and the address register increments to point to the next palette RAM location. The MPU then performs three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the BLUE read cycle, the 24/18 bit contents of the palette RAM at the location specified by the address register is loaded into the RED, GREEN and BLUE registers. The address register then increments to the next location which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the palette by initially writing the start address and then performing a sequence of RED, GREEN and BLUE reads. The address automatically increments to the next highest location after a BLUE read.

PRELIMINARY TECHNICAL DATA

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TABLE II. Address Register (ADDR) Operation

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00	X	0	1	Red Value
	01	X	0	1	Green Value
	10	X	0	1	Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	0	1	Color Palette RAM
	XXXX 0000	1	0	1	Reserved
	XXXX 0001	1	0	1	Overlay Color 1
	XXXX 0010	1	0	1	Overlay Color 2
	.	.	.	.	.
	.	.	.	.	.
	XXXX 1111	1	0	1	Overlay Color 15

2

Overlay Color Writes

The MPU writes to the address register (selecting OVERLAY REGISTER write mode, RS2 = 1, RS1 = 0 and RS0 = 0) with the address of the overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the Overlay Registers (RS2 = 1, RS1 = 0, RS0 = 1). After the BLUE write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and are written to the overlay register specified by the address register. The address register then increments to the next overlay register which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the overlay registers by initially writing the start address and then performing a sequence of RED, GREEN and BLUE writes. The address automatically increments to the next highest location after a BLUE write.

Overlay Color Reads

The MPU writes to the address register (selecting OVERLAY REGISTER read mode, RS2 = 1, RS1 = 1 and RS0 = 1) with the address of the overlay register to be read back. The contents of the overlay register are copied to the RED, GREEN and BLUE registers and the address register increments to point to the next highest overlay register. The MPU then performs three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0 – RS2 to select the Overlay Registers (RS2 = 1, RS1 = 0, RS0 = 1). After the BLUE read cycle, the 24/18 bit contents of the overlay register at the specified address register location is loaded into the RED, GREEN and BLUE registers. The address register then increments to the next overlay register which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the overlay registers by initially writing the start address and then performing a sequence of RED, GREEN and BLUE reads. The address automatically increments to the next highest location after a BLUE read.

Internal Address Register (ADDR)

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits (since there are only 15 overlay registers) of the address register (ADDR4–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Synchronization

The MPU interface operates asynchronously to the pixel port. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B as shown in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. The MPU can be accessed at any time, even when the pixel CLOCK is stopped.

8-Bit/6-Bit Color Operation

The Command Register on the ADV473 specifies whether the MPU is reading/writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical "0." It should be noted that when the ADV473 is in 6-bit mode, full-scale output current will be reduced by approximately 1.5% relative to the 8-bit mode. This is the case since the 2 LSBs of each of the three DACs are always set to zero in 6-bit mode.

PRELIMINARY DATA SHEET

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ister is 8 bits wide, CR0–CR7 and is directly mapped to the MPU data bus on the part, D0–D7. The command register can be written to or read from. It is not initialized, therefore it must be set. Figure 4 shows what each bit of the CR register controls and shows the values it must be programmed to for various modes of operation.

15-bit true-color, 8-bit true-color and 8-bit pseudo color. The mode of operation is determined by the S0 and S1 inputs, in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the video data. Table III illustrates the modes of operation.

Table III. Color Operation Modes

OL3-OL0	S1, S0	CR7, CR6	Mode	R7–R0	G7–G0	B7-B0
1111	XX	XX	Overlay Color 15	$XX	$XX	$XX
.	.	.	.	.	.	.
.	.	.	.	.	.	.
0001	XX	XX	Overlay Color 1	$XX	$XX	$XX
0000	00	00	24-Bit True-Color	R7–R0	G7–G0	B7–B0
0000	00	01	24-Bit True-Color	R7–R0	G7–G0	B7–B0
0000	00	10	24-Bit True-Color	R7–R0	G7–G0	B7–B0
0000	00	11	Reserved	Reserved	Reserved	Reserved
0000	01	00	24-Bit True-Color Bypass	R7–R0	G7–G0	B7–B0
0000	01	01	24-Bit True-Color Bypass	R7–R0	G7–G0	B7–B0
0000	01	10	24-Bit True-Color Bypass	R7–R0	G7–G0	B7–B0
0000	01	11	Reserved	Reserved	Reserved	Reserved
0000	10	00	8-Bit PseudoColor (Red)	P7–P0	Ignored	Ignored
0000	10	01	8-Bit Pseudo Color (Green)	Ignored	P7–P0	Ignored
0000	10	10	8-Bit PseudoColor (Blue)	Ignored	Ignored	P7–P0
0000	10	11	15-Bit True Color	orrrrrgg	gggbbbbb	Ignored
0000	11	00	8-Bit True-Color Bypass (Red)	rrrgggbb	Ignored	Ignored
0000	11	01	8-Bit True-Color Bypass (Green)	Ignored	rrrgggbb	Ignored
0000	11	10	8-Bit True-Color Bypass (Blue)	Ignored	Ignored	rrrgggbb
0000	11	11	15-Bit True-Color Bypass	0rrrrrgg	gggbbbbb	Ignored

PRELIMINARY TECHNICAL DATA

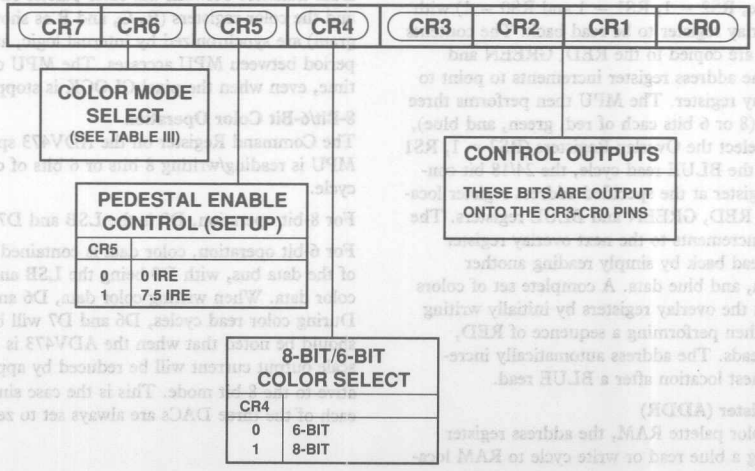


Figure 4. Command Register (CR)

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Twenty-four bits of RGB color information may be input into the ADV473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

Twenty-four bits of pixel information may be input into the ADV473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 drive the red DAC directly, G0–G7 drive the green DAC directly, and B0–B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

Eight bits of pixel information may be input into the ADV473 every clock cycle. The 8 bits of pixel information (P0–P7) are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same 8 bits of pixel data (P0–P7). Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Bypass Mode

Eight bits of pixel information may be input into the ADV473 every clock cycle. The 8 bits of pixel information are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6.

Table IV. 8-Bit True-Color Bypass Video Input Format

R0–R7 Inputs Selected	G0–G7 Inputs Selected	B0–B7 Input Selected	Inputs Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As seen in the table, 3 bits of red, 3 bits of green, and 2 bits of blue data are input. The 3 MSBs of the red and green DACs are driven directly by the inputs, while the 2 MSBs of the blue DAC are driven directly. The 5 LSBs for the red and green DACs, and the 6 LSBs for the blue DAC, are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

every clock cycle. The 15 bits of pixel information (5 bits of red, 5 bits of green, and 5 bits of blue) are input via the R0–R7 and G0–G7 inputs.

Table V. 15-Bit True-Color Video Input Format

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The 3 LSBs are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

Overlays

The overlay inputs, OL0–OL3, have priority regardless of the color mode as shown in Table III.

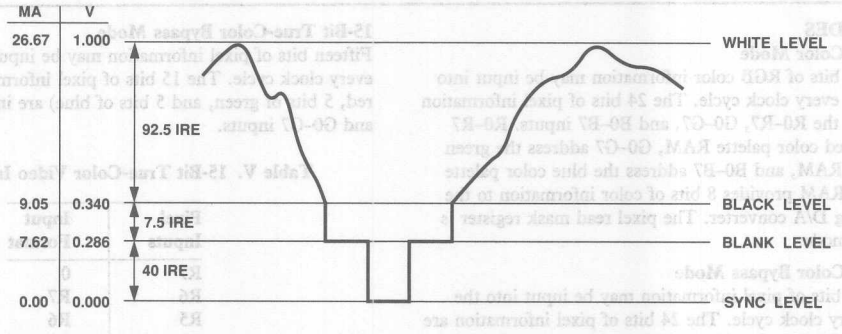
Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0 depending on the mode). Bit D0 also corresponds to data bus Bit D0.

PRELIMINARY TECHNICAL DATA

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NOTE:
75Ω DOUBLY-TERMINATED LOAD, SETUP=7.5 IRE, V_{REF} =1.235 V, R_{SET} =140Ω
RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. Composite Video Output Waveform (Setup = 7.5 IRE)

Table VI. Video Output Truth Table (Setup = 7.5 IRE)

Description	I_{OUT} (mA)	SYNC	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data+9.05	1	1	Data
DATA-SYNC	Data+1.44	0	1	Data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	XXH
SYNC	0	0	0	XXH

NOTE
Typical with full-scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, V_{REF} = 1.235 V, R_{SET} = 140 Ω. External voltage or current reference adjusted for 26.67 mA full-scale output.

PRELIMINARY TECHNICAL DATA

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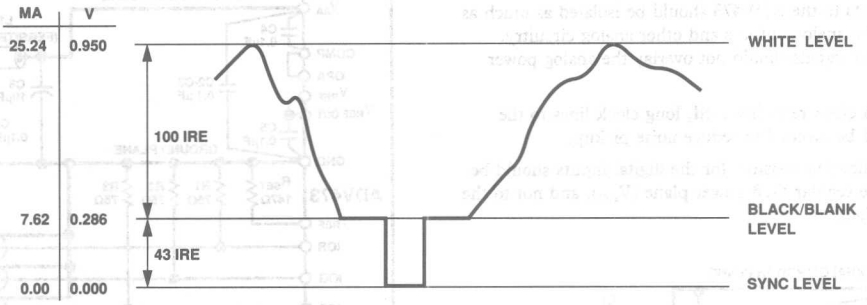


Figure 6. Composite Video Output Waveform (SETUP = 0 IRE)

Table VII. Video Output Truth Table (SETUP = 0 IRE)

Description	I_{OUT} (mA)	SYNC	BLANK	DAC Input Data
WHITE	25.24	1	1	FFH
DATA	Data+7.62	1	1	Data
DATA-SYNC	Data	0	1	Data
BLACK	7.62	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	7.62	1	0	XXH
SYNC	0	0	0	XXH

NOTE
Typical with full-scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, V_{REF} = 1.235 V, R_{SET} = 140 Ω. External voltage or current reference adjusted for 26.67 mA full-scale output.

PRELIMINARY TECHNICAL DATA

PC BOARD LAYOUT CONSIDERATIONS

The layout should be optimized for lowest noise on the ADV473 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV473 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV473, the analog output traces, and all the digital signal traces leading up to the ADV473.

Power Planes

The ADV473 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 7, 8 and 9. This bead should be located within three inches of the ADV473.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV473 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

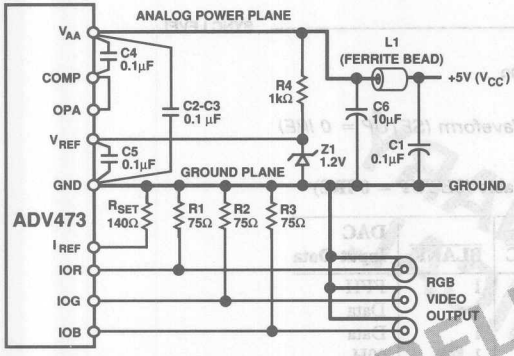
It is important to note that while the ADV473 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three-terminal voltage regulator for supplying power to the analog power plane.

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The digital inputs to the ADV473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV473 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not to the analog power plane.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R4	1kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.23V VOLTAGE REFERENCE	AD589JN

Figure 7. Typical Connection Diagram (External Voltage Reference)

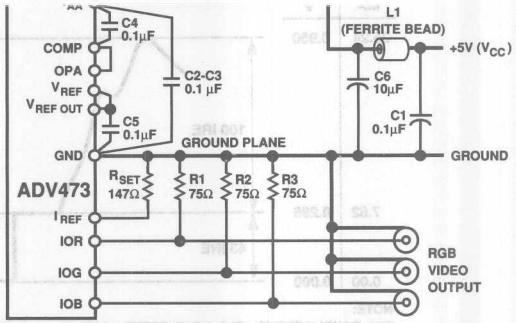
Analog Signal Interconnect

The ADV473 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

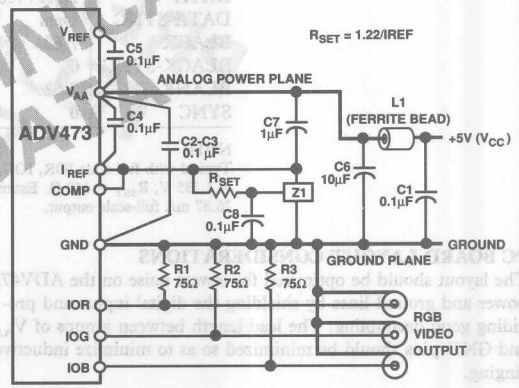
For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV473 to minimize reflections.

For more information on circuit board design and layout, see application note entitled "Design and Layout of a Video Graphics System for Reduced EMI" available from Analog Devices, Publication No. E1309-15-10/89.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R_{SET}	1% METAL FILM RESISTOR	

Figure 8. Typical Connection Diagram (Internal Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 — C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C7,C8	1µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
Z1	ADJUSTABLE REGULATOR	LM317LZ
R_{SET}	1% METAL FILM RESISTOR	

Figure 9. Typical Connection Diagram (External Current Reference)

PRELIMINARY TECHNICAL DATA

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Color Palette RAM-DAC

ADV476

FEATURES

Personal System/2* and VGA* Compatible
Plug-in Replacement for INMOS 171/176
66MHz Pipelined Operation
Three 6-Bit D/A Converters
256×18 Color Palette RAM
RS-343A/RS-170 Compatible Outputs
Blank on All Three Channels
Standard MPU Interface
Asynchronous Access to All Internal Registers
+5V CMOS Monolithic Construction
Low Power Dissipation
Standard 28-Pin, 0.6″ DIP and 44-Pin PLCC

APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

66MHz
50MHz
35MHz

GENERAL DESCRIPTION

The ADV476 (ADV®) is a pin compatible and software compatible RAM-DAC designed specifically for VGA and Personal System/2 color graphics.

The ADV476 is a complete analog output RAM-DAC on a single monolithic chip. The part contains a 256×18 color lookup table, a pixel mask register as well as a triple 6-bit video D/A converter. The ADV476 is capable of simultaneously displaying up to 256 colors, from a total color palette of 262,144 addressable colors.

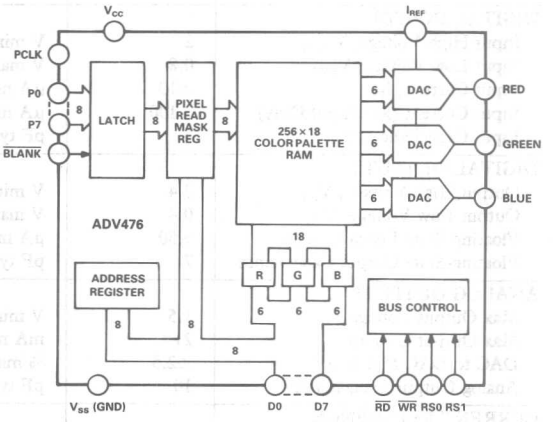
The on-chip asynchronous MPU bus allows access to the color lookup table without affecting the input video data via the pixel port. The pixel read mask register provides a convenient way of altering the displayed colors without updating the color lookup table. The ADV476 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV476 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation and small board area. The part is packaged in a 0.6″, 28-pin DIP and a 44-pin PLCC.

***Personal System/2 and VGA are trademarks of International Business Machines Corp.**

ADV is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Standard video refresh rates, 35MHz, 50MHz and 66MHz.
2. Fully compatible with VGA and Personal System/2 color graphics.
3. Guaranteed monotonic. Integral and differential linearity guaranteed to be a maximum of ±1LSB.
4. Low glitch energy, 75pV secs.

ADV476—SPECIFICATIONS (V_{CC} = +5V ±10%, I_{REF} = 8.88mA. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	6	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±0.5	LSB max	Guaranteed Monotonic
Full Scale Error	±5	% max	Full Scale = 2.15×I_{REF}×R_L, I_{REF}=8.39mA
Blank Level	±0.5	LSB max	$\overline{BLANK}$ = Logic Low
Offset Error	±0.5	LSB max	$\overline{BLANK}$ = Logic High
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	µA max	V_{CC}=5.5V, V_{IN}=0.4V to V_{CC}
Input Current ($\overline{RD}$ Input Only)	±100	µA max	V_{CC}=5.5V, V_{IN}=0.4V to V_{CC}
Input Capacitance, C_{IN}	7	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE}=500µA, V_{CC}=4.5V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK}=5.0mA, V_{CC}=4.5V
Floating-State Leakage Current	±50	µA max	V_{CC}=5.5V, 0.4V<V_{IN}<V_{CC}
Floating-State Output Capacitance	7	pF typ	
ANALOG OUTPUTS			
Max Output Voltage	1.5	V min	IO≤10mA, IO=2.15×I_{REF}
Max Output Current	21	mA min	VO≤1V
DAC to DAC Matching[2]	±2.5	% max	
Analog Output Capacitance	10	pF typ	$\overline{BLANK}$ = Logic Low
CURRENT REFERENCE			
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} −3/V_{CC}	V min/V max	I_{REF}=8.88mA
POWER SUPPLY			
Supply Voltage, V_{CC}	4.5/5.5	V min/V max	
Supply Current, I_{CC}	220	mA max	f_{MAX}=66MHz, IO=2.15×I_{REF}, D0 to D7 Unloaded
Power Supply Rejection Ratio	6	%/V	4.5<V_{CC}<5.5V, IO=2.15×I_{REF}, R_L=37.5Ω, C_L=30pF, I_{REF}=8.88mA
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−35	dB typ	
Glitch Impulse[3, 4]	75	pV secs typ	

NOTES

[1]Temperature range (T_{min} to T_{max}); 0 to +70°C.

[2]Relative to the midpoint of the distribution of the three DACs measured at full scale.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2×clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{CC} = +5V±10%. All Specifications T_{min} to T_{max}[2])

Parameter	66MHz Version	50MHz Version	35MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0, RS1 Setup Time
t_2	10	10	15	ns min	RS0, RS1 Hold Time
t_3	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	15	ns min	Write Data Setup Time
t_7	10	10	15	ns min	Write Data Hold Time
t_8	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$4\times t_{12}$	$4\times t_{12}$	$4\times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	4	ns min	Pixel & Control Setup Time
t_{11}	3	3	4	ns min	Pixel & Control Hold Time
t_{12}	15.3	20	28	ns min	Clock Cycle Time
t_{13}	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	ns max	Analog Output Delay
	5	5	5	ns min	
t_{16}	6	8	8	ns max	Analog Output Rise/Fall Time
t_{17}[3]	15.3	20	25	ns typ	Analog Output Settling Time
t_{18}	2	2	2	ns min	Analog Output Skew
t_{PD}	4	4	4	clocks	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load≤10 pF, 37.5Ω. D0–D7 output load≤50 pF. See timing notes in Figure 2.
[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.
Specifications subject to change without notice.

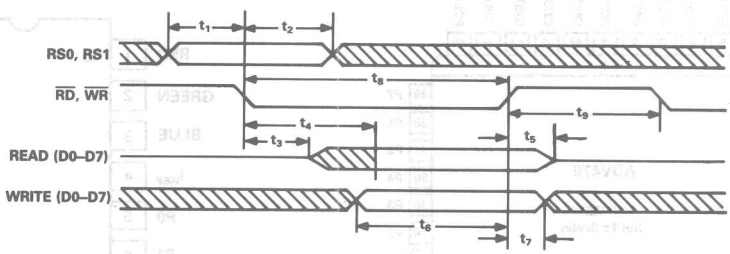
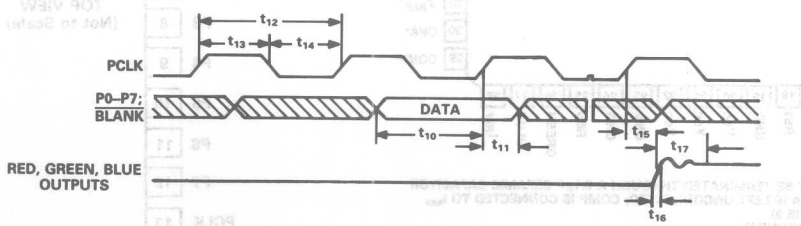


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE PCLK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1/4 LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND . . . . . +7V
Voltage on any Digital Pin . . . . . GND−0.5V to V_{CC}+0.5V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
Red, Green, Blue to GND[1] . . . . . 0V to V_{CC}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE[1, 2]

Model	Speed	Package Type	Package Option[3]
ADV476KN35	35MHz	28-Pin DIP	N-28
ADV476KN50	50MHz	28-Pin DIP	N-28
ADV476KN66	66MHz	28-Pin DIP	N-28
ADV476KP35	35MHz	44-Pin PLCC	P-44A
ADV476KP50	50MHz	44-Pin PLCC	P-44A
ADV476KP66	66MHz	44-Pin PLCC	P-44A

NOTES
[1]All devices are specified for 0 to +70°C operation.
[2]Devices are packaged in 0.6" 28-pin plastic DIPs (N-28), and 44-pin J-leaded PLCC (P-44A).
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

RECOMMENDED OPERATING CONDITIONS

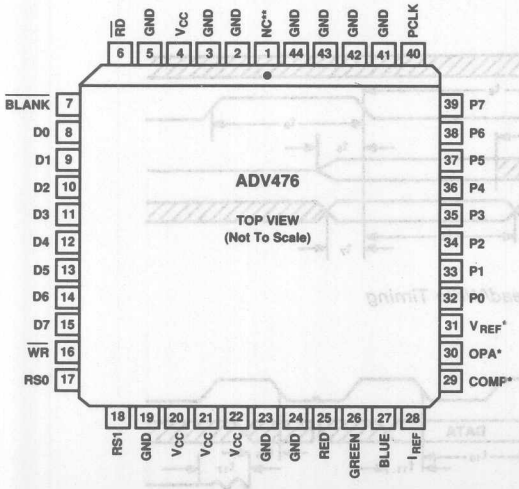
Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{CC}	4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Current	I_{REF}	−3		−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

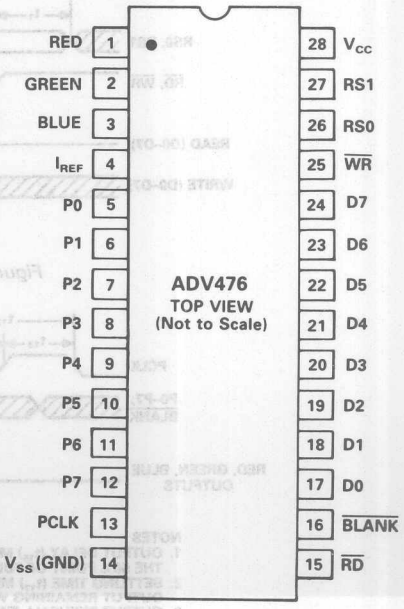


PLCC PIN CONFIGURATION



*V_{REF} MUST BE TERMINATED THROUGH A 0.1μF CERAMIC CAPACITOR TO V_{CC}. OPA IS LEFT UNCONNECTED; COMP IS CONNECTED TO I_{REF} (SEE FIGURE 8).
**NC = NO CONNECT

DIP PIN CONFIGURATION



The above pins allow the ADV476KP (44-Pin PLCC) to be alternatively driven by a voltage reference. If it is desired to use a voltage reference configuration instead of the current reference configuration described in this data sheet, the above listed pins must be connected as described in Figure 6 of the ADV478/ADV471 data sheet of this reference manual.

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{BLANK}$ signal is latched on the rising edge of PCLK. While $\overline{BLANK}$ is a logical zero, the pixel inputs are ignored.
PCLK	Clock input (TTL compatible). The rising edge of PCLK latches the P0–P7 data inputs and the $\overline{BLANK}$ control input. It is typically the pixel clock rate of the video system. PCLK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of PCLK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
RED, GREEN, BLUE	Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
V_{CC}	Analog power supply (5V ±10%).
GND	Analog ground.
I_{REF}	Current reference input. The relationship between the current input and the full scale output voltage of the DACs is given by the following expression: I_{REF} = VO (Full Scale)/2.15 × R_L R_L = Load Resistance
$\overline{WR}$	Write control input (TTL compatible). $\overline{WR}$ must be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{WR}$. See Figure 1.
$\overline{RD}$	Read control input (TTL compatible). $\overline{RD}$ must both be at logical zero when reading data from the device. See Figure 1.
RS0, RS1	Command control inputs (TTL compatible). RS0 and RS1 specify the type of read or write operation being carried out, i.e., address register or color palette RAM read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register and the color palette RAM over this 8-bit bidirectional data bus. D0 is the least significant bit.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green and Blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

MPU Interface

As illustrated in the functional block diagram, the ADV476 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM .

The RS0 and RS1 control inputs specify whether the MPU is accessing the address register or the color palette RAM, as shown in Table I. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers.

RS1	RS0	Addressed by MPU
0	0	Pixel Address Register (RAM Write Mode)
1	1	Pixel Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

Table I. Control Input Truth Table

To write color data, the MPU writes to the address register with the 8-bit address of the color palette RAM location which is to be modified. The MPU performs three successive write cycles (six bits of red data, six bits of green data and six bits of blue data). During the blue write cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (6 bits each of red, green and blue data). Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

This 6-bit color data is right justified, i.e., the lower six bits of the data bus with D0 being the LSB and D5 the MSB. D6 and D7 are ignored during a color write cycle and are set to zero during a color read cycle.

During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM during video screen retrace, i.e., during the video waveform blanking period, see Figure 5.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

	Value	RS1	RS0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00			Red Value
	01			Green Value
	10			Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	1	Color Palette RAM

Table II. Address Register (ADDR) Operation

$\overline{RD}$	$\overline{WR}$	RS0	RS1	ADDRa	ADDRb	Operation Performed	
1	0	0	0	X	X	Write Address Register;	D0–D7 → ADDR0–7 0 → ADDRa,b
1	0	1	0	0	0	Write Red Value;	Increment ADDRa–b
1	0	1	0	0	1	Write Green Value;	Increment ADDRa–b
1	0	1	0	1	0	Write Blue Value;	Modify RAM Location Increment ADDR0–7 Increment ADDRa–b
0	1	1	1	X	X	Read Address Register;	ADDR0–7 → D0–D7
0	1	1	0	0	0	Read Red Value;	Increment ADDRa–b
0	1	1	0	0	1	Read Green Value;	Increment ADDRa–b
0	1	1	0	1	0	Read Blue Value;	Increment ADDR0–7 Increment ADDRa–b
0	0	X	X	X	X	Invalid Operation	

Table III. Truth Table for Read/Write Operations

Frame Buffer Interface

The P0–P7 inputs are used to address the color palette RAM, as shown in Table IV. These inputs are latched on the rising edge of PCLK and address any of the 256 locations in the color palette RAM. The addressed location contains 18 bits of color (6 bits of red, 6 bits of green and 6 bits of blue) information. This data is transferred to the three DACs and is then converted to an analog output (RED, GREEN, BLUE), these outputs then control the red, green and blue electron guns in the monitor.

The $\overline{\text{BLANK}}$ input is also latched on the rising edge of PCLK. This is to maintain synchronization with the color data.

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
•	• •
•	• •
FFH	Color Palette RAM Location FFH

Table IV. Pixel Select/Color Palette Control Truth Table

Pixel Read Mask Register

The Pixel Read Mask Register in the ADV476 can be used to implement register level pixel processing, thereby cutting down on software overhead. This is achieved by gating the input pixel stream (P0–P7) with the contents of the pixel read mask register. The operation is a bitwise logical ANDing of the pixel data. The contents of this register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video frame buffer or the color palette RAM. The effect of this operation is to partition the color palette into a user determined number of color planes. This process can be used for special effects including animation, overlays and flashing objects.

(See also application note entitled "Animation Using the Pixel Read Mask Register of the ADV47x Series of Video RAM-DACs," available from Analog Devices (Pub No. E1316–15–10/89).

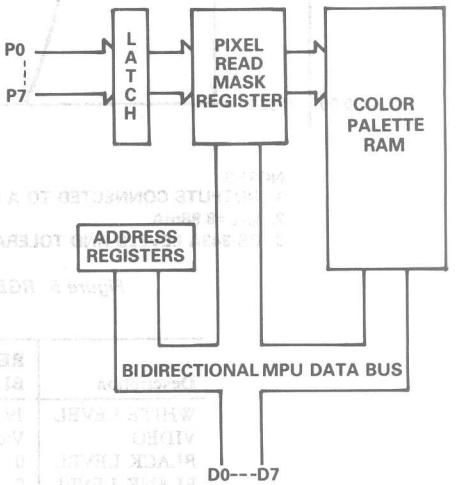


Figure 3. Block Diagram Showing Pixel Read Mask Register

Analog Interface

The ADV476 has three analog outputs, corresponding to the Red, Green and Blue video signals.

The Red, Green and Blue analog outputs of the ADV476 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5Ω load, such as a doubly-terminated 75Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly-terminated 75Ω load. This arrangement will develop RS-343A video output voltage levels across a 75Ω monitor. A simple method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged but the source termination resistance, Z_S, on each of the three DACs is increased from 75Ω to 150Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations" available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs, driving the doubly terminated 75Ω load of Figure 4a. The $\overline{\text{BLANK}}$ control input drives the analog outputs to the Black Level. $\overline{\text{BLANK}}$ is asserted prior to horizontal and vertical screen retrace. Table V details how the $\overline{\text{BLANK}}$ input modifies the output levels.

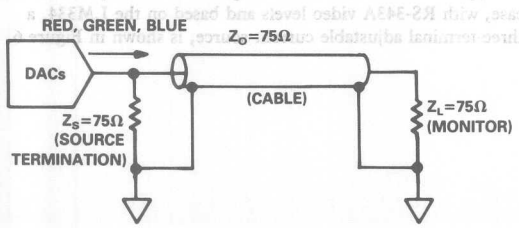


Figure 4a. Recommended Analog Output Termination for RS-343A

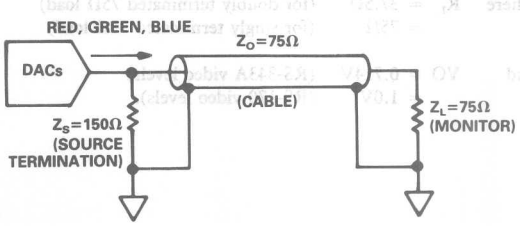
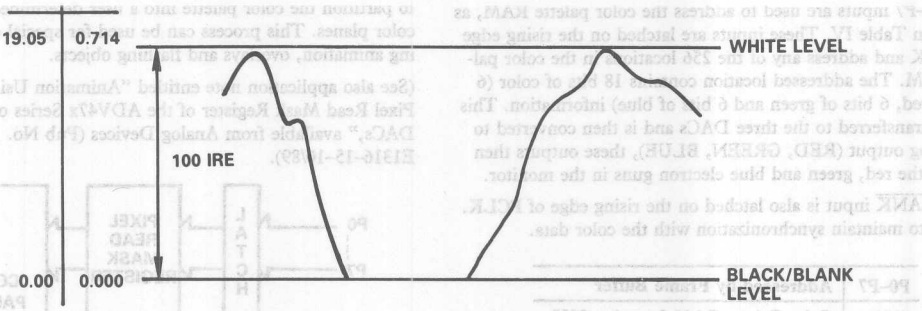


Figure 4b. Recommended Analog Output Termination for RS-170



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. I_{REF}=8.88mA.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. RGB Video Output Waveform

Description	RED, GREEN, BLUE, (mA)[1]	BLANK	DAC Input Data
WHITE LEVEL	19.05	1	FFH
VIDEO	Video	1	DATA
BLACK LEVEL	0	1	00H
BLANK LEVEL	0	0	xxH

NOTE
[1]Typical with full scale RED, GREEN, BLUE = 19.05mA. I_{REF} = 8.88mA.

Table V. Video Output Truth Table

Reference Input

The ADV476 requires an active current reference to enable the DACs provide stable and accurate video output levels. The relationship between the output voltage and the required input reference current is given by:

$$I_{REF} = \frac{VO\ (FULL\ SCALE)}{2.15 \times R_L}$$

where R_L = 37.5Ω (for doubly terminated 75Ω load)
= 75Ω (for singly terminated 75Ω load)

and VO = 0.714V (RS-343A video levels)
= 1.0V (RS-170 video levels).

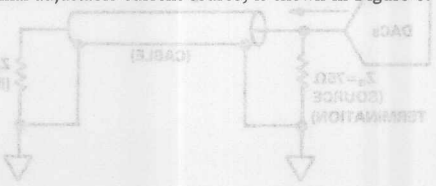
In a standard application which requires RS-343A video levels to be driven into a doubly terminated 75Ω load (R_L = 37.5Ω), the necessary reference input current is:

I_{REF} = 8.88mA.

To drive the same levels into a singly terminated 75Ω load (R_L = 75Ω), the reference current is:

I_{REF} = 4.44mA.

A suggested current reference design for the doubly terminated case, with RS-343A video levels and based on the LM334, a three-terminal adjustable current source, is shown in Figure 6.



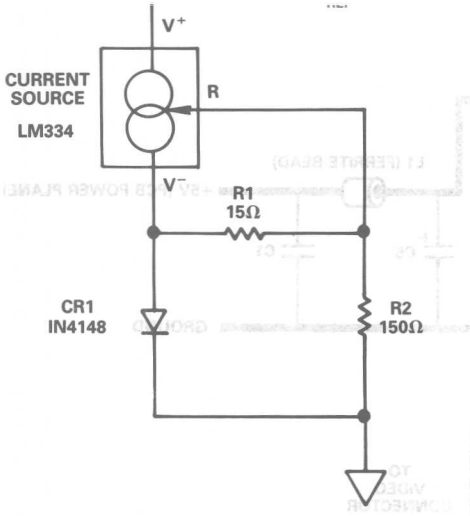


Figure 6. Current Reference Design Using an LM334 Current Source

PC BOARD LAYOUT CONSIDERATIONS

The ADV476 is optimally designed for lowest noise performance, both radiated and conducted noise. For optimum system noise performance, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV476 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{CC} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV476 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV476.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane (V_{CC}) should encompass the ADV476 and all associated analog circuitry. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located within three inches of the ADV476.

on the PC board, and the analog power plane should provide power to all ADV476 power pins, current reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors, see Figure 7.

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV476 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV476 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV476 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane and not the analog power plane.

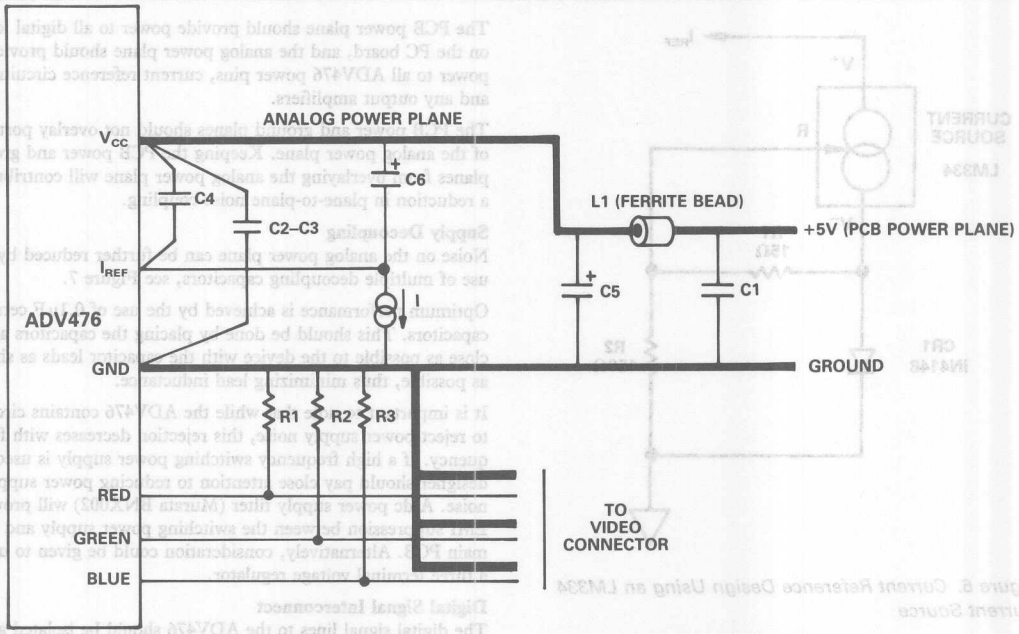
Analog Signal Interconnect

The ADV476 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75Ω. This termination resistance should be as close as possible to the ADV476 to minimize reflections.

Note: For additional information on PC Board Layout see application note "Design and Layout of a Video Graphics System for Reduced EMI," available from Analog Devices (Pub. No. E1309–15–10/89).



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C5	10μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C6	47μF TANTALUM CAPACITOR	MALLORY CSR13F476KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 7. ADV476 Typical Connection Diagram and Component List

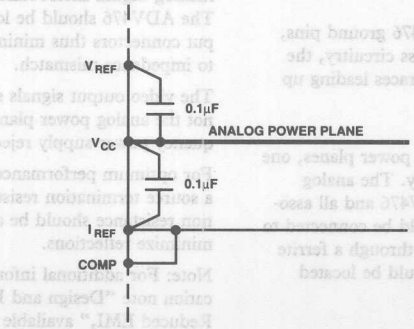


Figure 8. Connection of V_{REF} and COMP with the ADV476KP (44-Pin PLCC)

CMOS, 80 MHz Monolithic 256 Word Power-Down Color Palette RAM-DACs

ADV477/ADV475

FEATURES

Personal System/2* and VGA* Compatible
80, 66, 50 and 35 MHz Pipelined Operation
ADV478/ADV471 (ADV®) Pin and Functional Compatible
Power-Down Mode
On-Board Voltage Reference
Antisparkle Circuit
Analog Output Comparators
ADV477:
- **Triple 8-Bit D/A Converters**
- **256 × 24 Color Palette RAM**
- **15 × 24 Overlay Registers**

ADV475:
- **Triple 6-Bit D/A Converters**
- **256 × 18 Color Palette RAM**
- **15 × 18 Overlay Registers**

RS-343A/RS-170 Compatible Outputs
Sync on all Three Channels
Programmable Pedestal
+5 V CMOS Monolithic Construction
44-Pin PLCC Package

APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Laptop Computers
Desktop Publishing

AVAILABLE CLOCK RATES

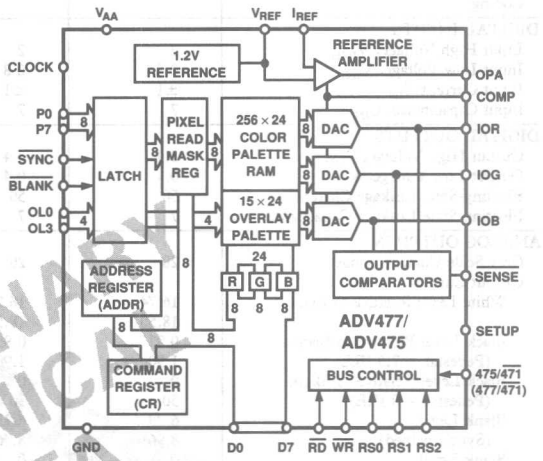
80 MHz
66 MHz
50 MHz
35 MHz

GENERAL DESCRIPTION

The ADV477 and ADV475 are pin-, functional-, and software-compatible RAM-DACs designed specifically for Personal System/2 (PS/2) compatible color graphics. They are a direct plug-in upgrade for the ADV478 and ADV471. Both support the existing 6-bit color VGA standard while also allowing for an upgrade path to 8-bit color resolution.

ADV is a trademark of Analog Devices, Inc.
***Personal System/2, PS/2, VGA and XGA are trademarks of International Business Machines Corp.**

FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN NAMES IN PARENTHESES DENOTE ADV477

PRELIMINARY TECHNICAL DATA

The ADV477 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. The ADV475 has a 256 × 18 color lookup table with triple 6-bit video D/A converters. New features on the ADV477/ADV475 include an on-board 1.2 V voltage reference, analog output comparators for self diagnostics and debugging as well as a power-down or sleep mode.

The power-down mode allows the ADV477/ADV475 to be put into a sleep mode with significant reduction in power consumption. This is ideal for laptop computers that may occasionally require the optional ability to drive an analog RGB monitor, but whose design is dictated by a desire to minimize power consumption.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc., at the hardware level. Also supported is a pixel read mask register and the ability to encode sync information on all three channels.

The ADV477/ADV475 generates RS343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADV477/ADV475—SPECIFICATIONS

(V_{AA}[1] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.)

Parameter	ADV477	ADV475	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	8	6	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity	±1	±0.25	LSB max	
Differential Nonlinearity	±1	±0.25	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale	
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	50	μA max	
Floating-State Leakage Capacitance	7	7	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	20	20	mA max	
Output Current				
White Level Relative to Black	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level Relative to Blank	0.95	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	1.90	mA max	
Black Level Relative to Blank	0	0	μA min	Typically 5 μA, SETUP = GND
(Pedestal = 0 IRE)	50	50	μA max	
Blank Level	6.29	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	8.96	mA max	
Blank Level	0	0	μA min	Typically 5 μA
(Sync Disabled)	50	50	μA max	
Sync Level	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB size	69.1	279.68	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.5	+1.5	V max	
Output Capacitance, C_{OUT}	30	30	pF max	f = 1 MHz, I_{OUT} = 0 mA
Output Impedance, R_{OUT}	10	10	kΩ typ	
VOLTAGE REFERENCE				
Internal Voltage Reference	1.1/1.3	1.1/1.3	V min/V max	Typically 1.235 V
External Voltage Reference Range	1.14/1.26	1.14/1.26	V min/V max	
POWER SUPPLY				
Supply Voltage, V_{AA}	4.75/5.25	4.75/5.25	V min/V max	80 MHz and 66 MHz Parts
	4.50/5.50	4.50/5.50	V min/V max	50 MHz and 35 MHz Parts
Supply Current, I_{AA}				
Normal Operation	200	200	mA max	Typically 160 mA
Power Down Mode[3]	10	10	mA max	Typically 5 mA
Power Supply Rejection Ratio	0.5	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE				
Clock and Data Feedthrough[4, 5]	−30	−30	dB typ	
Glitch Impulse[4, 5]	75	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	−23	dB typ	

NOTES
[1]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.
[2]Temperature Range (T_{MIN} to T_{MAX}): 0°C to + 70°C.
[3]External Voltage/Current Reference disabled. Temperature: +25 °C to +70 °C. All digital inputs at 0.4 V.
[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[5]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[6]DAC-to-DAC Crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[3], unless otherwise noted.)

Parameter	80 MHz Version	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0–RS2 Setup Time
t_2	10	10	10	10	ns min	RS0–RS2 Hold Time
t_3[4]	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	5	ns min	Read Data Hold Time
t_7	10	10	10	10	ns min	Write Data Setup Time
t_8	10	10	10	10	ns min	Write Data Hold Time
t_9	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	6 × t_{13}	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{12}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{13}	12.5	15.15	20	28	ns min	Clock Cycle Time
t_{14}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	13	20	28	ns max	Analog Output Settling Time
t_{19}	1	1	1	1	µs typ	$\overline{SENSE}$ Output Delay
t_{SK}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	4 × t_{13}	4 × t_{13}	4 × t_{13}	4 × t_{13}	ns min	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 2a.
[2]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.
[3]Temperature Range (T_{MIN} to T_{MAX}): 0°C to +70°C.
[4]t_3 and t_4 are measured with the load circuit of Figure 3 and are defined as the time required for an output to cross 0.4 V or 2.4 V.
[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.
[6]Settling time does not include clock and data feedthrough.

Specifications subject to change without notice.

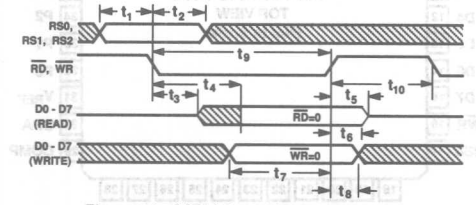


Figure 1. MPU Read/Write Timing

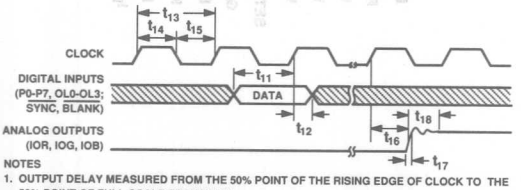


Figure 2a. Video Input/Output Timing

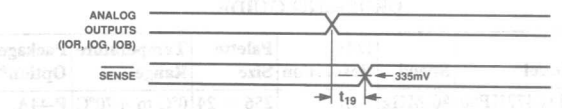


Figure 2b. Video Output vs. SENSE Timing

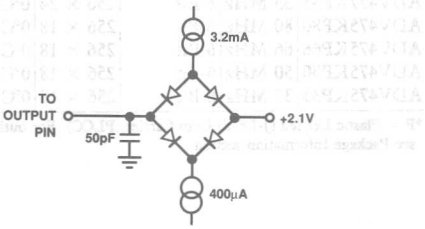


Figure 3. Load Circuit for Bus Access and Relinquish Time

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80 MHz, 66 MHz Parts		4.75	5.00	5.25	Volts
50 MHz, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
I_{REF} Current	I_{REF}				
Standard RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . 7 V
Voltage on any Digital Pin . . . GND − 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . 220°C
IOR, IOG, IOB to GND[1] . . . . . 0 V to V_{AA}

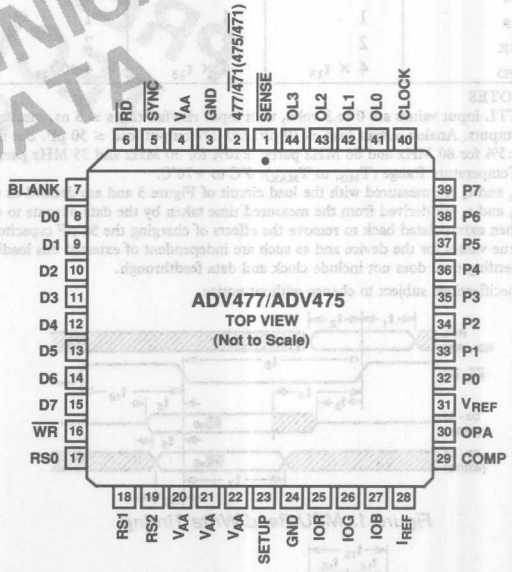
NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

PIN CONFIGURATION

PLCC



ORDERING GUIDE

Model	Speed	DAC Resolution	Palette Size	Temperature Range	Package Option*
ADV477KP80	80 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP66	66 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP50	50 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP35	35 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV475KP80	80 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP66	66 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP50	50 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP35	35 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A

*P = Plastic Leaded (J-Lead) Chip Carrier (PLCC). For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	Full-scale adjust control. Note that the IRE relationships are maintained, regardless of the full-scale output current. When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $R_{SET}\,(\Omega) = K \times 1{,}000 \times V_{REF}\,(v) / I_{OUT}\,(mA)$ K is defined in the table below. It is recommended that a 147 Ω value of R_{SET} resistor be used for doubly terminated 75 Ω loads (RS-343A applications). For PS/2 applications, where 0.7 V is driven into 50 Ω and which doesn't have $\overline{\text{SYNC}}$ encoded, a 182 Ω resistor is recommended. When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is: $I_{REF}\,(mA) = I_{OUT}\,(mA) / K$

Part	Color Resolution	Pedestal	K ($\overline{\text{SYNC}}$ Enabled)	K ($\overline{\text{SYNC}}$ Disabled)
ADV477	6-Bit	7.5 IRE	3.170	2.26
	8-Bit	7.5 IRE	3.195	2.28
	6-Bit	0 IRE	3.000	2.10
	8-Bit	0 IRE	3.025	2.12
ADV475	6-Bit	7.5 IRE	3.170	2.26
	8-Bit	0 IRE	3.000	2.10

COMP	Compensation pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.2v (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA}. When using the internal reference circuitry, this pin should only be connected to the bypass capacitor.
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION (continued)

Pin Mnemonic	Function
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{WR}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
475/$\overline{471}$ (477/$\overline{471}$)	ADV475 (ADV477) or ADV471 select input (TTL compatible). When this input is floating or a logical zero, the ADV477/ADV475 behaves exactly as an ADV471 with antisparkle capabilities. When this input is at a logical one, the extra capabilities of the ADV477/ADV475 are available. The Command Register (CR) becomes active.
$\overline{SENSE}$	Sense Output (TTL compatible). $\overline{SENSE}$ is a logical zero if one or more of the IOR, IOG and IOB outputs have exceeded the internal voltage reference level (335 mV).

TERMINOLOGY

BLANKING LEVEL
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)
The position of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and display images.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the Reference Black level and the blanking level.

SYNC LEVEL
The peak level of the composite SYNC signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface
The ADV477 and ADV475 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

Three address decode lines, RS0–RS2, specify whether the MPU is accessing the address register, the color palette RAM, the overlay registers, or read mask register. These controls also determine whether this access is a read or write function. Table I illustrates this decoding. The 8-bit address register is used to address the contents of the color palette RAM and overlay registers.

Table I. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Command Register*

*Available only when the 475/471 (477/471) pin is a logic "1."

Color Palette Writes
The MPU writes to the address register (selecting RAM write mode, RS2 = 0, RS1 = 0 and RS0 = 0) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and are written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the palette by initially writing the start address and then performing a sequence of red, green and blue writes. The address automatically increments to the next highest location after a blue write.

PRELIMINARY TECHNICAL DATA

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Color Palette Reads

The MPU writes to the address register (selecting RAM read mode, RS2 = 0, RS1 = 1 and RS0 = 1) with the address of the color palette RAM location to be read back. The contents of the palette RAM are copied to the red, green and blue registers and the address register increments to point to the next palette RAM location. The MPU then perform three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the blue read cycle, the 24/18 bit contents of the palette RAM at the location specified by the address register is loaded into the red, green and blue registers. The address register then increments to the next location which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the palette by initially writing the start address and then performing a sequence of red, green and blue reads. The address automatically increments to the next highest location after a blue read.

Overlay Color Writes

The MPU writes to the address register (selecting OVERLAY REGISTER write mode, RS2 = 1, RS1 = 0 and RS0 = 0) with the address of the overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers (RS2 = 1, RS1 = 0, RS0 = 1). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and written to the overlay register specified by the address register. The address register then increments to the next overlay register which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the overlay registers by initially writing the start address and then performing a sequence of red, green and blue writes. The address automatically increments to the next highest location after a blue write.

Overlay Color Reads

The MPU writes to the address register (selecting OVERLAY REGISTER read mode, RS2 = 1, RS1 = 1 and RS0 = 1) with the address of the overlay register to be read back. The contents of the overlay register are copied to the red, green and blue registers and the address register increments to point to the next highest overlay register. The MPU then perform three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the Overlay Registers (RS2 = 1, RS1 = 0, RS0 = 1). After the blue read cycle, the 24/18 bit contents of the overlay register at the specified address register location is loaded into the red, green and blue registers. The address register then increments to the next overlay register which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the overlay registers by initially writing the start address and then performing a sequence of red, green and blue reads. The address automatically increments to the next highest location after a blue read.

Internal Address Register (ADDR)

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits (since there are only 15 overlay registers) of the address register (ADDR4–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Note: The pixel clock must be active for MPU accesses to the color palette.

Synchronization

The MPU interface operates asynchronously to the pixel port. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B as shown in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Internal circuitry has been included to reduce noticeable sparkling on some CRT systems which can occur during MPU accesses to the color palette RAM.

Table II. Address Register (ADDR) Operation

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	0	1	Color Palette RAM
	xxxx 0000	1	0	1	Reserved
	xxxx 0001	1	0	1	Overlay Color 1
	xxxx 0010	1	0	1	Overlay Color 2
	.	.	.	.	.
	.	.	.	.	.
	xxxx 1111	1	0	1	Overlay Color 15

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by setting the 477/471 input of the ADV477 and 475/471 input of the 475/471 to a logic "0". The internal Command Register (CR) is disabled and 6-bit color resolution is automatically selected. Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical "0." It should be noted that when the ADV477 is in 6-bit mode, full-scale output current will be reduced by approximately 1.5% relative to the 8-bit mode. This is the case since the 2 LSBs of each of the three DACs are always set to zero in 6-bit mode.

ADV477/ADV475 Enhancements

The enhanced modes of operation provided by the ADV477/ADV475 can be implemented when the 477/471 and 475/471 pins on the ADV477 and ADV475, respectively, are at a logic "1." The internal Command Register (CR) now becomes active, thereby allowing for full programmability of these enhanced modes. Command bit CR1 sets the ADV477 to operate in 6-bit or 8-bit color resolution.

Command Register (CR)

The ADV477/ADV475 has an internal command register which becomes active when the 475/$\overline{471}$ (477/$\overline{471}$) pin is a logic "1." This register is 8 bits wide, CR0–CR7 and is directly mapped to the MPU data bus on the part, D0–D7. The command register can be written to or read from. It is not initialized, therefore it must be set if the 477/471 (475/471) pin is high. Figure 4 shows what each bit of the CR register controls and shows the values it must be programmed to for various modes of operation.

sleep mode. This is especially useful in power sensitive systems such as portable or lap-top computers. This power-down mode is controlled by the Power-Down bit (CR0) of the command register. When CR0 is "0", the device goes into power-down mode. When CR0 is "1", the part operates normally.

The power to three DACs and the RAM is turned off while CR0 is low. The contents of the palette RAM, however, remain valid in the power-down state and normal read/write operations can be made to the part over the MPU port. During the actual read/write operations (when CR0 = 0) the RAM will be temporarily powered up, and on completion of MPU accesses the RAM returns to its shut-down state.

The three DACs in the ADV477/ADV475 will be shut off in the power-down mode only when the part is operated in the voltage reference configuration (internal or external reference). A further decrease in power consumption can be achieved by turning off the external voltage reference.

If operating in the current reference configuration, the I_{REF} current needs to be reduced to 0 mA when in the power-down mode, in order to minimize the total power consumption.

On-Board Comparators and $\overline{\text{SENSE}}$ Control

The three on-board comparators can be used in conjunction with the $\overline{\text{SENSE}}$ output control to determine whether or not a CRT is connected to the RGB analog outputs.

$\overline{\text{SENSE}}$ will be a logic "0" if the voltage on one or more of the IOR, IOG and IOB outputs is greater than the internal voltage reference level of 335 mV. A loaded ($\overline{\text{SENSE}}$ = "1") and unloaded ($\overline{\text{SENSE}}$ = "0") RGB line is now discernible.

PRELIMINARY TECHNICAL DATA

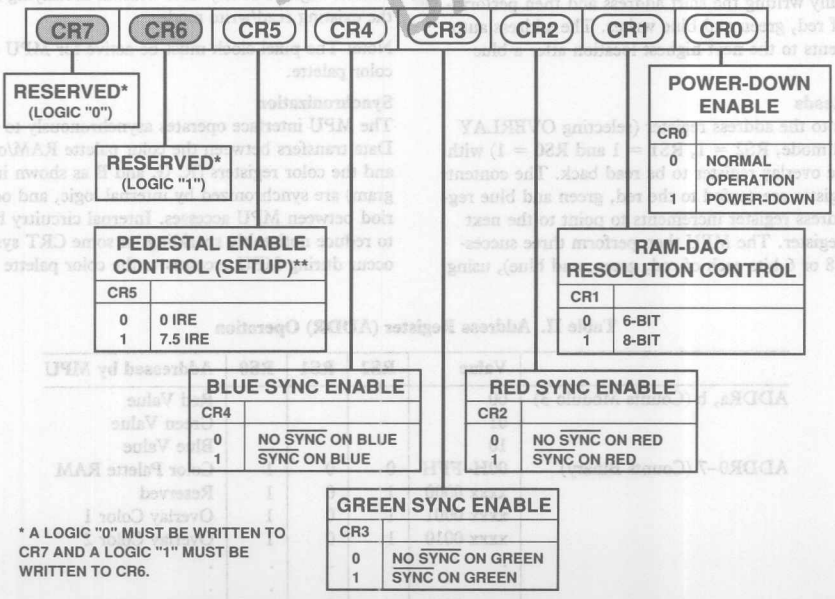


Figure 4. Command Register (CR)

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This internal voltage reference level has a ±5% tolerance when using an external voltage reference. A tolerance of ±10% is achievable with the ADV477/ADV475's internal voltage reference.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs, which are latched in on the rising edge of CLOCK, are used to address the color palette RAM and overlay registers, as shown in Table III. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides an RGB word (24 bits for the ADV477 and 18 bits for the ADV475) of color information for the three RGB D/A converters.

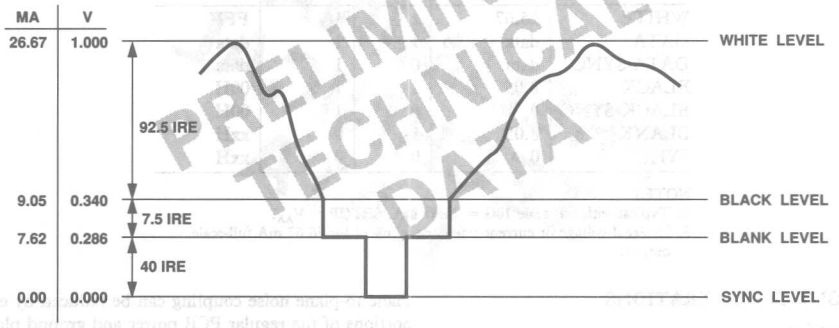
The SYNC and BLANK inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 5 and 6. Tables IV and V detail how the SYNC and BLANK inputs modify the output levels.

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)

OL0–OL3	P0–P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
.	.	.
.	.	.
0H	FFH	Color Palette RAM Location FFH
1H	xxH	Overlay Color 1
2H	xxH	Overlay Color 2
.	.	.
.	.	.
FH	xxH	Overlay Color 15

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV477 and ADV475 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. Composite Video Output Waveform (SETUP = V_{AA})

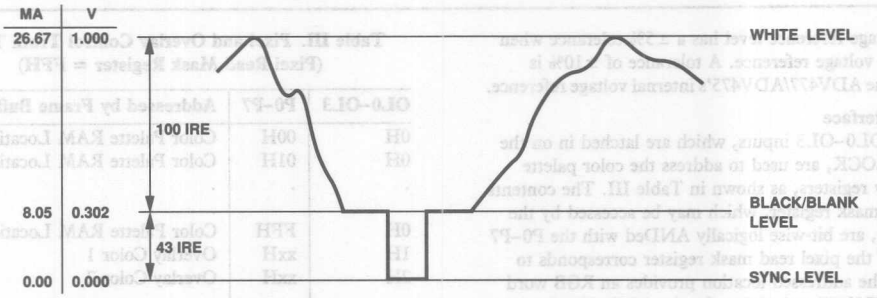
Table IV. Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	xxH
SYNC	0	0	0	xxH

NOTES
1. Typical with full scale 10G = 26.67 mA, SETUP = V_{AA}.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.

PRELIMINARY TECHNICAL DATA

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NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 6. Composite Video Output Waveform (SETUP = GND)

Table V. Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	data + 8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	8.05	1	0	xxH
SYNC	0	0	0	xxH

NOTES
1. Typical with full scale 10G = 26.67 mA, SETUP = V_{AA}.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.

PRELIMINARY TECHNICAL DATA

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the ADV477/ADV475 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV477/ADV475 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV477/ADV475, the analog output traces, and all the digital signal traces leading up to the ADV477/ADV475.

Power Planes

The ADV477/ADV475 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 7, 8 and 9. This bead should be located within three inches of the ADV477/ADV475.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV477/ADV475 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV475 and ADV477 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV477/ADV475 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

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Due to the high clock rates involved, long clock lines to the ADV477/ADV475 should be avoided to reduce noise pickup.

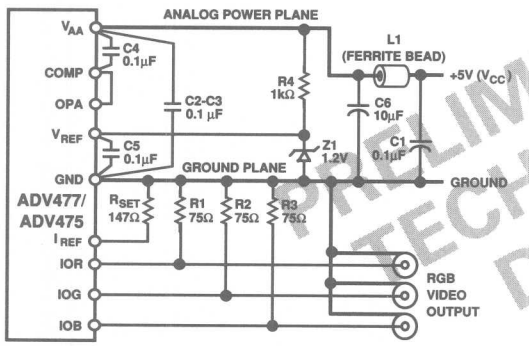
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV477/ADV475 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

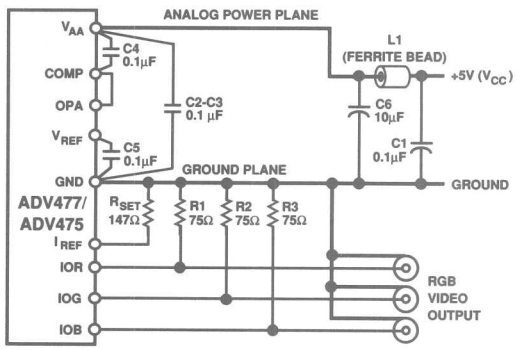
The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV477/ADV475 to minimize reflections.



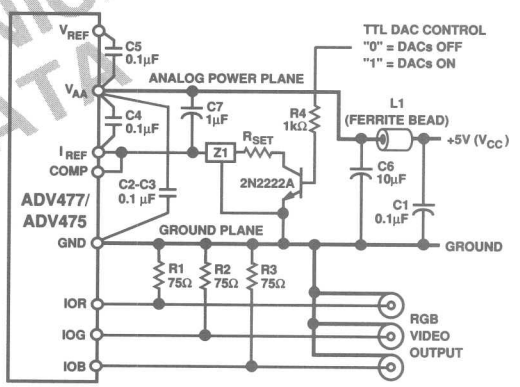
COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R4	1kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.23V VOLTAGE REFERENCE	AD589JN

Figure 7. Typical Connection Diagram (External Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R_{SET}	1% METAL FILM RESISTOR	

Figure 8. Typical Connection Diagram (Internal Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C7	1µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
Z1	ADJUSTABLE REGULATOR	LM317LZ
R_{SET}	1% METAL FILM RESISTOR	

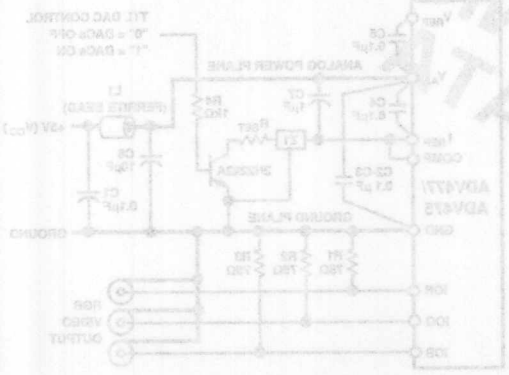
Figure 9. Typical Connection Diagram (External Current Reference)

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE PRF1215Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R4	1kΩ 5% RESISTOR	
RSET	1% METAL FILM RESISTOR	
Z1	1.23V VOLTAGE REFERENCE	AD589JH

Figure 2. Typical Connection Diagram
(External Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE PRF1215Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C7	1µF TANTALUM CAPACITOR	MALLORY CSR13G105KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
Z1	ADJUSTABLE BANDGAP REFERENCE	LM317LZ
RSET	1% METAL FILM RESISTOR	

Figure 3. Typical Connection Diagram
(External Current Reference)

PRELIMINARY TECHNICAL DATA

2

FEATURES

Personal System/2* Compatible
80MHz Pipelined Operation
Triple 8-Bit (6-Bit) D/A Converters
256×24(18) Color Palette RAM
15×24(18) Overlay Registers
RS-343A/RS-170 Compatible Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
External Voltage or Current Reference
Standard MPU Interface
+5V CMOS Monolithic Construction
44-Pin PLCC Package
Power Dissipation: 800mW

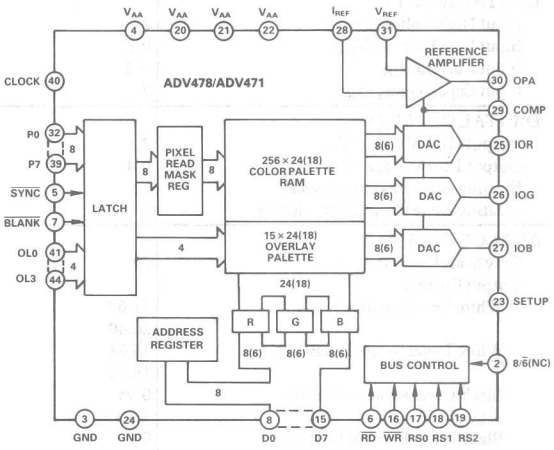
APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

80MHz
66MHz
50MHz
35MHz

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

GENERAL DESCRIPTION

The ADV478 (ADV®) and ADV471 are pin compatible and software compatible RAM-DACs designed specifically for Personal System/2 compatible color graphics.

The ADV478 has a 256×24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6 bits or 8 bits per color operation. The ADV471 has a 256×18 color lookup table with triple 6-bit video D/A converters.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. Fifteen overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is a pixel read mask register and sync generation on all three channels.

The ADV478 and ADV471 generate RS-343A compatible video signals into a doubly terminated 75Ω load, and RS-170 compatible video signals into a singly terminated 75Ω load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ±1LSB for the ADV478 and ±1/4LSB for the ADV471 over the full temperature range.

ADV is a registered trademark of Analog Devices, Inc.
*Personal System/2 is a trademark of International Business Machines Corp.

ADV478/ADV471 — SPECIFICATIONS (V_{AA}[1] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = +1.235V. R_{SET} = 147Ω. All specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)[3]	8 (6)	Bits	
Accuracy (Each DAC)[3]			
Integral Nonlinearity	±1 (1/4)	LSB max	
Differential Nonlinearity	±1 (1/4)	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	7	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating-State Leakage Current	50	μA max	
Floating-State Output Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
(SETUP = V_{AA})	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5μA
(SETUP = GND)	50	μA max	
Blank Level	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level	0	μA min	Typically 5μA
	50	μA max	
LSB Size[3]	69.1 (279.68)	μA typ	8/$\overline{6}$ = Logical 1 for ADV478
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.5	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	Tested in Voltage Reference Configuration with V_{REF} = 1.235V
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	80MHz and 66MHz Parts
	4.50/5.50	V min/V max	50MHz and 35MHz Parts
Supply Current, I_{AA}	220	mA max	Typically 180mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1kHz, COMP = 0.1μF
Power Dissipation	1100	mW max	Typically 900mW, V_{AA} = 5V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[4,5]	−30	dB typ	
Glitch Impulse[4,5]	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	dB typ	

NOTES

[1] ±5% for 80MHz and 66MHz parts; ±10% for 50MHz and 35MHz parts.

[2] Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[3] Numbers in parentheses indicate ADV471 parameter value.

[4] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

[5] TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, D0 – D7 output load ≤50pF. See timing notes in Figure 2.

[6] DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = 1.235V. R_{SET} = 147Ω. All Specifications T_{min} to T_{max}[3].)

Parameter	KP80 Version	KP66 Version	KP50 Version	KP35 Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0 – RS2 Setup Time
t_2	10	10	10	10	ns min	RS0 – RS2 Hold Time
t_3	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	10	10	ns min	Write Data Setup Time
t_7	10	10	10	10	ns min	Write Data Hold Time
t_8	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{11}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{12}	12.5	15.3	20	28	ns min	Clock Cycle Time
t_{13}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	30	ns max	Analog Output Delay
t_{16}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[4]	13	15.3	20	28	ns typ	Analog Output Settling Time
t_{18}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	ns min	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0 – D7 output load ≤50pF. See timing notes in Figure 2.
[2]±5% for 80MHz and 66MHz parts; ±5% for 50MHz and 35MHz parts.
[3]Temperature Range (T_{min} to T_{max}); 0 to +70°C.
[4]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.

Specifications subject to change without notice

TIMING DIAGRAMS

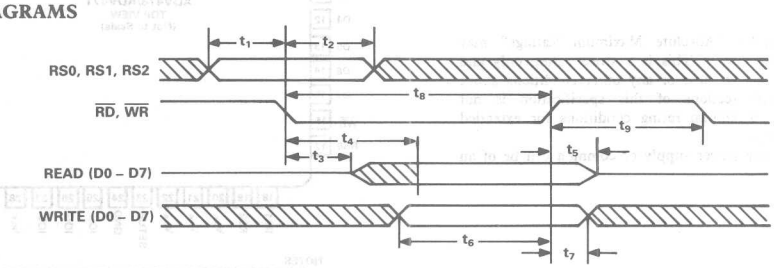
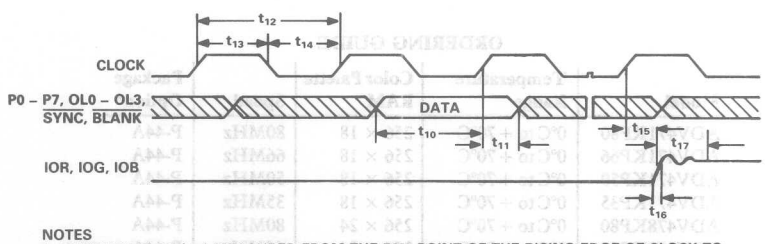


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB (ADV478) OR ±1/4LSB (ADV471).
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80MHz, 66MHz Parts		4.75	5.00	5.25	Volts
50, 35MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
Reference Current	I_{REF}	−3		−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ABSOLUTE MAXIMUM RATINGS*

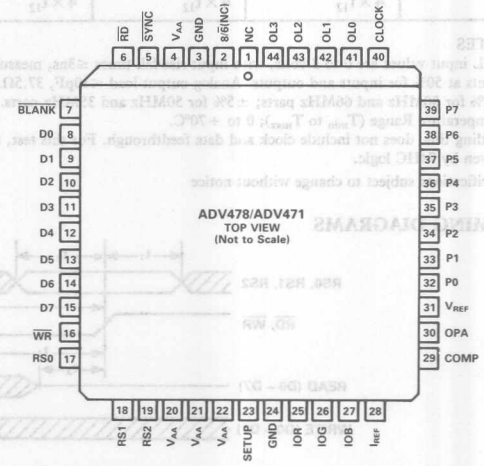
V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . GND −0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Junction Temperature (T_J) . . . . . +175°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG to GND[1] . . . . . 0V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

PLCC PIN CONFIGURATION



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Color Palette RAM	Speed	Package Option*
ADV471KP80	0°C to +70°C	256 × 18	80MHz	P-44A
ADV471KP66	0°C to +70°C	256 × 18	66MHz	P-44A
ADV471KP50	0°C to +70°C	256 × 18	50MHz	P-44A
ADV471KP35	0°C to +70°C	256 × 18	35MHz	P-44A
ADV478KP80	0°C to +70°C	256 × 24	80MHz	P-44A
ADV478KP66	0°C to +70°C	256 × 24	66MHz	P-44A
ADV478KP50	0°C to +70°C	256 × 24	50MHz	P-44A
ADV478KP35	0°C to +70°C	256 × 24	35MHz	P-44A

*P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level as illustrated in Tables IV and V. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Tables IV and V; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 – P7, OL0 – OL3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0 – P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 – OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table III. When accessing the overlay palette, the P0 – P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable (Figures 5 and 6).
I_{REF}	Full-scale adjust control. Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. When using an external voltage reference (Figure 5), a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $R_{SET}\ (\Omega) = K * 1{,}000 * V_{REF}\ (V)/I_{OUT}\ (mA)$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75Ω loads. When using an external current reference (Figure 6), the relationship between I_{REF} and the full-scale output current on each output is: $I_{REF}\ (mA) = I_{OUT}\ (mA)/K$

Mode	Pedestal	K	R_{SET} (Ω)
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

COMP	Compensation pin. If an external voltage reference is used (Figure 5), this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1μF ceramic capacitor must always be used to decouple this input to V_{AA} as shown in Figures 5 and 6.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
V_{AA}	Analog power. All V_{AA} pins must be connected to the Analog Power Plane.
GND	Analog ground. All GND pins must be connected to the Ground Plane.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0 – D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0 – RS2 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations. See Figure 1.

PIN FUNCTION DESCRIPTION (Continued)

Pin Mnemonic	Function
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0 – RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 – RS2 specify the type of read or write operation being performed as illustrated in Tables I and II.
D0 – D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This control input specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and are logical zero during color read cycles). This control input is implemented only on the ADV478.

TERMINOLOGY

Blanking Level
The level seperating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite SYNC Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

SYNC Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV478 and ADV471 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 – RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers or read mask register, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

To write color data, the MPU writes to the address register (selecting RAM or overlay write mode) with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the ADV471) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Reserved

Table I. Control Input Truth Table

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4 – 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G and B in the block diagram) are synchronized by internal logic and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM and overlay registers may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle (ADDR0 – 7), are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

	Value	RS2	RS1	RS0	Addressed By MPU
ADDRa,b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0 – 7 (Counts Binary)	00H – FFH	0	0	1	Color Palette RAM
	XXXX 0000	1	0	1	Reserved
	XXXX 0001	1	0	1	Overlay Color 1
	XXXX 0010	1	0	1	Overlay Color 2
	•	•	•	•	•
	•	•	•	•	•
	XXXX 1111	1	0	1	Overlay Color 15

Table II. Address Register (ADDR) Operation

ADV478 Data Bus Interface

On the ADV478, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8 bits (8/$\overline{6}$ = logical one) or 6 bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the ADV471), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

ADV471 Data Bus Interface

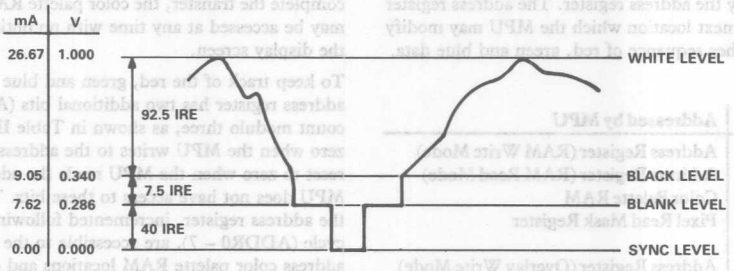
Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Frame Buffer Interface

The P0 – P7 and OL0 – OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table III.

OL0 – OL3	P0 – P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
•	•	•
•	•	•
0H	FFH	Color Palette RAM Location FFH
1H	XXH	Overlay Color 1
2H	XXH	Overlay Color 2
•	•	•
•	•	•
FH	XXH	Overlay Color 15

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. Composite Video Output Waveform (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK LEVEL	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK LEVEL	7.62	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = V_{AA}.
External voltage or current reference adjusted for 26.67mA full-scale output.

Table IV. Video Output Truth Table (SETUP = V_{AA})

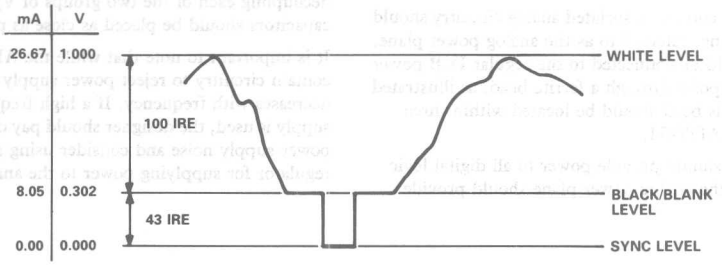
The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 – P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the ADV471) of color information to the three D/A converters.

For additional information on Pixel Mask Register, see application note "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs"(Publication Number E1316–15–10/89).

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables IV and V detail how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV478 and ADV471 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 4. Composite Video Output Waveform (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK LEVEL	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK LEVEL	8.05	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = GND
External voltage or current reference adjusted for 26.67mA full-scale output.

Table V. Video Output Truth Table (SETUP = GND)

Digital Signal Interconnect

The digital inputs to the ADV478/ADV471 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV478/ADV471 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

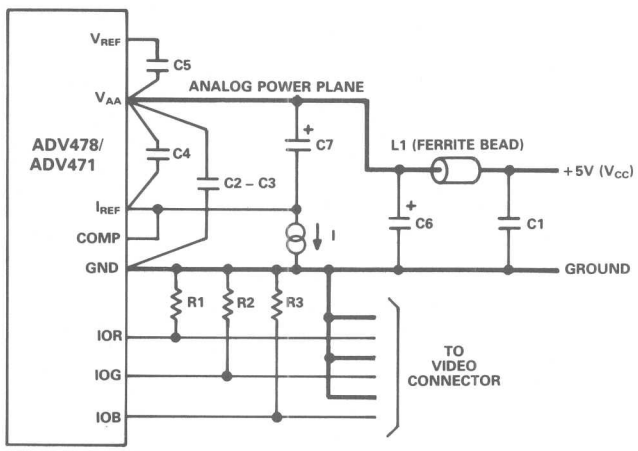
Analog Signal Interconnect

The ADV478/ADV471 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV478/ADV471 to minimize reflections.

NOTE: Additional information on PC Board layout can be obtained in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI" from Analog Devices (Publication Note E1309–15–10/89).



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
C7	47μF Tantalum Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C

Figure 6. Typical Connection Diagram and Component List (External Current Reference)

APPLICATION INFORMATION

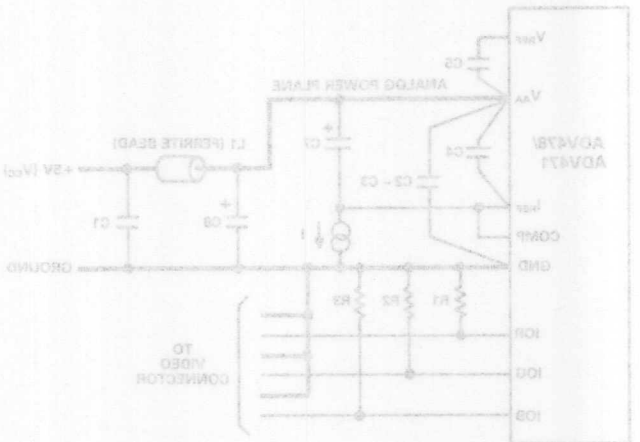
External Voltage vs. Current Reference

The ADV478/ADV471 is designed to have excellent performance using either an external voltage or current reference. The voltage reference design (Figure 5) has the advantages of temperature compensation, simplicity, lower cost and provides excellent power supply rejection. The current reference design (Figure 6) requires more components to provide adequate power supply rejection and temperature compensation (two transistors, three resistors and additional capacitors).

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that the DAC outputs be connected to a singly terminated 75Ωload. If the ADV478/ADV471 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.

If driving a large capacitive load (load RC> $1/(2\pi f_C)$), it is recommended that an output buffer (such as an AD848 or AD9617 with an unloaded gain>2) be used to drive a doubly terminated 75Ω load.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
C7	47μF Tantalum Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C

Figure 6. Typical Connection Diagram and Component List
(External Current Reference)

80 MHz, Triple 8-Bit Video DAC

ADV7120

FEATURES

80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP or 44-Pin PLCC Package
Power Dissipation: 400 mW

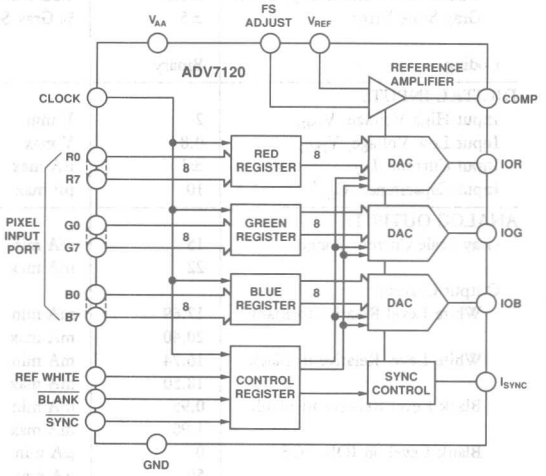
APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing
Direct Digital Synthesis (DDS)

SPEED GRADES

80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7120 (ADV®) is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV7120 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include composite sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV7120 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV7120 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6″, 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

ADV is a registered trademark of Analog Devices Inc.

ADV7120—SPECIFICATIONS

(V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{MIN} to T_{MAX}[1] unless otherwise noted).

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±0.5	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}* 12,082/R_{SET}) mA
			IOR, IOB = (V_{REF}* 8,627/R_{SET}) mA
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	9.5	mA max	
Sync Level on IOG	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	
Analog Output Skew	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[2]Sample tested at +25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

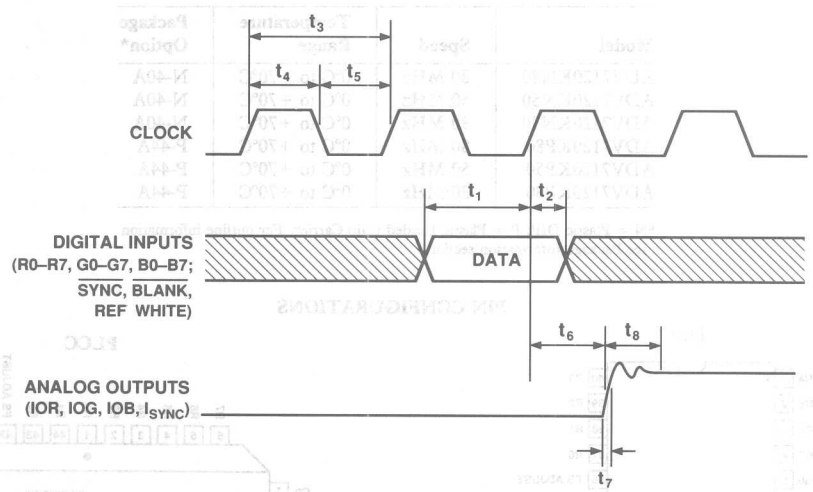
[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{max}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG, I_{SYNC} to GND[1] . . . . . 0 V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



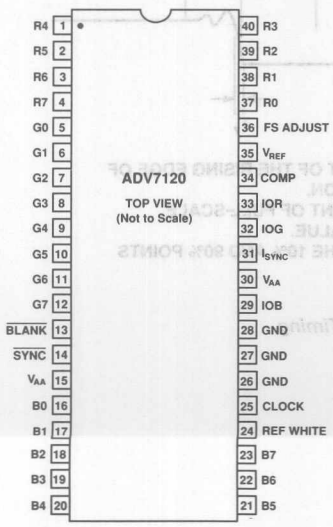
ORDERING GUIDE

Model	Speed	Temperature Range	Package Option*
ADV7120KN80	80 MHz	0°C to +70°C	N-40A
ADV7120KN50	50 MHz	0°C to +70°C	N-40A
ADV7120KN30	30 MHz	0°C to +70°C	N-40A
ADV7120KP80	80 MHz	0°C to +70°C	P-44A
ADV7120KP50	50 MHz	0°C to +70°C	P-44A
ADV7120KP30	30 MHz	0°C to +70°C	P-44A

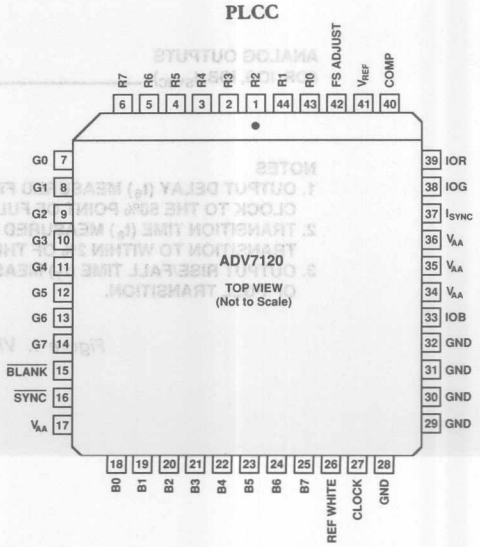
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R7, G0–G7, R0–R7 and REF WHITE pixel and control inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and REF WHITE pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the pixel input data (R0–R7, G0–G7 and B0–B7). REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output. This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: $I_{SYNC}\ (mA) = 3{,}455 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$ If sync information is not required on the green channel, I_{SYNC} should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $R_{SET}\ (\Omega) = 12{,}082 \times V_{REF}\ (V)/IOG\ (mA)$ The relationship between R_{SET} and the full-scale output current on IOR and IOB is given by: $IOR,\ IOB\ (mA) = 8{,}628 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.2 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7120 must be connected.
GND	Ground. All GND pins must be connected.

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

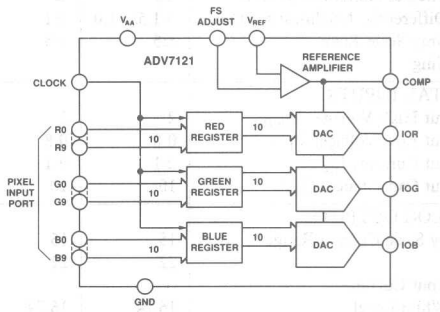
Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CMOS
80 MHz, Triple 10-Bit Video DACs
ADV7121/ADV7122

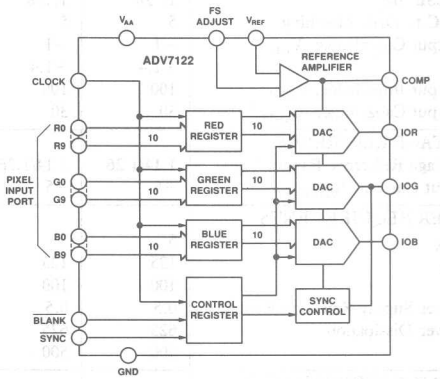
FEATURES
80 MHz Pipelined Operation
Triple 10-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP Package (ADV7121)
44-Pin PLCC Package (ADV7122)
Power Dissipation: 400 mW

APPLICATIONS
High Definition Television (HDTV)
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS)

SPEED GRADES
80 MHz
50 MHz
30 MHz



ADV7121 Functional Block Diagram



ADV7122 Functional Block Diagram

GENERAL DESCRIPTION

The ADV7121/ADV7122 (ADV®) is a video speed, digital-to-analog converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems including high definition television (HDTV). It consists of three, high speed, 10-bit, video D/A converters (RGB), a standard TTL input interface and high impedance, analog output, current sources.

The ADV7121/ADV7122 has three separate, 10-bit, pixel input ports, one each for red, green and blue video data. A single +5 V power supply, an external 1.23 V reference and pixel clock input is all that is required to make the part operational. The ADV7122 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$.

The ADV7121/ADV7122 is capable of generating RGB video output signals which are compatible with RS-343A, RS-170 and most proposed production system HDTV video standards, including SMPTE 240M.

The ADV7121/ADV7122 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The ADV7121 is packaged in a 0.6", 40-pin plastic DIP package. The ADV7122 is packaged in a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Guaranteed monotonic to 10 bits. Ten bits of resolution allows for implementation of linearization functions such as gamma correction and contrast enhancement.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A/RS-170 and the proposed SMPTE 240M standard for HDTV.

ADV is a registered trademark of Analog Devices, Inc.

Resolution (Each DAC)	10	10	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity, INL	±3	±2	LSB max	
Differential Nonlinearity, DNL	+1.5/−1.0	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale max	Max Gray Scale Current = (V_{REF}* 7,969/ R_{SET}) mA
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	10	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	15	15	mA min	
	22	22	mA max	
Output Current				
White Level	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB Size	17.28	17.28	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.4	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE				
Voltage Reference Range, V_{REF}	1.14/1.26	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	−5	mA typ	
POWER REQUIREMENTS				
V_{AA}	5	5	V nom	
I_{AA}	125	125	mA max	Typically 80 mA: 80 MHz Parts
	100	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio[2]	0.5	0.5	% / % max	Typically 0.12 %/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	625	mW max	Typically 400 mW: 80 MHz Parts
	500	500	mW max	Typically 350 mW: 50 MHz & 35 MHz Parts
DYNAMIC PERFORMANCE				
Glitch Impulse[2, 3]	50	50	pV secs typ	
DAC Noise[2, 3, 4]	200	200	pV secs typ	
Analog Output Skew	2	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}): 0 to +70°C.

[2]Sample tested at 25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

ADV7122—SPECIFICATIONS 560 Ω. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

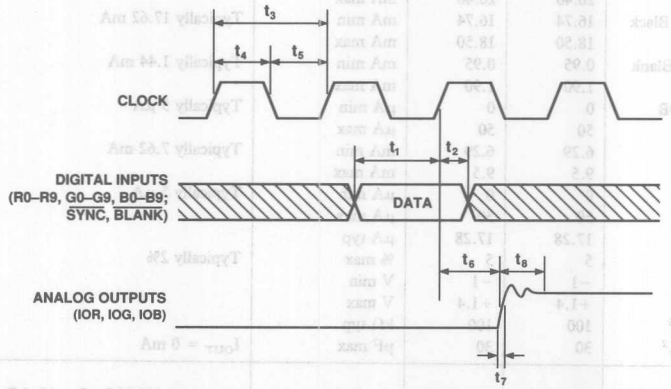
Parameter	J Version	K Version	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	10	10	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity, INL	±3	±2	LSB max	
Differential Nonlinearity, DNL	+1.5/−1.0	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}*12.082/R_{SET}) mA
				IOR, IOB = (V_{REF}*8,627/R_{SET}) mA
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	10	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	15	15	mA min	
	22	22	mA max	
Output Current				
White Level Relative to Blank	17.69	17.69	mA min	Typically 19.05 mA
	20.40	20.40	mA max	
White Level Relative to Black	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level Relative to Blank	0.95	0.95	mA min	Typically 1.44 mA
	1.90	1.90	mA max	
Black Level on IOR, IOB	0	0	μA min	Typically 5 μA
	50	50	μA max	
Black Level on IOG	6.29	6.29	mA min	Typically 7.62 mA
	9.5	9.5	mA max	
Sync Level on IOG	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB Size	17.28	17.28	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.4	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE				
Voltage Reference Range, V_{REF}	1.14/1.26	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	−5	mA typ	
POWER REQUIREMENTS				
V_{AA}	5	5	V nom	
I_{AA}	125	125	mA max	Typically 80 mA: 80 MHz Parts
	100	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio[2]	0.5	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.01 μF
Power Dissipation	625	625	mW max	Typically 400 mW: 80 MHz Parts
	500	500	mW max	Typically 350 mW: 50 MHz & 35 MHz Parts
DYNAMIC PERFORMANCE				
Glitch Impulse[2, 3]	50	50	pV secs typ	
DAC Noise[2, 3, 4]	200	200	pV secs typ	
Analog Output Skew	2	2	ns max	Typically 1 ns

NOTES
[1]Temperature Range (T_{min} to T_{max}): 0 to +70°C.
[2]Sample tested at 25°C to ensure compliance.
[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Versions	50 MHz Versions	30 MHz Versions	Units	Conditions/Comments
fmax	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C.
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.
4. SYNC AND BLANK DIGITAL INPUTS ARE NOT PROVIDED ON THE ADV7121.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ORDERING GUIDE

Model	Speed	Accuracy DNL	Accuracy INL	Temperature	Package Option[1]
ADV7121JN80	80 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121JN50	50 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121JN30	30 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121KN80	80MHz	±1	±2	0°C to +70°C	N-40A
ADV7121KN50	50MHz	±1	±2	0°C to +70°C	N-40A
ADV7121KN30	30 MHz	±1	±2	0°C to +70°C	N-40A
ADV7122JP80	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122JP50	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122JP30	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122KP80	80 MHz	±1	±2	0°C to +70°C	P-44A[2]
ADV7122KP50	50 MHz	±1	±2	0°C to +70°C	P-44A[2]
ADV7122KP30	30 MHz	±1	±2	0°C to +70°C	P-44A[2]

NOTES
[1]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]PLCC: Plastic Leaded Chip Carrier (J-lead).

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (5 secs) . . . . . 220°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG to GND[1] . . . . . 0 V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

2

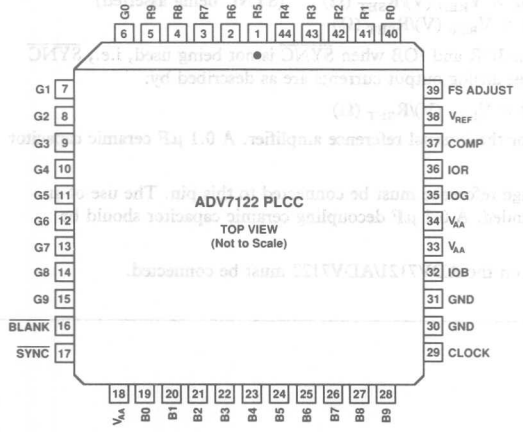
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATIONS

PLCC (P-44A) Package



DIP (N-40A) Package



Pin Mnemonic	Function
$\overline{\text{BLANK}}$*	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R9, G0–G9 and R0–R9 pixel inputs are ignored.
$\overline{\text{SYNC}}$*	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to logical zero.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
R0–R9, G0–G9, B0–B9	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: R_{SET} (Ω) = 12,082 × V_{REF} (V)/IOG (mA) The relationship between R_{SET} and the full-scale output current on IOR, IOG and IOB is given by: IOG* (mA) = 12,082 × V_{REF} (V)/R_{SET} (Ω) ($\overline{\text{SYNC}}$ being asserted) IOR, IOB (mA) = 8,628 × V_{REF} (V)/R_{SET} (Ω) The equation for IOG will be the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, i.e., $\overline{\text{SYNC}}$ tied permanently low. For the ADV7121, all three analog output currents are as described by: IOR, IOG, IOB (mA) = 7,969 × V_{REF} (V)/R_{SET} (Ω)
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.23V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7121/ADV7122 must be connected.
GND	Ground. All GND pins must be connected.

*$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ functions are not provided on the ADV7121.

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. A 10-bit DAC contains 1024 different levels, while an 8-bit DAC contains 256.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

2

CIRCUIT DESCRIPTION & OPERATION

The ADV7121/ADV7122 contains three 10-bit D/A converters, with three input channels, each containing a 10-bit register. Also integrated on board the part is a reference amplifier. CRT control functions $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are integrated on board the ADV7122.

Digital Inputs
Thirty bits of pixel data (color information) R0–R9, G0–G9 and B0–B9 are latched into the device on the rising edge of each clock cycle. This data is presented to to the three 10-bit DACs and is then converted to three analog (RGB) output waveforms. See Figure 2.

The ADV7122 has two additional control signals, which are latched to the analog video outputs in a similar fashion. $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs. Figure 3 shows the analog output, RGB video waveform of the ADV7121/ADV7122 . The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated.

Table I details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$.

All these digital inputs are specified to accept TTL logic levels.

Clock Input
The CLOCK input of the ADV7121/ADV7122 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

$$\textit{Dot Rate} = (\textit{Horiz Res}) \times (\textit{Vert Res}) \times (\textit{Refresh Rate}) / (\textit{Retrace Factor})$$

Horiz Res	=	Number of Pixels/Line.
Vert Res	=	Number of Lines/Frame.
Refresh Rate	=	Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.
Retrace Factor	=	Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

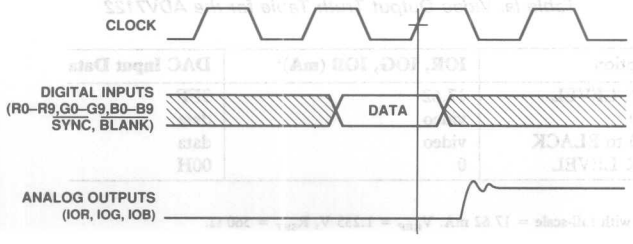


Figure 2. Video Data Input/Output

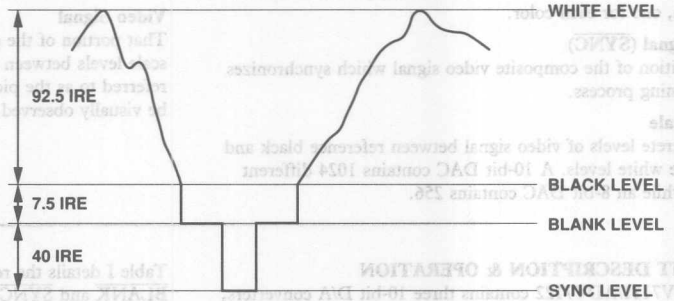
If we therefore have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate and a retrace factor of 0.8, then:

Dot Rate = 1024 × 1024 × 60/0.8
= 78.6 MHz

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7121/ADV7122 on the rising edge of CLOCK, as previously described in the "Digital Inputs" section. It is recommended that the CLOCK input to the ADV7121/ADV7122 be driven by a TTL buffer (e.g., 74F244).

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0	0	7.62	0.286
		0	0



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 560Ω .
3. RS–343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. RGB Video Output Waveform

Description	IOG (mA)[1]	IOR, IOB (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	3FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to BLANK	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	00H
BLACK to BLANK	1.44	1.44	0	1	00H
BLANK LEVEL	7.62	0	1	0	xxH
SYNC LEVEL	0	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA. V_{REF} = 1.235 V, R_{SET} = 560 Ω, I_{SYNC} connected to IOG.

Table Ia. Video Output Truth Table for the ADV7122

Description	IOR, IOG, IOB (mA)[1]	DAC Input Data
WHITE LEVEL	17.62	3FF
VIDEO	video	data
VIDEO to BLACK	video	data
BLACK LEVEL	0	00H

NOTE
[1]Typical with full-scale = 17.62 mA. V_{REF} = 1.235 V, R_{SET} = 560 Ω.

Table Ib. Video Output Truth Table for the ADV7121

Video Synchronization & Control

The ADV7122 has a single composite sync ($\overline{SYNC}$) input control. Many graphics processors and CRT controllers have the ability of generating horizontal sync (HSYNC), vertical sync (VSYNC) and composite $\overline{SYNC}$.

In a graphics system which does not automatically generate a composite $\overline{SYNC}$ signal, the inclusion of some additional logic circuitry will enable the generation of a composite $\overline{SYNC}$ signal.

The sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the ADV7122, the $\overline{SYNC}$ input should be tied to logic low.

Reference Input

An external 1.23 V voltage reference is required to drive the ADV7121/ADV7122. The AD589 from Analog Devices is an ideal choice of reference. It is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23 V output voltage for input currents between 50 μA and 5 mA. Figure 4 shows a typical reference circuit connection diagram. The voltage reference gets its current drive from the ADV7121/ADV7122's V_{AA} through an on-board 1 kΩ resistor to the V_{REF} pin. A 0.1 μF ceramic capacitor is required between the COMP pin and V_{AA}. This is necessary so as to provide compensation for the internal reference amplifier.

A resistance R_{SET} connected between FS ADJUST and GND determines the amplitude of the output video level according to Equations 1 and 2 for the ADV7122 and Equation 3 for the ADV7121:

$$IOG^{*}\ (mA) = 12{,}082 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots\ldots\ldots (1)$$

$$IOR,\ IOB\ (mA) = 8{,}628 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots\ldots (2)$$

$$IOR,\ IOG,\ IOB\ (mA) = 7{,}969 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots (3)$$

**Only applies to the ADV7122 when $\overline{SYNC}$ is being used. If $\overline{SYNC}$ is not being encoded onto the green channel, then Equation 1 will be similar to Equation 2.*

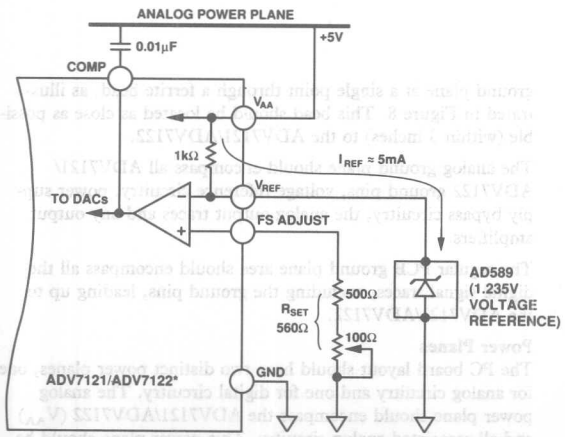


Figure 4. Reference Circuit

Using a variable value of R_{SET}, as shown in Figure 4, allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels as quoted in the specification page. These values typically correspond to the RS-343A video waveform values as shown in Figure 3.

D/A Converters

The ADV7121/ADV7122 contains three matched 10-bit D/A converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. As all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Outputs

The ADV7121/ADV7122 has three analog outputs, corresponding to the red, green and blue video signals.

The red, green and blue analog outputs of the ADV7121/ADV7122 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 5a shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor.

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 5b. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

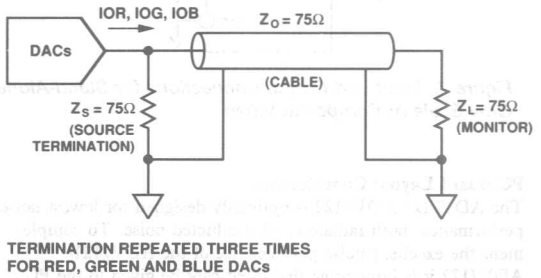


Figure 5a. Analog Output Termination for RS-343A

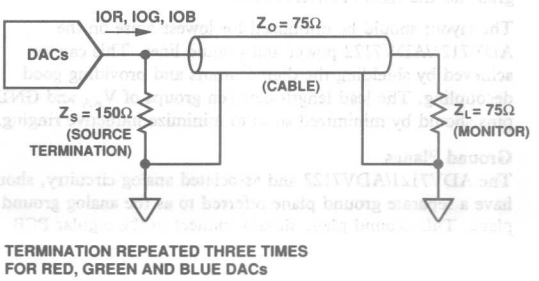


Figure 5b. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an Application Note entitled "Video Formats & Required Load Terminations" available from Analog Devices, publication no. E1228–15–1/89.

Figure 3 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75 Ω load of Figure 5a. As well as the gray scale levels, Black Level to White Level, the diagram also shows the contributions of $\overline{SYNC}$ and $\overline{BLANK}$ for the ADV7122. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table Ia details how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

Gray Scale Operation

The ADV7121/ADV7122 can be used for stand-alone, gray scale (monochrome) or composite video applications (i.e., only one channel used for video information). Any one of the three channels, RED, GREEN or BLUE can be used to input the digital video data. The two unused video data channels should be tied to logical zero. The unused analog outputs should be terminated with the same load as that for the used channel. In other words, if the red channel is used and IOR is terminated with a doubly-terminated 75 Ω load (37.5 Ω), IOB and IOG should be terminated with 37.5 Ω resistors. See Figure 6.

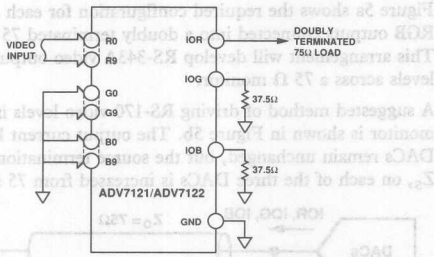


Figure 6. Input and Output Connections for Stand-Alone Gray Scale or Composite Video

Video Output Buffers

The ADV7121/ADV7122 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are described in the Analog Interface section and illustrated in Figure 5. However, in some applications it may be required to drive long "transmission line" cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between 2 and 4 will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

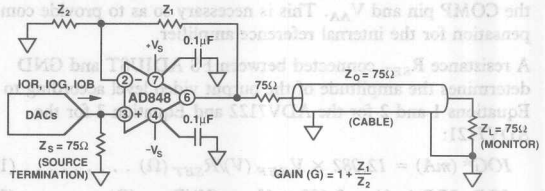


Figure 7. AD848 As an Output Buffer

PC Board Layout Considerations

The ADV7121/ADV7122 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7121/ADV7122 it is imperative that great care be given to the PC board layout. Figure 8 shows a recommended connection diagram for the ADV7121/ADV7122.

The layout should be optimized for lowest noise on the ADV7121/ADV7122 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ADV7121/ADV7122 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located as close as possible (within 3 inches) to the ADV7121/ADV7122.

The analog ground plane should encompass all ADV7121/ADV7122 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7121/ADV7122.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7121/ADV7122 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located within three inches of the ADV7121/ADV7122.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7121/ADV7122 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 8).

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV7121/ADV7122 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

The digital signal lines to the ADV7121/ADV7122 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7121/ADV7122 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

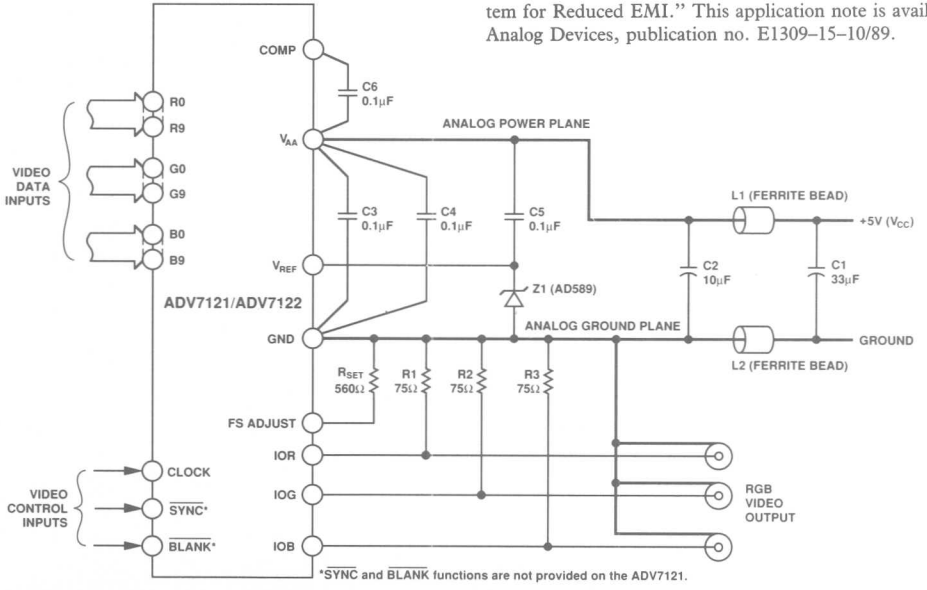
Analog Signal Interconnect

The ADV7121/ADV7122 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7121/ADV7122 so as to minimize reflections.

Additional information on PCB design is available in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, publication no. E1309–15–10/89.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33μF TANTALUM CAPACITOR	
C2	10μF TANTALUM	
C3, C4, C5,C6	0.1μF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 274300111 OR MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTER	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 8. ADV7121/ADV7122 Typical Connection Diagram and Component List

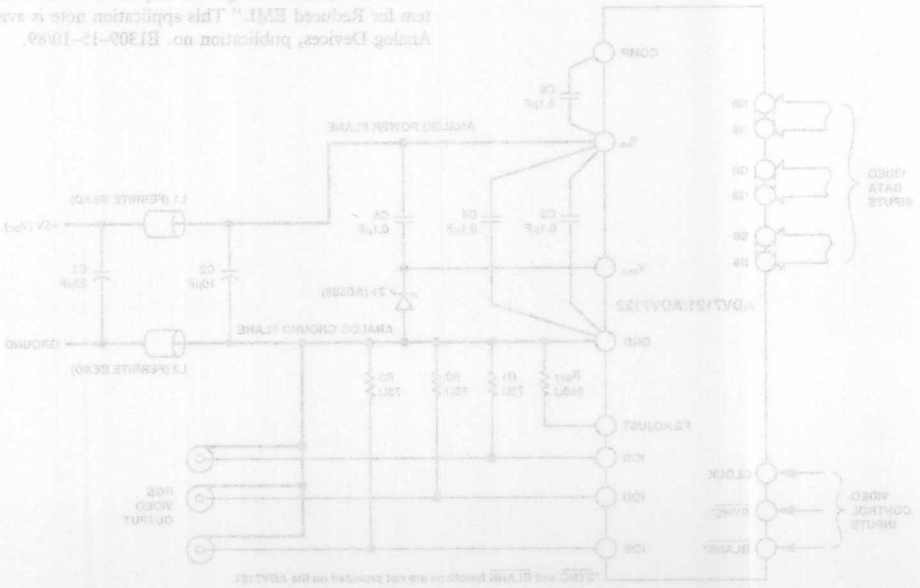


Figure 8. ADV7121/ADV7122 Typical Connection Diagram and Component List

CMOS Continuous Edge Graphics RAM-DACs (CEG/DACs)

ADV7141/ADV7146/ADV7148*

FEATURES

Proprietary Antialiasing Function
Dejagging of Lines, Arcs, Circles, Fonts, etc.
Effective 24-Bit True Color Performance
Dynamic Palette Load (DPL) Function
Plug-in Upgrade for Standard VGA RAM-DACs
ADV478/ADV471, ADV476 (ADV®) & Inmos 171/176†
Fully PS/2†, VGA† and 8514/A† Compatible
66 MHz Pipelined Operation
Triple 8-Bit/6-Bit D/A Converters
256 × 24 (18) Color Palette RAM
On-Board Gamma-Correction
On-Board Antisparkle Circuit
RS-343A/RS-170 Compatible Outputs
External Voltage or Current Reference
Standard MPU Interface
+5 V CMOS Monolithic Construction

APPLICATIONS

High Resolution Color Graphics
True Color Graphics
Digital Typography (Smooth Fonts)
Scientific Visualization
3-D Solids Modeling
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

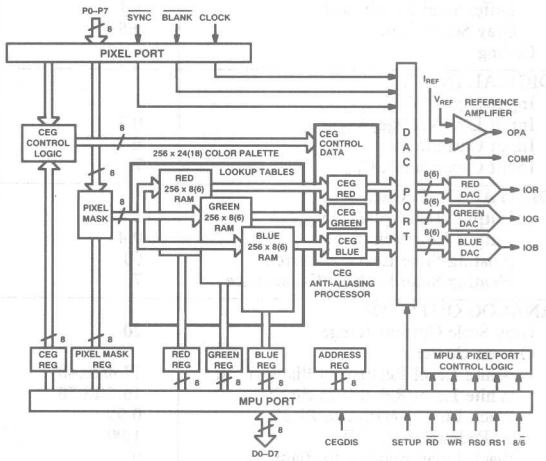
66 MHz
50 MHz
35 MHz

GENERAL DESCRIPTION

The Analog Devices' Continuous Edge Graphics† RAM-DAC (CEG†/DAC) dramatically improves image quality of standard analog color systems, by eliminating the jagged edges of computer generated images (antialiasing) and by providing an extended color palette for 3D modeling. This increased performance is achieved while at the same time maintaining full pin and functional compatibility with existing video RAM-DACs and color palettes used in VGA graphics systems.

The CEG/DAC implements a proprietary antialiasing or "dejagging" function. This is used to smooth the jagged edges associated with lines, circles and other nonrectangular objects displayed on a regular CRT screen. The part also allows for the effective display of 24-bit true color images on a standard 8-bit system, without the requirement of increased memory. More than 740,000 colors can be simultaneously displayed on an 8-bit/pixel system as against the 256 colors normally associated with 8-bit/pixel systems. This is achieved by a combination of the antialiasing function and a unique dynamic palette load

FUNCTIONAL BLOCK DIAGRAM



(DPL) feature. DPL allows for color palette writes (color alterations) during a single frame image.

The CEG/DAC combines a color lookup table (CLUT), three matched video speed computational units and associated control logic as well as three digital-to-analog converters (DACs). These all combine to significantly enhance the video image display quality of standard 8-bit/pixel graphics systems.

The ADV7148 and ADV7141 are pin and functional compatible with the ADV478 and ADV471, with the exception that the ADV7148 and the ADV7141 do not contain the overlay palette. The ADV7146 is pin and functional compatible with the ADV476 and the Inmos IMSG171/176.

CEG requires two closely connected components—the CEG/DAC chip and the software driver. Conventional antialiasing schemes are implemented entirely in software and operate on the pixel data in the graphics pipeline, resulting in a significant speed performance penalty. In contrast, the CEG software driver takes application software information and encodes the frame buffer with a sequence of data and commands for the CEG/DAC. The CEG/DAC hardware performs all of the antialiasing calculations. In this way, the visual benefits of antialiased graphics are provided with a minimal increase in software overhead.

*Protected by U.S. Patent Nos. 4,482,893 and 4,704,605.
†Inmos is a trademark of Inmos Ltd.
Personal System/2, VGA and 8514/A are trademarks of International Business Machines Corp.
Edsun Continuous Edge Graphics and CEG are registered trademarks of Edsun Laboratories, Inc.
ADV is a registered trademark of Analog Devices, Inc.

STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity[3]	±1 (±1/2)	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	μA max	
Floating-State Leakage Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank/Black	17.4/20.40	mA min/mA max	Typically 19.05 mA
White Level Relative to Black[4]	16.5/18.50	mA min/mA max	Typically 17.62 mA, SETUP = V_{AA}
Black Level Relative to Blank[4]	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5 μA, SETUP = GND
(Pedestal = 0 IRE)	50	μA max	
Blank Level[4]	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	mA max	
Blank Level	0	μA min	Typically 5 μA
(Sync Disabled)	50	μA max	
Sync Level[4]	0	μA min	Typically 5 μA
	50	μA max	
LSB size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	0/+1.5	V min/V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	
VOLTAGE REFERENCE			ADV7148 & ADV7141 Only
Voltage Reference Range	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	
CURRENT REFERENCE			ADV7146 Only
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} − 3/V_{CC}	V min/max	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	66 MHz Parts
	4.50/5.50	V min/V max	50 & 35 MHz Parts
Supply Current, I_{AA}	350	mA max	Typically 200 mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[5, 6]	−30	dB typ	
Glitch Impulse[5, 6]	75	pV secs typ	
DAC to DAC Crosstalk[7]	−23	dB typ	

NOTES
[1]±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C.
[3]Tested to 8-bit linearity (tested to 6-bit linearity, ADV7146 only).
[4]ADV7141 and ADV7148 only.
[5]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[6]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured at the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[7]DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = 5 V; SETUP = 0/6 = V_{AA}; V_{REF} = 1.235 V (ADV7140/ADV7141); I_{REF} = −8.36 mA (ADV7140); R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All Specifications T_{min} to T_{max}[3] unless otherwise noted.)

Parameter	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0–RS1 Setup Time
t_2	10	10	15	ns min	RS0–RS1 Hold Time
t_3[4]	2	2	2	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	ns min	Read Data Hold Time
t_7	10	10	15	ns min	Write Data Setup Time
t_8	15	15	15	ns min	Write Data Hold Time
t_9	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	4	ns min	Pixel & Control Setup Time
t_{12}	3	3	4	ns min	Pixel & Control Hold Time
t_{13}	15	20	28	ns min	Clock Cycle Time
t_{14}	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	20	28	ns max	Analog Output Settling Time
t_{SK}	2	2	2	ns max	Analog Output Skew
t_{PD}					Pipeline Delay
Compatibility Mode	3 × t_{13}	3 × t_{13}	3 × t_{13}	ns min	
CEG Mode	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts; t_{15} measured at V_{AA} = 5 V for 66 MHz parts.
[3]Temperature Range (T_{min} to T_{max}): 0 to +70°C.
[4]t_3 and t_4 are measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.4 V or 2.4 V.
[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.
[6]Settling time does not include clock and data feedthrough.
Specifications subject to change without notice.

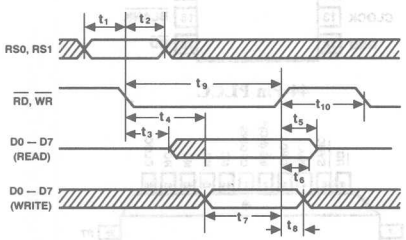


Figure 1. MPU Read/Write Timing

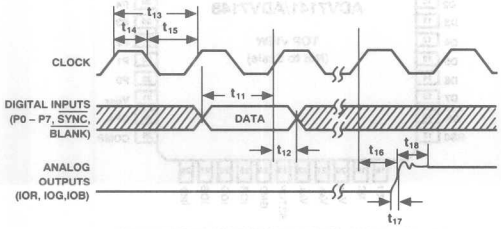


Figure 2. Video Input/Output Timing

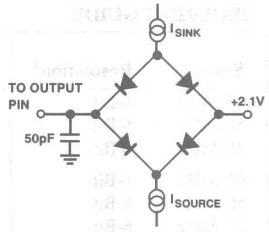


Figure 3. Load Circuit for Bus Access and Relinquish Time

NOTES
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANITION.
2. SETTLING TIME MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1 LSB.
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY	V_{AA}				
66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
AMBIENT OPERATING TEMPERATURE	T_A	0		+70	°C
OUTPUT LOAD	R_L		37.5		Ω
VOLTAGE REFERENCE CONFIGURATION					
Voltage Reference	V_{REF}	1.14	1.235	1.26	Volts
CURRENT REFERENCE CONFIGURATION					
I_{REF} CURRENT	I_{REF}				
STANDARD RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ABSOLUTE MAXIMUM RATINGS

V_{AA} to GND . . . . . −0.5 V to +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −45°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[1] . . . . . 0 V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

Model[1]	Speed	Resolution[2]	Package Option[3, 4]
ADV7146KN66	66 MHz	6-Bit	N-28
ADV7146KN50	50 MHz	6-Bit	N-28
ADV7146KN35	35 MHz	6-Bit	N-28
ADV7141KP66	66 MHz	6-Bit	P-44A
ADV7141KP50	50 MHz	6-Bit	P-44A
ADV7141KP35	35 MHz	6-Bit	P-44A
ADV7148KP66	66 MHz	8-Bit/6-Bit	P-44A
ADV7148KP50	50 MHz	8-Bit/6-Bit	P-44A
ADV7148KP35	35 MHz	8-Bit/6-Bit	P-44A

NOTES

[1]All devices are specified for 0°C to +70°C operation.

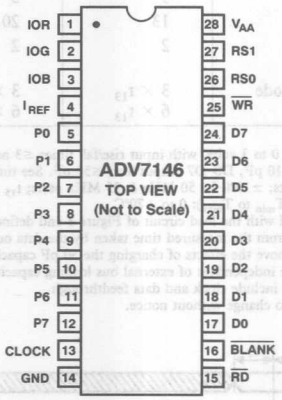
[2]Refers to "Compatibility Mode." In "CEG Mode," resolution for all options is 8 bits.

[3]28-pin DIP devices are packaged in 28-pin 0.6" plastic dual-in-line packages. 44-pin PLCC devices are packaged in 44-pin plastic leaded (J-lead) chip carriers.

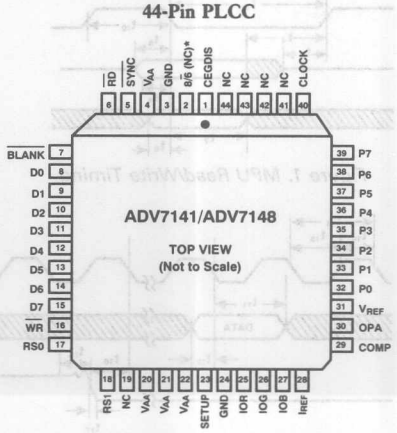
[4]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN CONFIGURATIONS

28-Pin DIP



44-Pin PLCC



NC = NO CONNECT; THESE PINS MAY BE LEFT UNCONNECTED
* (NC) INDICATES THE ADV7141 ONLY

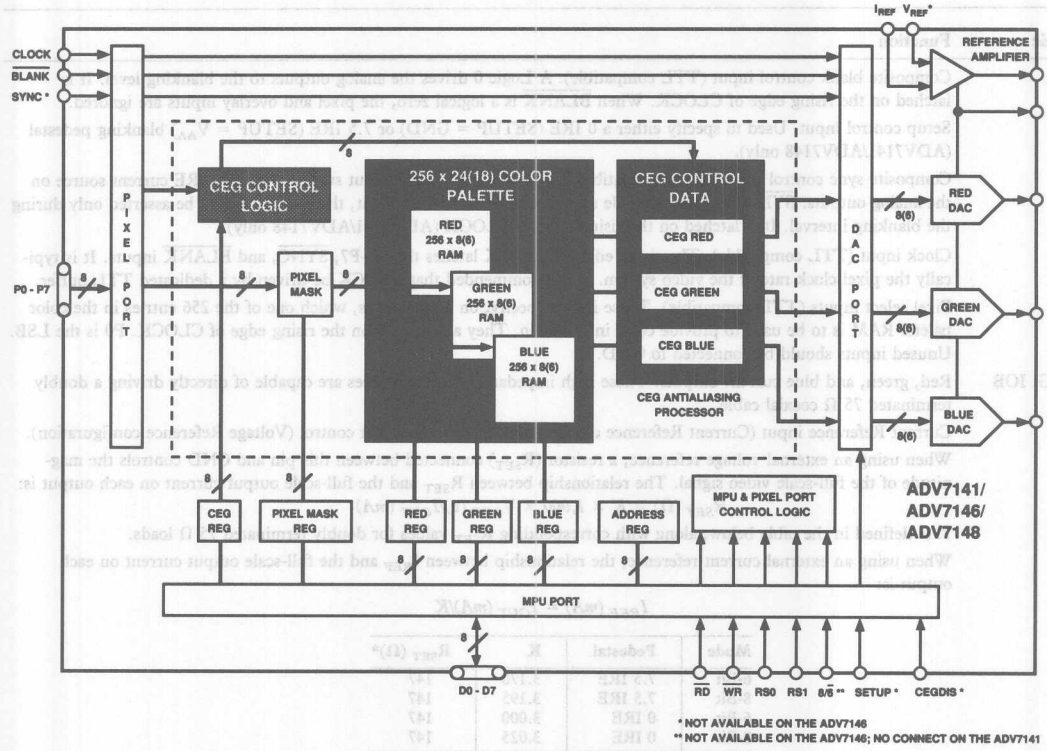
PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A Logic 0 drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal (ADV7141/ADV7148 only).
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK (ADV7141/ADV7148 only).
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	Current Reference input (Current Reference configuration)/Full-scale adjust control (Voltage Reference configuration). When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $$R_{SET}\,(\Omega) = K \times 1{,}000 \times V_{REF}\,(v)/I_{OUT}\,(mA)$$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75 Ω loads. When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is: $$I_{REF}\,(mA) = I_{OUT}\,(mA)/K$$

Mode	Pedestal	K	R_{SET} (Ω)*
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

*For PS/2 applications (i.e., 0.7 V into 50 Ω with no SYNC), a 182 Ω R_{SET} resistor is recommended.

COMP	Compensation pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA} (ADV7141/ADV7148 *only*).
V_{REF}	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.2 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA} (ADV7141/ADV7148 *only*).
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating (ADV7141/ADV7148 *only*).
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0–RS1 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations.
$\overline{\text{RD}}$	Read control input (TTL compatible). To read data from the device, $\overline{\text{RD}}$ must be a logical zero. RS0–RS1 are latched on the falling edge of $\overline{\text{RD}}$ during MPU read operations.
RS0, RS1	Register select inputs (TTL compatible). RS0–RS1 specify the type of read or write operation being performed.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This input specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant bit (MSB) while for 6-bit operation, D5 is the MSB. D6 and D7 are ignored during 6-bit operation. All parts operate in 8-bit format while in CEG mode. 6-Bit operation is the default VGA mode on the ADV7146 and ADV7141. The 8/$\overline{6}$ bit must be set to Logical 0 on the ADV7148 to make it VGA compatible. If left unconnected, this pin remains in a low state.
CEGDIS	CEG disable (TTL compatible). Driving this pin active high disables all CEG functions. Software will detect a non-CEG device if this pin is high (ADV7141/ADV7148 only). If left unconnected, this pin remains in a low state.



Functional Block Diagram of CEG/DAC

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite Sync Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

Sync Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

ANTIALIASING

Antialiasing is a technique used to smooth the jagged edges associated with lines, circles, and other nonrectangular objects represented on a CRT screen. Without antialiasing, each pixel (picture element) on a CRT is either "on" or "off." If the edge of a smooth shape passes through a pixel, the software is forced to approximate the edge as best it can (i.e., the pixel is "on" if more than half of the pixel is covered by the object). Even when a large number of pixels are used to represent an object, the eye quickly detects the series of "on" and "off" dots along the picture edge.

CEG achieves antialiasing by allowing the software to choose not only the discrete palette colors, but also a linear mix of those colors. For example, if only 1/3 of the pixel is covered by an object, the pixel would be displayed in the ratio of 33:67 between the object color and the background color. The eye perceives the new boundary as a completely smooth edge. The software driver defines the value of every pixel on a shape boundary, thereby dramatically increasing the perceived resolution of any computer display. By mixing colors in real time, the CEG/DAC can generate up to 800,000 simultaneously displayable colors without altering the contents of the standard 256 color look-up-table.

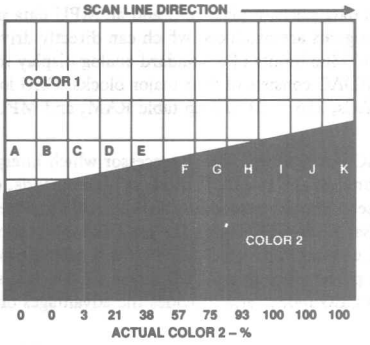


Figure 4. An Edge Crossing Scan Line

Figure 4 shows an enlargement of an object edge, with each square representing a screen pixel. An object is drawn in Color 2 on a background of Color 1—the actual colors are determined by the contents of the CLUT.

Without CEG, pixels labelled "A" through "E" will be displayed as Color 1 (Figure 5). Pixels are defined as Color 2 when more than 50% of the pixel is defined by that color, as shown in pixels "F" through "J." CEG blends colors to more closely approximate the intended color boundary as shown in Figure 6.

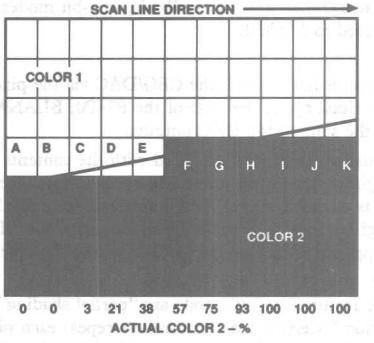


Figure 5. Traditional Pixel Coverage (Aliasing)

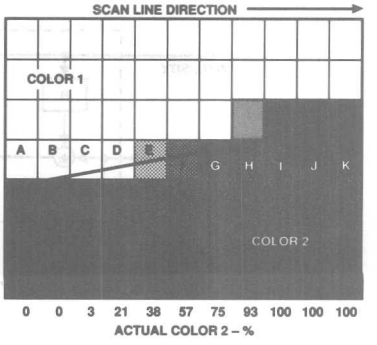


Figure 6. Dejagging or Antialiasing Using CEG

CEG FUNCTIONAL DESCRIPTION

CEG uses two data ports, a pixel port and an MPU data port. Three analog signals are produced which can directly drive the red, green, and blue inputs of a standard analog display monitor. The CEG/DAC consists of four major blocks: CEG logic, three 8-bit DACs, 256 × 24 lookup table RAM, and MPU control.

The CEG/DAC is a real-time signal processor which interprets data in the frame buffer as either colors, mix commands, or both. CEG uses a special sequence of lookup table accesses to enable and disable the CEG logic. The nonCEG mode allows full backward compatibility with current video palette products. The circuit is powered-up in nonCEG mode. CEG-aware software activates CEG modes and provides the advantages of alias-free images.

In nonCEG systems and software applications, the CEG/DAC behaves identical to normal palette DACs, providing complete physical and functional compatibility with all VGA compatible PCs. The CEG/DAC is available in packages compatible with the most popular palette DACs, including ADV471, ADV476, and ADV478 devices.

MPU Data Port

The MPU data port allows the system processor to access the color palette address register, color palette RAM and pixel mask register. Register selection is identical to the associated non-CEG, VGA compatible parts.

If the CEG device is operating in 8-bit mode, all 8 bits of the lookup table color data register are significant. In 6-bit modes, lookup table color data should be written and read back right-justified to/from D5–D0. During readback, in 6-bit modes, D6 and D7 are forced to Logic 0.

Pixel Port

Pixel information is latched into the CEG/DAC via the pixel port. For each clock cycle, the state of the P7–P0, BLANK and SYNC define the state of the DAC outputs.

Pixel port inputs are logically "AND"ed with the contents of the pixel mask register, for simple animation applications. The pixel mask register is accessed via the MPU interface. In general, the pixel mask register should be set to FFH for any of the CEG modes. See Appendix A for sample code to access the pixel mask register.

Two selectable features in CEG mode are "partial shading" and "pixel replication." Certain video controllers repeat each pixel twice in low resolution modes. In these modes, the pixel data is sampled every other CLOCK.

Systems which use only 4 bits per pixel should be connected to P3–P0, tying P7–P4 to ground. This type of system must use the "partial shading" Advanced-4 Method, which allows 8 colors (0–7) and 8 mix commands (8–15) in increments of 12%.

CEG PROGRAMMING BASICS

CEG Computation

When CEG is active, the CEG/DAC computes a real time weighted average on each of the primary colors which are read out of the palette RAM. This calculation, as represented by the generalized diagram of Figure 7, is expressed by the following equation:

$$P_{MC} = [(Color\ B \times Mix) + (Color\ A \times (31 - Mix) + 16)]\ 131$$

where: P_{MC} = mixed color.

Or alternatively, it can be described by:

Mixed color = (ratio of previous color × previous color) + (ratio of new color × new color)

The mixed colors, one mixed color each for red, green and blue are then input to a gamma correction circuit. The output of this circuit drive each of the three RGB-DACs.

CEG MODES

Although there is one algorithm in the CEG/DAC, there are three ways of encoding the pixels in the frame buffer, namely, the Basic-8, Advanced-4 and Advanced-8 methods. These are described as follows:

Basic-8 16 drawing colors with 8 mixes plus explicit loading of new or old color (suitable for CAD type applications where few colors are needed).

Advanced-4 8 drawing colors with 8-mix shading (suitable for antialiasing in 4-bits/pixel systems).

Advanced-8 223 drawing colors with full 32-mix shading (suitable for 3-D solid modeling and true-color image rendition).

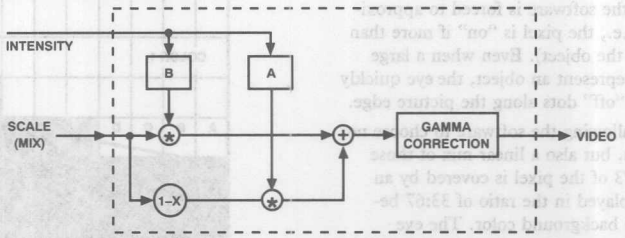


Figure 7. Block Diagram Representation of the CEG Algorithm

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV7141/ADV7146/ADV7148 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM, pixel mask register and address register.

The RS0–RS1 select inputs specify whether the MPU is accessing the address register, color palette RAM, or pixel mask register, as illustrated in Table I. The 8-bit address register is used to address the color palette RAM.

Table I. Control Input Truth Table

RS1	RS0	Addressed by MPU
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

To write color data, the MPU writes the address register with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue). During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for VGA backward compatible data). This color value is then written to the location in the palette RAM pointed to by the address register. The address register then increments and points to the next palette RAM location which the MPU may modify by simply writing another sequence of red, green and blue data. See Appendix A for sample code to write to the palette.

To read color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data. See Appendix A for sample code to read from the palette.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH.

For 8-bit operation, D0 is the LSB, and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

See Compatibility section for details of 6/8-bit operation.

Table II. Address Register (ADDR) Operation

	Value	RS1	RS0	Addressed by MPU
ADDRa, b				
Counts Modulo 3	00			Red Value
	01			Green Value
	10			Blue Value
ADDR0–7				
Counts Binary	00H–FFH	0	1	Color Palette RAM

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0–7), incremented following a blue read or write cycle, are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

Frame Buffer Interface

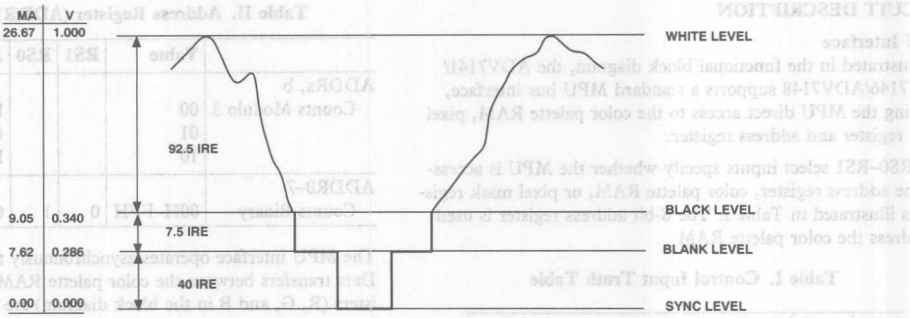
The P0–P7 inputs are used to address the color palette RAM, as shown in Table III.

Table III. Pixel Input Truth Table (Pixel Read Mask Register = FFH)

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
.	.
FFH	Color Palette RAM Location FFH

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits in compatibility mode) of color information to the three D/A converters.

(See Application Note entitled "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs" available from Analog Devices, Publication No. E1316-15-10/89.)



NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 8. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = V_{AA})

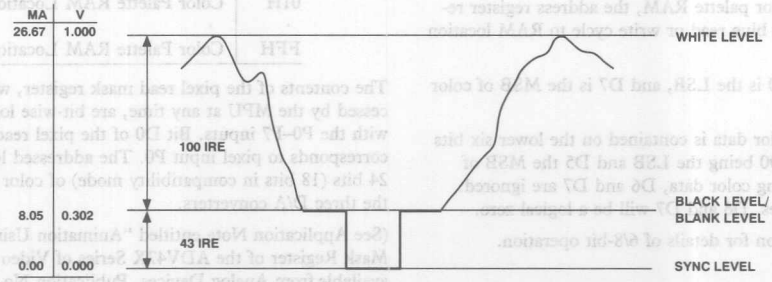
Table IV. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data + 9.05	1	1	Data
DATA-SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	xxH
SYNC	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 8, 9 and 10. Tables IV, V and VI detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input, on the ADV7141 and ADV7148, is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.



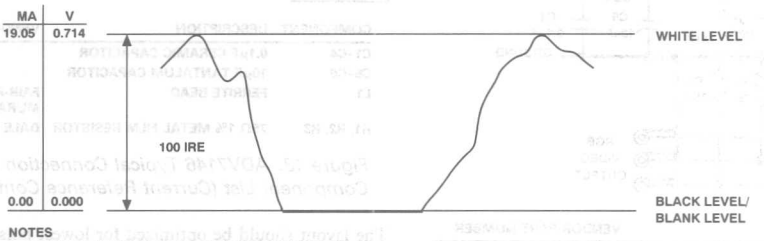
NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 9. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = GND)

Table V. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data + 8.05	1	1	Data
DATA-SYNC	Data	0	1	Data
BLACK	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	8.05	1	0	xxH
SYNC	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.



NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL CURRENT REFERENCE ADJUSTED FOR 19.05 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

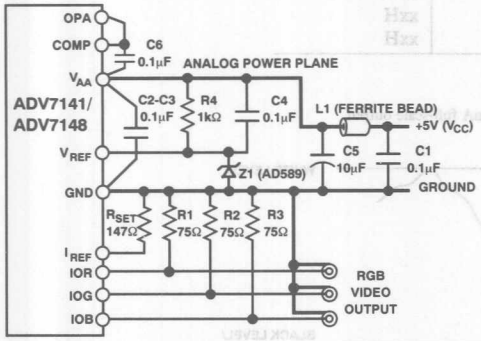
Figure 10. ADV7146 RGB Video Output Waveform

Table VI. ADV7146 RGB Video Output Truth Table

Description	I_{OUT} (mA)[1]	$\overline{BLANK}$	DAC Input Data
WHITE Level	19.05	1	FFH
VIDEO	Video	1	Data
BLACK Level	0	1	00H
BLANK Level	0	0	xxH

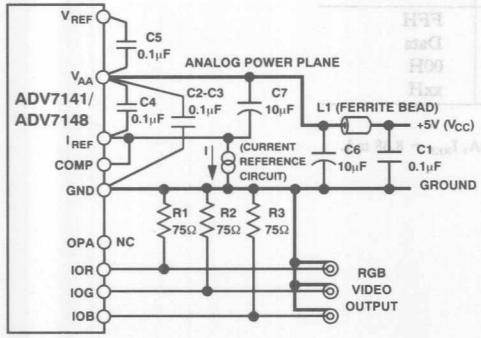
NOTE
[1]Typical with full-scale IOR, IOG, IOB = 19.05 mA, I_{REF} = 8.88 mA.

mally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of these parts, it is imperative that great care be given to the PC board layout. Figures 11, 12 and 13 show recommended connection diagrams for the ADV7141/ADV7148 in voltage reference and current reference modes and the ADV7146.



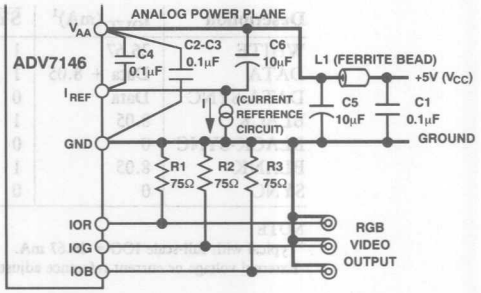
COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	147Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 11. ADV7148/ADV7141 Typical Connection Diagram and Component List (Voltage Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6–C7	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 12. ADV7148/ADV7141 Typical Connection Diagram and Component List (Current Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1µF CERAMIC CAPACITOR	
C5–C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 13. ADV7146 Typical Connection Diagram and Component List (Current Reference Configuration)

The layout should be optimized for lowest noise on the CEG/DAC power and ground lines. This is achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all the CEG/DAC ground pins, current/voltage reference circuitry, power supply bypass circuitry, the analog output traces, any output amplifiers and all the digital signal traces leading up to the CEG/DAC.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one digital circuitry. The analog power plane should encompass all the CEG/DAC power pins and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 11, 12 and 13. This bead should be located within three inches of the part.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all the CEG/DACs power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors.

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} (ADV7141/AD7148) should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the CEG/DAC contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the CEG/DAC should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the CEG/DAC should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The CEG/DAC should be located as close as possible to the output connectors thus minimizing noise pick-up and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the CEG/DAC so as to minimize reflections.

Additional information on PCB design is available in an Application Note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, Publication No. E1309–15–10/89.

REGISTER LEVEL PROGRAMMING OF THE CEG/DAC

Compatibility

CEG/DACs are available in several plug-in compatible replacements for most popular palette DACs including the Analog Devices ADV471, ADV476 and ADV478, the Inmos IMSG171 and IMSG176 and the Brooktree BT471 and BT478. All are compatible with standard VGA controllers.

The CEG/DAC powers-up in compatibility mode with the CEG circuitry bypassed. CEG mode is enabled with a software key sequence of reserved palette accesses. See Appendix A for a software example of setting the CEG mode.

In compatibility mode the ADV7141 and ADV7146 always use six bits for each red, green and blue palette component. The ADV7148 uses either 6 or 8 bits, depending on the setting of the 8/$\overline{6}$ pin (see Table VII below).

Table VII. CEG/DAC Bits per Color Component

	Compatibility Mode		CEG Mode
CEG/DAC	6-Bit Colors	8-Bit Colors	8-Bit Colors
ADV7141	*		*
ADV7146	*		*
ADV7148	*	*	*

In 6-bit compatibility mode the CEG/DAC shifts color data as it writes to and reads from the palette. The microprocessor writes right justified data in bits D5 to D0 into the palette. In the palette the data is stored left justified with bits D1 and D0 set to 0. During palette read operations the data is returned to the microprocessor in bits D5 to D0 with bits D7 and D6 set to 0.

The CEG mode byte, which is written to the blue palette location 223, is also shifted when it is written, but not when read.

All eight bits of the palette data register are significant when CEG is enabled. Set the CEG mode before writing CEG 8-bit palette information to avoid the shifting operations that occur when the chip is in compatibility mode.

The Encoding Methods

The Continuous Edge Graphics Level 3 specification describes in detail the two advanced encoding methods. Table VIII lists the characteristics of each CEG encoding method.

Basic-8 encoding provides 16 colors with 8 mixes, plus explicit loading of the A or B color registers. The Basic-8 method is appropriate for applications where 8-bits per pixel are available and a moderate number of colors are required, such as CAD applications.

Table VIII. CEG Encoding Methods

Encoding Method	Bits per Pixel	Palette Colors	Mixes	CEG Colors	DPL	Notes
Basic-8	8	16 + 16	8	16 × 16 × 8 = 2048		Mixes and Colors in the Same Pixel
Advanced-4	4	8	8	8 × 8 × 7/2 = 224	Yes	Mixes and Colors in Different Pixels
Advanced-8	8	223	32	223 × 222 × 32/2 = 792,096	Yes	Mixes and Colors in Different Pixels

The two Advanced methods store colors and op codes in different pixels. The Advanced-4 encoding supports 4-bits-per-pixel graphics, making it the CEG method to use in 4-bit systems such as the standard IBM VGA. Advanced-4 provides eight palette colors and eight mixes. Advanced-8 provides 223 drawing colors with full 32-mix shading. Use the Advanced-8 encoding method when there is a requirement for many colors, such as solid model rendering and computer imaging.

In the Advanced methods, an entry in the palette can also be reserved for the DPL op code. The dynamic palette further expands the number of colors available.

Basic-8 Encoding

The Basic-8 method encodes the 16 drawing colors and eight mixes into the eight bit pixel as shown in Figure 14. Table IX below shows the mix ratios that correspond to each pixel value in the mix field.

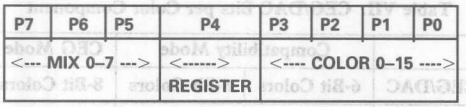


Figure 14. Pixel Encoding for Basic-8

Table IX. Basic-8 Mix Values

Mix Value	Ratio Color A	Ratio Color B
0	31/31	0/31
1	27/31	4/31
2	22/31	9/31
3	18/31	13/31
4	13/31	18/31
5	9/31	22/31
6	4/31	27/31
7	0/31	31/31

The register bit selects whether the color is placed in the A register or the B register. When the register bit is set to 0, the A register is used. When the register bit is set to 1, the B register is used. The register bit also selects which portion of the palette is accessed by the color field, because the A and B registers use different palette ranges.

The color field of the pixel data refers to the first 16 colors in the palette (Colors 0–15) when the register bit equals 0 (for the A register). When the register bit equals 1 (for the B register), the color field refers to the second 16 colors in the palette (colors 16 to 31). To find the palette location for the B register, add 16 to the color bits in P0–P3 (e.g., when the register bit = 1, color 0 refers to palette location 16). Generally, these two palette banks are loaded with the same sets of colors, but different colors can be used to increase the possible number of colors.

Advanced Encoding

In the two Advanced encoding methods, the pixel contains either a color or an op code. Mix op codes operate on the colors in the A and B registers. The companion publication, Continuous Edge Graphics Level 3, describes how the two colors are stored in the registers and how they are displayed. The Advanced-4 encoding method combines eight palette colors with eight mixes in the 4-bit pixel, providing 224 CEG colors. The 4 LSBs of the pixel value refer to either palette locations 0–7 or a mix op code as shown in Table X below.

As shown in the Figure 15, when using the Advanced-4 encoding, inputs P3–P0 contain data and inputs P7–P4 are ignored.

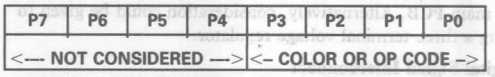


Figure 15. Pixel Encoding for Advanced-4

Table X. Advanced-4 Mix Values

Mix Value	Ratio Color A	Ratio Color B	Description
0	-	-	Palette Color 0
1	-	-	Palette Color 1
2	-	-	Palette Color 2
3	-	-	Palette Color 3
4	-	-	Palette Color 4
5	-	-	Palette Color 5
6	-	-	Palette Color 6
7	-	-	Palette Color 7 or DPL Op Code
8	31/31	0/31	Mix Op Code
9	27/31	4/31	Mix Op Code
10	22/31	9/31	Mix Op Code
11	18/31	13/31	Mix Op Code
12	13/31	18/31	Mix Op Code
13	9/31	22/31	Mix Op Code
14	4/31	27/31	Mix Op Code
15	0/31	31/31	Mix Op Code

Advanced-8 encoding uses 8-bit pixels and offers 223 palette colors with 32 mixes, resulting in 792,096 CEG colors. The eight bits of the pixel value refer to either a color in the palette or to an op code as shown in Table XI.

Table XI. Advanced-8 Mix Values

Mix Value	Ratio Color A	Ratio Color B	Description
0–190	-	-	Palette Colors
191	-	-	Palette Color or DPL Op Code
192	31/31	0/31	Mix Op Code
193	30/31	1/31	Mix Op Code
194	29/31	2/31	Mix Op Code
195	28/31	3/31	Mix Op Code
.	.	.	.
.	.	.	.
221	2/31	29/31	Mix Op Code
222	1/31	30/31	Mix Op Code
223	0/31	31/31	Mix Op Code
224–255	-	-	Palette Colors

DYNAMIC PALETTE LOADING (DPL)

The two Advanced CEG encoding methods can use dynamic palette loading, allowing the CEG/DAC to load palette colors from the bit map. With DPL enabled, an entry from the color palette is reserved as the DPL op code (7 in Advanced-4, 191 in Advanced-8). The data following this op code describes the new color to load and specifies the palette address. Note that CEG/DAC addresses are ANDed with the pixel mask register. To avoid misaddressing a DPL entry, load the mask with 255. See Mask Register for more information.

The DPL op code and data are not displayed on the screen. Instead, the color value preceding the DPL op code is repeated in place of the palette load sequence pixels. The two pixels preceding the DPL op code must be of the same kind (two colors or two mixes). For example, Color 1 Color 2 DPL is a valid sequence but Color Mix DPL is not.

DPL Examples

In the Advanced-8 encoding method, a DPL sequence requires five pixels, one for the op code, three for the new color and one for the palette address. Table XII below shows the sequence.

Table XII. DPL Op Code Sequence for Advanced-8

Pixel No.	1	2	3	4	5
Contents	DPL Op Code	New Red	New Green	New Blue	Palette Address

In 4-bits-per-pixel graphics two pixels are needed to specify one 8-bit color value. Therefore, in the Advanced-4 encoding, a DPL requires eight pixels; one for the op code, six for the new color (two each red, green and blue), and one for the palette address. Table XII shows the DPL op code sequence.

Figure 16 shows an example of a DPL op code sequence in the Advanced-4 encoding method and how the op code alters the palette and affects the display. In this example the color at palette address 2 is reassigned with the DPL. As the new color is loaded into the palette the CEG chip displays the pixel color to the left of the op code, Color 3, on the screen. After CEG loads the new color (shown as R2G2B2) at palette address 2, it is displayed whenever Color 2 is used.

Pixel Replication Compensation

Some VGA controllers repeat each pixel twice in low resolution displays (such as 320 × 200). The CEG chip, however, expects pixels in sequences and therefore it provides pixel replication compensation to undo this duplication. When pixel replication compensation is enabled, the CEG/DAC chip samples P7–P0 on every second CLOCK to ignore the repeated data (see Figure 17). Because the CEG/DAC is reversing a duplication made by the controller hardware, the compensation does not affect the graphics programmer. The bit map is written as before.

If the scan line period (video time plus $\overline{\text{BLANK}}$ time) has an even number of clock cycles, then even numbered pixels are displayed. That is, after the end of $\overline{\text{BLANK}}$, the first pixel is ignored, the second displayed, the third ignored, the fourth displayed etc. If the scan line period has an odd number of clock periods, then the first pixel after the end of $\overline{\text{BLANK}}$ is displayed, and the second is also displayed, and thereafter only even numbered pixels are displayed (the fourth, the sixth, etc.).

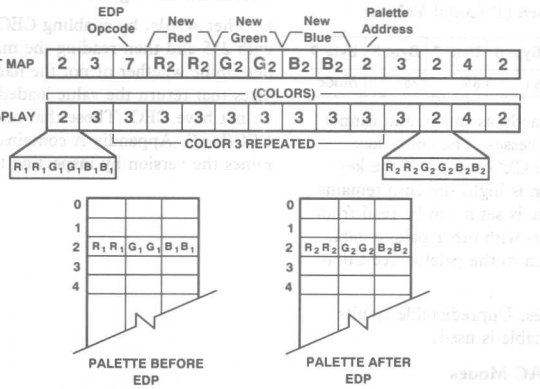


Figure 16. DPL Op Code in the Bit Map

Table XIII. DPL Op Code Sequence for Advanced-4

Pixel No.	1	2	3	4	5	6	7	8
Contents	DPL Op code	New Red	New Red	New Green	New Green	New Blue	New Blue	Palette Address
Color bits		R7–R4	R3–R0	G7–G4	G3–G0	B7–B4	B3–B0	

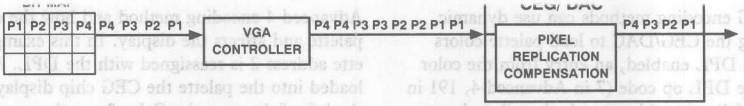


Figure 17. Pixel Replication Compensation

CEG/DAC MODES

The CEG/DAC supports a number of modes. A mode is a combination of attributes. The possible attributes are:

- CEG Encoding (Basic-8 or Advanced-4 or Advanced-8)
- Dynamic Palette Loading (DPL)
- Pixel Replication Compensation

The mode is selected under software control by a key sequence followed by a mode byte.

Enabling CEG

The CEG/DAC employs an unused sequence of palette accesses to enable the CEG logic. This long sequence was specially designed to prevent accidental mode changes. To enable the CEG/DAC the software must perform the following steps:

1. Write a palette read address (222).
2. Write three specific bytes of palette RAM data.
3. Repeat Steps 1 and 2 twice more.

There are eight bytes of special palette RAM data followed by the CEG mode byte. The mode byte determines the CEG functionality. Table XIV shows the special palette RAM data and the mode byte. The CEG/DAC Modes table shows the mode byte values. Appendix A contains sample software routines to set the VGA CEG/DAC mode.

Table XIV. CEG Key Sequence (Decimal Values)

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
67	69	71	69	68	83	85	78	Mode

The key sequence must be written exactly as shown and cannot be interrupted by any other palette accesses. The entire key sequence must be reentered to change CEG modes. If the key sequence is wrong or the CEGDIS pin is high, the chip remains in compatibility mode. After the mode is set it can be read from palette location 223 blue. Note that, as with other palette data, the mode byte is shifted as it is written to the palette (see Compatibility section).

Table XV shows the CEG/DAC modes. Unpredictable results can occur if a mode not listed in the table is used.

Table XV. CEG/DAC Modes

Mode	CEG Encoding Method	DPL	Pixel Replication
5	Basic-8		
6	Basic-8		*
9	Advanced-4		
10	Advanced-4		*
11	Advanced-4	*	
13	Advanced-8		
14	Advanced-8		*
15	Advanced-8	*	

Writing palette data to location 223 immediately disables CEG operations and returns the device to full power-up compatibility mode (there are no side effects to this and no need to clear any registers). Appendix A contains sample software that clears the CEG/DAC mode and returns the hardware to its initial power-up compatibility mode (in a VGA system).

Gamma Correction

The CEG/DAC automatically applies full gamma correction in all CEG modes. Gamma correction is required to compensate for the nonlinear relationship between the CEG/DAC outputs and the CRT display. To avoid any incompatibility, gamma correction is disabled in compatibility mode. The CEG/DAC uses a gamma value of 2.3 to perform this correction.

Identifying a CEG/DAC

Software determines whether a CEG/DAC is present by reading the mask register. Whenever a CEG mode set is selected, the four most significant bits of the mask register become write only. When read, these four MSBs do not relay the contents of the mask, but rather, give information about the CEG hardware installed.

Mask register Bit D7 is reserved and Bits D6–D4 read back the revision code of the CEG/DAC chip. The revision number always contains at least one "0" to allow software to distinguish CEG/DAC chips from other DACs. An ordinary palette DAC returns the full eight bits of the mask register.

In other words, by enabling CEG, loading the mask register with 255 and then reading the mask register, the software can determine whether or not the hardware uses a CEG/DAC. Devices that return the value loaded (those which read back 255) do not have CEG. Those that return a different value use a CEG/DAC. Appendix A contains sample software which determines the version by inspecting the mask register.

APPENDIX A. CEG SAMPLE CODE

The following code samples are available on diskette

Setting the CEG/DAC Mode

```
SET_CEG_MODE:   ; Set the CEG/DAC mode by entering a key sequence.
                ; 8086/286/386/486 assembler for a CEG/DAC in a VGA
                ; Desired MODE is passed in AL
        PUSH    DX              ; Save DX
        PUSH AX                 ; Save MODE for later
RVRT    equ     00001000b       ; Vertical retrace bit
        MOV     DX,     03DAH   ; Set to Video status port
SYNC0:  IN      AL,     DX      ; Get from Status Port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JNZ     SYNC0           ; Yes, wait until we aren't
SYNC1:  IN      AL,     DX      ; Get from status port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JZ      SYNC1           ; No, loop until we are
ENTER_KEY:
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     67      ; Write key byte 1
        OUT     DX,     AL
        MOV     AL,     69      ; Write key byte 2
        OUT     DX,     AL
        MOV     AL,     71      ; Write key byte 3
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     69      ; Write key byte 4
        OUT     DX,     AL
        MOV     AL,     68      ; Write key byte 5
        OUT     DX,     AL
        MOV     AL,     83      ; Write key byte 6
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write address in DX
        MOV     AL,     85      ; Write key byte 7
        OUT     DX,     AL
        MOV     AL,     78      ; Write key byte 8
        OUT     DX,     AL
        POP     AX              ; Retrieve desired MODE
        OUT     DX,     AL      ; Write the MODE
        POP     DX              ; Restore DX
        RET                     ; return from subroutine
```

Clearing the CEG/DAC Mode

```
CLEAR_CEG_MODE:                                  ; Clear CEG mode and return to
                                                 ; power-up compatibility mode
; 8086/286/386/486 assembler code to clear the CEG/DAC mode and
; return the hardware to its initial power-up Compatibility mode
; (in a VGA system)
;               To clear CEG mode:
;               1) Wait for the Beginning of a vertical retrace
;               2) Write to palette location 223d
                PUSH    DX                       ; Save DX
                PUSH    AX                       ; Save MODE for later
RVRT            equ     00001000b                ; Vertical retrace bit
; Trigger during vertical retrace so DPLs won't interrupt reset
                MOV     DX,     03DAH            ; Set to Video status port
SYNC0:          IN      AL,     DX               ; Get from Status Port
                TEST    AL,     RVRT             ; Are we in vertical retrace ?
                JNZ     SYNC0                    ; Yes, wait until we aren't
SYNC1:          IN      AL,     DX               ; Get from status port
                TEST    AL,     RVRT             ; Are we in vertical retrace ?
                JZ      SYNC1                    ; No, loop until we are
                                                 ; Safe to write
                MOV     DX,     03C8H
                MOV     AL,     223              ; Set write address
                OUT     DX,     AL
                MOV     DX,     03C9H
                MOV     AL,     0                ; Clear CEG mode
                OUT     DX,     AL               ; Write the byte
                POP     AX                       ; Restore AX
                POP     DX                       ; Restore DX
                RET
```

Determining the CEG/DAC Version (Reading the Mask Register)

```
GET_VERSION:                                     ; Identify CEG version number
; 8086\286\386\486 assembler code for the VGA sequence to
; determine the version by inspecting the mask register
                MOV     AL,     013DH            ; Any legal mode will do
                CALL    SET_CEG_MODE             ; Set the mode
                MOV     DX,     03C6H            ; Set DX to mask reg. address
                MOV     AL,     255              ; Write mask bits to all ones
                OUT     DX,     AL
                IN      AL,     DX               ; Read contents of mask reg
                SHR     AL,     1                ; Shift result to lowest bits
                SHR     AL,     1
                SHR     AL,     1
                SHR     AL,     1
                AND     AX,     7                ; Mask to keep only three bits
; The revision code is now in the low nibble of AL
; Valid revision codes are 0-6
; Revision code 7 indicates Non CEG compatible device
; This specification refers to chip revision 00
```

Writing the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; write to the palette
WRITE_PAL:                                  ; Write to Palette locations
                MOV   DX,   03C8h           ; Set up CEG/DAC for Write
                MOV   AL,   0               ; Will write location zero
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put data address into DX
                OUT   DX,   AL              ; Write Red Byte          Location 0
                OUT   DX,   AL              ; Write Green Byte        Location 0
                OUT   DX,   AL              ; Write Blue Byte         Location 0
; Palette Address will Auto-increment – keep writing
                OUT   DX,   AL              ; Write Red Byte          Location 1
                OUT   DX,   AL              ; Write Green Byte        Location 1
                OUT   DX,   AL              ; Write Blue Byte         Location 1
```

Reading the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; read from the palette
READ_PAL:                                   ; Read From Palette locations
                MOV   DX,   03C7h           ; Set up CEG/DAC for read
                MOV   AL,   50              ; Will read from location 50
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put Data address into DX
                IN    AL,   DX              ; Read Red Byte into AL
                IN    AH,   DX              ; Read Green Byte into AH
                IN    BL,   DX              ; Read Blue Byte into BL
; Palette Address will Auto-increment – keep reading
                IN    AL,   DX              ; Read Red Byte           Location 51
                IN    AH,   DX              ; Read Green Byte         Location 51
                IN    BL,   DX              ; Read Blue Byte          Location 51
```

Accessing the Pixel Mask Register

```
; 8086/286/386/486 assembler code for the VGA sequence to access the
; Pixel Mask Register
ACCESS_REG
                MOV   DX,   3C6h            ; Pixel Mask Register Port Address
                MOV   AL,   255             ; Write all ones to register
                OUT   DX,   AL              ;
                IN    DX,   AL              ; Read back contents of register
```

ADV7150/ADV7152

FEATURES

- 170 MHz Pipelined Operation
- Triple 10-Bit D/A Converters
- Triple 256 × 10 (256 × 30) Color Palette RAM
- On-Chip Clock Control Circuit
- Palette Priority Select Registers
- RS-343A/RS-170 Compatible Analog Outputs
- TTL Compatible Digital Inputs
- Standard MPU I/O Interface
  - 10-Bit Parallel Structure
  - 8+2 Byte Structure
- Pixel Data Serializer
  - Multiplexed Pixel Input Ports; 1:1, 2:1, 4:1 (ADV7150)
  - Multiplexed Pixel Input Ports; 1:1, 2:1 (ADV7152)
- +5 V CMOS Monolithic Construction
- 160-Pin PQFP (ADV7150)
- 100-Pin PQFP (ADV7152)

SPEED GRADES

- 170 MHz
- 135 MHz
- 110 MHz
- 85 MHz

MODES FOR ALL SPEED GRADES

- 24-Bit True Color
- Three 8-Bit Pseudo-Color Modes
  - On Red Pixel Port
  - On Green Pixel Port
  - On Blue Pixel Port
- 15-Bit True Color
  - 5 Bits Red, 5 Bits Green and 5 Bits Blue
  - 8 Bits Red and 7 Bits Green

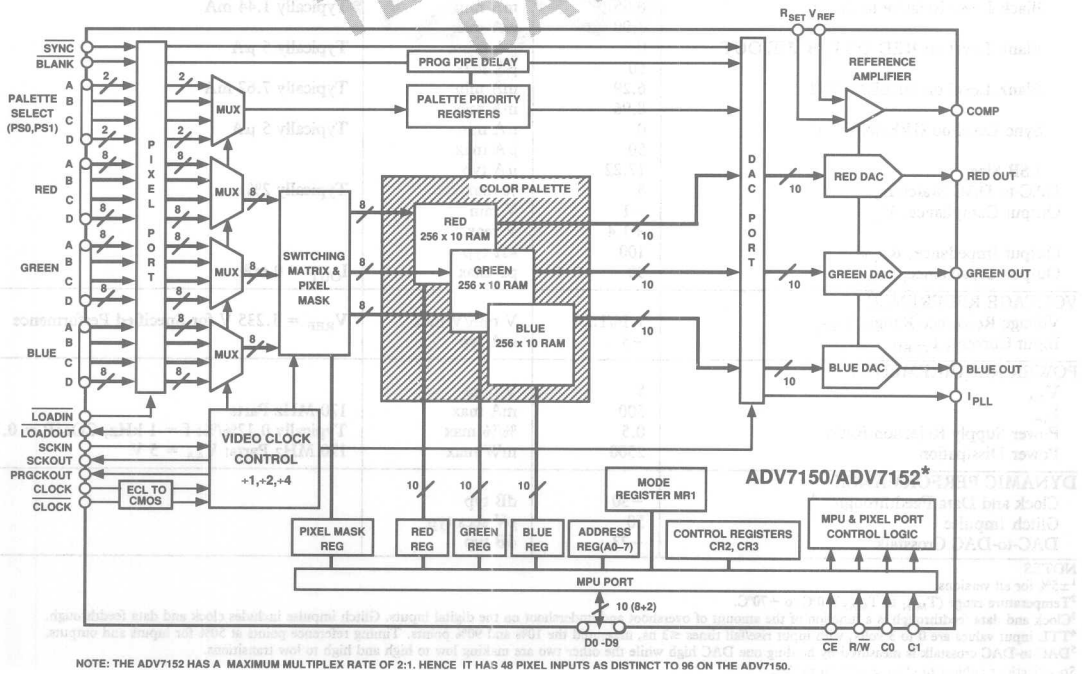
GENERAL DESCRIPTION

The ADV7150/ADV7152 (ADV®) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in the graphics systems of high performance, color graphics workstations. The ADV7150/ADV7152 integrates a number of graphic functions onto one device allowing 24-bit direct True-Color operation at the maximum screen update rate of 170 MHz. It can also be used in other modes, including 15-bit true color and 8-bit pseudo or indexed color. Either the RED, GREEN or BLUE input pixel ports can be used for pseudo color.

Continued on page 2-893

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



NOTE: THE ADV7152 HAS A MAXIMUM MULTIPLEX RATE OF 2:1. HENCE IT HAS 48 PIXEL INPUTS AS DISTINCT TO 96 ON THE ADV7150.

ADV is a registered trademark of Analog Devices, Inc.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADV7150/ADV7152—SPECIFICATIONS

(V_{AA}[1] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	10	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS (Excluding CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
CLOCK INPUTS (CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	V_{AA} − 1.0	V min	
Input Low Voltage, V_{INL}	V_{AA} − 1.6	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	20	μA max	
Floating-State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on RED OUT, BLUE OUT	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on GREEN OUT	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level on GREEN OUT	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	17.22	μA typ	
DAC-to-DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	100	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	500	mA max	170 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	2500	mW max	170 MHz Parts: V_{AA} = 5 V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−30	dB typ	
Glitch Impulse	50	pV secs typ	
DAC-to-DAC Crosstalk[5]	−23	dB typ	

NOTES
[1]±5% for all versions.
[2]Temperature range (T_{MIN} to T_{MAX}): 0°C to +70°C.
[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[4]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[5]DAC-to-DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted.)

Parameter	170 MHz Version	135 MHz Version	110 MHz Version	85 MHz Version	Units	Conditions/Comments
f_{MAX}	170	135	110	85	MHz	Clock Rate
LOADOUT						
1:1 MUX Mode						
Frequency	68	68	68	68	MHz	LOADOUT Clocking Rate
Period	14.71	14.71	14.71	14.71	ns max	LOADOUT Period
High Time	6	6	6	6	ns min	LOADOUT High Time
Low Time	6	6	6	6	ns min	LOADOUT Low Time
2:1 MUX Mode						
Frequency	68	68	55	42.5	MHz	LOADOUT Clocking Rate
Period	14.71	14.81	18.18	21.25	ns max	LOADOUT Period
High Time	6	6	8	8.5	ns min	LOADOUT High Time
Low Time	6	6	8	8.5	ns min	LOADOUT Low Time
4:1 MUX Mode						
Frequency	42.5	33.75	27.5	21.25	MHz	LOADOUT Clocking Rate
Period	23.5	30	36.4	47	ns max	LOADOUT Period
High Time	10	12	14.5	18.8	ns min	LOADOUT High Time
Low Time	10	12	14.5	18.8	ns min	LOADOUT Low Time
t_1	15	15	15	15	ns max	Pixel CLOCK to LOADOUT Delay
t_2	15	15	15	15	ns max	Pixel CLOCK to PRGCKOUT Delay
t_3	5	5	5	5	ns min	LOADIN to LOADOUT Setup Time
t_4	0	0	0	0	ns min	Video and Pixel Data Setup Time
t_5	5	5	5	5	ns min	Video and Pixel Data Hold Time
t_6	5	5	5	5	ns max	SCKIN to SCKOUT Delay
t_7	5.88	7.4	9.09	11.77	ns min	Clock Cycle Time
t_8	2.5	3	4	5	ns min	Clock Pulse Width High Time
t_9	2.5	3	4	5	ns min	Clock Pulse Width Low Time
t_{10}	12	12	12	12	ns min	Analog Output Delay
t_{11}	2	2	2	3	ns min	Analog Output Rise/Fall Time
t_{12}[4]	6	8	8	12	ns min	Analog Output Settling Time
t_{13}	0	0	0	0	ns min	R/$\overline{W}$, C0, C1 Setup Time
t_{14}	15	15	15	15	ns min	R/$\overline{W}$, C0, C1 Hold Time
t_{15}	50	50	50	50	ns min	$\overline{CE}$ Low Time
t_{16}	25	25	25	25	ns min	$\overline{CE}$ High Time
t_{17}[5]	5	5	5	5	ns min	$\overline{CE}$ Asserted to Data Bus Driven
t_{18}[5]	50	50	50	50	ns max	$\overline{CE}$ Asserted to Data Valid
t_{19}[6]	15	15	15	15	ns max	$\overline{CE}$ Disabled to Data Bus Three Stated
	5	5	5	5	ns min	
t_{20}	20	20	20	20	ns min	Write Data Setup Time
t_{21}	5	5	5	5	ns min	Write Data Hold Time
t_{SK}	2	2	2	2	ns max	Analog Output Skew
	0	0	0	0	ns typ	
t_{PD}	6	6	6	6	Clocks	Pipeline Delay

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 5.

[2]±5% for all versions.

[3]Temperature range (T_{MIN} to T_{MAX}); 0°C to + 70°C.

[4]Settling time does not include clock and data feedthrough.

[5]t_{17} and t_{18} are measured with the load circuit of Figure 1 and are defined as the time required for an output to cross 0.4 V or 2.4 V.

[6]t_{19} is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_{19}, quoted in the timing characteristics is the true value for the device and as such is independent of external bus loading capacitances.

PRELIMINARY TECHNICAL DATA

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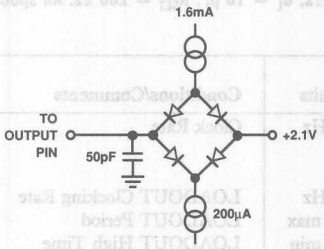


Figure 1. Load Circuit for Bus Access and Relinquish Time

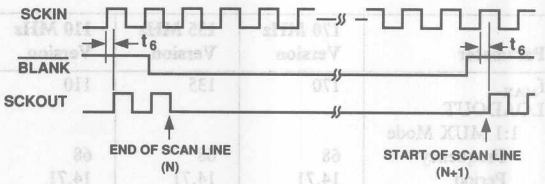


Figure 4. Video Data Serial Clock Input (SCKIN) vs. Serial Clock Output (SCKOUT)

TIMING WAVEFORMS

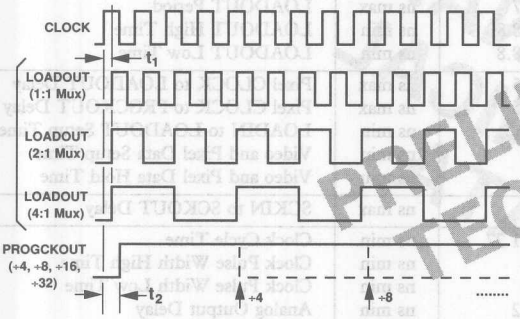
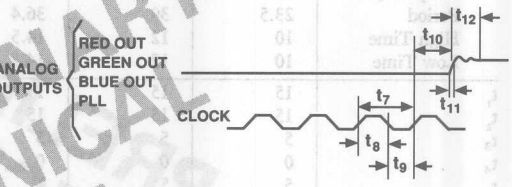
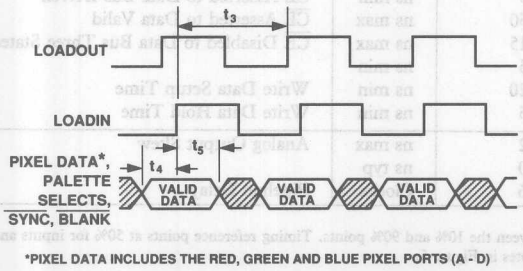


Figure 2. Video Output Clock Controls vs. Pixel Clock Input



NOTES:
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. SETTLING TIME MEASURED FROM 50% POINT OF FULL-SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB.
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.

Figure 5. Analog Outputs vs. Pixel Clock



*PIXEL DATA INCLUDES THE RED, GREEN AND BLUE PIXEL PORTS (A - D)

Figure 3. LOADOUT Timing vs. LOADIN and Pixel Data

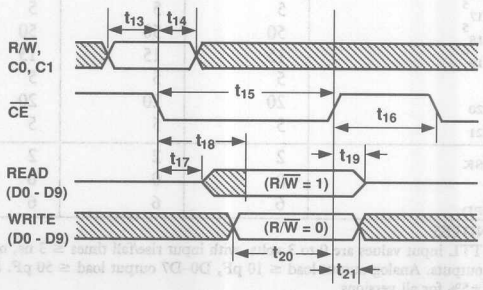


Figure 6. MPU Port Read/Write Timing

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Output Load	R_L		37.5		Ω

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on any Digital Pin . . . . . GND−0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[2] . . . . . −1.5 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

Model	Speed	Temperature Range	No. of Pins	Package Option*
ADV7150KS170	170 MHz	0°C to +70°C	160	S-160
ADV7150KS135	135 MHz	0°C to +70°C	160	S-160
ADV7150KS110	110 MHz	0°C to +70°C	160	S-160
ADV7150KS85	85 MHz	0°C to +70°C	160	S-160
ADV7152KS170	170 MHz	0°C to +70°C	100	S-100
ADV7152KS135	135 MHz	0°C to +70°C	100	S-100
ADV7152KS110	110 MHz	0°C to +70°C	100	S-100
ADV7152KS85	85 MHz	0°C to +70°C	100	S-100

*S = Plastic Quad Flatpack. For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



Continued from page 2-889

The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority registers, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The ADV7150 is capable of 1:1, 2:1 and 4:1 multiplexing while the ADV7152 implements 1:1 and 2:1 multiplexing. The on-board palette priority select registers enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled (i.e., mode selection and multiplex selection) through the MPU port by the various on-board control/command registers. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device.

The individual red, green and blue pixel input ports allow true-color, image rendition. True-color image rendition, at speeds of up to 170 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input port's flexibility allows for direct interface to most standard frame buffer memory configurations, including general purpose DRAM and VRAM designs.

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 24-bit true color resolution, while also allowing for the on-board implementation of linearization algorithms, such as gamma correction.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7150/ADV7152. The part can also be driven by an external clock generator chip circuit.

The ADV7150/ADV7152 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the user's system level debugging.

The ADV7150/ADV7152 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7150 is packaged in a 160-pin plastic quad flatpack (PQFP). The ADV7152 is packaged in a 100-pin plastic quad flatpack (PQFP).

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Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	$G3_A$	41	$PS1_D$	81	NC*	121	$R1_A$
2	$G3_B$	42	$B0_A$	82	D2	122	$R1_B$
3	$G3_C$	43	$B0_B$	83	NC*	123	$R1_C$
4	$G3_D$	44	$B0_C$	84	NC*	124	$R1_D$
5	$G4_A$	45	$B0_D$	85	GND	125	$R2_A$
6	$G4_B$	46	$B1_A$	86	GND	126	$R2_B$
7	$G4_C$	47	$B1_B$	87	D3	127	$R2_C$
8	$G4_D$	48	$B1_C$	88	D4	128	$R2_D$
9	$G5_A$	49	$B1_D$	89	D5	129	$R3_A$
10	$G5_B$	50	$B2_A$	90	V_{AA}	130	$R3_B$
11	$G5_C$	51	$B2_B$	91	D6	131	$R3_C$
12	$G5_D$	52	$B2_C$	92	D7	132	$R3_D$
13	$\overline{CLKIN}$	53	$B2_D$	93	D8	133	$R4_A$
14	CLKIN	54	$B3_A$	94	D9	134	$R4_B$
15	LOADIN	55	$B3_B$	95	GND	135	$R4_C$
16	LOADOUT	56	$B3_C$	96	GND	136	$R4_D$
17	V_{AA}	57	$B3_D$	97	GND	137	$R5_A$
18	V_{AA}	58	$B4_A$	98	$\overline{IOB}$	138	$R5_B$
19	PRGCKOUT	59	$B4_B$	99	$\overline{IOR}$	139	$R5_C$
20	SCKIN	60	$B4_C$	100	$\overline{IOG}$	140	$R5_D$
21	SCKOUT	61	$B4_D$	101	IOB	141	$R6_A$
22	GND	62	$B5_A$	102	IOG	142	$R6_B$
23	GND	63	$B5_B$	103	V_{AA}	143	$R6_C$
24	GND	64	$B5_C$	104	V_{AA}	144	$R6_D$
25	GND	65	$B5_D$	105	V_{AA}	145	$R7_A$
26	$G6_A$	66	$B6_A$	106	IOR	146	$R7_B$
27	$G6_B$	67	$B6_B$	107	COMP	147	$R7_C$
28	$G6_C$	68	$B6_C$	108	V_{REF}	148	$R7_D$
29	$G6_D$	69	$B6_D$	109	R_{SET}	149	$G0_A$
30	$G7_A$	70	$B7_A$	110	I_{PLL}	150	$G0_B$
31	$G7_B$	71	$B7_B$	111	GND	151	$G0_C$
32	$G7_C$	72	$B7_C$	112	V_{AA}	152	$G0_D$
33	$G7_D$	73	$B7_D$	113	V_{AA}	153	$G1_A$
34	$PS0_A$	74	$\overline{CE}$	114	V_{AA}	154	$G1_B$
35	$PS0_B$	75	R/$\overline{W}$	115	$\overline{SYNC}$	155	$G1_C$
36	$PS0_C$	76	C0	116	$\overline{BLANK}$	156	$G1_D$
37	$PS0_D$	77	C1	117	$R0_A$	157	$G2_A$
38	$PS1_A$	78	D0	118	$R0_B$	158	$G2_B$
39	$PS1_B$	79	D1	119	$R0_C$	159	$G2_C$
40	$PS1_C$	80	NC*	120	$R0_D$	160	$G2_D$

*NC = NO CONNECT.

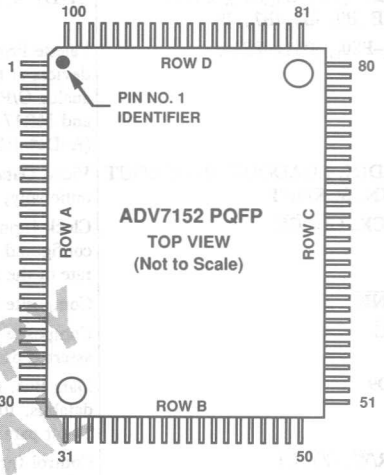
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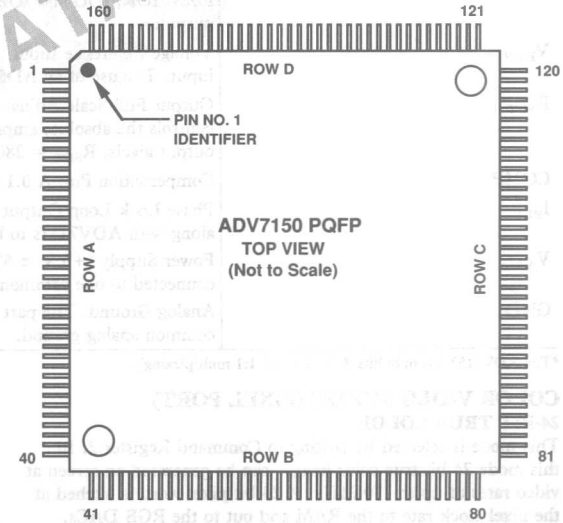
Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	$\overline{SYNC}$	41	SCKOUT	81	D5
2	$\overline{BLANK}$	42	GND	82	V_{AA}
3	$R0_A$	43	GND	83	D6
4	$R0_B$	44	GND	84	D7
5	GND	45	GND	85	D8
6	$R1_A$	46	GND	86	D9
7	$R1_B$	47	$G6_A$	87	GND
8	$R2_A$	48	$G6_B$	88	GND
9	$R2_B$	49	$G7_A$	89	$\overline{IOB}$
10	$R3_A$	50	$G7_B$	90	$\overline{IOR}$
11	$R3_B$	51	$PS0_A$	91	$\overline{IOG}$
12	$R4_A$	52	$PS0_B$	92	IOB
13	$R4_B$	53	$PS1_A$	93	IOG
14	$R5_A$	54	$PS1_B$	94	V_{AA}
15	$R5_B$	55	$B0_A$	95	I_{PLL}
16	$R6_A$	56	$B0_B$	96	IOR
17	$R6_B$	57	$B1_A$	97	COMP
18	$R7_A$	58	$B1_B$	98	V_{REF}
19	$R7_B$	59	$B2_A$	99	R_{SET}
20	$G0_A$	60	$B2_B$	100	V_{AA}
21	$G0_B$	61	$B3_A$		
22	$G1_A$	62	$B3_B$		
23	$G1_B$	63	$B4_A$		
24	$G2_A$	64	$B4_B$		
25	$G2_B$	65	$B5_A$		
26	NC*	66	$B5_B$		
27	$G3_A$	67	$B6_A$		
28	$G3_B$	68	$B6_B$		
29	$G4_A$	69	$B7_A$		
30	$G4_B$	70	$B7_B$		
31	$G5_A$	71	$\overline{CE}$		
32	$G5_B$	72	$R/\overline{W}$		
33	$\overline{CLOCK}$	73	C1		
34	CLOCK	74	C0		
35	LOADIN	75	D0		
36	LOADOUT	76	D1		
37	V_{AA}	77	D2		
38	V_{AA}	78	GND		
39	PRGCKOUT	79	D3		
40	SCKIN	80	D4		

*NC = NO CONNECT.

100-Pin PQFP



160-Pin PQFP



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PIN DESCRIPTION

Pin	Function
RED ($R0_A$–$R0_D$/$R7_A$–$R7_D$), GREEN ($G0_A$–$G0_D$/$G7_A$–$G7_D$), BLUE ($B0_A$–$B0_D$/$B7_A$–$B7_D$)	Pixel Port: 96 pixel select inputs, 8 bits for red, green and blue. Each bit is multiplexed (A–D)* 4:1, 2:1 or 1:1. All inputs are TTL compatible.
$PS0_A$–$PS0_D$, $PS1_A$–$PS1_D$	Palette Priority Select Inputs: These inputs allow for switching between multiple palette devices at the pixel rate. The device can be preprogrammed to completely shut off the DAC analog O/Ps. If the values of PS0 and PS1 match the values programmed into bits MR16 and MR17 of the Mode Register, then the device is selected. Each bit is multiplexed (A–D)* 4:1, 2:1 or 1:1. All inputs are TTL compatible.
LOADIN, LOADOUT, PRGCKOUT SCKIN, SCKOUT	Video Data Control Inputs/Outputs: These inputs/outputs are used to load pixel data and, optionally, to control external video frame buffer timing and control synchronization.
CLOCK, $\overline{\text{CLOCK}}$	Clock Inputs: These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
$\overline{\text{BLANK}}$	Composite Blank: Drives the analog outputs to the blanking level.
$\overline{\text{SYNC}}$	Composite Sync Input: Drives the IOG analog output to the sync level. It can only be asserted during the blanking period.
D0–D9	Data Bus: Data is written to and is read from the device over this 10-bit, bidirectional databus. 10-bit data or 8-bit data can be used. The databus can be configured for either 10-bit parallel data or byte data (8+2).
$\overline{\text{CE}}$, R/$\overline{\text{W}}$, CO, C1	Control Inputs: These inputs control the writing to and reading from the address reg, color palette, palette select registers, mode control registers, etc., of the device.
IOR, IOG, IOB ($\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$)	Analog Video Current Outputs (Differential Outputs): These RGB video outputs are capable of directly driving RS-343A and RS-170 video levels into doubly terminated 75 Ω loads. IOR, IOG and IOB can be tied to GND if it is not required to have differential outputs.
V_{REF}	Voltage Reference Input: An external 1.235 V voltage reference is required to drive this input. The use of an AD589 (2-terminal voltage reference) is recommended.
R_{SET}	Output Full-Scale Adjust Control: A resistor connected between this pin and analog ground controls the absolute amplitude of the output video signal. To maintain RS-343A video output levels, R_{SET} = 280 Ω.
COMP	Compensation Pin: A 0.1 μF capacitor should be connected between this pin and V_{AA}.
I_{PLL}	Phase Lock Loop Output Current: This is used to enable multiple ADV7150/ADV7152s along with ADV7151s to be synchronized with pixel resolution.
V_{AA}	Power Supply (+5 V ± 5%): The part contains multiple power supply pins; all should be connected to one common +5 V analog power supply.
GND	Analog Ground: The part contains multiple ground pins; all should be connected to one common analog ground.

*The ADV7152 has only bits A-B (2:1 and 1:1 multiplexing).

COLOR VIDEO MODES (PIXEL PORT)

24-BIT TRUE COLOR

This mode is selected by writing to Command Register 2. In this mode 24-bit true color images can be generated on screen at video rates of up to 170 MHz. A 24-bit pixel word is latched at the pixel clock rate to the RAM and out to the RGB DACs.

15-BIT TRUE COLOR

The ADV7150/ADV7152 can be programmed to run in 15-bit true-color mode. There are two 15-bit true-color modes; the first mode uses the red, green and blue pixel ports while the second mode uses only the red and green pixel ports. Command Register 2 sets the various 15-bit modes. The diagrams show the various pixel port mapping schemes for 15-bit true-color.

15-Bit True Color (Mode 1)

When this mode is set, 15 bits of video data are latched to the device over the upper five bits of each of the RED (R7–R3), GREEN (G7–G3) and BLUE (B7–B3) pixel ports (see Figure 7). The lower 3 bits are ignored. Internally this data is shifted to the lower 5 bits of the LUT decode register, therefore addressing locations 0 to 32 of the look-up table. Each of these 32 addressed locations for the red, green and blue channels can contain an 8- or 10-bit color value, which is latched to each of the three DACs.

15-Bit True Color (Mode 2)

When this mode is set, 15 bits of video data are latched to the device over all 8 bits of the RED (R7–R0) and 7 bits of the

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GREEN (G6–G0) pixel ports (see Figure 8). G7 and the data on the BLUE (B7–B0) pixel port is ignored. Internally, this data is shifted to the lower 5 bits of the red, green and blue LUT decode registers, therefore addressing locations 0 to 32 of the look-up table. Each of these 32 addressed locations for the red, green and blue channels can contain an 8- or 10-bit color value which is latched to each of the three DACs.

8-BIT PSEUDO COLOR

This mode is again selected by writing to Command Register 2. In this mode 8-bit pseudo color images can be generated on screen at video rates of up to 170 MHz. 256 colors can be displayed out of a total color palette of 16.7 million addressable colors.

This mode has three further submodes. The pixel input data can be encoded onto either the RED, GREEN or BLUE input pixel stream.

SUBMODE a: 8-bit pseudo color on RED
SUBMODE b: 8-bit pseudo color on GREEN
SUBMODE c: 8-bit pseudo color on BLUE

2

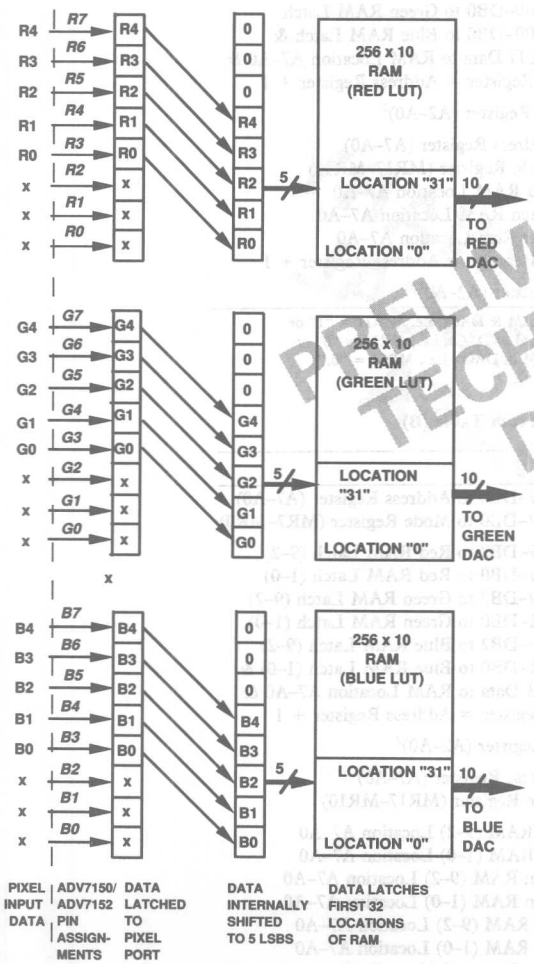


Figure 7. 15-Bit True-Color Mapping Using Red, Green and Blue Pixel Ports (Mode 1)

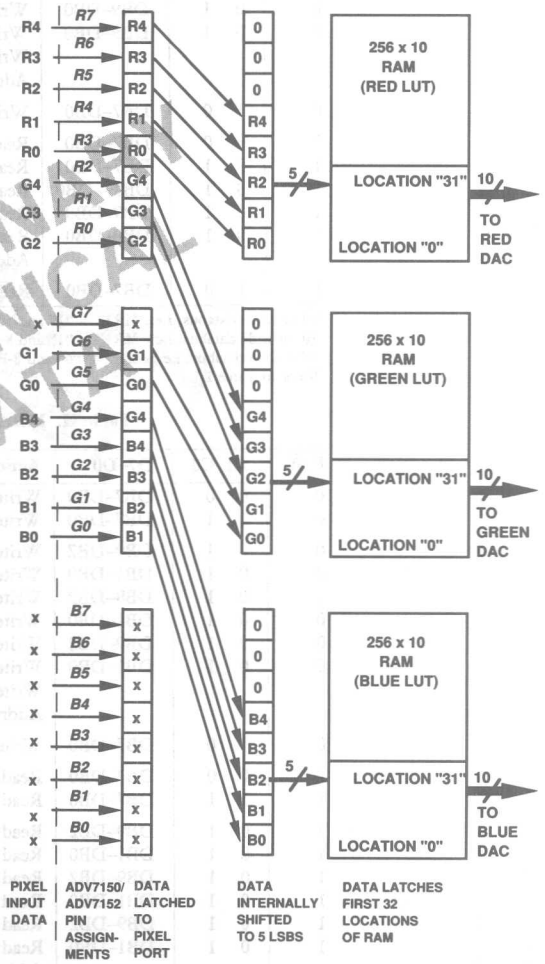


Figure 8. 15-Bit True-Color Mapping Using Red and Green Pixel Ports (Mode 2)

PRELIMINARY TECHNICAL DATA

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MPU INTERFACE & CONTROL

The ADV7150/ADV7152 supports a standard MPU Interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the address register, mode register and all the control registers as well as the color palette. The following tables describe the setup for reading and writing to all of the devices registers.

Table I. Interface Truth Table (A)

R/$\overline{W}$	C1	C0	D9–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB0	Write DB9–DB0 to Red RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Green RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Blue RAM Latch & Write RGD Data to RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9—DB0	Read Red RAM Location A7–A0
1	0	1	DB9–DB0	Read Green RAM Location A7–A0
1	0	1	DB9–DB0	Read Blue Ram Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]10-bit wide databus, i.e., MR12 = "1" and 10-bit RAM & DACs, i.e., MR11 = "1" or 10-bit wide databus, i.e., MR12 = "1" and 8-Bit RAM & DACs, i.e., MR11 = "0" or 8-bit wide databus, i.e., MR12 = "0" and 8-Bit RAM & DACs, i.e., MR11 = "0."
[2]Refer to Table III.

Table II. Interface Truth Table (B)

R/$\overline{W}$	C1	C0	D7–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB2	Write DB9–DB2 to Red RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Red RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Green RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Green RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Blue RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Blue RAM Latch (1–0) & Write RGB Data to RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9–DB2	Read Red RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Red RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Green RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Green RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Blue RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Blue RAM (1–0) Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]8-bit wide databus, i.e., MR12 = "0" and 10-Bit RAM & DACs, i.e., MR11 = "1."
[2]Refer to Table III.

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REGISTER PROGRAMMING

Direct writes and reads can be made to the address register and the mode register. The control registers, seven of which are listed in the table, are indexed addressable. The first write to the control register specifies which particular register is to be accessed.

Address Register (ADDR) A7–A0

As illustrated in the previous tables, the C0 and C1 control inputs, in conjunction with this address register, specify which control/mode register or color palette location is accessed by the MPU port. The address register is 8 bits wide and can be read from as well as written to. When writing to or reading from the color palette on a sequential basis, only the start address needs to be written. After a red, green and blue write sequence, the address register is automatically incremented.

Mode Register 1 (MR1)

The mode register is a 10-bit wide register. However, for programming purposes it may be considered as an 8-bit wide register (MR18 and MR19 are both reserved).

The diagram below shows the various operations under the control of the mode register. This register can be read from as well as written to. In read mode, MR18 and MR19 are both returned as zeros.

MODE REGISTER (MR1) BIT DESCRIPTION

Reset Control (MR10)

This bit is used to reset the pixel port sampling sequence. This ensures that the pixel sequence ABCD starts at A. It is reset by writing a 1 followed by a zero followed by a 1.

RAM-DAC Resolution Control (MR11)

When this is programmed with a 1, the RAM is 30 bits deep (10 bits each for red, green and blue), and each of the three DACs is configured for 10-bit resolution.

When MR11 is programmed with a 0, the RAM is 24 bits deep (8 bits each for red, green and blue), and the DACs are configured for 8-bit resolution. The two LSBs of the 10-bit DACs are pulled down to zero.

MPU Data Bus Width (MR12)

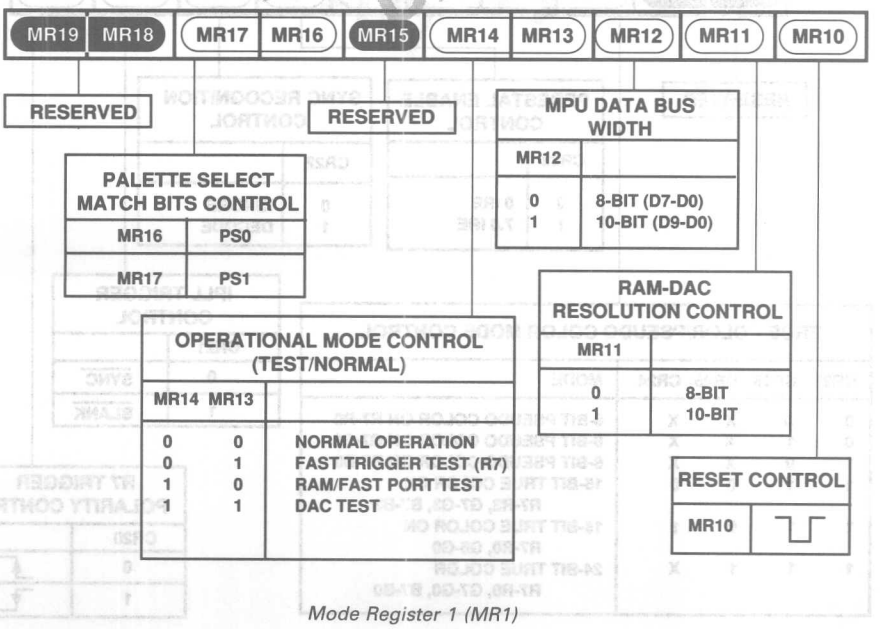
This bit determines the width of the MPU port. It is configured as either a 10-bit wide (D9–D0) or 8-bit wide (D7–D0) bus. 10-bit data can be written to the device when configured 8-bit wide mode. The eight MSBs are first written on D7–D0, then the two LSBs are written over D1–D0. Bits D9–D8 are zeros in 8-bit mode.

Operational Mode Control (Test/Normal) (MR14–MR13)

When these bits are zero, the part operates in normal mode. All other combinations are used in conjunction with the device's various test/diagnostic modes (see Test Diagnostics section).

Palette Select Match Bits Control (MR17–MR16)

These bits allow multiple palette devices to work together. When PS1–PS0 match MR17–MR16, the device is selected (see Palette Priority Select Inputs section).



Mode Register 1 (MR1)

PRELIMINARY TECHNICAL DATA

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CONTROL REGISTERS

The ADV7150/ADV7152 has seven control registers. To access each register, two write operations must be performed. The first write to the address register specifies which of the seven registers is to be accessed. The second access determines the value written to that particular control register.

Table III lists the various control registers and their respective addresses.

Table III. Control Registers Descriptions

ADDR Register	Control Registers* (A2–A0)
00H	Pixel Test Register
01H	DAC Test Register
02H	$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and I_{PLL} Test Register
03H	ID Register (Read Only)
04H	Pixel Mask Register
05H	Reserved
06H	Command Register 2
07H	Command Register 3

*C1 = 1; C0 = 0.

Pixel Test Register

This register is used when the device is in test/diagnostic mode. It is an 8-bit wide read-only register which allows MPU access to the pixel port (see Test Diagnostics section).

DAC Test Register

This register is used when the device is in test/diagnostic mode. It is a 10-bit wide read/write register which allows MPU access to the DAC port (see Test Diagnostics section).

$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ & I_{PLL} Test Register:

This register is used when the device is in test/diagnostic mode. It is a 3-bit wide (3 LSBs) read/write register which allows MPU access to these particular pixel control bits (see Test Diagnostics section).

ID Register

This is an 8-bit wide read-only register. For the ADV7150, it will always return the hexadecimal value 8EH and for the ADV7152, 8CH will be returned.

Pixel Mask Register

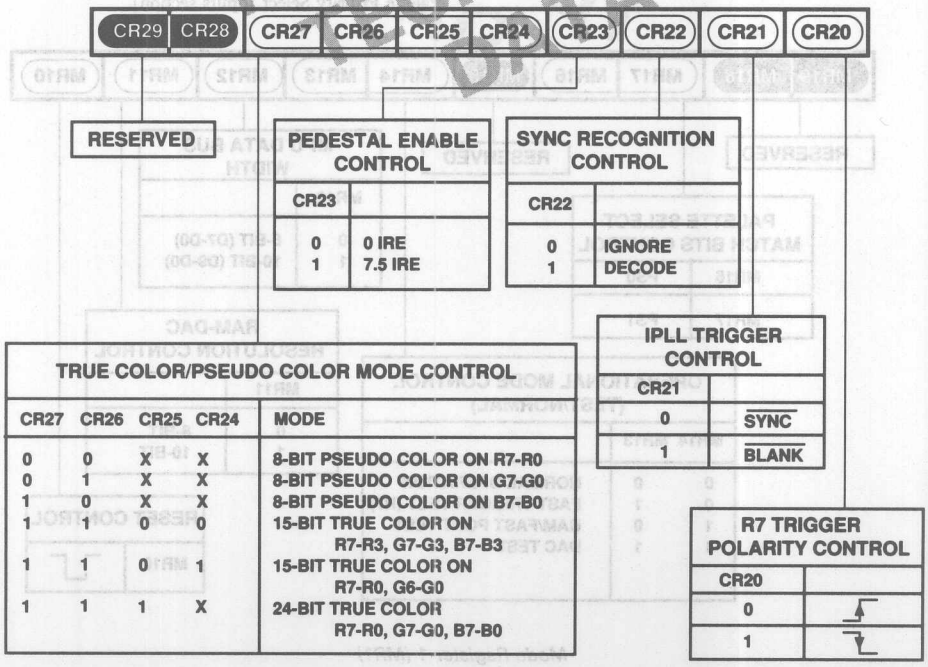
The contents of the pixel read mask register are individually bitwise logically ANDed with the red, green and blue pixel input stream of data. It is an 8-bit read/write register with D0 corresponding to R0, G0 and B0.

Command Register 2 (CR2)

This register contains a number of control bits as shown in the diagram. CR2 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR28 and CR29 are both reserved).

The diagram below shows the various operations under the control of CR2. This register can be read from as well written to. In read mode, CR28 and CR29 are both returned as zeros.

PRELIMINARY TECHNICAL DATA



Command Register 2 (CR2)

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COMMAND REGISTER 2 (CR2) BIT DESCRIPTION

R7 Trigger Polarity Control (CR20)
This bit is used when the device is in test/diagnostic mode. It determines whether the pixel data is latched into the test registers in the rising or falling edge of R7 (see test diagnostics section).

I_{PLL} Trigger Control (CR21)
This bit specifies whether the PLL output is triggered from $\overline{BLANK}$ or $\overline{SYNC}$.

$\overline{SYNC}$ Recognition Control (CR22)
This bit specifies whether the video $\overline{SYNC}$ input is to be encoded onto the IOG analog output or ignored.

Pedestal Enable Control (CR23)
This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

True-Color/Pseudo-Color Mode Control (CR27-CR24)
These 4 bits specify the various color modes. These include a 24-bit true-color mode, two 15-bit true-color modes and three 8-bit pseudo color modes.

Command Register 3 (CR3)
This register contains a number of control bits as shown in the diagram. CR3 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR38 and CR39 are both reserved).

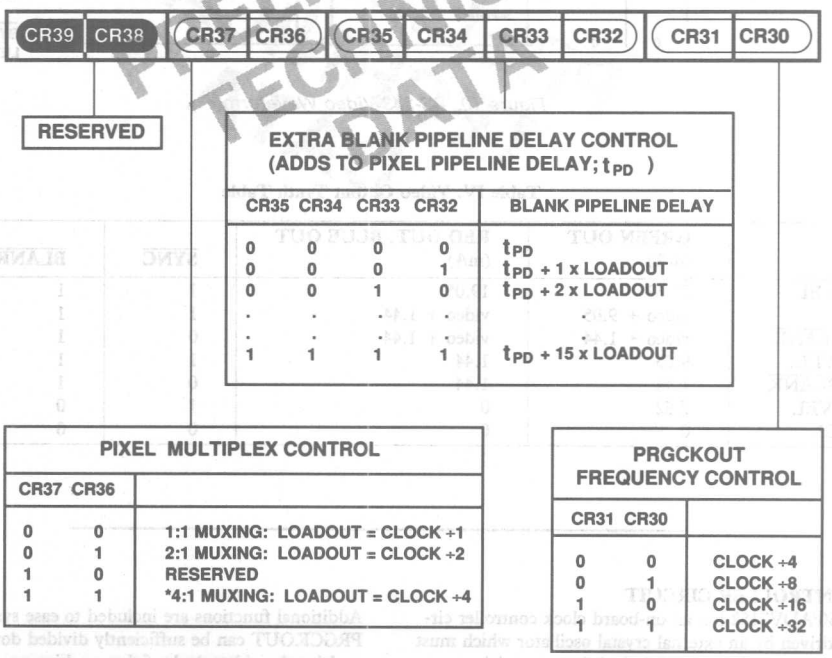
The diagram below shows the various operations under the control of CR3. This register can be read from as well as written to. In read mode, CR38 and CR39 are both returned as zeros.

COMMAND REGISTER 3 (CR3) BIT DESCRIPTION

PRGCKOUT Frequency Control (CR31–CR30)
These bits specify the output frequency of the PRGCKOUT output. PRGCKOUT is a divided down version of the pixel CLOCK.

$\overline{BLANK}$ Pipeline Delay Control (CR35–CR32)
These bits specify the additional pipeline delay that can be added to the $\overline{BLANK}$ function, relative to the overall device pipeline delay (t_{PD}). As the $\overline{BLANK}$ control normally enters the video DAC from a shorter pipeline than the video pixel data, this control is useful in deskewing the pipeline differential.

Pixel Multiplex Control (CR37–CR36)
These bits specify the device's multiplex mode. It, therefore, also determines the frequency of the LOADOUT signal. LOADOUT is a divided down version of the pixel CLOCK.



*ON THE ADV7152, THIS STATE IS RESERVED.

Command Register 3 (CR3)

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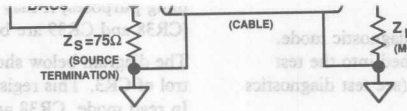


Figure 9. RS-343A Termination

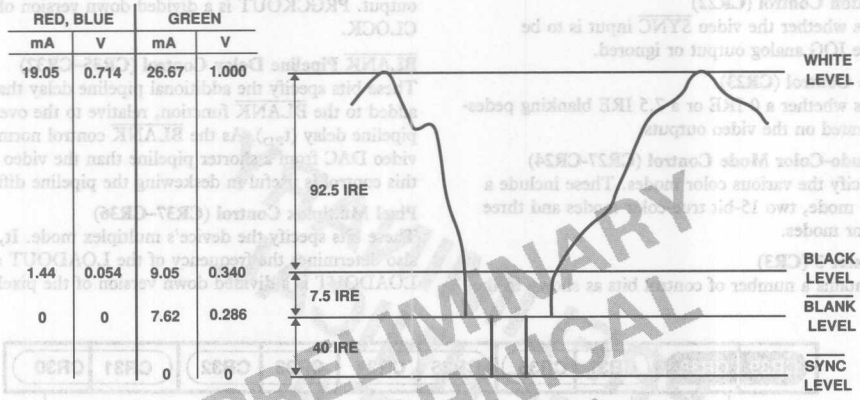


Figure 10. RS-343 Video Waveform

PRELIMINARY TECHNICAL DATA

Table IV. Video Output Truth Table

Description	GREEN OUT (mA)	RED OUT, BLUE OUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	3FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to $\overline{BLANK}$	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	000H
BLACK to $\overline{BLANK}$	1.44	1.44	0	1	000H
$\overline{BLANK}$ LEVEL	7.62	0	1	0	XXXH
$\overline{SYNC}$ LEVEL	0	0	0	0	XXXH

CLOCK CONTROLLER CIRCUIT

The ADV7150/ADV7152 has an on-board clock controller circuit. This is driven by an external crystal oscillator which must be capable of generating differential clock inputs to drive $\overline{CLOCK}$ and CLOCK of the ADV7150/ADV7152.

No additional external clocking devices are necessary. A sophisticated on-board clocking arrangement generates all the required internal clocking signals.

Additional functions are included to ease system design. The PRGCKOUT can be sufficiently divided down and can be used to drive the video clock of the graphics processor.

In its simplest form, the LOADOUT pin can be tied directly to the LOADIN pin, as shown. The pixel data LOADIN rate will be determined by the multiplex rate.

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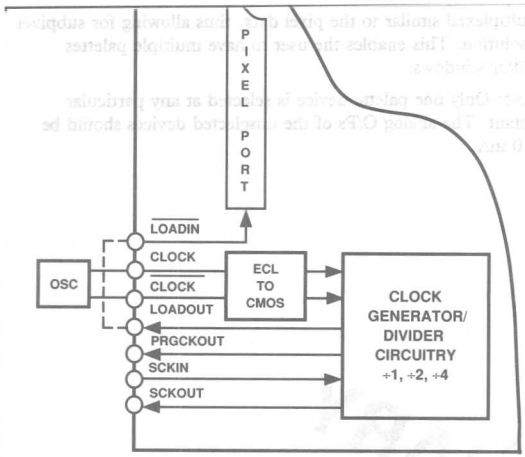


Figure 11. Clock Circuitry

TEST DIAGNOSTICS

Test diagnostic circuitry on the ADV7150/ADV7152 allows the user to debug both the device itself and its interface to other components in the system. Essentially, the video or pixel path through the device can be monitored via the MPU. Monitoring points, in the form of test registers are positioned at the PIXEL PORT, RAM and DAC PORT. Control of the test modes is determined by the Mode Register (MR1) and Command Register 2. Data is latched to the various test registers along the video path by either the pixel CLOCK or by using one bit of pixel data as a trigger bit (R7). This latter case is useful when the pixel CLOCK is connected to a free running source.

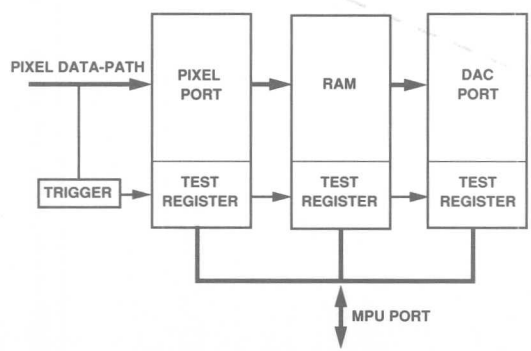


Figure 12.

Mode 0
Normal Chip Operation. In this mode, the test registers are configured as in Figure 13. Both the pixel test register and the DAC test register are triggered every clock cycle. This is transparent to the general user. It becomes useful when there is and verified.

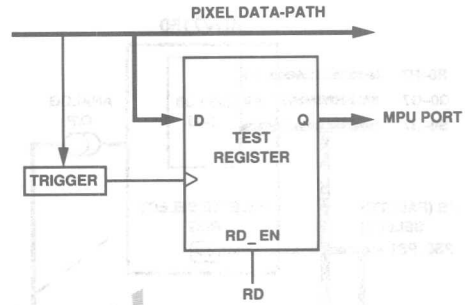


Figure 13.

Mode 1
Pixel Data-Path Trigger. In this mode, the test register trigger is activated by a transition on the R7 bit of the pixel port, Figure 13. Bit 0 of command register 2 controls whether the trigger is activated by a rising edge or a falling edge of R7. The trigger bit is piped through the chip along with the pixel data. This means that each test register captures the pixel with the transition on R7 as it is piped through the chip. Once the data has been captured, it can be read out at any time, even if the pattern is cyclical with the same pixel repeatedly activating the trigger.

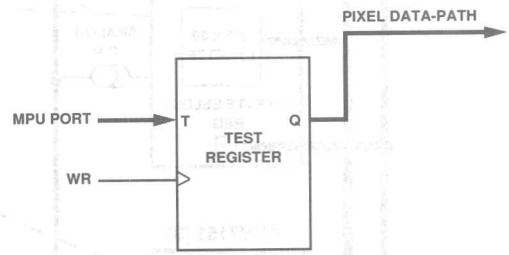


Figure 14.

Mode 2
RAM Fast-Port Test. Is this mode, the pixel test register is configured as in Figure 13, and the DAC test register configured as in Figure 14. The DAC test register is triggered every clock cycle. Data written into the pixel test register enters the fast data path, passes through the palette, and gets captured at the DAC test register.

Mode 3
DAC Test. In this mode, the DAC test register and the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ & PLL test register are configured as in Figure 14. Data written to the DAC test register, and the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and PLL test register is reflected at the DAC outputs. This allows the DACs to be tested over the microport.

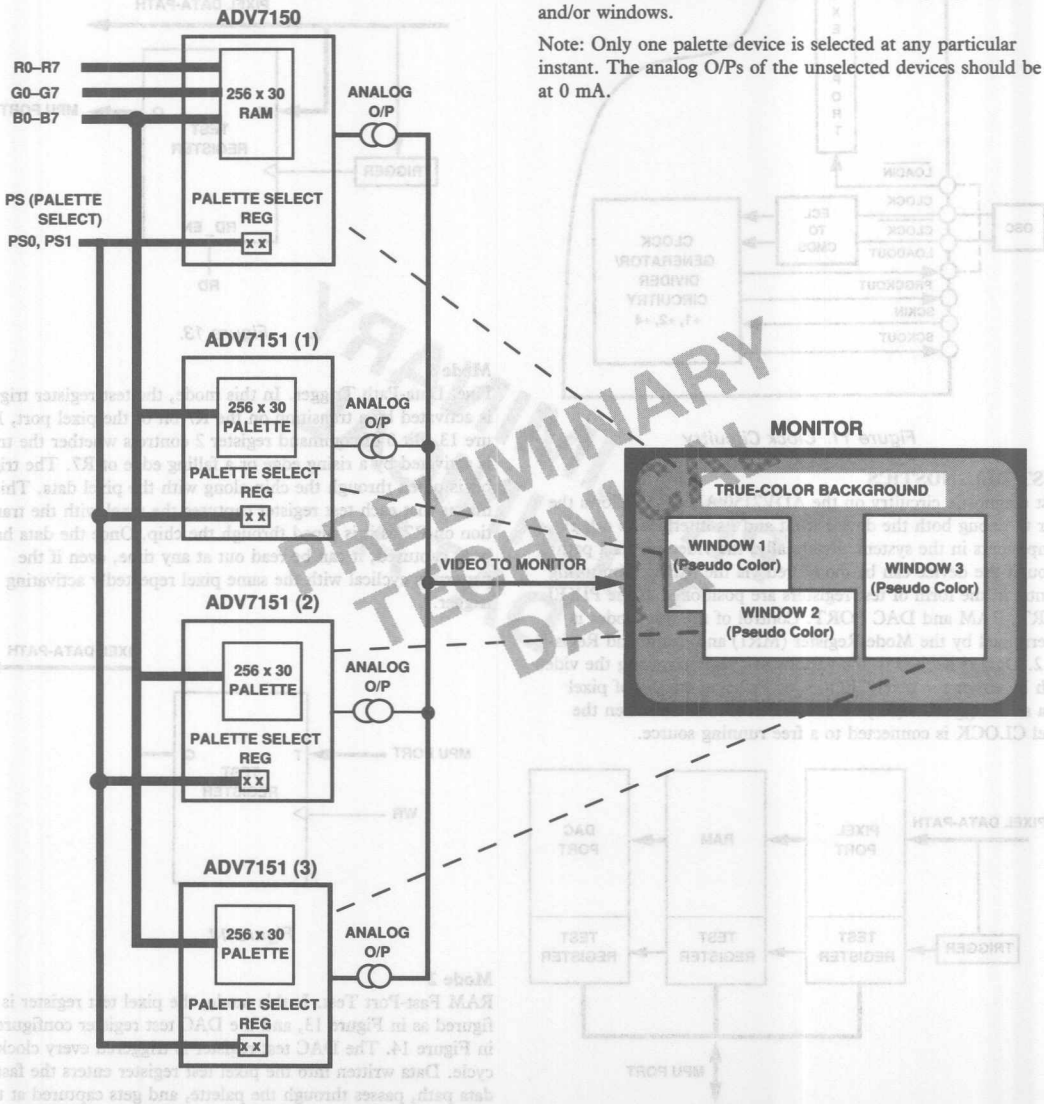
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Palette Priority Select Inputs

The palette priority selection function allows up to 4 palette devices to be used with their analog O/Ps connected together. During initialization, internal registers, which prioritize each device, are programmed. PS0 and PS1 inputs will select one of the preprogrammed devices at any instant. PS0 and PS1 are multiplexed similar to the pixel data, thus allowing for subpixel resolution. This enables the user to have multiple palettes and/or windows.

Note: Only one palette device is selected at any particular instant. The analog O/Ps of the unselected devices should be at 0 mA.



PRELIMINARY TECHNICAL DATA

Figure 15.

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PC Board Considerations
The layout should be optimized for lowest noise on the ADV7150/ADV7152 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes
The ground plane should encompass all ADV7150/ADV7152 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7150/ADV7152, the analog output traces, and all the digital signal traces leading up to the ADV7150/ ADV7152.

Power Planes
The ADV7150/ADV7152 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7150/ADV7152.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7150/ADV7152 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling
For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7150/ADV7152 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect
The digital inputs to the ADV7150/ADV7152 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7150/ADV7152 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect
The ADV7150/ADV7152 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV7150/ADV7152 to minimize reflections.

PRELIMINARY TECHNICAL DATA

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ADV7151

FEATURES

- 170 MHz Pipelined Operation
- Triple 10-Bit D/A Converters
- Triple 256 × 10 (256 × 30) Color Palette RAM
- On-Chip Clock Control Circuit
- Palette Priority Select Registers
- RS-343A/RS-170 Compatible Analog Outputs
- TTL Compatible Digital Inputs
- 32-Bit Pixel Input Port (8-Bit Pixel Words)
- Standard MPU I/O Interface
  - 10-Bit Parallel Structure
  - 8+2 Byte Structure
- Pixel Data Serializer
  - Multiplexed Pixel Input Ports; 1:1, 2:1, 4:1
- +5 V CMOS Monolithic Construction
- 100-Pin PQFP

SPEED GRADES

- 170 MHz
- 135 MHz
- 110 MHz
- 85 MHz

GENERAL DESCRIPTION

The ADV7151 (ADV®) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in the graphics systems of high performance, color graphics workstations. The ADV7151 integrates a number of graphic functions onto one device allowing 8-bit indexed Pseudo-Color operation at the maximum screen update rate of 170 MHz.

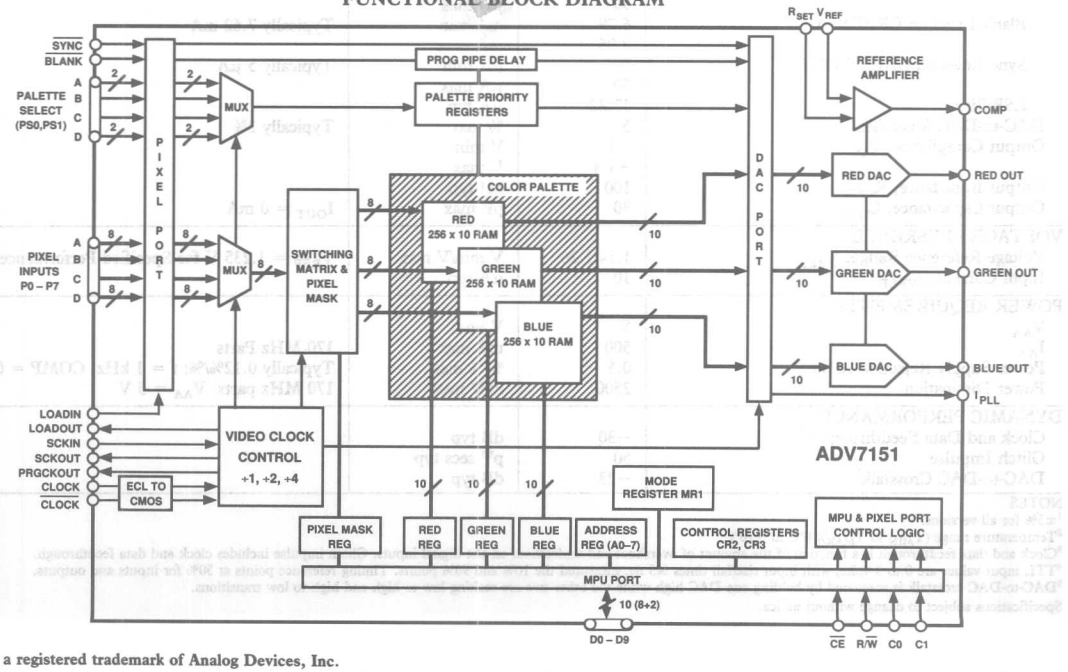
The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority registers, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The on-board palette priority select registers enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled (i.e., mode selection and multiplex selection) through the MPU port by the various on-board control/command registers. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device.

Pseudo-color image rendition, at speeds of up to 170 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input port's flexibility allows for direct interface to most standard frame buffer memory configurations, including general purpose DRAM and VRAM designs.

(continued on page 2–911)

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



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ADV7151—SPECIFICATIONS (V_{AA}[1] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	10	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding		Binary	
DIGITAL INPUTS (Excluding CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
CLOCK INPUTS (CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	V_{AA} − 1.0	V min	
Input Low Voltage, V_{INL}	V_{AA} − 1.6	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	20	μA max	
Floating-State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on RED OUT, BLUE OUT	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on GREEN OUT	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level on GREEN OUT	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	17.22	μA typ	
DAC-to-DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	100	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	10	μA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	500	mA max	170 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	2500	mW max	170 MHz parts: V_{AA} = 5 V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−30	dB typ	
Glitch Impulse	50	pV secs typ	
DAC-to-DAC Crosstalk[5]	−23	dB typ	

NOTES
[1]±5% for all versions.
[2]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.
[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[4]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[5]DAC-to-DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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TIMING CHARACTERISTICS[1]

(V_{AA}[2] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted.)

Parameter	170 MHz Version	135 MHz Version	110 MHz Version	85 MHz Version	Units	Conditions/Comments
f_{MAX}	170	135	110	85	MHz	Clock Rate
LOADOUT						
1:1 MUX Mode						
Frequency	68	68	68	68	MHz	LOADOUT Clocking Rate
Period	14.71	14.71	14.71	14.71	ns max	LOADOUT Period
High Time	6	6	6	6	ns min	LOADOUT High Time
Low Time	6	6	6	6	ns min	LOADOUT Low Time
2:1 MUX Mode						
Frequency	68	67.5	55	42.5	MHz	LOADOUT Clocking Rate
Period	14.71	14.81	18.18	21.25	ns max	LOADOUT Period
High Time	6	6	8	8.5	ns min	LOADOUT High Time
Low Time	6	6	8	8.5	ns min	LOADOUT Low Time
4:1 MUX Mode						
Frequency	42.5	33.75	27.5	21.25	MHz	LOADOUT Clocking Rate
Period	23.5	30	36.4	47	ns max	LOADOUT Period
High Time	10	12	14.5	18.8	ns min	LOADOUT High Time
Low Time	10	12	14.5	18.8	ns min	LOADOUT Low Time
t_1	15	15	15	15	ns max	Pixel CLOCK to LOADOUT Delay
t_2	15	15	15	15	ns max	Pixel CLOCK to PROGCKOUT Delay
t_3	5	5	5	5	ns min	LOADIN to LOADOUT Setup Time
t_4	0	0	0	0	ns min	Video and Pixel Data Setup Time
t_5	5	5	5	5	ns min	Video and Pixel Data Hold Time
t_6	5	5	5	5	ns max	SCKIN to SCKOUT Delay
t_7	5.88	7.4	9.09	11.77	ns min	Clock Cycle Time
t_8	2.5	3	4	5	ns min	Clock Pulse Width High Time
t_9	2.5	3	4	5	ns min	Clock Pulse Width Low Time
t_{10}	12	12	12	12	ns min	Analog Output Delay
t_{11}	2	2	2	3	ns min	Analog Output Rise/Fall Time
t_{12}[4]	6	8	8	12	ns min	Analog Output Settling Time
t_{13}	0	0	0	0	ns min	R/$\overline{W}$, C0, C1 Setup Time
t_{14}	15	15	15	15	ns min	R/$\overline{W}$, C0, C1 Hold Time
t_{15}	50	50	50	50	ns min	$\overline{CE}$ Low Time
t_{16}	25	25	25	25	ns min	$\overline{CE}$ High Time
t_{17}[5]	5	5	5	5	ns min	$\overline{CE}$ Asserted to Data Bus Driven
t_{18}[5]	50	50	50	50	ns max	$\overline{CE}$ Asserted to Data Valid
t_{19}[6]	15	15	15	15	ns max	$\overline{CE}$ Disabled to Data Bus Three Stated
	5	5	5	5	ns min	
t_{20}	20	20	20	20	ns min	Write Data Setup Time
t_{21}	5	5	5	5	ns min	Write Data Hold Time
t_{SK}	2	2	2	2	ns max	Analog Output Skew
	0	0	0	0	ns typ	
t_{PD}	6	6	6	6	Clocks	Pipeline Delay

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 5.

[2]±5% for all versions.

[3]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[4]Settling time does not include clock and data feedthrough.

[5]t_{17} and t_{18} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.4 V or 2.4 V.

[6]t_{19} is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_{19}, quoted in the timing characteristics is the true value for the device and, as such, is independent of external bus loading capacitances.

Specifications subject to change without notice.

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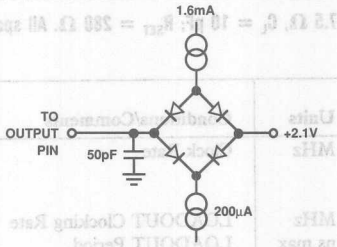


Figure 1. Load Circuit for Bus Access and Relinquish Time

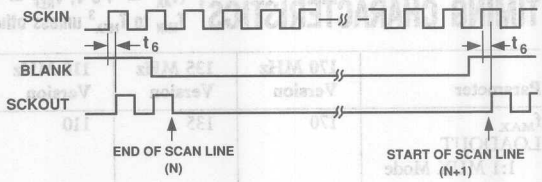


Figure 4. Video Data Serial Clock Input (SCKIN) vs. Serial Clock Output (SCKOUT)

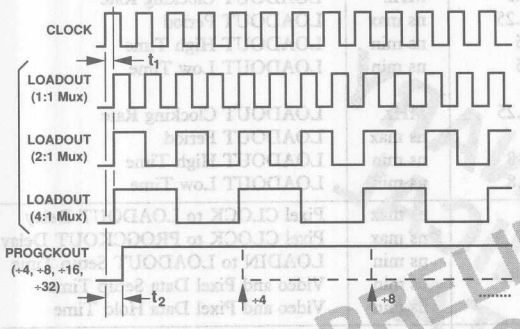
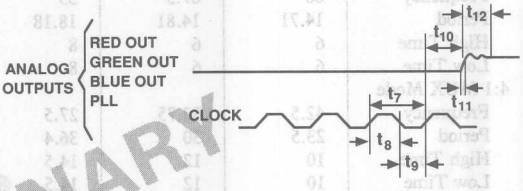
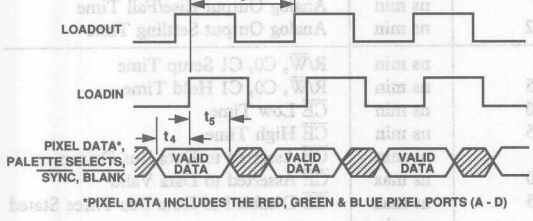


Figure 2. Video Output Clock Controls vs. Pixel Clock Input



NOTES:
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. SETTLING TIME MEASURED FROM 50% POINT FULL-SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ± 1LSB.
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.

Figure 5. Analog Outputs vs. Pixel Clock



*PIXEL DATA INCLUDES THE RED, GREEN & BLUE PIXEL PORTS (A - D)

Figure 3. LOADOUT Timing vs. LOADIN and Pixel Data

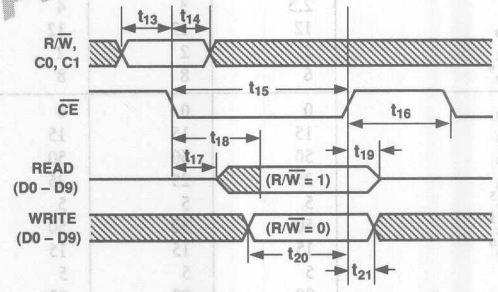


Figure 6. MPU Port Read/Write Timing

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Output Load	R_L		37.5		Ω

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on any Digital Pin . . . . . GND−0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[2] . . . . . −1.5 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



(continued from page 2–907)

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 8-bit pseudo-color resolution, while also allowing for the on-board implementation of linearization algorithms, such as gamma correction.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7151. The part can also be driven by an external clock generator chip circuit.

The ADV7151 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the users system level debugging.

The ADV7151 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The part is packaged in an 100-lead PQFP.

ORDERING GUIDE

Model	Speed	Temperature Range	No. of Pins	Package Option*
ADV7151KS170	170 MHz	0°C to +70°C	100	S-100
ADV7151KS135	135 MHz	0°C to +70°C	100	S-100
ADV7151KS110	110 MHz	0°C to +70°C	100	S-100
ADV7151KS85	85 MHz	0°C to +70°C	100	S-100

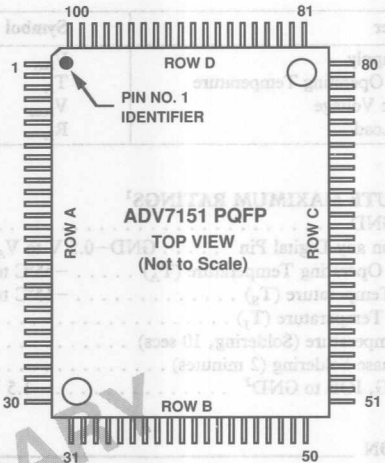
*S = Plastic Quad Flat Pack. For outline information see Package Information section.

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No.	Mnemonic	No.	Mnemonic	No.	Mnemonic
1	V_{AA}	41	GND	81	V_{AA}
2	$\overline{SYNC}$	42	GND	82	D6
3	$\overline{BLANK}$	43	NC*	83	D7
4	NC*	44	GND	84	D8
5	NC*	45	GND	85	D9
6	NC*	46	NC*	86	GND
7	$P0_A$	47	NC*	87	GND
8	$P0_B$	48	$PS0_A$	88	$\overline{IOB}$
9	$P0_C$	49	$PS0_B$	89	$\overline{IOR}$
10	$P0_D$	50	$PS0_C$	90	$\overline{IOG}$
11	$P1_A$	51	$PS0_D$	91	IOB
12	$P1_B$	52	$PS1_A$	92	IOG
13	$P1_C$	53	$PS1_B$	93	V_{AA}
14	$P1_D$	54	$PS1_C$	94	V_{AA}
15	NC*	55	$PS1_D$	95	IOR
16	$P2_A$	56	$P5_A$	96	COMP
17	$P2_B$	57	$P5_B$	97	V_{REF}
18	$P2_C$	58	$P5_C$	98	R_{SET}
19	$P2_D$	59	$P5_D$	99	I_{PLL}
20	NC*	60	$P6_A$	100	GND
21	NC*	61	$P6_B$		
22	$P3_A$	62	$P6_C$		
23	$P3_B$	63	$P6_D$		
24	$P3_C$	64	NC*		
25	$P3_D$	65	$P7_A$		
26	NC*	66	$P7_B$		
27	NC*	67	$P7_C$		
28	$P4_A$	68	$P7_D$		
29	$P4_B$	69	NC*		
30	$P4_C$	70	$\overline{CE}$		
31	$P4_D$	71	R/$\overline{W}$		
32	$\overline{CLOCK}$	72	C0		
33	CLOCK	73	C1		
34	LOADIN	74	D0		
35	LOADOUT	75	D1		
36	V_{AA}	76	D2		
37	V_{AA}	77	GND		
38	PRGCKOUT	78	D3		
39	SCKIN	79	D4		
40	SCKOUT	80	D5		

*NC = NO CONNECT.



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PIN DESCRIPTION

Pin	Function
Pixel Select Inputs ($P0_A$ . . . $P0_D$–$P7_A$ . . . $P7_D$)	Pixel Port: 32 Pixel Select Inputs. Each 8-bit index word selects either a 24-bit or 30-bit color value. Each bit is multiplexed (A-D) 4:1, 2:1 or 1:1. All inputs are TTL compatible.
$PS0_A$ . . $PS0_D$, $PS1_A$ . . . $PS1_D$	Palette Priority Select Inputs: These inputs allow for switching between multiple palette devices at the pixel rate. The device can be preprogrammed to completely shut off the DAC analog O/Ps. If the values of PS0 and PS1 match the values programmed into bits MR6 and MR7 of the Mode Register, then the device is selected.
LOADIN, LOADOUT, PRGCKOUT, SCKIN, SCKOUT	Video Data Control Inputs/Outputs: These inputs/outputs are used to load pixel data and, optionally, to control external video frame buffer timing and control synchronization.
CLOCK, $\overline{\text{CLOCK}}$	Clock Inputs: These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
$\overline{\text{BLANK}}$	Composite Blank: Drives the analog outputs to the blanking level.
$\overline{\text{SYNC}}$	Composite Sync Input: Drives the IOG analog output to the sync level. It can only be asserted during the blanking period.
D0–D9	Data Bus: Data is written to and is read from the device over this 10-bit, bidirectional data bus. 10-bit data or 8-bit data can be used. The data bus can be configured for either 10-bit parallel data or byte data (8+2). Byte data is right justified, i.e., 8 LSBs first, then 2 MSBs.
$\overline{\text{CE}}$, R/$\overline{\text{W}}$, CO, C1	Control Inputs: These inputs control the writing to and reading from the address reg, color palette, palette select registers, mode control registers etc., of the device.
IOR, IOG, IOB ($\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$)	Analog Video Current Outputs (Differential Outputs): These RGB video outputs are capable of directly driving RS-343A and RS-170 video levels into doubly terminated 75 Ω loads. $\overline{\text{IOR}}$, $\overline{\text{IOG}}$ and $\overline{\text{IOB}}$ can be tied to GND if it is not required to have differential outputs.
V_{REF}	Voltage Reference Input: An external 1.235 V voltage reference is required to drive this input. The use of an AD589 (2-terminal voltage reference) is recommended.
R_{SET}	Output Full-Scale Adjust Control: A resistor connected between this pin and analog ground controls the absolute amplitude of the output video signal. To maintain RS-343A video output levels, R_{SET} = 280 Ω
COMP	Compensation Pin: A 0.1 μF capacitor should be connected between this pin and V_{AA}.
I_{PLL}	Phase Lock Loop Output Current: This is used to enable multiple ADV7151s and ADV7150/ADV7152s to be synchronized with pixel resolution.
V_{AA}	Power Supply (+5 V ± 5%): The part contains multiple power supply pins; all should be connected to one common +5 V analog power supply.
GND	Analog Ground: The part contains multiple ground pins; all should be connected to one common analog ground.

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COLOR VIDEO MODES (PIXEL PORT)

8-BIT PSEUDO COLOR

This mode is selected by writing to Command Register 2. In this mode 8-bit pseudo color images can be generated on screen at video rates of up to 170 MHz. Two hundred fifty-six colors can be displayed out of a total color palette of 16.7 million addressable colors. The 8-bit pixel select or pixel index word selects a 24-bit or 30-bit RGB value which drives the red, green and blue DACs.

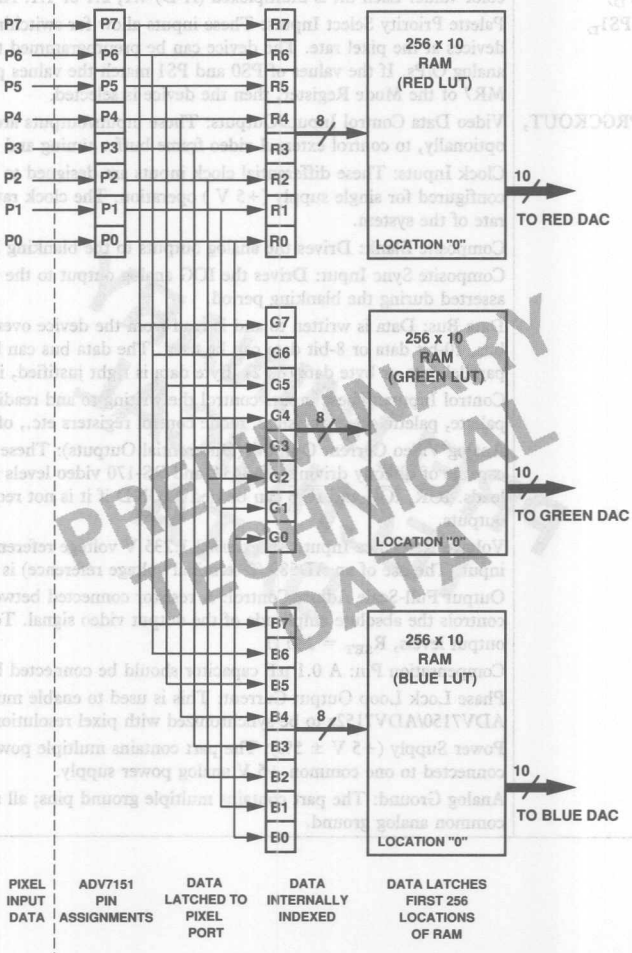


Figure 7. 8-Bit Pseudo-Color (Indexed Color) Mapping

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MPU INTERFACE & CONTROL

The ADV7151 supports a standard MPU Interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the address register, mode register and all the control registers as well as the color palette. The following tables describe the setup for reading and writing to all of the devices registers.

R/$\overline{W}$	C1	C0	D9–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB0	Write DB9–DB0 to Red RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Green RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Blue RAM Latch & Write RGB Data To RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9–DB0	Read Red RAM Location A7–A0
1	0	1	DB9–DB0	Read Green RAM Location A7–A0
1	0	1	DB9–DB0	Read Blue Ram Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]10-bit wide databus, i.e., MR12 = "1" and 10-bit RAM & DACs, i.e., MR11 = "1" or 10-bit wide databus, i.e., MR12 = "1" and 8-Bit RAM & DACs, i.e., MR11 = "0" or 8-bit wide databus, i.e., MR12 = "0" and 8-Bit RAM & DACs, i.e., MR11 = "0."
[2]Refer to table entitled "Control Registers Description."

R/$\overline{W}$	C1	C0	D7–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB2	Write DB9–DB2 to Red RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Red RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Green RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Green RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Blue RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Blue RAM Latch (1–0) & Write RGB Data to RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9–DB2	Read Red RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Red RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Green RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Green RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Blue RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Blue RAM (1–0) Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]8-bit wide databus, i.e., MR12 = "0" and 10-Bit RAM & DACs, i.e., MR11 = "1."
[2]Refer to table entitled "Control Registers Description."

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the mode register. The control registers, the 7 of which are listed in the table are indexed adressable. The first write to the control register specifies which particular register is to be accessed.

Address Register (ADDR) A7–A0
As illustrated in the previous tables, the C0 and C1 control inputs, in conjunction with this address register specify which control/mode register, or color palette location is accessed by the MPU port. The address register is 8 bits wide and can be read from as well as written to. When writing to or reading from the color palette on a sequential basis, only the start address needs to be written. After a red, green and blue write sequence, the address register is automatically incremented.

Mode Register 1 (MR1)
The mode register is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (MR18 and MR19 are both reserved).

The diagram below shows the various operations under the control of the mode register. This register can be read from as well written to. In read mode, MR18 and MR19 are both returned as zeroes.

MODE REGISTER (MR1) BIT DESCRIPTION
Reset Control (MR10)
This bit is used to reset the pixel port sampling sequence. This ensures that the pixel sequence ABCD starts at A. It is reset by writing a 1 followed by a zero followed by a 1.

RAM-DAC Resolution Control (MR11)
When this is programmed with a 1, the RAM is 30-bits deep (10 bits each for red, green and blue) and each of the three DACs is configured for 10-bit resolution.

When MR11 is programmed with a 0, the RAM is 24-bits deep (8 bits each for red, green and blue) and the DACs are configured for 8-bit resolution. The two LSBs of the 10-bit DACs are pulled down to zero.

as either a 10-bit wide (D9–D0) or 8-bit wide (D7–D0) bus. 10-bit data can be written to the device when configured 8-bit wide mode. The 8 MSBs are first written on D7–D0, then the two LSBs are written over D1–D0. Bits D9–D8 are zeroes in 8-bit mode.

Operational Mode Control (Test/Normal) (MR14–MR13)
When these bits are zero the part operates in normal mode. All other combinations are used in conjunction with the devices various test/diagnostic modes (see Test Diagnostics section).

Palette Select Match Bits Control (MR17–MR16)
These bits allow multiple palette devices to work together. When PS1–PS0 match MR17–MR16, the device is selected (see Palette Priority Select Inputs section).

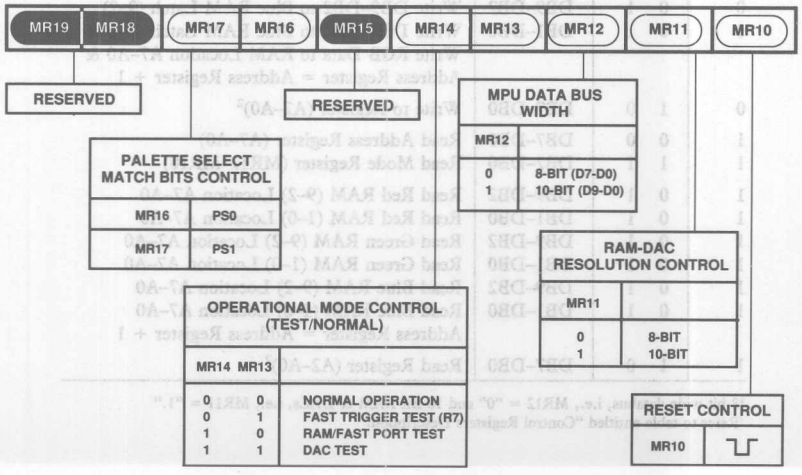
Control Registers
The ADV7151 has 7 control registers. To access each register, two write operations must be performed. The first write to the address register specifies which of the 7 registers is to be accessed. The second access determines the value written to that particular control register.

The table below lists the various control registers and their respective addresses.

Control Registers Descriptions

ADDR Register (A2–A0)	Control Registers*
00H	Pixel Test Register
01H	DAC Test Register
02H	$\overline{SYNC}$, $\overline{BLANK}$ and I_{PLL} Test Register
03H	ID Register (Read Only)
04H	Pixel Mask Register
05H	Reserved
06H	Command Register 2
07H	Command Register 3

*C1 = 1; C0 = 0.



Mode Register 1 (MR1)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Pixel Test Register
This register is used when the device is in test/diagnostic mode. It is an 8-bit wide read-only register which allows MPU access to the pixel port (see Test Diagnostics section).

DAC Test Register
This register is used when the device is in test/diagnostic mode. It is a 10-bit wide read/write register which allows MPU access to the DAC port (see Test Diagnostics section).

$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ & I_{PLL} Test Register
This register is used when the device is in test/diagnostic mode. It is a 3-bit wide (3 LSBs) read/write register which allows MPU access to these particular pixel control bits (see Test Diagnostics section).

ID Register
This is an 8-bit wide read-only register. For the ADV7151 it will always return the hexadecimal value 8FH.

Pixel Mask Register
The contents of the pixel read mask register are individually bit-wise logically ANDed with the red, green and blue pixel input stream of data. It is an 8-bit read/write register with D0 corresponding to R0, G0 and B0.

Command Register 2 (CR2)
This register contains a number of control bits as shown in the diagram. CR2 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR28 and CR29 are both reserved).

The diagram below shows the various operations under the control of CR2. This register can be read from as well as written to. In read mode, CR28 and CR29 are both returned as zeroes.

COMMAND REGISTER 2 (CR2) BIT DESCRIPTION

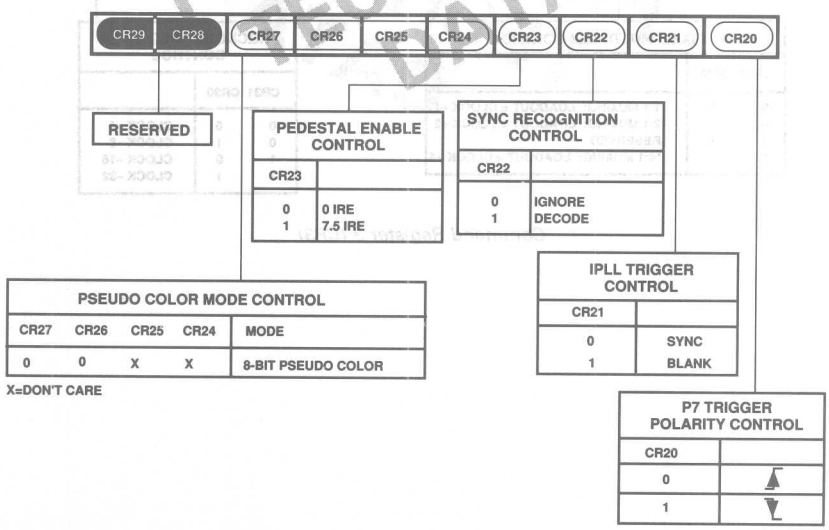
P7 Trigger Polarity Control (CR20)
This bit is used when the device is in test/diagnostic mode. It determines whether the pixel data is latched into the test registers in the rising or falling edge of R7 (see Test Diagnostics section).

I_{PLL} Trigger Control (CR21)
This bit specifies whether the PLL output is triggered from $\overline{\text{BLANK}}$ or $\overline{\text{SYNC}}$.

$\overline{\text{SYNC}}$ Recognition Control (CR22)
This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be encoded onto the IOG analog output or ignored.

Pedestal Enable Control (CR23)
This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

Pseudo-Color Mode Control (CR27–CR24)
These 4 bits are used to set up the 8-bit pseudo-color mode. These bits must be set as described in the figure.



Command Register 2 (CR2)

PRELIMINARY TECHNICAL DATA

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Command Register 3 (CR3)

This register contains a number of control bits as shown in the diagram. CR3 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR38 and CR39 are both reserved).

The diagram below shows the various operations under the control of CR3. This register can be read from as well written to. In read mode, CR38 and CR39 are both returned as zeroes.

COMMAND REGISTER 3 (CR3) BIT DESCRIPTION

PRGCKOUT Frequency Control (CR31–CR30)

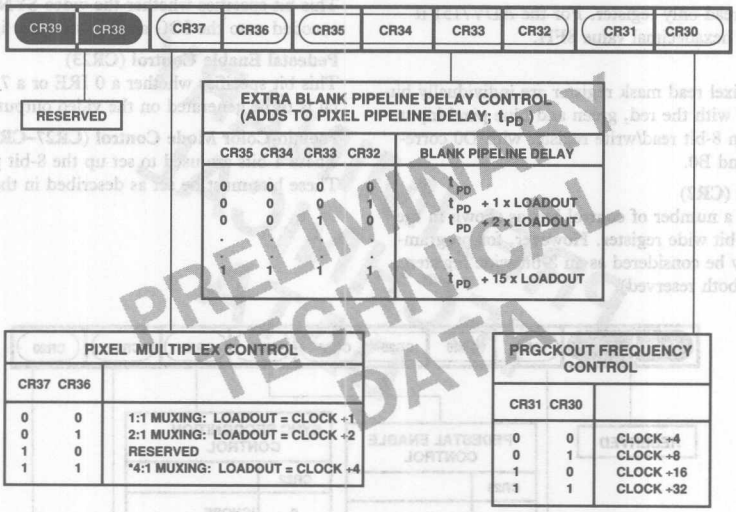
These bits specify the output frequency of the PRGCKOUT output. PRGCKOUT is a divided down version of the pixel CLOCK.

$\overline{\text{BLANK}}$ Pipeline Delay Control (CR35–CR32)

These bits specify the additional pipeline delay that can be added to the $\overline{\text{BLANK}}$ function, relative to the overall device pipeline delay (t_{PD}). As the $\overline{\text{BLANK}}$ control normally enters the video DAC from a shorter pipeline than the video pixel data, this control is useful in deskewing the pipeline differential.

Pixel Multiplex Control (CR37–CR36)

These bits specify the device's multiplex mode. It, therefore, also determines the frequency of the LOADOUT signal. LOADOUT is a divided down version of the pixel CLOCK.



Command Register 3 (CR3)

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

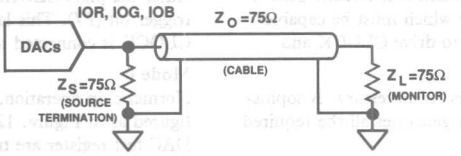
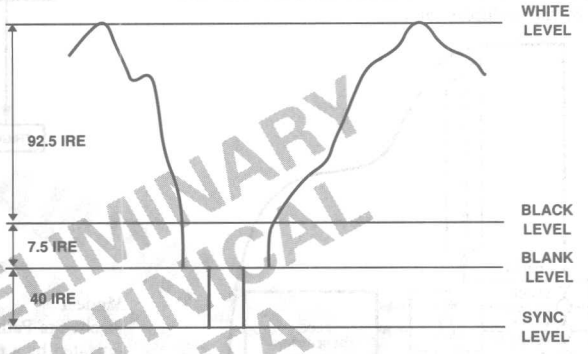


Figure 8. RGB Output Termination for RS-343A

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0	0	7.62	0.286
		0	0



PRELIMINARY TECHNICAL DATA

Figure 9. RGB Video Output Waveform

Video Output Truth Table

Description	GREEN OUT (mA)	RED OUT, BLUE OUT (mA)	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	3FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to $\overline{\text{BLANK}}$	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	000H
BLACK to $\overline{\text{BLANK}}$	1.44	1.44	0	1	000H
$\overline{\text{BLANK}}$ LEVEL	7.62	0	1	0	XXXH
$\overline{\text{SYNC}}$ LEVEL	0	0	0	0	XXXH

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The ADV7151 has an on-board clock controller circuit. This is driven by an external crystal oscillator which must be capable of generating differential clock inputs to drive CLOCK and $\overline{\text{CLOCK}}$ of the ADV7151.

No additional external clocking devices are necessary. A sophisticated on-board clocking arrangement generates all the required internal clocking signals.

Additional functions are included to ease system design. The PRGCKOUT can be sufficiently divided down and can be used to drive the video clock of the graphics processor.

In its simplest form, the LOADOUT pin can be tied directly to the LOADIN pin, as shown. The pixel data LOADIN rate will be determined by the multiplex rate.

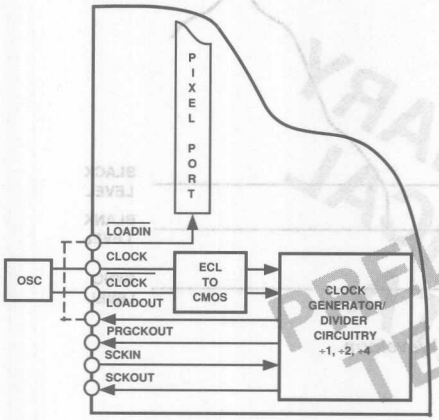


Figure 10.

TEST DIAGNOSTICS

Test diagnostic circuitry on the ADV7151 allows the user to debug both the device itself and its interface to other components in the system. Essentially, the video or pixel path through the device can be monitored via the MPU. Monitoring points, in the form of test registers, are positioned at the PIXEL PORT, RAM and DAC PORT. Control of the test modes is determined by the Mode Register (MR1) and Command Register 2. Data is either the pixel CLOCK or by using one bit of pixel data as a trigger bit (P7). This latter case is useful when the pixel CLOCK is connected to a free running source.

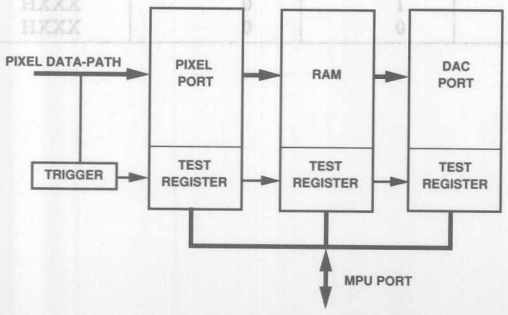


Figure 11.

Mode 0

Normal chip operation. In this mode, the test registers are configured as in Figure. 12. Both the pixel test register and the DAC test register are triggered every clock cycle. This is transparent to the general user. It becomes useful when there is independent control over the CLOCK. By stopping the clock in the low state, the data in the test registers can be read out and verified.

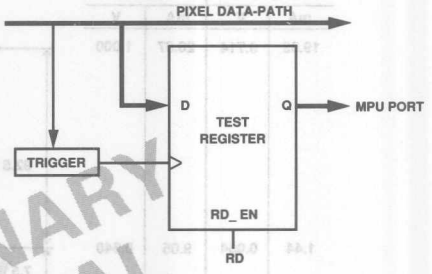


Figure 12.

Mode 1

Pixel Data Path Trigger. In this mode, the test register trigger is activated by a transition on the P7 bit of the pixel port, Figure 12. Bit 0 of Command Register 2 controls whether the trigger is activated by a rising edge or a falling edge of P7. The trigger bit is piped through the chip along with the pixel data. This means that each test register captures the pixel with the transition on P7 as it is piped through the chip. Once the data has been captured, it can be read out at any time, even if the pattern is cyclical with the same pixel repeatedly activating the trigger.

Mode 2

RAM Fast Port Test. In this mode, the pixel test register is configured as in Figure 12, and the DAC test register configured as in Figure 13. The DAC test register is triggered every clock cycle. Data written into the pixel test register enters the fast data path, passes through the palette, and gets captured at the DAC test register.

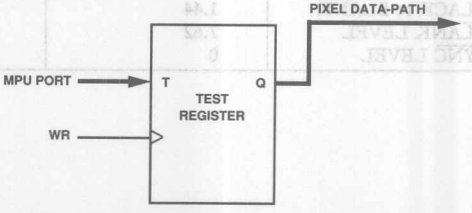


Figure 13.

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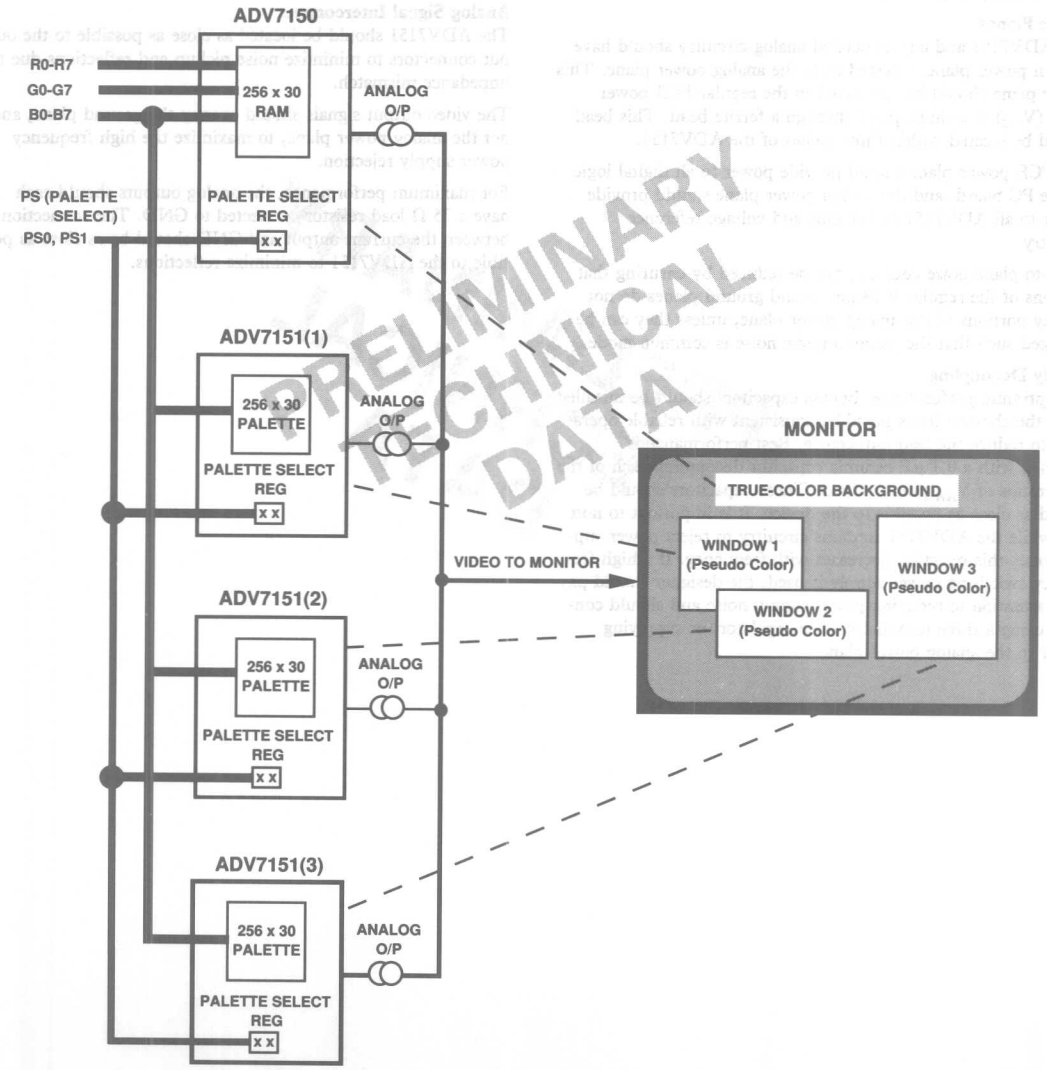
Mode 3
DAC Test. In this mode, the DAC test register and the $\overline{SYNC}$, $\overline{BLANK}$ & PLL test register are configured as in Figure 13. Data written to the DAC test register, and the $\overline{SYNC}$, $\overline{BLANK}$ and PLL test register is reflected at the DAC outputs. This allows the DACs to be tested over the MPU port.

Palette Priority Select Inputs
The palette priority selection function allows up to four palette devices to be used with their analog O/Ps connected together.

During initialization, internal registers, which prioritize each device, are programmed. PS0 and PS1 inputs will select one of the preprogrammed devices at any instant. PS0 and PS1 are multiplexed similar to the pixel data, thus allowing for subpixel resolution. This enables the user to have multiple palettes and/or windows.

Note: Only one palette device is selected at any particular instant. The analog O/Ps of the unselected devices should be at 0 mA.

2



PRELIMINARY TECHNICAL DATA

Figure 14.

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PC Board Considerations

The layout should be optimized for lowest noise on the ADV7151 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7151 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7151, the analog output traces, and all the digital signal traces leading up to the ADV7151.

Power Planes

The ADV7151 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7151.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7151 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device. It is important to note that while the ADV7151 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7151 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7151 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

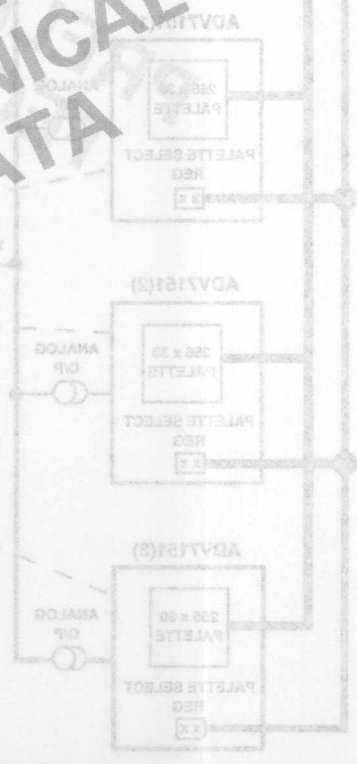
Analog Signal Interconnect

The ADV7151 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV7151 to minimize reflections.

PRELIMINARY TECHNICAL DATA



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8-Bit, High Speed, Multiplying D/A Converter (Universal Digital Logic Interface)

DAC-08

FEATURES

- **Fast Settling Output Current 85ns**
- **Full-Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to 0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance ..... −10V to +18V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift ..... ±10ppm/°C**
- **Wide Power Supply Range ..... ±4.5V to ±18V**
- **Low Power Consumption ..... 33mW @ ±5V**
- **Low Cost**
- **Available in Die Form**

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

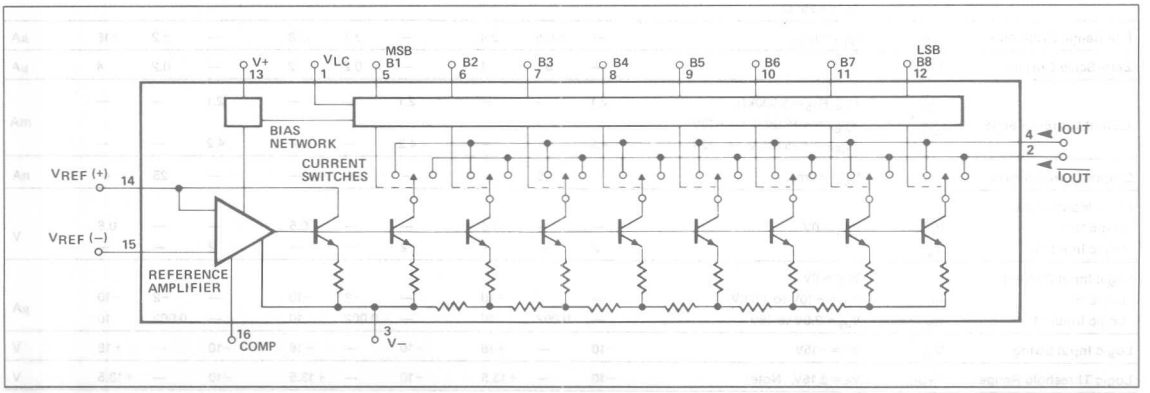
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
- DAC-08AQ, Q ..... –55°C to +125°C
- DAC-08HQ, EQ, CQ, HP, EP, CP, CS ..... 0°C to +70°C

Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Q Package ..... –65°C to +150°C
Storage Temperature P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply 36V
Logic Inputs ..... V– to V– plus 36V
V_{LC} ..... V– to V+
Analog Current Outputs (at V_S – = 15V) 4.25mA
Reference Input (V_{14} to V_{15}) ..... V– to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	76	36	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS

at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55°C \le T_A \le +125°C$ for DAC-08/08A, $0°C \le T_A \le +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H MIN	DAC-08A/H TYP	DAC-08A/H MAX	DAC-08E MIN	DAC-08E TYP	DAC-08E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Resolution			8	—	—	8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity	NL		—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF, $T_A = 25°C$, (Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t_{PLH}	$T_A = 25°C$	—	35	60	—	35	60	—	35	60	ns
All bits switched	t_{PHL}	(Note)	—	35	60	—	35	60	—	35	60	ns
Full-Scale Tempco (Note)	TCI_{FS}		—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
		DAC-08E	—	—	—	—	—	±50	—	—	—	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale current change <1/2 LSB, $R_{OUT} > 20M\Omega$ typical	−10	—	+18	−10	—	+18	−10	—	+18	V
Full Range Current	I_{FR4}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$ $T_A = +25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4	—	±1	±8	—	±2	±16	μA
Zero-Scale Current	I_{ZS}		—	0.1	1	—	0.2	2	—	0.2	4	μA
Output Current Range	IOR_1	$R_{14}, R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$	2.1	—	—	2.1	—	—	2.1	—	—	mA
	IOR_2	$V_{REF} = +25.0V$, $V- = -12V$	4.2	—	—	4.2	—	—	4.2	—	—	mA
Output Current Noise		$I_{REF} = 2mA$	—	25	—	—	25	—	—	25	—	nA
Logic Input Levels												
Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input "1"	V_{IL}		2	—	—	2	—	—	2	—	—	V
Logic Input Current		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	—	−2	−10	—	−2	−10	—	−2	−10	μA
Logic Input "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	—	0.002	10	—	0.002	10	—	0.002	10	μA
Logic Input Swing	V_{IS}	$V- = -15V$	−10	—	+18	−10	—	+18	−10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$, (Note)	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	V
Reference Bias Current	I_{15}		—	−1	−3	—	−1	−3	—	−1	−3	μA
Reference Input Slew Rate	dI/dt	$R_{EQ} = 200\Omega$ See fast pulsed $R_L = 100\Omega$ ref. info. $C_C = 0pF$ following. (Note)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = 4.5V$ to $18V$	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	$V- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$

NOTE: Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-08/08A, $0°C \leq T_A \leq +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H MIN	DAC-08A/H TYP	DAC-08A/H MAX	DAC-08E MIN	DAC-08E TYP	DAC-08E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	—	−4.3	−5.8	—	−4.3	−5.8	
	I+	$V_S = +5V, -15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I−		—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I−		—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_d	$\pm 5V$, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		$+5V, -15V$, $I_{REF} = 2.0mA$	—	108	136	—	103	136	—	108	136	
		$\pm 15V$, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

ORDERING INFORMATION†

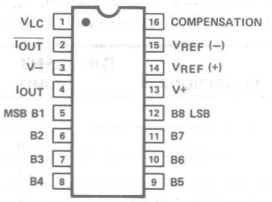
NL	16-PIN DUAL-IN-LINE PACKAGE HERMETIC	PLASTIC	LCC	OPERATING TEMPERATURE RANGE
0.1%	DAC08AQ*	—	—	MIL
	DAC08HQ	DAC08HP	—	COM
0.19%	DAC08Q*	—	DAC08RC/883	MIL
	DAC08EQ	DAC08EP	—	COM
0.39%	DAC08CQ	DAC08CP	—	COM
	—	DAC08CS††	—	

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

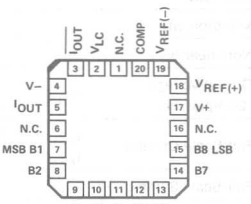
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

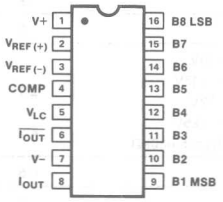
PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE (Q-Suffix)

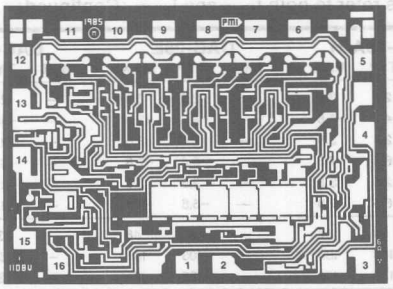


DAC-08RC/883 20-LEAD LCC (RC-Suffix)



16-LEAD SO (S-Suffix)

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.087 × 0.063 inch, 5,270 sq. mils
(2.209 × 1.60 mm, 3.54 sq. mm)

1. V_{LC}
2. $\overline{I_{OUT}}$
3. V−
4. I_{OUT}
5. BIT 1 (MSB)
6. BIT 2
7. BIT 3
8. BIT 4
9. BIT 5
10. BIT 6
11. BIT 7
12. BIT 8 (LSB)
13. V+
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 125°C$ for DAC-08NT, DAC-08GT devices; $T_A = 25°C$ for DAC-08N, DAC-08G and DAC-08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08NT LIMIT	DAC-08N LIMIT	DAC-08GT LIMIT	DAC-08G LIMIT	DAC-08GR LIMIT	UNITS
Resolution			8	8	8	8	8	Bits MIN
Monotonicity			8	8	8	8	8	Bits MIN
Nonlinearity	NL		±0.1	±0.1	±0.19	±0.19	±0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	V MAX V MIN
Full-Scale Current	I_{FS4} or I_{FS2}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full-Scale Symmetry	I_{FSS}		±8	±8	±8	±8	±16	μA MAX
Zero-Scale Current	I_{ZS}		2	2	4	4	4	μA MAX
Output Current Range	I_{FS1} or I_{FS2}	V− = −10V, V_{REF} = +15V V− = −12V, V_{REF} = +25V $R_{14}, R_{15} = 5.000k\Omega$	2.1 4.2	2.1 4.2	2.1 4.2	2.1 4.2	2.1 4.2	mA MIN mA MIN
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	2	2	2	V MIN
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	$V_{LC} = 0V$ $V_{IN} = -10V$ to +0.8V $V_{IN} = 2.0V$ to 18V	 ±10 ±10	 ±10 ±10	 ±10 ±10	 ±10 ±10	 ±10 ±10	 μA MAX
Logic Input Swing	V_{IS}	V− = −15V	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	V MAX V MIN
Reference Bias Current	I_{15}		−3	−3	−3	−3	−3	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V $I_{REF} = 1.0mA$	0.01	0.01	0.01	0.01	0.01	%FS/%V MAX
Power Supply Current	I+	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	174	174	174	174	174	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

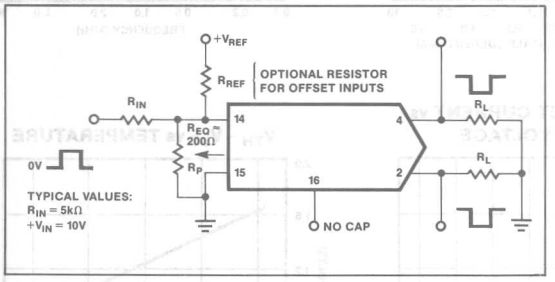
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2.0mA$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25°C$, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, $T_A = 25°C$	85	ns

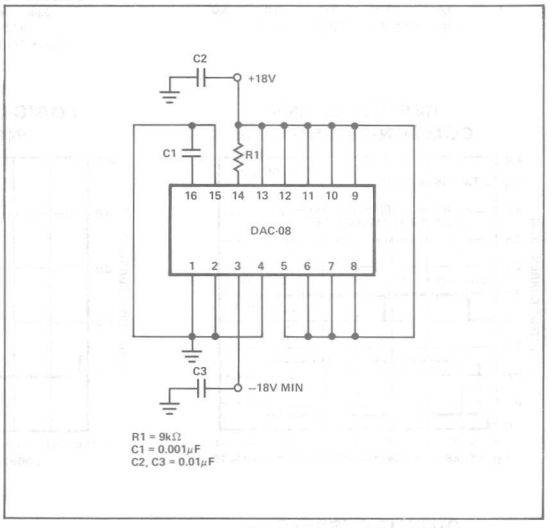
NOTE:
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.

2

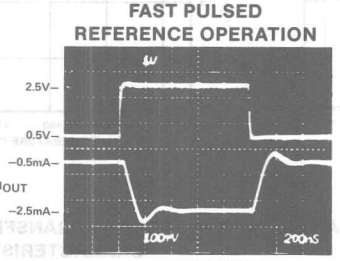
PULSED REFERENCE OPERATION



BURN-IN CIRCUIT

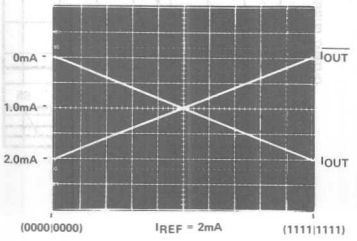


FAST PULSED REFERENCE OPERATION

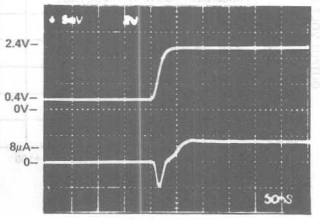


REQ ≈ 200Ω
RL = 100Ω
CC = 0
200NSEC/DIVISION

TRUE AND COMPLEMENTARY OUTPUT OPERATION

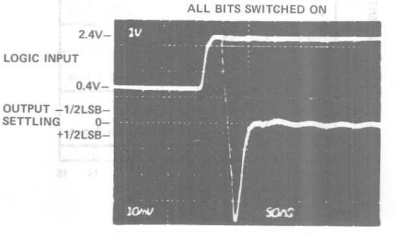


LSB SWITCHING



50NSEC/DIVISION

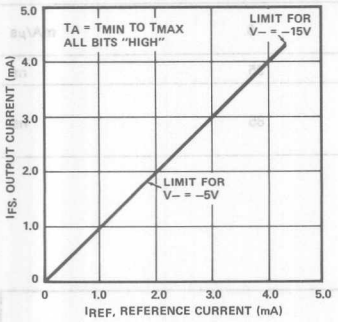
FULL-SCALE SETTLING TIME



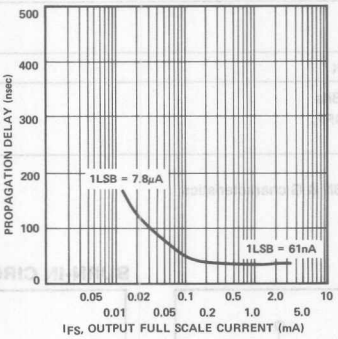
SETTLING TIME FIXTURE 50NSEC/DIVISION
IFS = 2mA, RL = 1kΩ
1/2LSB = 4μA

TYPICAL PERFORMANCE CHARACTERISTICS

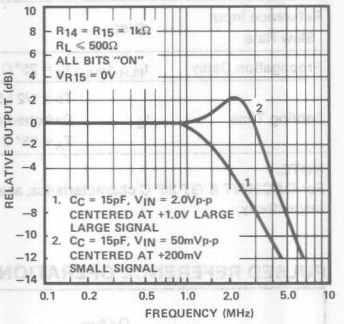
FULL-SCALE CURRENT vs REFERENCE CURRENT



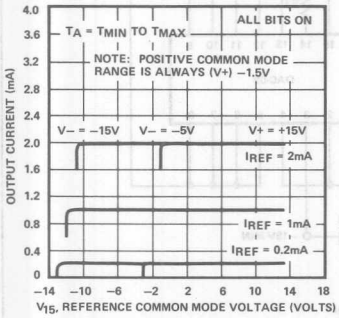
LSB PROPAGATION DELAY vs I_{FS}



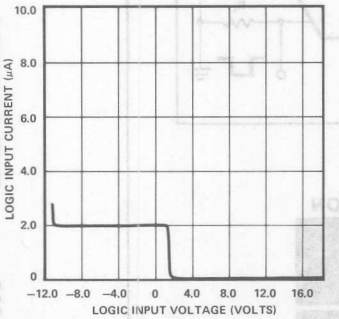
REFERENCE INPUT FREQUENCY RESPONSE



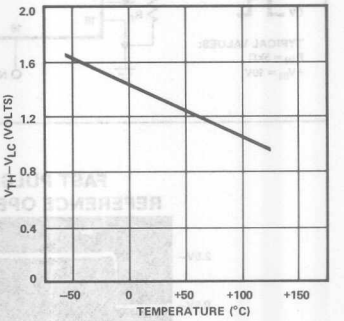
REFERENCE AMP COMMON-MODE RANGE



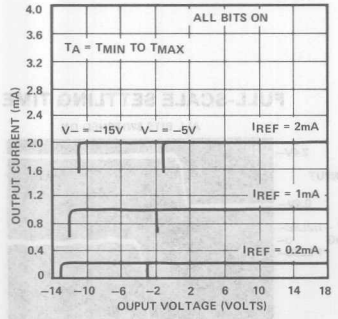
LOGIC INPUT CURRENT vs INPUT VOLTAGE



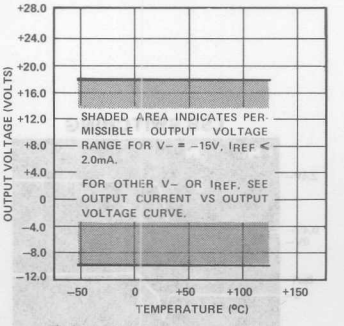
$V_{TH} - V_{LC}$ vs TEMPERATURE



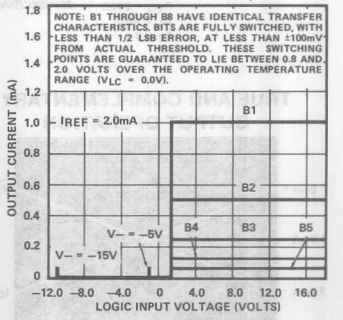
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE

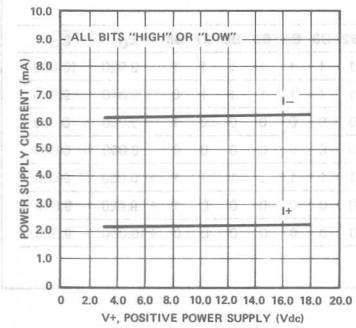


BIT TRANSFER CHARACTERISTICS

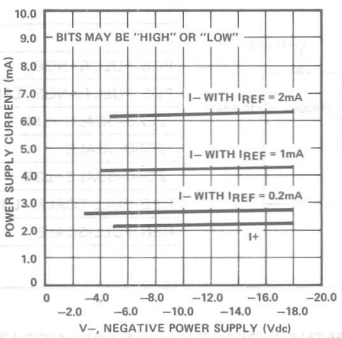


TYPICAL PERFORMANCE CHARACTERISTICS

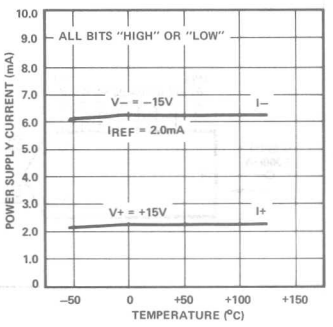
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V–



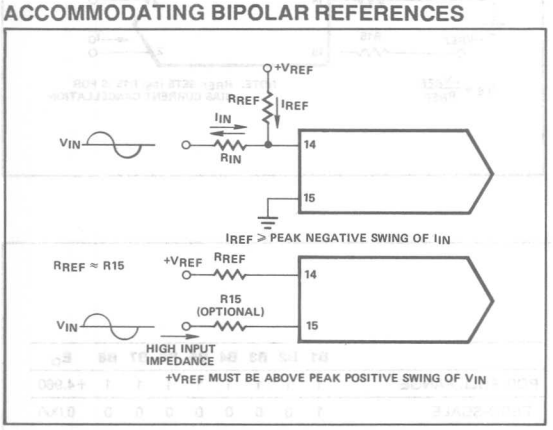
POWER SUPPLY CURRENT vs TEMPERATURE



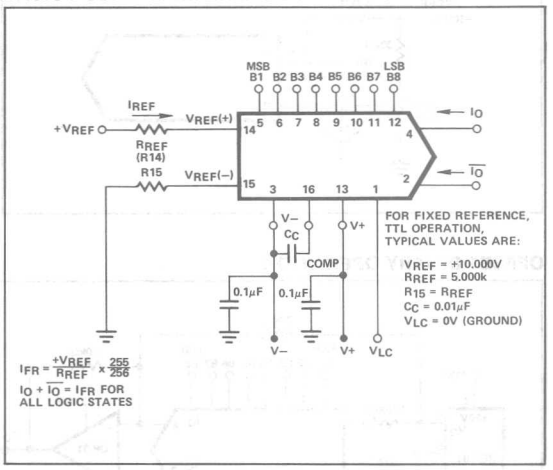
2

BASIC CONNECTIONS

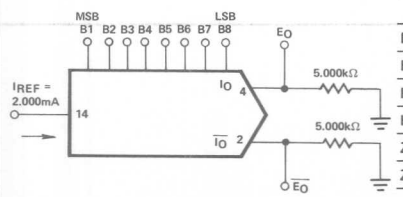
ACCOMMODATING BIPOLAR REFERENCES



BASIC POSITIVE REFERENCE OPERATION



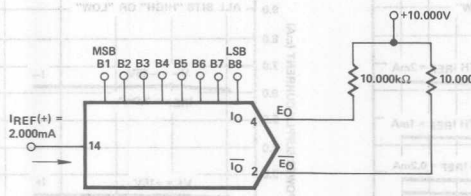
BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	− .000
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

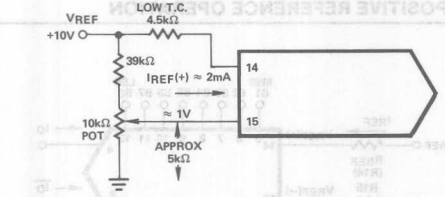
BASIC CONNECTIONS

BASIC BIPOLAR OUTPUT OPERATION

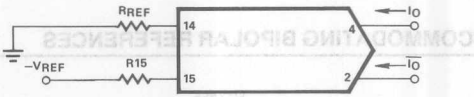


	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS. FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	+10.000
POS. FULL RANGE −LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
ZERO-SCALE +LSB	1	0	0	0	0	0	0	1	− 0.080	+ 0.160
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO-SCALE −LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG. FULL-SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	− 9.840
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



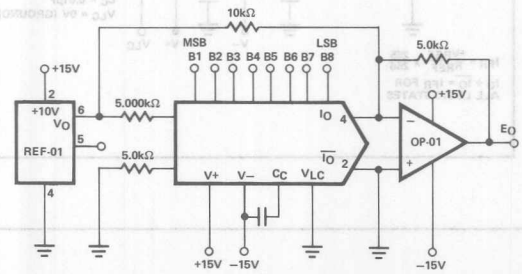
BASIC NEGATIVE REFERENCE OPERATION



$I_{FS} \approx \frac{-V_{REF}}{R_{REF}}$

NOTE. R_{REF} SETS I_{FS}; R15 IS FOR BIAS CURRENT CANCELLATION.

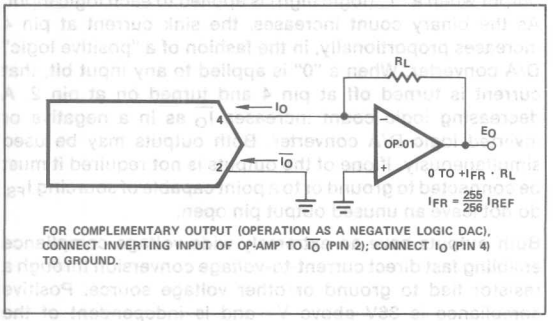
OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

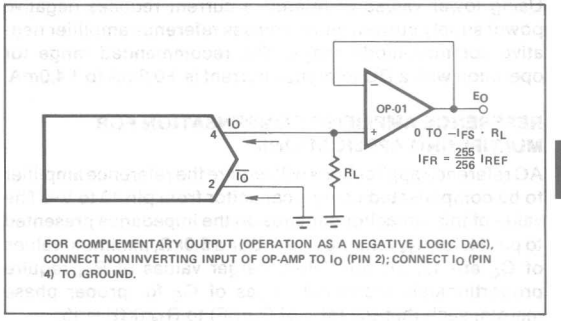
BASIC CONNECTIONS

POSITIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

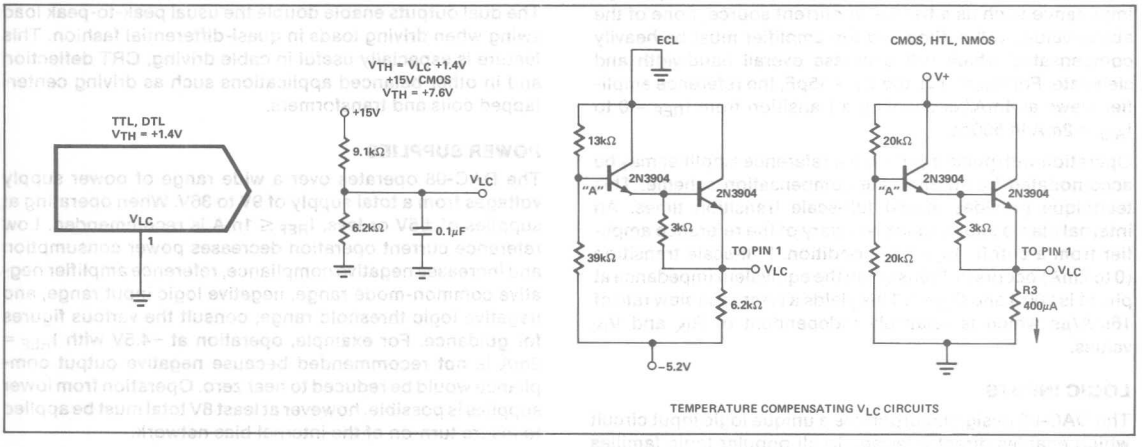
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NONINVERTING INPUT OF OP-AMP TO I_O (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

2

INTERFACING WITH VARIOUS LOGIC FAMILIES



TEMPERATURE COMPENSATING V_{LC} CIRCUITS

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V. The positive common-mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. if a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved

method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C(pF) to R_{14} (kΩ) = 15.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus (I_{REF} × 1kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} × 1kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq$ 1mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)(V+) + (I-)(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for min-

imum overall full-scale drift. Settling times of the DAC-08 decrease approximately 10% at −55° C; at +125° C an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended For variable reference applications, see previous section entitled "Reference Amplifier Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85ns at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

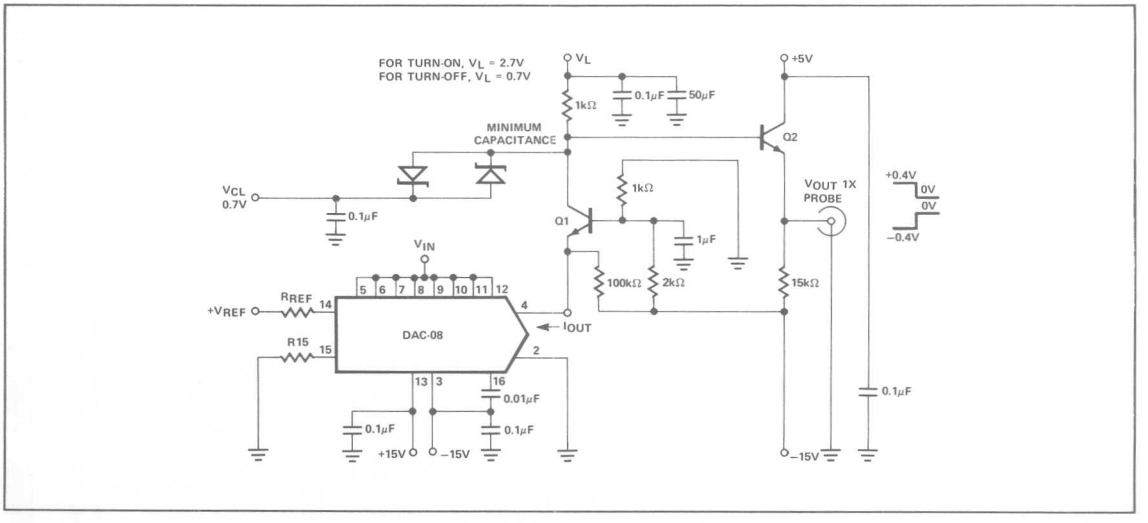
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

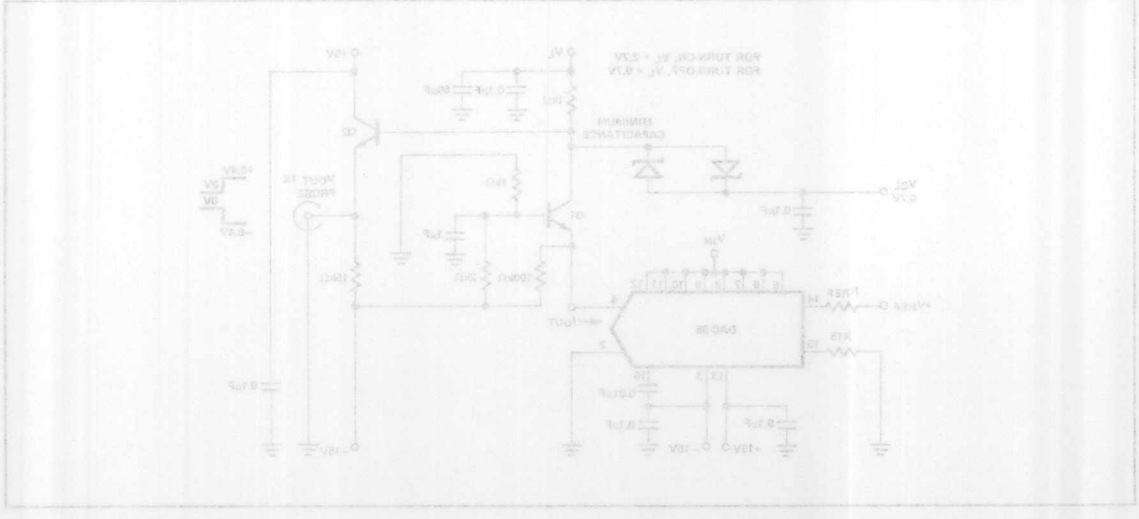
Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

SETTLING TIME MEASUREMENT





ANALOG DEVICES

10-Bit High-Speed Multiplying D/A Converter (Universal Digital Logic Interface)

DAC-10

FEATURES

- **Fast Settling 85ns**
- **Low Full-Scale Drift ..... 10ppm/°C**
- **Nonlinearity to 0.05% Max Over Temp Range**
- **Complementary Current Outputs ..... 0 to 4mA**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Wide Power Supply Range .. +5, −7.5 Min to ±18V Max**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**
- **Available in Die Form**

ORDERING INFORMATION †

	PACKAGE: 18-PIN CERDIP
NL LSB	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2	DAC10FX
±1	DAC10GX
±1	DAC10GS

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying digital-to-analog converters provide high-speed performance and full-scale accuracy.

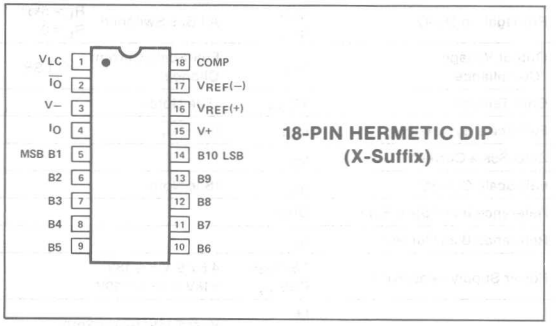
Advanced circuit design achieves 85ns settling times with very low 'glitch' energy and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable-threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as ±0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18V power supply range, with 85mW power consumption attainable at lower supplies.

A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

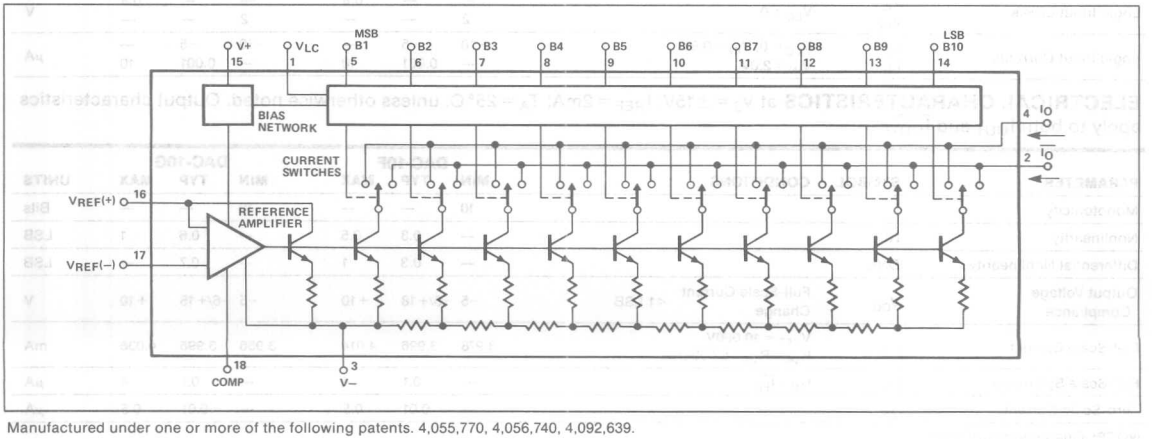
Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

PIN CONNECTIONS



18-PIN HERMETIC DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents. 4,055,770, 4,056,740, 4,092,639.

DAC-10

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
DAC-10FX, GX, GS ..... 0°C to +70°C
Junction Temperatre (T_j) ..... –65°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply 36V
Logic Inputs ..... V– to V– plus 36V
V_{LC} ..... V– to V+
Analog Current Outputs ..... +18V to –18V
Reference Inputs (V_{16} to V_{17}) ..... V– to V+
Reference Input Differential Voltage
(V_{16} to V_{17}) ..... ±18V
Reference Input Current (I_{16}) 2.5mA

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	84	15	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $0°C \le T_A \le 70°C$ FOR DAC-10F and G, unless otherwise noted.

Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

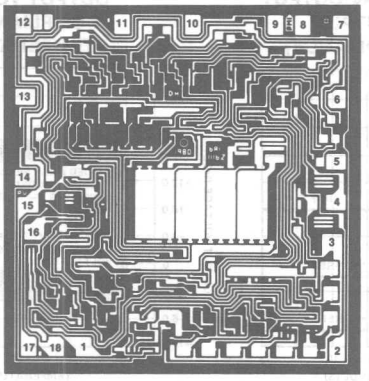
PARAMETER	SYMBOL	CONDITIONS	DAC-10F MIN	DAC-10F TYP	DAC-10F MAX	DAC-10G MIN	DAC-10G TYP	DAC-10G MAX	UNITS
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Settling Time	t_S	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)	—	85	135	—	85	150	ns
Output Capacitance	C_O		—	18	—	—	18	—	pF
Propagation Delay	t_{PLH} t_{PHL}	All Bits Switched $R_L = 5k\Omega$ $R_L = 0$	— —	50 50	— —	— —	50 50	— —	ns
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	— —	−5.5 +10	— —	— —	−5.5 +10	— —	V
Gain Tempco	TCI_{FS}	(See Note)	—	±10	±25	—	±10	±50	ppm/°C
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA
Full-Scale Current	I_{FR}	(See Note)	3.960	3.996	4.032	3.920	3.996	4.072	mA
Reference Input Slew Rate	DI/dt		—	6	—	—	6	—	mA/μs
Reference Bias Current	I_B		—	−1	−3	—	−1	−3	μA
Power Supply Sensitivity	$PSSI_{FS}^+$ $PSSI_{FS}^-$	$4.5V \le V+ \le 18V$ $-18V \le V- \le -10V$	— —	0.001 0.0012	0.01 0.01	— —	0.001 0.0012	0.01 0.01	$\%\Delta I_{FS}/\%\Delta V$
Power Supply Current	I+ I− I+ I−	$V_S = \pm 15V$; $I_{REF} = 2mA$ $V_S = +5V, -7.5V$; $I_{REF} = 1mA$	— — — —	2.3 −9 1.8 −5.9	4 −15 4 −9	— — — —	2.3 −9 1.8 −5.9	4 −15 4 −9	mA
Power Dissipation	P_d	$V_S = \pm 15V$; $I_{REF} = 2mA$ $V_S = +5V, -7.5V$; $I_{REF} = 1mA$	— —	231 85	285 88	— —	231 85	285 88	mW
Logic Input Levels	V_{IL} V_{IH}	$V_{LC} = 0$	— 2	— —	0.8 —	— 2	— —	0.8 —	V
Logic Input Currents	I_{IL} I_{IH}	$V_{LC} = 0$; $V_{IN} = 0.8V$ $V_{IN} = 2.0V$	−10 —	−5 0.001	— 10	−10 —	−5 0.001	— 10	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $T_A = 25°C$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10F MIN	DAC-10F TYP	DAC-10F MAX	DAC-10G MIN	DAC-10G TYP	DAC-10G MAX	UNITS
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	−5	−6/+18	+10	−5	−6/+15	+10	V
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$, $R_{14} = R_{15} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.091 × 0.087 inch, 7917 sq. mils
(2.311 × 2.210 mm, 5.107 sq. mm)

1. V_{LC} (LOGIC) THRESHOLD CONTROL
2. $\overline{I_O}$
3. V–
4. I_O
5. B1 (MSB)
6. B2
7. B3
8. B4
9. B5
10. B6
11. B7
12. B8
13. B9
14. B10 (LSB)
15. V+
16. V_{REF} (+)
17. V_{REF} (–)
18. COMPENSATION

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10N LIMIT	DAC-10G LIMIT	UNITS
Resolution			10	10	Bits MIN
Monotonicity			10	10	Bits MIN
Nonlinearity	NL		±0.5	±1	LSB MAX
Output Voltage Compliance	V_{OC}	True 1 LSB	+10 −5	+10 −5	V MAX V MIN
Output Current Range		I_{FS} ±3.996 MA	±18	±40	μA MAX
Zero-Scale Current	I_{ZS}	All Bits OFF	0.5	0.5	μA MAX
Logic Input "1"	V_{IH}	$I_{IN} = 100nA$	2	2	V MIN
Logic Input "0"	V_{IL}	V_{LC} @ Ground $I_{IN} = -100\mu A$	0.8	0.8	V MAX
Positive Supply Current	I+	V+ = 15V	4	4	mA MAX
Negative Supply Current	I–	V– = –15V	–15	–15	mA MAX

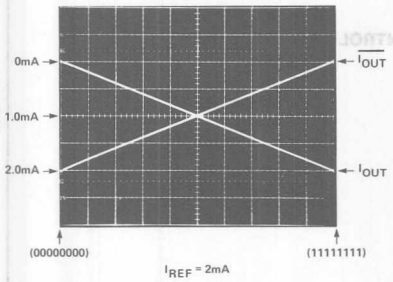
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

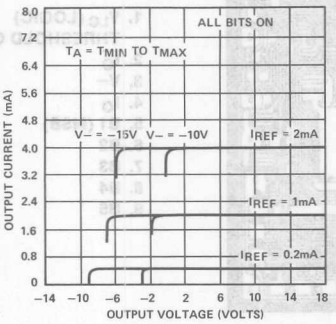
PARAMETER	SYMBOL	CONDITIONS	DAC-10N TYPICAL	DAC-10G TYPICAL	UNITS
Settling Time	t_S	To ±1/2 LSB When Output is Switched from 0 to FS	85	85	ns
Gain Temperature Coefficient (TC)		V_{REF} Tempco Excluded	±10	±10	ppm FS/°C
Output Capacitance			18	18	pF
Output Resistance			10	10	MΩ

TYPICAL PERFORMANCE CHARACTERISTICS

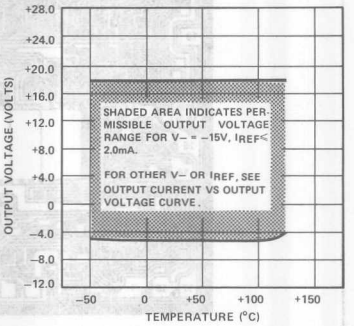
TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



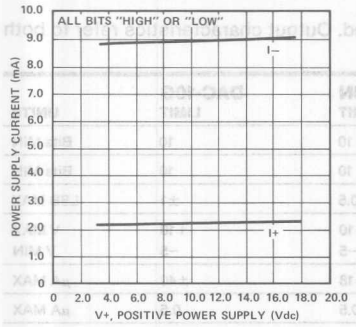
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



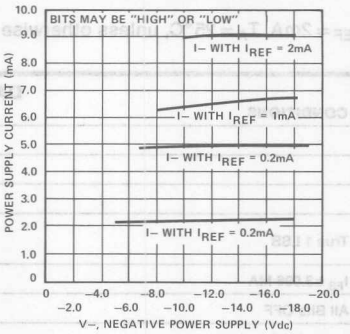
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



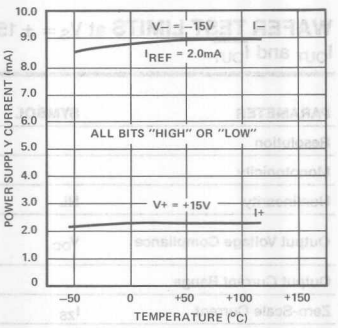
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V–

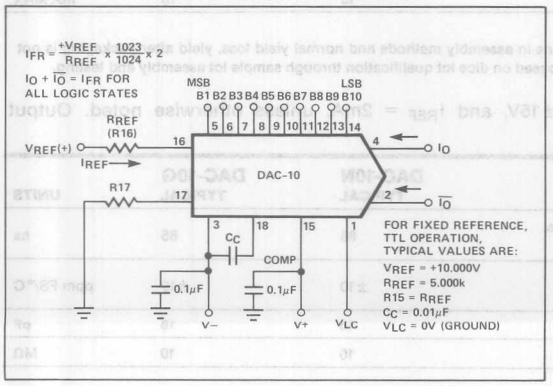


POWER SUPPLY CURRENT vs TEMPERATURE

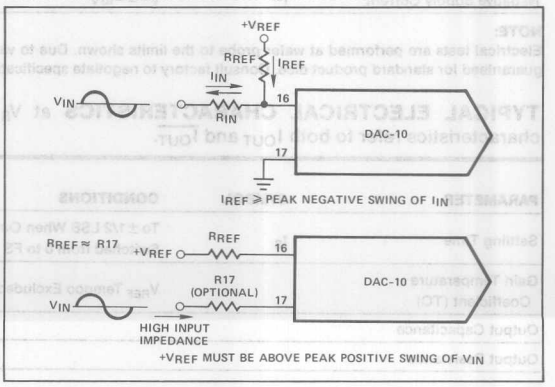


BASIC CONNECTIONS

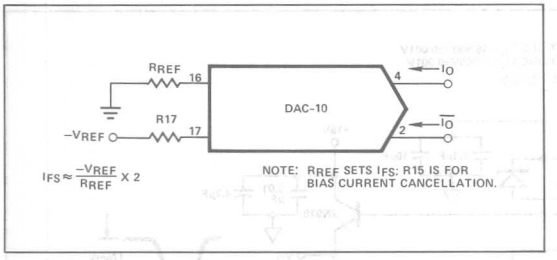
BASIC POSITIVE REFERENCE OPERATION



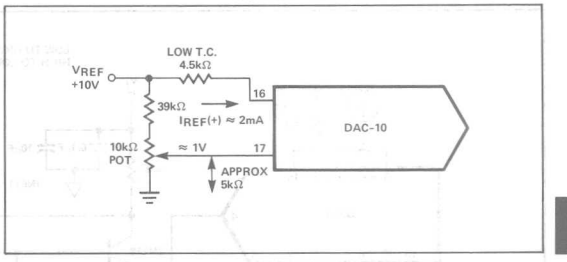
ACCOMMODATING BIPOLAR REFERENCES



BASIC NEGATIVE REFERENCE OPERATION

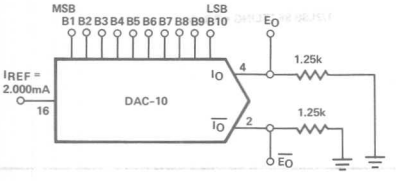


RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



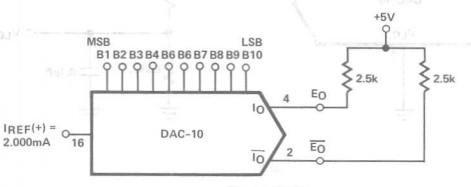
2

BASIC UNIPOLAR NEGATIVE OPERATION



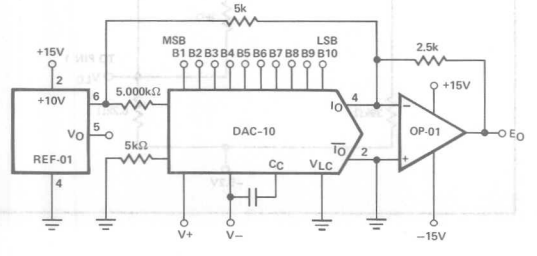
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	−4.995	−0.000
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	−2.505	−2.490
HALF-SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	−2.500	−2.495
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	−2.495	2.500
ZERO-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	−0.005	−4.990
ZERO-SCALE	0	0	0	0	0	0	0	0	0	0	0.000	3.996	−0.000	−4.995

BASIC BIPOLAR OUTPUT OPERATION



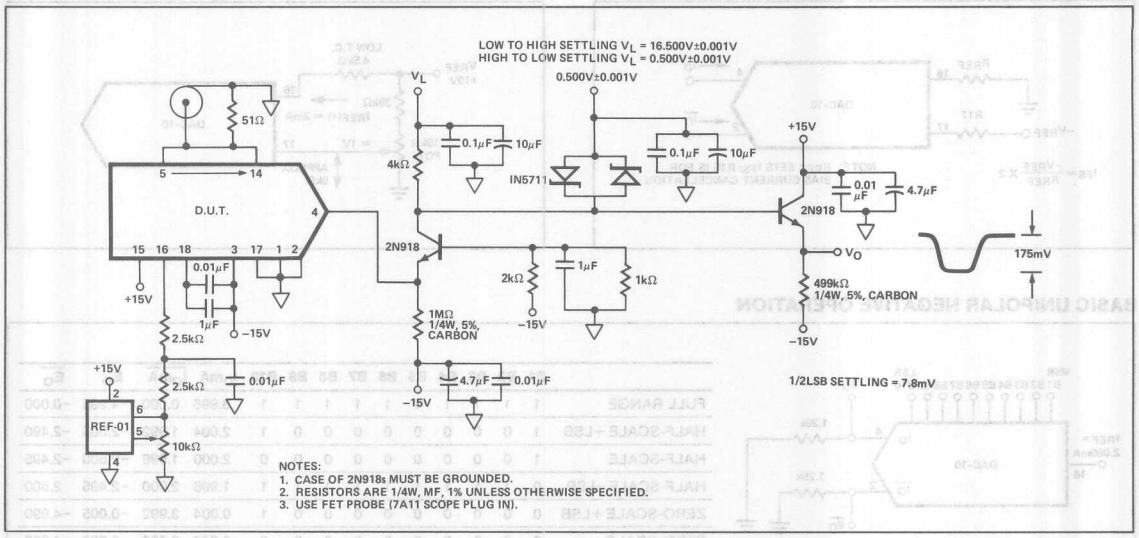
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O	$\overline{E_O}$
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	−4.990	+5.000
POS FULL RANGE −LSB	1	1	1	1	1	1	1	1	1	0	−4.980	+4.990
ZERO-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	−0.010	+0.020
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO-SCALE −LSB	1	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	−4.980
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	−4.990

OFFSET BINARY OPERATION

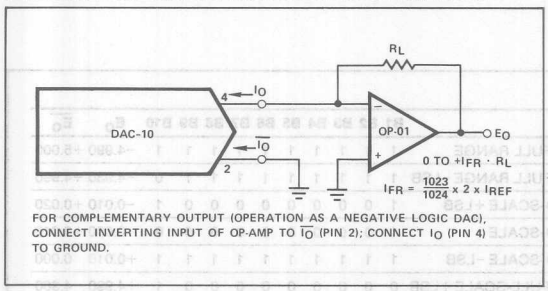


	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	−4.990
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	−5.000

SETTLING TIME MEASUREMENT

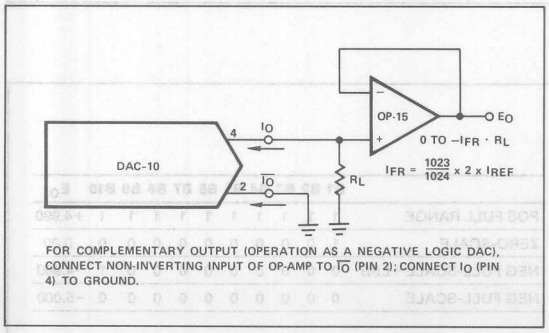


POSITIVE LOW IMPEDANCE OUTPUT OPERATION



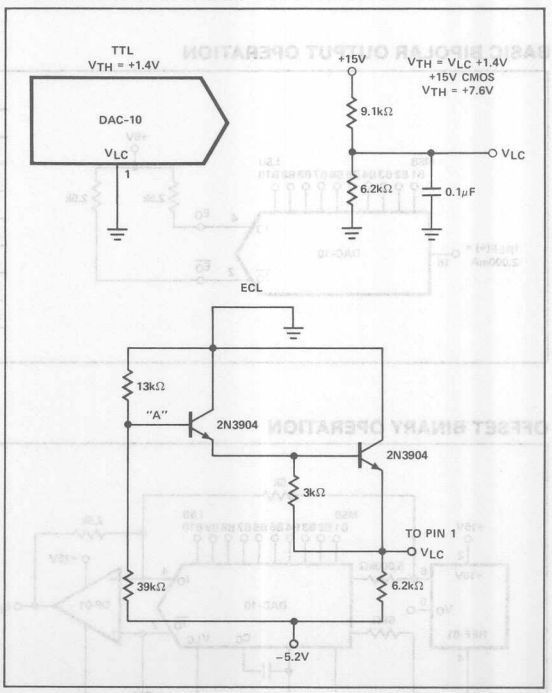
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

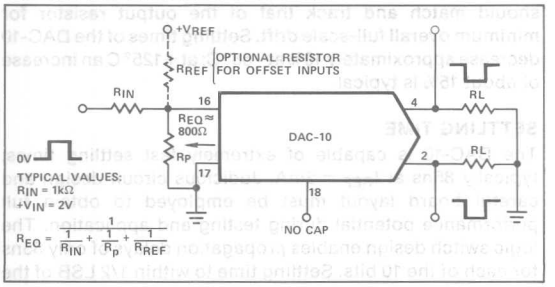


FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

INTERFACING WITH VARIOUS LOGIC FAMILIES



PULSED REFERENCE OPERATION



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the V_{REF} (+) terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (–) at pin 17; reference current flows from ground through R16 into V(+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 17. The negative common-mode range of the reference amplifier is given by: V_{CM}– = V– plus ($I_{REF} \times 2k\Omega$) plus 2V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 2mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V–. The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus ($I_{REF} \times 2k\Omega$) plus 3V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC}. For TTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1.1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V– and is independent of the positive supply. Negative compliance is +10V above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain within acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-10 decrease approximately 10% at –55° C; at +125° C an increase of about 15% is typical.

SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at I_{REF} = 2mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 130ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 4kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a 4kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 0111111111 to 1000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

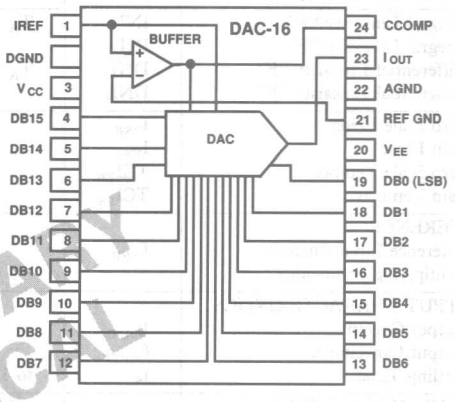
16-Bit, High Speed Multiplying DAC

DAC-16

FEATURES
- ±1 LSB Differential Linearity
- ±2 LSB Integral Linearity
- 500 ns Settling Time
- 4 mA Full-Scale Output
- 2 MHz Multiplying Bandwidth
- TTL/CMOS Compatible
- 10:1 Reference Input Range
- Monotonic over Full Temperature Range
- Available in Die Form

APPLICATIONS
- Communications
- Process Control
- Digital Attenuators
- Servos

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The DAC-16 is a 16-bit high speed, multiplying, current output digital-to-analog converter with a settling time of 500 ns max and a multiplying bandwidth of 2 MHz. A unique combination of low distortion, high signal-to-noise ratio, and high speed make the DAC-16 ideally suited to performing waveform synthesis and modulation in communications, instrumentation, and ATE systems. Input reference current is buffered with a gain of eight, resulting in a full-scale output current of 4 mA from a reference current of only 500 μA. The 16-bit parallel digital input bus is TTL/CMOS compatible. Operating from +5 V and −15 V supplies, the DAC-16 consumes 190 mW typ and is available in a 24-pin plastic skinny-DIP package and in die form.

For applications conforming to MIL-STD-883B, contact your local ADI sales office for DAC-16 specifications for operation over the −55°C to +125°C temperature range.

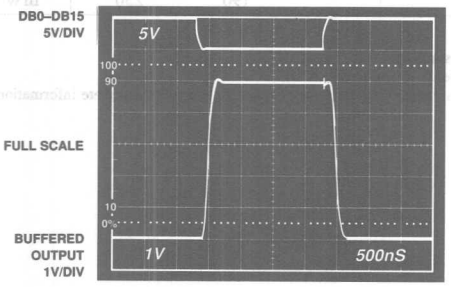


Figure 1. Full-Scale Transient Response

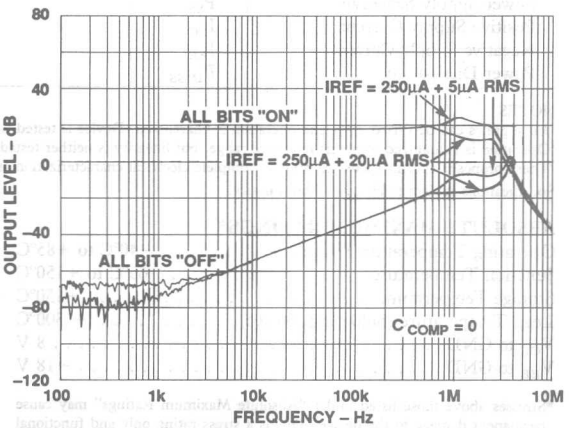


Figure 2. Multiplying Bandwidth

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter		Condition	Min	Typ	Max	Units
Integral Linearity "E"	INL	T_A = +25°C	−2	±1.2	+2	LSB
Integral Linearity "E"	INL		−4	±1.6	+4	LSB
Differential Linearity "E"	DNL	T_A = +25°C	−1	±.5	+1	LSB
Differential Linearity "E"	DNL		−1	±.7	+1.5	LSB
Integral Linearity "F"	INL	T_A = +25°C	−4	±1.4	+4	LSB
Integral Linearity "F"	INL		−6	±2	+6	LSB
Differential Linearity "F"	DNL	T_A = +25°C	−1	±.5	+1.5	LSB
Differential Linearity "F"	DNL		−1	±.6	+2	LSB
Zero Scale Error	I_{ZSE}				±2	LSB
Gain Error	I_{FSE}				0.3	% FS
Zero Scale Tempco	TCI_{ZE}			0.025		ppm/°C
Gain Tempco	TCI_{FS}			5		ppm/°C
REFERENCE[2]						
Reference Input Current	I_{REF}		50		500	μA
Multiplying Bandwidth		−3 dB		2		MHz
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}			+4		mA
Output Capacitance	C_{OUT}			10		pF
Settling Time	t_S	to 1 LSB		500		ns
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Input Current	I_{IN}	V_{IN} = 5.0 V, DB0–DB10			5	μA
Logic Input Current	I_{IN}	V_{IN} = 5.0 V, DB11–DB15			75	μA
Input Capacitance	C_{IN}			8		pF
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	P_{SS}				10	ppm/V
Positive Supply Current	I_{CC}			15	20	mA
Negative Supply Current	I_{EE}			7.5	10	mA
Power Dissipation	P_{DISS}			190	250	mW

PRELIMINARY TECHNICAL DATA

NOTES
[1]All supplies can be varied ±5% and operation is guaranteed. Device is tested with nominal supplies.
[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[3]These proposed specifications are prior to complete electrical characterization and are not guaranteed. Contact your local sales office for complete information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature Range . . . . . −40°C to +85°C
Junction Temperature . . . . . −65°C to +150°C
Storage Temperature . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . + 300°C
V_{CC} to GND . . . . . 8 V
V_{EE} to GND . . . . . −18 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

10-Bit Current-Output D/A Converter

DAC-100

2

FEATURES

- **Fast Settling ..... 225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable ..... Tempcos to ±15ppm/°C Max**
- **Commercial, Industrial and Military Models Available**
- **TTL Compatible Logic Inputs**
- **Wide Supply Range ..... ±6V to ±18V**
- **Available in Die Form**

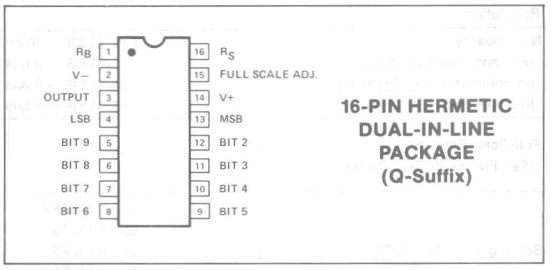
GENERAL DESCRIPTION

The DAC-100 is a complete 10-bit resolution digital-to-analog converter constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, matched bipolar offset and feedback resistors. Resistors are included for use with an external op amp for voltage output applications.

Although all units have 10-bit resolution, a wide choice of linearity and temperature coefficient options are provided to allow price/performance optimization.

The small size, wide operating temperature range, and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters.

PIN CONNECTIONS



16-PIN HERMETIC DUAL-IN-LINE PACKAGE (Q-Suffix)

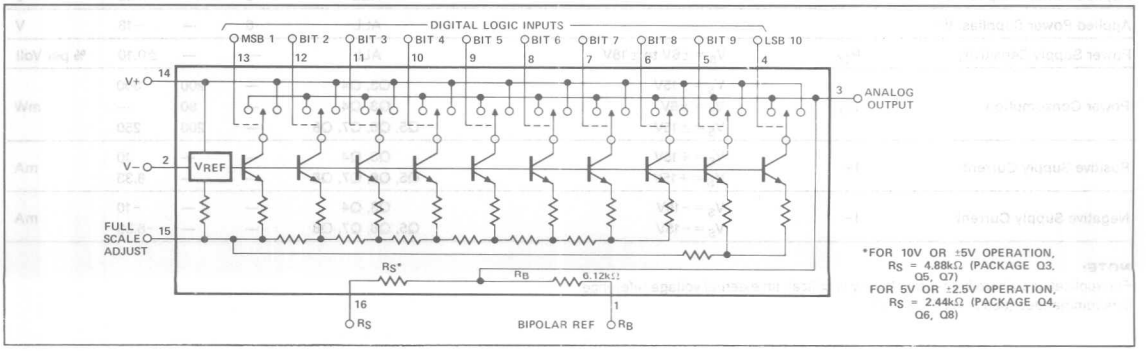
ORDERING INFORMATION †

N.L.* %FS MAX	TEMPCO* ppm/°C MAX	MILITARY TEMPERATURE V_O = ±5V/10V	MILITARY TEMPERATURE V_O = ±2.5V/5V	INDUSTRIAL TEMPERATURE V_O = ±5V/10V	INDUSTRIAL TEMPERATURE V_O = ±2.5V/5V	COMMERCIAL TEMPERATURE V_O = ±5V/10V	COMMERCIAL TEMPERATURE V_O = ±2.5V/5V
±0.05	±60	DAC100ACQ5/883	DAC100ACQ6/883	DAC100ACQ7	DAC100ACQ8	DAC100ACQ3	DAC100ACQ4
±0.10	±30	–	–	DAC100BBQ7	DAC100BBQ8	–	–
±0.10	±60	DAC100BCQ5/883	–	–	–	DAC100BCQ3	DAC100BCQ4
±0.20	±60	DAC100CCQ5/883	DAC100CCQ6/883	DAC100CCQ7	–	DAC100CCQ3	DAC100CCQ4
±0.30	±120	–	–	–	–	DAC100DDQ3	–

* Part number construction: The 1st letter following DAC-100 (A-D) refers to the nonlinearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ Supply to V– Supply ..... 0 to +36V
V+ Supply to Output ..... 0 to +18V
V– Supply to Output ..... 0 to –18V
Logic Inputs to Output ..... –1V to +6V
Operating Temperature Range Q3, Q4 ..... 0°C to +70°C
Q5, Q6, Q7, Q8 ..... –55°C to +125°C
Junction Temperature ..... –25°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W

NOTES:
1. Ratings apply to DICE and packaged parts, unless otherise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

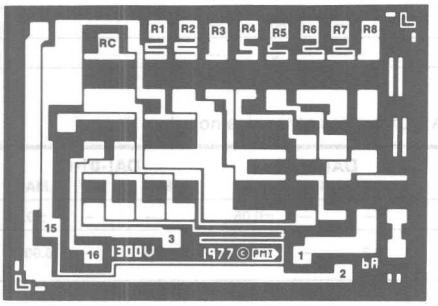
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for Q7 and Q8 devices; $0°C \le T_A \le +70°C$ for Q3 and Q4; $-55°C \le T_A \le +125°C$ for Q5 and Q6 devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-100	MIN	TYP	MAX	UNITS
Resolution				10	—	—	Bits
Nonlinearity (For nonlinearity/tempco combinations, see Ordering Information)	NL	(±1/2LSB — 10 bits)	A—	—	—	±0.05	%FS
		(±1/2LSB — 9 bits)	B—	—	—	±0.1	
		(±1/2LSB — 8 bits)	C—	—	—	±0.2	
		(±3/4LSB — 8 bits)	D—	—	—	±0.3	
Full-Scale Tempco (See Full-Scale Test Circuit)	T_C		—B	—	—	±30	ppm/°C
			—C	—	—	±60	
			—D	—	—	±120	
Settling Time $T_A = 25°C$	t_S	to ±0.05% FS	ALL	—	—	375	ns
		to ±0.1% FS	ALL	—	—	300	
		to ±0.2% FS	ALL	—	—	225	
		to ±0.4% FS	ALL	—	—	150	
		to ±0.8% FS	ALL	—	—	100	
Full-Range Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω Trimpot® between Adjust and V–)	V_{FR}	Connect FS Adjust to V– 10V Models (Q3, Q5, Q7) (See Full-Scale Test Circuit) 5V Models (Q4, Q6, Q8)		10	—	11.1	V
		$V_{IN} = 0.7V$ (See Basic Unipolar Voltage Output Circuit)		5	—	5.55	
Zero-Scale Output Voltage	V_{ZS}	$V_{IN} = 2.1V$	ALL	—	—	0.013	%FS
Logic Inputs: High	V_{INH}	Measured with respect to output pin	ALL	2.1	—	—	V
Logic Inputs: Low	V_{INL}	Measured with respect to output pin	ALL	—	—	0.7	V
Logic Input Current, Each Input	I_{IN}	$V_{IN} = 0$ to $+6V$	ALL	—	—	5	µA
Logic Input Resistance	R_{IN}	$V_{IN} = 0$ to $+6V$	ALL	—	3	—	mΩ
Logic Input Capacitance	C_{IN}		ALL	—	2	—	pF
Output Resistance	R_O		ALL	—	500	—	kΩ
Output Capacitance	C_O		ALL	—	13	—	pF
Applied Power Supplies: V+			ALL	+6	—	+18	V
Applied Power Supplies: V–			ALL	–6	—	–18	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 6V$ to $\pm 18V$	ALL	—	—	±0.10	% per Volt
Power Consumption	P_D	$V_S = \pm 15V$	Q3, Q4	—	200	300	mW
		$V_S = \pm 6V$	Q3, Q4	—	80	—	
		$V_S = \pm 15V$	Q5, Q6, Q7, Q8	—	200	250	
Positive Supply Current	I+	$V_S = +15V$	Q3, Q4	—	—	10	mA
		$V_S = +15V$	Q5, Q6, Q7, Q8	—	—	8.33	
Negative Supply Current	I–	$V_S = -15V$	Q3, Q4	—	—	–10	mA
		$V_S = -15V$	Q5, Q6, Q7, Q8	—	—	–8.33	

NOTE:
For applications where long-term stability is critical, an external voltage reference is recommended (see PMI REF-01/02).

DICE CHARACTERISTICS

DAR-01



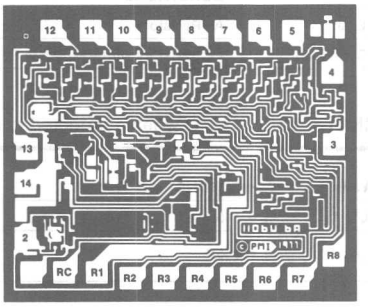
DIE SIZE .090 × .064 inch, 5760 sq. mils
(2.286 × 1.701 mm, 3.888 sq. mm)

1. R_B
2. V–
3. OUTPUT
15. FULL-SCALE ADJ
16. R_S

R — Pads are connected to similarly marked pads on DAI-01

Note: Pads 4 — 14, See DAI-01

DAI-01



DIE SIZE 0.080 x 0.067 inch, 5,360 sq. mils
(2.032 x 1.702 mm, 3.458 sq. mm)

2. V–
3. OUTPUT
4. BIT 10 (LSB)
5. BIT 9
6. BIT 8
7. BIT 7
8. BIT 6
9. BIT 5
10. BIT 4
11. BIT 3
12. BIT 2
13. BIT 1 (MSB)
14. V+

R — Pads are connected to similarly marked pads on DAR-01

Note: Pads 1, 2, 15, 16, See DAR-01

These die versions are available on special order; contact your PMI sales office.

WAFER TEST LIMITS at $T_A = 25°C$ for the R-2R Ladder Network comprised of R1—R8, R12, R23, R34, R45 and R56 when connected to an ideal DAI-01, unless otherwise noted.

		DAR-01-N			DAR-01-G			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Nonlinearity	VR1 = 3.2V	—	—	±0.035	—	—	±0.05	%

WAFER TEST LIMITS at $T_A = 25°C$, VR1 = 3.2V, unless otherwise noted.

		DAR-01			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resistance R1	Absolute Measurement	2.56	—	3.84	kΩ
Ratio RC1 to R1	Ideal = 1.00503 to 1	−1	—	+1	%
Ratio R1 to RS1	Ideal = 1.29959 to 1	−1	—	+1	%
Ratio R1 to RS2	Ideal = 1.29959 to 1	−1	—	+1	%
Ratio RB to R1	Ideal = 1.92211 to 1	−1	—	+1	%

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

PARAMETER	CONDITIONS	DAR-01 MIN	DAR-01 TYP	DAR-01 MAX	UNITS
Absolute Temperature Coefficient	All Resistors	—	±180	—	ppm/°C
Tracking Temperature Coefficient	All Resistors with Respect to R1	—	3	—	ppm/°C

WAFER TEST LIMITS at $T_A = 25°C$ when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAI-01-N MIN	DAI-01-N TYP	DAI-01-N MAX	DAI-01-G MIN	DAI-01-G TYP	DAI-01-G MAX	UNITS
Nonlinearity	NL	$V_S = \pm 15V$	—	—	±0.05	—	—	±0.1	%
Internal Reference Voltage	V_{MCR}	$V_S = \pm 15V$	6.6	—	6.900	6.6	—	6.900	V

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	CONDITIONS	DAI-01 MIN	DAI-01 TYP	DAI-01 MAX	UNITS
Resolution		10	—	10	Bits
Analog Output Current	All Bits Low, V– Connected to FS Adjust	1840	—	2274	μA
Zero-Scale Output Current	All Bits High, V– Connected to FS Adjust	—	—	±0.011	$\%I_{FS}$
Logic Input "0"	Measured with Respect to Output	—	—	0.7	V
Logic Input "1"	Measured with Respect to Output	2.1	—	—	V
Supply Current	All Bits High, V– Connected to FS Adjust	—	—	8.33	mA
Power Supply Rejection	$V_S = \pm 6V$ to $\pm 18V$	—	—	0.1	$\%I_{FS}/V$

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

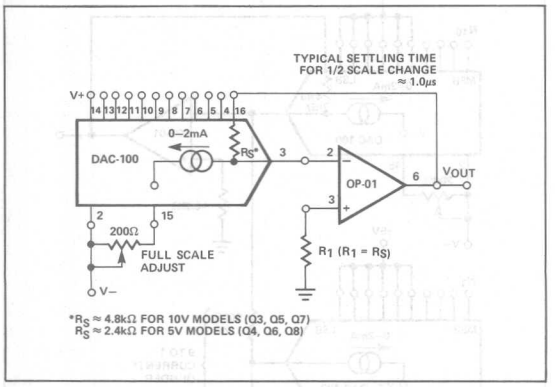
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	CONDITIONS	DAI-01-N MIN	DAI-01-N TYP	DAI-01-N MAX	DAI-01-G MIN	DAI-01-G TYP	DAI-01-G MAX	UNITS
Full-Scale Temperature Coefficient (Note)		—	±60	—	—	±60	—	ppm/°C

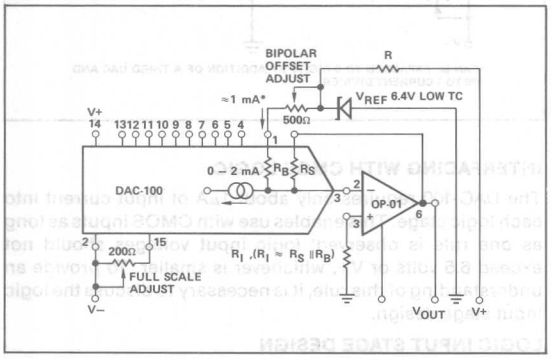
NOTE:
Full-Scale Temperature Coefficient is defined as the change in output voltage measured in the basic unipolar voltage output test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

BASIC CONNECTIONS

BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT



BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

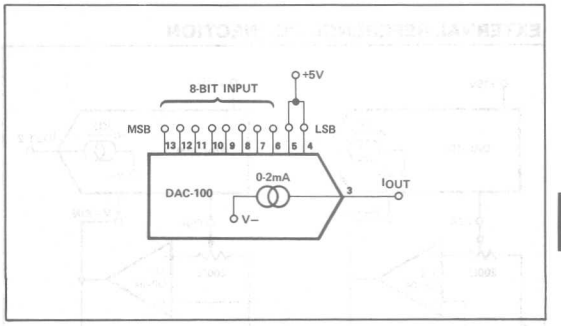


APPLICATIONS INFORMATION

FULL RANGE OUTPUT ADJUSTMENT — The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the full-scale adjust pin and V–. Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS — The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs **must** be tied to logic high for proper operation. "Floating" logic inputs can cause improper operation.

REDUCED RESOLUTION APPLICATION



LOGIC CODING — The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero-scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON".

LOGIC COMPATIBILITY — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

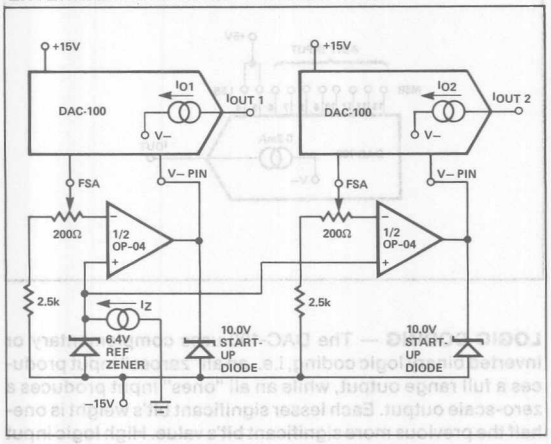
NONLINEARITY (NL) — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of full-scale range (FSR) or given in terms of LSB value. The end points are zero-scale output to full-scale output for unipolar operation and minus full-scale to positive full-scale for bipolar operation.

BIPOLAR OPERATION — The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

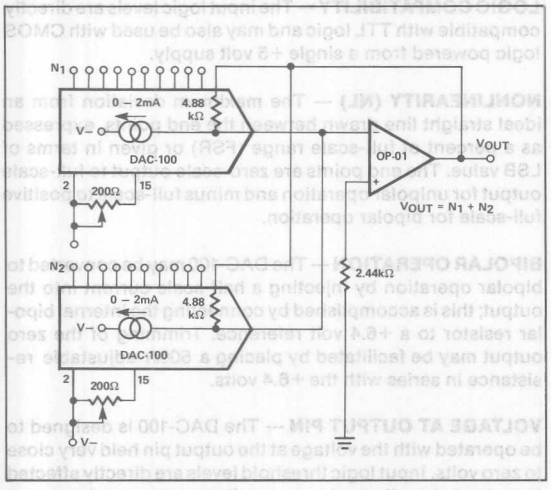
VOLTAGE AT OUTPUT PIN — The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output to ground is a convenient way of clamping the output to this limit.

TYPICAL APPLICATIONS

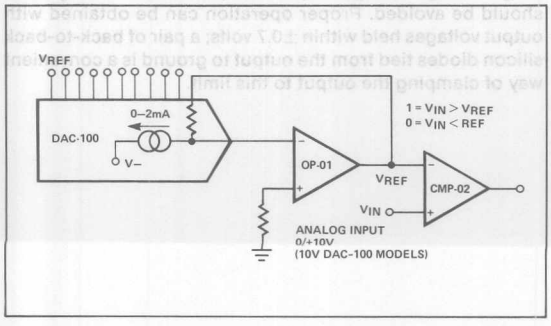
EXTERNAL REFERENCE CONNECTION



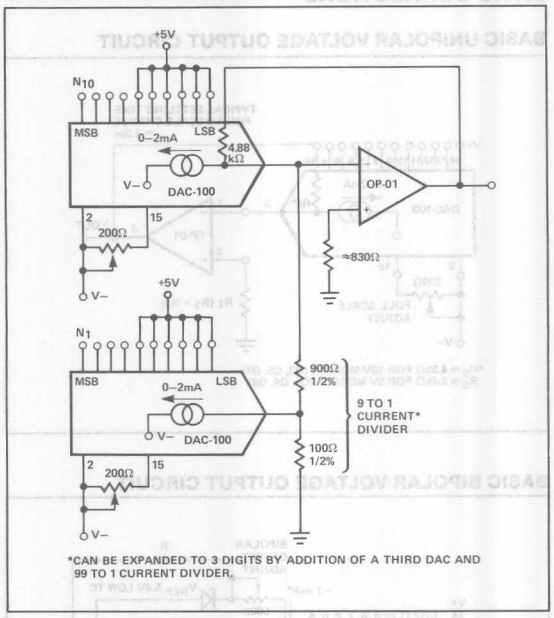
ANALOG SUM OF TWO DIGITAL NUMBERS



DIGITALLY PROGRAMMED LEVEL DETECTOR



BINARY-CODED-DECIMAL D/A CONVERSION



*CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC AND 99 TO 1 CURRENT DIVIDER.

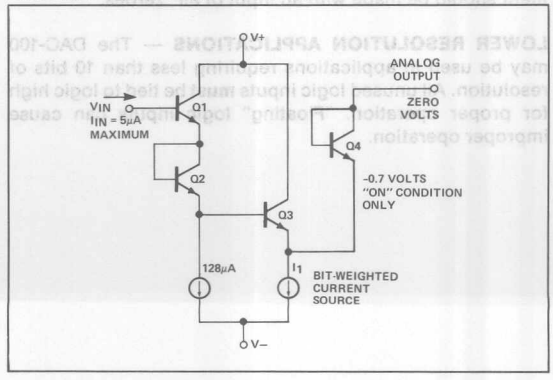
INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about 1μA of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

DAC-100 — LOGIC INPUT STAGE



Switching is accomplished by forward biasing Q4, diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

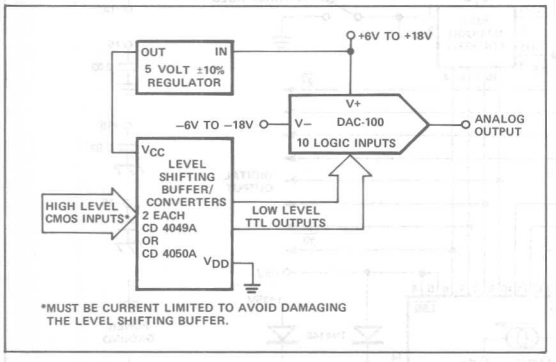
$$1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts the DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE



HIGH LEVEL CMOS INTERFACING

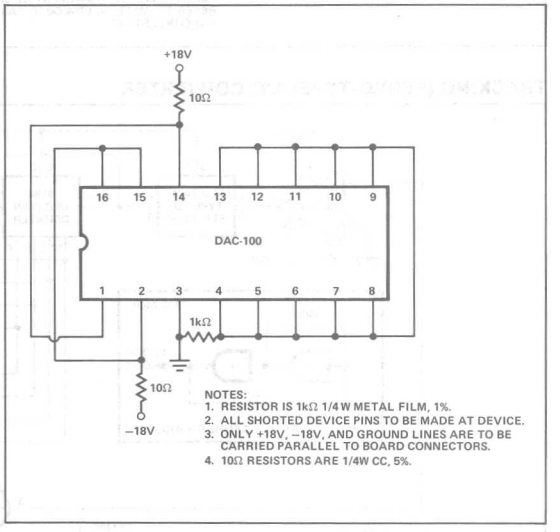
The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with the DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 to CMOS interfacing method to be used in either type of application.

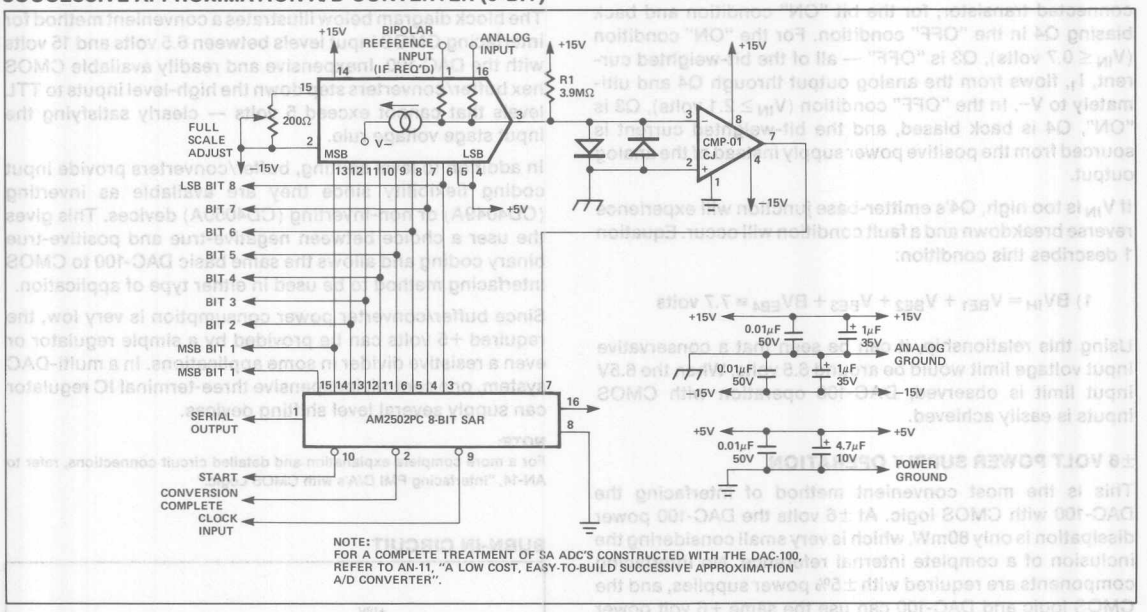
Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

NOTE:
For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."

BURN-IN CIRCUIT

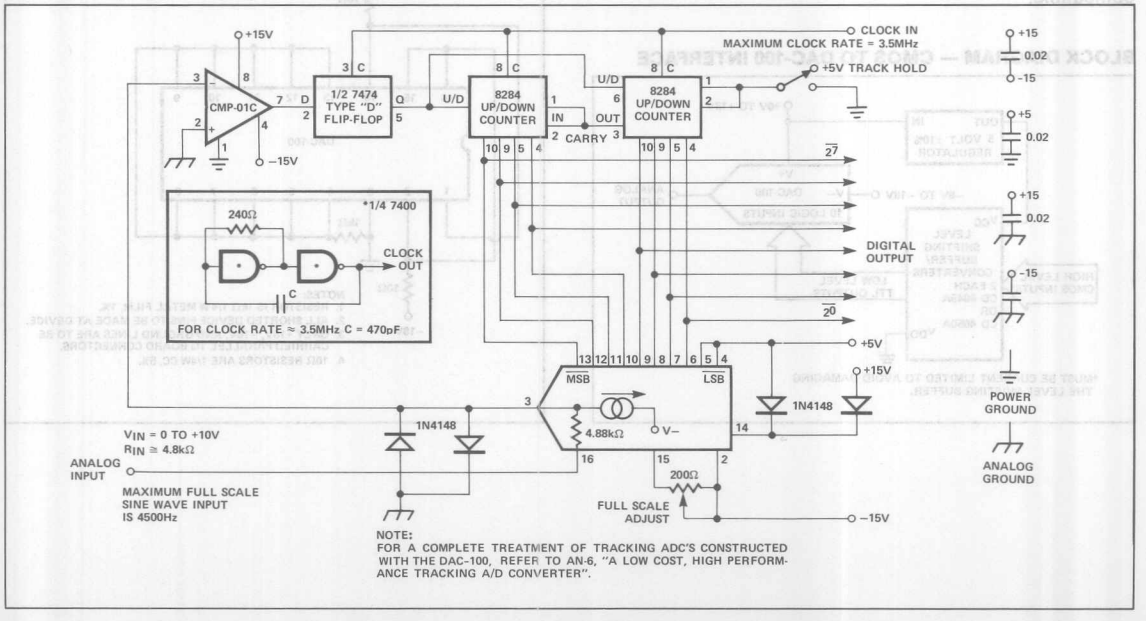


SUCCESSIVE APPROXIMATION A/D CONVERTER (8-BIT)



NOTE:
FOR A COMPLETE TREATMENT OF SA ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-11, "A LOW COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION A/D CONVERTER".

TRACKING (SERVO-TYPE) A/D CONVERTER



NOTE:
FOR A COMPLETE TREATMENT OF TRACKING ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-6, "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER".

DAC-312

FEATURES

- **Differential Nonlinearity** ..... ±1/2LSB
- **Nonlinearity** 0.05%
- **Fast Settling Time** 250ns
- **High Compliance** ..... −5V to +10V
- **Differential Outputs** ..... 0 to 4mA
- **Guaranteed Monotonicity** ..... 12 Bits
- **Low Full-Scale Tempco** ..... 10ppm/°C
- **Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS**
- **Low Power Consumption** 225mW
- **Industry Standard AM6012 Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

DNL	PACKAGE: CERDIP 20-PIN	PACKAGE: PLASTIC 20-PIN	OPERATING TEMPERATURE RANGE
±1/2LSB	DAC312ER*	–	COM
±1LSB	DAC312FR	–	XIND
±1LSB	DAC312HR	–	XIND
±1LSB	–	DAC312HP	XIND
±1LSB	–	DAC312HS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

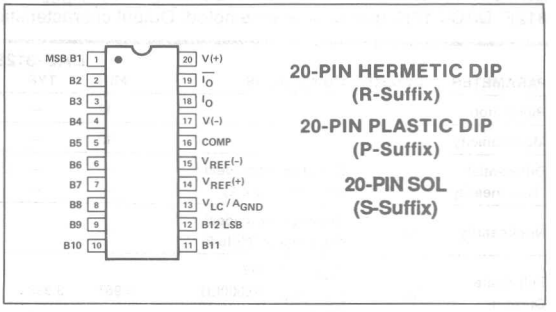
GENERAL DESCRIPTION

The DAC-312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

Based on the segmented design approach pioneered by PMI with the COMDAC® line of data converters, the DAC-312 combines a 9-bit master D/A converter with a 3-bit (MSB's) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

PIN CONNECTIONS

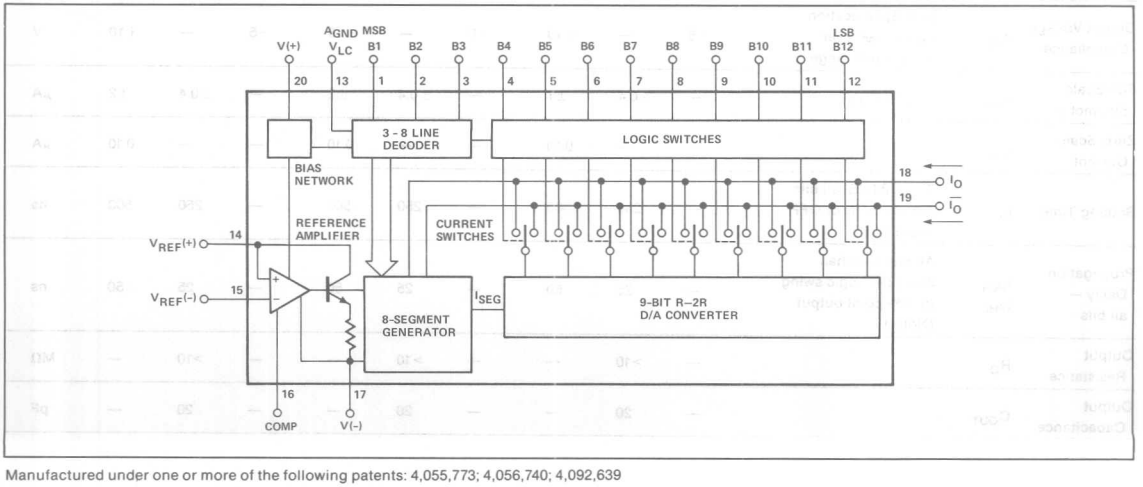


20-PIN HERMETIC DIP (R-Suffix)

20-PIN PLASTIC DIP (P-Suffix)

20-PIN SOL (S-Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

DAC-312

High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the DAC-312 along with an excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/−11V to ±18V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
- DAC-312E ..... 0°C to +70°C
- DAC-312F, DAC-312H ..... −40°C to +85°C

Junction Temperature ..... −65°C to +150°C
Storage Temperature (T_J) ..... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Power Supply Voltage ..... ±18V
Logic Inputs ..... −5V to +18V
Analog Current Outputs ..... −8V to +12V
Reference Inputs V_{14}, V_{15} ..... V− to V+
Reference Input Differential Voltage (V_{14}, V_{15}) ..... ±18V
Reference Input Current (I_{14}) 1.25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 1.0mA, 0°C ≤ T_A ≤ 70°C for DAC-312E and −40°C ≤ T_A ≤ +85°C for DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

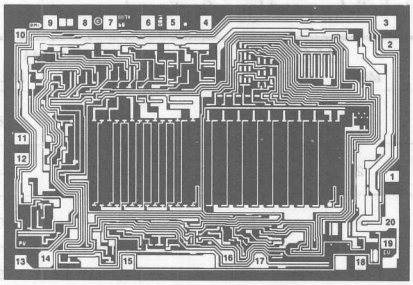
			DAC-312E			DAC-312F			DAC-312H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			12	—	—	12	—	—	12	—	—	Bits
Monotonicity			12	—	—	12	—	—	12	—	—	Bits
Differential Nonlinearity	DNL	Deviation from ideal step size (Note 2)	—	—	±0.0125	—	—	±0.0250	—	—	±0.0250	%FS
			—	—	±0.5	—	—	±1	—	—	±1	LSB
Nonlinearity	INL	Deviation from ideal straight line (Note 2)	—	—	±0.05	—	—	±0.05	—	—	±0.05	%FS
Full-Scale Current	I_{FS}	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ (Note 2)	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}		—	±5	±20	—	±10	±40	—	±80	—	ppm/°C
			—	±0.005	±0.002	—	±0.001	±0.004	—	±0.008	—	%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specification guaranteed over compliance range	−5	—	+10	−5	—	+10	−5	—	+10	V
Full-Scale Symmetry	I_{FSS}	$\lvert I_{FS} \rvert - \lvert \overline{I_{FS}} \rvert$	—	±0.4	±1	—	±0.4	±2	—	±0.4	±2	μA
Zero-Scale Current	I_{ZS}		—	—	0.10	—	—	0.10	—	—	0.10	μA
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF (Note 1)	—	250	500	—	250	500	—	250	500	ns
Propagation Delay — all bits	t_{PLH} t_{PHL}	All bits switched 50% point logic swing to 50% point output (Note 1)	—	25	50	—	25	50	—	25	50	ns
Output Resistance	R_O		—	>10	—	—	>10	—	—	>10	—	MΩ
Output Capacitance	C_{OUT}		—	20	—	—	20	—	—	20	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $0°C \le T_A \le 70°C$ for DAC-312E and $-40°C \le T_A \le +85°C$ for DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-312E MIN	DAC-312E TYP	DAC-312E MAX	DAC-312F MIN	DAC-312F TYP	DAC-312F MAX	DAC-312H MIN	DAC-312H TYP	DAC-312H MAX	UNITS
Logic Input Levels "0"	V_{IL}	V_{LC} = GND	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2	—	—	2	—	—	2	—	—	V
Logic Input Current	I_{IN}	V_{IN} = −5 to +18V	—	—	40	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}		−5	—	+18	−5	—	+18	−5	—	+18	V
Reference Bias Current	I_{15}		0	−0.5	−2	0	−0.5	−2	0	−0.5	−2	μA
Reference Input Slew Rate	dI/dt	$R_{14(eq)} = 800\Omega$ C_C = 0pF (Note 1)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5V to +16.5V, V− = −15V	—	±0.0005	±0.001	—	±0.0005	±0.001	—	±0.0005	±0.001	%FS/%ΔV
	$PSSI_{FS-}$	V− = −13.5V to −16.5V, V+ = +15V	—	±0.00025	±0.001	—	±0.00025	±0.001	—	±0.00025	±0.001	
Power Supply Range	V+	V_{OUT} = 0V	4.5	—	18	4.5	—	18	4.5	—	18	V
	V−		−18	—	−10.8	−18	—	−10.8	−18	—	−10.8	
Power Supply Current	I+	V+ = +5V, V− = −15V	—	3.3	7	—	3.3	7	—	3.3	7	mA
	I−		—	−13.9	−18	—	−13.9	−18	—	−13.9	−18	
	I+	V+ = +15V, V− = −15V	—	3.9	7	—	3.9	7	—	3.9	7	
	I−		—	−13.9	−18	—	−13.9	−18	—	−13.9	−18	
Power Dissipation	P_d	V+ = +5V, V− = −15V	—	225	305	—	225	305	—	225	305	mW
		V+ = +15V, V− = −15V	—	267	375	—	267	375	—	267	375	

NOTES:
1. Guaranteed by design.
2. T_A = 25°C for DAC-312H grade only.

DICE CHARACTERISTICS



1. B1 (MSB)	11. B11
2. B2	12. B12 (LSB)
3. B3	13. V_{LC}/A_{GND}
4. B4	14. V_{REF} (+)
5. B5	15. V_{REF} (−)
6. B6	16. COMP
7. B7	17. V−
8. B8	18. I_O
9. B9	19. $\overline{I_O}$
10. B10	20. V+

DIE SIZE 0.141 × 0.096 inch, 13,536 sq. mils (3.58 × 2.44 mm, 8.74 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-312N LIMIT	DAC-312G LIMIT	UNITS
Resolution			12	12	Bits MIN
Monotonicity			12	12	Bits MIN
Nonlinearity			±0.05	±0.05	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1/2 LSB	+10 −5	+10 −5	V MAX V MIN
Full-Scale Current		$V_{REF} = 10.000V$ $R_{14}, R_{15} = 10.000k\Omega$	4.031 3.967	4.063 3.935	mA MAX mA MIN
Full-Scale Symmetry	I_{FSS}		±1	±2	μA MAX
Zero-Scale Current	I_{ZS}		0.1	0.1	μA MAX
Differential Nonlinearity	DNL	Deviation from ideal step size	±0.012 ±1/2	±0.025 ±1	%FS MAX Bits (LSB) MAX
Logic Input Levels "0"	V_{IL}	V_{LC} = GND	0.8	0.8	V MAX
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2	2	V MIN
Logic Input Swing	V_{IS}		+18 −5	+18 −5	V MAX V MIN
Reference Bias Current	I_{15}		−2	−2	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = +13.5V to +16.5V, V− = −15V V− = −13.5V to −16.5V, V+ = +15V	±0.001 ±0.001	±0.001 ±0.001	%/% MAX
Power Supply Current	I+ I−	$V_S = \pm 15V$ $I_{REF} \leq 1.0mA$	7 −18	7 −18	mA MAX
Power Dissipation	P_D	$V_S = +15V$ $I_{REF} \leq 1.0mA$	375	375	mW MAX

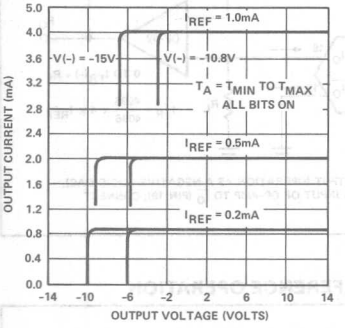
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C; $V_S = \pm 15V$, and $I_{REF} = 1.0mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

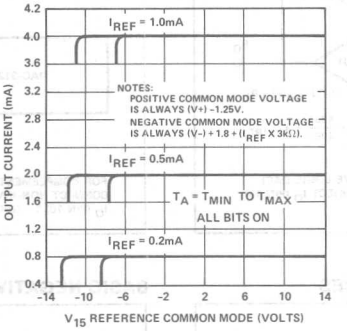
PARAMETER	SYMBOL	CONDITIONS	DAC-312N TYPICAL	DAC-312G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	25	25	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF.	250	250	ns
Full-Scale	TC_{IFS}		±10	±10	ppm/°C

TYPICAL PERFORMANCE CHARACTERISTICS

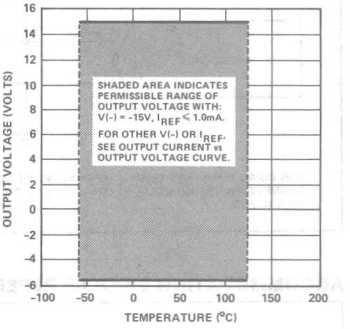
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



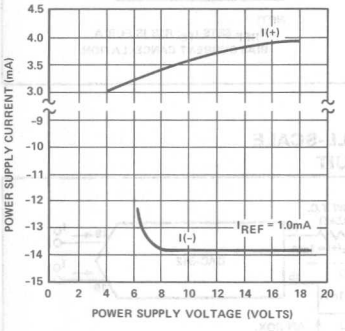
REFERENCE AMPLIFIER COMMON-MODE RANGE



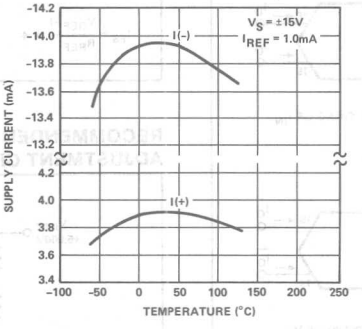
OUTPUT COMPLIANCE vs TEMPERATURE



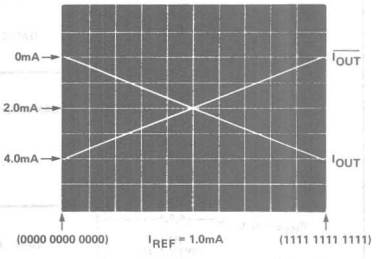
POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



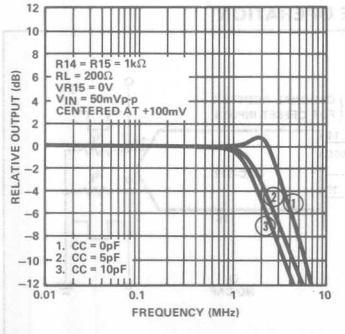
POWER SUPPLY CURRENT vs TEMPERATURE



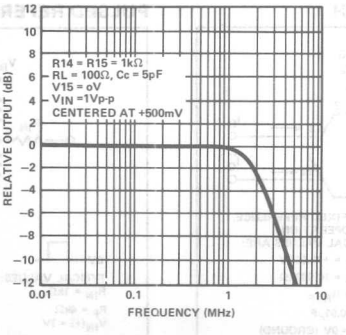
TRUE AND COMPLEMENTARY OUTPUT OPERATION



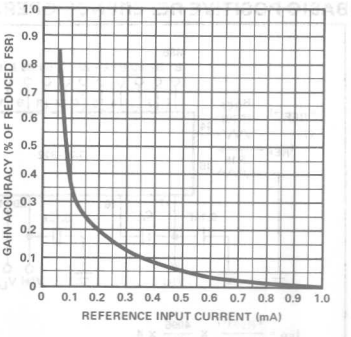
REFERENCE AMPLIFIER SMALL-SIGNAL FREQUENCY RESPONSE



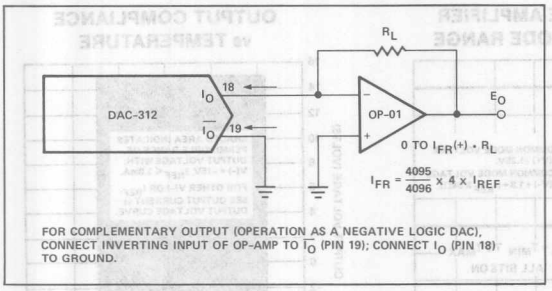
REFERENCE AMPLIFIER LARGE-SIGNAL FREQUENCY RESPONSE



GAIN ACCURACY vs REFERENCE CURRENT

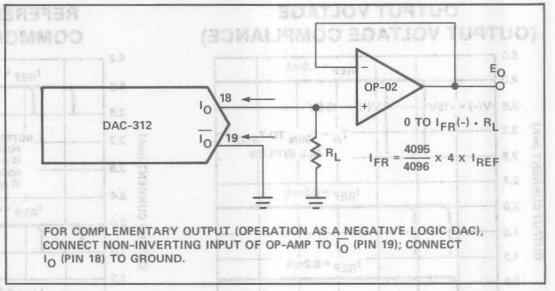


NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



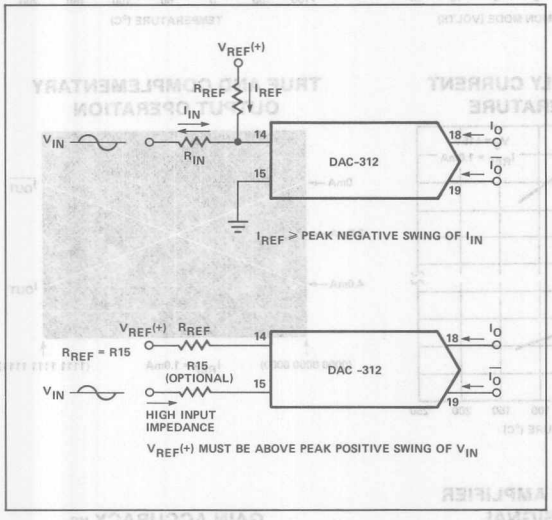
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

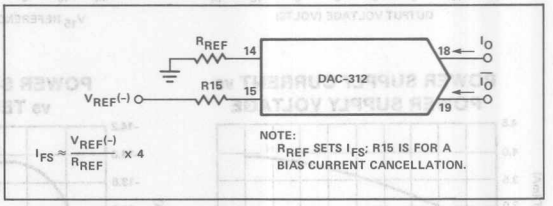


FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

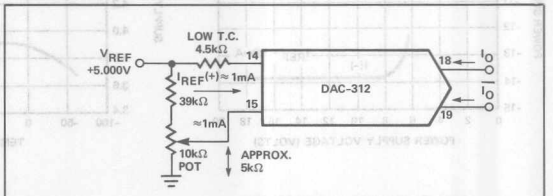
ACCOMMODATING BIPOLAR REFERENCES



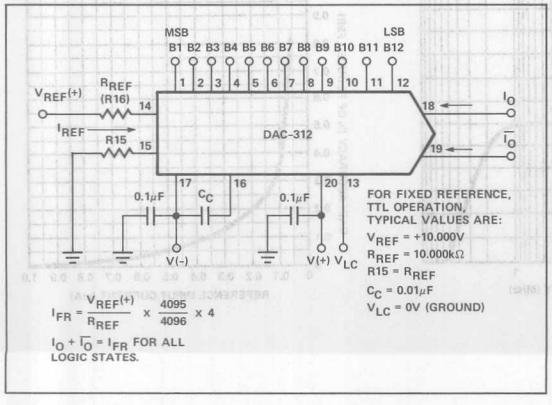
BASIC NEGATIVE REFERENCE OPERATION



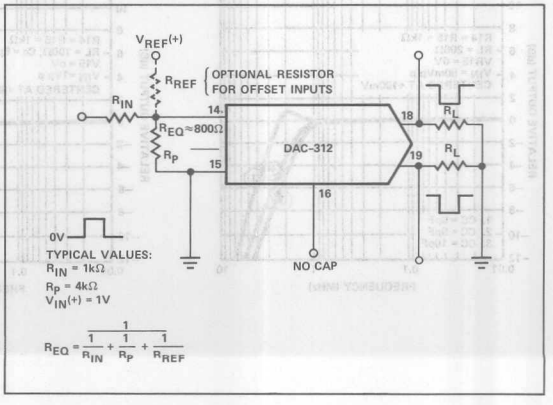
RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



BASIC POSITIVE REFERENCE OPERATION

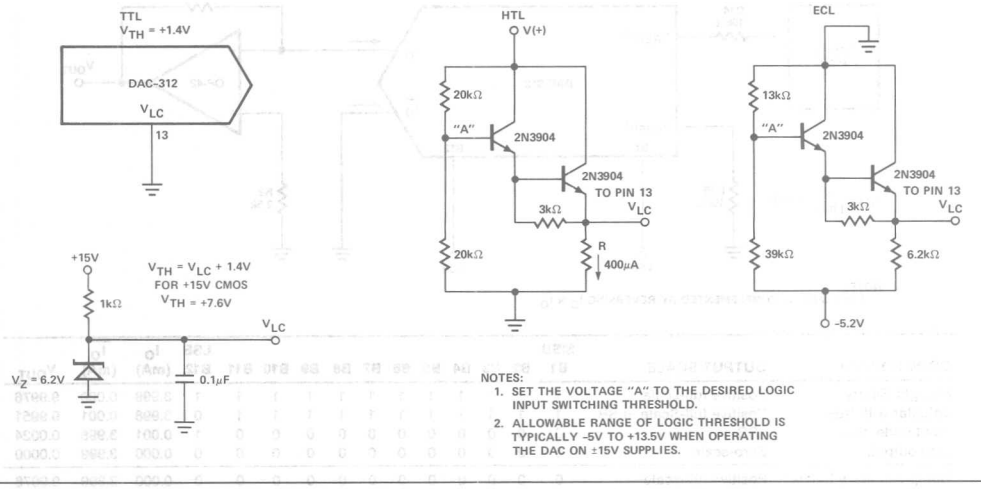


PULSED REFERENCE OPERATION



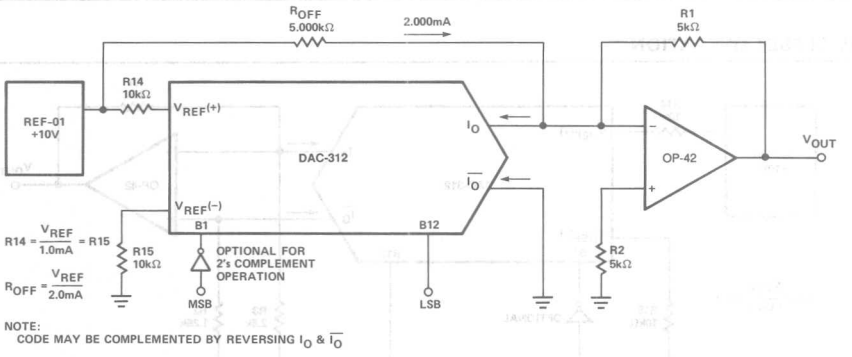
BASIC CONNECTIONS

INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTES:
1. SET THE VOLTAGE "A" TO THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13.5V WHEN OPERATING THE DAC ON ±15V SUPPLIES.

BIPOLAR OFFSET (TRUE ZERO)

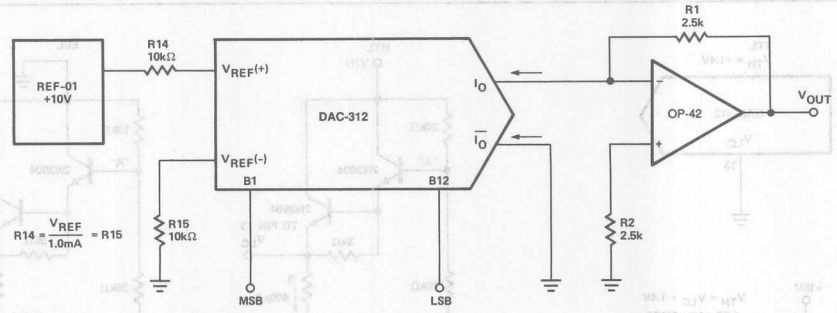


NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Offset binary;	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output.	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	−LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0049
	Negative full-scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000
2's complement;	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
MSB complemented	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
(Need inverter at B1).	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0049
	Negative full-scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000

BASIC CONNECTIONS

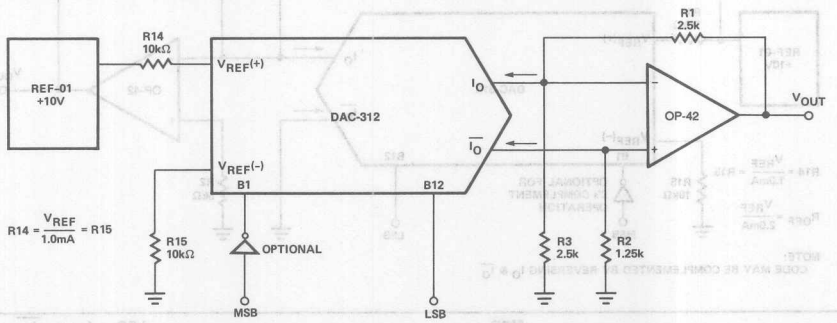
BASIC UNIPOLAR OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight Binary;	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
unipolar with true	Positive full-Scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
input code, true	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
zero output.	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary binary;	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
unipolar with	Positive full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
complementary input	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
code, true zero output.	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight offset binary;	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.00	9.9976
symmetrical about zero,	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(−) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
	Negative full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
1's complement;	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
MSB complemented	(−) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
(need inverter at B1).	Negative full-scale −LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM}– = V– plus (I_{REF} X 3kΩ) plus 1.23V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA. Although some degradation of gain accuracy will be realized at reduced values of I_{REF}. (See Gain Accuracy vs Reference Current).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14 for R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –5 and +10V. This enables direct interface with +15V CMOS logic, even when the DAC-312 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by : V– plus (I_{REF} X 3kΩ) plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 7mA typical; external circuitry should be designed to accommodate this current.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-312 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1$mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −9V with $I_{REF} =$ 1mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-312 are guaranteed to apply over the entire rated operating temperature range. Full-Scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-312 decrease approximately 10% at −55° C; at +125° C an increase of about 15% is typical.

SETTLING TIME

The DAC-312 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0$mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the DAC-312 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of the settling time requires the ability to accurately resolve ±1/2 LSB of current, which is ±500nA for 4mA FSR. In order to assure the measurement is of the actual settling time and not the R.C. time of the output network, the resistive termination on the output of the DAC must be 500 ohms or less. This does, however, place certain limitations on the testing apparatus. At I_{REF} values of less than 0.5mA, it is difficult to prevent RC damping of the output and maintain adequate sensitivity. Because the DAC-312 has 8 equal current sources for the 3 most significant bits, the major carry occurs at the code change of 000111111111 to 111000000000. The worst case settling time occurs at the zero to full-scale transition and it requires 9.2 time constants for the DAC output to settle to within ±1/2 LSB (0.0125%) of its final value.

The DAC-312 switching transients or "glitches" are on the order of 500mV-ns. This is most evident when switching through the major carry and may be further reduced by adding small capacitive loads at the output with a minor sacrifice in transition speeds.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

DIFFERENTIAL vs INTEGRAL NONLINEARITY

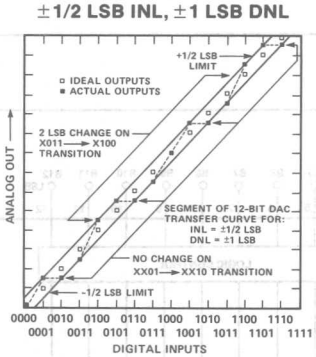
Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Drive." On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2 LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

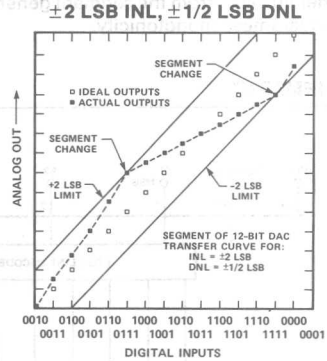
2

DIFFERENTIAL LINEARITY COMPARISON

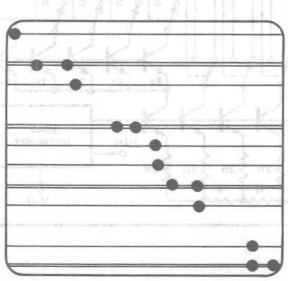
D/A CONVERTER WITH ±1/2 LSB INL, ±1 LSB DNL



D/A CONVERTER WITH ±2 LSB INL, ±1/2 LSB DNL

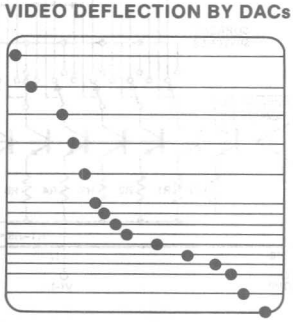


VIDEO DEFLECTION BY DACs



ENLARGED "POSITIONAL" OUTPUTS

VIDEO DEFLECTION BY DACs



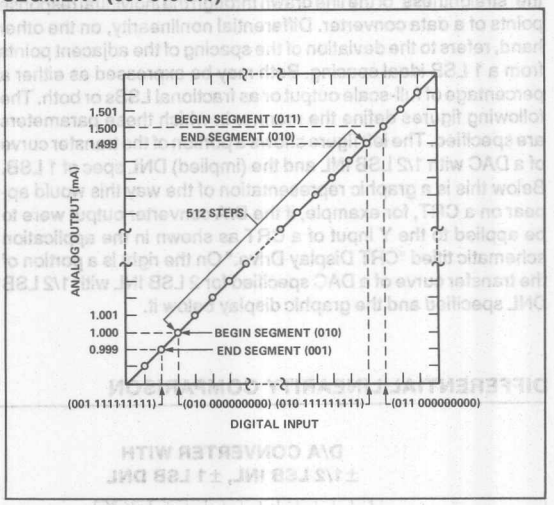
ENLARGED "POSITIONAL" OUTPUTS

DESCRIPTION OF OPERATION

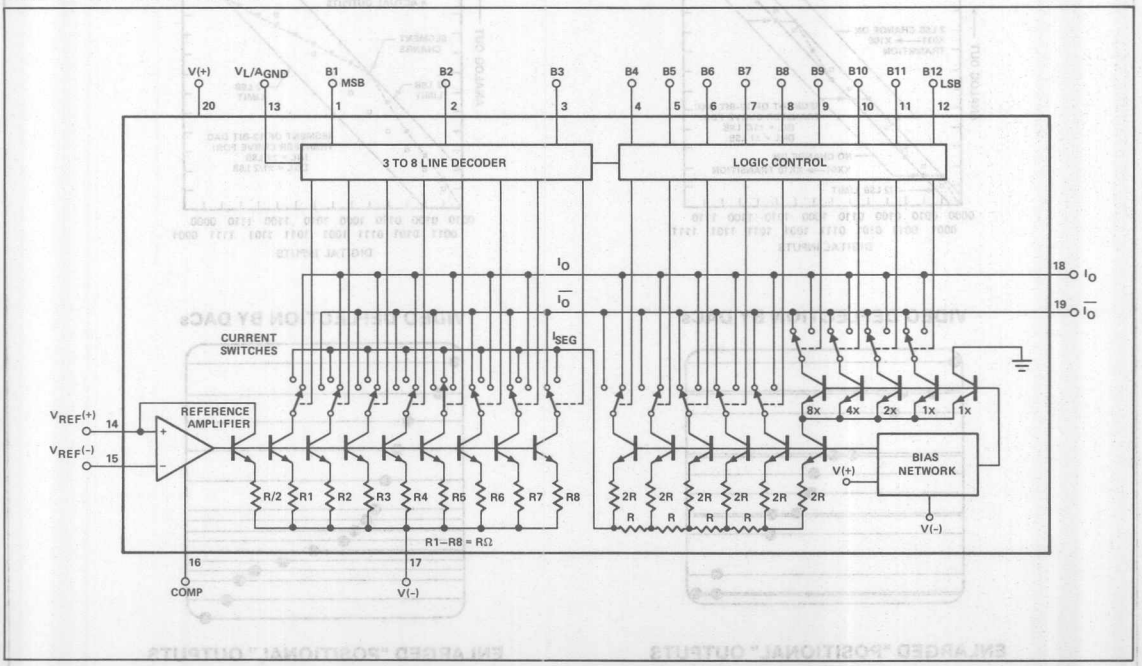
The DAC-312 is divided into two major sections, an 8-segment generator and a 9-bit master/slave D/A Converter. In operation the device performs as follows (See Simplified Schematic):

The three most significant bits (MSB's) are inputs to a 3-to-8 line decoder. The selected resistor (R5 in the figure) is connected to the master/slave 9-bit D/A Converter. All lower order resistors (R1 through R4) are summed into the I_O line, while all higher order resistors (R6 through R8) are summed into the $\overline{I_O}$ line. The R5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or $\overline{I_O}$ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2mA (4 X 0.5mA/segment) +0.375mA (from master/slave D/A Converter) are summed into I_O giving an I_O of 2.375mA. $\overline{I_O}$ has a current of 1.625mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from $\overline{I_O}$, with the selected resistor feeding its current to the master/slave D/A Converter; thus each increment of the 3 MSB's allows the current in the 9-bit D/A Converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

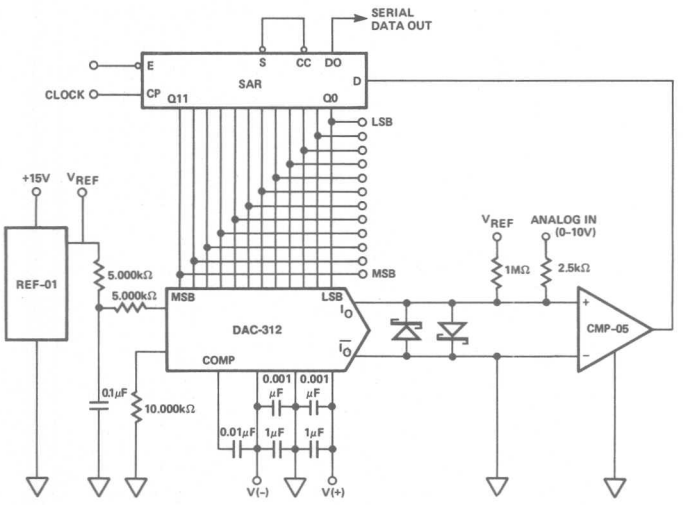
EXPANDED TRANSFER CHARACTERISTIC SEGMENT (001 010 011)



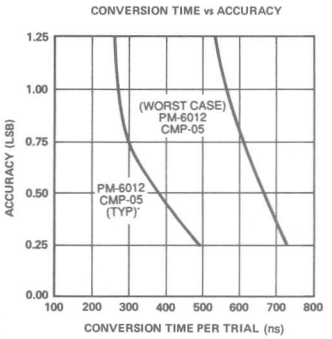
SIMPLIFIED SCHEMATIC



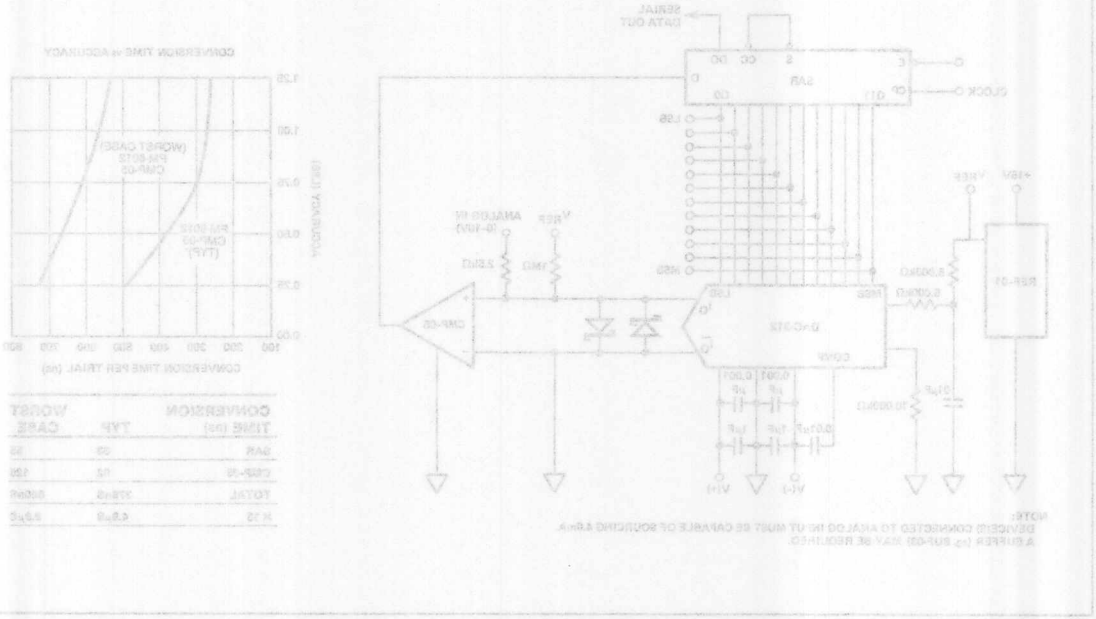
12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375nS	680nS
×13	4.9μS	8.8μS



CMOS 12-Bit Multiplying D/A Converter "With Memory"

DAC-8012

FEATURES

- **Data Readback Capability for System Self Check**
- **Fast TTL/CMOS Compatible Data Register**
- **±1/2 LSB Max Linearity Error Over the Full Operating Temperature Range**
- **±1 LSB Max Gain Error — No User Adjustment Required**
- **Less Than 0.04 LSB Max Zero Scale Error (10nA)**
- **Single +5V to +15V Supply**
- **Small 20-Pin 0.3" Wide DIP**
- **Improved ESD Resistance**
- **Latch-Up Resistant**
- **Adds Data Readback Feature to PM-7545 Pinout**
- **Available in Die Form**

GENERAL DESCRIPTION

The DAC-8012 is a monolithic 12-bit CMOS multiplying DAC with internal data latches and three-state data readback buffers. The latches and readback buffers perform like a "memory" location. Data loads into the latches as a single 12-bit wide word allowing direct connection to 12-bit and 16-bit busses.

Four-quadrant multiplying capability and 12-bit linearity simplifies wide-bandwidth, low-distortion, digitally-controlled precision attenuator and filter applications.

The powerful data readback function allows users to perform data path verification between the controlling processor and the DAC-8012. System self check results after writing a data word to the DAC-8012, then reading it back to the processor, verifying no change in data takes place. The readback function simplifies the design of automatic test equipment, industrial automation, robotics, and processor-controlled instrumentation. Reduction of software coding results with processors using direct memory execution instructions. In remote systems, data set-points are held in the DAC register which can be interrogated upon system fault recovery.

ORDERING INFORMATION †

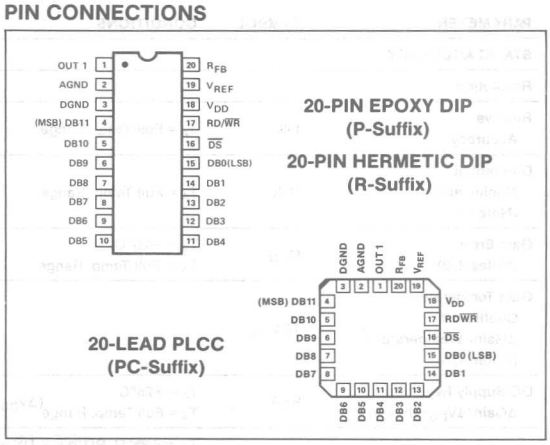
	PACKAGE: 20-PIN			
RELATIVE ACCURACY	MAXIMUM GAIN ERROR T_A = +25°C V_{DD} = +5V	MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8012AR	DAC8012ER	DAC8012GP
±1 LSB	±3 LSB	DAC8012BR	DAC8012FR	DAC8012HP
±1 LSB	±3 LSB	–	DAC8012FP	–
±1 LSB	±3 LSB	–	DAC8012FPC	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

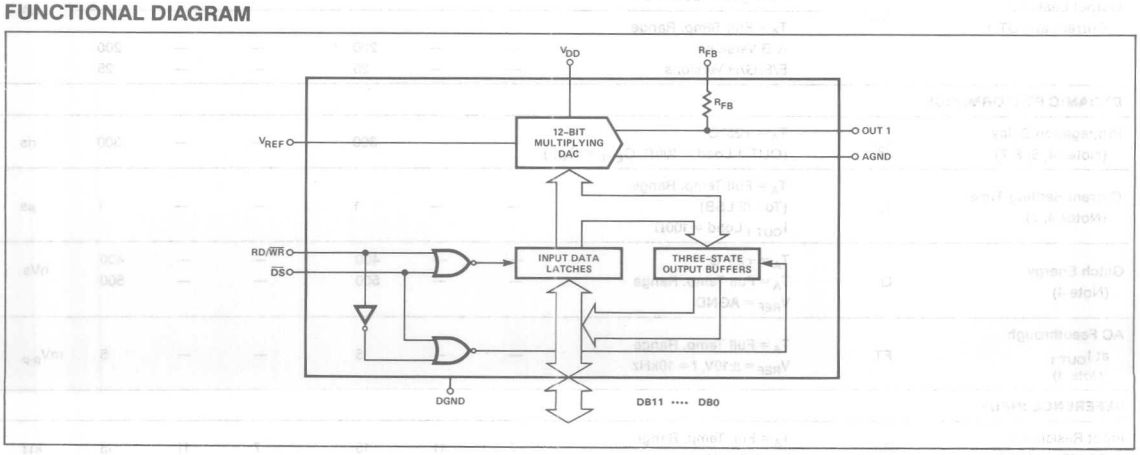
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... –0.3V, +17V
Digital Input Voltage to DGND ..... –0.3V, V_{DD}
AGND to DGND ..... –0.3, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... –0.3V, V_{DD}
Operating Temperature Range
Military (AR, BR) Grades ..... –55°C to +125°C
Industrial (ER, FR, FP, FPC) Grades ..... –40°C to +85°C
Commercial (GP, HP) Grades ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\ 1}$ = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G MIN	DAC-8012A/E/G TYP	DAC-8012A/E/G MAX	DAC-8012B/F/H MIN	DAC-8012B/F/H TYP	DAC-8012B/F/H MAX	UNITS
STATIC ACCURACY									
Resolution			12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1	LSB
Differential Nonlinearity (Note 1)	DNL	T_A = Full Temp. Range	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±1 ±2	— —	— —	±3 ±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature (Notes 4, 5)	TCG_{FS}		—	—	±5	—	—	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 4)	PSR	T_A = +25°C T_A = Full Temp. Range (ΔV_{DD} = ±5%)	— —	— —	0.002 0.004	— —	— —	0.002 0.004	%/%
Output Leakage Current at OUT 1	I_{LKG}	T_A = +25°C, RD/$\overline{WR}$ = $\overline{DS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range A/B Versions E/F/G/H Versions	— —	— —	200 25	— —	— —	200 25	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 6, & 7)	t_{pD}	T_A = +25°C (OUT 1 Load = 100Ω, C_{EXT} = 13pF)	—	—	300	—	—	300	ns
Current Settling Time (Notes 4, 7)	t_s	T_A = Full Temp. Range (To 1/2 LSB) $I_{OUT\ 1}$ Load = 100Ω	—	—	1	—	—	1	μs
Glitch Energy (Note 4)	Q	T_A = +25°C T_A = Full Temp. Range V_{REF} = AGND	— —	— —	400 500	— —	— —	400 500	nVs
AC Feedthrough at $I_{OUT\ 1}$ (Note 4)	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz	—	—	5	—	—	5	mV_{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

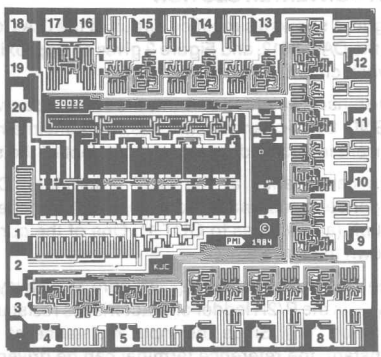
			DAC-8012A/E/G			DAC-8012B/F/H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG OUTPUTS									
Output Capacitance (Note 4)		V_{DD} = +5V or +15V T_A = Full Temp. Range							
$C_{OUT\,1}$	C_{OUT}	DB0-DB11 = 0V, RD/$\overline{WR}$ = $\overline{DS}$ = 0V	—	—	70	—	—	70	pF
		DB0-DB11 = V_{DD}, RD/$\overline{WR}$ = $\overline{DS}$ = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	μA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance									
DB0-DB11	C_{IN}	T_A = Full Temp. Range	—	—	12	—	—	12	pF
RD/$\overline{WR}$, $\overline{DS}$ (Note 4)			—	—	6	—	—	6	
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	I_O = 400μA	4.0	—	—	4.0	—	—	V
Output Low Voltage	V_{OL}	I_O = –1.6mA	—	—	0.4	—	—	0.4	V
Three-State Output Leakage Current			—	—	10	—	—	10	μA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Write Hold Time	t_{WH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Read to Data Strobe Setup Time	t_{RSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Read Hold Time	t_{RH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Write Mode Data Strobe Width	t_{WRS}	T_A = +25°C	180	—	—	180	—	—	ns
		T_A = Full Temp. Range	250	—	—	250	—	—	
Read Mode Data Strobe Width	t_{RDS}	T_A = +25°C	220	—	—	220	—	—	ns
		T_A = Full Temp. Range	290	—	—	290	—	—	
Data Setup Time	t_{DSU}	T_A = +25°C	210	—	—	210	—	—	ns
		T_A = Full Temp. Range	250	—	—	250	—	—	
Data Hold Time	t_{DH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Data Valid Time (Notes 4, 9)	t_{CO}	T_A = +25°C	—	—	300	—	—	300	ns
		T_A = Full Temp. Range	—	—	400	—	—	400	
Output Active Time from Deselection (Notes 4, 9)	t_{OTD}	T_A = +25°C	—	—	215	—	—	215	ns
		T_A = Full Temp. Range	—	—	375	—	—	375	
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	μA

ELECTRICAL CHARACTERISTICS at V_{DD} = ±15V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G MIN	DAC-8012A/E/G TYP	DAC-8012A/E/G MAX	DAC-8012B/F/H MIN	DAC-8012B/F/H TYP	DAC-8012B/F/H MAX	UNITS
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	13.5	—	—	13.5	—	—	V
Input Low Voltage	V_{INL}	T_A = Full Temp. Range	—	—	1.5	—	—	1.5	V
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	µA
		T_A = Full Temp. Range	—	—	10	—	—	10	µA
Input Capacitance DB0-DB11	C_{IN}	T_A = Full Temp. Range	—	—	12	—	—	12	pF
Input Capacitance RD/$\overline{WR}$, $\overline{DS}$ (Note 4)	C_{IN}	T_A = Full Temp. Range	—	—	10	—	—	10	pF
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	I_O = 3mA	13.5	—	—	13.5	—	—	V
Output Low Voltage	V_{OL}	I_O = –3mA	—	—	1.5	—	—	1.5	V
Three-State Output Leakage Current			—	—	10	—	—	10	µA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	ns
Data Strobe to Write Hold Time	t_{WH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	ns
Read to Data Strobe Setup Time	t_{RSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	ns
Data Strobe to Read Hold Time	t_{RH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Mode Data Strobe Width	t_{WRS}	T_A = +25°C	100	—	—	100	—	—	ns
		T_A = Full Temp. Range	120	—	—	120	—	—	ns
Read Mode Data Strobe Width	t_{RDS}	T_A = +25°C	110	—	—	110	—	—	ns
		T_A = Full Temp. Range	150	—	—	150	—	—	ns
Data Setup Time	t_{DSU}	T_A = +25°C	90	—	—	90	—	—	ns
		T_A = Full Temp. Range	120	—	—	120	—	—	ns
Data Hold Time	t_{DH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	ns
Data Strobe to Output Valid Time (Note 9)	t_{CO}	T_A = +25°C	—	—	180	—	—	180	ns
		T_A = Full Temp. Range	—	—	220	—	—	220	ns
Output Active Time for Deselection (Note 9)	t_{OTD}	T_A = +25°C	—	—	180	—	—	180	ns
		T_A = Full Temp. Range	—	—	250	—	—	250	ns
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	µA

NOTES:
1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED but NOT TESTED.
5. Typical value is 2ppm/°C for V_{DD} = +5V.
6. From digital input change to 90% of final analog output.
7. All digital inputs = 0V to V_{DD}; or V_{DD} to 0V.
8. Sample tested at +25°C to ensure compliance.
9. See load circuits for switching tests.

DICE CHARACTERISTICS



DIE SIZE 0.121 × 0.112 inch, 13,552 sq. mils
(3.07 × 2.85 mm, 8.75 sq. mm)

1. OUT 1
2. AGND
3. DGND
4. DB11 (MSB)
5. DB10
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0 (LSB)
16. $\overline{DS}$
17. $\overline{RD}/\overline{WR}$
18. V_{DD}
19. V_{REF}
20. R_{FB}

2

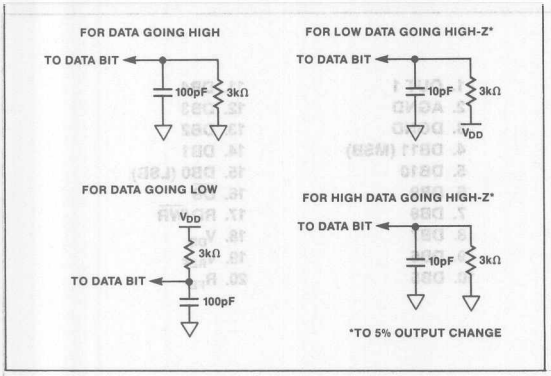
WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111 1111	±3	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R_{REF}	Pad 19	6/15	kΩ MIN/ kΩ MAX
Output High Voltage	V_{OH}	V_{DD} = 5V, I_O = 400μA	4.0	V MIN
Output Low Voltage	V_{OL}	V_{DD} = 5V, I_O = −1.6mA	0.4	V MAX
Digital Input High	V_{INH}	V_{DD} = 5V V_{DD} = 15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = 5V V_{DD} = 15V	0.8 1.5	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	V_{DD} = ±5%	0.004	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		12	pF
Output Capacitance	$C_{OUT\,1}$	DAC Latches Loaded with 0000 0000 0000	70	pF
	$C_{OUT\,1}$	DAC Latches Loaded with 1111 1111 1111	150	pF
Propagation Delay	t_{pD}	V_{DD} = 15V V_{DD} = 5V	300	ns



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ±1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will not decrease for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT1 to AGND.

PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

FEEDTHROUGH GLITCH ENERGY

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with V_{REF} = AGND.

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A Converter section of the DAC-8012, and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

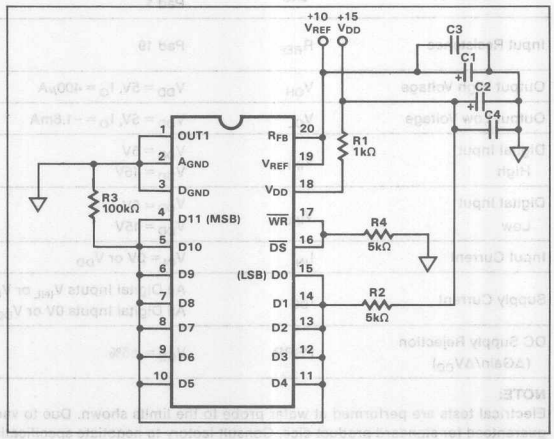
The binary-weighted currents are switched between OUT 1 and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT 1 terminal, $C_{OUT\ 1}$, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT 1). One of the current switches is shown in Figure 2.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however, when the circuit is not powered up the switch assumes an open state.

BURN-IN CIRCUIT



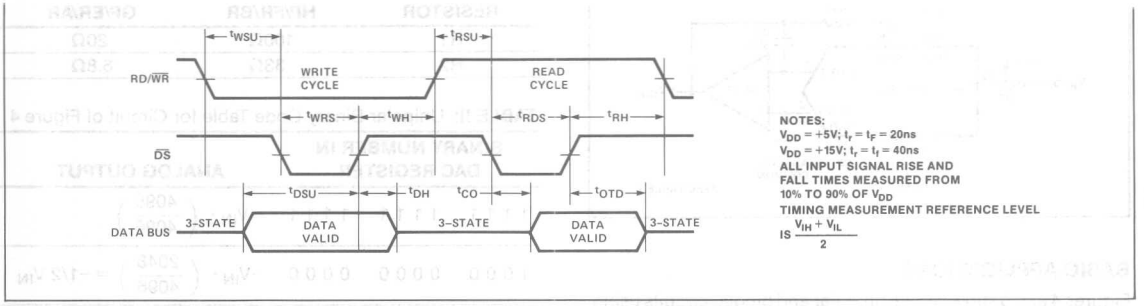


FIGURE 1: Simplified D/A Circuit of DAC-8012

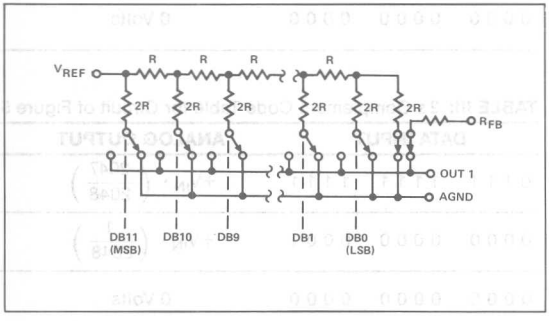
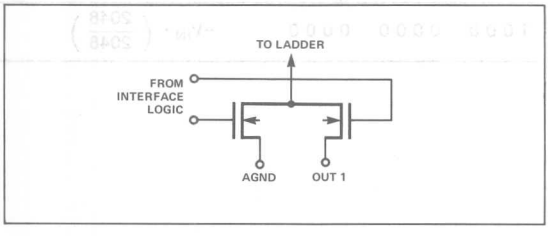


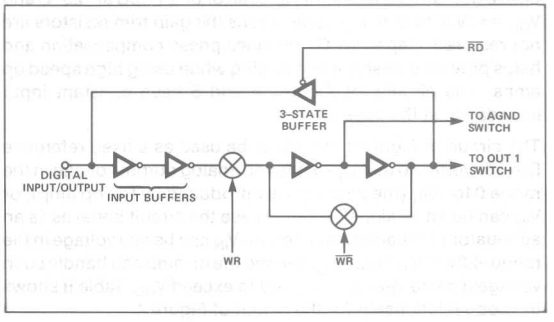
FIGURE 2: N-Channel Current Steering Switch



DIGITAL SECTION

Figure 3 shows the digital I/O structure for one bit. When the data strobe ($\overline{DS}$) and the RD/$\overline{WR}$ lines are held low, data at the digital input is fed through the input buffers and the data latches which control the DAC current output switches are transparent. Data is latched when either $\overline{DS}$ or RD/$\overline{WR}$ go high. When the data strobe $\overline{DS}$ is held low and the RD/$\overline{WR}$ line is held high, the three-state buffer becomes active and the data from the latches is fed through the three-state buffers to the digital input/output lines. This is known as the Read Cycle, or data readback.

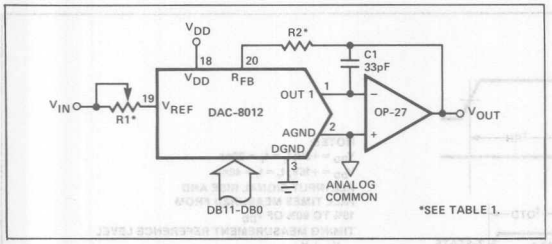
FIGURE 3: Digital Input/Output Structure



The input buffers are simple CMOS inverters designed such that when the DAC-8012 is operated with V_{DD} = +5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0V to 3.0V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and D_{GND}) as is practically possible. The DAC-8012 may be operated with any supply voltage in the range $5V \leq V_{DD} \leq 15V$. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

The three-state output buffers, in the active mode, provide TTL-compatible digital outputs with a fan-out of one TTL load when the DAC-8012 is operated with +5V power supply. When powered from +15V, the output buffers provide output logic levels of 1.5V and 13.5V. Three-state output leakage is typically 10nA.

FIGURE 4: Unipolar Binary Operation



BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the DAC-8012. Resistor R1 is used to trim for full scale. The following versions: DAC-8012AR, DAC-8012ER, DAC-8012GP, have a guaranteed maximum gain error of ±1 LSB at +25°C and V_{DD} = +5V, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20V \leq V_{IN} \leq +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software, using an exclusive OR instruction.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1	100Ω	20Ω
R2	33Ω	6.8Ω

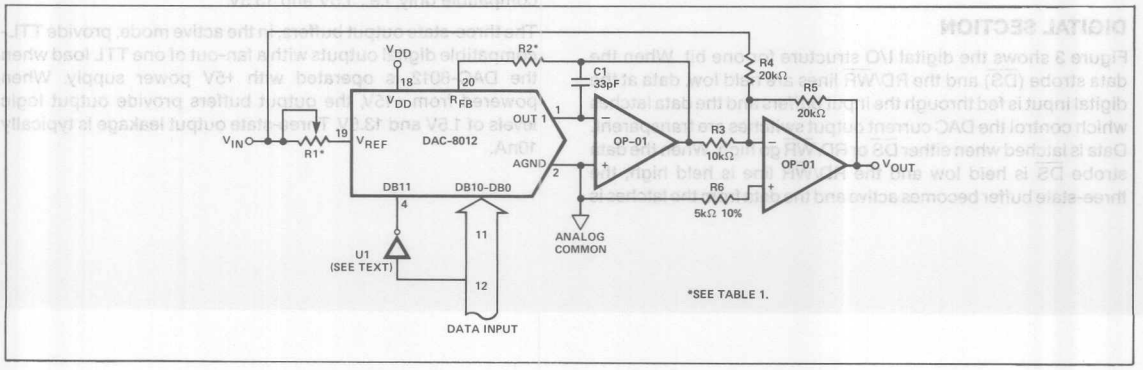
TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
1111 1111 1111	$-V_{IN} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0 Volts

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT	ANALOG OUTPUT
0111 1111 1111	$+V_{IN} \cdot \left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{IN} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{2048}\right)$

FIGURE 5: Bipolar Operation (2's Complement Code)



APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the DAC-8012. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When RD/$\overline{WR}$ and $\overline{DS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which RD/$\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse RD/$\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

INTERFACING THE DAC-8012 TO MICROPROCESSORS

Figure 6 shows the interface configuration for the 68000 16-bit microprocessor. No external logic is required to write data into the DAC or to readback data from the DAC-8012 latches. Analog circuitry has been removed for clarity.

FIGURE 6: 68000 16-Bit Microprocessor to DAC-8012 Interface

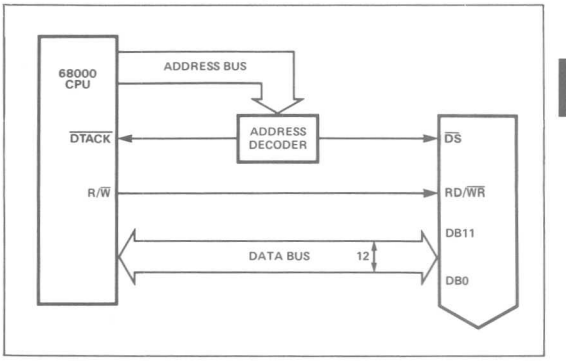
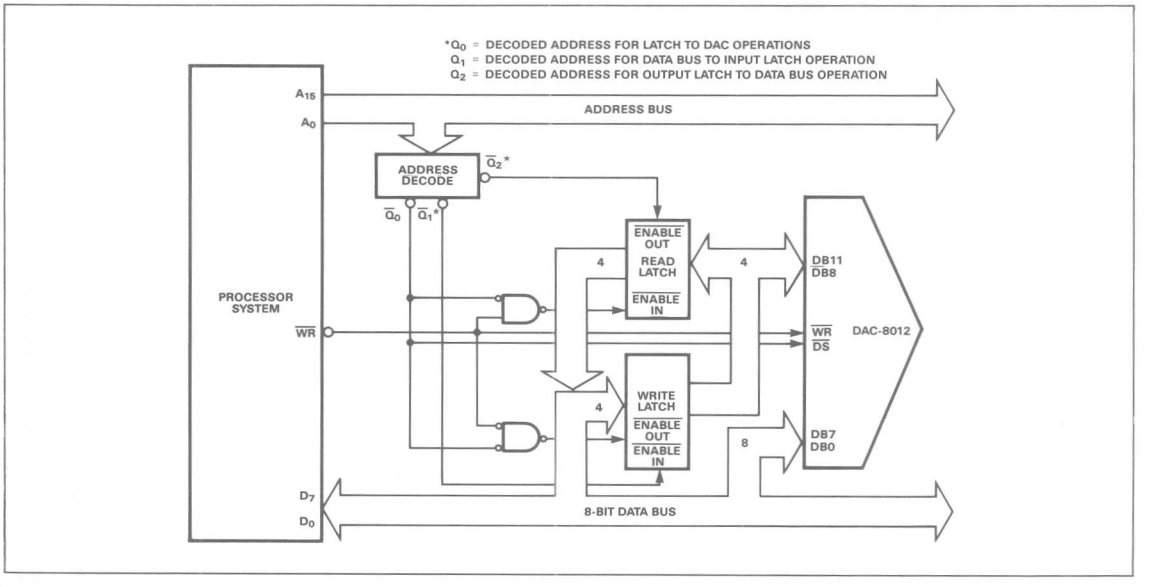
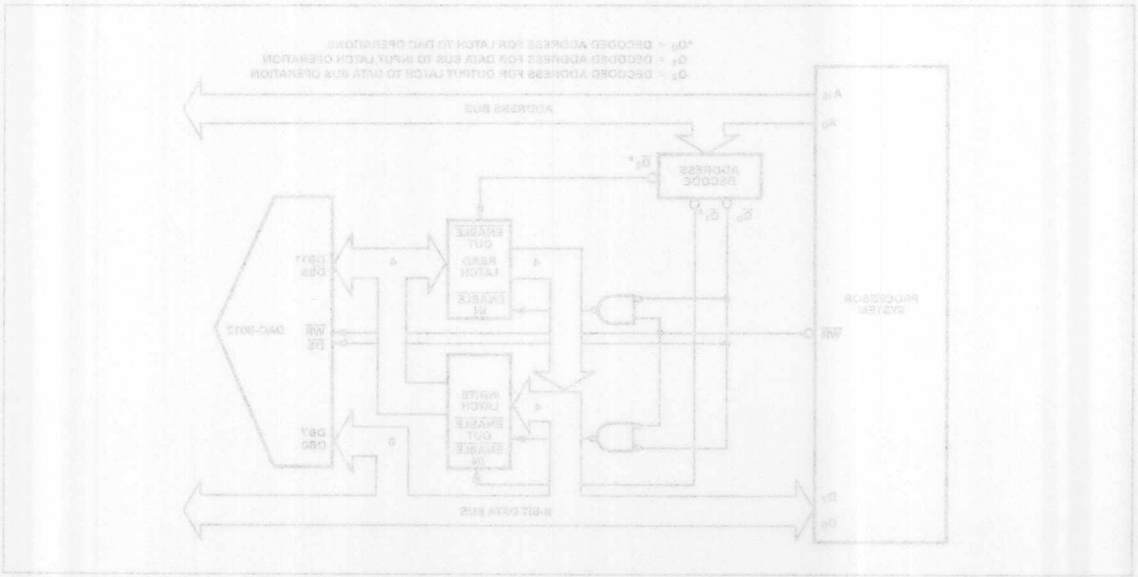


FIGURE 7: 8-Bit Processor to DAC-8012 Interface





DAC-8043

FEATURES

- 12-Bit Accuracy in an 8-Pin Mini-Dip
- Fast Serial Data Input
- Double Data Buffers
- Low ±1/2 LSB Max INL and DNL
- Max Gain Error: ±1 LSB
- Low 5ppm/°C Max Tempco
- ESD Resistant
- Low Cost
- Available in Die Form

APPLICATIONS

- Auto-Calibration Systems
- Process Control and Industrial Automation
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Filters

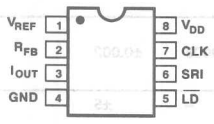
ORDERING INFORMATION†

	PACKAGE		
RELATIVE ACCURACY	MILITARY* TEMPERATURE –55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO+70°C
±1/2 LSB	DAC8043AZ	DAC8043EZ	DAC8043GP
±1/2 LSB	DAC8043AZ/883	–	–
±1 LSB	–	DAC8043FZ	–
±1 LSB	–	DAC8043FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in.

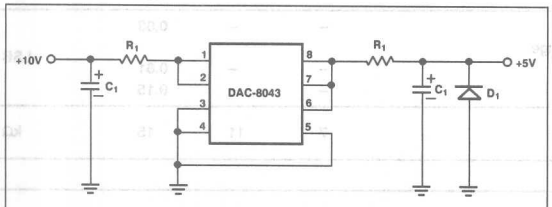
PIN CONNECTIONS



8-PIN EPOXY DIP
(P-Suffix)

8-PIN CERDIP
(Z-Suffix)

BURN-IN CIRCUIT



NOTES:
R_1 = 10Ω
C_1 = 10µF
D_1 = 1N4001 OR EQUIVALENT
MAXIMUM POWER SUPPLY CURRENT PER DEVICE IS +1.5mA, –0mA
POWER-UP SEQUENCE: +5V, +10V
POWER-DOWN SEQUENCE: +10V, +5V

GENERAL DESCRIPTION

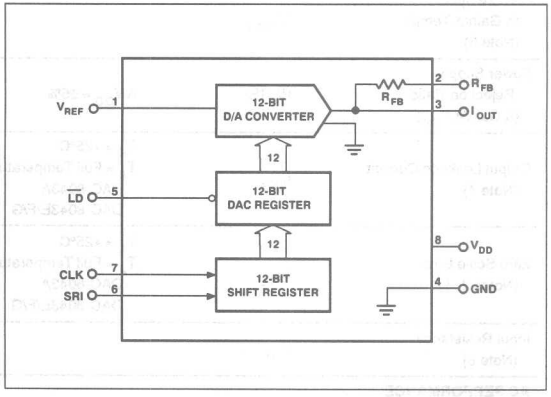
The DAC-8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-pin mini-DIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC-8043 is ideal for applications where PC board space is at a premium. Also, improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load-DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

The DAC-8043's fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM-7543.

Operating from a single +5V power supply, the DAC-8043 is the ideal low power, small size, high performance solution to many application problems. It is available in plastic and cerdip packages that are compatible with auto-insertion equipment.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted.)

V_{DD} to GND ..... +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 3) ..... –0.3V to V_{DD}
Operating Temperature Range
AZ Versions ..... –55°C to +125°C
EZ/FZ/FP Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

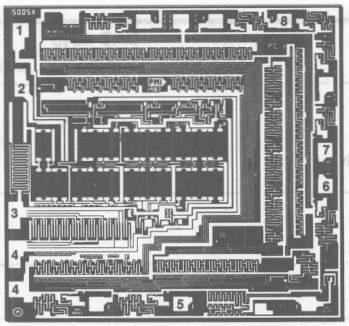
PARAMETER	SYMBOL	CONDITIONS	DAC-8043 MIN	DAC-8043 TYP	DAC-8043 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	–	–	Bits
Nonlinearity (Note 1)	INL	DAC-8043A/E/G	–	–	±1/2	LSB
		DAC-8043F	–	–	1	
Differential Nonlinearity (Note 2)	DNL	DAC-8043A/E	–	–	±1/2	LSB
		DAC-8043F/G	–	–	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				
		DAC-8043A/E	–	–	1	LSB
		DAC-8043F/G	–	–	2	
		T_A = Full Temperature Range				
		All Grades	–	–	2	
Gain Tempco (Δ Gain/Δ Temp) (Note 5)	TC_{GFS}		–	–	±5	ppm/°C
Power Supply Rejection Ratio (Δ Gain/Δ V_{DD})	PSRR	Δ V_{DD} = ±5%	–	±0.0006	±0.002	%/%
Output Leakage Current (Note 4)	I_{LKG}	T_A = +25°C	–	–	±5	nA
		T_A = Full Temperature Range				
		DAC-8043A	–	–	±100	
		DAC-8043E/F/G	–	–	±25	
Zero Scale Error (Notes 7, 12)	I_{ZSE}	T_A = +25°C	–	–	0.03	LSB
		T_A = Full Temperature Range				
		DAC-8043A	–	–	0.61	
		DAC-8043E/F/G	–	–	0.15	
Input Resistance (Note 8)	R_{IN}		7	11	15	kΩ
AC PERFORMANCE						
Output Current Settling Time (Notes 5, 6)	t_S	T_A = +25°C	–	0.25	1	µs

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8043 MIN	TYP	MAX	UNITS
Digital to Analog Glitch Energy (Note 5,10)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	–	2	20	nVs
Feedthrough Error (V_{REF} to I_{OUT}) (Note 5, 11)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz Digital Input = 0000 0000 0000 T_A = +25°C	–	0.7	1	mV_{p-p}
Total Harmonic Distortion (Note 5)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	–	–85	–	dB
Output Noise Voltage Density (Notes 5, 13)	e_n	10Hz to 100kHz between R_{FB} and I_{OUT}	–	–	17	$nV/\sqrt{Hz}$
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 9)	I_{IL}	V_{IN} = 0V to +5V	–	–	±1	µA
Input Capacitance (Note 5, 11)	C_{IN}	V_{IN} = 0V	–	–	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT}	Digital Inputs = V_{IH}	–	–	110	pF
		Digital Inputs = V_{IL}	–	–	80	
TIMING CHARACTERISTICS (NOTES 5, 14)						
Data Setup Time	t_{DS}	T_A = Full Temperature Range	40	–	–	ns
Data Hold Time	t_{DH}	T_A = Full Temperature Range	80	–	–	ns
Clock Pulse Width High	t_{CH}	T_A = Full Temperature Range	90	–	–	ns
Clock Pulse Width Low	t_{CL}	T_A = Full Temperature Range	120	–	–	ns
Load Pulse Width	t_{LD}	T_A = Full Temperature Range	120	–	–	ns
LSB Clock Into Input Register to Load DAC Register Time	t_{ASB}	T_A = Full Temperature Range	0	–	–	ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	–	–	500	µA MAX
		Digital Inputs = 0V or V_{DD}	–	–	100	

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT}; All digital inputs = 0V.
5. Guaranteed by design and not tested.
6. I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay.
7. V_{REF} = +10V, all digital inputs = 0V.
8. Absolute temperature coefficient is less than +300ppm/°C.
9. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
10. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
11. All digital inputs = 0V.
12. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = (R_{REF} x I_{LKG} x 4096)/V_{REF}.
13. Calculations from en = $\sqrt{4K\,TRB}$ where:
    K = Boltzmann constant, J/°K, R = resistance, Ω
    T = resistor temperature, °K, B = bandwidth, Hz
14. Tested at V_{IN} = 0V or V_{DD}.



1. V_{REF}
2. R_{FB}
3. I_{OUT}
4. GND
5. $\overline{LD}$
6. SRI
7. CLK
8. V_{DD}

Substrate (die backside) is internally connected to V_{DD}.

DIE SIZE 0.116 x 0.109 inch, 12,644 sq. mils (2.95 x 2.77 mm, 8.17 sq. mm)

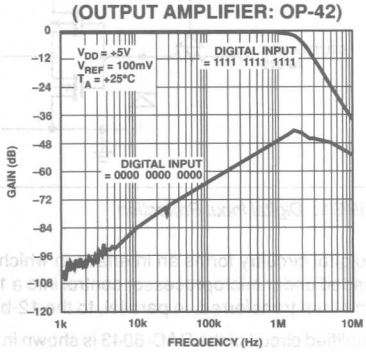
WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = +10V; I_{OUT} = GND = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8043GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	500 100	µA MAX

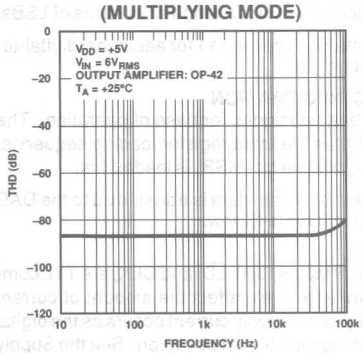
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

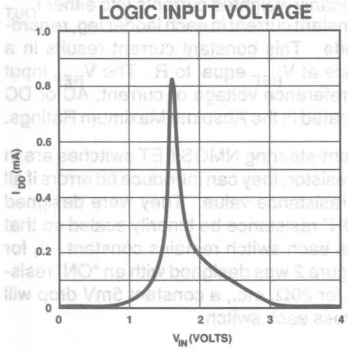
GAIN vs FREQUENCY (OUTPUT AMPLIFIER: OP-42)



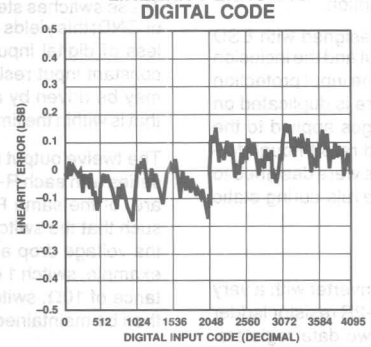
TOTAL HARMONIC DISTORTION vs FREQUENCY (MULTIPLYING MODE)



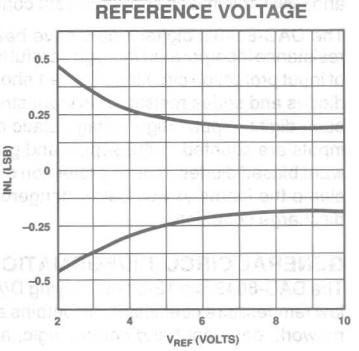
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



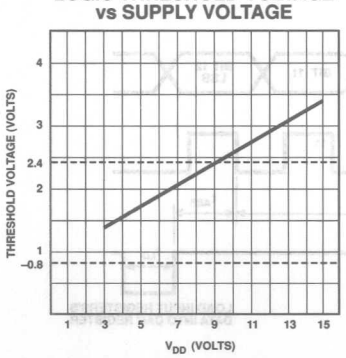
LINEARITY ERROR vs DIGITAL CODE



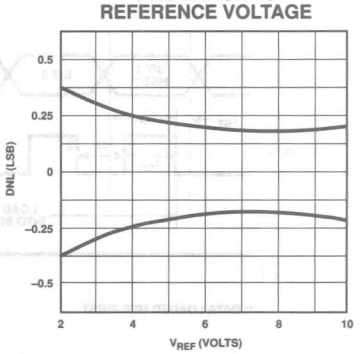
LINEARITY ERROR vs REFERENCE VOLTAGE



LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



PARAMETER DEFINITIONS

INTEGRAL NONLINEARITY (INL)

This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs.

Refer to PMI 1988 Data Book section 11 for additional digital-to-analog converter definitions.

INTERFACE LOGIC INFORMATION

The DAC-8043 has been designed for ease of operation. The timing diagram illustrates the input register loading sequence. Note that the most significant bit (MSB) is loaded first.

Once the input register is full, the data is transferred to the DAC register by taking $\overline{LD}$ momentarily low.

DIGITAL SECTION

The DAC-8043's digital inputs, SRI, $\overline{LD}$, and CLK, are TTL compatible. The input voltage levels affect the amount of current drawn from the supply; peak supply current occurs as the digital input (V_{IN}) passes through the transition region. See the Supply Current vs. Logic Input Voltage graph located under the typical performance characteristics curves. Maintaining the digital input voltage levels as close as possible to the supplies, V_{DD} and GND, minimizes supply current consumption.

The DAC-8043's digital inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry. Figure 1 shows the input protection diodes and series resistor; this input structure is duplicated on each digital input. High voltage static charges applied to the inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes were designed to clamp the inputs to well below dangerous levels during static discharge conditions.

GENERAL CIRCUIT INFORMATION

The DAC-8043 is a 12-bit multiplying D/A converter with a very low temperature coefficient. It contains an R-2R resistor ladder network, data input and control logic, and two data registers.

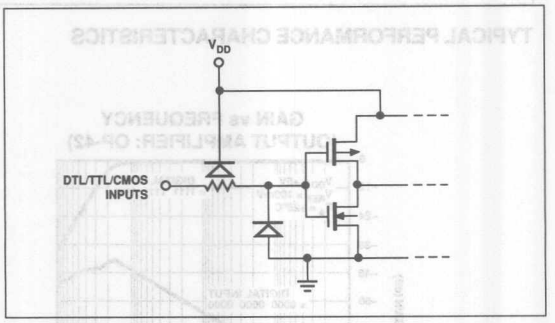


FIGURE 1: *Digital Input Protection*

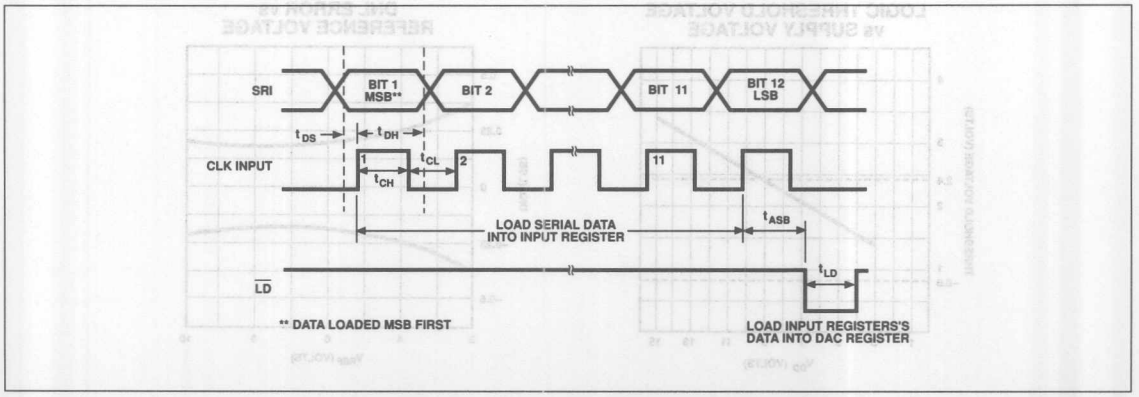
The digital circuitry forms an interface in which serial data can be loaded under microprocessor control into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

A simplified circuit of the DAC-8043 is shown in Figure 2. An inverted R-2R ladder network consisting of silicon-chrome, highly-stable (+50ppm/°C) thin-film resistors, and twelve pairs of NMOS current-steering switches.

These switches steer binarily weighted currents into either I_{OUT} or GND; this yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R. The V_{REF} input may be driven by any reference voltage or current, AC or DC that is within the limits stated in the Absolute Maximum Ratings.

The twelve output current-steering NMOS FET switches are in series with each R-2R resistor, they can introduce bit errors if all are of the same R_{ON} resistance value. They were designed such that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 2 was designed with an "ON" resistance of 10Ω, switch 2 for 20Ω, etc., a constant 5mV drop will then be maintained across each switch.

WRITE CYCLE TIMING DIAGRAM



To further insure accuracy across the full temperature range, permanently "ON" MOS switches were included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit," Figure 2, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

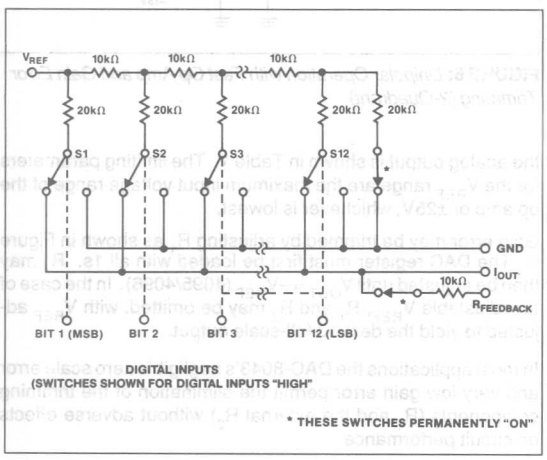


FIGURE 2: *Simplified DAC Circuit*

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent analog circuit for the DAC-8043. The (D x V_{REF})/R current source is code dependent and is the current generated by the DAC. The current source I_{LKG} consists of surface and junction leakages and doubles approximately every 10°C. C_{OUT} is the output capacitance; it is the result of the N-channel MOS switches and varies from 80 to 110pF depending on the digital input code. R_O is the equivalent output resistance that also varies with digital input code. R is the nominal R-2R resistor ladder resistance.

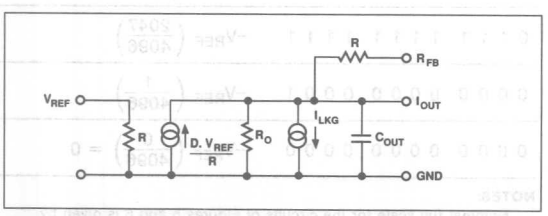


FIGURE 3: *Equivalent Analog Circuit*

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The DAC-8043's output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 10kΩ (the feedback resistor alone when all digital inputs are LOW) and 7.5kΩ (the feedback resistor in parallel with approximate30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations.

This variation is best illustrated by using the circuit of Figure 4 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and :

R_O = 10kΩ for more than four bits of logic 1.
R_O = 30kΩ for any single bit of logic 1.

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{ERROR_1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\ V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR_2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3\ V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = +10V) of 2.4mV for the DAC-8043, it is clearly important that VOS be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

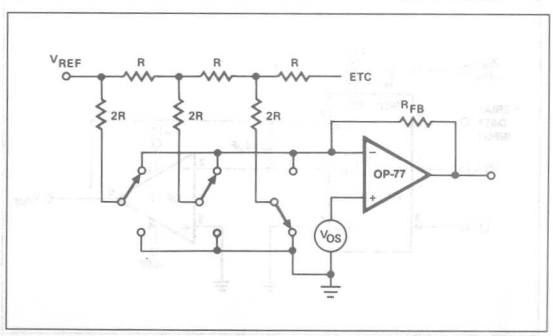


FIGURE 4: *Simplified Circuit*

The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance. The use of a small compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output. The DAC-8043's output capacitance and the R_{FB} resistor form a pole that must be outside the amplifier's unity gain crossover frequency.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT} and GND (pins 3 and 4) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 5 and 6). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than +200µV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

UNIPOLAR OPERATION (2-QUADRANT)

The circuit shown in Figures 5 and 6 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and

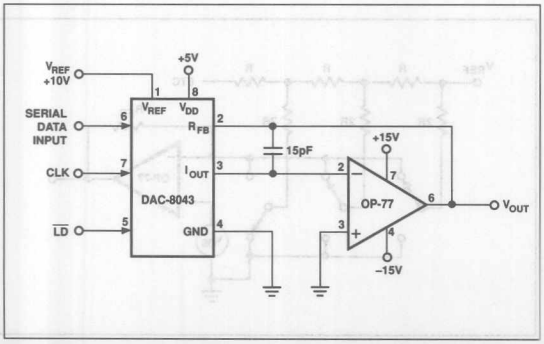


FIGURE 5: *Unipolar Operation with High Accuracy Op Amp (2-Quadrant)*

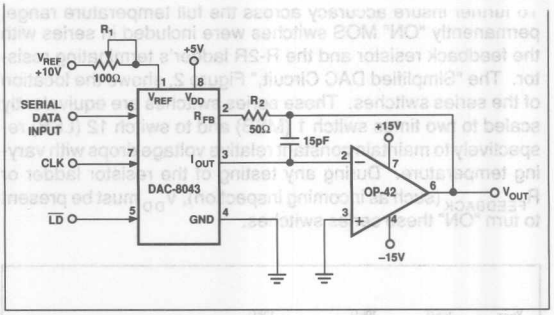


FIGURE 6: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

the analog output is shown in Table 1. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or ±25V, whichever is lowest.

Gain error may be trimmed by adjusting R_1 as shown in Figure 6. The DAC register must first be loaded with all 1s. R_1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and R_2 may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In most applications the DAC-8043's negligible zero scale error and very low gain error permit the elimination of the trimming components (R_1 and the external R_2) without adverse effects on circuit performance.

TABLE 1: Unipolar Code Table

DIGITAL INPUT MSB	DIGITAL INPUT LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 5 and 6)
1111	1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000 0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000	0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111	1111 1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000	0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000	0000 0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 5 and 6 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 5 and 6 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}\,(2^{-n})$.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB		LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 7)
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0
0111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 7 is given by
   $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 7 is given by
   $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

BIPOLAR OPERATION (4-QUADRANT)

Figure 7 details a suggested circuit for bipolar, or offset binary operation. Table 2 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R_3 and R_4 causes offset and full scale errors while an R_5 to R_4 and R_3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted, adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

2

ANALOG/DIGITAL DIVISION

The transfer function for the DAC-8043 connected in the multiplying mode as shown in Figures 5, 6, and 7 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 8 and becomes:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON," the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12 "ON."

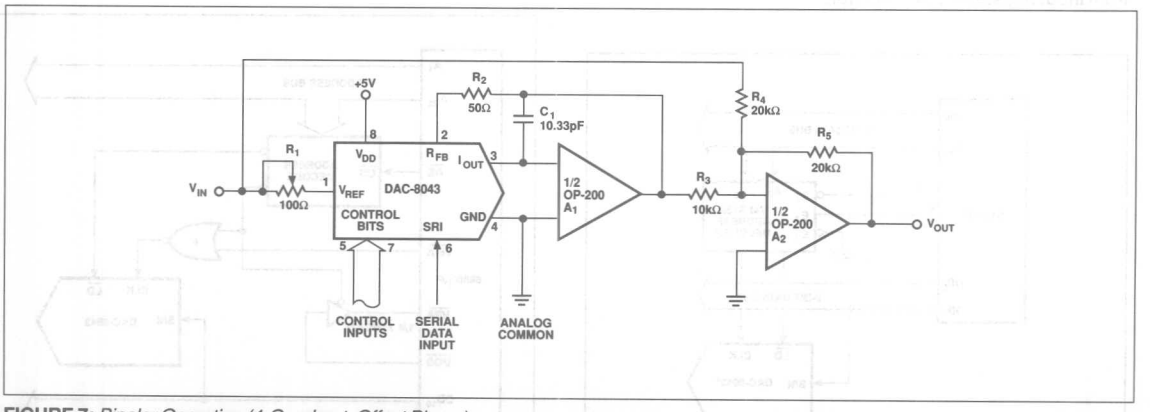


FIGURE 7: *Bipolar Operation (4-Quadrant, Offset Binary)*

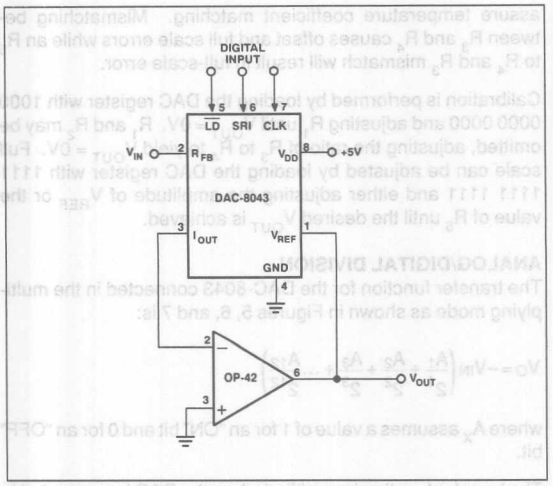


FIGURE 8: *Analog/Digital Divider*

INTERFACING TO THE MC6800

As shown in Figure 9, the DAC-8043 may be interfaced to the 6800 by successively executing memory WRITE instructions while manipulating the data between WRITEs, so that each WRITE presents the next bit.

In this example the most significant bits are found in memory location 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the DB_7 line.

The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/$\overline{W}$, and ϕ2. A WRITE to address 4000 transfers data from input register to DAC register.

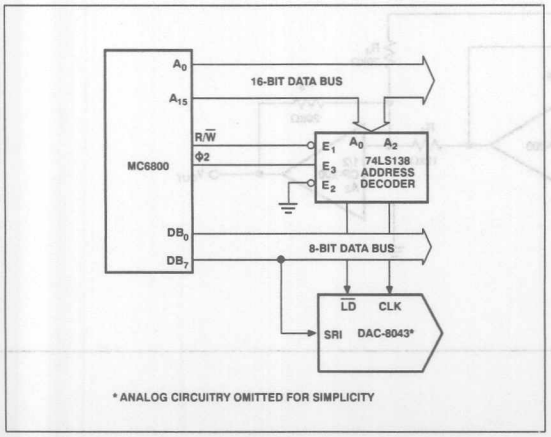


FIGURE 9: *DAC-8043–MC6800 Interface*

DAC-8043 INTERFACE TO THE 8085

The DAC-8043's interface to the 8085 microprocessor is shown in Figure 10. Note that the microprocessor's SOD line is used to present data serially to the DAC.

Data is clocked into the DAC-8043 by executing memory write instructions. The clock input is generated by decoding address 8000 and WR. Data is loaded into the DAC register with a memory write instruction to address A000.

Serial data supplied to the DAC-8043 must be present in the right-justified format in registers H and L of the microprocessor.

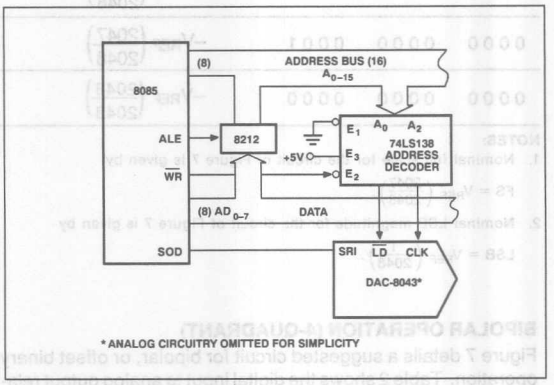


FIGURE 10: *DAC-8043–8085 Interface*

DAC-8043 TO 68000 INTERFACING

The DAC-8043 interfacing to the 68000 microprocessor is shown in Figure 11. Again, serial data to the DAC is taken from one of the microprocessor's data bus lines.

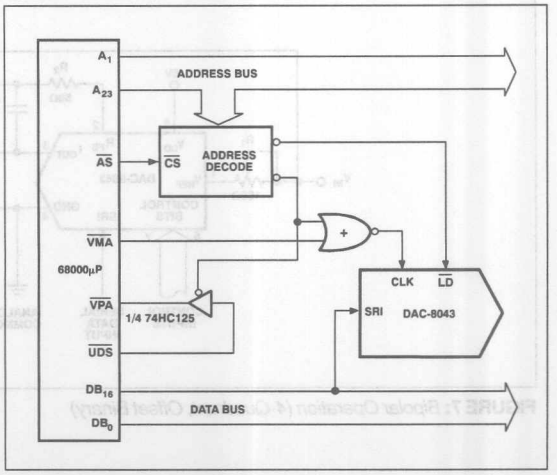


FIGURE 11: *DAC-8043–68000μP Interface*

12-Bit Serial Daisy-Chain CMOS D/A Converter

DAC-8143

FEATURES

- Fast, Flexible, Microprocessor Interfacing in Serially-Controlled Systems
- Buffered Digital Output-Pin for Daisy-Chaining Multiple DACs
- Minimizes Address-Decoding in Multiple DAC Systems – Three Wire Interface for Any Number of DACs
  - One Data Line
  - One CLK Line
  - One Load Line
- Improved Resistance to ESD
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available in Die Form

APPLICATIONS

- Multiple-Channel Data Acquisition Systems
- Process Control and Industrial Automation
- Test Equipment
- Remote Microprocessor-Controlled Systems

ORDERING INFORMATION †

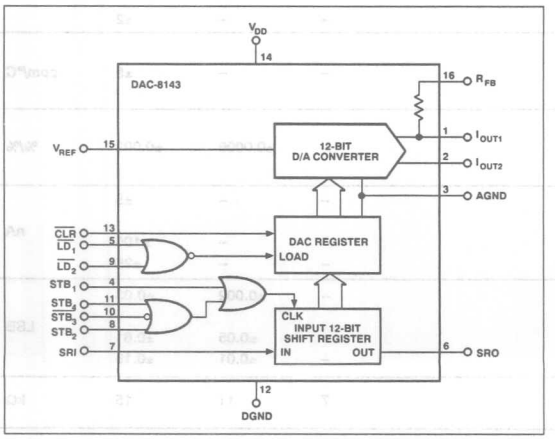
		PACKAGE: 16-PIN	
NON-LINEARITY	GAIN ERROR	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	±1 LSB	DAC8143AQ	DAC8143EQ
±1/2 LSB	±1 LSB	DAC8143AQ/883	–
±1 LSB	±2 LSB	–	DAC8143FP
±1 LSB	±2 LSB	–	DAC8143FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL BLOCK DIAGRAM



GENERAL INFORMATION

The DAC-8143 is a 12-bit serial-input daisy-chain CMOS D/A converter, which features serial data input and buffered serial data output. It was designed for multiple serial DAC systems, where serially daisy-chaining one DAC after another is greatly simplified.

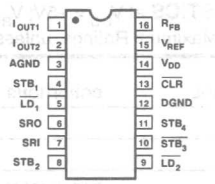
The DAC-8143 also minimizes address decoding lines enabling simpler logic interfacing. It allows 3-wire interface for any number of DACs: one data line, one CLK line, and one load line.

Serial data in the input register (MSB first) is sequentially clocked out to the SRO pin as the new data word (MSB first) is simultaneously clocked in from the SRI pin. The strobe inputs are used to clock in/out data on the rising or falling (user selected) strobe edges (STB_1, STB_2, $\overline{STB_3}$, STB_4).

When the shift register's data has been updated, the new data word is transferred to the DAC register with use of $\overline{LD_1}$ and $\overline{LD_2}$ inputs.

Continued

PIN CONNECTIONS

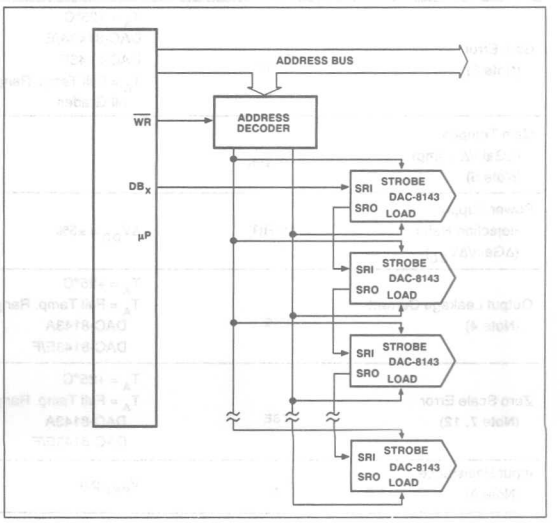


16-PIN EPOXY DIP (P-Suffix)

16-PIN CERDIP (Q-Suffix)

16-PIN SOL (S-Suffix)

MULTIPLE DAC-8143s WITH 3-WIRE INTERFACE



GENERAL INFORMATION *Continued*

Separate LOAD control inputs allow simultaneous output updating of multiple DACs. An asynchronous CLEAR input resets the DAC register without altering data in the input register.

Improved linearity and gain error performance permits reduced circuit parts count through the elimination of trimming components. Also, fast interface timing reduces timing design consideration while minimizing microprocessor wait states.

The DAC-8143 is available in standard cerdip and plastic packages that are compatible with auto-insertion equipment.

Cerdip and plastic packages devices come in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... +17V
V_{REF} to DGND ..... ±25V
V_{RFB} to DGND ..... ±25V
AGND to DGND ..... V_{DD}+0.3V
DGND to AGND ..... V_{DD}+0.3V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}
Operating Temperature Range
AQ Version ..... –55°C to +125°C
EQ/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do not apply voltage higher than V_{DD} or less than DGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	DAC-8143 TYP	DAC-8143 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	–	–	Bits
Nonlinearity (Note 1)	INL	DAC-8143A/E	–	–	±1/2	LSB
		DAC-8143F	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	DAC-8143A/E	–	–	±1/2	LSB
		DAC-8143F	–	–	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				
		DAC-8143A/E	–	–	±1	LSB
		DAC-8143F	–	–	±2	
		T_A = Full Temp. Range All Grades	–	–	±2	
Gain Tempco (ΔGain/Δ Temp) (Note 5)	TC_{GFS}		–	–	±5	ppm/°C
Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	±0.0006	±0.002	%/%
Output Leakage Current (Note 4)	I_{LKG}	T_A = +25°C	–	–	±5	nA
		T_A = Full Temp. Range				
		DAC-8143A	–	–	±100	
		DAC-8143E/F	–	–	±25	
Zero Scale Error (Note 7, 12)	I_{ZSE}	T_A = +25°C	–	±0.002	±0.03	LSB
		T_A = Full Temp. Range				
		DAC-8143A	–	±0.05	±0.61	
		DAC-8143E/F	–	±0.01	±0.15	
Input Resistance (Note 8)	R_{IN}	V_{REF} pin	7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 5, 6)	t_s		–	0.380	1	µs
AC Feedthrough Error (V_{REF} to I_{OUT1}) (Notes 5, 11)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz T_A = 25°C	–	–	2.0	mV_{p-p}
Digital to Analog Glitch Energy (Notes 5, 10)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF	–	–	20	nVs
Total Harmonic Distortion (Note 5)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	–	–	–92	dB
Output Noise Voltage Density (Notes 5, 13)	e_n	10Hz to 100kHz between R_{FB} and I_{OUT}	–	–	13	$nV/\sqrt{Hz}$
DIGITAL INPUTS/OUTPUT						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 9)	I_{IN}	V_{IN} = 0V to +5V	–	–	±1	µA
Input Capacitance (Note 5)	C_{IN}	V_{IN} = 0V	–	–	8	pF
Digital Output High	V_{OH}	I_{OH} = –200µA	4	–	–	V
Digital Output Low	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = all 1s Digital Inputs = all 0s	– –	– –	90 90	pF
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = all 0s Digital Inputs = all 1s	– –	– –	60 60	pF
TIMING CHARACTERISTICS (Note 5)						
Serial Input to Strobe Setup Times (t_{STB} = 80ns)	t_{DS1}	STB_1 used as the strobe	50	–	–	ns
	t_{DS2}	STB_2 used as the strobe	20	–	–	
	t_{DS3}	STB_3 used as the strobe, T_A = +25°C	10	–	–	
		STB_3 used as the strobe, T_A = Full Temp. Range	20	–	–	
	t_{DS4}	STB_4 used as the strobe	20	–	–	
Serial Input to Strobe Hold Times (t_{STB} = 80ns)	t_{DH1}	STB_1 used as the strobe, T_A = +25°C	40	–	–	ns
		STB_1 used as the strobe, T_A = Full Temp. Range	50	–	–	
	t_{DH2}	STB_2 used as the strobe, T_A = +25°C	50	–	–	
		STB_2 used as the strobe, T_A = Full Temp. Range	60	–	–	
	t_{DH3}	STB_3 used as the strobe	80	–	–	
	t_{DH4}	STB_4 used as the strobe	80	–	–	

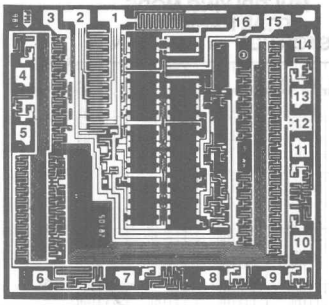
Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	TYP	MAX	UNITS
STB to SRO Propagation Delay (Note 15)	t_{PD}	T_A = 25°C T_A = Full Temp. Range	– –	– –	220 300	ns
SRI Data Pulse Width	t_{SRI}		100	–	–	ns
STB_1 Pulse Width ($\overline{STB_1}$ = 80ns) (Note 14)	t_{STB1}		80	–	–	ns
STB_2 Pulse Width ($\overline{STB_2}$ = 100ns) (Note 14)	t_{STB2}		80	–	–	ns
STB_3 Pulse Width ($\overline{STB_3}$ = 80ns) (Note 14)	t_{STB3}		80	–	–	ns
STB_4 Pulse Width ($\overline{STB_4}$ = 80ns) (Note 14)	t_{STB4}		80	–	–	ns
Load Pulse Width	t_{LD1},t_{LD2}	T_A = +25°C T_A = Full Temp. Range	140 180	– –	– –	ns
LSB Strobe into Input Register to Load DAC Register Time	t_{ASB}		0	–	–	ns
CLR Pulse Width	t_{CLR}		80	–	–	ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All Digital Inputs = V_{IH} or V_{IL} All Digital Inputs = 0V or V_{DD}	– –	– –	2 0.1	mA
Power Dissipation	P_D	Digital Inputs = 0V or V_{DD} 5V x 0.1mA Digital Inputs = V_{IH} or V_{IL} 5V x 2mA	– –	– –	0.5 10	mW

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT1}; all digital inputs = V_{IL}, V_{REF} = +10V; Specification also applies for I_{OUT2} when all digital inputs = V_{IH}.
5. Guaranteed by design and not tested.
6. I_{OUT1} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: ts = propagation delay (t_{PD}) +9τ, where τ equals measured time constant of the final RC decay.
7. V_{REF} = +10V, all digital inputs = 0V.
8. Absolute temperature coefficient is less than +300ppm/°C.
9. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
10. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
11. All digital inputs = 0V.
12. Calculated from worst case R_{REF}: I_{ZSE} (in LSBs) = (R_{REF} x I_{LKG} x 4096) /V_{REF}.
13. Calculations from $e_n = \sqrt{4K\,TRB}$ where: K = Boltzmann constant, J/°KR = resistance Ω T = resistor temperature, °K B = bandwidth, Hz
14. Minimum low time pulse width for STB_1, STB_2, and STB_4, and minimum high time pulse width for STB_3.
15. Measured from active strobe edge (STB) to new data output at SRO; C_L =50pF.

DICE CHARACTERISTICS



DIE SIZE 0.099 x 0.107 inch, 10,543 sq. mils
(2.51 x 2.72 mm, 6.83 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. STB_1
5. $\overline{LD_1}$
6. SR0
7. SRI
8. $\overline{STB_2}$
9. $\overline{LD_2}$
10. $\overline{STB_3}$
11. STB_4
12. DGND
13. $\overline{CLR}$
14. V_{DD} (Substrate)
15. V_{REF}
16. R_{FB}

Substrate (die backside) is internally connected to V_{DD}.

For additional DICE information, refer to 1990/91 Data Book, Section 2.

2

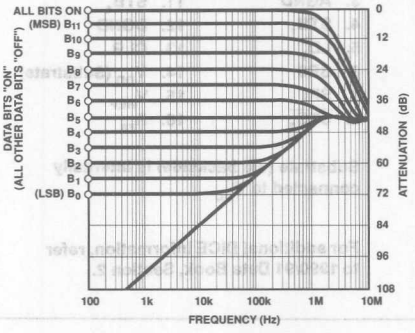
WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8143G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}	V_{REF} pad	7/15	kΩ MIN/MAX
DIGITAL INPUTS/OUTPUT				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA MAX
Digital Output HIGH	V_{OH}	I_{OH} = –200µA	4	V MIN
Digital Output LOW	V_{OL}	I_{OL} = 1.6mA	0.4	V MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2.0 0.1	mA MAX

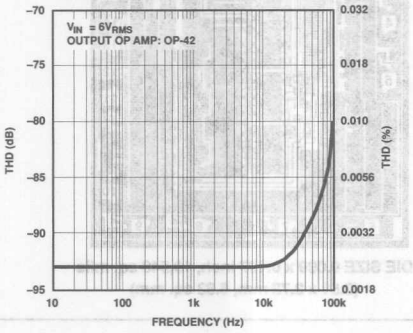
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

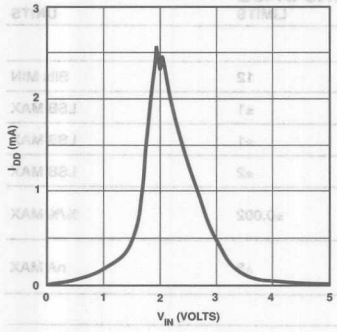
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



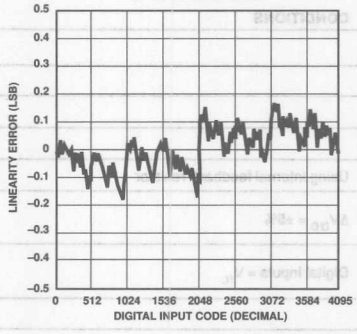
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



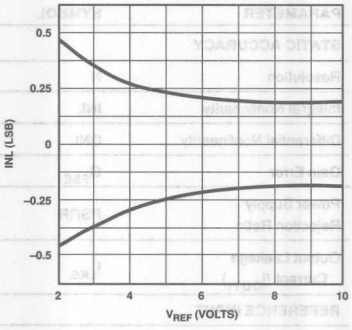
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



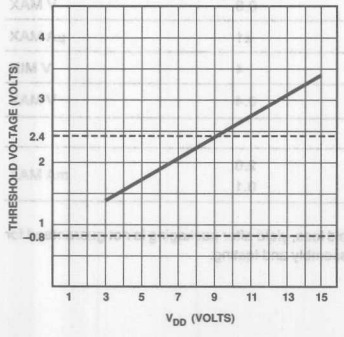
LINEARITY ERROR vs DIGITAL CODE



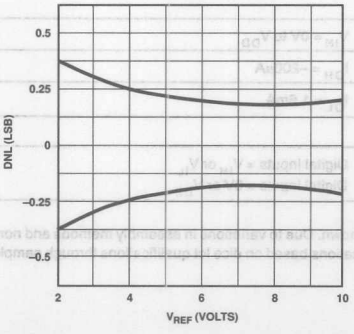
LINEARITY ERROR vs REFERENCE VOLTAGE



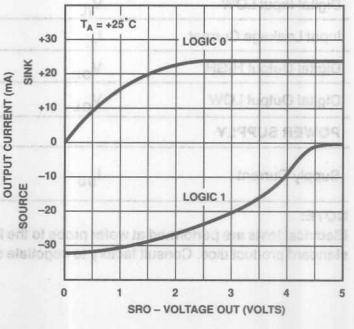
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



DIGITAL OUTPUT VOLTAGE vs OUTPUT CURRENT



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e., zero to full-scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} to ground.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

Refer to PMI 1988 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT INFORMATION

The DAC-8143 is a 12-bit serial-input, buffered serial-output, multiplying CMOS D/A converter. It has an R-2R resistor ladder network, a 12-bit input shift register, 12-bit DAC register, control logic circuitry, and a buffered digital output stage.

The control logic forms an interface in which serial data is loaded, under microprocessor control, into the input shift register and then transferred, in parallel, to the DAC register. In addition, buffered serial output data is present at the SRO pin when input data is loaded into the input register. This buffered data follows the digital input data (SRI) by 12 clock cycles and is available for daisy-chaining additional DACs.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

A simplified circuit of the DAC-8143 is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches. These switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It was essential to design these switches such that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10Ω, switch 2 for 20Ω, etc., a constant 5mV drop would then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches were included in series with the feedback resistor and the R-2R ladder's terminating resistor. The Simplified DAC Circuit, Figure 1, shows the location of these switches. These series switches are equivalently scaled to two times switch 1 (MSB) and top switch 12 (LSB) to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

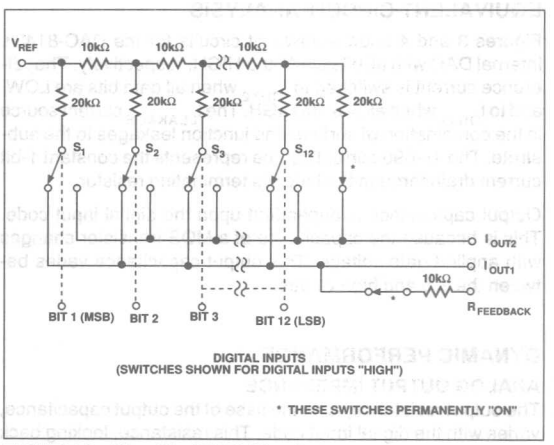


FIGURE 1: *Simplified DAC Circuit*

The DAC-8143 digital inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes were designed to clamp the inputs well below dangerous levels during static discharge conditions.

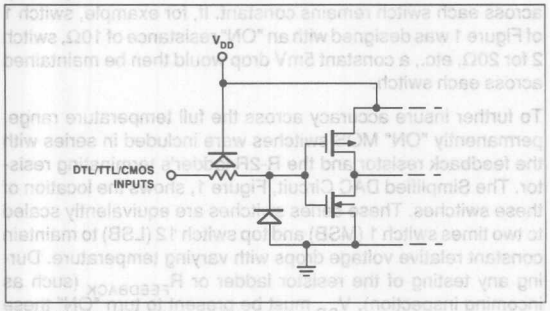


FIGURE 2: *Digital Input Protection*

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC-8143's internal DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW, and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the capacitance of a MOS transistor changes with applied gate voltage. This output capacitance varies between the low and high values.

DYNAMIC PERFORMANCE

ANALOG OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT1} terminal, varies between 11kΩ (the feedback resistor alone when all digital input are LOW) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations.

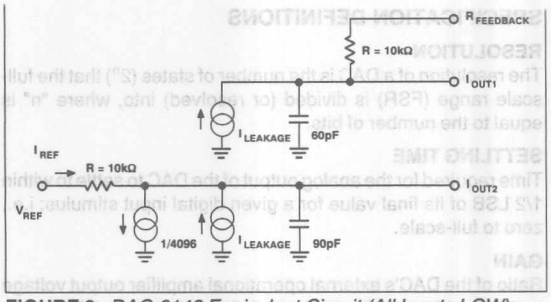


FIGURE 3: *DAC-8143 Equivalent Circuit (All Inputs LOW)*

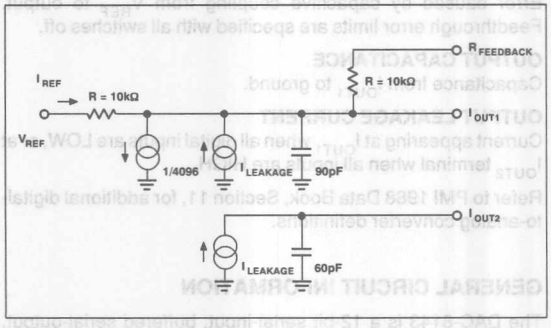


FIGURE 4: *DAC-8143 Equivalent Circuit (All Inputs HIGH)*

The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC-8143. The use of a small compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 7 and 8).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 5-30pF) should be used across the amplifiers to minimize overshoot and ringing. For low speed or static applications,

AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

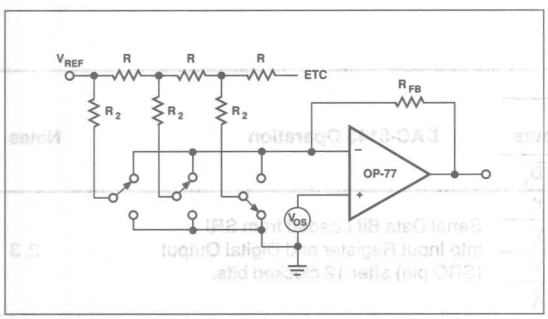


FIGURE 5: *Simplified Circuit*

Where RO is a function of the digital code, and :

R_O = 10kΩ for more than four bits of logic 1,
R_O = 30kΩ for any single bit of logic 1.

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{ERROR_1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$$

at code 0100 0000 0000,

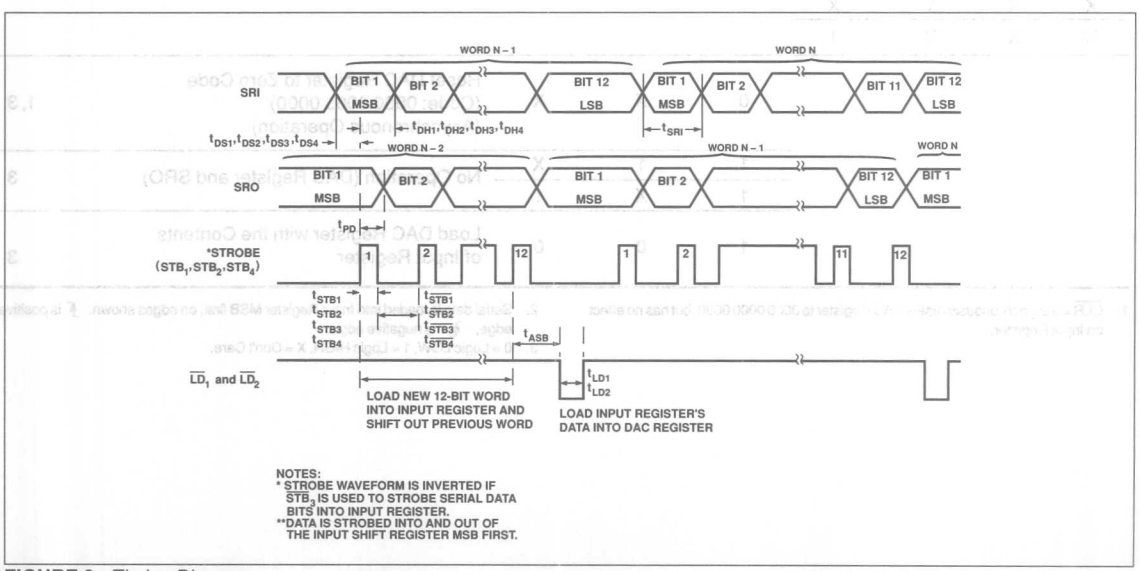
$$V_{ERROR_2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3\,V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = +10V) of 2.4mV for the DAC-8143, it is clearly important that V_{OS} be minimized, using either the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-97, OP-07, OP-27, and OP-42.

INTERFACE LOGIC OPERATION

The microprocessor interface of the DAC-8143 has been designed with multiple STROBE and LOAD inputs to maximize interfacing options. Control signals decoding may be done on-chip or with the use of external decoding circuitry (see Figure 12).



NOTES:
* STROBE WAVEFORM IS INVERTED IF $\overline{STB_3}$ IS USED TO STROBE SERIAL DATA BITS INTO INPUT REGISTER.
**DATA IS STROBED INTO AND OUT OF THE INPUT SHIFT REGISTER MSB FIRST.

FIGURE 6: *Timing Diagram*

Serial data is clocked into the input register and buffered output stage with STB_1, STB_2, or STB_4. The strobe inputs are active on the rising edge. $\overline{STB_3}$ may be used with a falling edge clock data.

Serial data output (SRO) follows the serial data input (SRI) by 12 clocked bits.

Holding any STROBE input at its selected state (i.e., STB_1, STB_2 or STB_4 at logic HIGH or STB_3 at logic LOW) will act to prevent any further data input.

When a new data word has been entered into the input register, it is transferred to the DAC register by asserting both LOAD inputs.

The $\overline{CLR}$ input allows asynchronous resetting of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{REF}$.

INTERFACE INPUT DESCRIPTION

STB_1 (Pin 4), STB_2 (Pin 8), STB_4 (Pin 11) – Input Register and Buffered Output Strobe. Inputs Active on Rising Edge. Selected to load serial data into input register and buffered output stage. See Table 1 for details.

$\overline{STB_3}$ (Pin 10) – Input Register and Buffered Output Strobe Input. Active on Falling Edge. Selected to load serial data into input register and buffered output stage. See Table 1 for details.

$\overline{LD_1}$ (Pin 5), $\overline{LD_2}$ (Pin9) – Load DAC Register Inputs. Active Low. Selected together to load contents of input register into DAC register.

$\overline{CLR}$ (Pin 13) – Clear Input. Active Low. Asynchronous. When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

TABLE 1: DAC-8143 Truth Table

DAC-8143 Logic Inputs							DAC-8143 Operation	Notes
Input Register/ Digital Output		Control Inputs		DAC Register Control Inputs				
STB_4	$\overline{STB_3}$	STB_2	STB_1	$\overline{CLR}$	$\overline{LD_2}$	$\overline{LD_1}$		
0	1	0	↑	X	X	X	Serial Data Bit Loaded from SRI into Input Register and Digital Output (SRO pin) after 12 clocked bits.	2, 3
0	1	↑	0	X	X	X		
0	↓	0	0	X	X	X		
↑	1	0	0	X	X	X		
1	X	X	X				No Operation (Input Register and SRO)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Reset DAC Register to Zero Code (Code: 0000 0000 0000) (Asynchronous Operation)	1, 3
				1	1	X	No Operation (DAC Register and SRO)	3
				1	X	1		
				1	0	0	Load DAC Register with the Contents of Input Register	3

1. $\overline{CLR}$ = 0 asynchronously resets DAC Register to 0000 0000 0000, but has no effect on Input Register.
2. Serial data is loaded into Input Register MSB first, on edges shown. ↑ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

APPLICATIONS INFORMATION

UNIPOLAR OPERATON (2-QUADRANT)

The circuit shown in Figures 7 and 8 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and +10(4095/4096)V depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The V_{REF} voltage range is the maximum input voltage range of the op amp or ±25V, whichever is lowest.

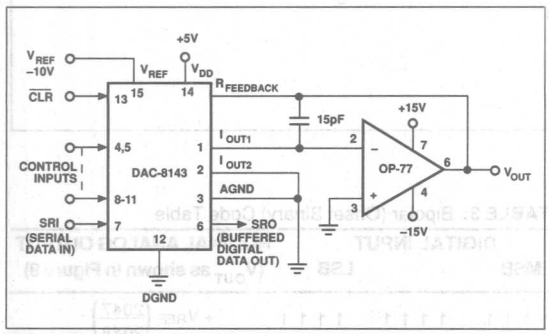


FIGURE 7: *Unipolar Operation with High Accuracy Op Amp (2-Quadrant)*

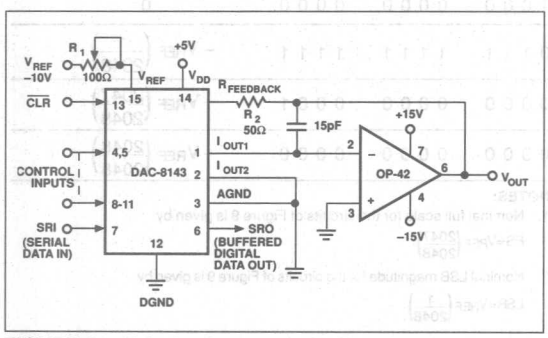


FIGURE 8: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

In many applications, the DAC-8143's zero scale error and low gain error, permit the elimination of external trimming components without adverse effects on circuit performance.

For applications requiring a tighter gain error than 0.024% at 25°C for the top grade part, or 0.048% for the lower grade part, the circuit in Figure 8 may be used. Gain error may be trimmed by adjusting R_1.

The DAC register must first be loaded with all 1s. R_1 is then adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

TABLE 2: Unipolar Code Table

DIGITAL INPUT MSB		LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 7 and 8)
1 1 1 1	1 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0	0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{2049}{4096}\right)$
1 0 0 0	0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{2047}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 7 and 8 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 7 and 8 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$

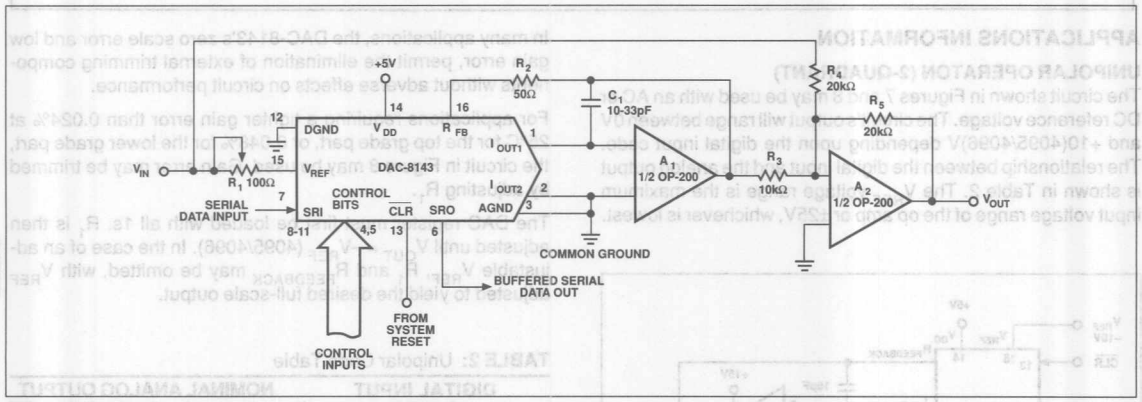


FIGURE 9: *Bipolar Operation (4-Quadrant, Offset Binary)*

BIPOLAR OPERATION (4-QUADRANT)

Figure 9 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input-to-analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB intput.

Resistor R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient match. Mismatching between R_3 and R_4 causes offset and full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted by adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and adjusting either the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

DAISY-CHAINING DAC-8143s

Many applications use multiple serial-input DACs that use numerous inter-connecting lines for address decoding and data

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB			LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 9)
1 1 1 1	1 1 1 1	1 1 1 1		$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0	0 0 0 0	0 0 0 1		$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0	0 0 0 0	0 0 0 0		0
0 1 1 1	1 1 1 1	1 1 1 1		$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0	0 0 0 0	0 0 0 1		$-V_{REF}\left(\frac{2047}{2048}\right)$
0 0 0 0	0 0 0 0	0 0 0 0		$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuits of Figure 9 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuits of Figure 9 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

lines. In addition, they use some type of buffering to reduce loading on the bus. The DAC-8143 is ideal for just such an application. It not only reduces the number of inter-connecting lines, but also reduces bus loading. The DAC-8143 can be daisy-chained with only three lines: one data line, one CLK line, and one Load line, see Figure 10.

ANALOG/DIGITAL DIVISION

The transfer function for the DAC-8143 connect in the multiplying mode as shown in Figures 7 and 8 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 11 and is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON" the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1}, I_{OUT2}, and AGND (pins 1, 2 and 3)being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 7 and 8). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than ±200µV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

It is recommended that the digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital input pass through the transition region (see the Supply Current vs. Logic Input Voltage graph under the Typical Performance Characteristics). The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e., rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

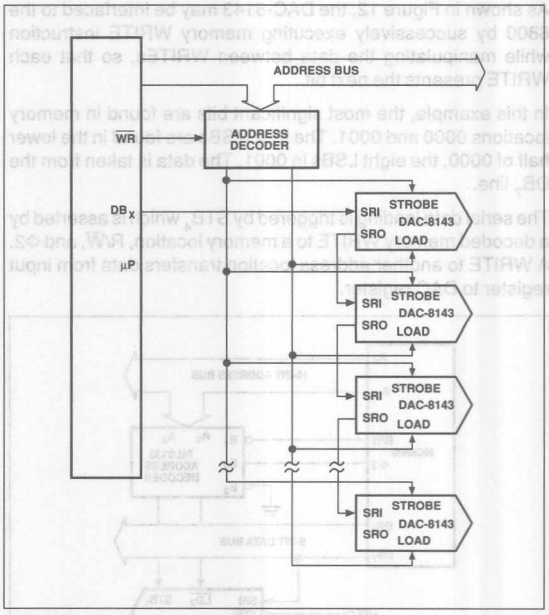


FIGURE 10: *Multiple DAC-8143s with 3-Wire Interface*

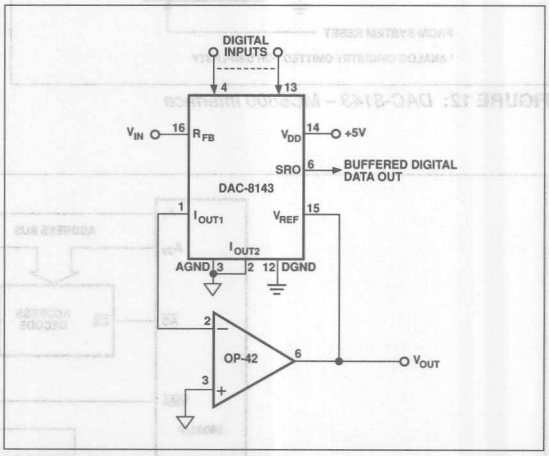


FIGURE 11: *Analog/Digital Divider*

INTERFACING TO THE MC6800

As shown in Figure 12, the DAC-8143 may be interfaced to the 6800 by successively executing memory WRITE instruction while manipulating the data between WRITEs, so that each WRITE presents the next bit.

In this example, the most significant bits are found in memory locations 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the DB_7 line.

The serial data loading is triggered by STB_4 which is asserted by a decoded memory WRITE to a memory location, R/$\overline{W}$, and $\Phi 2$. A WRITE to another address location transfers data from input register to DAC register.

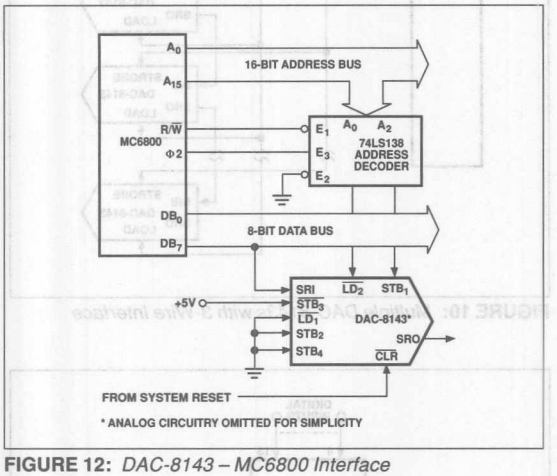


FIGURE 12: *DAC-8143 – MC6800 Interface*

DAC-8143 INTERFACE TO THE 8085

The DAC-8143's interface to the 8085 microprocessor is shown in Figure 13. Note that the microprocessor's SOD line is used to present data serially to the DAC.

Data is strobed into the DAC-8143 by executing memory write instructions. The strobe 2 input is generated by decoding an address location and $\overline{WR}$. Data is loaded into the DAC register with a memory write instruction to another address location.

Serial data supplied to the DAC-8143 must be present in the right-justified format in registers H and L of the microprocessor.

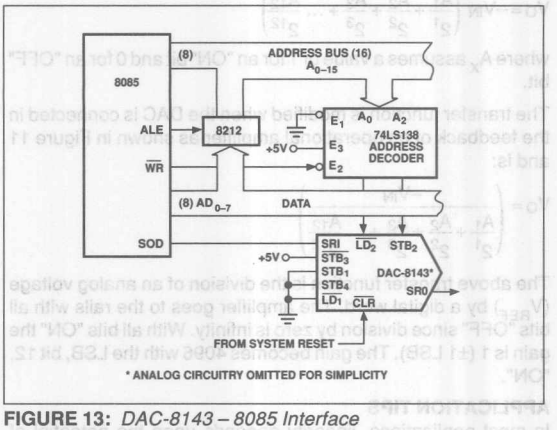


FIGURE 13: *DAC-8143 – 8085 Interface*

DAC-8143 INTERFACE TO THE 68000

Figure 14 shows the DAC-8143 configured to the 68000 microprocessor. Serial data input is similar to that of the 6800 in Figure 12.

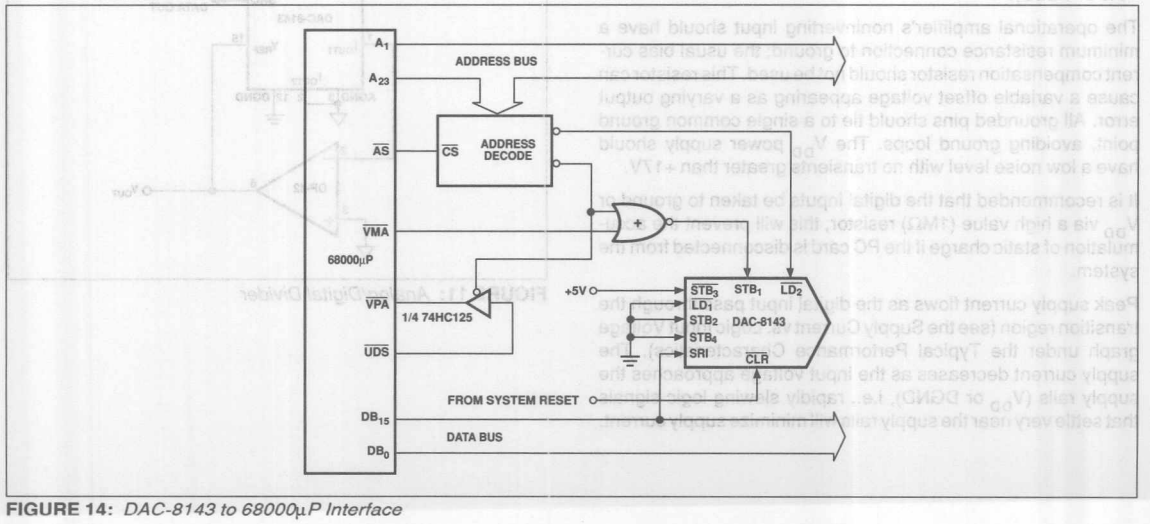


FIGURE 14: *DAC-8143 to 68000μP Interface*

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Packaged in a Narrow 0.3" 24-Pin DIP
- Direct Parallel Load of All 12 Bits for High DataThroughput
- On-Chip Latches for Both DACs
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 0.2% Typically
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Robotics/Process Control
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8221AW	DAC8221EW	–
±1/2 LSB	±2 LSB	–	–	DAC8221GP
±1 LSB	±4 LSB	–	DAC8221FW	DAC8221HP
±1 LSB	±4 LSB	–	DAC8221FP	DAC8221HS††

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

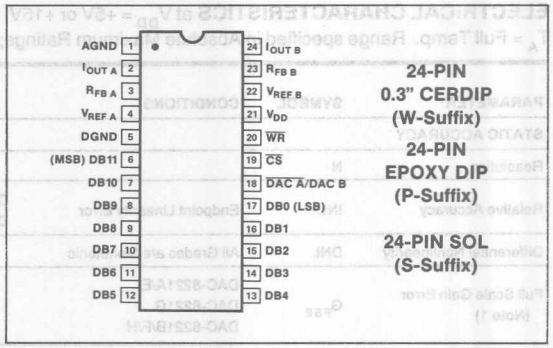
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

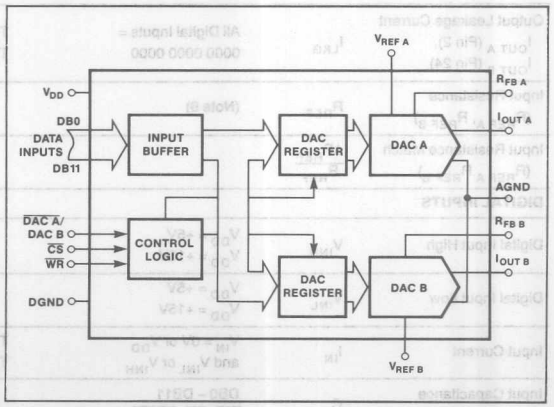
The DAC-8221 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. This device is electrically similar to DAC-8212 with improved microprocessor interface timing and is packaged in a narrow 0.300" DIP. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8221 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8221 operates on a single supply from +5V to +15V. Maximum power dissipation with 0V and +5V logic levels and a +5V supply is less than 0.5mW. The DAC-8221 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit or wider bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic LOW, the input data registers are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A}$/DAC B control input. For applications requiring double-buffering, see the DAC-8222.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF\ A}$, $V_{REF\ B}$ to AGND ..... ±25V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +5V or +15V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp. Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS		DAC-8221 MIN	DAC-8221 TYP	DAC-8221 MAX	UNITS
STATIC ACCURACY							
Resolution	N			12	–	–	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8221A/E/G	–	±0.2	±1/2	LSB
			DAC-8221B/F/H	–	±0.4	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic		–	±0.2	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8221A/E		–	±0.1	±1	LSB
		DAC-8221G		–	±0.4	±2	
		DAC-8221B/F/H		–	±0.6	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)		–	±2	±5	ppm/°C
Output Leakage Current $I_{OUT\ A}$ (Pin 2), $I_{OUT\ B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C	–	±1	±10	nA
			T_A = Full Temp. Range	–	±2	±50	
Input Resistance ($R_{REF\ A}$, $R_{REF\ B}$)	R_{REF}	(Note 9)		8	22	15	kΩ
Input Resistance Match ($R_{REF\ A}$ $R_{REF\ B}$)	$\frac{\Delta R_{REF}}{R_{REF}}$			–	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5V		2.4	–	–	V
		V_{DD} = +15V		13.5	–	–	
Digital Input Low	V_{INL}	V_{DD} = +5V		–	–	0.8	V
		V_{DD} = +15V		–	–	1.5	
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH}	T_A = +25°C	–	±0.006	±1	μA
			T_A = Full Temp. Range	–	±0.1	±10	
Input Capacitance (Note 2)	C_{IN}	DB0 – DB11		–	–	10	pF
		$\overline{WR}$, $\overline{CS}$, DAC A/DAC B		–	–	15	

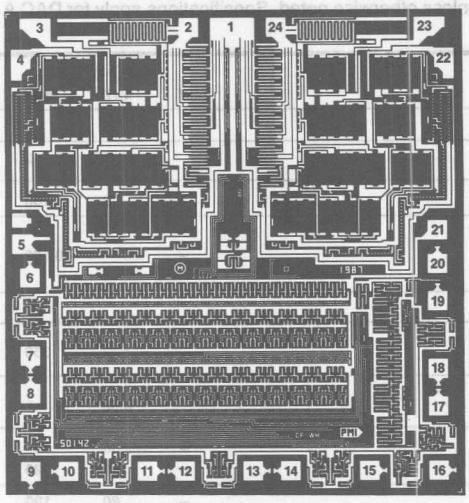
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\,A} = V_{REF\,B}$ = +10V, $V_{OUT\,A} = V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8221 MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	–	1	2	mA
		All Digital Inputs 0V or V_{DD}	–	2	100	µA
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{pd}	T_A = +25°C	–	–	350	ns
Current Settling Time (Notes 5, 6)	t_s	T_A = +25°C	–	0.45	1	µs
Output Capacitance	$C_{OUT\,A}$ $C_{OUT\,B}$	DAC Latches Loaded with 0000 0000 0000	– –	30 60	90 120	pF
	$C_{OUT\,A}$ $C_{OUT\,B}$	DAC Latches Loaded with 1111 1111 1111	– –	60 30	120 90	
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	

SWITCHING CHARACTERISTICS (Notes 2, 3)		V_{DD} = +5V +25°C	–40°C TO +85°C (Note 8)	–55°C TO +125°C	V_{DD} = +15V ALL TEMPS (Note 10)	
Chip Select to Write Set-Up Time	t_{CS}	130	160	160	70	ns MIN
Chip Select to Write Hold Time	t_{CH}	0	0	0	0	ns MIN
DAC Select to Write Set-Up Time	t_{AS}	120	140	160	70	ns MIN
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns MIN
Data Valid to Write Set-Up Time	t_{DS}	190	210	220	90	ns MIN
Data Valid to Write Hold Time	t_{DH}	0	0	0	10	ns MIN
Write Pulse Width	t_{WR}	140	180	170	90	ns MIN

NOTES:
1. Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. See timing diagram.
4. From 50% of digital input to 90% of final analog output current. $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
5. $\overline{WR}$, $\overline{CS}$ = 0V; DB0 – DB11 = 0V to V_{DD} or V_{DD} to 0V.
6. Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
7. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
8. These limits apply for the commercial and industrial grade products.
9. Absolute temperature coefficient is approximately +50ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

DICE CHARACTERISTICS



DIE SIZE 0.124 x 0.132 inch, 16,368 sq. mils
(3.15 x 3.35 mm, 10.55 sq. mm)

1. AGND
2. $I_{OUT\ A}$
3. $R_{FB\ A}$
4. $V_{REF\ A}$
5. DGND
6. DB11 (MSB)
7. DB10
8. DB9
9. DB8
10. DB7
11. DB6
12. DB5
13. DB4
14. DB3
15. DB2
16. DB1
17. DB0 (LSB)
18. $\overline{\text{DAC A/DAC B}}$
19. $\overline{\text{CS}}$
20. $\overline{\text{WR}}$
21. V_{DD}
22. $V_{REF\ B}$
23. $R_{FB\ B}$
24. $I_{OUT\ B}$

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF\ A} = V_{REF\ B}$ = +10V, $V_{OUT\ A} = V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = 25°C.

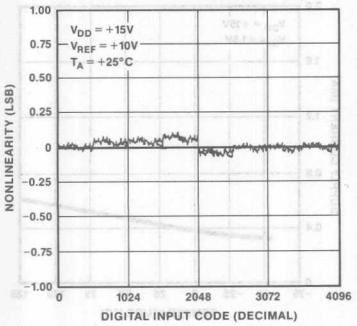
			DAC-8221GBC	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB MAX
Full Scale Gain Error (Note 1)	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage ($I_{OUT\ A}$, $I_{OUT\ B}$)	I_{LKG}	Digital Inputs = 0000 0000 0000 Pads 2 and 24	±10	nA MAX
Input Resistance ($R_{REF\ A}$, $R_{REF\ B}$)	R_{REF}	Pads 4 and 22	8/15	kΩMIN/ kΩMAX
$R_{REF\ A}$, $R_{REF\ B}$ Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% MAX
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}; V_{INL} or V_{INH}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%	0.002	%/% MAX

NOTES:
1. Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$.

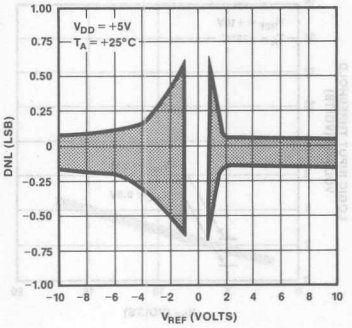
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

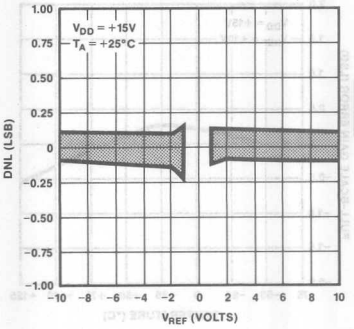
CHANNEL-TO-CHANNEL MATCHING (DAC A & B ARE SUPERIMPOSED)



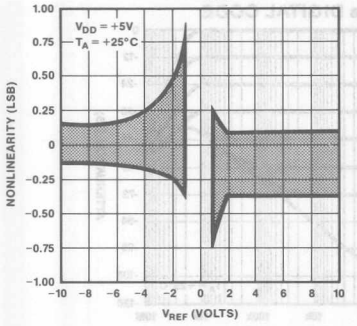
DIFFERENTIAL NONLINEARITY vs V_{REF}



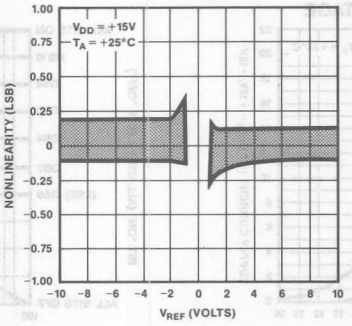
DIFFERENTIAL NONLINEARITY vs V_{REF}



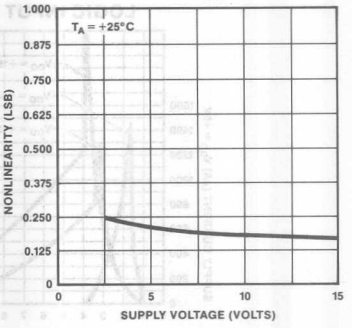
NONLINEARITY vs V_{REF}



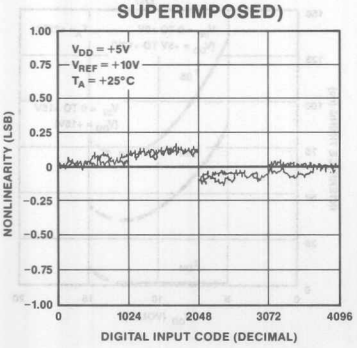
NONLINEARITY vs V_{REF}



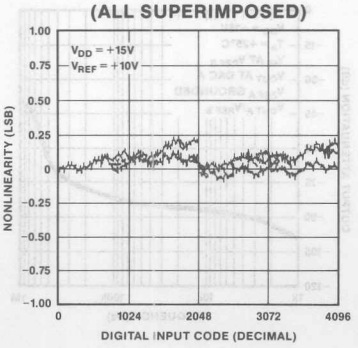
NONLINEARITY vs V_{DD}



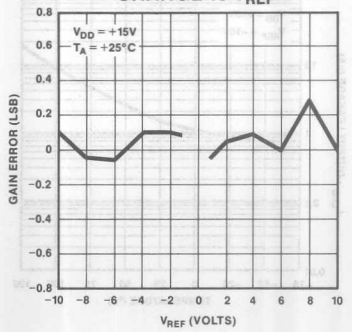
NONLINEARITY vs CODE (DAC A & B ARE SUPERIMPOSED)



NONLINEARITY vs CODE AT T_A = −55°C, +25°C, +125°C FOR DAC A & B (ALL SUPERIMPOSED)

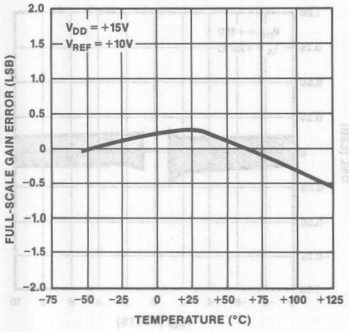


ABSOLUTE GAIN ERROR CHANGE vs V_{REF}

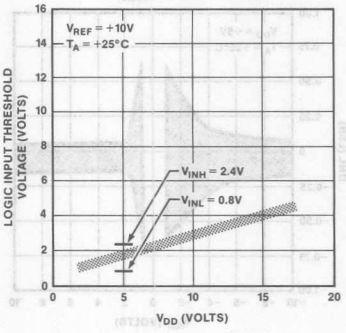


TYPICAL PERFORMANCE CHARACTERISTICS

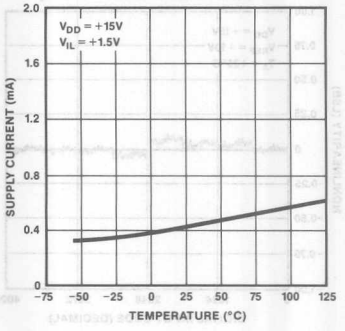
FULL-SCALE GAIN ERROR vs TEMPERATURE



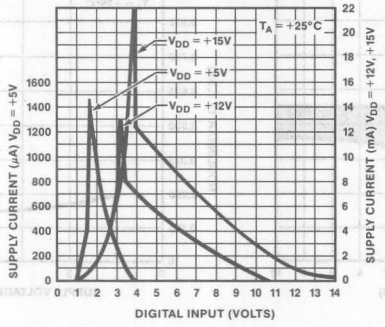
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



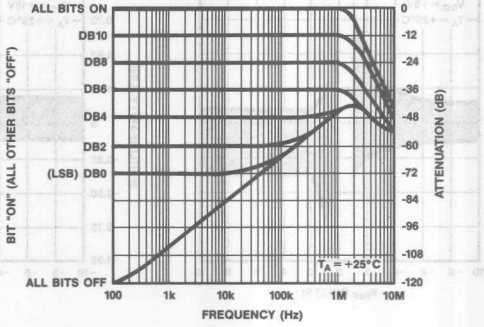
SUPPLY CURRENT vs TEMPERATURE



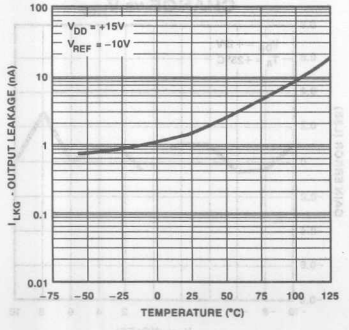
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



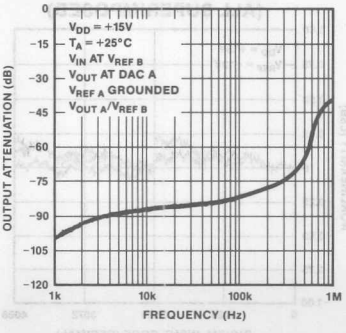
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



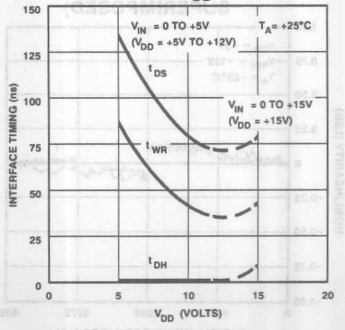
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



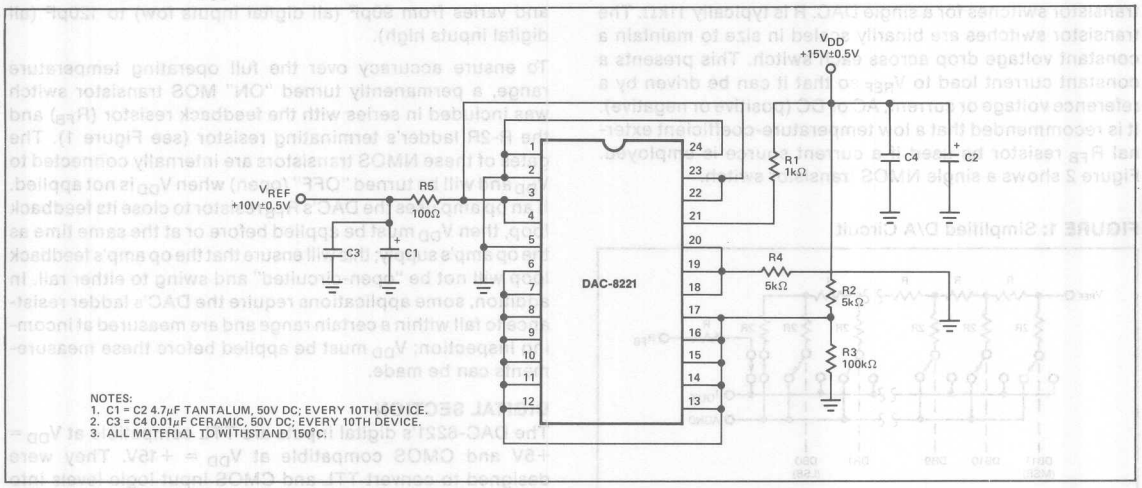
ANALOG CROSSTALK vs FREQUENCY



INTERFACE TIMING vs V_{DD}

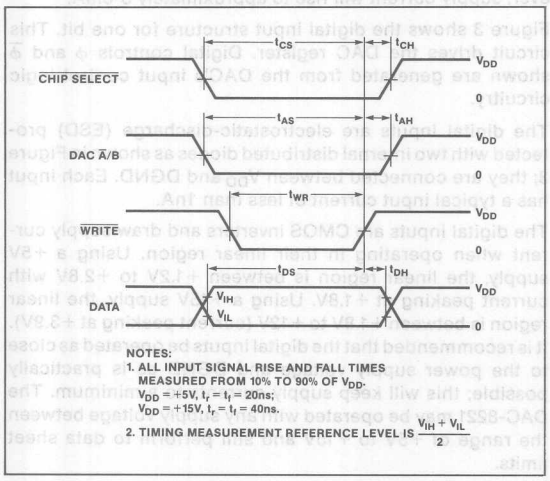


BURN-IN CIRCUIT



NOTES:
1. C1 = C2 4.7μF TANTALUM, 50V DC; EVERY 10TH DEVICE.
2. C3 = C4 0.01μF CERAMIC, 50V DC; EVERY 10TH DEVICE.
3. ALL MATERIAL TO WITHSTAND 150°C.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
   V_{DD} = +5V, $t_r = t_f$ = 20ns;
   V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

Refer to PMI 1990/91 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC-8221 incorporates two multiplying 12-bit current output CMOS digital-to-analog converters on one monolithic chip. It contains two highly-stable thin-film R-2R resistor-ladder networks, two 12-bit DAC registers, and one 12-bit input buffer. It also contains the DAC control logic circuitry and 24 single-pole, double-throw NMOS transistor current switches.

transistor switches for a single DAC. R is typically 11kΩ. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. This presents a constant current load to V_{REF} so that it can be driven by a reference voltage or current, AC or DC (positive or negative). It is recommended that a low temperature-coefficient external R_{FB} resistor be used if a current source is employed. Figure 2 shows a single NMOS transistor switch.

FIGURE 1: Simplified D/A Circuit

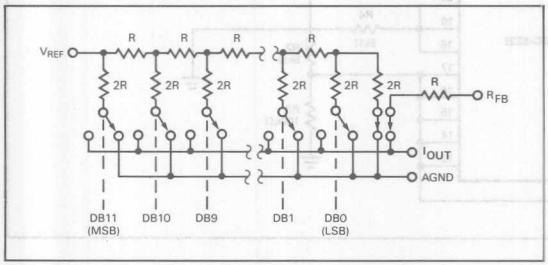
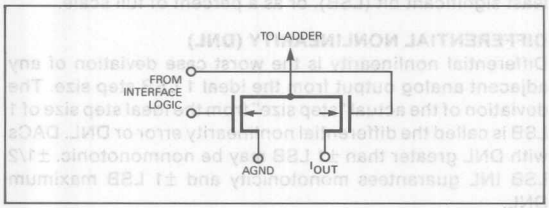


FIGURE 2: N-Channel Current Steering Switch



The binary-weighted currents are switched between I_{OUT} and AGND by the transistor switches. Selection between I_{OUT} and AGND is determined by the digital input code. It is important to keep the voltage difference between I_{OUT} and AGND terminals as close to zero as practical to preserve data sheet limits. It is easily accomplished by connecting the DAC's AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The amplifier's feedback resistor can be eliminated by connecting the op amp's output directly to the DAC's R_{FB} terminal (by using the DAC's internal feedback resistor, R_{FB}), see Figure 6. The amplifier also provides the current-to-voltage conversion for the DAC's output current.

The output voltage is dependent on V_{REF} and the digital input code and is given by:

$$V_{OUT} = -V_{REF} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

and varies from 90pF (all digital inputs low) to 120pF (all digital inputs high).

To ensure accuracy over the full operating temperature range, a permanently turned "ON" MOS transistor switch was included in series with the feedback resistor (R_{FB}) and the R-2R ladder's terminating resistor (see Figure 1). The gates of these NMOS transistors are internally connected to V_{DD} and will be turned "OFF" (open) when V_{DD} is not applied. If an op amp uses the DAC's R_{FB} resistor to close its feedback loop, then V_{DD} must be applied before or at the same time as the op amp's supply; this will ensure that the op amp's feedback loop will not be "open-circuited" and swing to either rail. In addition, some applications require the DAC's ladder resistance to fall within a certain range and are measured at incoming inspection; V_{DD} must be applied before these measurements can be made.

DIGITAL SECTION

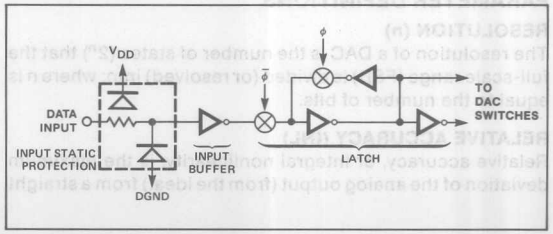
The DAC-8221's digital inputs are TTL compatible at $V_{DD} = +5V$ and CMOS compatible at $V_{DD} = +15V$. They were designed to convert TTL and CMOS input logic levels into voltage levels that will drive the internal circuitry. The DAC-8221 can use +5V CMOS logic levels with $V_{DD} = +12V$; however, supply current will rise to approximately 5-6mA.

Figure 3 shows the digital input structure for one bit. This circuit drives the DAC register. Digital controls ϕ and $\overline{\phi}$ shown are generated from the DAC's input control logic circuitry.

The digital inputs are electrostatic-discharge (ESD) protected with two internal distributed diodes as shown in Figure 3; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

The digital inputs are CMOS inverters and draw supply current when operating in their linear region. Using a +5V supply, the linear region is between +1.2V to +2.8V with current peaking at +1.8V. Using a +15V supply, the linear region is between +1.8V to +12V (current peaking at +3.9V). It is recommended that the digital inputs be operated as close to the power supply voltage and DGND as is practically possible; this will keep supply currents to a minimum. The DAC-8221 may be operated with any supply voltage between the range of +5V to +15V and still perform to data sheet limits.

FIGURE 3: Digital Input Structure For One Bit



INTERFACE CONTROL LOGIC INFORMATION

DAC SELECTION

Both DAC registers share a common 12-bit input port. The control input ($\overline{\text{DAC A}}$/DAC B) selects which DAC can accept data from the input port.

MODE SELECTION

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to activity on DB0—DB11 pins.

HOLD MODE

The selected DAC register retains the data which was present on DB0—DB11 pins just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 4 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8221 and OP-270 dual op amp (use two OP-42s for applications requiring higher speeds). Table 1 shows the corresponding code table. Table 3 shows the recommended values for R1, R2, R3, and R4. Low temperature-coefficient (approximately 50ppm/°C) resistors or trimmers should be used. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device where $V_{REF} = \pm 10V$ is 0.048%, and 0.097% for the low grade. Capacitors C1 and C2 provide phase compensation to reduce overshoot and ringing when high-speed op amps are used.

TABLE 1: Unipolar Binary Code Table (Refer to Figure 4)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE:
1 LSB = $(2^{-12})(V_{REF}) = \frac{1}{4096}(V_{REF})$

FIGURE 4: Dual DAC Unipolar Operation (2-Quadrant Multiplication)

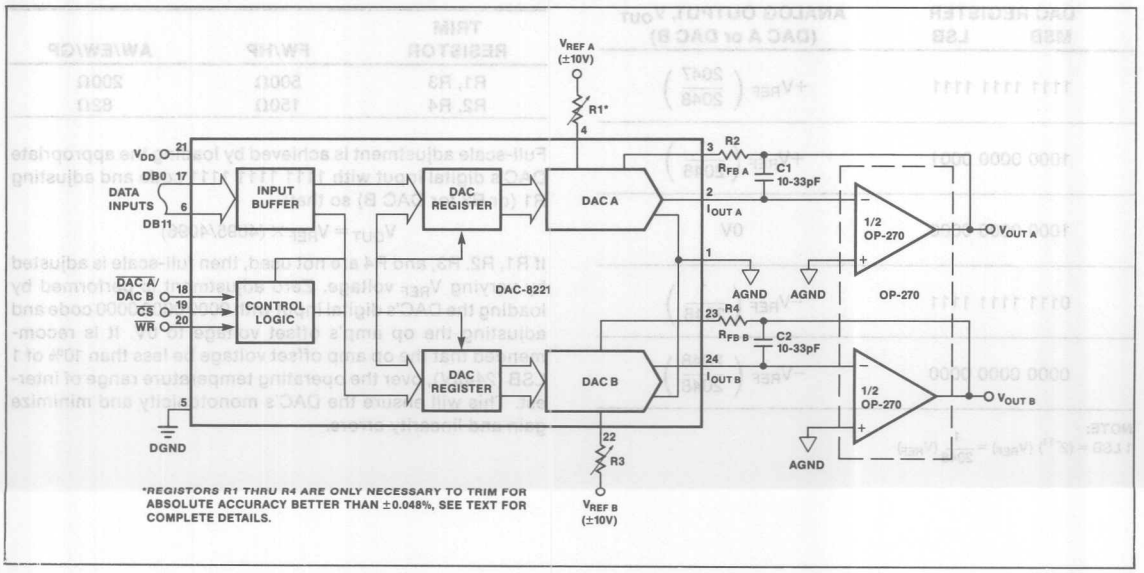


FIGURE 5: Dual DAC Bipolar Operation (4-Quadrant Operation)

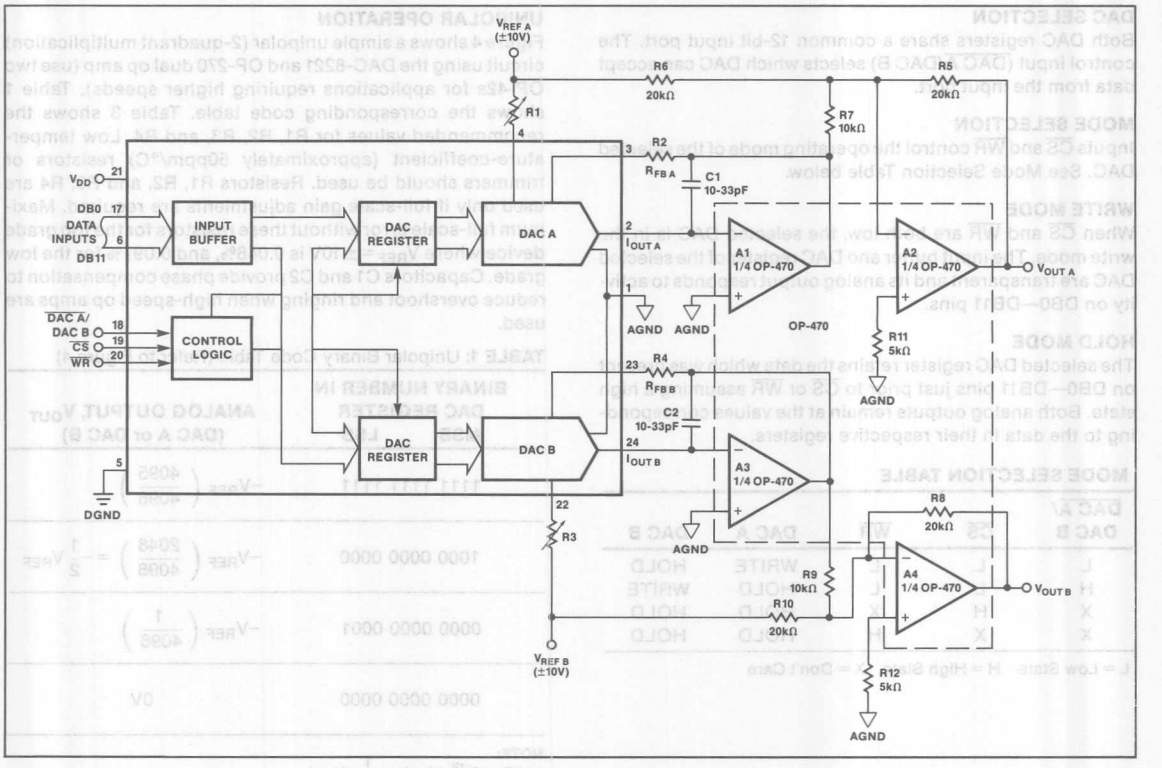


TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 5)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTE:
1 LSB = (2^{-11}) (V_{REF}) = $\frac{1}{2048}$ (V_{REF})

TABLE 3: Recommended Trim Resistor Values vs Grade for Figures 4 and 5

TRIM RESISTOR	FW/HP	AW/EW/GP
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

Full-scale adjustment is achieved by loading the appropriate DAC's digital input with 1111 1111 1111 code and adjusting R1 (or R3 for DAC B) so that:

$$V_{OUT} = V_{REF} \times (4095/4096)$$

If R1, R2, R3, and R4 are not used, then full-scale is adjusted by varying V_{REF} voltage. Zero adjustment is performed by loading the DAC's digital input with 0000 0000 0000 code and adjusting the op amp's offset voltage to 0V. It is recommended that the op amp offset voltage be less than 10% of 1 LSB (244μV), over the operating temperature range of interest. This will ensure the DAC's monotonicity and minimize gain and linearity errors.

BIPOLAR OPERATION

The bipolar (offset binary) 4-quadrant configuration using the DAC-8221 is shown in Figure 5, and the corresponding code is shown in Table 2. The circuit makes use of the OP-470, a quad op amp (use four OP-42s for applications requiring higher speeds).

Again, resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = \pm 10V$ is 0.048%, and 0.097% for the low grade. See Table 3 for the recommended values. If they are used, then low temperature-coefficient (approximately 50ppm/°C) resistors or trimmers should be used.

If resistors R1 thru R4 are omitted, then R5, R6, R7 (R8, R9, and R10 for DAC B) should be ratio-matched to 0.01% to keep gain error within data sheet limits. They should also have matching temperature-coefficient characteristics if operating over the full temperature range.

Zero-output is adjusted by loading the appropriate DAC's digital input with 1000 0000 0000 code and varying R1 (R3 for DAC B) so that $V_{OUT\,A}$ (or $V_{OUT\,B}$) equals 0V. If R1, R2 (R3, R4 for DAC B) are omitted, then zero output is adjusted by varying R6, R7 ratios (R9, R10 for DAC B). Full-scale is set by loading the appropriate DAC's digital inputs with 1111 1111 1111 code and varying R5 (R8 for DAC B) or V_{REF}.

SINGLE SUPPLY OPERATION

CURRENT SWITCHING MODE

Because the DAC-8221's R-2R resistor-ladder terminating resistor is internally connected to AGND, it lends itself well for single supply operation in the current steering mode configuration. This means that AGND can be raised above system ground as shown in Figure 6. The output voltage will swing between +5V and +10V depending on the digital input code.

The output expression is given by:

$$V_{OUT} = V_{OS} + (D/4096)(V_{OS})$$

where V_{OS} = Offset Reference Voltage (+5V in Figure 6)
D = Decimal Equivalent of the Digital Input Word

FIGURE 6: Single Supply Operation (Current Switching Mode)

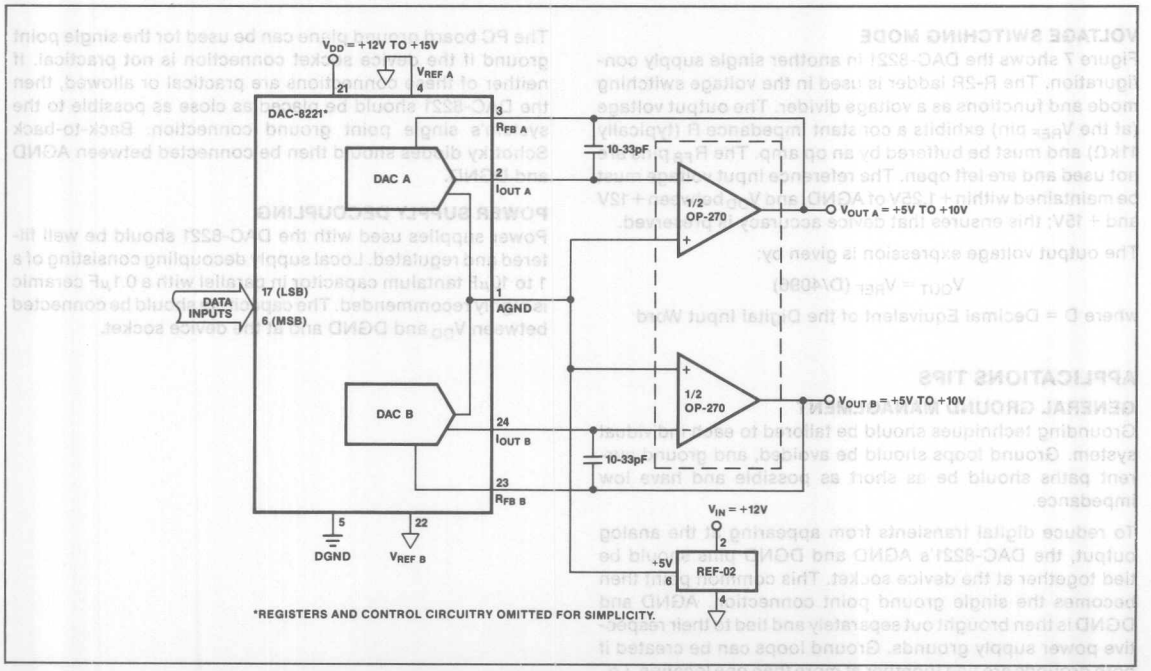
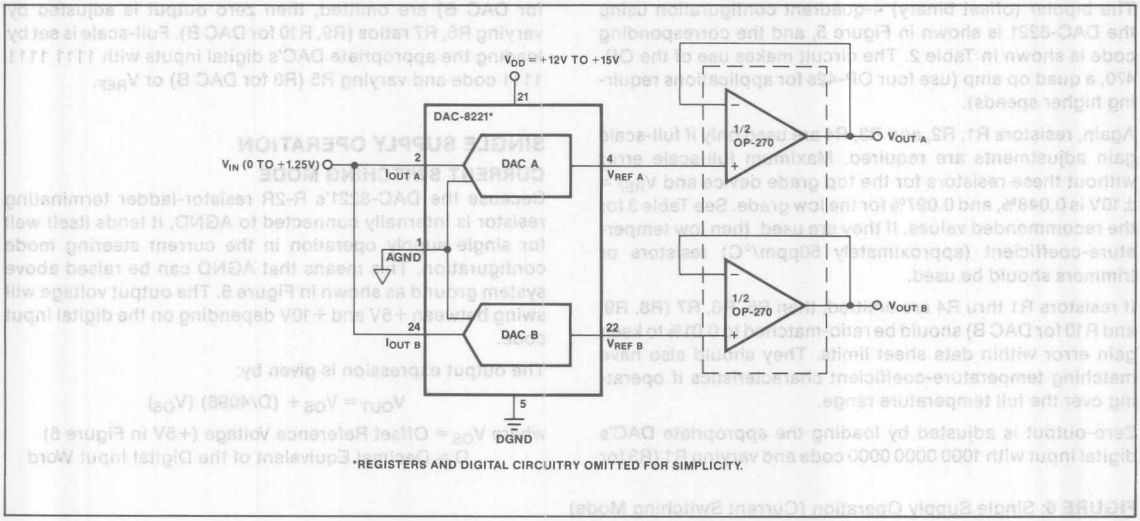


FIGURE 7: Single Supply Operation (Voltage Switching Mode)



VOLTAGE SWITCHING MODE

Figure 7 shows the DAC-8221 in another single supply configuration. The R-2R ladder is used in the voltage switching mode and functions as a voltage divider. The output voltage (at the V_{REF} pin) exhibits a constant impedance R (typically 11kΩ) and must be buffered by an op amp. The R_{FB} pins are not used and are left open. The reference input voltage must be maintained within +1.25V of AGND, and V_{DD} between +12V and +15V; this ensures that device accuracy is preserved.

The output voltage expression is given by:

$$V_{OUT} = V_{REF}\ (D/4096)$$

where D = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have low impedance.

To reduce digital transients from appearing at the analog output, the DAC-8221's AGND and DGND pins should be tied together at the device socket. This common point then becomes the single ground point connection. AGND and DGND is then brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

The PC board ground plane can be used for the single point ground if the device socket connection is not practical. If neither of these connections are practical or allowed, then the DAC-8221 should be placed as close as possible to the system's single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC-8221 should be well filtered and regulated. Local supply decoupling consisting of a 1 to 10μF tantalum capacitor in parallel with a 0.1μF ceramic is highly recommended. The capacitors should be connected between V_{DD} and DGND and at the device socket.

FIGURE 8: Digitally-Programmable Window Detector (Upper/Lower Limit Detector)

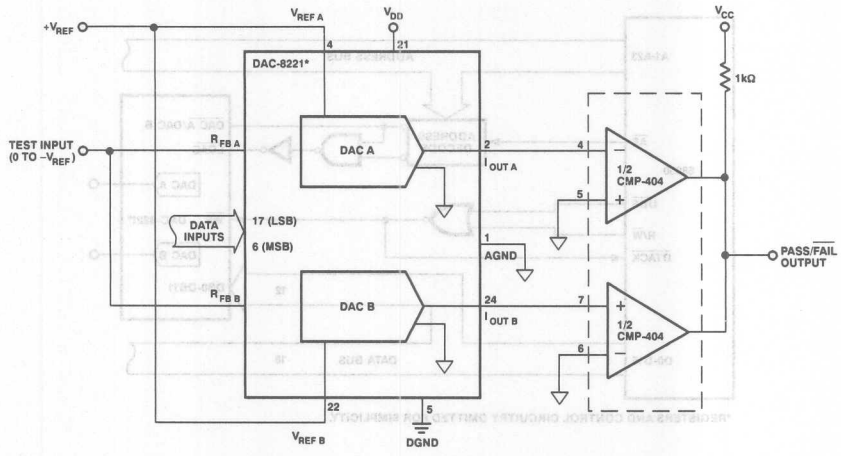


FIGURE 9: DAC-8221 To 8086 Interface

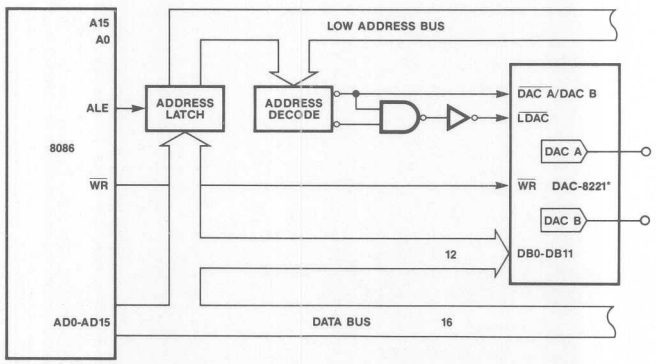
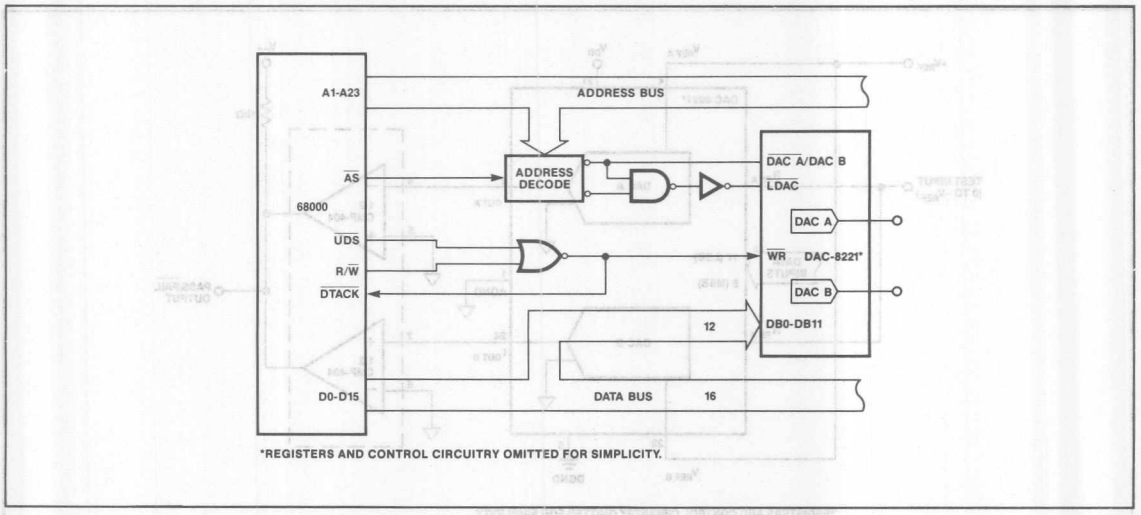


FIGURE 10: DAC-8221 To 68000 Interface



Dual 12-Bit Double-Buffered Multiplying CMOS D/A Converter

DAC-8222

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 1% Max
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Robotics/Process Control/Automation
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8222AW	DAC8222EW	–
±1/2 LSB	±2 LSB	–	–	DAC8222GP
±1 LSB	±4 LSB	–	DAC8222FW	DAC8222HP
±1 LSB	±4 LSB	–	DAC8222FP	DAC8222HS††

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

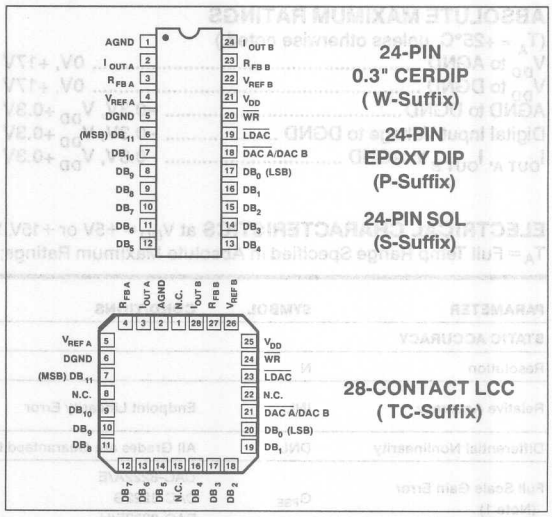
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

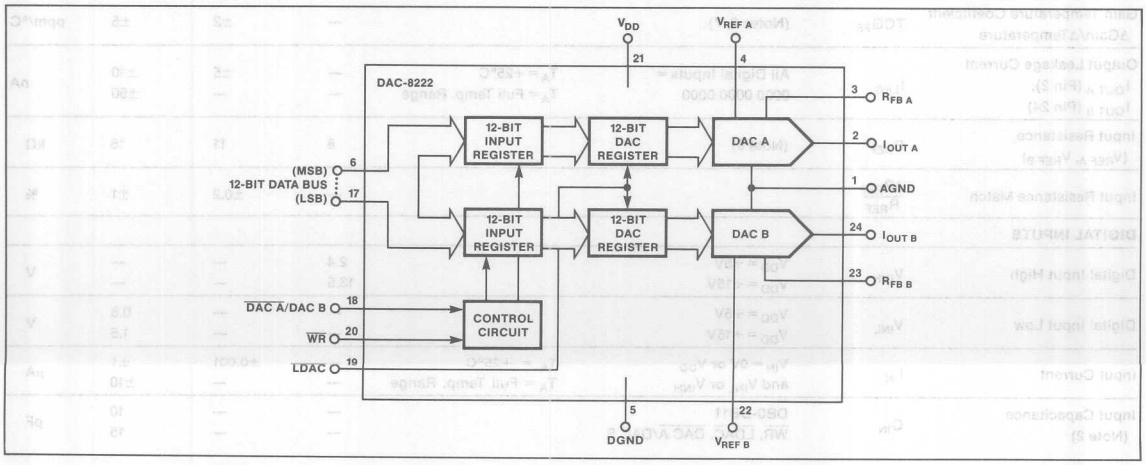
GENERAL DESCRIPTION

The DAC-8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC-8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC-8222 to be packaged in a narrow 24-pin 0.3" DIP and save PCB space.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



logic low at these inputs, the DAC registers become transparent. This allows direct unbuffered data to flow directly to either DAC output selected by DAC A/DAC B. Also, the DAC's double-buffered digital inputs will allow both DACs to be updated simultaneously.

DAC-8222's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The chip consists of two thin-film R-2R resistor ladder networks, four 12-bit registers, and DAC control logic circuitry. The device has separate reference-input and feedback resistors for each DAC and operates on a single supply from +5V to +15V. Maximum power dissipation at +5V using zero or V_{DD} logic levels is less than 0.5mW.

The DAC-8222 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +5V or +15V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range Specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS		DAC-8222 MIN	DAC-8222 TYP	DAC-8222 MAX	UNITS
STATIC ACCURACY							
Resolution	N			12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8222A/E/G	—	—	±1/2	LSB
			DAC-8222F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic		—	—	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8222A/E		—	—	±1	LSB
		DAC-8222G		—	—	±2	
		DAC-8222F/H		—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)		—	±2	±5	ppm/°C
Output Leakage Current $I_{OUT\ A}$ (Pin 2), $I_{OUT\ B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C	—	±5	±10	nA
			T_A = Full Temp. Range	—	—	±50	
Input Resistance ($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	(Note 9)		8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$			—	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5V		2.4	—	—	V
		V_{DD} = +15V		13.5	—	—	
Digital Input Low	V_{INL}	V_{DD} = +5V		—	—	0.8	V
		V_{DD} = +15V		—	—	1.5	
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH}	T_A = +25°C	—	±0.001	±1	μA
			T_A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 2)	C_{IN}	DB0-DB11		—	—	10	pF
		WR, LDAC, DAC A/DAC B		—	—	15	

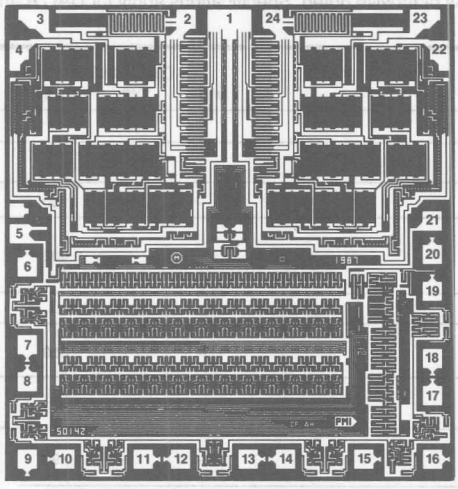
T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8222 MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	–	–	2	mA
		All Digital Inputs 0V or V_{DD}	–	10	100	µA
DC Power Supply Rejection Ration ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{PD}	T_A = +25°C	–	–	350	ns
Current Settling Time (Notes 5, 6)	t_s	T_A = +25°C	–	–	1	µs
Output Capacitance	C_O	Digital Inputs = All 0s $C_{OUT\ A}$, $C_{OUT\ B}$	–	–	90	pF
		Digital Inputs = All 1s $C_{OUT\ A}$, $C_{OUT\ B}$	–	–	120	
AC Feedthrough at $I_{OUT\ A}$ or $I_{OUT\ B}$	FT_A	$V_{REF\ A}$ to $I_{OUT\ A}$; $V_{REF\ A}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	dB
	FT_B	$V_{REF\ B}$ to $I_{OUT\ B}$; $V_{REF\ B}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	

SWITCHING CHARACTERISTICS (Notes 2, 3)	SYMBOL	V_{DD} = +5V +25°C	V_{DD} = +5V –40°C TO +85°C (Note 8)	V_{DD} = +5V –55°C TO +125°C	V_{DD} = +15V ALL TEMPS (Note 10)	
DAC Select to Write Set-Up Time	t_{AS}	150	180	210	60	ns MIN
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns MIN
LDAC to Write Set-Up Time	t_{LS}	80	100	120	60	ns MIN
LDAC to Write Hold Time	t_{LH}	20	20	20	20	ns MIN
Data Valid to Write Set-Up Time	t_{DS}	220	240	260	100	ns MIN
Data Valid to Write Hold Time	t_{DH}	0	0	0	10	ns MIN
Write Pulse Width	t_{WR}	130	160	170	90	ns MIN
LDAC Pulse Width	t_{LWD}	100	120	130	60	ns MIN

NOTES:
1. Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. See timing diagram.
4. From 50% of digital input to 90% of final analog output current. $V_{REF\ A}$ = $V_{REF\ B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
5. $\overline{WR}$, $\overline{LDAC}$ = 0V; DB0 – DB11 = 0V to V_{DD} or V_{DD} to 0V.
6. Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
7. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
8. These limits apply for the commercial and industrial grade products.
9. Absolute temperature coefficient is approximately +50ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

DICE CHARACTERISTICS



DIE SIZE 0.124 × 0.132 inch, 16,368 sq. mils
(3.15 × 3.55 mm, 10.56 sq. mm)

1. AGND
2. $I_{OUT\ A}$
3. $R_{FB\ A}$
4. $V_{REF\ A}$
5. DGND
6. DB11(MSB)
7. DB10
8. DB9
9. DB8
10. DB7
11. DB6
12. DB5
13. DB4
14. DB3
15. DB2
16. DB1
17. DB0(LSB)
18. $\overline{\text{DAC A/DAC B}}$
19. $\overline{\text{LDAC}}$
20. $\overline{\text{WR}}$
21. V_{DD}
22. $V_{REF\ B}$
23. $R_{FB\ B}$
24. $I_{OUT\ B}$

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF\ A} = V_{REF\ B}$ = +10V, $V_{OUT\ A} = V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = 25°C.

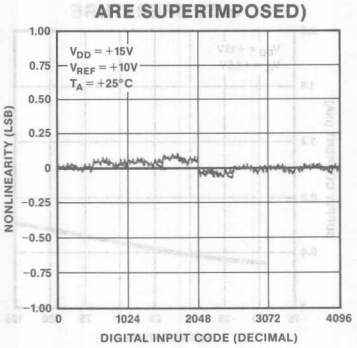
			DAC-8222G	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB MAX
Full Scale Gain Error (Note 1)	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage ($I_{OUT\ A}$, $I_{OUT\ B}$)	I_{LKG}	Digital Inputs = 0000 0000 0000 Pad 2 and 24	±50	nA MAX
Input Resistance ($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	Pad 4 and 22	8/15	kΩ MIN/ kΩ MAX
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% MAX
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}; V_{INL} or V_{INH}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV_{DD})	PSR	ΔV_{DD} = ±5%	0.002	%/% MAX

NOTES:
1. Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$.

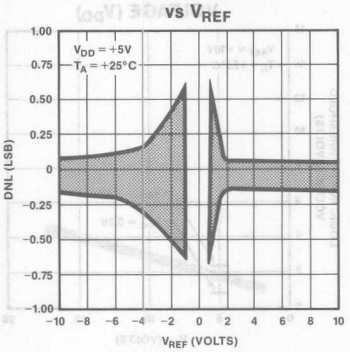
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

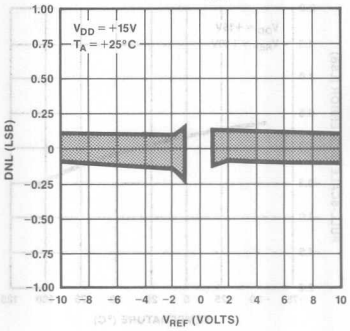
CHANNEL-TO-CHANNEL MATCHING (DAC A & B ARE SUPERIMPOSED)



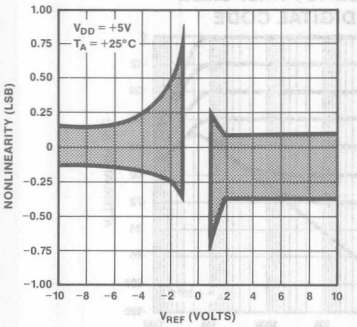
DIFFERENTIAL NONLINEARITY vs V_{REF}



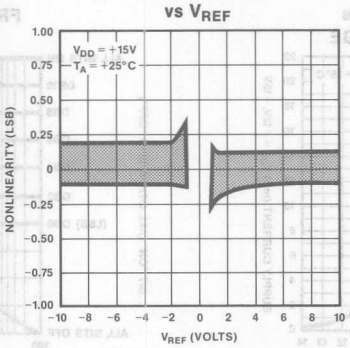
DIFFERENTIAL NONLINEARITY vs V_{REF}



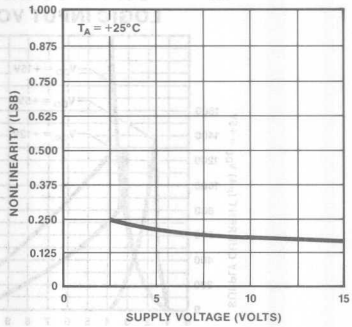
NONLINEARITY vs V_{REF}



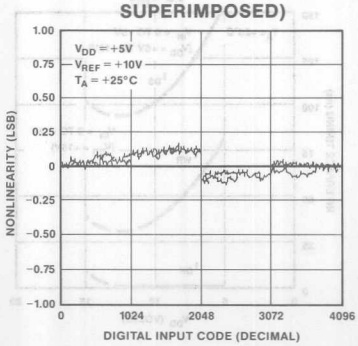
NONLINEARITY vs V_{REF}



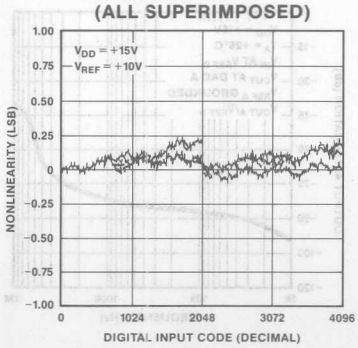
NONLINEARITY vs V_{DD}



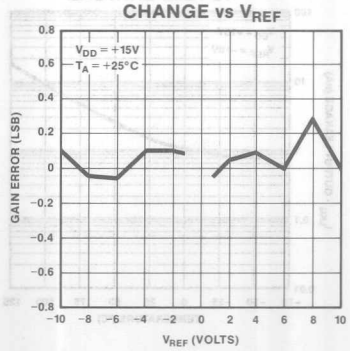
NONLINEARITY vs CODE (DAC A & B ARE SUPERIMPOSED)



NONLINEARITY vs CODE AT T_A = −55°C, +25°C, +125°C FOR DAC A & B (ALL SUPERIMPOSED)

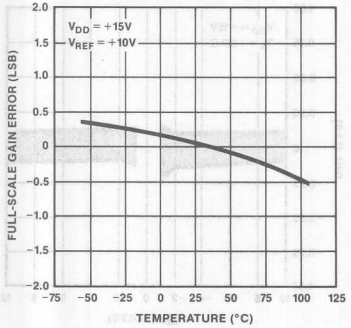


ABSOLUTE GAIN ERROR CHANGE vs V_{REF}

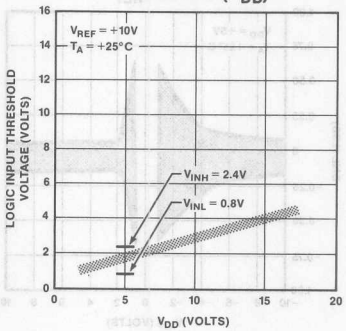


TYPICAL PERFORMANCE CHARACTERISTICS

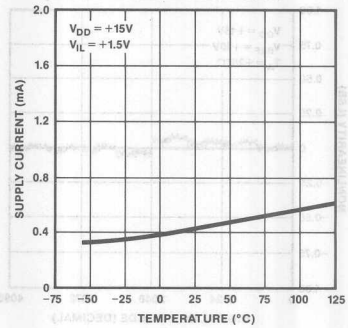
FULL-SCALE GAIN ERROR vs TEMPERATURE



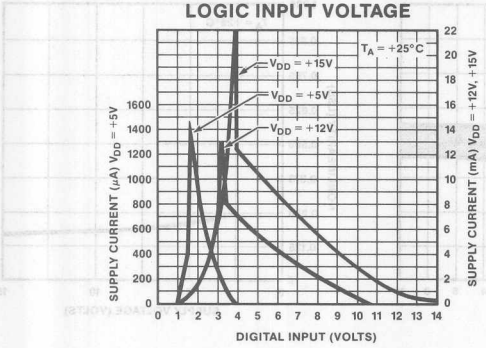
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



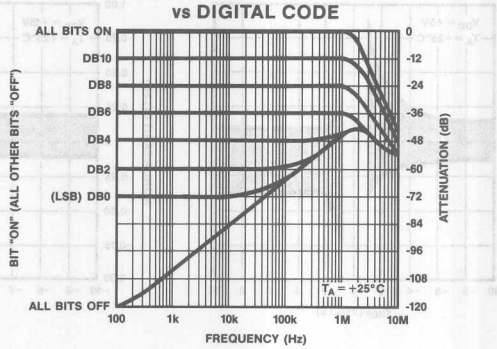
SUPPLY CURRENT vs TEMPERATURE



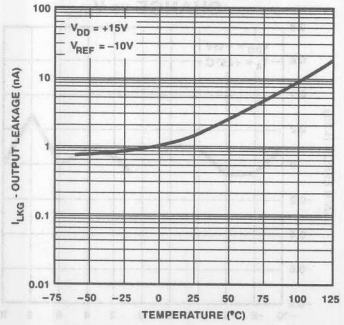
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



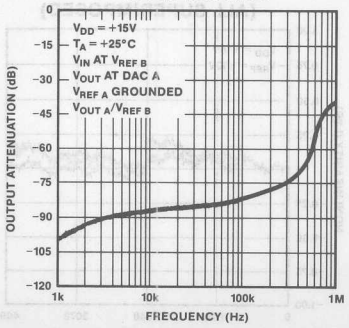
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



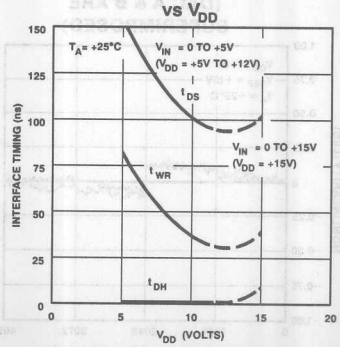
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



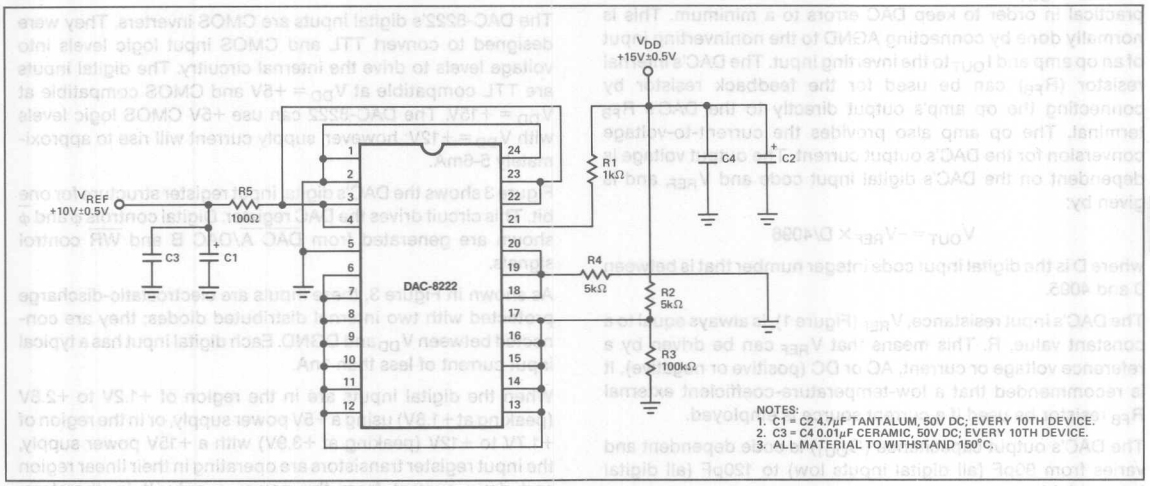
ANALOG CROSSTALK vs FREQUENCY



INTERFACE TIMING vs V_{DD}



BURN-IN CIRCUIT



PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC-8222 contains four 12-bit registers (two input registers and two DAC registers), two highly-stable thin-film R-2R resistor ladder networks, and interface control logic circuitry. Also included are 24 single-pole, double-throw, NMOS transistor current switches.

FIGURE 1: Simplified Single DAC Circuit Configuration. (Switches Are Shown For All Digital Inputs At Zero)

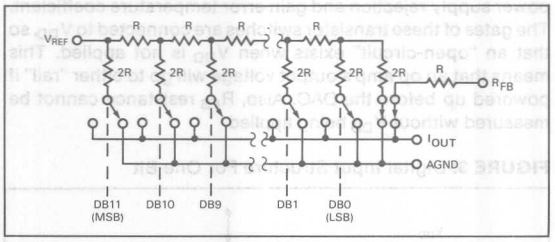


FIGURE 2: N-Channel Current Steering Switch

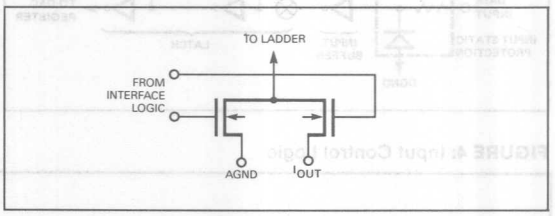


Figure 1 shows a simplified circuit for the R-2R ladder network and transistor switches for one DAC. R is typically 11kΩ. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. Figure 2 shows a single NMOS transistor switch.

The binary-weighted currents are switched between I_{OUT} and AGND by the N-channel MOS transistor switches. The selection between I_{OUT} and AGND is determined by the digital input code. It is important to note here that the voltage difference

between I_{OUT} and AGND terminals be as close to zero as practical in order to keep DAC errors to a minimum. This is normally done by connecting AGND to the noninverting input of an op amp and I_{OUT} to the inverting input. The DAC's internal resistor (R_{FB}) can be used for the feedback resistor by connecting the op amp's output directly to the DAC's R_{FB} terminal. The op amp also provides the current-to-voltage conversion for the DAC's output current. The output voltage is dependent on the DAC's digital input code and V_{REF}, and is given by:

$$V_{OUT} = -V_{REF} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

The DAC's input resistance, V_{REF} (Figure 1), is always equal to a constant value, R. This means that V_{REF} can be driven by a reference voltage or current, AC or DC (positive or negative). It is recommended that a low-temperature-coefficient external R_{FB} resistor be used if a current source is employed.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90pF (all digital inputs low) to 120pF (all digital inputs high).

Figure 1 shows a transistor switch in series with the R-2R ladder terminating resistor and R_{FB} resistor. They were designed into the DAC to binarily match the ladder leg switches and improve power supply rejection and gain error temperature coefficient. The gates of these transistor switches are connected to V_{DD}, so that an "open-circuit" exists when V_{DD} is not applied. This means that an op amp's output voltage will go to either "rail" if powered up before the DAC. Also, R_{FB} resistance cannot be measured without V_{DD} being applied.

FIGURE 3: Digital Input Structure For One Bit

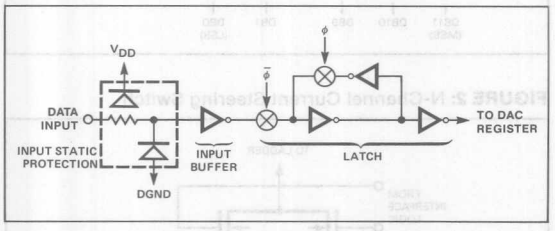
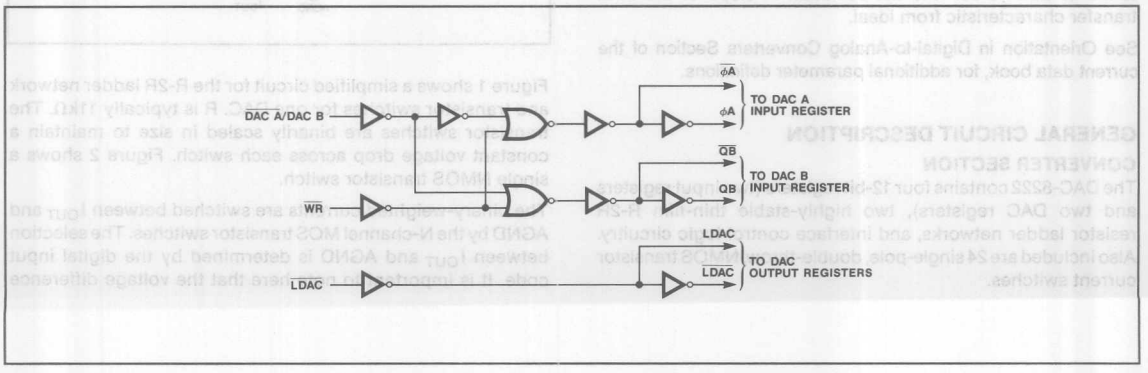


FIGURE 4: Input Control Logic



DIGITAL SECTION

The DAC-8222's digital inputs are CMOS inverters. They were designed to convert TTL and CMOS input logic levels into voltage levels to drive the internal circuitry. The digital inputs are TTL compatible at $V_{DD} = +5V$ and CMOS compatible at $V_{DD} = +15V$. The DAC-8222 can use +5V CMOS logic levels with $V_{DD} = +12V$; however, supply current will rise to approximately 5-6mA.

Figure 3 shows the DAC's digital input register structure for one bit. This circuit drives the DAC register. Digital controls ϕ and $\overline{\phi}$ shown are generated from DAC A/DAC B and WR control signals.

As shown in Figure 3, these inputs are electrostatic-discharge protected with two internal distributed diodes; they are connected between V_{DD} and DGND. Each digital input has a typical input current of less than 1nA.

When the digital inputs are in the region of +1.2V to +2.8V (peaking at +1.8V) using a +5V power supply, or in the region of +1.7V to +12V (peaking at +3.9V) with a +15V power supply, the input register transistors are operating in their linear region and draw current from the power supply. It is, therefore, recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible to keep supply currents at a minimum. The DAC-8222 may be operated with any supply voltage between the range of +5V to +15V.

INTERFACE CONTROL LOGIC

The DAC-8222's input control logic circuitry is shown in Figure 4. Note how the WR signal is used in conjunction with DAC A/DAC B to load data into either input register. LDAC loads data from the input registers to the DAC register; the DAC's analog output voltage is determined by the data contained in each DAC register.

The truth table for the DAC registers is shown in the Mode Selection Table. Note how the input register is transparent when WR is low and LDAC is high, and that the DAC register is transparent when WR is high and LDAC is low (LDAC updates the DAC's analog output voltage). The DAC is transparent from input to output when WR and LDAC are both low, and the DAC is latched (input and output is not being updated) when WR and LDAC are both high.

MODE SELECTION TABLE

DIGITAL INPUTS			REGISTER STATUS			
			DAC A		DAC B	
DAC A/$\overline{B}$	$\overline{WR}$	$\overline{LDAC}$	INPUT REGISTER	DAC REGISTER	INPUT REGISTER	DAC REGISTER
L	L	L	WRITE	WRITE	LATCHED	WRITE
H	L	L	LATCHED	WRITE	WRITE	WRITE
L	L	H	WRITE	LATCHED	LATCHED	LATCHED
H	L	H	LATCHED	LATCHED	WRITE	LATCHED
X	H	L	LATCHED	WRITE	LATCHED	WRITE
X	H	H	LATCHED	LATCHED	LATCHED	LATCHED

L = Low H = High X = Don't Care

INTERFACE CONTROL LOGIC

DAC A/DAC B (Pin 18)–DAC Selection. Active low for DAC A and active high for DAC B.

$\overline{WR}$ (Pin 20)–WRITE. Active Low. Used to write data into either DAC A or DAC B input registers, or active high latches data into the input registers.

$\overline{LDAC}$(Pin 19)–LOAD DAC. Active Low. Used to simultaneously transfer data from DAC A and DAC B input registers to both DAC outputs. The DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{WR}$ and $\overline{LDAC}$ are low. Data is latched into the output registers on the rising edge of $\overline{LDAC}$.

WRITE TIMING CYCLES

Two timing diagrams are shown and are at the user's discretion which to use.

The TWO CYCLE UPDATE, as the name implies, allows both DAC registers to be loaded and the outputs updated in two cycles. Data is first loaded into one DAC's input register on the first write cycle, and then new data loaded into the other DAC's input register while simultaneously updating both DAC outputs on the second cycle.

The THREE CYCLE UPDATE allows DAC A and DAC B registers to be loaded and analog output to be updated at a later time. The first two cycles load both DACs as above, and the third cycle updates the outputs.

The $\overline{LDAC}$ and $\overline{DAC\ A}$/DAC B control pins can be tied together and controlled with a single strobe. When using the DAC in this configuration, DAC B must be loaded first.

WRITE CYCLE TIMING DIAGRAM

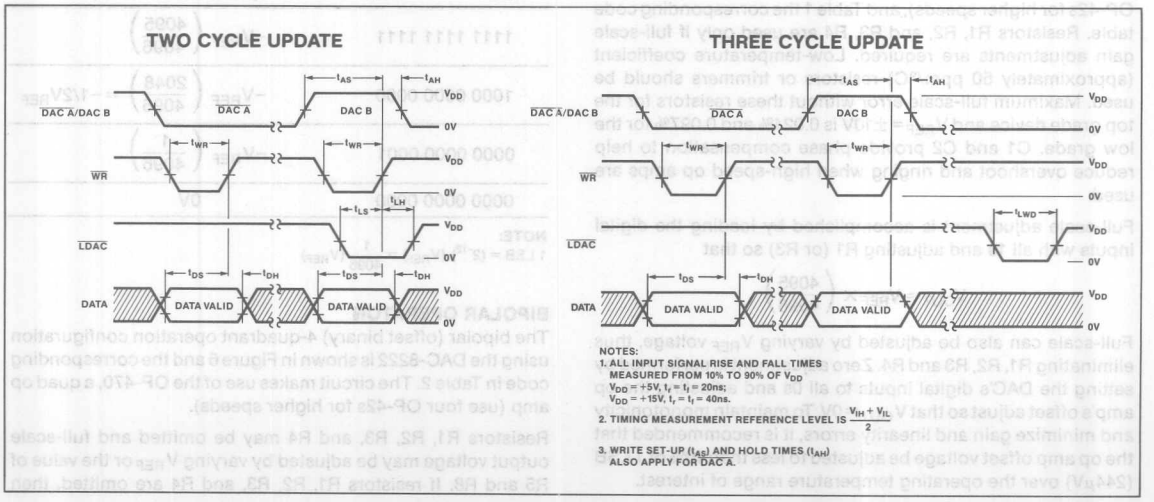
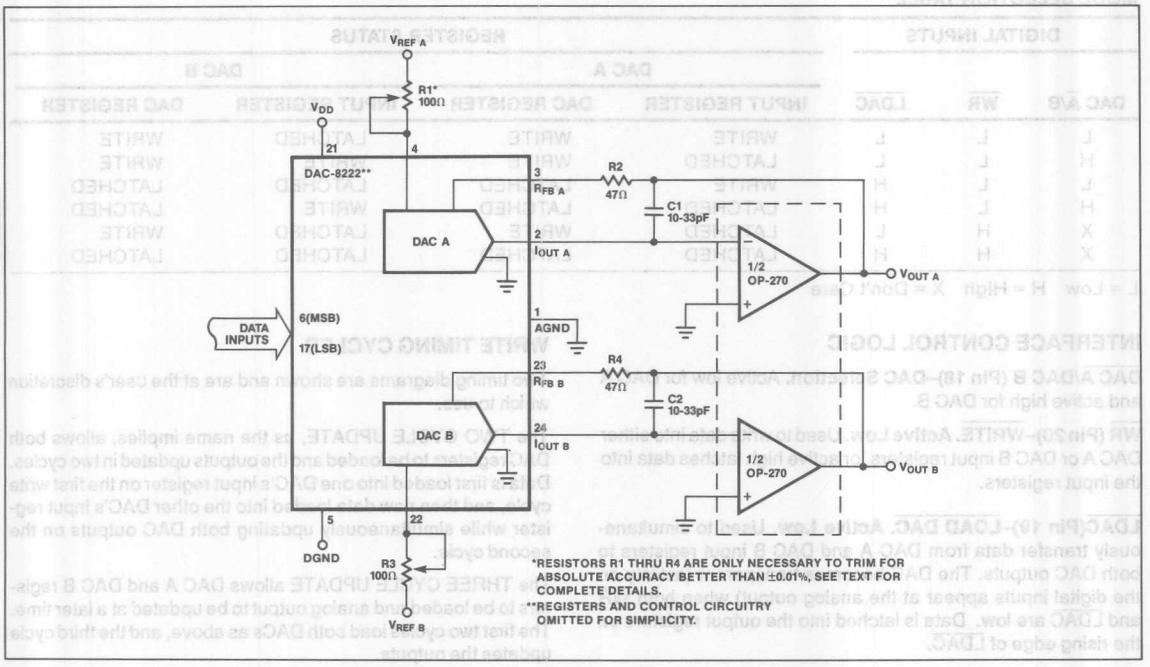


FIGURE 5: Unipolar Configuration (2-Quadrant Multiplication)



APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 5 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8222 and OP-270 dual op amp (use two OP-42s for higher speeds), and Table 1 the corresponding code table. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Low-temperature coefficient (approximately 50 ppm/°C) resistors or trimmers should be used. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = \pm 10V$ is 0.024% and 0.097% for the low grade. C1 and C2 provide phase compensation to help reduce overshoot and ringing when high-speed op amps are used.

Full-scale adjustment is accomplished by loading the digital inputs with all 1s and adjusting R1 (or R3) so that

$$V_{OUT} = V_{REF} \times \left(\frac{4095}{4096}\right)$$

Full-scale can also be adjusted by varying V_{REF} voltage, thus eliminating R1, R2, R3 and R4. Zero adjustment is performed by setting the DAC's digital inputs to all 0s and adjusting the op amp's offset adjust so that $V_{OUT} = 0V$. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244μV) over the operating temperature range of interest.

TABLE 1: Unipolar Binary Code Table (Refer to Figure 5)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE:
1 LSB = (2^{-12}) $(V_{REF}) = \frac{1}{4096}(V_{REF})$

BIPOLAR OPERATON

The bipolar (offset binary) 4-quadrant operation configuration using the DAC-8222 is shown in Figure 6 and the corresponding code in Table 2. The circuit makes use of the OP-470, a quad op amp (use four OP-42s for higher speeds).

Resistors R1, R2, R3, and R4 may be omitted and full-scale output voltage may be adjusted by varying V_{REF} or the value of R5 and R8. If resistors R1, R2, R3, and R4 are omitted, then

FIGURE 6: Bipolar Configuration (4-Quadrant Multiplication)

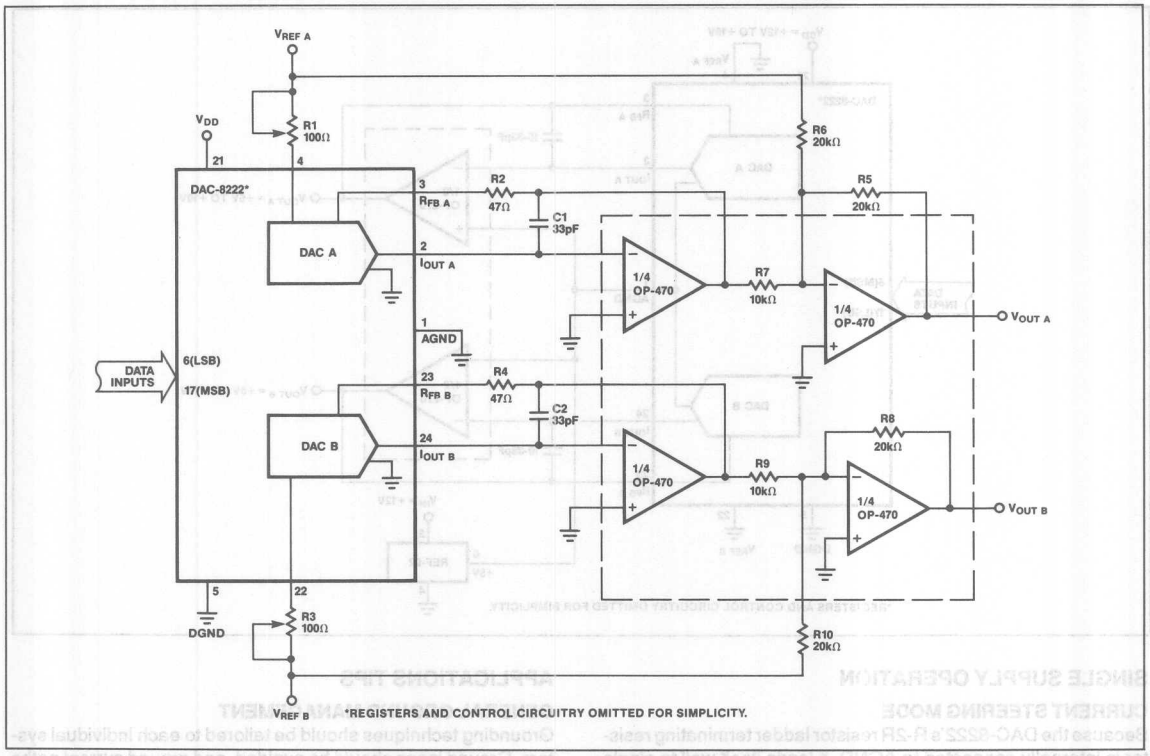


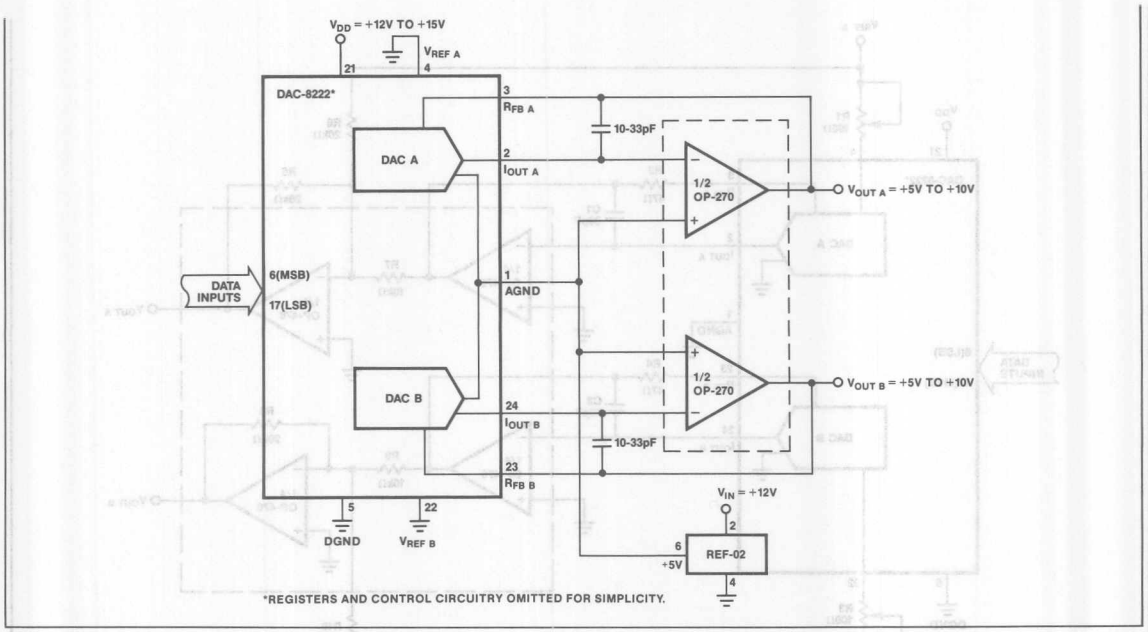
TABLE 2: Bipolar (Offset Binary) Code Table
(Refer to Figure 6)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTE:
1 LSB = (2^{-11}) (V_{REF}) = $\frac{1}{2048}$ (V_{REF})

resistors R5, R6, R7, should be ratio-matched to 0.01% so that gain error meets data sheet specifications. (Corresponding resistors, R8, R9, and R10 for DAC B should also be matched to 0.01%). The resistors should have identical temperature coefficients if operating over the full temperature range.

Zero and full-scale are adjusted one of two ways and are at the users discretion. Zero-output can be adjusted by first setting the digital inputs to 1000 0000 0000 and adjusting R1 (R3 for DAC B) so that $V_{OUT\,A}$ (or $V_{OUT\,B}$) equals 0V. If R1, R2 (R3, R4 for DAC B) are omitted, then V_{OUT} = 0V can be adjusted by varying R6, R7 (R9, R10 for DAC B) ratios. Full-scale is adjusted by setting the digital inputs to 1111 1111 1111 and varying R5 (R8 for DAC B). Full-scale can also be adjusted by varying V_{REF}. Full-scale output is equal to V_{REF} minus one LSB.



SINGLE SUPPLY OPERATION

CURRENT STEERING MODE

Because the DAC-8222's R-2R resistor ladder terminating resistor is internally connected to AGND, it lends itself well to single supply operation in the current steering mode. This means that AGND can be raised above system ground as shown in Figure 7. The output voltage range will be from +5V to +10V depending on the digital input code and is given by:

$V_{OUT} = V_{OS} + (n/4096)\ (V_{OS})$

where V_{OS} = Offset Reference Voltage (+5V in Figure 7)
n = Decimal Equivalent of the Digital Input Word

VOLTAGE SWITCHING MODE

Figure 8 shows the DAC-8222 in a single supply voltage switching mode of operation. In this configuration, the DAC's R-2R ladder acts as a voltage divider. The output voltage at the V_{REF} pin exhibits a constant impedance R (typically 11kΩ) and must be buffered by an op amp. R_{FB} pins are not used in this circuit configuration. The reference input voltage must be maintained within +1.25V of AGND and V_{DD} from +12V to +15V to preserve device accuracy.

The output voltage expression is given by:

$V_{OUT} = V_{REF}\ (n/4096)$

where n = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have a low impedance.

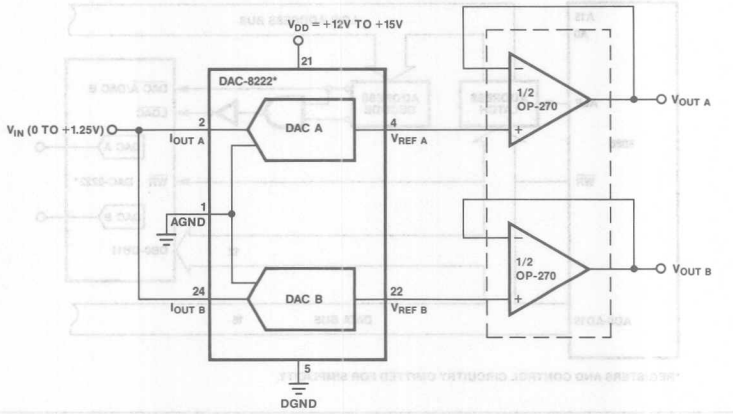
The DAC-8222's AGND and DGND pins should be tied together at the device socket to prevent digital transients from appearing at the analog output. This common point then becomes the single ground point connection. AGND and DGND should then be brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

A PC board ground plane can be used for the single point ground connection should the connections not be practical at the device socket. If neither of these connections is practical or allowed, then the device should be placed as close as possible to the system's single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

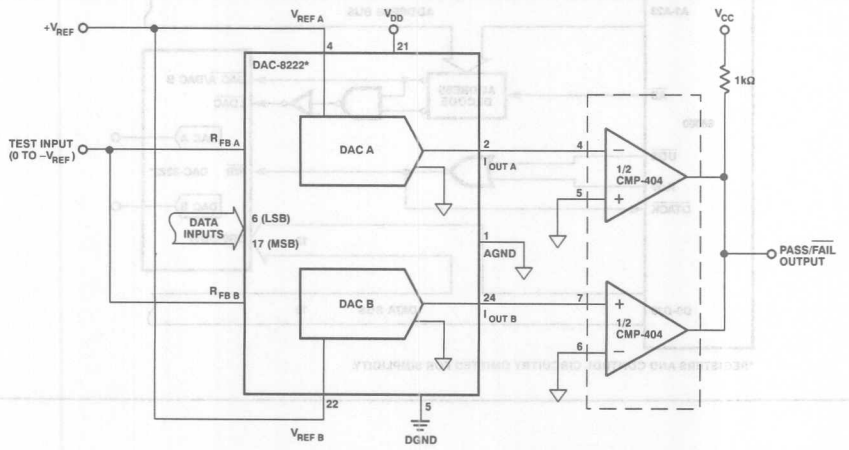
Power supplies used with the DAC-8222 should be well filtered and regulated. Local supply decoupling consisting of a 1 to 10μF tantalum capacitor in parallel with a 0.1μF ceramic is highly recommended. The capacitors should be connected between the V_{DD} and DGND pins and at the device socket.

FIGURE 8: Single Supply Operation (Voltage Switching Mode)



*REGISTERS AND DIGITAL CIRCUITRY OMITTED FOR SIMPLICITY.

FIGURE 9: Digitally-Programmable Window Detector (Upper/Lower Limit Detector)



*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

BASIC APPLICATIONS

PROGRAMMING WINDOW DETECTOR

Figure 9 shows the DAC-8222 used in a programmable window detector configuration. The required upper and lower limits for the test are loaded into DAC A and DAC B. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero.

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8222's versatile loading structure greatly simplifies interfacing to 16-bit bus systems; it also reduces the number of "glue" logic components. Data loading into its 12-bit wide data input is achieved by use of only two control signals, $\overline{WR}$ and $\overline{LDAC}$. DAC selection is controlled with a single DAC A/$\overline{DAC}$ B line.

Figures 10 and 11 show how easily the DAC-8222 interfaces with the 8086 and 68000 16-bit microprocessors.

FIGURE 10: DAC-8222 To 8086 Interface

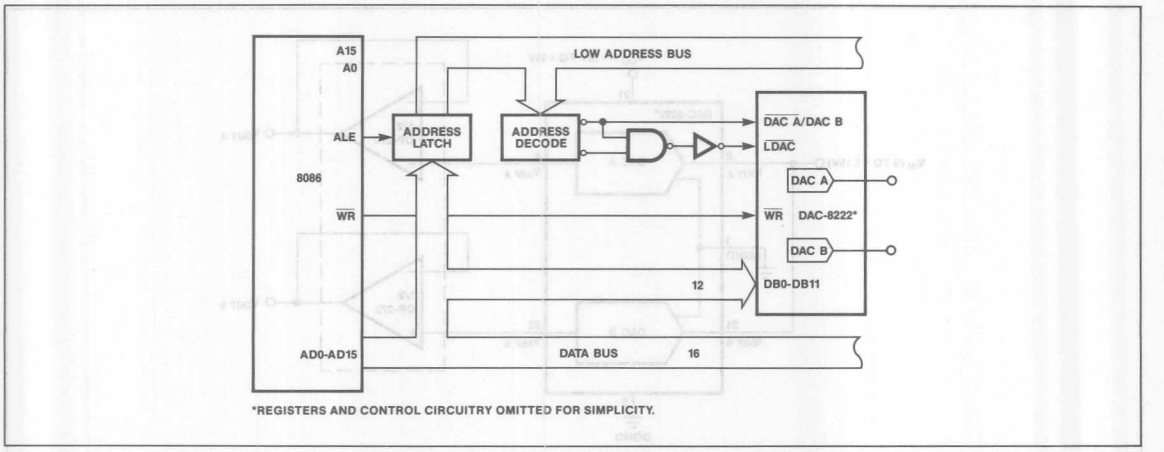
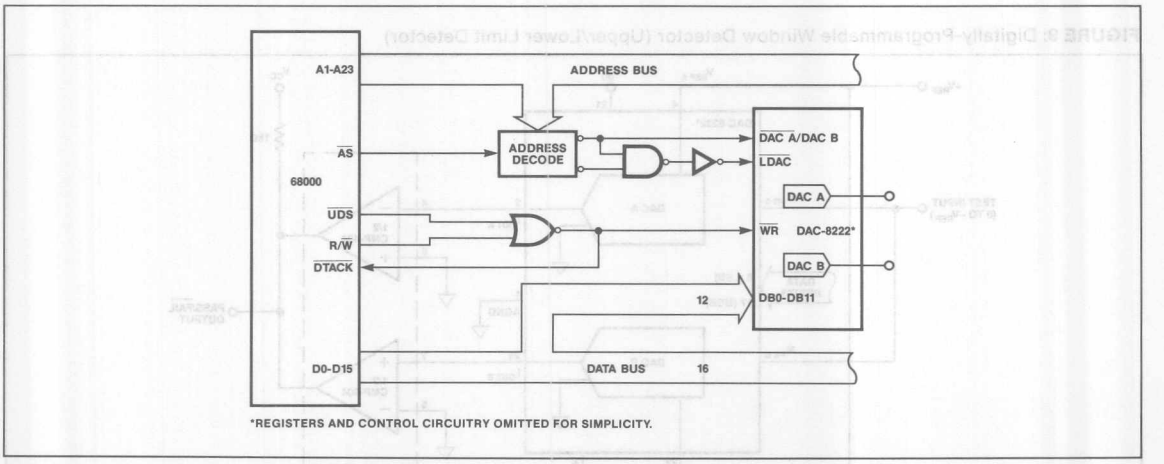


FIGURE 11: DAC-8222 To 68000 Interface



Dual 8-Bit CMOS D/A Converter with Voltage Output

DAC-8228

FEATURES

- Two 8-Bit Voltage Out DACs in a Single Chip
- Fits 7528/7628 Sockets
- Adjustment Free Internal CMOS Op Amps
- Single +12V to +15V Operation
- TTL Compatible Over Full V_{DD} Range
- Fast Interface Timing ..... T_{WR} = 50ns
- Improved Resistance to ESD
- Available in Small Outline Package
- CerDIP and Epoxy Packages Come in the Extended Industrial Temperature Range of –40°C to +85°C
- Available in Die Form

APPLICATIONS

- Disk Drive Systems
- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Multi-Channel Microprocessor-Controlled Systems
- Servo Control Systems

ORDERING INFORMATION †

		PACKAGE: 20-PIN DIP/SOL
RELATIVE ACCURACY	GAIN ERROR	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	±2 LSB	DAC8228FR
±1/2 LSB	±2 LSB	DAC8228FP
±1/2 LSB	±2 LSB	DAC8228FS

† All commercial and industrial temperature range parts are available with burn-in.

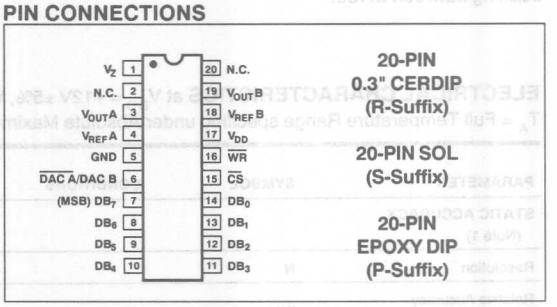
GENERAL DESCRIPTION

The DAC-8228 is a dual 8-bit, voltage output, CMOS, D/A converter in a single chip. It was designed to drop into AD7528/7628 sockets eliminating two external op amps in applications such as hard disk drives. These applications generally operate the AD7528/7628 with zero volts applied to V_{REF} and offset AGND to +2.5 or +5 volts. The DAC-8228 is tested under both these conditions.

The DAC-8228 can also be used in those applications requiring a unipolar output voltage. It can deliver an output voltage between 0V and +10V with V_{DD} = +14V (maximum output voltage is V_{DD} –4V). The DAC-8228's reference input can accept a negative voltage from 0V to –10V (the DAC's internal unity-gain inverting amplifier inverts the input signal). Choose the DAC-8229 for bipolar operation.

Continued

PIN CONNECTIONS

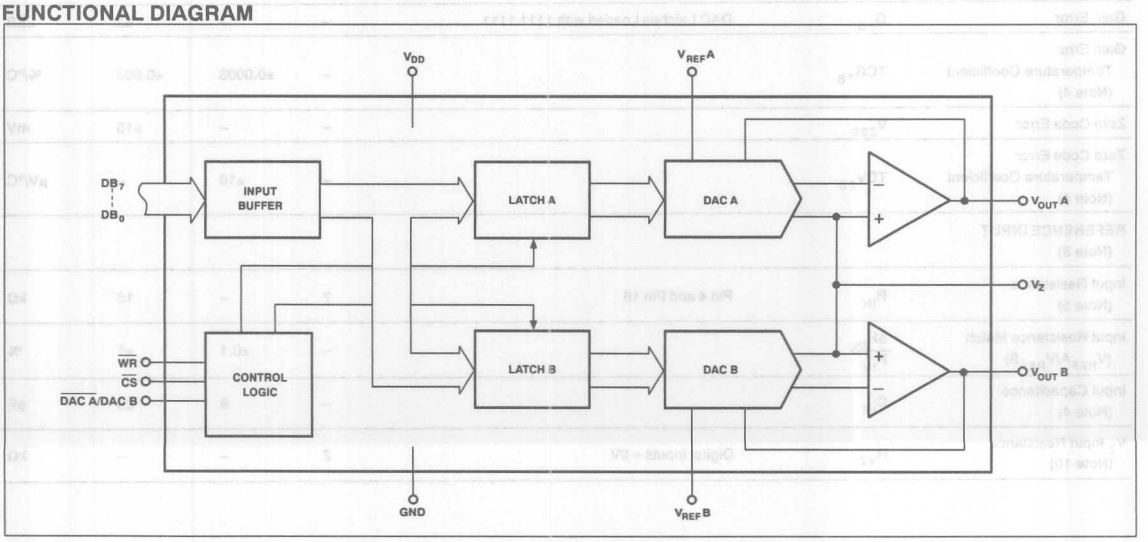


20-PIN 0.3" CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

FUNCTIONAL DIAGRAM



The DAC-8228 offers CerDIP and plastic packaged devices in the extended industrial temperature range of –40°C to +85°C. Applications requiring the military temperature range should use the DAC-8229. To make the DAC-8229 pin and functionally compatible with the DAC-8228, AGND A and AGND B should be tied together to function as V_Z, and V_{SS} connected to GND.

The DAC-8228 consists of two CMOS voltage output amplifiers, two high-accuracy R-2R resistor ladder networks, interface control logic, and two 8-bit registers. An internal regulator maintains TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range.

The DAC-8228 dissipates only 90mW in the space saving 20-pin 0.3" DIP or the 20-lead SO surface mount package. Its compact size, low power, and economical cost per channel, makes it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

Using PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with its highly-stable thin-film resistor ladder, allows the DAC-8228 to offer superior matching and temperature tracking between DACs.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to V_Z or GND ..... –0.3V, +17V
V_Z to GND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
$V_{REF\ A}$, $V_{REF\ B}$ to GND ..... –17V, V_Z
$V_{OUT\ A}$, $V_{OUT\ B}$ to V_Z (Note 1) ..... –0.3V, V_{DD}
Operating Temperature Range
FR/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to GND is 50mA.
2. Use proper anti-static handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4)	TCG_{FS}		–	±0.0003	±0.002	%/°C
Zero Code Error	V_{ZSE}		–	–	±15	mV
Zero Code Error Temperature Coefficient (Note 4)	TCV_{ZS}		–	±10	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}	Pin 4 and Pin 18	7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF
V_Z Input Resistance (Note 10)	R_{VZ}	Digital Inputs = 0V	2	–	–	kΩ

T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. Continued

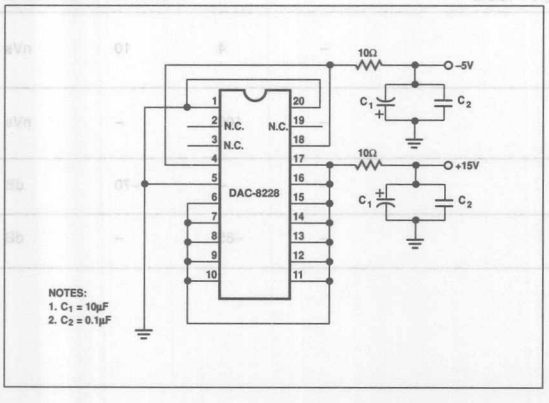
PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Supply Current (Note 6)	I_{DD}		–	–	7	mA
Power Dissipation	P_D	V_{DD} = +12V 12 x 7mA	–	–	84	mW
		V_{DD} = +15V 15 x 7mA	–	–	105	
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = +25°C Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Note 4, 7)	t_s	Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	T_A = +25°C $V_{REF}B$ to $V_{OUT}A$ or $V_{REF}A$ to $V_{OUT}B$ $V_{REF}B = V_{REF}A = 20V_{p-p}$ @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
Digital Charge Injection	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	100	–	nVs
AC Feedthrough (Notes 4, 11)	FT		–	–	–70	dB
Harmonic Distortion	THD	T_A = +25°C $V_{IN} = 6V_{RMS}$ @ f = 1kHz	–	–85	–	dB

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

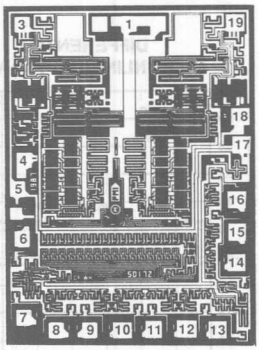
PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–	–	ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and not subject to production test.
5. Input resistance temperature coefficient = +300ppm/°C.
6. $V_{IN} = V_{INL}$ or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is 0V to –10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. Resistance looking into the V_Z terminal.
11. $V_{REF}A$, $V_{REF}B$ = 20V_{p-p} Sinewave @ f = 10kHz; $V_{REF}A$ to $V_{OUT}A$ or $V_{REF}B$ to $V_{OUT}B$, both DAC latches loaded with 0000 0000.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.082x 0.111 inch, 9,102 sq. mils
(2.08 x 2.82 mm, 5.87 sq. mm)

1. AMPLIFIER REFERENCE (V_Z)
2. N.C.
3. VOLTAGE OUTPUT ($V_{OUT}A$)
4. DAC A REFERENCE INPUT ($V_{REF}A$)
5. GROUND (GND)
6. DAC SELECTION ($\overline{DAC}$ A/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. VOLTAGE OUTPUT ($V_{OUT}B$)
20. N.C.

Substrate (die backside) is internally connected to V_{DD}.

2

WAFER TEST LIMITS at $V_{DD} = V_{DD} = +12V \pm 5\%$, $V_{REF} = 0V$, $V_Z = 2.5V$ or $V_{DD} = +15V \pm 5\%$, $V_{REF} = 0V$, $V_Z = +5V$, $T_A = +25°C$.

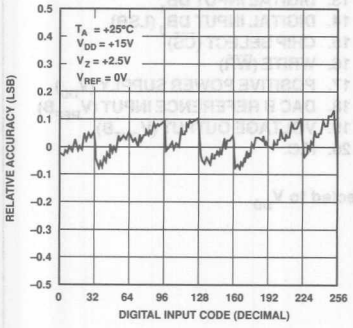
PARAMETER	SYMBOL	CONDITIONS	DAC-8228GBC LIMITS	UNITS
Relative Accuracy (Note 3)	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity (Notes 1, 3)	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Zero Code Error	V_{ZSE}		±15	mV MAX
Input Resistance	R_{IN}	Pad 4 and 18	7/15	kΩ MIN/kΩ MAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\frac{\Delta R_{IN}}{R_{IN}}$		1	% MAX
V_Z Input Resistance (Note 3)	R_{VZ}	Digital Inputs = 0V	2	kΩ MIN
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	±1	µA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	$V_{DD} = \pm 5\%$	0.01	%/% MAX
Positive Supply Current (Note 2)	I_{DD}		7	mA MAX

NOTES:
1. All dice guaranteed monotonic over the full operating temperature range.
2. $V_{IN} = V_{INL}$ or V_{INH}; output unloaded.
3. Resistance looking into the V_Z terminal.

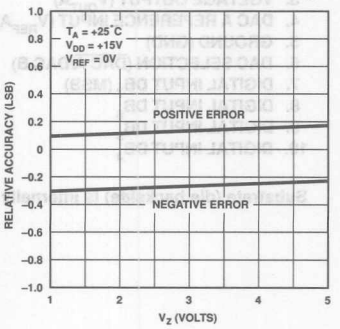
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

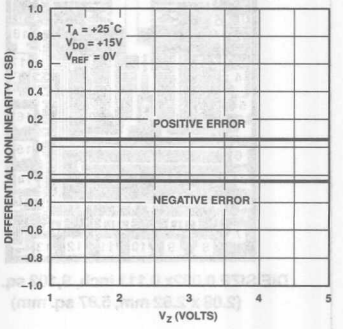
RELATIVE ACCURACY vs CODE (V_{REF}= 0V, V_Z = +2.5V)



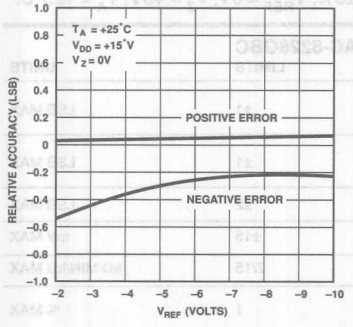
RELATIVE ACCURACY vs V_Z



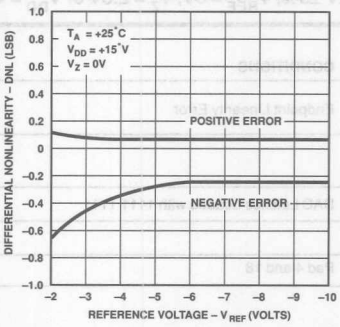
DIFFERENTIAL NONLINEARITY vs V_Z



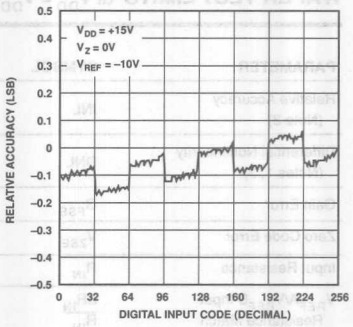
RELATIVE ACCURACY vs REFERENCE VOLTAGE



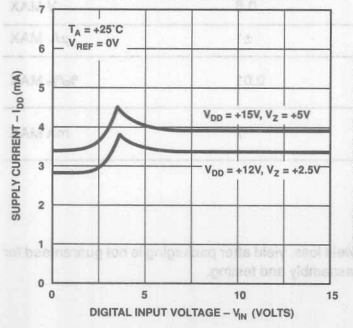
DIFFERENTIAL NONLINEARITY vs REFERENCE VOLTAGE



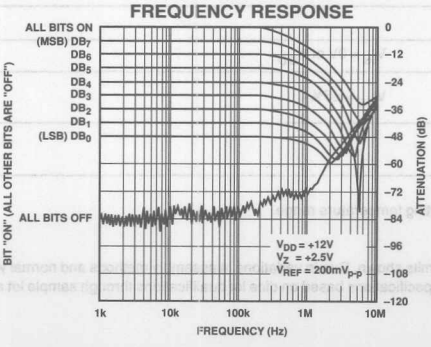
RELATIVE ACCURACY vs CODE (V_{REF}= –10V, V_Z = 0V)



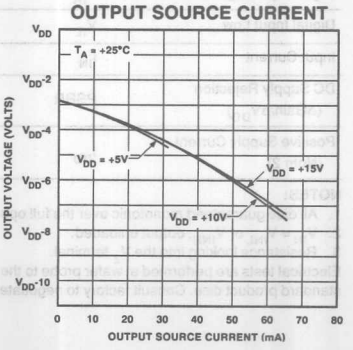
SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



MULTIPLYING MODE FREQUENCY RESPONSE

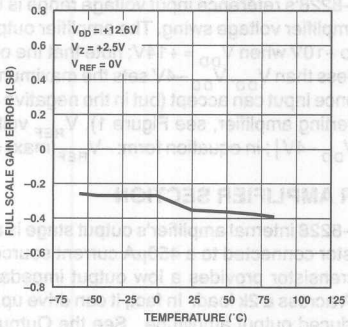


OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

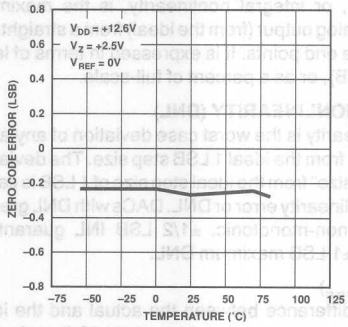


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

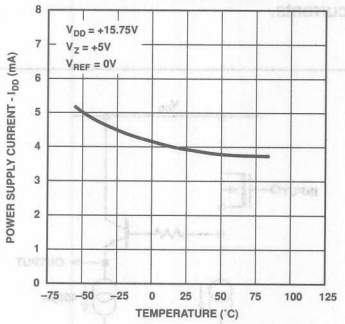
FULL SCALE GAIN ERROR vs TEMPERATURE



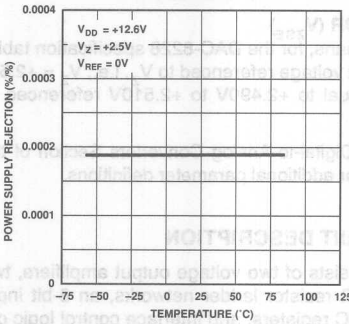
ZERO CODE ERROR vs TEMPERATURE



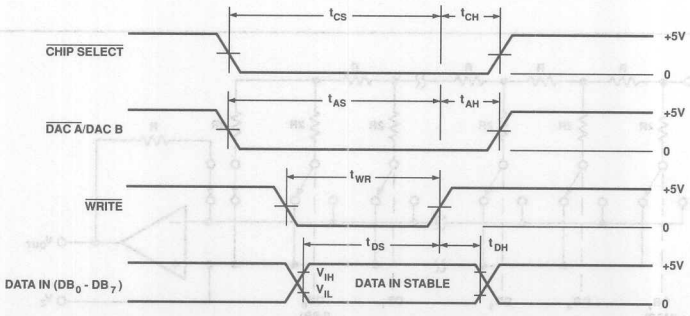
POWER SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION vs TEMPERATURE



WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bits (LSB), or as a percent of full-scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 may be non-monotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal. Zero code error is not included in this measurement.

ZERO CODE ERROR (V_{ZSE})

Zero Code Error means, for the DAC-8228 specification table, the amount of offset voltage referenced to V_Z, i.e., V_Z = +2.5V, ±10mV offset is equal to +2.490V to +2.510V referenced to ground.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

The DAC-8228 consists of two voltage output amplifiers, two high accuracy R-2R resistor ladder networks, an 8-bit input buffer, two 8-bit DAC registers, and interface control logic circuitry.

Also included are 16 single-pole, double-throw NMOS transistor switches. These switches, which are controlled by the digital

[illegible] the amplifier inverting input and V_Z, see Figure 1. This configuration inverts the reference input voltage, and also allows biasing V_Z above digital ground simplifying many applications.

REFERENCE INPUT

The DAC-8228's reference input voltage range is limited by the internal amplifier voltage swing. The amplifier output can swing from 0V to +10V when V_{DD} = +14V; note that the output voltage is 4 volts less than V_{DD}. V_{DD} –4V sets the maximum voltage that the reference input can accept (but in the negative direction due to the inverting amplifier, see Figure 1). V_{REF} voltage range is 0V to $-|V_{DD}-4V|$; in equation form: $-V_{REF}(max) = |V_{DD}-4V|$.

BUFFER AMPLIFIER SECTION

The DAC-8228 internal amplifier's output stage is an NPN bipolar transistor connected to a 450µA current source, see Figure 2. This transistor provides a low output impedance that can drive 5mA across a 2k load. In fact, it can drive up to 65mA, but with a reduced output amplitude. See the Output Voltage vs. Output Source Current graph under the typical electrical characteristics curves. The user must use caution that the package power dissipation is not exceeded when driving low impedances and high currents.

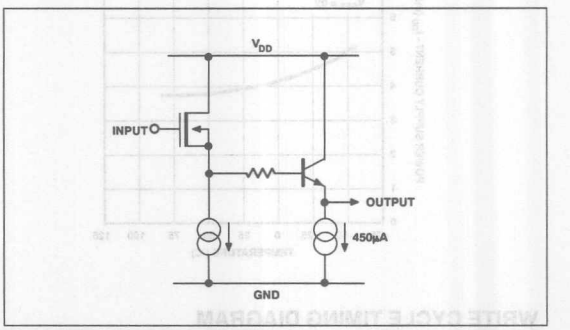


FIGURE 2: *Amplifier Output Stage*

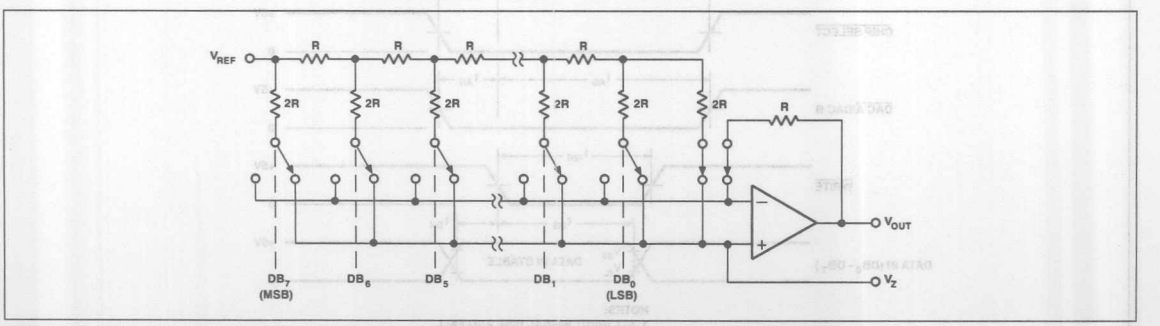


FIGURE 1: *Simplified single DAC configuration (switches shown for all digital inputs at logic "0").*

Figure 3 depicts a typical output current-sink versus voltage graph for the amplifier's output stage. It shows the output coming out of its saturation region and starting to appear resistive as the output approaches zero volts.

The amplifier's internal gain stages were designed to maintain sufficient gain over its common mode range. This results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during manufacturing. This eliminates user offset trimming.

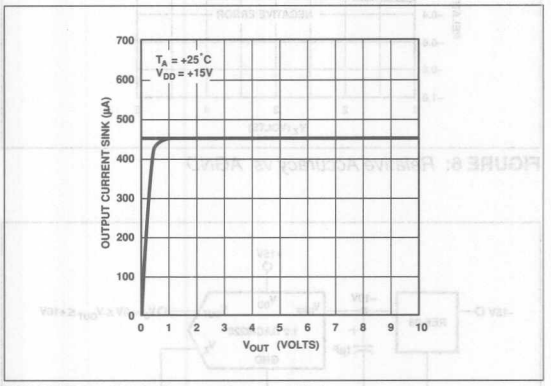


FIGURE 3: *DAC Output Current Sink*

DIGITAL SECTION

Figure 4 shows one digital input structure of the DAC-8228. A built-in 5V regulator and level shifter converts TTL digital input signals into CMOS levels to drive the internal circuitry. This provides full TTL compatibility over a V_{DD} range of 5 to 15V.

As shown in Figure 4, each digital input is protected from electrostatic-discharge with two internal diodes connected between V_{DD} and GND. Each input has a typical input current of less than 1nA.

INTERFACE CONTROL INFORMATION

DAC SELECTION

DAC A and DAC B both share a common 8-bit input port. The control input, $\overline{\text{DAC A}}$/DAC B, selects which DAC can accept data from the input port. A logic low selects DAC A and a logic high selects DAC B.

DAC OPERATION

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operation of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to the codes on the digital input pins.

HOLD MODE

The selected DAC register latches the data present on the digital input pins just prior to $\overline{\text{CS}}$ and $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

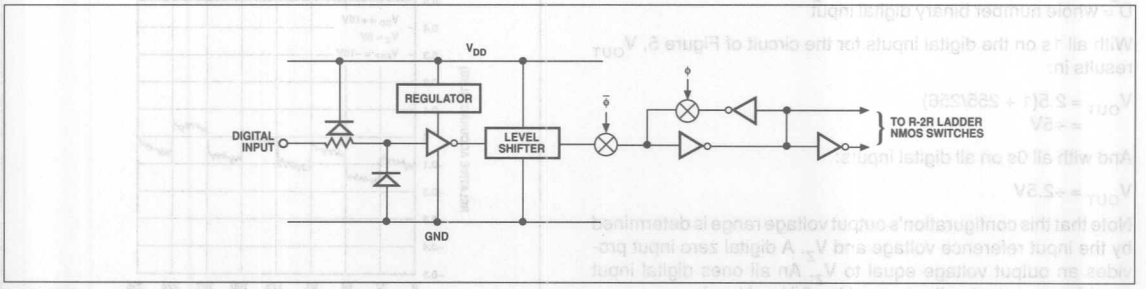


FIGURE 4: *Simplified Digital Input Structure*

APPLICATIONS INFORMATION

Figure 5 shows the DAC-8228 configured to operate with V_Z biased above ground. Note how the reference source is connected between V_Z and ground; also note how the DAC's V_{REF} pin is connected directly to ground. Not shown but equally important is that the reference voltage source at V_Z is common to both DAC A and DAC B.

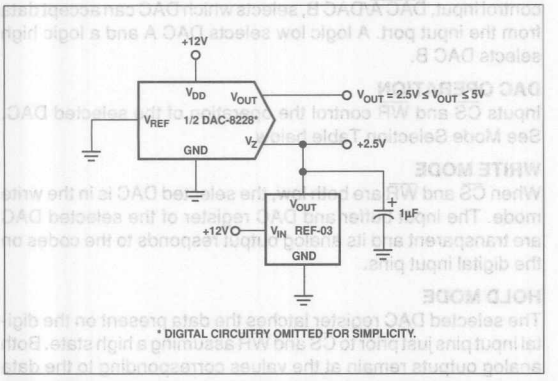


FIGURE 5: *Single Supply Configuration (+2.5V ≤ V_{OUT} ≤ +5V)*

The +2.5V reference voltage is obtained from PMI's REF-03; if greater accuracy is desired, use the REF-43. The REF-02 or REF-05, depending on accuracy required, can be used for +5V applications.

The transfer equation for the circuit of Figure 5 is:

$$V_{OUT} = V_Z (1 + D/256)$$

where
V_Z = Reference voltage applied to V_Z
D = whole number binary digital input

With all 1s on the digital inputs for the circuit of Figure 5, V_{OUT} results in:

$$V_{OUT} = 2.5(1 + 255/256)$$
$$= +5V$$

And with all 0s on all digital inputs:

$$V_{OUT} = +2.5V$$

Note that this configuration's output voltage range is determined by the input reference voltage and V_Z. A digital zero input provides an output voltage equal to V_Z. An all ones digital input provides an output voltage equal to: $2(V_Z - V_{REF})$.

Figure 6 shows a plot of Relative Accuracy versus V_Z voltage.

Figure 7 shows the DAC-8228 in another single supply configuration. In this circuit, a PMI REF-08 is used for the reference voltage source and V_Z is grounded. The output swings from 0V to +10V, see Figure 8.

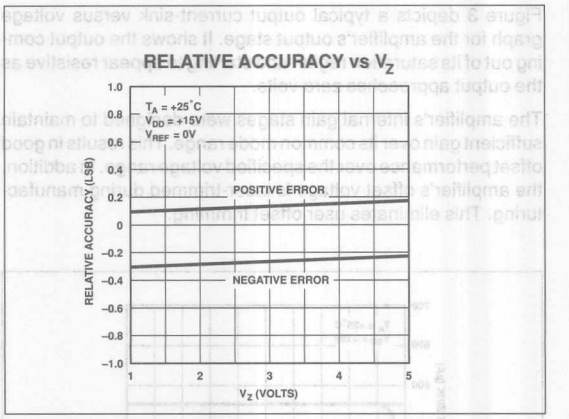


FIGURE 6: *Relative Accuracy vs. AGND*

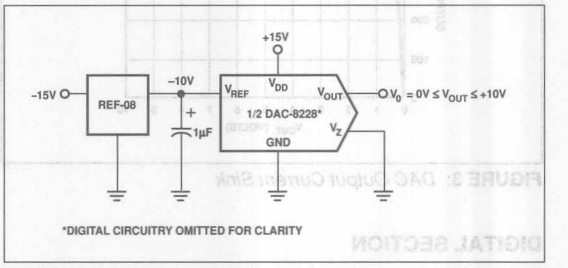


FIGURE 7: *Single Supply Configuration ($V_O \leq V_{OUT} \leq +10V$)*

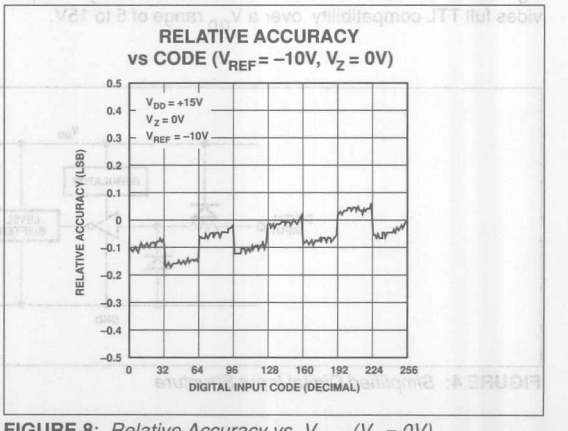


FIGURE 8: *Relative Accuracy vs. V_{REF} (V_Z = 0V)*

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8228's versatile input structure allows direct interface to 8- or 16-bit microprocessors. Its simplicity reduces the number of required glue logic components. Figures 9 and 10 show the DAC-8228 interface configurations with the 6800 and 8085 microprocessors.

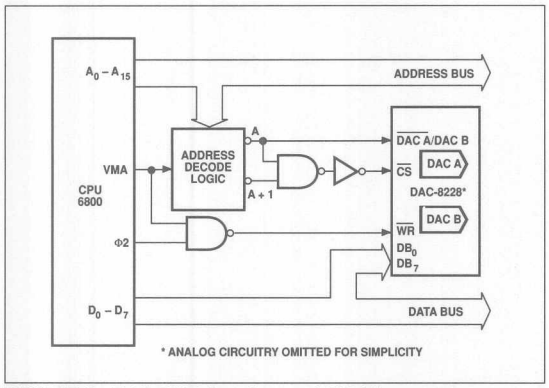


FIGURE 9: *DAC-8228 Interface to 6800 Microprocessor*

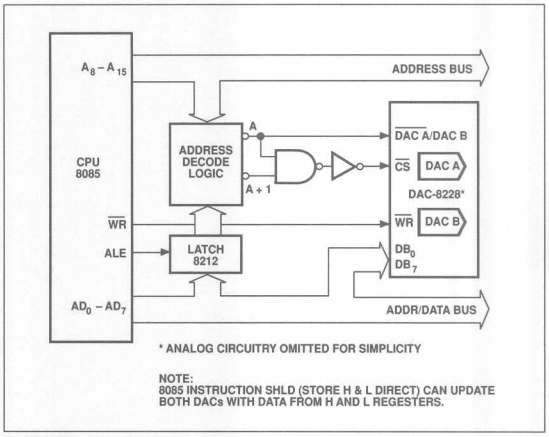


FIGURE 10: *DAC-8228 Interface to 8085 Microprocessor*

2

FEATURES

- Two 8-Bit DACs In A Single Chip
- Adjustment-Free Internal CMOS Amplifiers
- Single or Dual Supply Operation
- TTL Compatible Over Full V_{DD} Range
- 5 Microsecond Settling Time
- Fast Interface Timing ..... t_{WR} = 50ns
- Improved Resistance to ESD
- Fits AD/PM-7528 And AD/PM-7628 Sockets
- Available In Small Outline Package
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available In Die Form

APPLICATIONS

- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Disk Drive Systems
- Multi-Channel Microprocessor-Controlled Systems

GENERAL DESCRIPTION

The DAC-8229 is a dual 8-bit, voltage output, multiplying CMOS D/A converter. Its reference input accepts a ±2.5V signal, inverts and delivers it to the output with an internal amplifier. It can also accept –10V at V_{REF} with a corresponding +10V output (the maximum positive input signal that it can accept is +2.5V).

The DAC-8229 was designed to operate with dual supplies; however, it can be operated with a single supply by connecting

Continued

ORDERING INFORMATION†

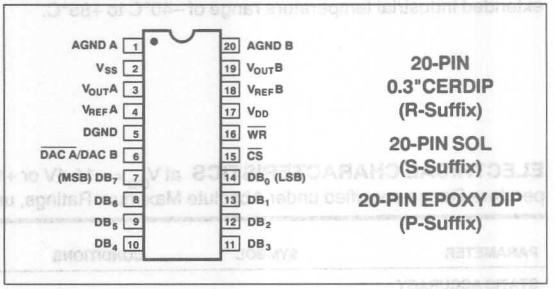
PACKAGE: 20-PIN DIP/SOL			
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED†† INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2LSB	±2LSB	DAC8229AR	DAC8229ER
±1/2LSB	±2LSB	——	DAC8229FP
±1/2LSB	±2LSB	——	DAC8229FS

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

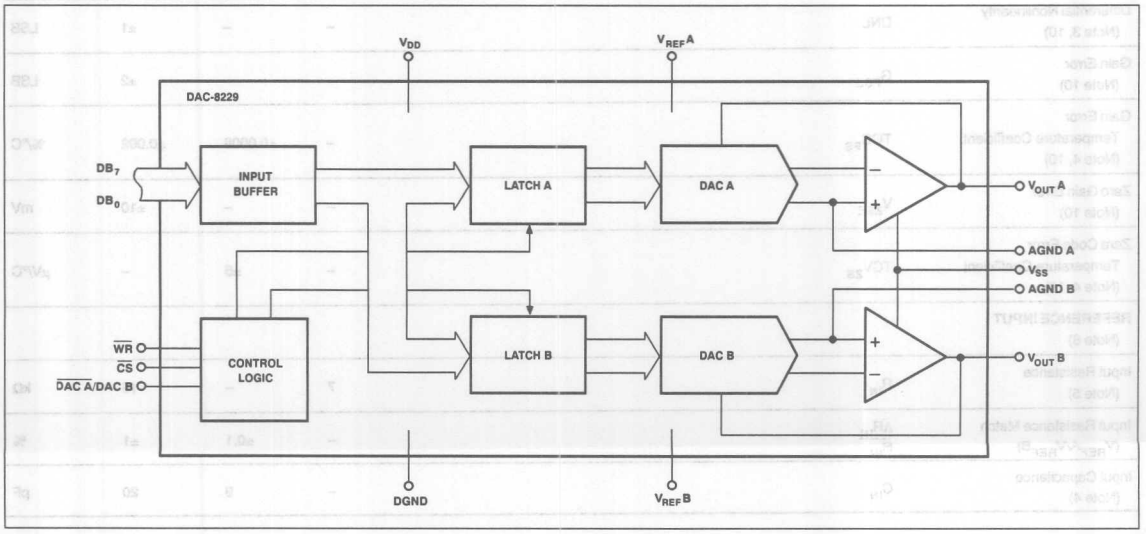
† All commercial and industrial temperature range parts are available with burn-in.

†† Cerdip and epoxy packaged devices available in the extended industrial temperature range.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION *Continued*

V_{SS}, AGND A, and AGND B to ground. Its operating characteristics will then be similar to that of the DAC-8228 (whose pin-out allows it to drop into the AD/PM-7528 and AD/PM-7628 sockets).

An internal regulator provides TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range. Also, each DAC input latch is addressable for easy microprocessor interfacing.

The DAC-8229 dissipates less than 109mW in the space-saving 20-pin 0.3" DIP or the 20-lead SO surface-mount package. Its compact size, low power, and economical cost per channel, make it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with PMI's highly-stable thin-film R-2R resistor ladder, offers superior matching and temperature tracking between DACs.

The DAC-8229 offers cerdip or epoxy packaged devices in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND or DGND ..... –0.3V, +17
VV_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
V_{REF} to AGND ..... –17V, +4V
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature Range
DAC-8229AR Version ..... –55°C to +125°C
DAC-8229ER/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. Use proper antistatic handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

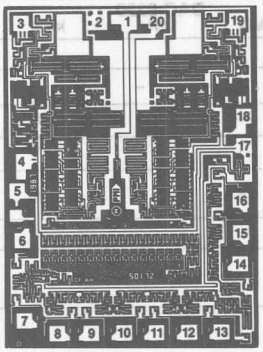
ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

			DAC-8229			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2,10)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3, 10)	DNL		–	–	±1	LSB
Gain Error (Note 10)	G_{FSE}		–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4, 10)	TCG_{FS}		–	±0.0008	±0.002	%/°C
Zero Gain Error (Note 10)	V_{ZSE}		–	–	±10	mV
Zero Code Error Temperature Coefficient (Note 4, 10)	TCV_{ZS}		–	±5	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}		7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF

ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8229 MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Positive Supply Current (Note 6)	I_{DD}		–	–	6	mA
Negative Supply Current (Note 6)	I_{SS}		–	–	5	mA
DC Power Supply Rejection Ratio (Δ Gain/ΔV_{DD}) (Note 10)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = 25°C V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Notes 4,7)	t_S	V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	$V_{REF}B$ to $V_{OUT}A$ or $V_{REF}A$ to $V_{OUT}B$ $V_{REF}B = V_{REF}A = 20V_{p-p}$ @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
AC Feedthrough (Notes 4, 11)	F_T	T_A = 25°C T_A = Full Temp. Range	– –	– –	–70 –65	dB
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–	–	ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and are not subject to production test.
5. Input resistance temperature coefficient = +300 ppm/°C.
6. $V_{IN} = V_{INL}$ or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is +3V to –10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. V_{REF} = +2.5V, $R_{PULLDOWN}$ = 20kΩ (a pulldown resistor to V_{SS} is used for these tests).
11. $V_{REF}A$, $V_{REF}B = 20V_{p-p}$ Sinewave @ f = 10kHz; $V_{REF}A$ to $V_{REF}B$ or $V_{REF}B$ to $V_{REF}A$.



DIE SIZE 0.082 x 0.111 inch, 9,102 sq. mils
(2.08 x 2.82 mm, 5.87 sq. mm)

1. ANALOG GROUND (AGND A)
2. NEGATIVE POWER SUPPLY (V_{SS})
3. VOLTAGE OUTPUT (V_{OUT} A)
4. DAC A REFERENCE INPUT (V_{REF} A)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC\ A}$/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT (V_{REF} B)
19. VOLTAGE OUTPUT (V_{OUT} B)
20. ANALOG GROUND (AGND B)

Substrate (die backside) is internally connected to V_{DD}.

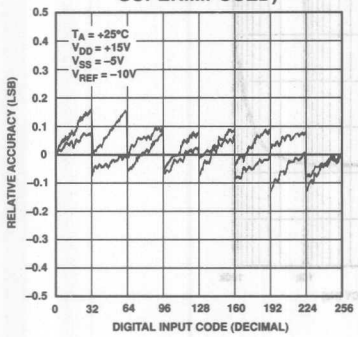
WAFER TEST LIMITS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ± 10%; V_{REF} = ±2.5V; AGND = 0V; T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8229GBC LIMIT	UNITS
Relative Accuracy (Note 3)	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity (Notes 1, 3)	DNL		±1	LSB MAX
Gain Error (Note 3)	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Zero Code Error (Note 3)	V_{ZSE}		±10	mV MAX
Input Resistance	R_{IN}	Pad 4 and 18	7/15	kΩ MIN/kΩ MAX
V_{REF}A/V_{REF}B Input Resistance Match	$\frac{\Delta R_{IN}}{R_{IN}}$		1	% MAX
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$) (Note 3)	PSRR	V_{DD} = ±5%	0.01	%/% MAX
Positive Supply Current (Note 2)	I_{DD}		6	mA MAX
Negative Supply Current (Note 2)	I_{SS}		5	mA MAX

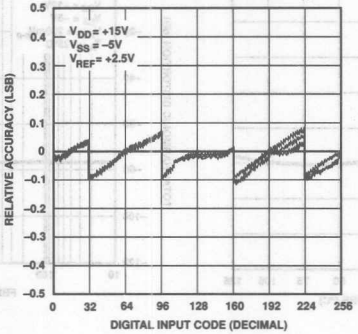
NOTES:
1. All dice guaranteed monotonic over the full operating temperature range.
2. $V_{IN} = V_{INL}$ or V_{INH}; output unloaded.
3. V_{REF} = +2.5V, $R_{PULLDOWN}$ = 20kΩ (a pulldown resistor to V_{SS} is used for these tests).

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

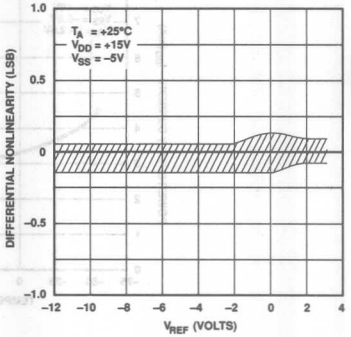
DAC A-TO-DAC B MATCHING (DACs A & B ARE SUPERIMPOSED)



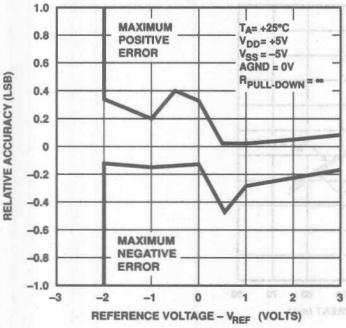
RELATIVE ACCURACY (DAC A) vs CODE AT T_A = –55°C, +25°C, +125°C (SUPERIMPOSED)



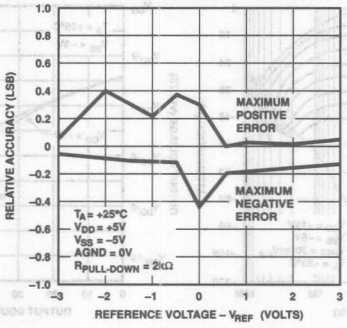
DIFFERENTIAL NONLINEARITY vs V_{REF}



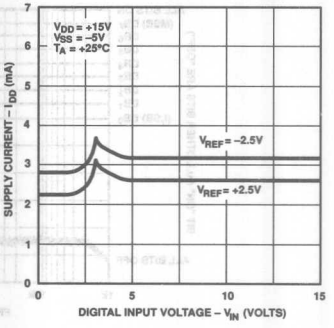
RELATIVE ACCURACY vs REFERENCE VOLTAGE



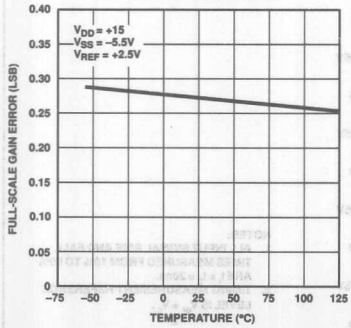
RELATIVE ACCURACY vs REFERENCE VOLTAGE



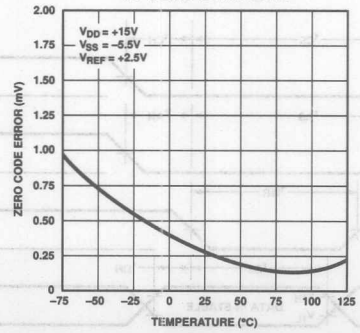
SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



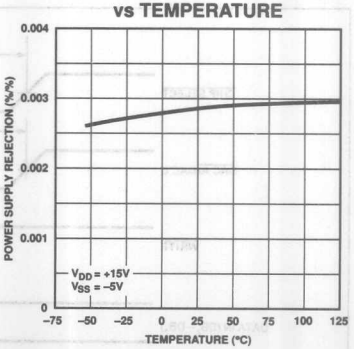
FULL-SCALE GAIN ERROR vs TEMPERATURE



ZERO CODE ERROR vs TEMPERATURE

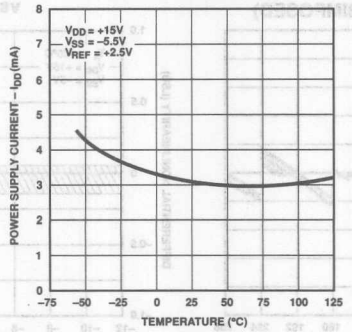


POWER SUPPLY REJECTION vs TEMPERATURE

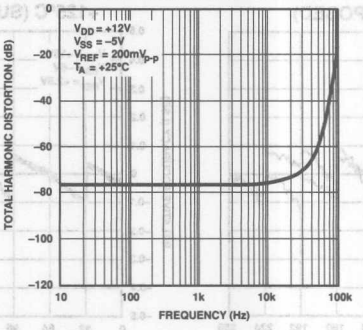


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

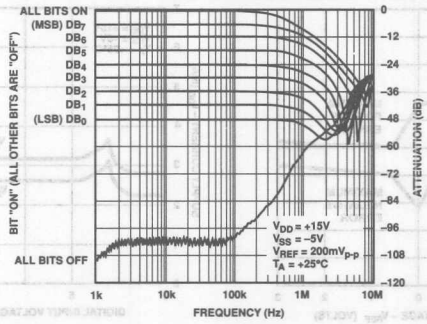
POWER SUPPLY CURRENT vs TEMPERATURE



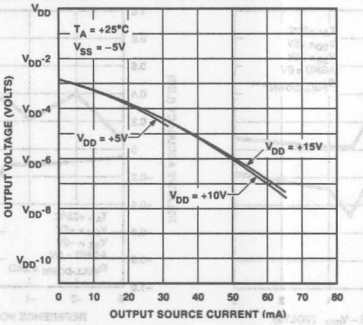
TOTAL HARMONIC DISTORTION vs FREQUENCY



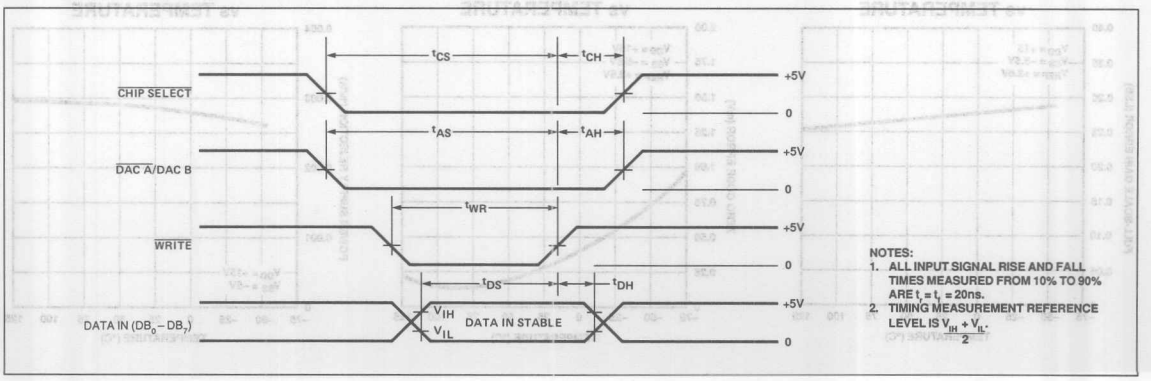
MULTIPLYING MODE, FREQUENCY RESPONSE vs DIGITAL CODE



OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

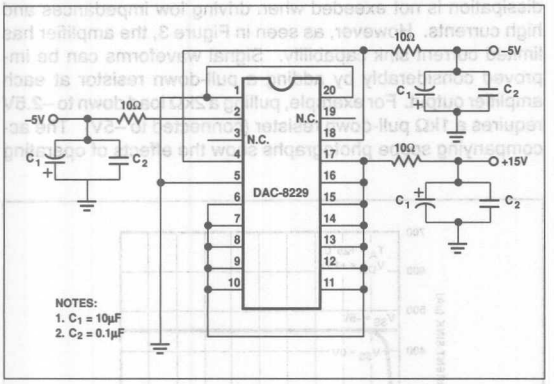


WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

BURN-IN CIRCUIT



PARAMETER DEFINITIONS

RESOLUTION (N)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be non-monotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal. Zero code error is not included in this measurement.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

The DAC-8229 consists of two voltage output amplifiers, two high accuracy R-2R resistor ladder networks, an 8-bit input buffer, two 8-bit DAC registers, and interface control logic circuitry.

Also included are 16 single-pole, double-throw NMOS transistor switches. These switches, which are controlled by the digital input code, were designed to switch each R-2R resistor leg between the amplifier inverting input and AGND.

A simplified circuit of the R-2R resistor ladder and output amplifier is illustrated in Figure 1. The signal is inverted from the V_{REF} input to the output. Note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section under Single Supply Operation.

REFERENCE INPUT

The DAC-8229's internal output amplifier has a maximum voltage swing in the negative direction of –2.5V (limited by V_{SS}). In

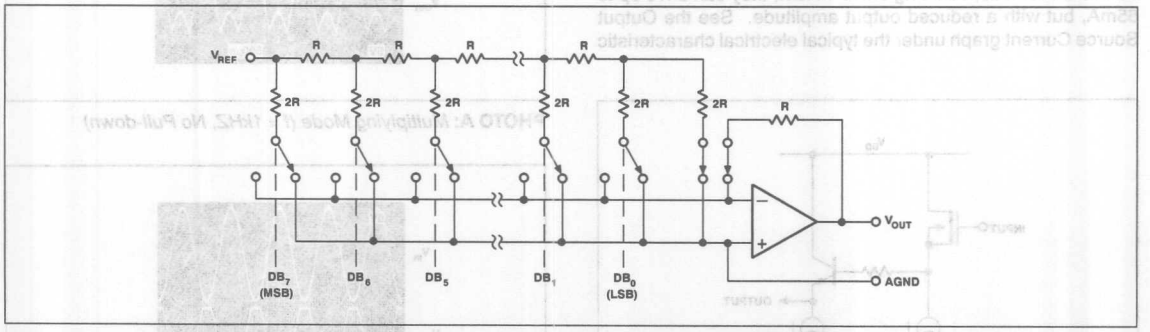


FIGURE 1: *Simplified single DAC configuration (switches shown for all digital inputs at logic "0").*

the positive direction, the voltage swing is limited to 4V less than V_{DD}. These limitations set the maximum levels that the reference input (V_{REF}) can accept. Note that the positive V_{REF} limit is set by the negative supply voltage, V_{SS}, and the negative V_{REF} limit is set by (V_{DD} –4V).

For example, maximum V_{REF} input in the positive direction is +2.5V and –11V with V_{DD} = +15V. The equation for the absolute value in the negative direction takes the form of:

$|-V_{REF}\ max| = V_{DD} - 4V.$

The equation shows that –8V is the maximum voltage that can be applied in the negative direction at V_{REF} with V_{DD} = +12V.

The DAC-8229's output voltage equation is:

$-V_{OUT} = V_{REF} \times D/256$

where D is the digital input code number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

The DAC-8229's amplifier output stage is an NPN bipolar transistor. This transistor provides a low-impedance high-output current capability. The emitter of the NPN transistor is loaded with a 450µA NMOS current source that is connected to V_{SS}; (see Figure 2). This current is sunk into the negative supply allowing the amplifier's output to go to –2.5V.

Figure 3 depicts a typical output current-sink versus voltage graph for the DAC-8229. It shows the output amplifier's current sink capability with V_{SS} = –5V and 0V. With V_{SS} = –5V, the amplifier still operates in the saturation region as the output goes to zero; however, with V_{SS} = 0V, the amplifier comes out of its saturation region and starts appearing resistive as the output approaches zero.

The DAC-8229's internal amplifiers can each drive +10 volts across a 2kΩ load, sourcing 5mA. In fact, they can drive up to 65mA, but with a reduced output amplitude. See the Output Source Current graph under the typical electrical characteristic curves. The user must use caution that the package power dissipation is not exeeded when driving low impedances and high currents. However, as seen in Figure 3, the amplifier has limited current sink capability. Signal waveforms can be improved considerably by adding a pull-down resistor at each amplifier output. For example, pulling a 2kΩ load down to –2.5V requires a 1kΩ pull-down resister (connected to –5V) The accompanying scope photographs show the effects of operating

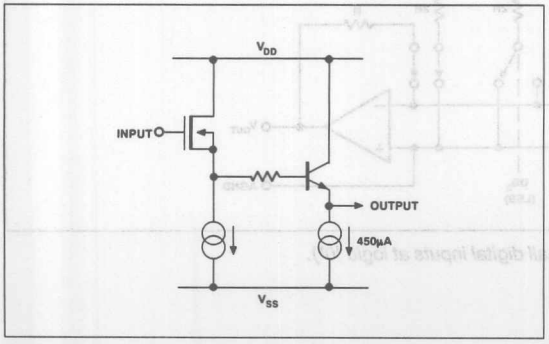


FIGURE 2: *Amplifier Output Stage*

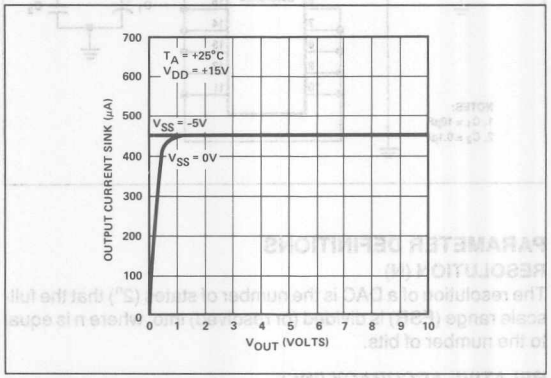


FIGURE 3: *DAC Output Current Sink*

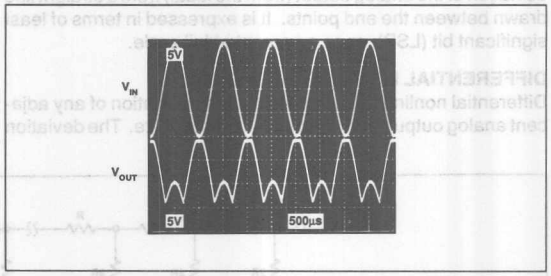


PHOTO A: *Multiplying Mode (f = 1kHZ, No Pull-down)*

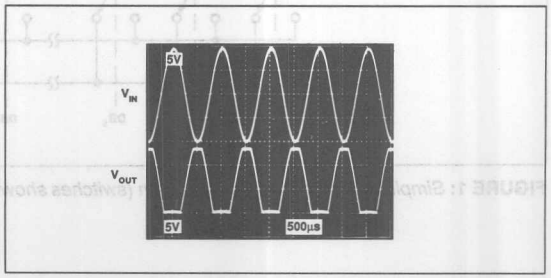


PHOTO B: *Multiplying Mode (f = 1kHZ, with 1kΩ Pull-down)*

A is that without the pull-down resistor, and B with the 1kΩ pull-down resistor. Note signal improvement using the pull-down resistor. Figure 4 shows this circuit configuration and the table lists other resistor values.

PULL-DOWN RESISTOR vs LOAD RESISTOR VALUES

(V_{DD} = +15V; V_{SS} = –5V)

LOAD	PULL-DOWN
2kΩ	1kΩ
5kΩ	4kΩ
10kΩ	10kΩ
15kΩ	12kΩ
20kΩ	16kΩ
25kΩ	400kΩ
>30kΩ	None Required

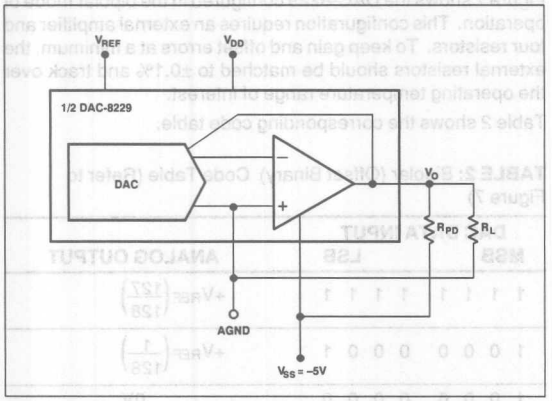


FIGURE 4: *R_{LOAD} and $R_{PULL-DOWN}$ Circuit Configuration with the DAC-8229*

The DAC-8229 can also operate with ±5V supplies, V_{DD} = +5V and V_{SS} = –5V. See the Relative Accuracy vs. Reference Voltage graphs under the typical characteristics curves. The graphs are shown with and without a 2kΩ pull-down resistor. Note how the DAC stays within the specified limit except when V_{REF} = –2V and without the pull-down resistor.

The amplifier's internal gain stages were designed to maintain sufficient gain over its common mode range. This results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during manufacturing. This eliminates user offset trimming in many applications.

2

DIGITAL SECTION

Figure 5 shows one digital input structure of the DAC-8229. A built-in 5V regulator and level shifter converts TTL digital input signals into CMOS levels to drive the internal circuitry. This provides full TTL compatibility over a V_{DD} range of 5 to 15V.

As shown in Figure 5, each digital input is protected from electrostatic-discharge with two internal diodes connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

INTERFACE CONTROL INFORMATION

DAC SELECTION

DAC A and DAC B both share a common 8-bit input port. The control input, $\overline{\text{DAC A}}$/DAC B, selects which DAC can accept data from the input port. A logic low selects DAC A and a logic high selects DAC B.

DAC OPERATION

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operation of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to the codes on the digital input pins.

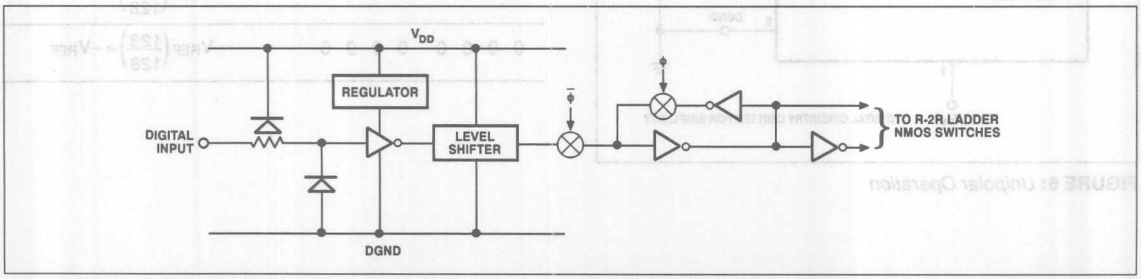


FIGURE 5: *Simplified Digital Input Structure*

HOLD MODE

The selected DAC register latches the data present on the digital input pins just prior to $\overline{CS}$ and $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

DAC A/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 6 shows the DAC-8229 configured to operate in the unipolar mode, and Table 1 shows the corresponding code table. The equation for 1 LSB and the analog output voltage is:

$1\ LSB = V_{REF} \times 2^{-8}$, or $V_{REF} \times 1/256$

and

$-V_{OUT} = V_{REF} \times D/256$

where D is the digital input number between 0 and 255.

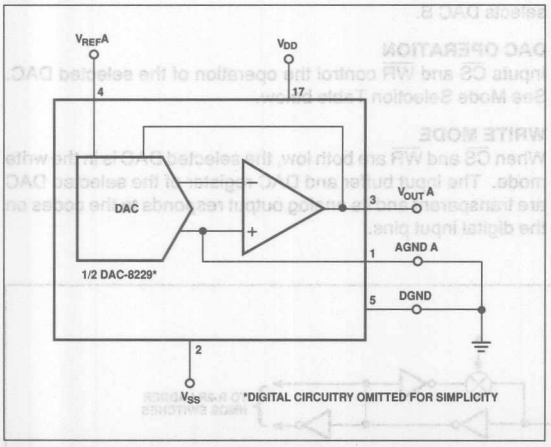


FIGURE 6: *Unipolar Operation*

TABLE 1: Unipolar Code Table (Refer to Figure 6)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = \frac{-V_{REF}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

BIPOLAR OPERATION

Figure 7 shows the DAC-8229 configured in the bipolar mode of operation. This configuration requires an external amplifier and four resistors. To keep gain and offset errors at a minimum, the external resistors should be matched to ±0.1% and track over the operating temperature range of interest.

Table 2 shows the corresponding code table.

TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 7)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

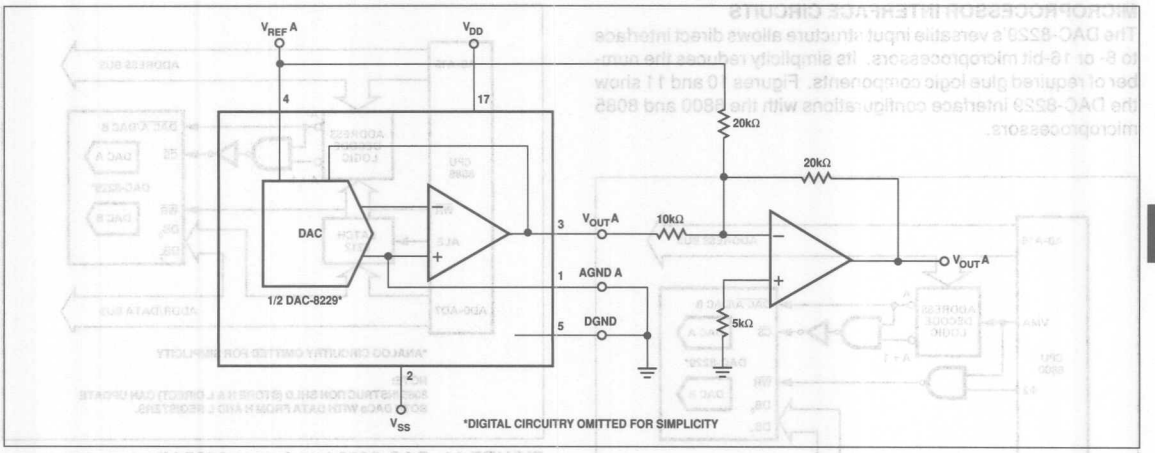


FIGURE 7: *Bipolar Operation*

SINGLE SUPPLY OPERATION

Some applications require the AGND pin to be biased above ground for single supply operation. A popular scheme is shown in Figure 8. It consists of connecting a +2.5 volt reference (such as PMI's REF-03) to the AGND pin, V_{REF} and V_{SS} pins grounded, and +12V to V_{DD}. Both DAC A and DAC B AGND pins are separate and can be independently biased.

The resulting transfer equation is:

$V_{OUT}(D) = 2.5(1 + D/256)$

where D is the whole number binary digital input.

V_{OUT} for the circuit of Figure 8 results in:

$V_{OUT}(255) = 2.5(1 + 255/256) = +5V$

$V_{OUT}(0) = +2.5V.$

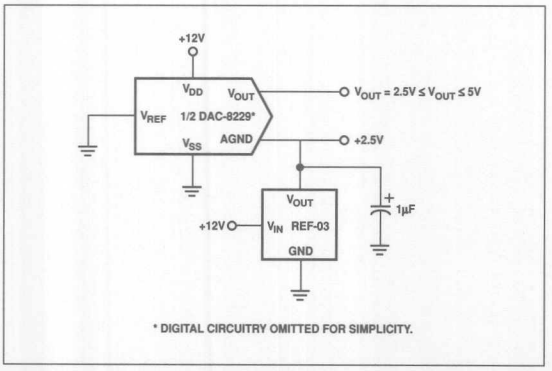


FIGURE 8: *Single Supply Configuration*

Figure 9 shows a typical plot of the DAC-8229 in the single-supply configuration of Figure 8. It is plotted for various values of AGND voltage biased above ground. It shows relative accuracy degrading as AGND is taken above +4V; however, it contributes only 1 LSB error at +5V.

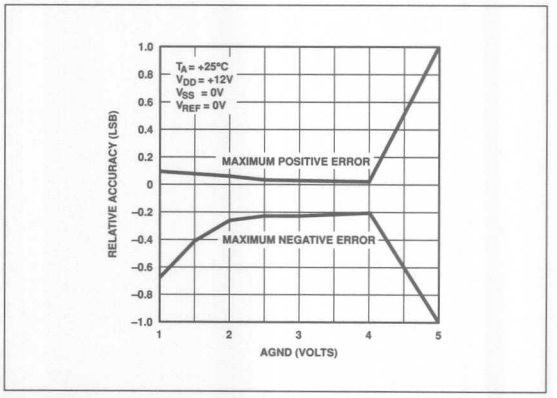


FIGURE 9: *Relative Accuracy vs. AGND*

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8229's versatile input structure allows direct interface to 8- or 16-bit microprocessors. Its simplicity reduces the number of required glue logic components. Figures 10 and 11 show the DAC-8229 interface configurations with the 6800 and 8085 microprocessors.

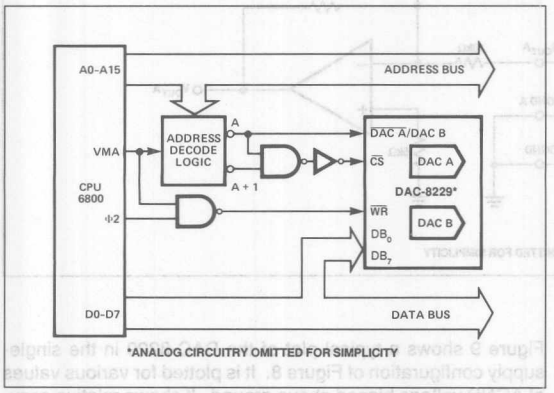


FIGURE 10: *DAC-8229 Interface to 6800 Microprocessor*

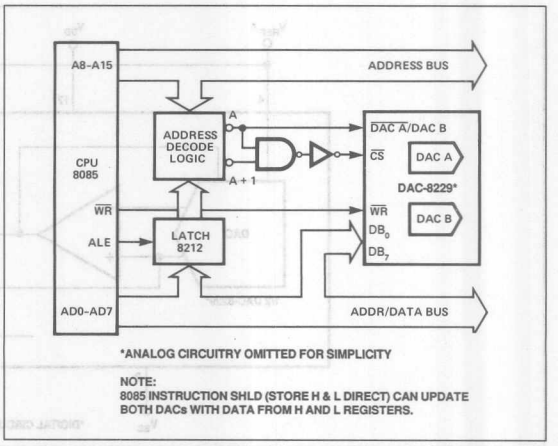


FIGURE 11: *DAC-8229 Interface to 8085 Microprocessor*

FEATURES

- Two Matched 12-Bit DACs on One Chip
- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface with 8-Bit Microprocessors
- Double-Buffered Digital Inputs
- RESET to Zero Pin
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- Latch-Up Resistant
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package
- Available in Die Form

APPLICATIONS

- Multi-Channel Microprocessor-Controlled Systems
- Robotics/Process Control/Automation
- Automatic Test Equipment
- Programmable Attenuator, Power Supplies, Window Comparators
- Instrumentation Equipment
- Battery Operated Equipment

GENERAL DESCRIPTION

The DAC-8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that interfaces directly with 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC-8222 or DAC-8221.

The DAC-8248's double-buffered digital inputs allow both DAC's analog output to be updated simultaneously. This is particularly useful in multiple DAC systems where a common $\overline{\text{LDAC}}$ signal updates all DACs at the same time. A single $\overline{\text{RESET}}$ pin resets both outputs to zero.

ORDERING INFORMATION†

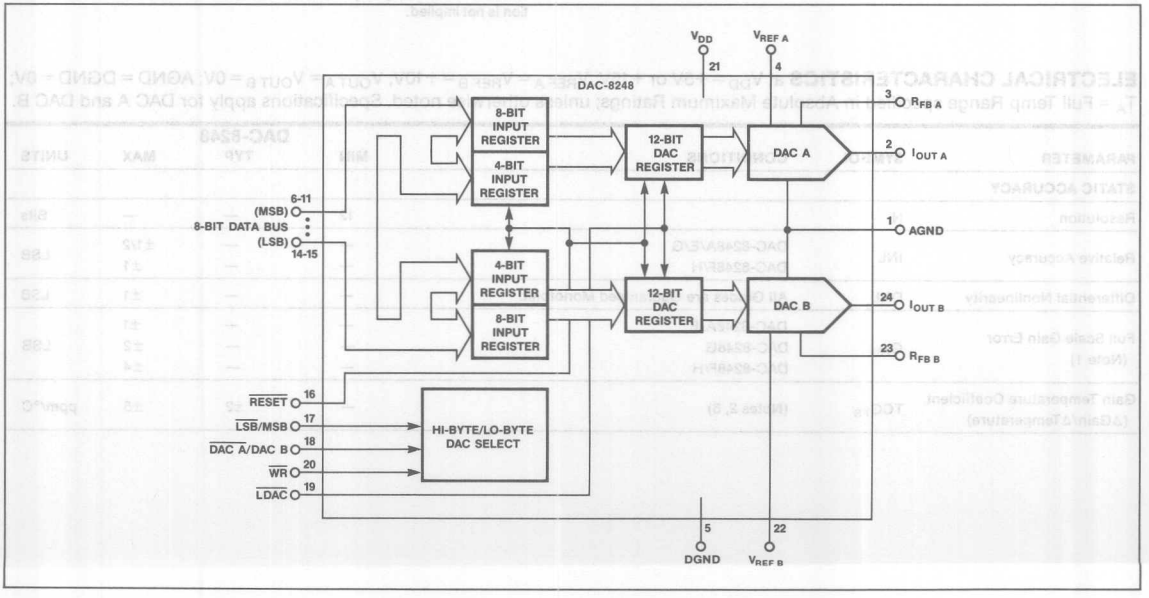
RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE −40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8248AW	DAC8248EW	—
±1/2 LSB	±2 LSB	—	—	DAC8248GP
±1 LSB	±4 LSB	—	DAC8248FW	DAC8248HP
±1 LSB	±4 LSB	—	DAC8248FP	DAC8248HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

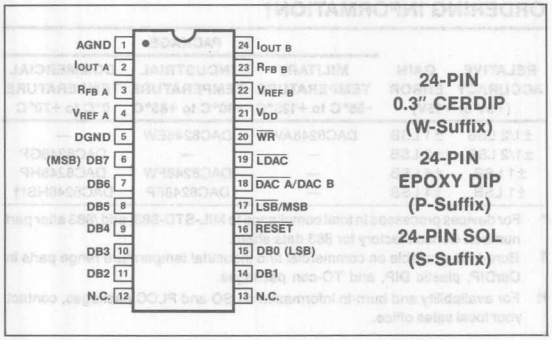
FUNCTIONAL DIAGRAM



ature range. The DAC consists of two thin-film R-2R resistor ladder networks, two 12-bit, two 8-bit, and two 4-bit data registers, and control logic circuitry. Separate reference input and feedback resistors are provided for each DAC. The DAC-8248 operates on a single supply from +5V to +15V, and it dissipates less than 0.5mW at +5V (using zero or V_{DD} logic levels). The device is packaged in a space-saving 0.3", 24-pin DIP.

The DAC-8248 is manufactured with PMI's highly-stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

PIN CONNECTIONS



24-PIN 0.3" CERDIP (W-Suffix)

24-PIN EPOXY DIP (P-Suffix)

24-PIN SOL (S-Suffix)

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF\ A}$, $V_{REF\ B}$ to AGND ..... ±25V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
  AW Version ..... –55°C to +125°C
  EW, FW, FP Versions ..... –40°C to +85°C
  GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods. This is a stress rating only and functional operation at or above this specification is not implied.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V; $V_{REF\ A} = V_{REF\ B}$ = +10V; $V_{OUT\ A} = V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS	DAC-8248 MIN	DAC-8248 TYP	DAC-8248 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Relative Accuracy	INL	DAC-8248A/E/G	—	—	±1/2	LSB
		DAC-8248F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	—	—	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8248A/E	—	—	±1	LSB
		DAC-8248G	—	—	±2	
		DAC-8248F/H	—	—	±4	
Gain Temperature Coefficient (ΔGain/ΔTemperature)	TCG_{FS}	(Notes 2, 6)	—	±2	±5	ppm/°C

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V; $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; $V_{OUT\,A}$ = $V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

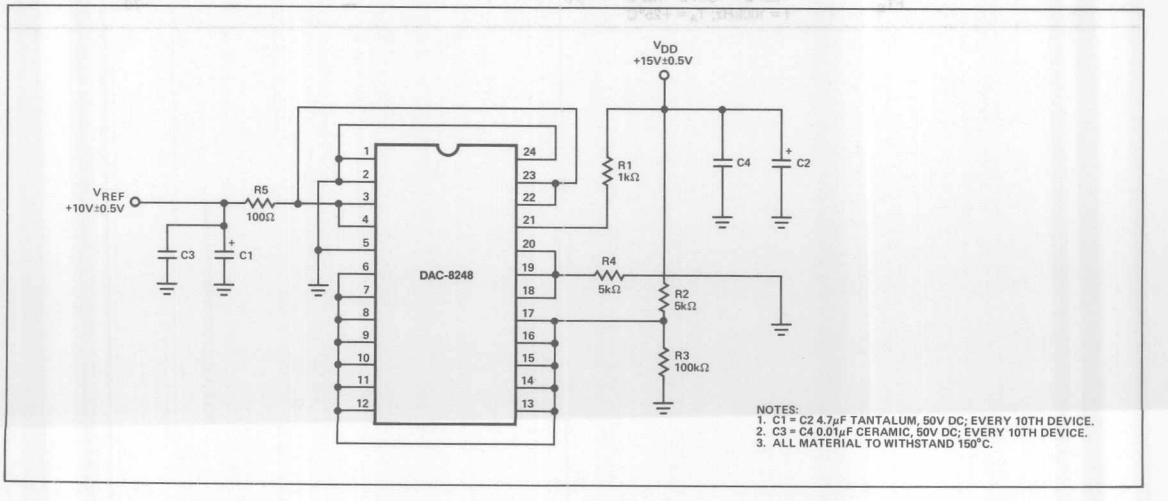
PARAMETER	SYMBOL	CONDITIONS	DAC-8248 MIN	TYP	MAX	UNITS
Output Leakage Current $I_{OUT\,A}$ (Pin 2), $I_{OUT\,B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0s T_A = +25°C T_A = Full Temp. Range	— —	±5 —	±10 ±50	nA
Input Resistance ($V_{REF\,A,\,REF\,B}$)	R_{REF}	(Note 9)	8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		—	±0.2	±1	%
DIGITAL INPUTS						
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	— —	— —	V
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	— —	— —	0.8 1.5	V
Input Current (V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH})	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	±0.001 —	±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB11 $\overline{WR}$, $\overline{LDAC}$, $\overline{DAC\ A}$/DAC B, $\overline{LSB}$/$\overline{MSB}$, $\overline{RESET}$	— —	— —	10 15	pF
POWER SUPPLY						
Supply Current	I_{DD}	Digital Inputs = V_{INL} or V_{INH} Digital Inputs = 0V or V_{DD}	— —	— 10	2 100	mA μA
DC Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 3, 4)	t_{PD}	T_A = +25°C	—	—	350	ns
Output Current Settling Time (Notes 4, 5)	t_s	T_A = +25°C	—	—	1	μs
Output Capacitance	C_O	Digital Inputs = all 0s $C_{OUT\,A}$, $C_{OUT\,B}$ Digital Inputs = all 1s $C_{OUT\,A}$, $C_{OUT\,B}$	— —	— —	90 120	pF
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = 20V_{p-p} f = 100kHz; T_A = +25°C	—	—	−70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = 20V_{p-p} f = 100kHz; T_A = +25°C	—	—	−70	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\,A} = V_{REF\,B}$ = +10V; $V_{OUT\,A} = V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8248				UNITS
			V_{DD} = +5V			V_{DD} = +15V	
SWITCHING CHARACTERISTICS (Notes 2, 7)			+25°C	−40°C TO +85°C (Note 8)	−55°C TO +125°C	ALL TEMPS (Note 10)	
$\overline{LSB}$/MSB Select to Write Set-Up Time	t_{CBS}		130	170	180	80	ns MIN
$\overline{LSB}$/MSB Select to Write Hold Time	t_{CBH}		0	0	0	0	ns MIN
DAC Select to Write Set-Up Time	t_{AS}		180	210	220	80	ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0	ns MIN
LDAC to Write Set-Up Time	t_{LS}		120	150	160	80	ns MIN
LDAC to Write Hold Time	t_{LH}		0	0	0	0	ns MIN
Data Valid to Write Set-Up Time	t_{DS}		160	210	220	70	ns MIN
Data Valid to Write Hold Time	t_{DH}		0	0	0	10	ns MIN
Write Pulse Width	t_{WR}		130	150	170	90	ns MIN
LDAC Pulse Width	t_{LWD}		100	110	130	60	ns MIN
Reset Pulse Width	t_{RWD}		80	90	90	60	ns MIN

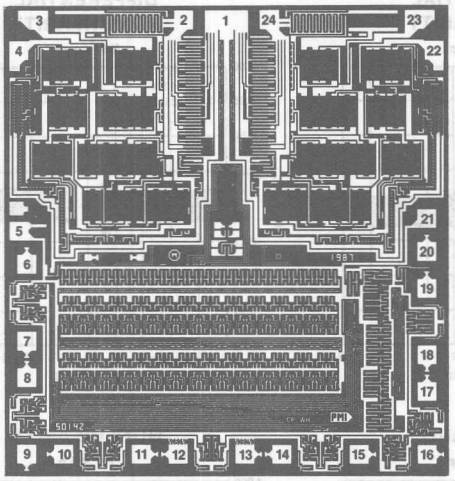
NOTES:
1. Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. From 50% of digital input to 90% of final analog output current. $V_{REF\,A} = V_{REF\,B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
4. $\overline{WR}$, $\overline{LDAC}$ = 0V; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
5. Settling time is measured from 50% of the digital input change to where the output settles within 1/2 LSB of full scale.
6. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
7. See Timing Diagram.
8. These limits apply for the commercial and industrial grade products.
9. Absolute Temperature Coefficient is approximately +50 ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

BURN-IN CIRCUIT



NOTES:
1. C1 = C2 4.7μF TANTALUM, 50V DC; EVERY 10TH DEVICE.
2. C3 = C4 0.01μF CERAMIC, 50V DC; EVERY 10TH DEVICE.
3. ALL MATERIAL TO WITHSTAND 150°C.

DICE CHARACTERISTICS



1. AGND
2. $I_{OUT\ A}$
3. $R_{FB\ A}$
4. $V_{REF\ A}$
5. DGND
6. DB7(MSB)
7. DB6
8. DB5
9. DB4
10. DB3
11. DB2
12. N.C.
13. N.C.
14. DB1
15. DB0(LSB)
16. $\overline{\text{RESET}}$
17. $\overline{\text{LSB}}$/MSB
18. $\overline{\text{DAC A}}$/DAC B
19. $\overline{\text{LDAC}}$
20. $\overline{\text{WR}}$
21. V_{DD}
22. $V_{REF\ B}$
23. $R_{FB\ B}$
24. $I_{OUT\ B}$

Substrate (die backside) is internally connected to V_{DD}.

DIE SIZE 0.124 × 0.132 inch, 16,368 sq. mils (3.15 × 3.55 mm, 10.56 sq. mm)

2

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF\ A} = V_{REF\ B}$ = +10V, $V_{OUT\ A} = V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = 25°C.

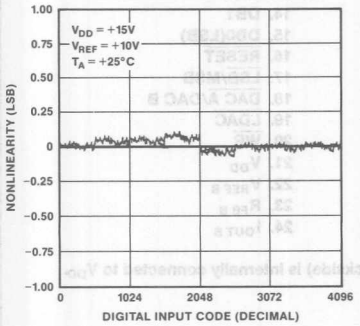
PARAMETER	SYMBOL	CONDITIONS	DAC-8248G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB MAX
Full Scale Gain Error (Note 1)	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage ($I_{OUT\ A}$, $I_{OUT\ B}$)	I_{LKG}	Digital Inputs = 0000 0000 0000 Pad 2 and 24	±50	nA MAX
Input Resistance ($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	Pad 4 and 22	8/15	kΩMIN/ kΩMAX
$V_{REF\ A}$, $V_{REF\ B}$ Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	%MAX
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}; V_{INL} or V_{INH}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV_{DD})	PSR	ΔV_{DD} = ±5%	0.002	%/% MAX

NOTES:
1. Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$.

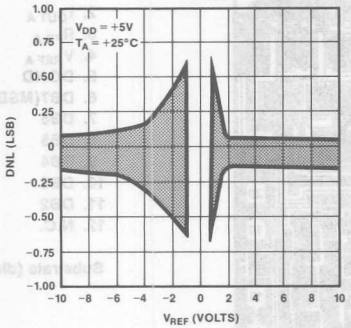
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

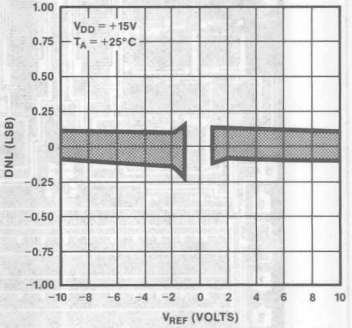
CHANNEL-TO-CHANNEL MATCHING (DAC A & B ARE SUPERIMPOSED)



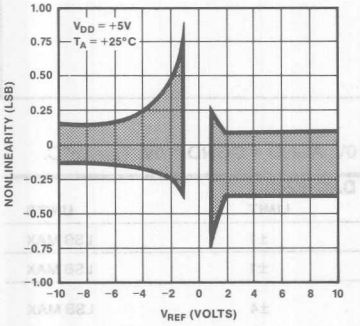
DIFFERENTIAL NONLINEARITY vs V_{REF}



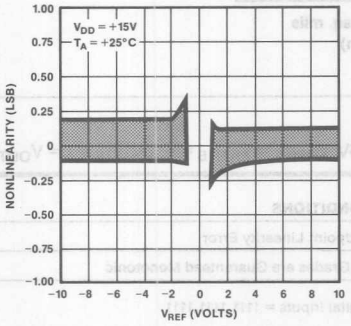
DIFFERENTIAL NONLINEARITY vs V_{REF}



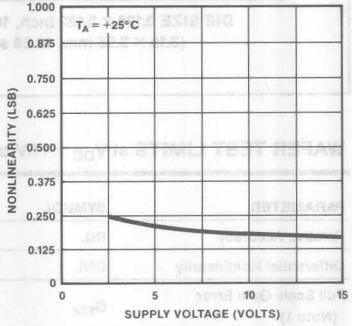
NONLINEARITY vs V_{REF}



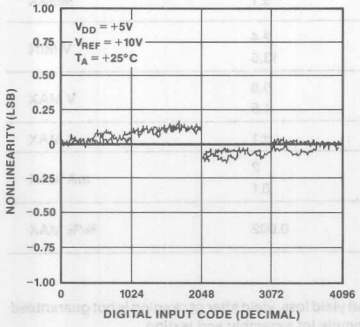
NONLINEARITY vs V_{REF}



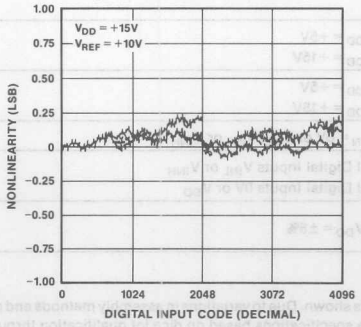
NONLINEARITY vs V_{DD}



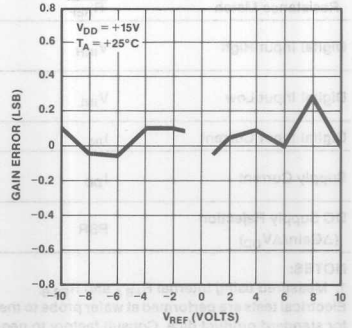
NONLINEARITY vs CODE (DAC A & B ARE SUPERIMPOSED)



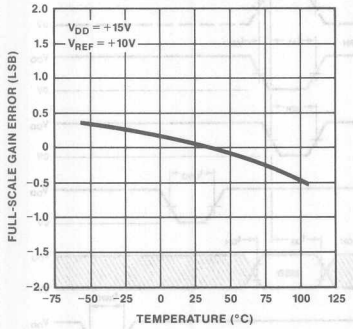
NONLINEARITY vs CODE AT T_A = −55°C, +25°C, +125°C FOR DAC A & B (ALL SUPERIMPOSED)



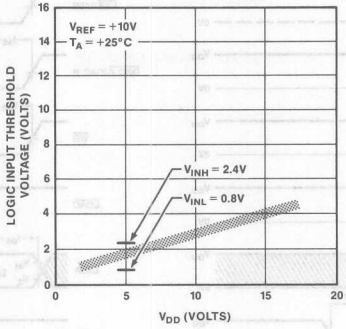
ABSOLUTE GAIN ERROR CHANGE vs V_{REF}



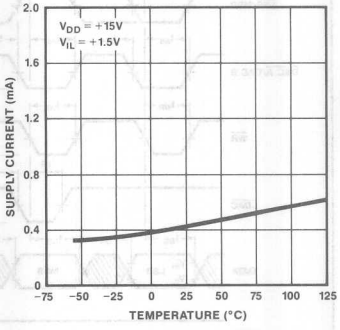
FULL-SCALE GAIN ERROR vs TEMPERATURE



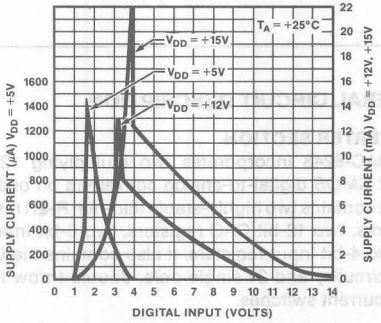
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



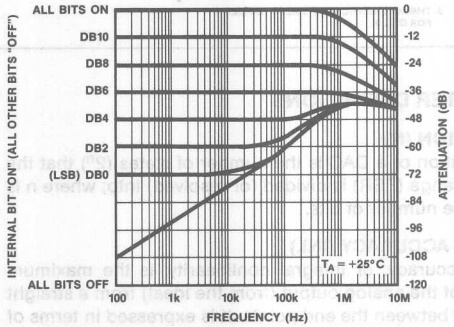
SUPPLY CURRENT vs TEMPERATURE



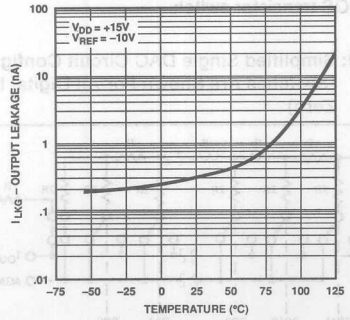
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



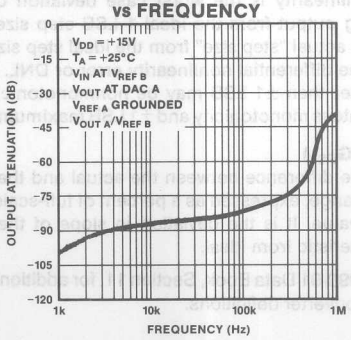
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



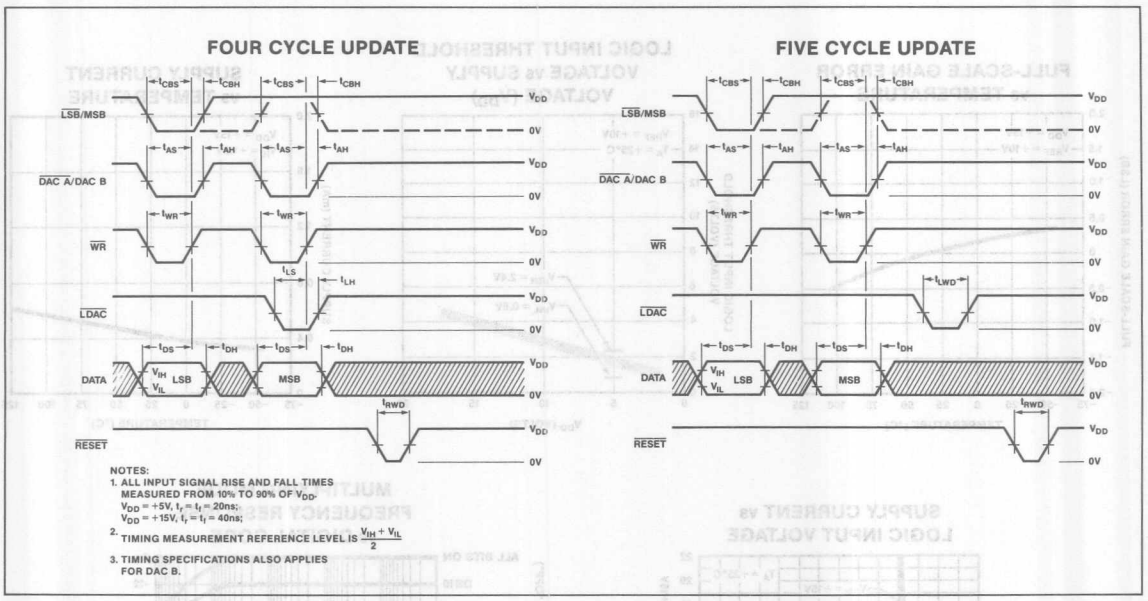
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



ANALOG CROSSTALK vs FREQUENCY



WRITE TIMING CYCLE DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION (N)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

Refer to PMI 1990/91 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC-8248 incorporates two multiplying 12-bit current output CMOS digital-to-analog converters on one monolithic chip. It contains two highly-stable thin-film R-2R resistor ladder networks, two 12-bit DAC registers, two 8-bit input registers, and two 4-bit input registers. It also contains the DAC control logic circuitry and 24 single-pole, double-throw NMOS transistor current switches.

Figure 1 shows a simplified circuit for the R-2R ladder and transistor switches for a single DAC. R is typically 11kΩ. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. Figure 2 shows a single NMOS transistor switch.

FIGURE 1: Simplified Single DAC Circuit Configuration. (Switches Are Shown For All Digital Inputs At Zero)

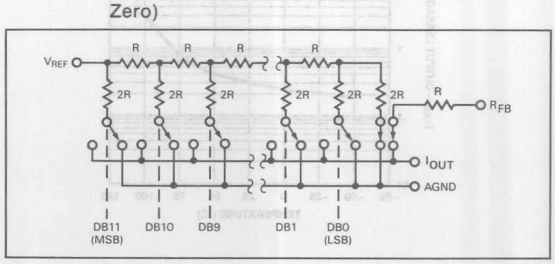
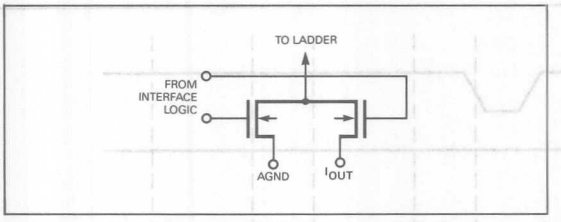


FIGURE 2: N-Channel Current Steering Switch



The binary-weighted currents are switched between I_{OUT} and AGND by the transistor switches. Selection between I_{OUT} and AGND is determined by the digital input code. It is important to keep the voltage difference between I_{OUT} and AGND terminals as close to zero as practical to preserve data sheet limits. It is easily accomplished by connecting the DAC's AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The amplifier's feedback resistor can be eliminated by connecting the op amp's output directly to the DAC's R_{FB} terminal (by using the DAC's internal feedback resistor, R_{FB}). The amplifier also provides the current-to-voltage conversion for the DAC's output current.

The output voltage is dependent on the DAC's digital input code and V_{REF}, and is given by:

$$V_{OUT} = V_{REF} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

The DAC's input resistance, R_{REF}, is always equal to a constant value, R. This means that V_{REF} can be driven by a reference voltage or current, AC or DC (positive or negative). It is recommended that a low-temperature-coefficient external R_{FB} resistor be used if a current source is employed.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90pF (all digital inputs low) to 120pF (all digital inputs high).

To ensure accuracy over the full operating temperature range, permanently turned "ON" MOS transistor switches were included in series with the feedback resistor (R_{FB}) and the R-2R ladder's terminating resistor (see Figure 1). The gates of these NMOS transistors are internally connected to V_{DD} and will be turned "OFF" (open) if V_{DD} is not applied. If an op amp is using the DAC's R_{FB} resistor to close its feedback loop, then V_{DD} must be applied before or at the same time as the op amp's supply; this will prevent the op amp's output from becoming "open-circuited" and swinging to either rail. In addition, some applications require the DAC's ladder resistance to fall within a certain range and are measured at incoming inspection; V_{DD} must be applied before these measurements can be made.

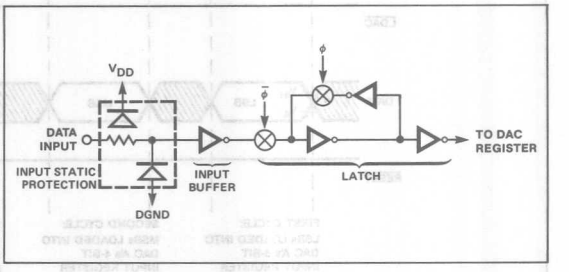
DIGITAL SECTION

The DAC-8248's digital inputs are TTL compatible at V_{DD} = +5V and CMOS compatible at V_{DD} = +15V. They were designed to convert TTL and CMOS input logic levels into voltage levels that will drive the internal circuitry. The DAC-8248 can use +5V CMOS logic levels with V_{DD} = +12V; however, supply current will increase to approximately 5-6mA.

Figure 3 shows the DAC's digital input structure for one bit. This circuitry drives the DAC registers. Digital controls, ϕ and $\overline{\phi}$, shown are generated from the DAC's input control logic circuitry.

2

FIGURE 3: Digital Input Structure For One Bit



The digital inputs are electrostatic-discharge (ESD) protected with two internal distributed diodes as shown in Figure 3; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

The digital inputs are CMOS inverters and draw supply current when operating in their linear region. Using a +5V supply, the linear region is between +1.2V to +2.8V with current peaking at +1.8V. Using a +15V supply, the linear region is from +1.2V to +12V (current peaking at +3.9V). It is recommended that the digital inputs be operated as close to the power supply voltage and DGND as is practically possible; this will keep supply currents to a minimum. The DAC-8248 may be operated with any supply voltage between the range of +5V to +15V and still perform to data sheet limits.

The DAC-8248's 8-bit wide data port loads a 12-bit word in two bytes: 8-bits then 4-bits (or 4-bits first then 8-bits, at users discretion) in a right justified data format. This data is loaded into the input registers with the $\overline{LSB}$/MSB and $\overline{WR}$ control pins.

Data transfer from the input registers to the DAC registers can be automatic. It can occur upon loading of the second data byte into the input register, or can occur at a later time through a strobed transfer using the $\overline{LDAC}$ control pin.

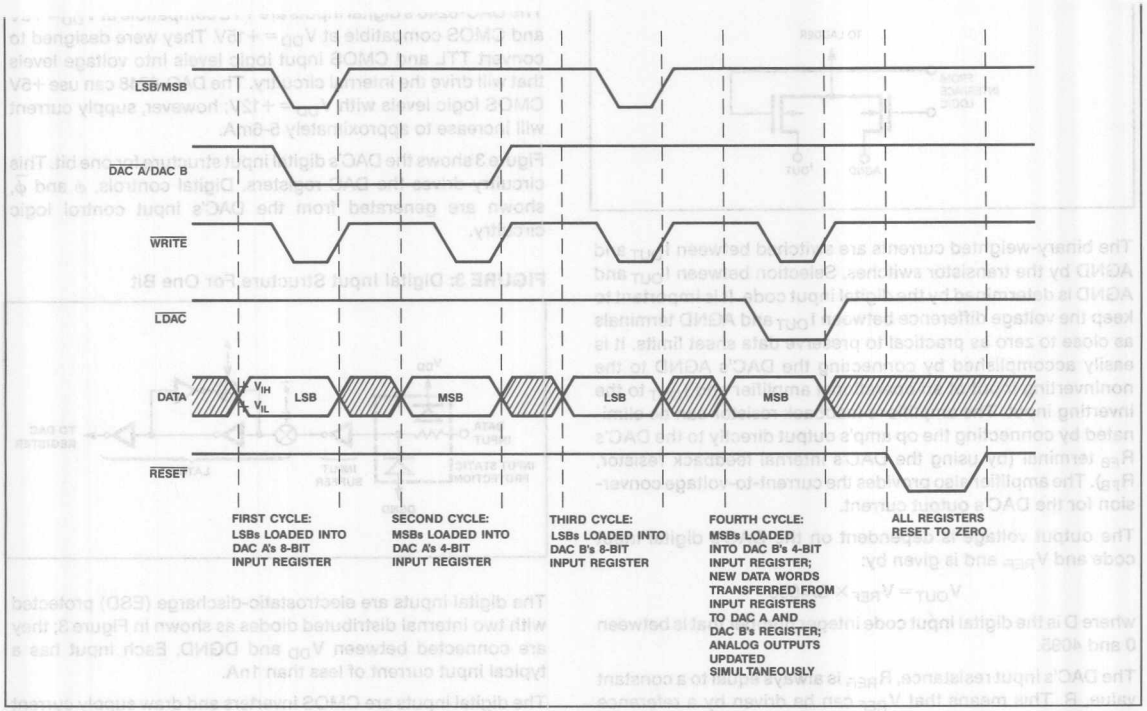
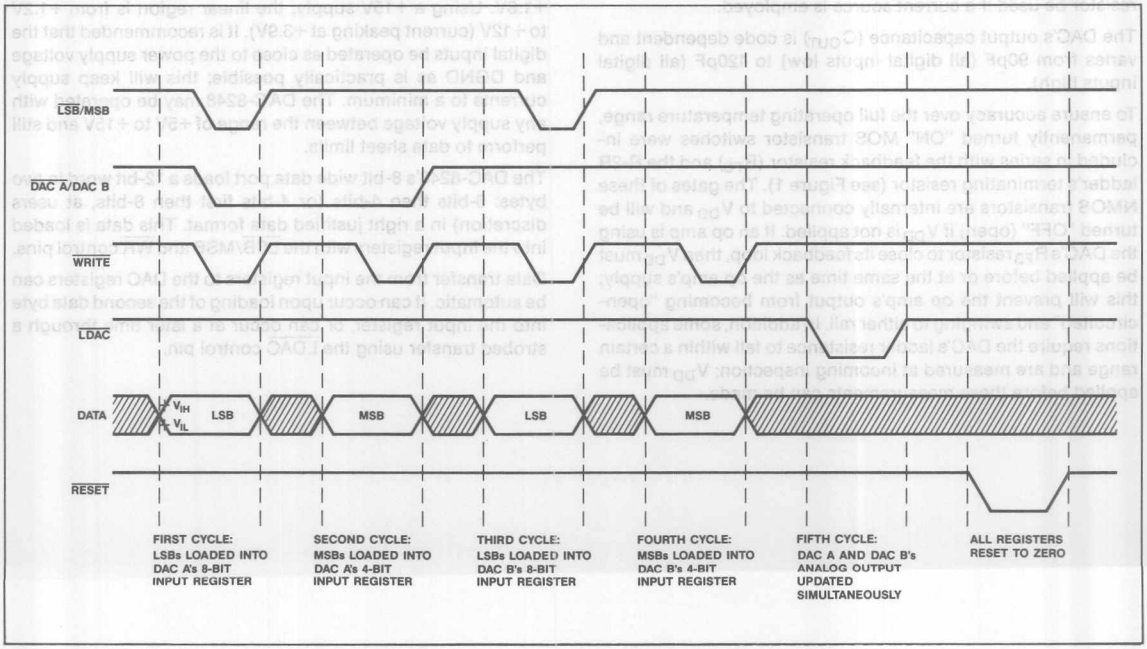


FIGURE 5: Five Cycle Update Timing Diagram



the DAC register. The first cycle loads the first data byte into the input register; the second cycle loads the second data byte and simultaneously transfers the full 12-bit data word to the DAC register. It takes four cycles to load and transfer two complete digital words for both DAC's, see Figure 4 (Four Cycle Update Timing Diagram) and the Mode Selection Table.

STROBED DATA TRANSFER MODE

Strobed data transfer allows the full 12-bit digital word to be loaded into the input registers and transferred to the DAC registers at a later time. This transfer mode requires five cycles: four to load two new data words into both DACs, and the fifth to transfer all data into the DAC registers. See Figure 5 (Five Cycle Update Timing Diagram) and the Mode Selection Table.

operations serves two functions: the DAC output updating may be more precisely controlled, and multiple DACs in a multiple DAC system can be updated simultaneously.

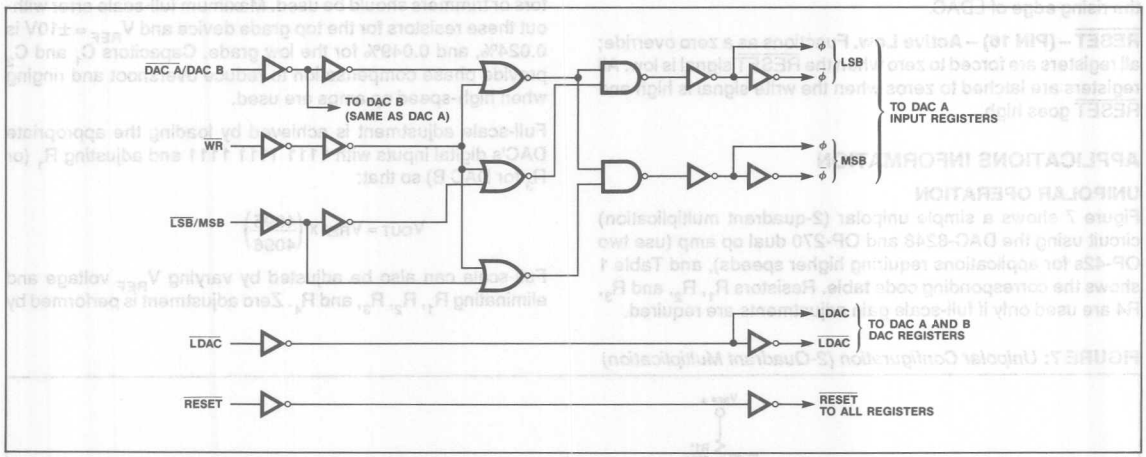
RESET

The DAC-8248 comes with a $\overline{\text{RESET}}$ pin that is useful in system calibration cycles and/or during system power-up. All registers are reset to zero when $\overline{\text{RESET}}$ is low, and latched at zero on the rising edge of the $\overline{\text{RESET}}$ signal when $\overline{\text{WRITE}}$ is high.

INTERFACE CONTROL LOGIC

The DAC-8248's control logic is shown in Figure 6. This circuitry interfaces with the system bus and controls the DAC functions.

FIGURE 6: Input Control Logic



MODE SELECTION TABLE

DIGITAL INPUTS					REGISTER STATUS					
					DAC A			DAC B		
					INPUT REGISTER		DAC	INPUT REGISTER		DAC
DAC $\overline{\text{A}}$/B	$\overline{\text{WR}}$	$\overline{\text{LSB}}$/MSB	$\overline{\text{RESET}}$	$\overline{\text{LDAC}}$	LSB	MSB	REGISTER	LSB	MSB	REGISTER
L	L	L	H	H	WR	LAT	LAT	LAT	LAT	LAT
L	L	L	H	L	WR	LAT	WR	LAT	LAT	WR
L	L	H	H	H	LAT	WR	LAT	LAT	LAT	LAT
L	L	H	H	L	LAT	WR	WR	LAT	LAT	WR
H	L	L	H	H	LAT	LAT	LAT	WR	LAT	LAT
H	L	L	H	L	LAT	LAT	WR	WR	LAT	WR
H	L	H	H	H	LAT	LAT	LAT	LAT	WR	LAT
H	L	H	H	L	LAT	LAT	WR	LAT	WR	WR
X	H	X	H	H	LAT	LAT	LAT	LAT	LAT	LAT
X	H	X	H	L	LAT	LAT	WR	LAT	LAT	WR
X	X	X	L	X	ALL REGISTERS ARE RESET TO ZEROS					
X	H	X	↓	X	ZEROS ARE LATCHED IN ALL REGISTERS					

L = Low H = High X = Don't Care WR = Registers Being Loaded LAT = Registers Latched

INTERFACE CONTROL LOGIC PIN FUNCTIONS

$\overline{\text{LSB}}$/MSB – (PIN 17) $\overline{\text{LEAST SIGNIFICANT BIT}}$(Active Low)/ MOST SIGNIFICANT BIT (Active High). Selects lower 8-bits (LSBs) or upper 4-bits (MSBs); either can be loaded first. It is used with the $\overline{\text{WR}}$ signal to load data into the input registers. Data is loaded in a right justified format.

$\overline{\text{DAC A}}$/DAC B – (PIN 18) DAC SELECTION. Active low for DAC A and Active High for DAC B.

$\overline{\text{WR}}$ – (PIN 20) $\overline{\text{WRITE}}$ – Active Low. Used with the $\overline{\text{LSB}}$/MSB signal to load data into the input registers, or Active High to latch data into the input registers.

$\overline{\text{LDAC}}$ – (PIN 19) LOAD DAC. Used to transfer data simultaneously from DAC A and DAC B input registers to both DAC output registers. The DAC register becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ are low. Data is latched into the output registers on the rising edge of $\overline{\text{LDAC}}$.

$\overline{\text{RESET}}$ – (PIN 16) – Active Low. Functions as a zero override; all registers are forced to zero when the $\overline{\text{RESET}}$ signal is low. All registers are latched to zeros when the write signal is high and $\overline{\text{RESET}}$ goes high.

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 7 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8248 and OP-270 dual op amp (use two OP-42s for applications requiring higher speeds), and Table 1 shows the corresponding code table. Resistors R_1, R_2, and R_3, R4 are used only if full-scale gain adjustments are required.

TABLE 1: Unipolar Binary Code Table (Refer to Figure 7)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE:
1 LSB = $(2^{-12})(V_{REF}) = \frac{1}{4096}(V_{REF})$

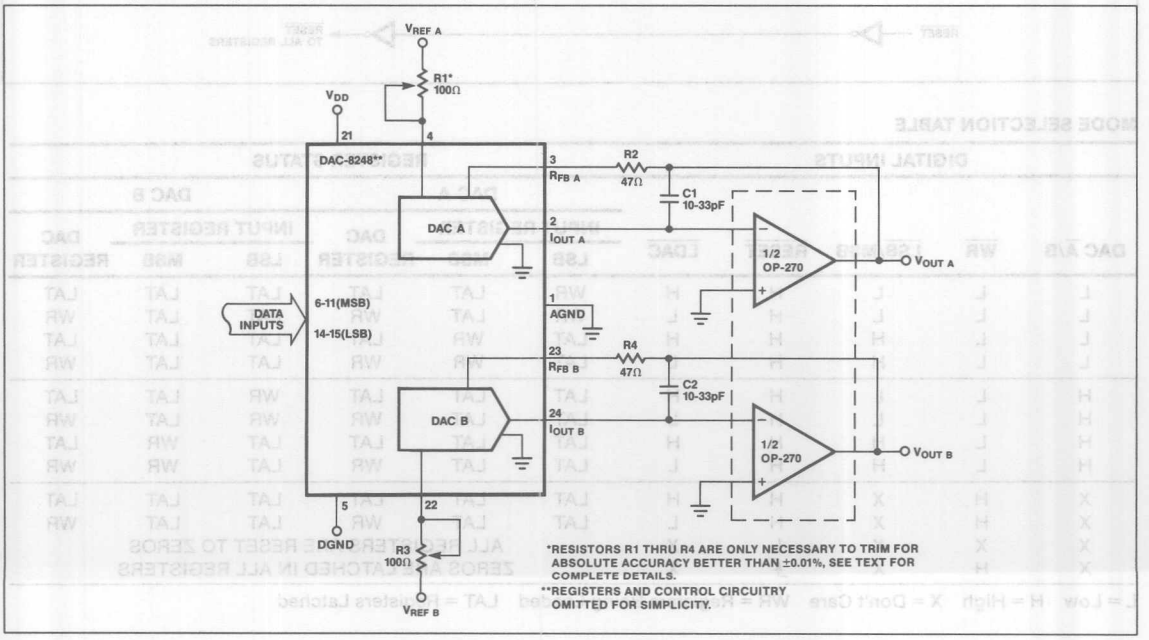
Low temperature-coefficient (approximately 50ppm/°C) resistors or trimmers should be used. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = \pm 10V$ is 0.024%, and 0.049% for the low grade. Capacitors C_1 and C_2 provide phase compensation to reduce overshoot and ringing when high-speed op amps are used.

Full-scale adjustment is achieved by loading the appropriate DAC's digital inputs with 1111 1111 1111 and adjusting R_1 (or R_3 for DAC B) so that:

$$V_{OUT} = V_{REF} \times \left(\frac{4095}{4096}\right)$$

Full-scale can also be adjusted by varying V_{REF} voltage and eliminating R_1, R_2, R_3, and R_4. Zero adjustment is performed by

FIGURE 7: *Unipolar Configuration (2-Quadrant Multiplication)*



loading the appropriate DAC's digital inputs with 0000 0000 0000 and adjusting the op amp's offset voltage to 0V. It is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244μV), and over the operating temperature range of interest. This will ensure the DAC's monotonicity and minimize gain and linearity errors.

BIPOLAR OPERATION

The bipolar (offset binary) 4-quadrant configuration using the DAC-8248 is shown in Figure 8, and the corresponding code is shown in Table 2. The circuit makes use of the OP-470, a quad op amp (use four OP-42s for applications requiring higher speeds).

The full-scale output voltage may be adjusted by varying V_{REF} or the value of R5 and R8, and thus eliminating resistors R1, R2, R3, and R4. If resistors R1 through R4 are omitted, then R5, R6, R7 (R8, R9, and R10 for DAC B) should be ratio-matched to 0.01% to keep gain error within data sheet specifications. The resistors should have identical temperature-coefficients if operating over the full temperature range.

Zero and full-scale are adjusted in one of two ways and are at the users discretion. Zero-output is adjusted by loading the appropriate DAC's digital inputs with 1000 0000 0000 and varying R1 (R3 for DAC B) so that $V_{OUT\,A}$ (or $V_{OUT\,B}$) equals 0V. If R1, R2 (R3, R4 for DAC B) are omitted, then zero output can be adjusted by varying R6, R7 ratios (R9, R10 for DAC B). Full-scale is adjusted by loading the appropriate DAC's digital inputs with 1111 1111 1111 and varying R5 (R8 for DAC B).

TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 8)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

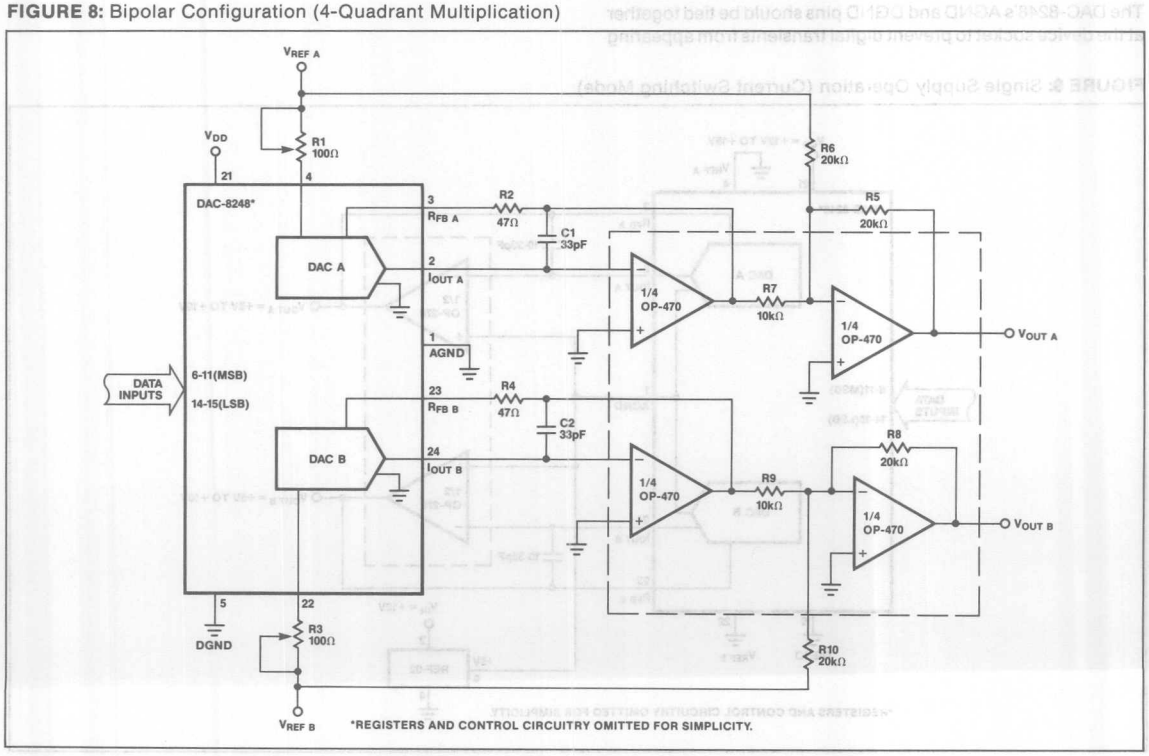
NOTE:
1 LSB = (2^{-11}) (V_{REF}) = $\frac{1}{2048}$ (V_{REF})

SINGLE SUPPLY OPERATION

CURRENT STEERING MODE

Because the DAC-8248's R-2R resistor ladder terminating resistor is internally connected to AGND, it lends itself well for single supply operation in the current steering mode configuration. This means that AGND can be raised above system

FIGURE 8: Bipolar Configuration (4-Quadrant Multiplication)



ground as shown in Figure 9. The output voltage will be between +5V and +10V depending on the digital input code. The output expression is given by:

$$V_{OUT} = V_{OS} + (D/4096)(V_{OS})$$

where V_{OS} = Offset Reference Voltage (+5V in Figure 9)
D = Decimal Equivalent of the Digital Input Word

VOLTAGE SWITCHING MODE

Figure 10 shows the DAC-8248 in another single supply configuration. The R-2R ladder is used in the voltage switching mode and functions as a voltage divider. The output voltage (at the V_{REF} pin) exhibits a constant impedance R (typically 11kΩ) and must be buffered by an op amp. The R_{FB} pins are not used and are left open. The reference input voltage must be maintained within +1.25V of AGND, and V_{DD} between +12V and +15V; this ensures that device accuracy is preserved.

The output voltage expression is given by:

$$V_{OUT} = V_{REF}\,(D/4096)$$

where D = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have a low impedance.

The DAC-8248's AGND and DGND pins should be tied together at the device socket to prevent digital transients from appearing at the analog output. This common point then becomes the single ground point connection. AGND and DGND is then brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

PC board ground plane can be used for the single point ground connection should the connections not be practical at the device socket. If neither of these connections are practical or allowed, then the device should be placed as close as possible to the systems single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC-8248 should be well filtered and regulated. Local supply decoupling consisting of a 1 to 10μF tantalum capacitor in parallel with a 0.1μF ceramic is highly recommended. The capacitors should be connected between the V_{DD} and DGND pins and at the device socket.

FIGURE 9: Single Supply Operation (Current Switching Mode)

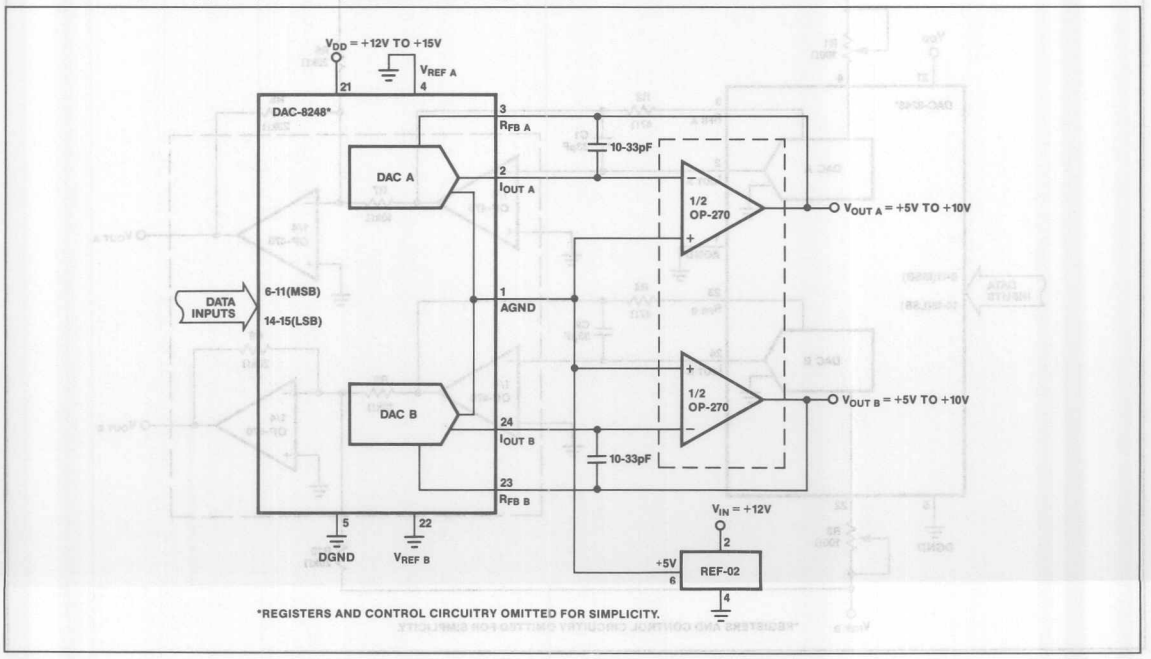
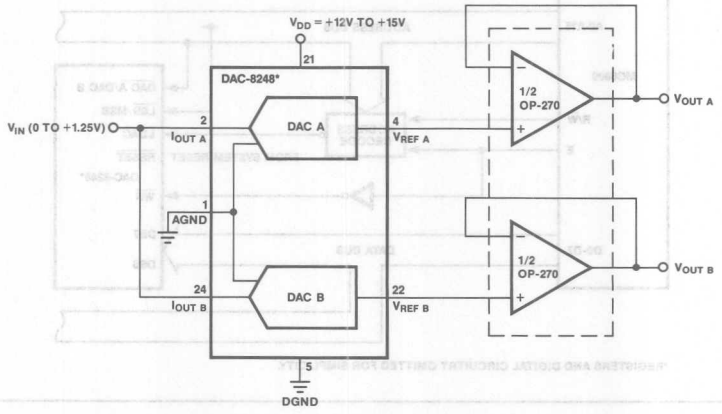


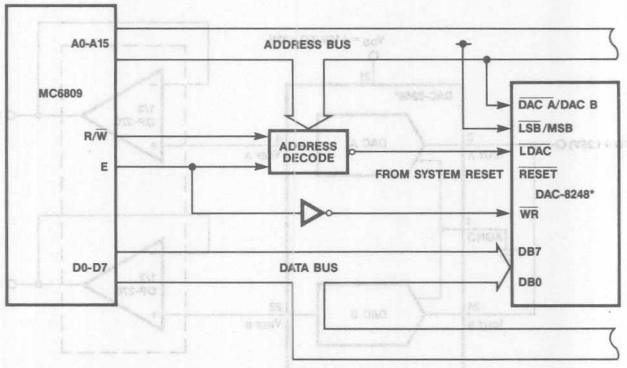
FIGURE 10: Single Supply Operation (Voltage Switching Mode)



*REGISTERS AND DIGITAL CIRCUITRY OMITTED FOR SIMPLICITY.

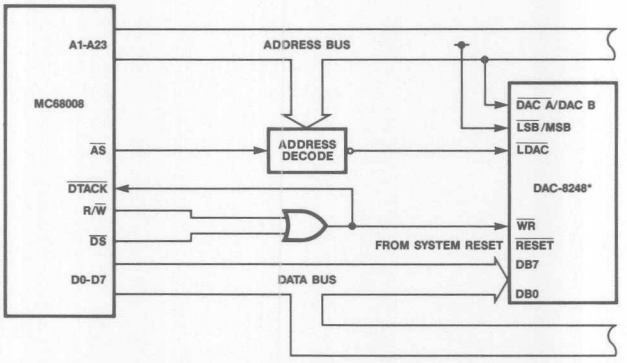
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FIGURE 12: DAC-8248 To MC6809 Interface



*REGISTERS AND DIGITAL CIRCUITRY OMITTED FOR SIMPLICITY.

FIGURE 13: DAC-8248 To MC68008 Interface



*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

DAC-8408

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28 Pin JEDEC Plastic Chip Carrier
- ±1/4 LSB End-Point Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5V)
- Low Power Consumption
- Latch-Up Resistant
- Available in Die Form

APPLICATIONS

- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multi-Channel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

ORDERING INFORMATION †

		PACKAGE		
			EXTENDED	
		COMMERCIAL	INDUSTRIAL	MILITARY*
		TEMPERATURE	TEMPERATURE	TEMPERATURE
INL	DNL	0°C to +70°C	−40°C to +85°C	−55°C to +125°C
±1/4LSB	±1/2LSB	DAC8408GP	DAC8408ET	DAC8408AT
±1/2LSB	±1LSB	–	DAC8408FT	DAC8408BT
±1/2LSB	±1LSB	–	DAC8408FPC††	–
±1/2LSB	±1LSB	–	DAC8408FS	–
±1/2LSB	±1LSB	–	DAC8408FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

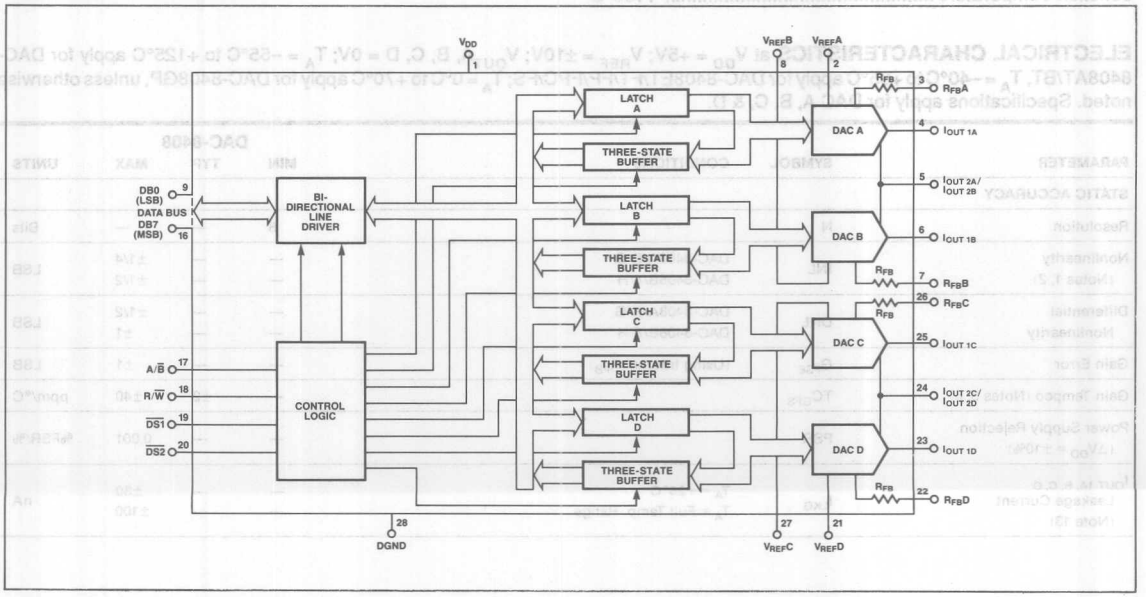
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The DAC-8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

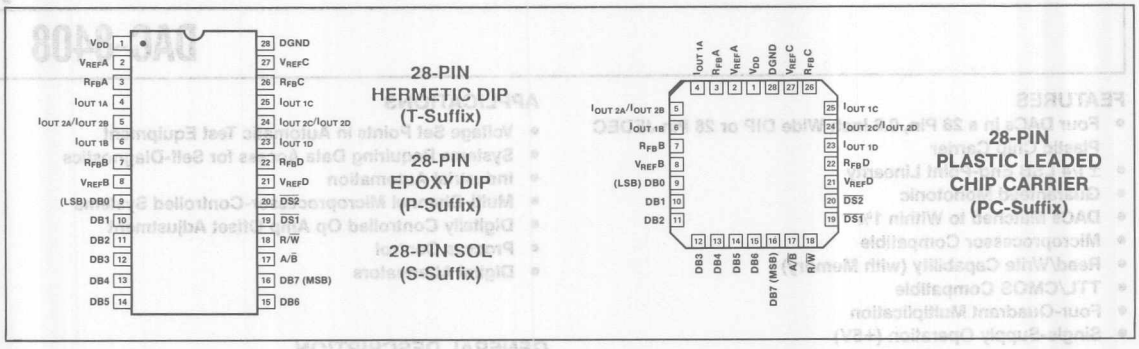
A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ determine which DAC will accept data. Data loading is similar to that of a RAM's write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The DAC-8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC-8408 operates on a single +5 volt supply and dissipates less than 20mW. The DAC-8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

FUNCTIONAL DIAGRAM



DAC-8408

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... 0, +7V
V_{DD} to DGND ..... 0, +7V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$,
$I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND ..... –0.3V to V_{DD} + 0.3V
$R_{FB}A$, $R_{FB}B$, $R_{FB}C$, $R_{FB}D$ to I_{OUT} ..... ±25V
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$,
$I_{OUT\ 2C}$, $I_{OUT\ 2D}$ to DGND .....–0.3V to V_{DD} + 0.3V
DB0 through DB7 to DGND .....–0.3V to V_{DD} + 0.3V
Control Logic
Input Voltage to DGND ..... –0.3V + V_{DD} + 0.3V
$V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ to
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... ±25V
Operating Temperature Range
Commercial Grade (GP) ..... 0°C to +70°C
Industrial Grade (ET, FT, FP, FPC, FS) ..... –40°C to +85°C
Military Grade (AT, BT) ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	55	10	°C/W
28-Pin Plastic DIP (P)	53	27	°C/W
28-Pin SOL (S)	68	23	°C/W
28-Contact PLCC (PC)	66	29	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} + 0.3V or less than –0.3V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Nonlinearity (Notes 1, 2)	INL	DAC-8408A/E/G	—	—	±1/4	LSB
		DAC-8408B/F/H	—	—	±1/2	
Differential Nonlinearity	DNL	DAC-8408A/E/G	—	—	±1/2	LSB
		DAC-8408B/F/H	—	—	±1	
Gain Error	G_{FSE}	(Using Internal R_{FB}	—	—	±1	LSB
Gain Tempco (Notes 3, 6)	TC_{GFS}		—	±2	±40	ppm/°C
Power Supply Rejection (ΔV_{DD} = ±10%)	PSR		—	—	0.001	%FSR/%
$I_{OUT\ 1A, B, C, D}$ Leakage Current (Note 13)	I_{LKG}	T_A = +25°C	—	—	±30	nA
		T_A = Full Temp. Range	—	—	±100	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Input Voltage Range			—	—	±20	V
Input Resistance Match (Note 4)		$R_{A, B, C, D}$	—	—	±1	%
Input Resistance	R_{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V_{IL}		—	—	0.8	V
Digital Input High	V_{IH}		2.4	—	—	V
Input Current (Note 5)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	±0.01 —	±1.0 ±10.0	µA
Input Capacitance (Note 6)	C_{IN}		—	—	8	pF
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	1.6mA Sink	—	—	0.4	V
Digital Output High	V_{OH}	400µA Source	4	—	—	V
Output Leakage Current	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	— —	±0.005 ±0.075	±1.0 ±10.0	µA
DAC OUTPUTS (Note 6)						
Propagation Delay (Note 7)	t_{pD}		—	150	180	ns
Settling Time (Notes 11, 12)	t_s		—	190	250	ns
Output Capacitance	C_{OUT}	DAC Latches All "0's" DAC Latches All "1's"	— —	— —	30 50	pF
AC Feedthrough	FT	($20V_{p-p}$ @ F = 100kHz)	54	—	—	dB
SWITCHING CHARACTERISTICS (Notes 6, 10)						
Write to Data Strobe Time	t_{DS1} or t_{DS2}	T_A = +25°C T_A = Full Temp. Range	90 145	— —	— —	ns
Data Valid to Strobe Set-Up Time	t_{DSU}	T_A = +25°C T_A = Full Temp. Range	150 175	— —	— —	ns
Data Valid to Strobe Hold Time	t_{DH}		10	—	—	ns
DAC Select to Strobe Set-Up Time	t_{AS}		0	—	—	ns
DAC Select to Strobe Hold Time	t_{AH}		0	—	—	ns
Write Select to Strobe Set-Up Time	t_{WSU}		0	—	—	ns
Write Select to Strobe Hold Time	t_{WH}		0	—	—	ns

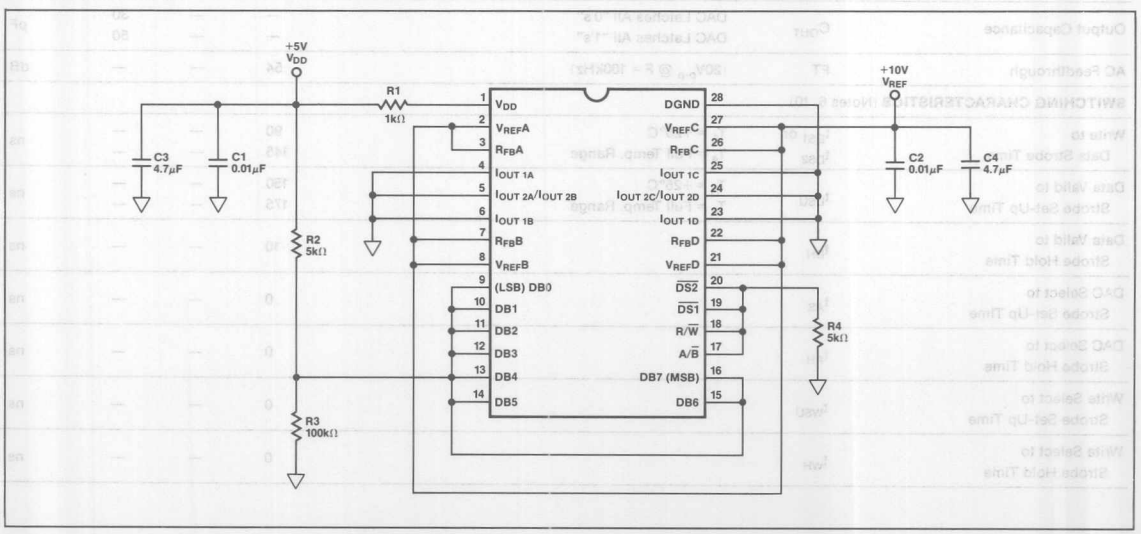
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noted. Specifications apply for DAC A, B, C, & D. *Continued*

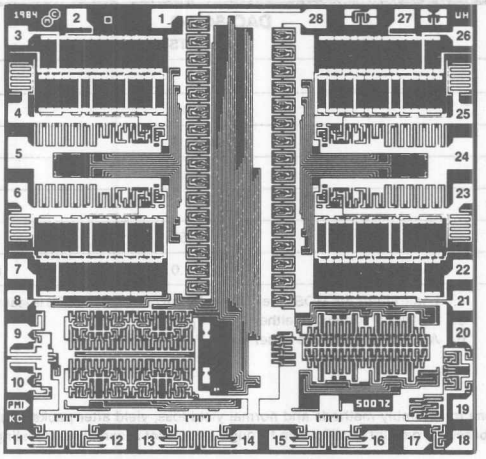
PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
Read to Data Strobe Width	t_{RDS}	$T_A = +25°C$	220	—	—	ns
		T_A = Full Temp. Range	350	—	—	
Data Strobe to Output Valid Time	t_{CO}	$T_A = +25°C$	320	—	—	ns
		T_A = Full Temp. Range	430	—	—	
Output Data to Deselect Time	t_{OTD}	$T_A = +25°C$	200	—	—	ns
		T_A = Full Temp. Range	270	—	—	
Read Select to Strobe Set-Up Time	t_{RSU}		0	—	—	ns
Read Select to Strobe Hold Time	t_{RH}		0	—	—	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	—	5.5	V
Supply Current (Note 8)	I_{DD}		—	—	50	μA
Supply Current (Note 9)	I_{DD}	$T_A = +25°C$	—	—	1.0	mA
		T_A = Full Temp. Range	—	—	1.5	

NOTES:
1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/°C of FSR (FSR = Full Scale Range = V_{REF} − 1 LSB.)
4. Input Resistance Temperature Coefficient = +300ppm/°C.
5. Logic Inputs are MOS gates. Typical input current at +25°C is less than 10nA.
6. Guaranteed by design.
7. From Digital Input to 90% of final analog output current.
8. All Digital Inputs "0" or V_{DD}.
9. All Digital Inputs V_{IH} or V_{IL}.
10. See Timing Diagram.
11. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
12. Extrapolated: t_s (1/2 LSB) = t_{pd} + 6.2τ where τ = the measured first time constant of the final RC decay.
13. All Digital Inputs = 0V; V_{REF} = +10V.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.130 × 0.124 inch, 16,120 sq. mils
(3.30 × 3.15 mm, 10.4 sq. mm)

1. V_{DD}
2. $V_{REF}A$
3. $R_{FB}A$
4. $I_{OUT\ 1A}$
5. $I_{OUT\ 2A}/I_{OUT\ 2B}$
6. $I_{OUT\ 1B}$
7. $R_{FB}B$
8. $V_{REF}B$
9. DB0 (LSB)
10. DB1
11. DB2
12. DB3
13. DB4
14. DB5
15. DB6
16. DB7 (MSB)
17. A/$\overline{B}$
18. R/$\overline{W}$
19. $\overline{DS1}$
20. $\overline{DS2}$
21. $V_{REF}D$
22. $R_{FB}D$
23. $I_{OUT\ 1D}$
24. $I_{OUT\ 2C}/I_{OUT\ 2D}$
25. $I_{OUT\ 1C}$
26. $R_{FB}C$
27. $V_{REF}C$
28. DGND

WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = +25°C, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Nonlinearity (Note 1)	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using Internal R_{FB}	±1	LSB MAX
Power Supply Rejection (ΔV_{DD} = ±10%) (Note 2)	PSR	Using Internal R_{FB}	0.001	%FSR/% MAX
$I_{OUT\ 1A, B, C, D}$ Leakage Current	I_{LKG}	All Digital Inputs = 0V V_{REF} = +10V	±30	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Note 3)	R_{IN}		6/14	kΩ MIN/MAX
Input Resistance Match	R_{IN}		±1	% MAX
DIGITAL INPUTS				
Digital Input Low	V_{IL}		0.8	V MAX
Digital Input High	V_{IH}		2.4	V MIN
Input Current (Note 4)	I_{IN}		±1.0	μA MAX

WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = +25°C, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

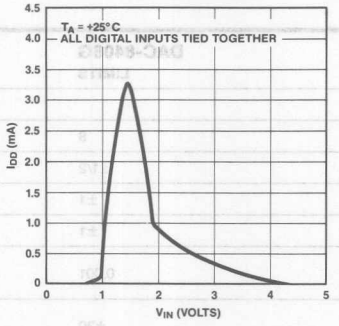
PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
DATA BUS OUTPUTS				
Digital Output Low	V_{OL}	1.6mA Sink	0.4	V MAX
Digital Output High	V_{OH}	400μA Source	4	V MIN
Output Leakage Current	I_{LKG}		±1.0	μA MAX
POWER SUPPLY				
Supply Current (Note 5)	I_{DD}		50	μA MAX
Supply Current (Note 6)	I_{DD}		1.0	mA MAX

NOTES:
1. This is an endpoint linearity specification.
2. FSR is Full Scale Range = V_{REF} − 1 LSB.
3. Input Resistance Temperature Coefficient approximately equals +300ppm/°C.
4. Logic inputs are MOS gates. Typical input current at +25°C is less than 10nA.
5. All Digital Inputs are either "0" or V_{DD}.
6. All Digital Inputs are either V_{IH} or V_{IL}.

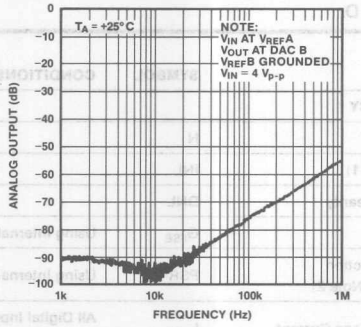
Electrical tests are performed at wafer probe to the limits shown, Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

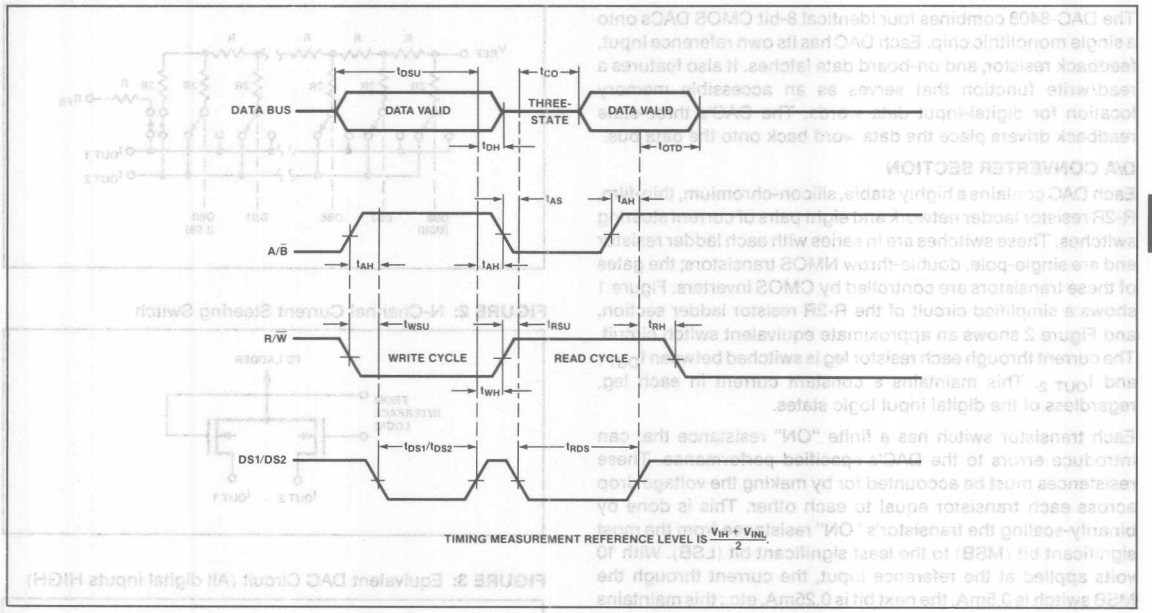
SUPPLY CURRENT vs LOGIC LEVEL



ANALOG CROSSTALK vs FREQUENCY



TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION

Resolution is the number of states (2^n) that the full-scale range (FSR) of a DAC is divided (or resolved) into.

NONLINEARITY

Nonlinearity (Relative Accuracy) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in LSB, %, or ppm of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1LSB step size. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain Error (full-scale error) is a measure of the output error between the ideal and actual DAC output. The ideal full-scale output is V_{REF} – 1 LSB.

OUTPUT CAPACITANCE

Output Capacitance is that capacitance between $I_{OUT\ 1A}$, $I_{OUT\ 1B}$, $I_{OUT\ 1C}$, or $I_{OUT\ 1D}$ and AGND.

AC FEEDTHROUGH ERROR

This is the error caused by capacitance coupling from V_{REF} to the DAC output with all switches off.

SETTLING TIME

Settling Time is the time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input signal.

PROPAGATION DELAY

This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output-current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

This is the portion of input signal that appears at the output of a DAC from another DAC's reference input. It is expressed as a ratio in dB.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch energy transferred to the output of one DAC due to a change in digital input code from other DACs. It is specified in nVs.

CIRCUIT INFORMATION

The DAC-8408 combines four identical 8-bit CMOS DACs onto a single monolithic chip. Each DAC has its own reference input, feedback resistor, and on-board data latches. It also features a read/write function that serves as an accessible memory location for digital-input data words. The DAC's three-state readback drivers place the data word back onto the data bus.

D/A CONVERTER SECTION

Each DAC contains a highly stable, silicon-chromium, thin-film, R-2R resistor ladder network and eight pairs of current steering switches. These switches are in series with each ladder resistor and are single-pole, double-throw NMOS transistors; the gates of these transistors are controlled by CMOS inverters. Figure 1 shows a simplified circuit of the R-2R resistor ladder section, and Figure 2 shows an approximate equivalent switch circuit. The current through each resistor leg is switched between $I_{OUT\,1}$ and $I_{OUT\,2}$. This maintains a constant current in each leg, regardless of the digital input logic states.

Each transistor switch has a finite "ON" resistance that can introduce errors to the DAC's specified performance. These resistances must be accounted for by making the voltage drop across each transistor equal to each other. This is done by binarily-scaling the transistor's "ON" resistance from the most significant bit (MSB) to the least significant bit (LSB). With 10 volts applied at the reference input, the current through the MSB switch is 0.5mA, the next bit is 0.25mA, etc.; this maintains a constant 10mV drop across each switch and the converter's accuracy is maintained. It also results in a constant resistance appearing at the DAC's reference input terminal; this allows the DAC to be driven by a voltage or current source, AC or DC of positive or negative polarity.

Shown in Figure 3 is an equivalent output circuit for DAC A. The circuit is shown with all digital inputs high. The leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder terminating resistor. The situation is reversed with all digital inputs low, as shown in Figure 4. The output capacitance is code dependent, and therefore, is modulated between the low and high values.

FIGURE 1: Simplified D/A Circuit of DAC-8408

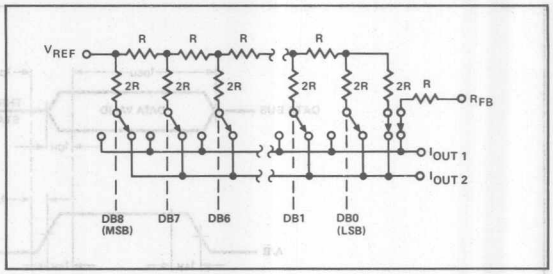


FIGURE 2: N-Channel Current Steering Switch

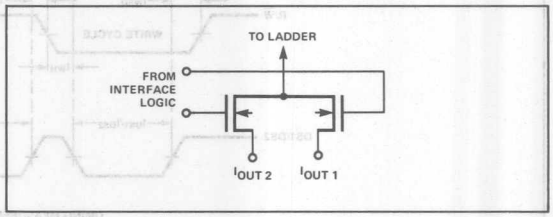


FIGURE 3: Equivalent DAC Circuit (All digital inputs HIGH)

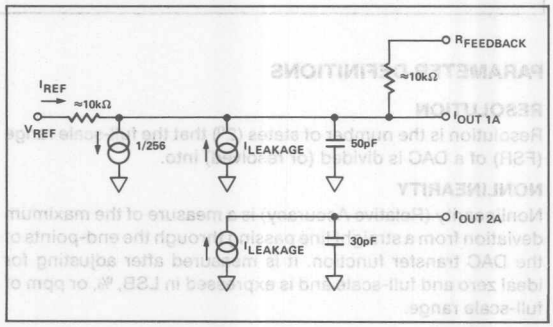
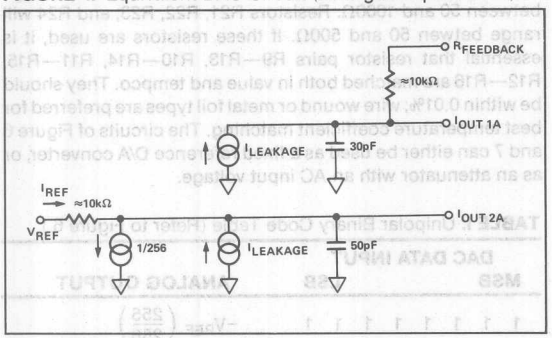


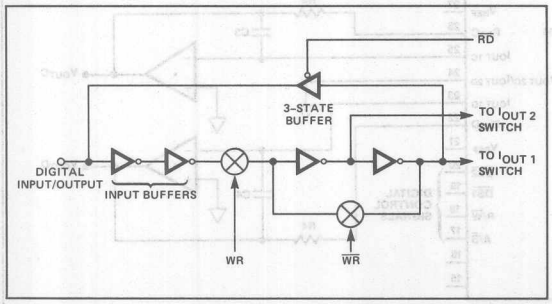
FIGURE 4: Equivalent DAC Circuit (All digital inputs LOW)



DIGITAL SECTION

Figure 5 shows the digital input/output structure for one bit. The digital WR, $\overline{WR}$, and $\overline{RD}$ controls shown in the figure are internally generated from the external A/$\overline{B}$, R/$\overline{W}$, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4V and 0.8V) are converted into CMOS logic levels. When the digital input is in the region of 1.2 to 1.8V, the input stages operate in their linear region and draw current from the +5V supply (see Typical Supply Current vs Logic Level curve on page 6). It is recommended that the digital input voltages be as close to V_{DD} and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three-state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three-state digital readback leakage-current is typically 5nA.

FIGURE 5: Digital Input/Output Structure



INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACs A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection: Control inputs, $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection: Control inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC.

Write Mode: When the control inputs $\overline{DS}$ and R/$\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0—DB7.

Hold Mode: The selected DAC latch retains the data that was present on the bus line just prior to $\overline{DS}$ or R/$\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

MODE SELECTION TABLE

CONTROL LOGIC					
DS1	DS2	A/$\overline{B}$	R/$\overline{W}$	MODE	DAC
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A&C
L	L	L	L	WRITE	B&D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE H = HIGH STATE X = IRRELEVANT

BASIC APPLICATIONS

Some basic circuit configurations are shown in Figures 6 and 7. Figure 6 shows the DAC-8408 connected in a unipolar configuration (2-Quadrant Multiplication), and Table I shows the Code Table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = $V_{REF} - 1\ LSB = V_{REF}(1-2^{-8})$ or $V_{REF} \times (255/256)$ with all digital inputs high. Low temperature coefficient (approximately 50ppm/°C) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are not required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code-dependent. This produces a code-dependent, differential nonlinearity term at the amplifier's output which can have a maximum value of 0.67 × the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential-nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (1 LSB = $2^{-8} \times V_{REF}$ or $1/256 \times V_{REF}$), or less than 3.9mV over the operating temperature range. Zero-scale output voltage (with all digital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C3, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

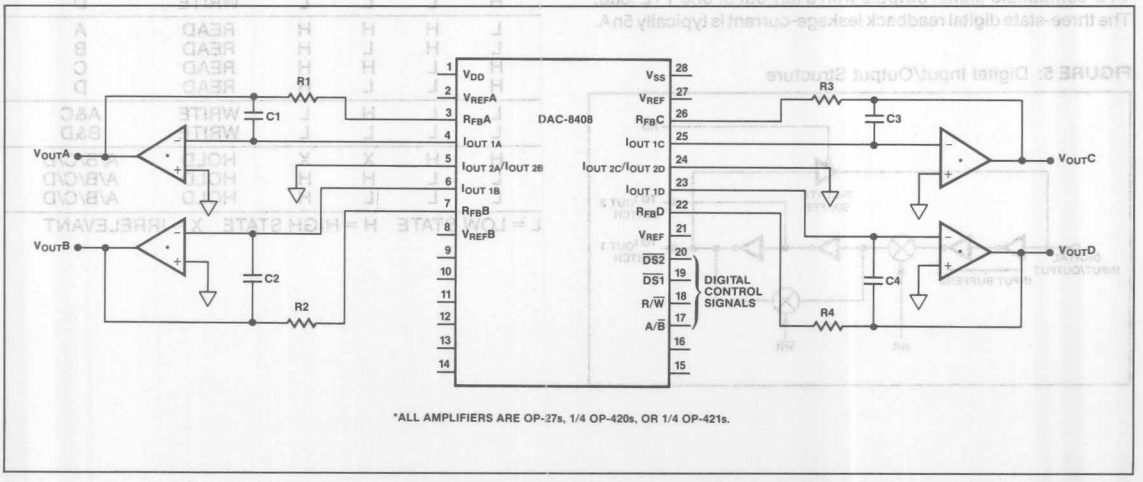
Figure 7 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table II shows the Code Table. Trimmer resistors R17, R18, R19, and R20 are used only if gain error adjustments are required and range between 50 and 1000Ω. Resistors R21, R22, R23, and R24 will range betwen 50 and 500Ω. If these resistors are used, it is essential that resistor pairs R9—R13, R10—R14, R11—R15, R12—R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 6 and 7 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage.

TABLE I: Unipolar Binary Code Table (Refer to Figure 6.)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = \frac{-V_{IN}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTE:
1 LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

FIGURE 6: Quad DAC Unipolar Operation (2-Quadrant Multiplication)



*ALL AMPLIFIERS ARE OP-27s, 1/4 OP-420s, OR 1/4 OP-421s.

FIGURE 7: Quad DAC Bipolar Operation (4-Quadrant Multiplication)

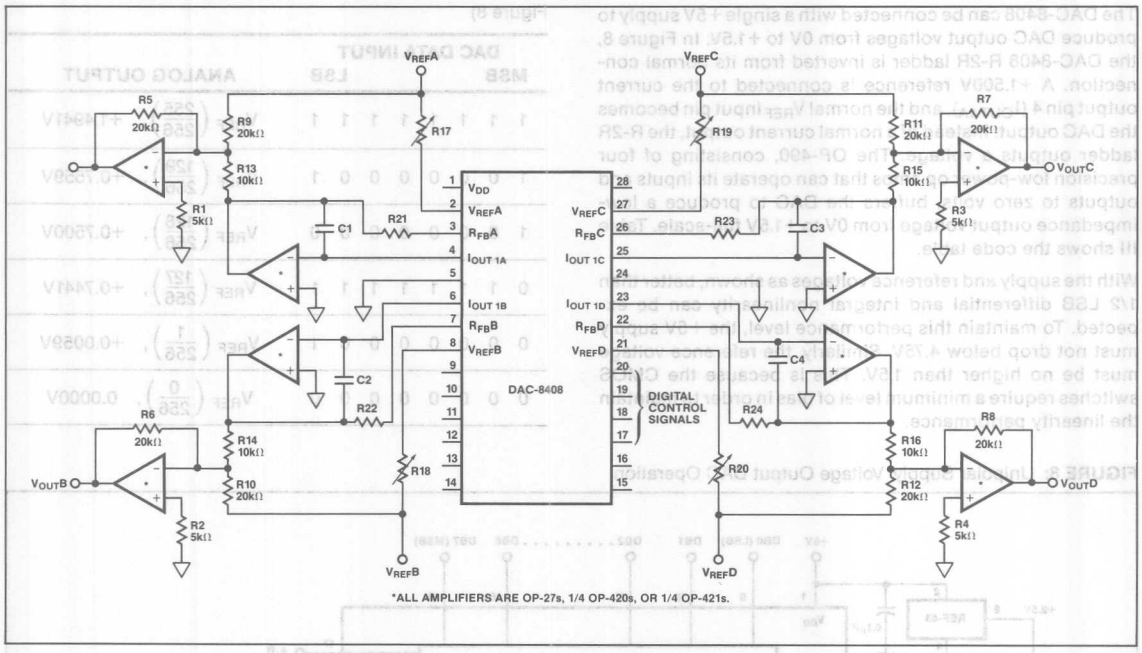


TABLE II: Bipolar (Offset Binary) Code Table (Refer to Figure 7.)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT (DAC A OR DAC B)
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right)$

NOTE:
1 LSB = (2^{-7}) $(V_{REF}) = \frac{1}{128}$ (V_{REF})

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can appear as noise at the DAC-8408's analog output. Note that in Figures 5 and 6, $I_{OUT\ 2A}/I_{OUT\ 2B}$ and $I_{OUT\ 2C}/I_{OUT\ 2D}$ are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the DAC-8408 socket. In systems where AGND and DGND are tied together on the backplane, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing: During the period when both $\overline{DS}$ and R/$\overline{W}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the R/$\overline{W}$ should not go low until the data bus is fully settled (DATA VALID).

produce DAC output voltages from 0V to +1.5V. In Figure 8, the DAC-8408 R-2R ladder is inverted from its normal connection. A +1.500V reference is connected to the current output pin 4 ($I_{OUT\,1A}$), and the normal V_{REF} input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low-power op amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low-impedance output voltage from 0V to +1.5V full-scale. Table III shows the code table.

With the supply and reference voltages as shown, better than 1/2 LSB differential and integral nonlinearity can be expected. To maintain this performance level, the +5V supply must not drop below 4.75V. Similarly, the reference voltage must be no higher than 1.5V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$V_{REF}\left(\frac{255}{256}\right)$, +1.4941V
1	0	0	0	0	0	0	1	$V_{REF}\left(\frac{129}{256}\right)$, +0.7559V
1	0	0	0	0	0	0	0	$V_{REF}\left(\frac{128}{256}\right)$, +0.7500V
0	1	1	1	1	1	1	1	$V_{REF}\left(\frac{127}{256}\right)$, +0.7441V
0	0	0	0	0	0	0	1	$V_{REF}\left(\frac{1}{256}\right)$, +0.0059V
0	0	0	0	0	0	0	0	$V_{REF}\left(\frac{0}{256}\right)$, 0.0000V

FIGURE 8: Unipolar Supply, Voltage Output DAC Operation

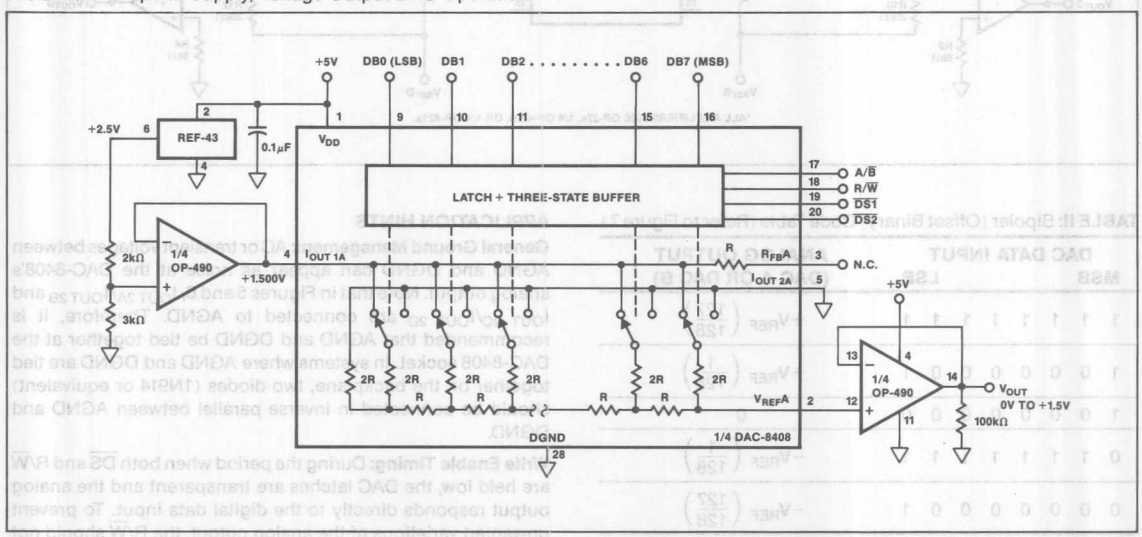
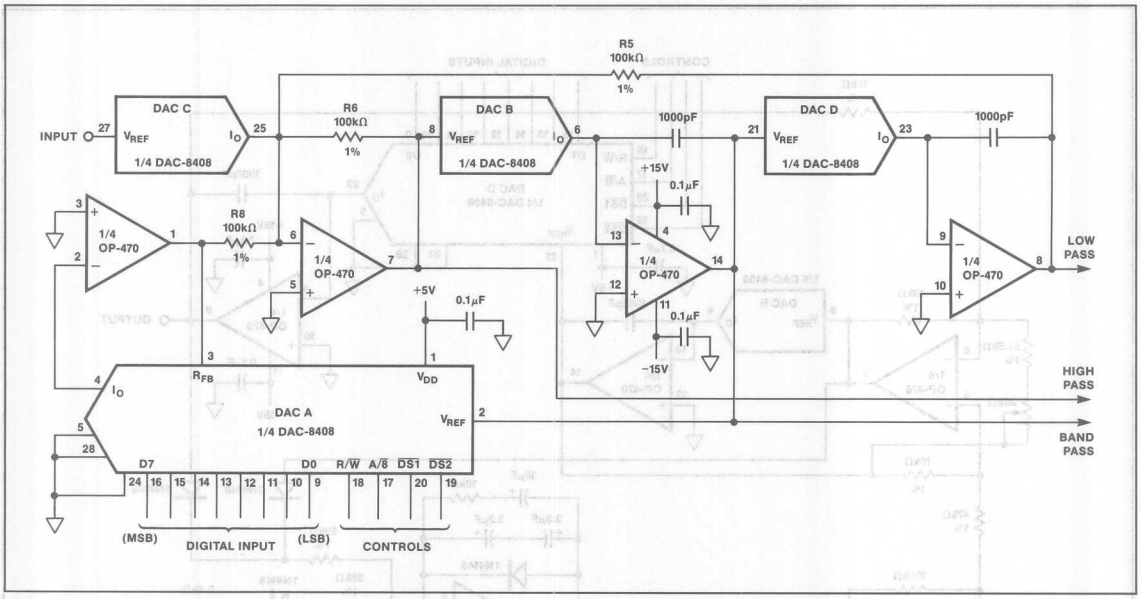


FIGURE 9: A Digitally Programmable Universal Active Filter

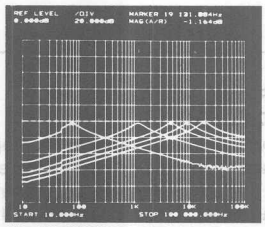


A DIGITALLY PROGRAMMABLE ACTIVE FILTER

A powerful D/A converter application is a programmable active filter design as shown in Figure 9. The design is based on the state-variable filter topology which offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load which sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is also true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

The network analyzer photo shown in Figure 10 superimposes five actual bandpass responses ranging from the lowest frequency of 75Hz (1 LSB ON) to a full-scale frequency of 19.132kHz (all bits ON), which is equivalent to a 256 to 1 dynamic range. The frequency is determined by $f_c = 1/2\pi RC$ where R is the ladder resistance (R_{IN}) of the DAC -8408, and C is 1000pF. Note that from device to device, the resistance R_{IN} varies. Thus some tuning may be necessary.

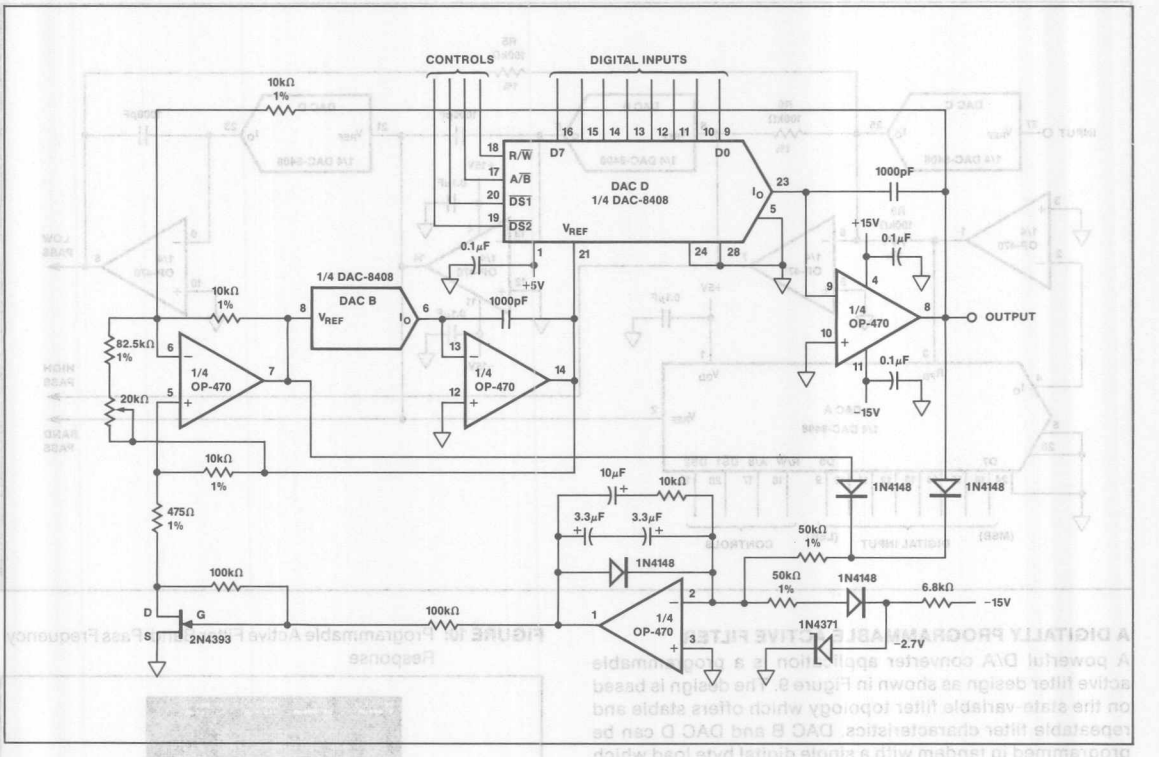
FIGURE 10: Programmable Active Filter Band-Pass Frequency Response



THE CIRCUIT PROVIDES FULL 8-BIT (> 2 DECADE) DYNAMIC RANGE OF FREQUENCY CONTROL

All components used are available off-the-shelf. Using low drift thin-film resistors, the DAC-8408 exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP-470's low input offset voltage assures an unusually low DC offset at the filter output.

FIGURE 11: A Digitally Programmable, Low-Distortion Sinewave Oscillator



A LOW-DISTORTION, PROGRAMMABLE SINEWAVE OSCILLATOR

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 11. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $f_c = 1/2\pi RC$. Positive feedback is accomplished via the 82.5kΩ and the 20kΩ potentiometer. The Q of the oscillator is determined by the ratio of 10kΩ and 475Ω in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave amplitude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%.

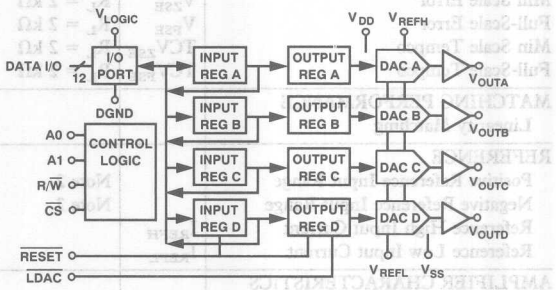
Quad, 12-Bit DAC Voltage Output with Readback

DAC-8412/DAC-8413

FEATURES
- +5 to ±15 Volt Operation
- Unipolar or Bipolar Operation
- True Voltage Output
- Double-Buffered Inputs
- Reset to Min or Center Scale
- Fast Bus Access Time
- Readback

APPLICATIONS
- Automatic Test Equipment
- Digitally Controlled Calibration
- Servo Controls
- Process Control Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8412 and DAC-8413 are quad, 12-bit, voltage output DACs with readback capability. Built using a complementary BiCMOS process, these monolithic DACs offer the user very high package density.

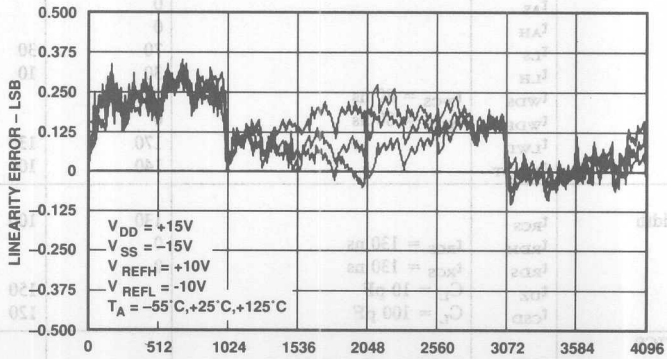
Output voltage swing is set by the two reference inputs V_{REFH} and V_{REFL}. By setting the V_{REFL} input to 0 volts and V_{REFH} to a positive voltage, the DAC will provide a unipolar positive output range. A similar configuration with V_{REFH} at 0 volts and V_{REFL} at a negative voltage will provide a unipolar negative output range. Bipolar outputs are configured by connecting both V_{REFH} and V_{REFL} to nonzero voltages. This method of setting output voltage range has advantages over other bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

Digital controls allow the user to load or read back data from any DAC, load any DAC and transfer data to all DACs at one time.

An active low $\overline{\text{RESET}}$ loads all DAC output registers to mid-scale for the DAC-8412 and zero scale for the DAC-8413.

The DAC-8412/DAC-8413 are available in 28-pin plastic DIP, cerdip, PLCC and LCC packages. They can be operated from a wide variety of supply and reference voltages with supplies ranging from single +5 volt to ±15 volts, and references from +2.5 to ±10 volts. Power dissipation is less than 330 mW with ±15 volt supplies and only 60 mW with a +5 volt supply.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC-8412/DAC-8413/883 data sheet which specifies operation over the −55°C to +125°C temperature range.



INL VS. CODE OVER TEMPERATURE

DAC-8412/DAC-8413—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +15.0 V, V_{SS} = −15.0 V, V_{LOGIC} = +5.0 V, V_{REFH} = +10.0 V, V_{REFL} = −10.0 V, −40°C ≤ T_A ≤ +85°C unless otherwise specified. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL			0.25	±0.5	LSB
Integral Linearity "F"	INL				±1	LSB
Differential Linearity	DNL	Monotonic Over Temperature	−1			LSB
Min Scale Error	V_{ZSE}	R_L = 2 kΩ			±2	LSB
Full-Scale Error	V_{FSE}	R_L = 2 kΩ			±2	LSB
Min Scale Tempco	TCV_{ZSE}	R_L = 2 kΩ		15		ppm/°C
Full-Scale Tempco	TCV_{FSE}	R_L = 2 kΩ		20		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 2	V_{REFL} + 2.5		V_{DD} − 2.5	V
Negative Reference Input Range		Note 2	−10		V_{REFH} − 2.5	V
Reference High Input Current	I_{REFH}		−2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		0	+2	+2.75	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−5		+5	mA
Settling Time	t_S	to 0.01%		6		µsec
Slew Rate	SR	10% to 90%		2.2		V/µsec
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Output High Voltage	V_{OH}	I_{OH} = +0.4 mA	2.4			V
Logic Output Low Voltage	V_{OL}	I_{OL} = −1.6 mA			0.4	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
Crosstalk				>72		dB
Large Signal Bandwidth		−3 dB, V_{REFH} = 0 to +10 V p-p		160		kHz
LOGIC TIMING CHARACTERISTICS		Note 3				
WRITE						
Chip Select Write Pulse Width	t_{WCS}		80	40		ns
Write Setup	t_{WS}	t_{WCS} = 80 ns	0			ns
Write Hold	t_{WH}	t_{WCS} = 80 ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70	30		ns
Load Hold	t_{LH}		30	10		ns
Write Data Setup	t_{WDS}	t_{WCS} = 80 ns	20			ns
Write Data Hold	t_{WDH}	t_{WCS} = 80 ns	0			ns
Load Pulse Width	t_{LWD}		170	130		ns
Reset Pulse Width	t_{RESET}		140	100		ns
READ						
Chip Select Read Pulse Width	t_{RCS}		130	100		ns
Read Data Hold	t_{RDH}	t_{RCS} = 130 ns	0			ns
Read Data Setup	t_{RDS}	t_{RCS} = 130 ns	0			ns
Data to Hi Z	t_{DZ}	C_L = 10 pF		150		ns
Chip Select to Data	t_{CSD}	C_L = 100 pF		120	160	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	14.25 V≤V_{DD}≤15.75 V			150	ppm/V
Positive Supply Current	I_{DD}	V_{REFH} = +2.5 V		8.5	12	mA
Negative Supply Current	I_{SS}		−10	−6.5		mA
Power Dissipation	P_{DISS}				330	mW

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.

[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[3]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

(@ $V_{DD} = V_{LOGIC} = +5.0$ V ±5%, $V_{SS} = 0.0$ V, $V_{REFH} = 2.5$ V, $V_{REFL} = 0.0$ V, and $V_{SS} = -5.0$ V ±5%, $V_{REFL} = -2.5$ V, $-40°C \le T_A \le +85°C$ unless otherwise specified. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL			1/2	±1	LSB
Integral Linearity "F"	INL				±2	LSB
Integral Linearity "E"	INL	$V_{SS} = 0.0$ V; Note 2			±2	LSB
Integral Linearity "F"	INL	$V_{SS} = 0.0$ V; Note 2			±4	LSB
Differential Linearity	DNL	Monotonic Over Temp	−1			LSB
Min Scale Error	V_{ZSE}	$V_{SS} = -5.0$ V			±4	LSB
Full-Scale Error	V_{FSE}	$V_{SS} = -5.0$ V			±4	LSB
Min Scale Error	V_{ZSE}	$V_{SS} = 0.0$ V			±8	LSB
Full-Scale Error	V_{FSE}	$V_{SS} = 0.0$ V			±8	LSB
Min Scale Tempco	TCV_{ZSE}			100		ppm/°C
Full-Scale Tempco	TCV_{FSE}			100		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 3	$V_{REFL} + 2.5$		$V_{DD} - 2.5$	V
Negative Reference Input Range		$V_{SS} = 0.0$ V	0		$V_{REFH} - 2.5$	V
Negative Reference Input Range		$V_{SS} = -5.0$ V	−2.5		$V_{REFH} - 2.5$	V
Reference High Input Current	I_{REFH}	Code 000H	−1.0		+1.0	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−1.25		+1.25	mA
Settling Time	t_S	to 0.01%		6		µs
Slew Rate	SR	10% to 90%		2.2		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	$T_A = +25°C$	2.4			V
Logic Input Low Voltage	V_{INL}	$T_A = +25°C$			0.8	V
Logic Output High Voltage	V_{OH}	$I_{OH} = +0.4$ mA	2.4			V
Logic Output Low Voltage	V_{OL}	$I_{OL} = -1.6$ mA			0.45	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
LOGIC TIMING CHARACTERISTICS		Note 4				
WRITE						
Chip Select Write Pulse Width	t_{WCS}		150	90		ns
Write Setup	t_{WS}	$t_{WCS} = 150$ ns	0			ns
Write Hold	t_{WH}	$t_{WCS} = 150$ ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70	30		ns
Load Hold	t_{LH}		50	20		ns
Write Data Setup	t_{WDS}	$t_{WCS} = 150$ ns	20			ns
Write Data Hold	t_{WDH}	$t_{WCS} = 150$ ns	0			ns
Load Pulse Width	t_{LWD}		180	130		ns
Reset Pulse Width	t_{RESET}		150	110		ns
READ						
Chip Select Read Pulse Width	t_{RCS}		170	120		ns
Read Data Hold	t_{RDH}	$t_{RCS} = 170$ ns	20			ns
Read Data Setup	t_{RDS}	$t_{RCS} = 170$ ns	0			ns
Data to Hi Z	t_{DZ}	$C_L = 10$ pF		200		ns
Chip Select to Data	t_{CSD}	$C_L = 100$ pF		220	320	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS			100		ppm/V
Positive Supply Current	I_{DD}			7	12	mA
Negative Supply Current	I_{SS}	$V_{SS} = -5.0$ V	−10			mA

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with $V_{DD} = +4.75$ V.

[2]For single supply operation only ($V_{REFL} = 0.0$ V, $V_{SS} = 0.0$ V): Due to internal offset errors, INL and DNL are measured beginning at code 2 (002_H).

[3]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[4]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = +15.0 V, V_{SS} = −15.0 V, V_{LOGIC} = +5.0 V, V_{REFH} = +10.0 V, V_{REFL} = −10.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	DAC-8412GBC DAC-8413GBC Limit	Units
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Min Scale Offset	V_{ZSE}		±1	LSB max
Full-Scale Offset	V_{FSE}		±1	LSB max
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}		1	µA max
Logic Output High Voltage	V_{OH}	I_{OH} = +0.4 mA	2.4	V min
Logic Output Low Voltage	V_{OL}	I_{OL} = −1.6 mA	0.4	V max
Positive Supply Current	I_{DD}	V_{REFH} = +2.5 V	12	mA max
Negative Supply Current	I_{SS}		−10	mA min

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

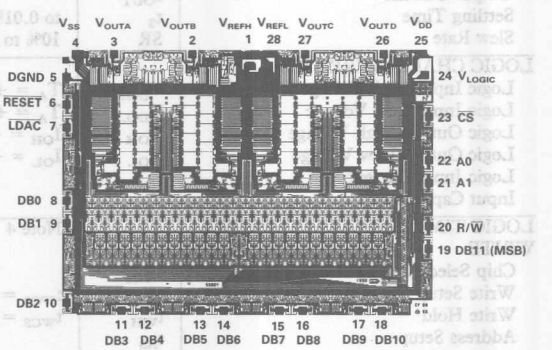
V_{SS} to V_{DD} . . . . . −0.3 V, +33.0 V
V_{SS} to V_{LOGIC} . . . . . −0.3 V, +33.0 V
V_{LOGIC} to DGND . . . . . −0.3 V, +18.0 V
V_{SS} to V_{REFL} . . . . . −0.3 V, +V_{SS}−2.0 V
V_{REFH} to V_{DD} . . . . . +2.0 V, +33.0 V
V_{REFH} to V_{REFL} . . . . . +2.0 V, V_{SS}−V_{DD}
Current into Any Pin[4] . . . . . ±15 mA
Digital Input Voltage to DGND . . . . −0.3 V, V_{LOGIC} +0.3 V
Digital Output Voltage to DGND . . . . . −0.3 V, +7.0 V
Operating Temperature Range
ET, FT, EP, FP, FPC, FTC . . . . . −40°C to +85°C
AT, BT, BTC . . . . . −55°C to +125°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation Package . . . . . 1000 mW
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Units
28-Pin Hermetic DIP (T)	50	7	°C/W
28-Pin Plastic DIP (P)	48	22	°C/W
28-Lead Hermetic Leadless Chip Carrier (TC)	70	28	°C/W
28-Lead Plastic Leaded Chip Carrier (PC)	63	25	°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket.

DICE CHARACTERISTICS



DIE SIZE 0.225 × 0.165 INCH, 37,125 SQ. MILS
(5.715 × 4.191 mm, 23.95 sq. mm)

DIE SUBSTRATE IS CONNECTED TO V_{DD}

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog outputs are protected from short circuit to ground or either supply.



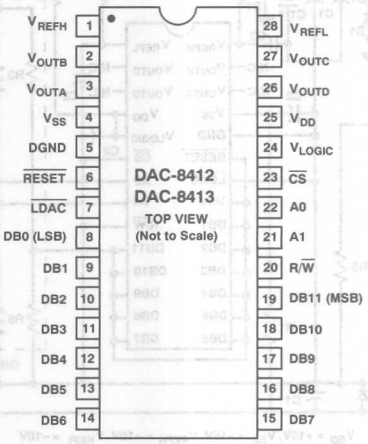
ORDERING INFORMATION*

INL (LSB)	Military† Temperature −55°C to +125°C	Extended Industrial† Temperature −40°C to +85°C	Package
±1		DAC8412FPC	PLCC
±1		DAC8412FTC	LCC
±1.5	DAC8412BTC/883		LCC
±0.5		DAC8412ET	Cerdip
±0.75	DAC8412AT/883		Cerdip
±1		DAC8412FT	Cerdip
±1.5	DAC8412BT/883		Cerdip
±0.5		DAC8412EP	Plastic
±1		DAC8412FP	Plastic
±1		DAC8412GBC	Dice
±1		DAC8413FPC	PLCC
±1		DAC8413FTC	LCC
±1.5	DAC8413BTC/883		LCC
±0.5		DAC8413ET	Cerdip
±0.75	DAC8413AT/883		Cerdip
±1		DAC8413FT	Cerdip
±1.5	DAC8413BT/883		Cerdip
±0.5		DAC8413EP	Plastic
±1		DAC8413FP	Plastic
±1		DAC8413GBC	Dice

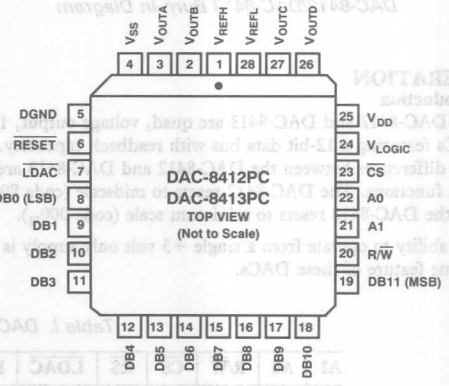
*Burn-in is available on extended industrial temperature range parts in cerdip and LCC packages. For ordering information, see databook.
†A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.

PIN CONFIGURATIONS

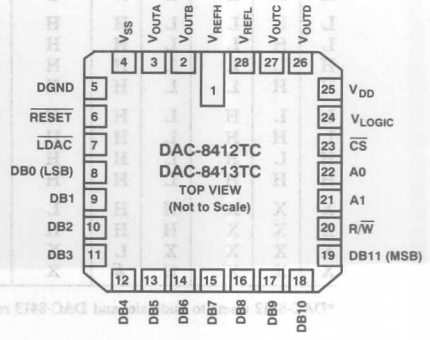
DIP Pinout

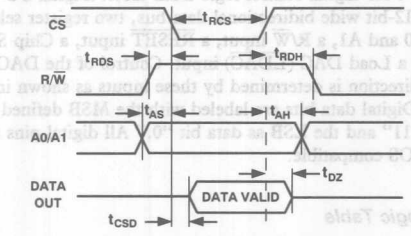


PLCC Pinout

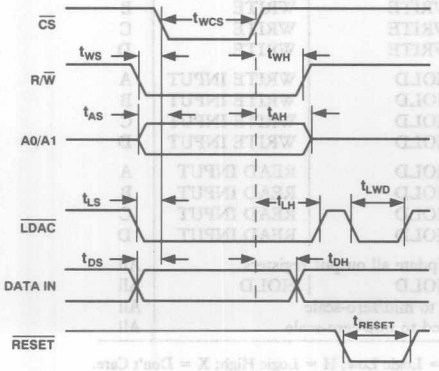


LCC Pinout

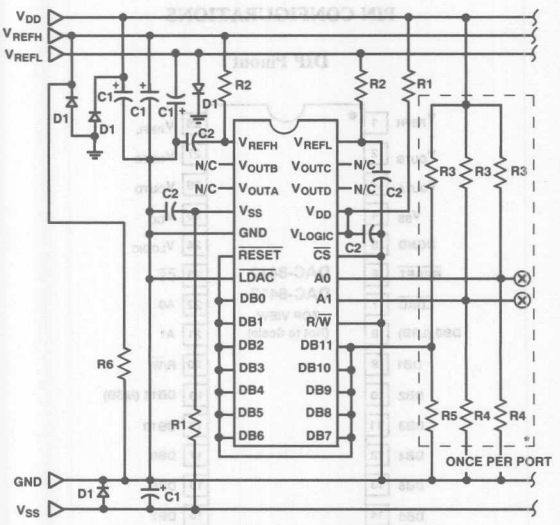




Data Output (Read) Timing



Data WRITE (Input and Output Registers) Timing



V_{DD} = +15V, V_{SS} = −15V, V_{REFH} = +10V, V_{REFL} = −10V
R1 = 10Ω, R2 = 100Ω, R3 = 5kΩ, R4 = 10kΩ, R5 = 100kΩ,
R6 = 47Ω for LCC, R6 = 100Ω for DIP
C1 = 4.7 µF (ONCE PER PORT), C2 = 0.01µF (EACH DEVICE)
D1 = 1N4001 OR EQUIVALENT (ONCE PER PORT)

DAC-8412/DAC-8413 Burn-In Diagram

OPERATION

Introduction

The DAC-8412 and DAC-8413 are quad, voltage output, 12-bit DACs featuring a 12-bit data bus with readback capability. The only differences between the DAC-8412 and DAC-8413 are the reset functions. The DAC-8412 resets to midscale (code 800_H) and the DAC-8413 resets to minimum scale (code 000_H).

The ability to operate from a single +5 volt only supply is a unique feature of these DACs.

Operation of the DAC-8412 and DAC-8413 can be viewed by dividing the system into three separate functional groups: the digital I/O and logic, the digital to analog converters and the output amplifiers.

DACs

Each DAC is a voltage switched, high impedance (R = 50 kΩ), R-2R ladder configuration. Each 2R resistor is driven by a pair of switches that connect the resistor to either V_{REFH} or V_{REFL}.

Reference Inputs

All four DACs share common reference high (V_{REFH}) and reference low (V_{REFL}) inputs. The voltages applied to these reference inputs set the output high and low voltage limits of all four of the DACs. Each reference input has voltage restrictions with respect to the other reference and to the power supplies. The V_{REFL} can be set at any voltage between V_{SS} and V_{REFH} − 2.5 volts, and V_{REFH} can be set to any value between $+V_{DD}$ − 2.5 volts and V_{REFL} + 2.5 volts. Note that because of these restrictions the DAC-8412 references cannot be inverted (i.e., V_{REFL} cannot be greater than V_{REFH}).

It is important to note that the DAC-8412's V_{REFH} input both sinks and sources current. Also the input current of both V_{REFH} and V_{REFL} are code dependent. Many references have limited current sinking capability and must be buffered with an amplifier to drive V_{REFH}. The V_{REFL} has no such special requirements.

It is recommended that the reference inputs be bypassed with 0.2 µF capacitors when operating with ±10 volt references.

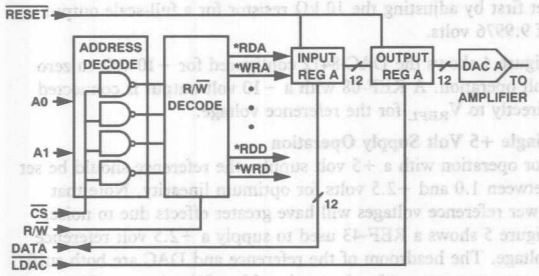
Digital I/O

See Table I for digital control logic truth table. Digital I/O consists of a 12-bit wide bidirectional data bus, two register select inputs, A0 and A1, a R/$\overline{W}$ input, a $\overline{RESET}$ input, a Chip Select ($\overline{CS}$), and a Load DAC ($\overline{LDAC}$) input. Control of the DACs and bus direction is determined by these inputs as shown in Table I. Digital data bits are labeled with the MSB defined as data bit "11" and the LSB as data bit "0." All digital pins are TTL/CMOS compatible.

Table I. DAC-8412/DAC-8413 Logic Table

A1	A0	R/$\overline{W}$	$\overline{CS}$	$\overline{RS}$	$\overline{LDAC}$	INPUT REG	OUTPUT REG	MODE	DAC
L	L	L	L	H	L	WRITE	WRITE	WRITE	A
L	H	L	L	H	L	WRITE	WRITE	WRITE	B
H	L	L	L	H	L	WRITE	WRITE	WRITE	C
H	H	L	L	H	L	WRITE	WRITE	WRITE	D
L	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	A
L	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	B
H	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	C
H	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	D
L	L	H	L	H	H	READ	HOLD	READ INPUT	A
L	H	H	L	H	H	READ	HOLD	READ INPUT	B
H	L	H	L	H	H	READ	HOLD	READ INPUT	C
H	H	H	L	H	H	READ	HOLD	READ INPUT	D
X	X	X	H	H	L	HOLD	Update all output registers		All
X	X	X	H	H	H	HOLD	HOLD	HOLD	All
X	X	X	X	L	X	*All registers reset to mid/zero-scale			All
X	X	X	H	↓	X	*All registers latched to mid/zero-scale			All

*DAC-8412 resets to midscale, and DAC-8413 resets to zero scale. L = Logic Low; H = Logic High; X = Don't Care.



*NOTE: THE SIGNALS RDA, WRA, ETC., ARE INTERNAL CONTROL SIGNALS. THEY ARE INCLUDED FOR CLARIFICATION ONLY.

Figure 1. I/O Logic Diagram

See Figure 1 for a simplified I/O logic diagram. The register select inputs A0 and A1 select individual DAC registers "A" (binary code 00) through "D" (binary code 11). Decoding of the registers is enabled by the $\overline{CS}$ input. When $\overline{CS}$ is high no decoding takes place, and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the $\overline{LDAC}$ input. By taking $\overline{LDAC}$ low while $\overline{CS}$ is high, all output registers can be updated simultaneously. Note that the t_{LWD} required pulse width for updating all DACs is a minimum of 170 ns.

The R/$\overline{W}$ input, when enabled by $\overline{CS}$, controls the writing to and reading from the input register.

Coding

Both the DAC-8412 and DAC-8413 use binary coding. The output voltage can be calculated by:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) * N}{4096}$$

where N is the digital code in decimal.

RESET

The $\overline{RESET}$ function can be used either at power-up or at any time during the DAC's operation. The $\overline{RESET}$ function is independent of $\overline{CS}$. This pin is active LOW and sets the DAC output registers to either center code for the DAC-8412, or zero code for the DAC-8413. The reset to center code is most useful when the DAC is configured for bipolar references and an output of zero volts after reset is desired.

Supplies

Supplies required are V_{SS}, V_{DD} and V_{LOGIC}. The V_{SS} supply can be set between −15 volts and 0 volts. V_{DD} is the positive supply; its operating range is between +5 and +15 volts.

V_{LOGIC} is the digital output reference voltage for the readback function. It is normally connected to +5 volts. This pin is a logic reference input only. It does not supply current to the device. *If you are not using the readback function, V_{LOGIC} can be hard-wired to V_{DD}.* While V_{LOGIC} does not supply current to the DAC-8412, it does supply currents to the digital outputs when readback is used.

Amplifiers

Unlike many voltage output DACs, the DAC-8412 features buffered voltage outputs. Each output is capable of both sourcing and sinking 5 mA at ±10 volts, eliminating the need for external amplifiers in most applications. These amplifiers are short circuit protected.

Careful attention to grounding is important to accurate operation of the DAC-8412. This is not because the DAC-8412 is more sensitive than other 12-bit DACs, but because with four outputs and two references there is greater potential for ground loops. Since the DAC-8412 has no analog ground, the ground must be specified with respect to the reference.

Reference Configurations

Output voltage ranges can be configured as either unipolar or bipolar, and within these choices a wide variety of options exists. The unipolar configuration can be either positive or negative voltage output, and the bipolar configuration can be either symmetrical or nonsymmetrical.

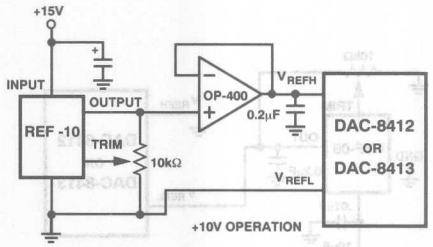


Figure 2. Unipolar +10 V Operation

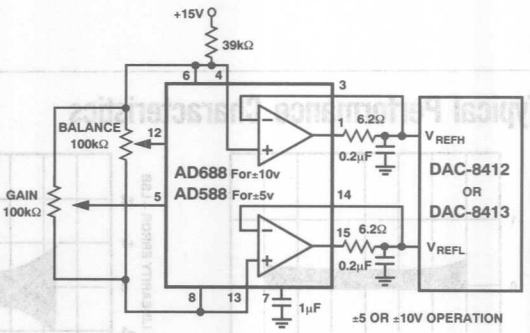


Figure 3. Symmetrical Bipolar Operation

Figure 3 (Symmetrical Bipolar Operation) shows the DAC-8412 configured for ±10 volt operation. *Note: See the AD688 data sheet for a full explanation of reference operation.* Adjustments may not be required for many applications since the AD688 is a very high accuracy reference. However if additional adjustments are required, adjust the DAC-8412 full scale first. Begin by loading the digital full-scale code (FFF_H), and then adjust the Gain Adjust potentiometer to attain a DAC output voltage of 9.9976 volts. Then, adjust the Balance Adjust to set the center scale output voltage to 0.000 volts.

The 0.2 μF bypass capacitors shown at the reference inputs in Figure 3 should be used whenever ±10 volt references are used. Applications with single references or references to ±5 volts may not require the 0.2 μF bypassing. The 6.2 Ω resistor in series with the output of the reference amplifier is to keep the

resistor values are acceptable, provided that the drop across the resistor doesn't exceed a V_{BE}. Assuming a minimum V_{BE} of 0.6 volts and a maximum current of 2.75 mA, then the resistor should be under 200 Ω for the loading of a single DAC-8412.

Using two separate references is not recommended. Having two references could cause different drifts with time and temperature; whereas with a single reference, most drifts will track.

Unipolar positive full-scale operation can usually be set with a reference with the correct output voltage. This is preferable to using a reference and dividing down to the required value. For a 10 volt full-scale output, the circuit can be configured as shown in Figure 2. In this configuration the full-scale value is

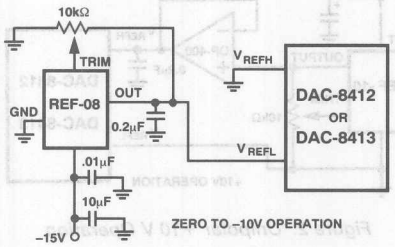


Figure 4. Unipolar −10 V Operation

Figure 4 shows the DAC-8412 configured for −10 volt to zero volt operation. A REF-08 with a −10 volt output is connected directly to V_{REFL} for the reference voltage.

Single +5 Volt Supply Operation

For operation with a +5 volt supply, the reference should be set between 1.0 and +2.5 volts for optimum linearity. Note that lower reference voltages will have greater effects due to noise. Figure 5 shows a REF-43 used to supply a +2.5 volt reference voltage. The headroom of the reference and DAC are both sufficient to support a +5 volt supply with ±5% tolerance. V_{DD} and V_{LOGIC} should be connected to the same supply and separate bypassing to each pin should be used.

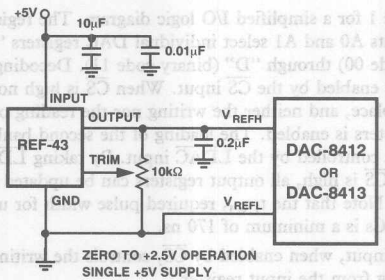
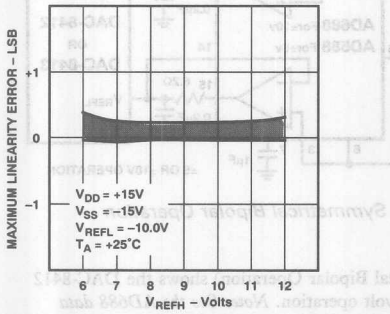
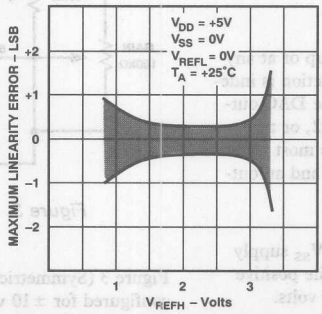


Figure 5. +5 V Single Supply Operation

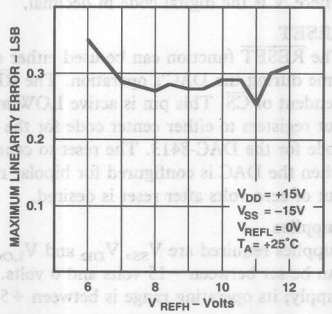
Typical Performance Characteristics



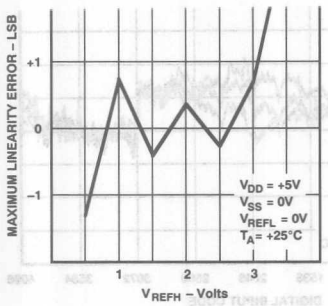
Differential Linearity vs. V_{REFH}



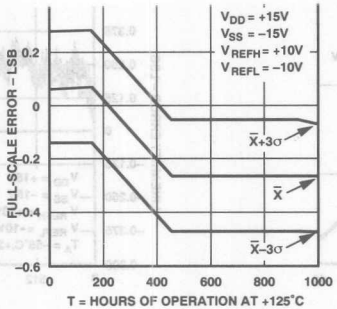
Differential Linearity vs. V_{REFH}



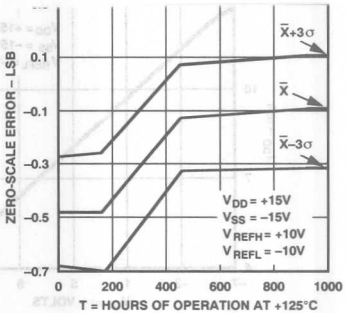
INL vs. V_{REFH}



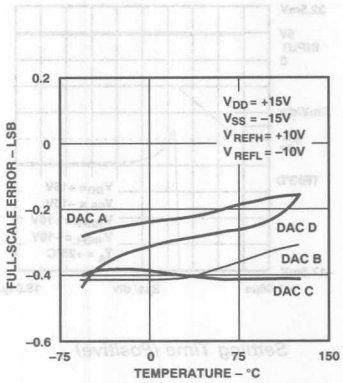
INL vs. V_{REFH}



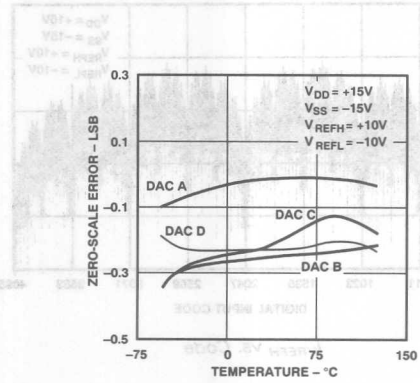
Full-Scale Error vs. Time Accelerated by Burn-In



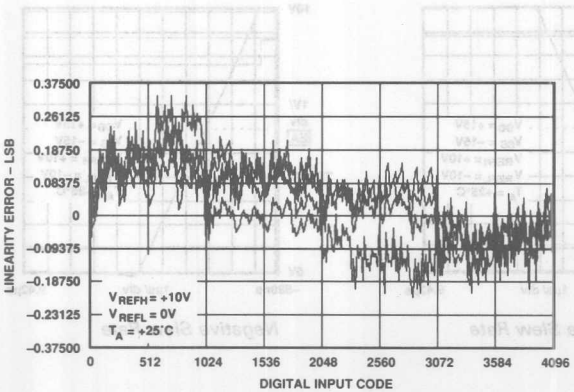
Zero-Scale Error vs. Time Accelerated by Burn-In



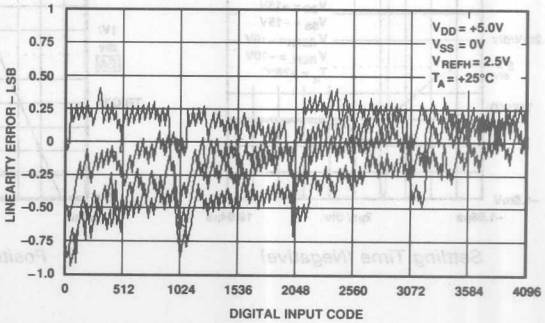
Full-Scale Error vs. Temperature



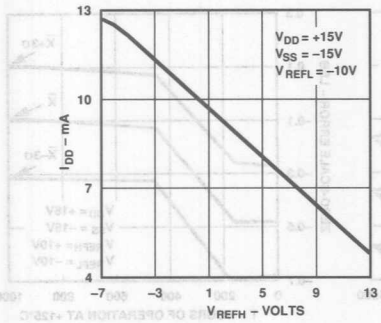
Zero-Scale Error vs. Temperature



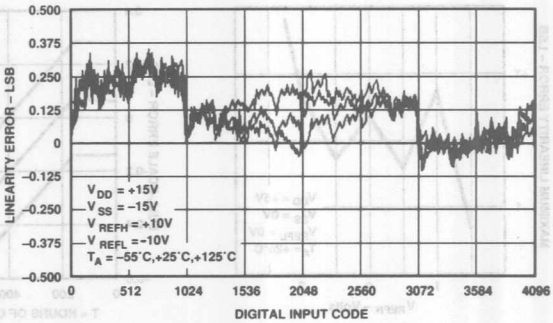
Channel-to-Channel Matching (V_{SUPPLY} = ±15 V)



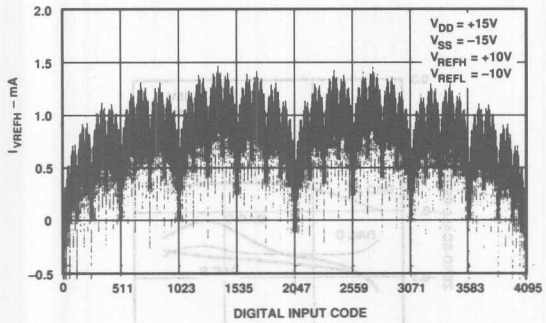
Channel-to-Channel Matching (V_{SUPPLY} = +5 V)



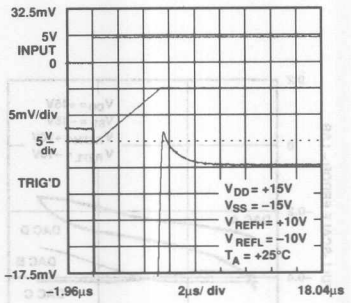
I_{DD} vs. V_{REFH} All DACS High



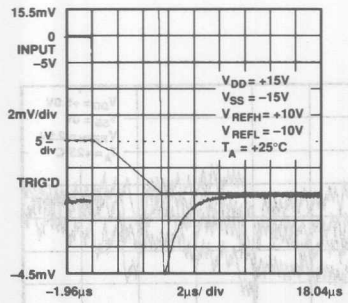
INL vs. Code



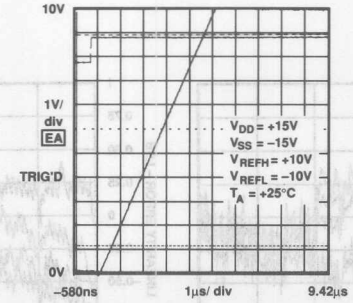
I_{VREFH} vs. Code



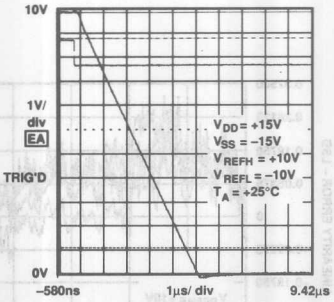
Settling Time (Positive)



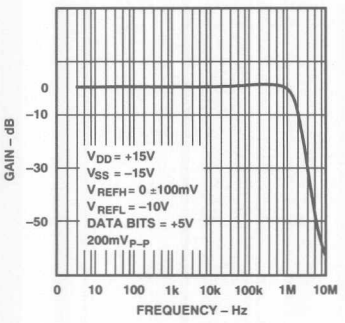
Settling Time (Negative)



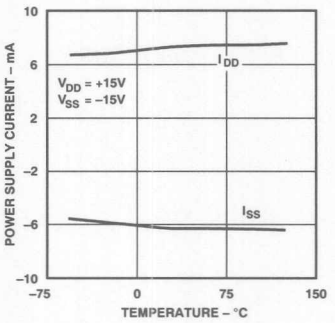
Positive Slew Rate



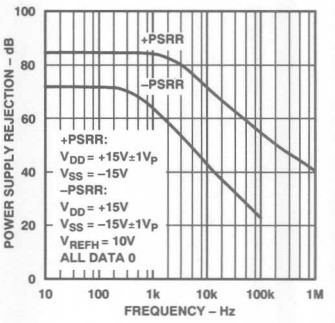
Negative Slew Rate



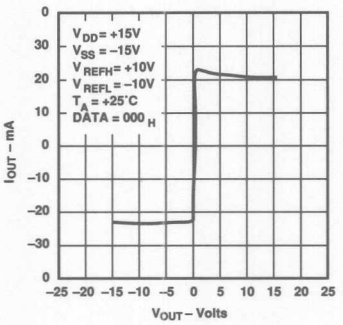
Small Signal Response



Power Supply Current vs. Temperature



PSRR vs. Frequency



I_{OUT} *vs.* V_{OUT}

FEATURES

- **No Adjustments Required, Total Error ± 1LSB Max Over Temperature**
- **Four Voltage-Output DACs on a Single Chip**
- **Internal 10V bandgap Reference**
- **Operates from Single +15V Supply**
- **Fast 50ns Data Load Time, All Temperatures**
- **Pin-for-Pin Replacement for PM-7226 and AD7226, Eliminates External Reference**

APPLICATIONS

- **Process Controls**
- **Multi-Channel Microprocessor Controlled:**
  - **– System Calibration**
  - **– Op Amp Offset and Gain Adjust**
  - **– Level and Threshold Setting**

GENERAL DESCRIPTION

The DAC-8426 is a complete quad voltage output D/A converter with internal reference. This product fits directly into any existing 7226 socket where the user currently has a 10V external reference. The external reference is no longer necessary. The internal reference of the DAC-8426 is laser-trimmed to ±0.4% offering a 25ppm/°C temperature coefficient and 5mA of external load driving capability.

The DAC-8426 contains four 8-bit voltage-output CMOS D/A converters on a single chip. A 10V output bandgap reference sets the output full-scale voltage. The circuit also includes four input latches and interface control logic.

One of the four latches, selected by the address inputs, is loaded from the 8-bit data bus input when the write strobe is active low. All digital inputs are TTL/CMOS (5V) compatible. The on-board amplifiers can drive up to 10mA from either a single or dual supply. The on-board reference that is always connected to the internal DACs has 5mA available to drive external devices.

Continued

ORDERING INFORMATION†

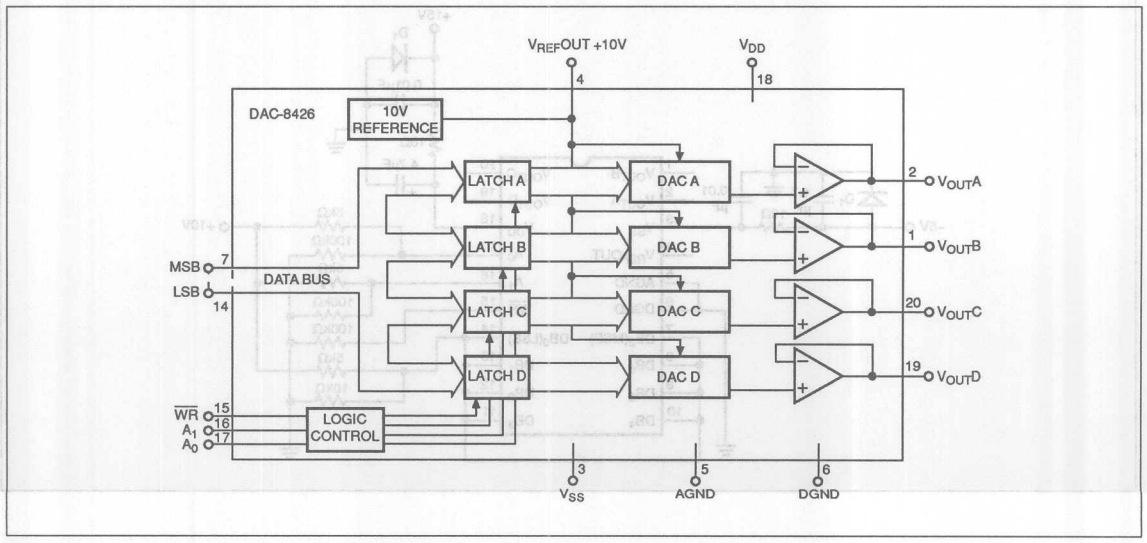
TOTAL UNADJUSTED ERROR (LSB)	MIL TEMP –55°C to +125°C	XIND TEMP –40°C to +85°C
±1	DAC8426AR	DAC8426ER
±1	–	DAC8426EP
±2	DAC8426BR	DAC8426FR
±2	–	DAC8426FP
±2	–	DAC8426FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

SIMPLIFIED SCHEMATIC

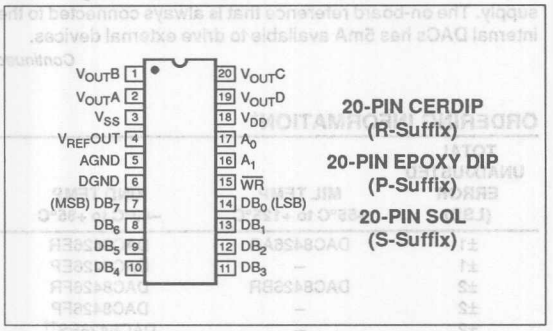


GENERAL DESCRIPTION *Continued*

Its compact size, low power, and economical cost-per-channel, make the DAC-8426 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

PMI's advanced oxide-based, silicon-gate, CMOS process allows the DAC-8426's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND or DGND ..... –0.3V, +17V
V_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3V, +5V
Digital Input Voltage to DGND ..... –0.3V, V_{DD}
V_{REF}OUT to AGND (Note 1) ..... –0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature
Military AR/BR ..... –55°C to +125°C
Extended Industrial ER/EP/FR/FP/FS ..... –40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

THERMAL RESISTANCE

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
20-Pin CerDIP (R)	70	7	°C/W
20-Pin Plastic DIP (P)	61	24	°C/W
20-Pin SOL (S)	80	22	°C/W

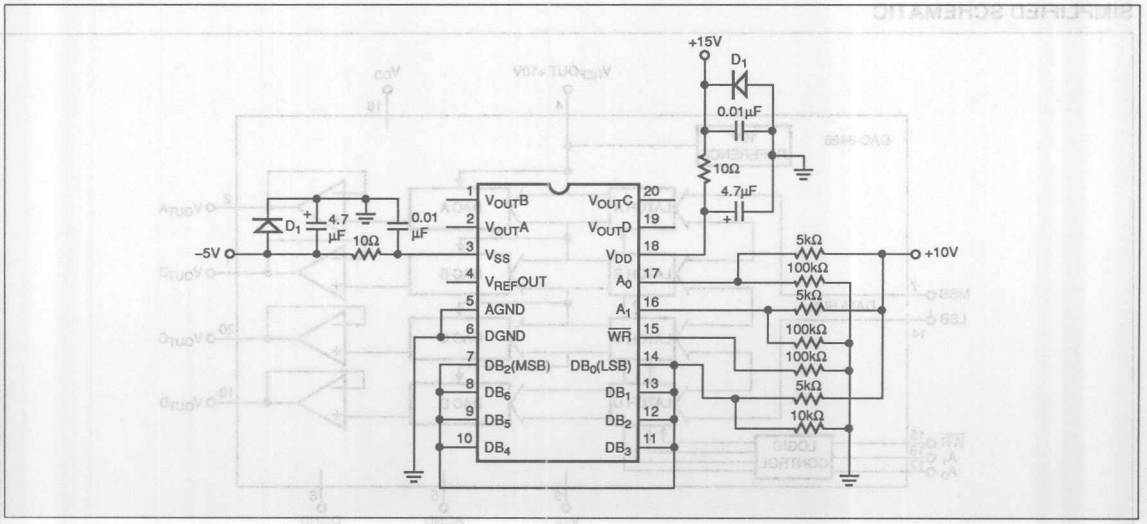
NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets. Remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

BURN-IN CIRCUIT



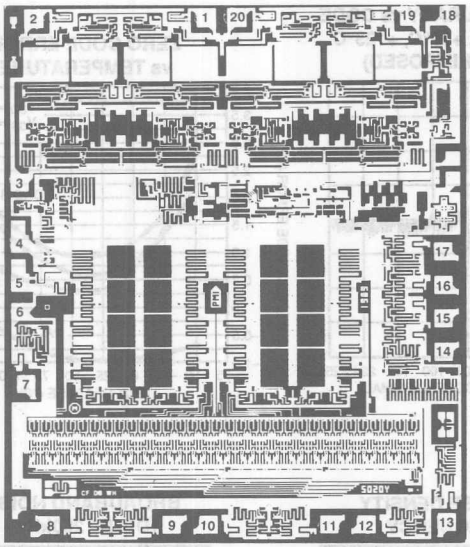
ELECTRICAL CHARACTERISTICS: V_{DD} = +15V ±10%, AGND = DGND = 0V, V_{SS} = 0V, T_A = –55°C to +125°C applies for DAC-8426AR/BR, T_A = –40°C to +85°C applies for DAC-8426ER/EP/FR/FP/FS, unless otherwise noted.

				DAC-8426			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP[6]**	**MAX**	**UNITS**
STATIC PERFORMANCE							
Resolution	N			8	—	—	Bits
Total Unadjusted Error (Note 1)	TUE	Includes Reference	A,E	—	—	±1	LSB
			B,F	—	—	±2	
Relative Accuracy	INL		A,E	—	—	±1/2	LSB
			B,F	—	—	±1	
Differential Nonlinearity (Note 2)	DNL			—	—	±1	LSB
Full-Scale Temperature Coefficient	TCG_{FS}	Includes Reference		—	25	—	ppm/°C
Zero Scale Error	V_{ZSE}			—	—	20	mV
Zero Scale Error Temperature Coefficient	TCV_{ZS}	Dual Supply	V_{SS} = –5V	—	10	—	µV/°C
REFERENCE OUTPUT							
Output Voltage	$V_{REF}OUT$	No Load	A,E	9.96	—	10.04	V
			B,F	9.92	—	10.08	
Temperature Coefficient	$TCV_{REF}OUT$			—	20	—	ppm/°C
Load Regulation	LD_{REG}	ΔI_L = 5mA		—	0.02	0.1	%/mA
Line Regulation	LN_{REG}	ΔV_{DD} ±10%		—	0.008	0.04	%/V
Output Noise (Note 3)	e_{NRMS}	f = 0.1 to 10Hz		—	3	10	μV_{p-p}
Output Current	$I_{REF}OUT$	$\Delta V_{REF}OUT$ < 40mV		5	7	—	mA
DIGITAL INPUTS							
Logic Input "0"	V_{INL}			—	—	0.8	V
Logic Input "1"	V_{INH}			2.4	—	—	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		—	0.1	10	µA
Input Capacitance (Note 3)	C_{IN}			—	4	8	pF
POWER SUPPLIES							
Positive Supply Current (Note 4)	I_{DD}			—	6	14	mA
Negative Supply Current (Note 4)	I_{SS}	Dual Supply	V_{SS} = –5V	—	4	10	mA
Power Dissipation (Note 5)	P_{DISS}			—	90	210	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%		—	0.0002	0.01	%/%

PARAMETER	SYMBOL	CONDITIONS		DAC-8426 MIN	TYP[6]	MAX	UNITS
DAC OUTPUT							
Output Current (Source) (Note 3)	I_{OUT}SOURCE	Digital In = All Ones		10	—	—	mA
Output Current (Sink) (Note 3)	I_{OUT}SINK	Digital In = All Zeroes	V_{SS} = –5V	350	450	—	µA
Minimum Load Resistance	$R_{L(MIN)}$	Digital In = All Ones		2	—	—	kΩ
DYNAMIC PERFORMANCE (NOTE 3)							
V_{OUT} Slew Rate	SR			—	4	—	V/µs
V_{OUT} Settling Time (Positive or Negative)	t_S	To ± 1/2 LSB, R_L = 2kΩ		—	3	—	µs
Digital Crosstalk	Q			—	10	—	nVs
SWITCHING CHARACTERISTICS (Note 3)							
Address To Write Setup Time	t_{AS}			0	—	—	ns
Address To Write Hold Time	t_{AH}			0	—	—	ns
Data Valid To Write Setup Time	t_{DS}			70	—	—	ns
Data Valid To Write Hold Time	t_{DH}			10	—	—	ns
Write Pulse Width	t_{WR}			50	—	—	ns

NOTES:
1. Includes Full-Scale Error, Relative Accuracy, and Zero Code Error. Note ±1 LSB = ±0.39% error.
2. All devices guaranteed monotonic over the full operating temperature range.
3. Guaranteed and not subject to production test.
4. Digital inputs $V_{IN} = V_{INL}$ or V_{INH}; V_{OUT} and V_{REF}OUT unloaded.
5. P_{DISS} calculated by $I_{DD} \times V_{DD}$.
6. Typicals represent measured characteristics at T_A = +25°C.

DICE CHARACTERISTICS



1. $V_{OUT\ B}$
2. $V_{OUT\ A}$
3. V_{SS}
4. $V_{REF}OUT$
5. AGND
6. DGND
7. DB_7 (MSB)
8. DB_6
9. DB_5
10. DB_4
11. DB_3
12. DB_2
13. DB_1
14. DB_0 (LSB)
15. $\overline{WR}$
16. A_1
17. A_0
18. V_{DD}
19. $V_{OUT\ D}$
20. $V_{OUT\ C}$

DIE SIZE 0.129 x 0.152 inch, 19,608 sq. mils
(3.28 x 3.86 mm, 12.65 sq. mm)

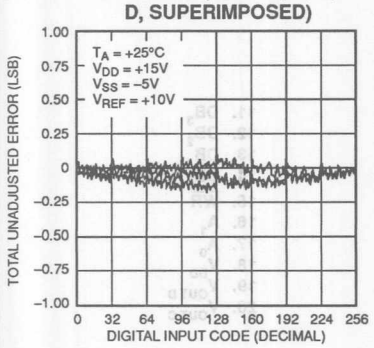
WAFER TEST LIMITS at V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; unless otherwise specified. T_A = +25°C. All specifications apply for DACs A, B, C, and D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8426GBC LIMITS	UNITS
Total Unadjusted Error	TUE		±2	LSB Max
Relative Accuracy	INL		±1	LSB Max
Differential Nonlinearity	DNL		±1	LSB Max
Full-Scale Error	G_{FSE}		±1	LSB Max
Zero Code Error	V_{ZSE}		±20	mV Max
DAC Output Current	I_{OUT}SOURCE	Digital In = All Ones	10	mA Min
Reference Output Voltage	$V_{REF}OUT$	No Load	9.96 10.04	V Min V Max
Load Regulation	LD_{REG}	ΔI_L = 5mA	0.1	%/mA Max
Line Regulation	LN_{REG}	ΔV_{DD} = ±10V	0.04	%/V Max
Reference Output Current	$I_{REF}OUT$	$\Delta V_{REF}OUT$ < 40mV	5	mA Min
Logic Inputs High	V_{INH}		2.4	V Min
Logic Inputs Low	V_{INL}		0.8	V Max
Logic Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA Max
Positive Supply Current	I_{DD}	V_{IN} = V_{INL} or V_{INH}	14	mA Max
Negative Supply Current	I_{SS}	V_{IN} = V_{INL} or V_{INH}, V_{SS} = –5V	10	mA Max

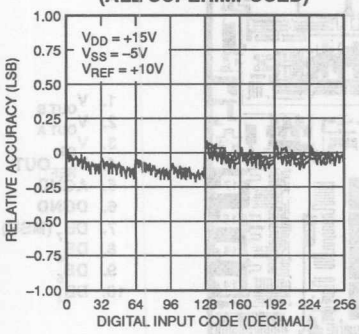
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

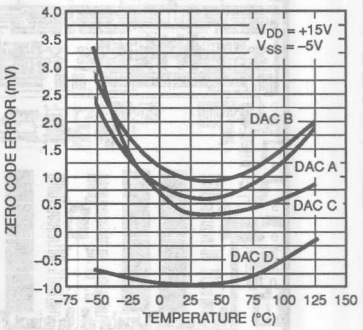
CHANNEL-TO-CHANNEL MATCHING (DACs A, B, C, D, SUPERIMPOSED)



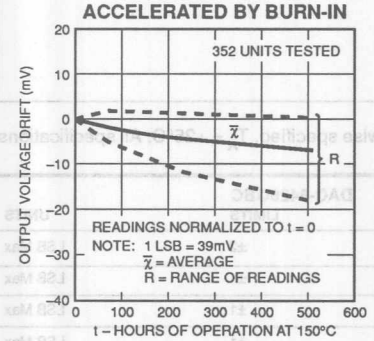
RELATIVE ACCURACY vs CODE AT T_A = –55°C, +25°C, +125°C (ALL SUPERIMPOSED)



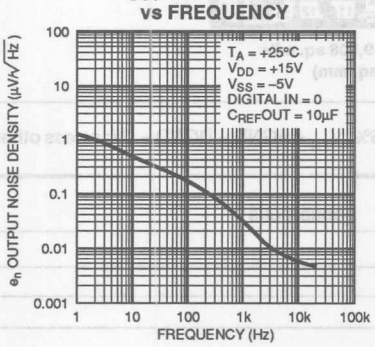
ZERO CODE ERROR vs TEMPERATURE



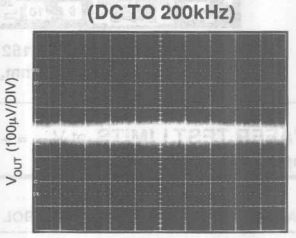
LONG TERM DRIFT ACCELERATED BY BURN-IN



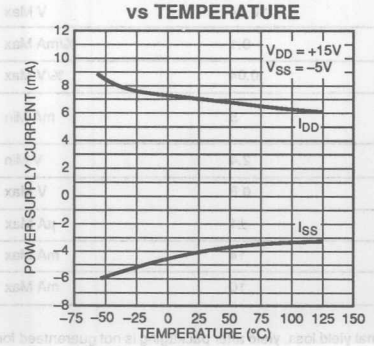
V_{OUT} NOISE DENSITY vs FREQUENCY



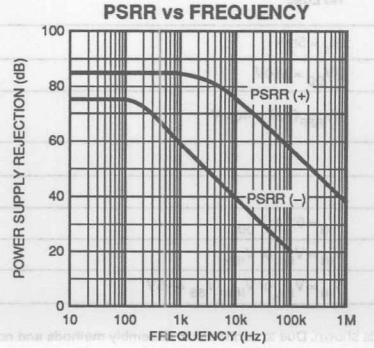
BROADBAND NOISE (DC TO 200kHz)



POWER SUPPLY CURRENT vs TEMPERATURE



PSRR vs FREQUENCY



$$PSRR(+) = -20 \text{ LOG} \left(\frac{V_{OUT}(0)}{\Delta V_{DD}} \right),$$

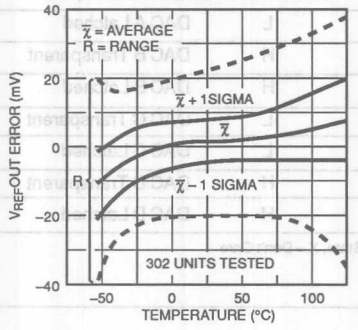
V_{DD} = +15V ±1V_p, V_{SS} = 0V

$$PSRR(-) = -20 \text{ LOG} \left(\frac{V_{OUT}(0)}{\Delta V_{SS}} \right),$$

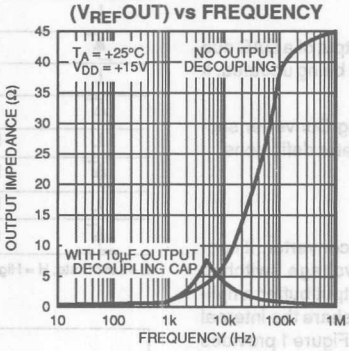
V_{DD} = +15V , V_{SS} = –4V ±1V_p

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

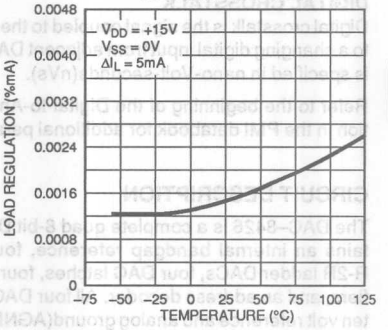
V_{REF}OUT ERROR FROM 10.000V vs TEMPERATURE



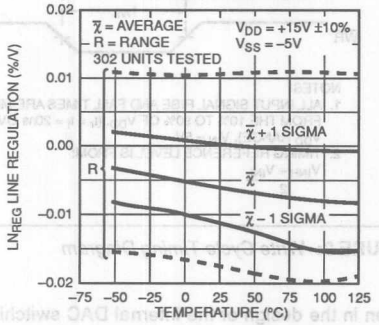
OUTPUT IMPEDANCE (V_{REF}OUT) vs FREQUENCY



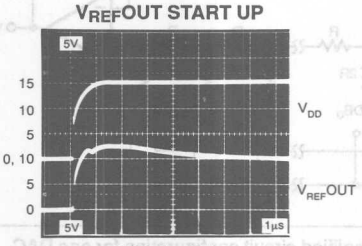
V_{REF}OUT LOAD REGULATION vs TEMPERATURE



V_{REF}OUT LINE REGULATION vs TEMPERATURE



V_{REF}OUT START UP



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR (TUE)

This specification includes the Full-Scale-Error, Relative Accuracy Zero-Code-Error and the internal reference voltage. The ideal Full-Scale output voltage is 10V minus 1 LSB which equals 9.961 volts. Each LSB equals 10V x (1/256) = 0.039 volts.

DIGITAL CROSSTALK

Digital crosstalk is the signal coupled to the output of a DAC due to a changing digital input from adjacent DACs being updated. It is specified in nano-Volt-seconds(nVs).

Refer to the beginning of the Digital-to-Analog Converter section in the PMI databook for additional parameter definitions.

CIRCUIT DESCRIPTION

The DAC–8426 is a complete quad 8-bit D/A converter. It contains an internal bandgap reference, four voltage switched R-2R ladder DACs, four DAC latches, four output buffer amplifiers, and an address decoder. All four DACs share the internal ten volt reference and analog ground(AGND). Figure 1 provides an equivalent DAC plus buffer schematic.

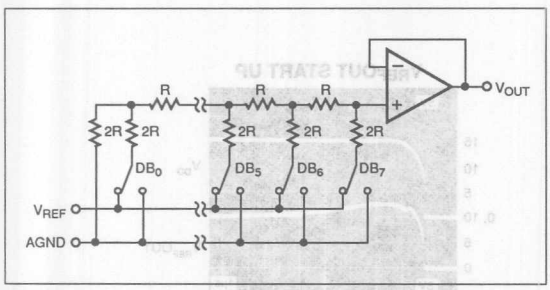


FIGURE 1: Simplified circuit configuration for one DAC. (Switches are shown for all "1s" on the digital inputs.)

The eleven digital inputs are compatible with both TTL and 5V(or higher) CMOS logic. Table 1 shows the DAC control logic truth table for $\overline{WR}$, A_1, and A_0 operation. When $\overline{WR}$ is active low the input latch of the selected DAC is transparent, and the DAC's output responds to the data present on the eight digital data inputs(DBx). The data (DBx) is latched into the addressed DAC's latch on the positive edge of the $\overline{WR}$ control signal. The important timing requirements are shown in the Write Cycle Timing Diagram, Figure 2.

INTERNAL TEN VOLT REFERENCE

The internal 10V bandgap reference of the DAC-8426 is trimmed to the output voltage and temperature drift specifications. This internal reference is connected to the reference inputs of the four internal 8-bit D/A converters. The output terminal of the internal 10V reference is available on pin 4. The 10V output of the reference is produced with respect to the AGND pin. This reference output can be used to supply as much as 5mA of additional current to external devices. Care has been taken in the design of the internal DAC switching to minimize transients on the reference voltage terminal(V_{REF}OUT). Other devices connected to this reference terminal should have well behaved input loading characteristics. D/A converters such as the PMI PM-7226A have been designed to minimize reference input transient currents and can be directly connected to the DAC-8426 10V reference. Devices exhibiting large current transients due to internal switching should be buffered with an op amp to maintain good overall system noise performance. A 10µF reference output bypass capacitor is required.

TABLE 1: DAC Control Logic Truth Table

LOGIC CONTROL			DAC-8426
$\overline{WR}$	A_1	A_0	OPERATION
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
↑	L	L	DAC A Latched
L	L	H	DAC B Transparent
↑	L	H	DAC B Latched
L	H	L	DAC C Transparent
↑	H	L	DAC C Latched
L	H	H	DAC D Transparent
↑	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

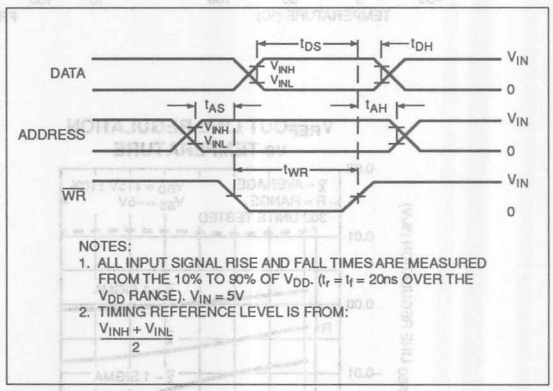


FIGURE 2: *Write Cycle Timing Diagram*

BUFFER AMPLIFIER SECTION

The four internal unity-gain voltage buffers provide low output impedance capable of sourcing 5mA or sinking 350µA. Typical output slew rates of ±4V/µs are achieved with 10V full-scale output changes and R_L = 2kΩ. Figure 3 photographs show large-signal and settling time response. Capacitive loads to 3300pF maximum, and resistive loads to 2kΩ minimum can be applied.

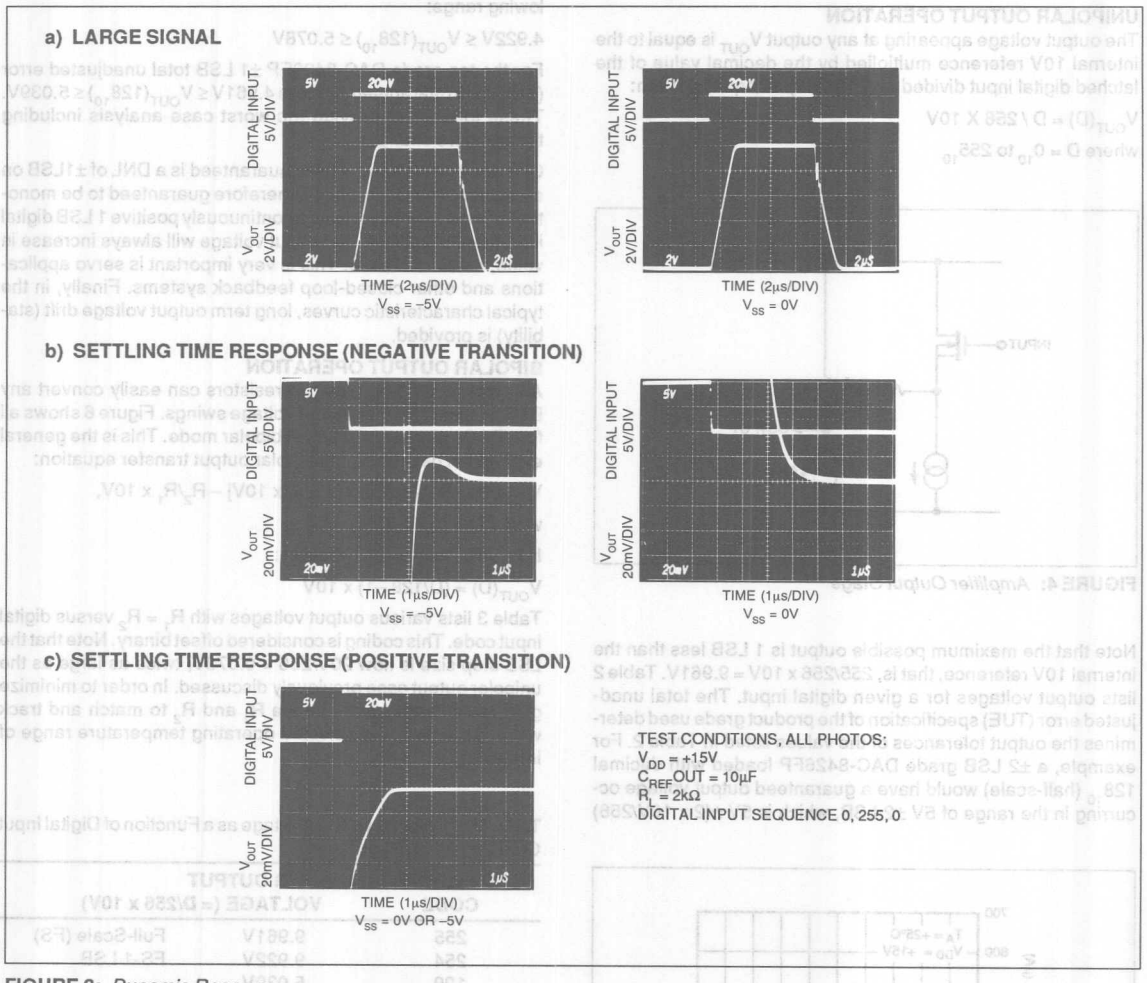


FIGURE 3: *Dynamic Response*

The outputs can withstand an indefinite short-circuit to AGND to typically 50mA. The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

The amplifier's emitter follower output stage consists of an intrinsic NPN bipolar transistor with a 400µA NMOS pull-down current-source load connected to V_{SS}. This circuit configuration shown in Figure 4 enables the output amplifier to develop output voltages very close to AGND. Only the negative supply of the four output buffer amplifiers are connected to V_{SS}. Operating the DAC-8426 from dual supplies (V_{DD} = +15V and V_{SS} = –5V) improves negative going output settling time near zero volts.

When operating single supply (V_{DD} = +15V and V_{SS} = 0V) the output sink current decreases as the output approaches zero voltage. Within 200mV of AGND (single-supply operation) the internal sinking capability appears resistive at a value of approximately 1200Ω. The buffer amplifier output current and voltage characteristics are plotted in Figure 5.

UNIPOLAR OUTPUT OPERATION

The output voltage appearing at any output V_{OUT} is equal to the internal 10V reference multiplied by the decimal value of the latched digital input divided by 2^8 (=256). In equation form:

$V_{OUT}(D) = D / 256 \times 10V$

where $D = 0_{10}$ to 255_{10}

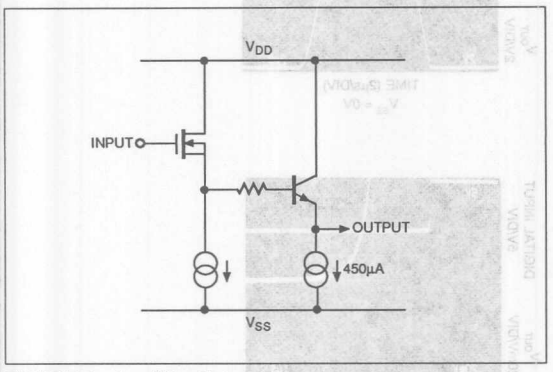


FIGURE 4: *Amplifier Output Stage*

Note that the maximum possible output is 1 LSB less than the internal 10V reference, that is, 255/256 x 10V = 9.961V. Table 2 lists output voltages for a given digital input. The total unadjusted error (TUE) specification of the product grade used determines the output tolerances of the values listed in Table 2. For example, a ±2 LSB grade DAC-8426FP loaded with decimal 128_{10} (half-scale) would have a guaranteed output voltage occurring in the range of 5V ±2 LSB, which is 5V ±(2 x 10V/256) lowing range:

$4.922V \le V_{OUT}(128_{10}) \le 5.078V$

For the top grade DAC-8426EP ±1 LSB total unadjusted error (TUE), the guaranteed range is $4.961V \le V_{OUT}(128_{10}) \le 5.039V$. These tolerances provide the worst case analysis including temperature changes.

One additional characteristic guaranteed is a DNL of ±1LSB on all grades. The DAC-8426 is therefore guaranteed to be monotonic. In the situation where a continuously positive 1 LSB digital increment is applied, the output voltage will always increase in value, never decrease. This is very important is servo applications and other closed-loop feedback systems. Finally, in the typical characteristic curves, long term output voltage drift (stability) is provided.

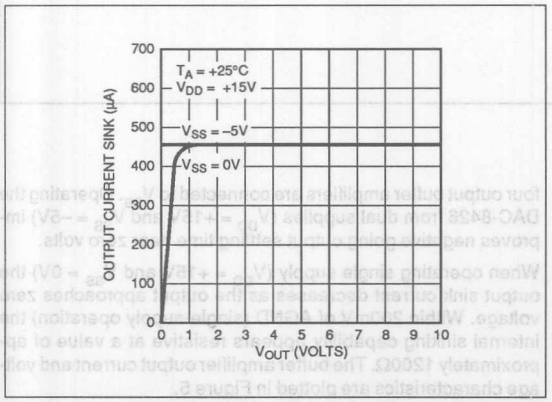


FIGURE 5: *DAC Output Current Sink*

BIPOLAR OUTPUT OPERATION

An external op amp plus two resistors can easily convert any DAC output to bipolar output voltage swings. Figure 6 shows all four DACs output operating in bipolar mode. This is the general expression describing the bipolar output transfer equation:

$V_{OUT}(D) = [(1+R_2/R_1) \times D/256 \times 10V] - R_2/R_1 \times 10V,$

where $D = 0_{10}$ to 255_{10}

If $R_1 = R_2$, then V_{OUT} becomes:

$V_{OUT}(D) = (D/128 - 1) \times 10V$

Table 3 lists various output voltages with $R_1 = R_2$ versus digital input code. This coding is considered offset binary. Note that the LSB step size is now 20V/256 = 0.078V, twice as large as the unipolar output case previously discussed. In order to minimize gain and offset errors, choose R_1 and R_2 to match and track within 0.1% over the selected operating temperature range of interest.

TABLE 2: Unipolar Output Voltage as a Function of Digital Input Code.

DIGITAL INPUT CODE	ANALOG OUTPUT VOLTAGE (= D/256 x 10V)	
255	9.961V	Full-Scale (FS)
254	9.922V	FS-1 LSB
129	5.039V	
128	5.000V	Half-Scale
127	4.961V	
1	0.039V	1 LSB
0	0.000V	Zero-Scale

OFFSETTING AGND

Since the DAC ladder and bandgap reference are terminated at AGND, it is possible to offset AGND positive with respect to DGND. The 10V output span remains if a positive offset is applied to AGND. The offset voltage source connected to AGND must be capable of sinking 14mA. AGND cannot be taken

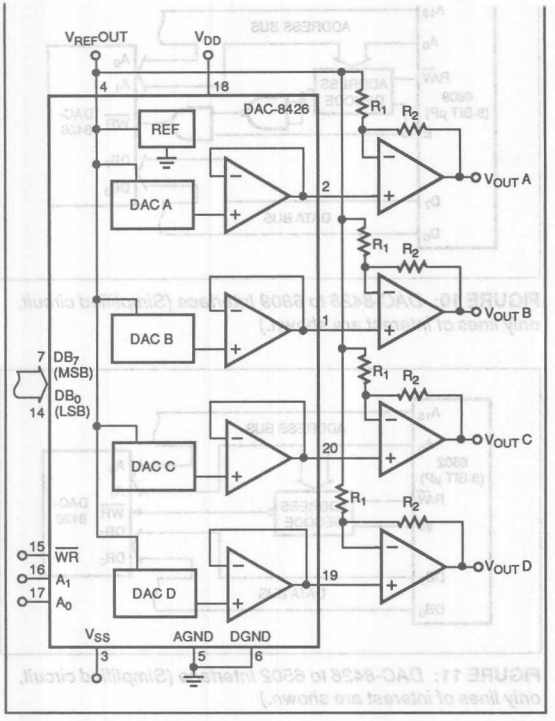


FIGURE 6: *Bipolar Operation*

negative with respect to DGND; this would forward bias an internal diode. Allowance must be made at V_{DD} to maintain 3.5V of headroom above V_{REF}OUT. This connection setup is useful in single supply applications where virtual ground needs to be slightly positive with respect to ground. In this application connect V_{SS} to DGND to take advantage of the extra buffer output current sinking capability when the DAC output is programmed to all zeros code, see Figure 7.

CONNECTION AND LAYOUT GUIDELINES

Layout and design techniques used in the interface between digital and analog circuitry require special attention to detail. The following considerations should be evaluated prior to PCB layout.

1. Return signal paths through the ground system should be carefully considered. High-speed digital logic current pulses traveling on return ground traces generate glitches that can be radiated to the analog circuits if the ground path layout produces loop antennas. Ground planes can minimize this situation. Separate digital and analog grounding areas to minimize crosstalk. Ideally a single common-point ground should be on the same PCB board as the DAC-8426. The analog ground returns should take advantage of the appropriate placement of power supply bypass capacitors.

TABLE 3: Bipolar Output Voltage as a Function of Digital Input Code

DIGITAL INPUT CODE	ANALOG OUTPUT VOLTAGE (= D/256 x 10V)	
255	9.922V	Full-Scale (FS)
254	9.844V	FS-1 LSB
129	0.078V	
128	0.000V	Zero-Scale
127	–0.078V	
1	–9.922V	
0	–10.000V	Neg Full-Scale

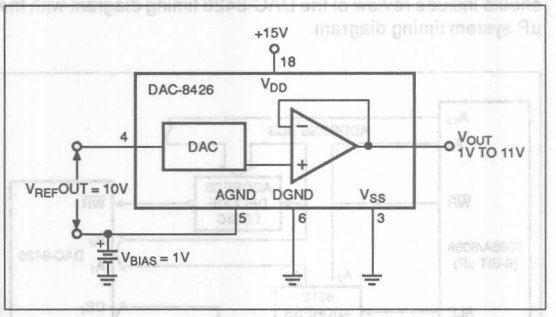


FIGURE 7: *AGND Biasing Scheme Providing Offset Output Range*

2. For optimum performance, bypass V_{DD} and V_{SS} (if using negative supply voltage) with 0.1µF ceramic disk capacitors to shunt high-frequency spikes. Also use in parallel 6.8µ to 10µF capacitors to provide a charge reservoir for lower frequency load change requirements. The reference output (V_{REF}OUT) should be bypassed with a 10µF tantulum capacitor to optimize reference output stability during data input changes. This helps to minimize digital crosstalk.
3. Power Supply Sequencing — No special requirements exist with the DAC-8426. However, users should be aware that often the 5V logic supply may be powered up momentarily prior to the +15V analog supply. In this situation, the DAC-8426 ESD input protection diodes will forward bias if the applied input logic is at logic "1". No damage will result to the input since the DAC-8426 is designed to withstand momentary currents of up to 130mA. This situation will likely exist for any DAC or ADC operating from a separate analog supply.
4. ESD input protection — Attention has been given in the design of the DAC-8426 to ESD sensitivity. Using the human body model test technique (MIL-STD 3015.4) the DAC-8426 generally will withstand 1500V ESD transients on all pins. Handling and testing prior to PCB insertion generally exposes ICs to the toughest environment they will experience. Once the IC is soldered in the PCB, it is still important to consider any traces that connect to PCB edge connectors. These traces should be protected with appropriate devices

especially if the boards will experience field replacement or adjustment. Handling the exposed edge connectors by field maintaince people in a low humidity environment can produce 20kV ESD transients which will be detrimental to almost any integrated IC connected to the edge connector.

MICROPROCESSOR INTERFACING

The DAC-8426 easily interfaces to most 8- and 16-bit wide databus systems. Serial and 4-bit busses can also be accommodated with additional latches and control circuitry. Interfacing can be accomplished with data bus transfers running with 50ns write pulse widths.

Examples of various microprocessor interface circuits are provided in Figures 8 through 12. These figures have omitted circuitry not essential to the bus interface. The design process should include review of the DAC-8426 timing diagram with the µP system timing diagram.

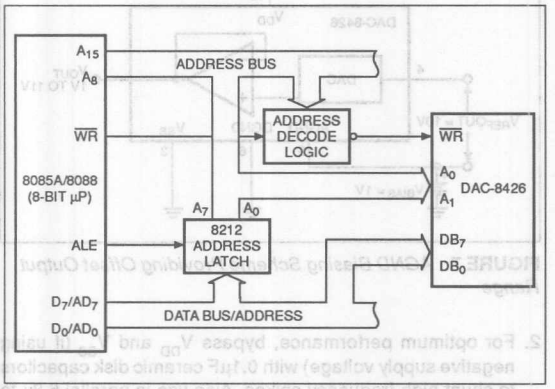


FIGURE 8: *DAC-8426 to 8085A Interface (Simplified circuit, only lines of interest are shown.)*

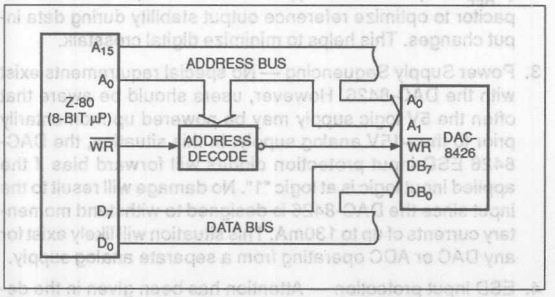


FIGURE 9: *DAC-8426 to Z-80 Interface (Simplified circuit, only lines of interest are shown.)*

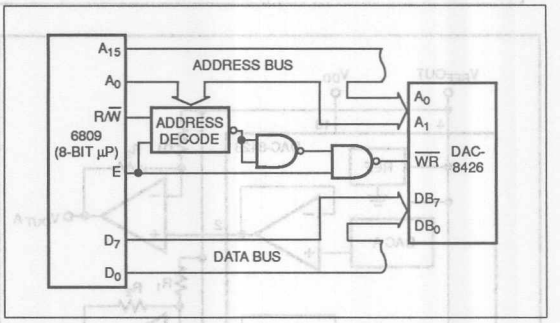


FIGURE 10: *DAC-8426 to 6809 Interface (Simplified circuit, only lines of interest are shown.)*

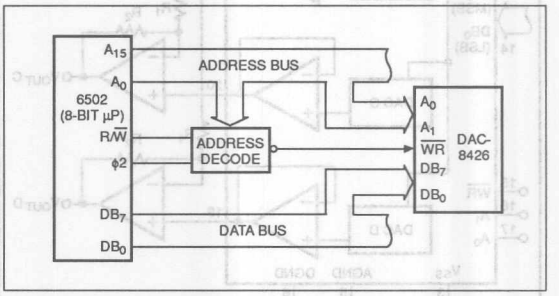


FIGURE 11: *DAC-8426 to 6502 Interface (Simplified circuit, only lines of interest are shown.)*

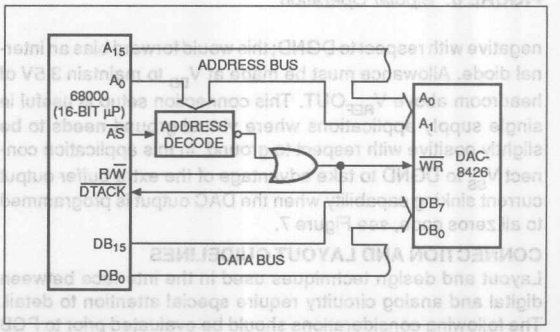


FIGURE 12: *DAC-8426 to 68000 Interface (Simplified circuit, only lines of interest are shown.)*

Octal 8-Bit CMOS D/A Converter

DAC-8800

FEATURES

- ±1/2 LSB Total Unadjusted Error
- 2μs Settling Time
- Serial Data Input
- ±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
- Unipolar and Bipolar Operation
- TTL Input Compatible
- 20-Pin DIP or SOL Package
- Low Cost

APPLICATIONS

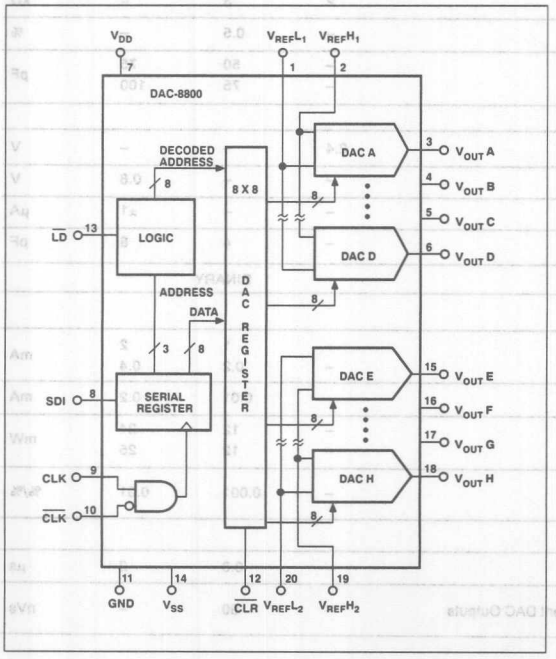
- Voltage Set Point Control
- Digital Offset & Gain Adjustment
- Microprocessor Controlled Calibration
- General Purpose Trimming Adjustments

GENERAL DESCRIPTION

The DAC-8800 TrimDAC™ is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear ($\overline{CLR}$) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

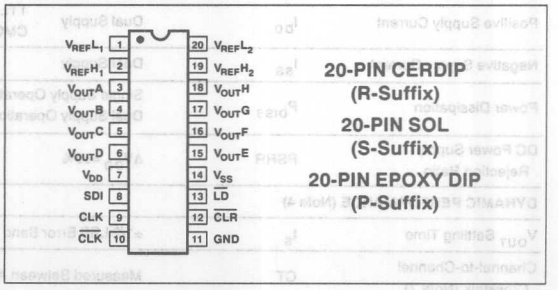
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 20-PIN	PLASTIC 20-PIN	SO 20-PIN	
DAC8800BR*	–	–	–55°C to +125°C
DAC8800FR	DAC8800FP	DAC8800FS††	–40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO package, contact your local sales office.

PIN CONNECTIONS



20-PIN CERDIP (R-Suffix)
20-PIN SOL (S-Suffix)
20-PIN EPOXY DIP (P-Suffix)

ELECTRICAL CHARACTERISTICS

$V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C, B GRADE: –55°C ≤ T_A ≤ +125°C.

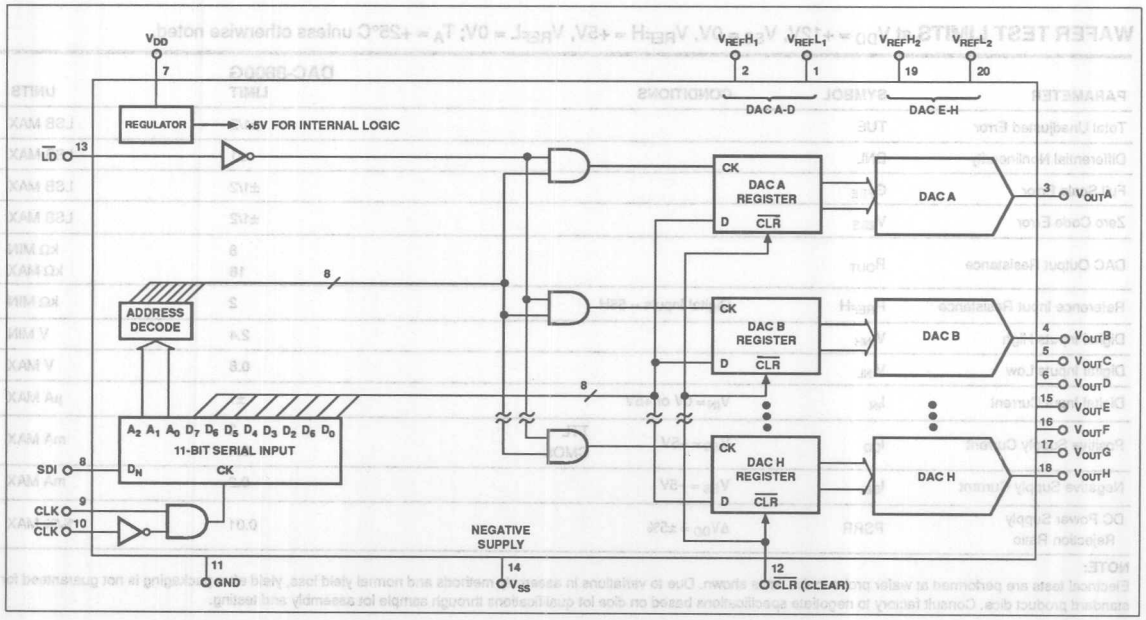
			DAC-8800			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
STATIC ACCURACY	All specifications apply for DACs A, B, C, D, E, F, G, H					
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 2)	TUE		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Error	G_{FSE}		–	–	±1/2	LSB
Zero Code Error	V_{ZSE}		–	–	±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$		–	0.5	–	%
REFERENCE INPUT						
Voltage Range (Note 5)	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$	–	$(V_{DD}-4)$	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}	–	$V_{REF}H$	
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3	–	kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H	–	0.5	–	%
Reference Input Capacitance (Note 4)	C_{REF}	Digital Inputs All Zeros	–	50	75	pF
		Digital Inputs All Ones	–	75	100	
DIGITAL INPUTS						
Logic High	V_{INH}		2.4	–	–	V
Logic Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or +5V	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES (Note 6)						
Positive Supply Current	I_{DD}	Dual Supply TTL	–	1	2	mA
		Dual Supply CMOS	–	0.2	0.4	
Negative Supply Current	I_{SS}	Dual Supply	–	0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation	–	12	24	mW
		Dual Supply Operation	–	12	25	
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} =±5%	–	0.001	0.01	%/%
DYNAMIC PERFORMANCE (Note 4)						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band	–	0.8	2	µs
Channel-to-Channel Crosstalk (Note 7)	CT	Measured Between Adjacent DAC Outputs	–	80	–	nVs

$V_{REF}L$ = 0V, for DUAL SUPPLY V_{DD} ... V_{SS} ... V_{REF} ...
$-55°C \le T_A \le +125°C$. *Continued*

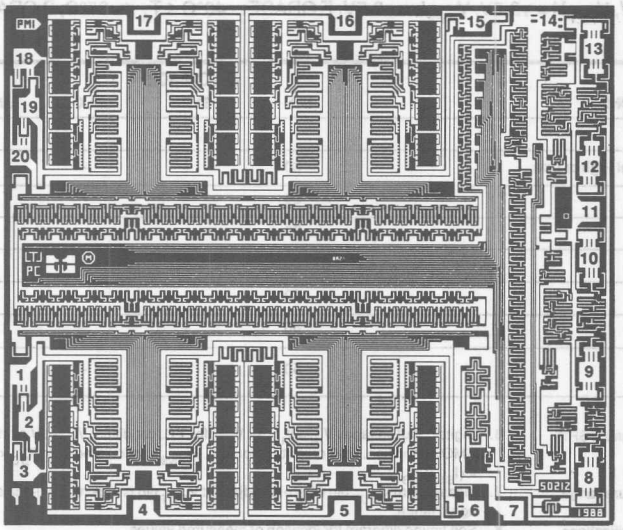
PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Notes 4, 8)						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60	–	–	ns
Data Setup Time	t_{DS}		30	–	–	ns
Data Hold Time	t_{DH}		30	–	–	ns
DAC Register Load Pulse Width	t_{LD}		50	–	–	ns
Clear Pulse Width	t_{CLR}		50	–	–	ns
Clock Edge to Load Time	t_{CKLD}		50	–	–	ns
Load Edge to Next Clock Edge Time	t_{LDCK}		50	–	–	ns

NOTES:
1. Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS}, and PSRR which are tested in DUAL SUPPLY mode.
2. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
3. All devices guaranteed monotonic over the full operating temperature range.
4. Guaranteed by design and not subject to production test.
5. V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H \ge V_{REF}L$.
6. Digital Input voltages $V_{IN} = V_{INL}$ or V_{INH} for TTL condition; V_{IN} = 0V or +5V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
7. Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.
8. See timing diagram for location of measured values.

DETAILED DAC-8800 BLOCK DIAGRAM



DICE CHARACTERISTICS



1. $V_{REF}L_1$
2. $V_{REF}H_1$
3. $V_{OUT}A$
4. $V_{OUT}B$
5. $V_{OUT}C$
6. $V_{OUT}D$
7. V_{DD}
8. SDI
9. CLK
10. $\overline{CLK}$
11. GND
12. $\overline{CLR}$
13. $\overline{LD}$
14. V_{SS}
15. $V_{OUT}E$
16. $V_{OUT}F$
17. $V_{OUT}G$
18. $V_{OUT}H$
19. $V_{REF}H_2$
20. $V_{REF}L_2$

DIE SIZE 0.151 × 0.130 inch, 19,630 sq. mils
(3.8354 × 3.3033 mm, 12.664 sq. mm)

WAFER TEST LIMITS at V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		DAC-8800G LIMIT	UNITS
Total Unadjusted Error	TUE			±1/2	LSB MAX
Differential Nonlinearity	DNL			±1	LSB MAX
Full Scale Error	G_{FSE}			±1/2	LSB MAX
Zero Code Error	V_{ZSE}			±1/2	LSB MAX
DAC Output Resistance	R_{OUT}			8 16	kΩ MIN kΩ MAX
Reference Input Resistance	$R_{REF}H$	Digital Inputs = 55H		2	kΩ MIN
Digital Inputs High	V_{INH}			2.4	V MIN
Digital Inputs Low	V_{INL}			0.8	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or +5V		±1	µA MAX
Positive Supply Current	I_{DD}	V_{SS} = –5V	TTL CMOS	2 0.4	mA MAX
Negative Supply Current	I_{SS}	V_{SS} = –5V		0.2	mA MAX
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		0.01	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to V_{SS} ..... 0V, +20V
V_{DD} to GND ..... 0V, +20V
V_{SS} to GND ..... –20V, 0V
Digital Input Voltage to GND ..... GND – 0.3V, V_{DD} + 0.3V
$V_{REF}H$ to GND ..... $V_{REF}L$, V_{DD}
$V_{REF}L$ to GND ..... V_{SS}, $V_{REF}H$
V_{OUT} to GND ..... $V_{REF}L$, $V_{REF}H$
Operating Temperature Range
Military, DAC-8800BR ..... –55°C to +125°C
Extended Industrial, DAC-8800FR,FP,FS ...–40°C to +85°C
Maximum Junction Temperature (T_j Max) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... $(T_j \text{ Max} - T_A)/\Theta_{JA}$

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SO (S)	88	25	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

2

TABLE 1: PIN Function Description

PIN	MNEMONIC	DESCRIPTION
1	$V_{REF}L_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}L_1$ determines the lowest negative DAC output voltage. $V_{REF}L_1$ must be equal to or more positive than V_{SS}.
2	$V_{REF}H_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}H_1$ determines the highest positive DAC output voltage.
3	$V_{OUT}A$	DAC A Output } Output voltage determined by external $V_{REF}H_1$ and $V_{REF}L_1$.
4	$V_{OUT}B$	DAC B Output
5	$V_{OUT}C$	DAC C Output
6	$V_{OUT}D$	DAC D Output
7	V_{DD}	Positive supply, allowable input voltage range +4.5V to +16V.
8	SDI	Serial Data Input } TTL Input Compatible
9	CLK	Serial Clock Input, positive edge triggered
10	$\overline{CLK}$	Clock Enable or Serial Clock Input, negative edge triggered
11	GND	Ground
12	$\overline{CLR}$	Clear Input (Active Low), Asynchronous TTL compatible input that resets all DAC registers to zero code.
13	$\overline{LD}$	Load DAC Register Strobe, TTL compatible input that transfers data bits from serial input register into the decoded DAC register. See Table 2.
14	V_{SS}	Negative Supply, allowable input voltage range 0V to –12V.
15	$V_{OUT}E$	DAC E Output } Output voltage determined by external $V_{REF}H_2$ and $V_{REF}L_2$.
16	$V_{OUT}F$	DAC F Output
17	$V_{OUT}G$	DAC G Output
18	$V_{OUT}H$	DAC H Output
19	$V_{REF}H_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}H_2$ determines the highest positive DAC output voltage.
20	$V_{REF}L_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}L_2$ determines the lowest negative DAC output voltage. $V_{REF}L_2$ must be equal to or more positive than V_{SS}.

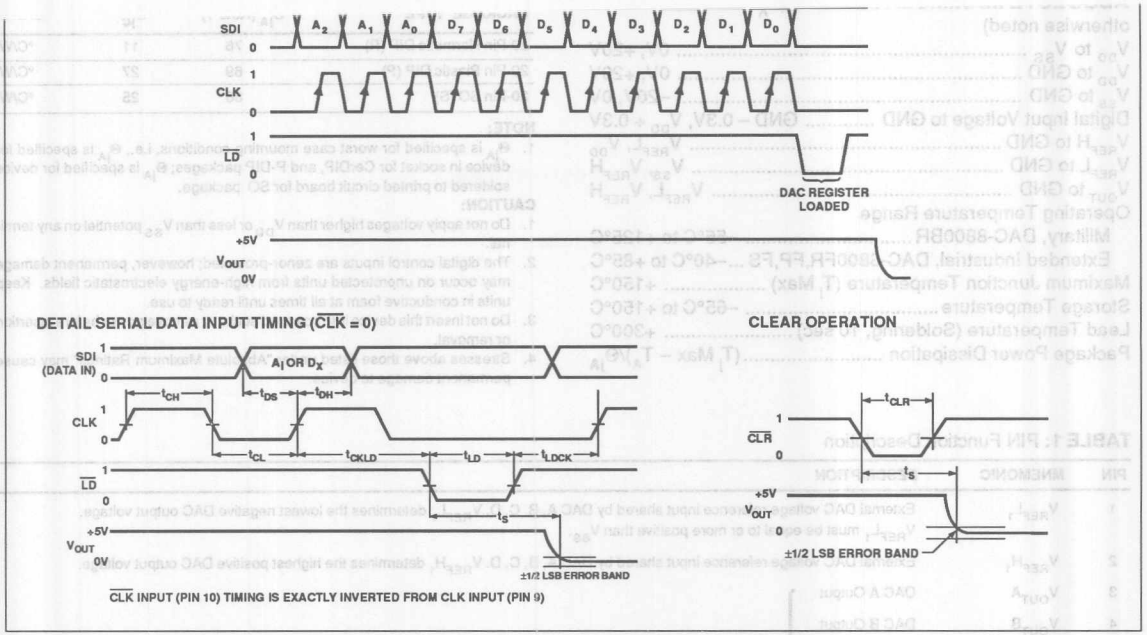


FIGURE 1: *Timing Diagrams*

TABLE 2: Serial Input Decode Table

LAST → FIRST

LSB D_0	D_1	D_2	D_3	D_4	D_5	D_6	MSB D_7	LSB A_0	A_1	MSB A_2

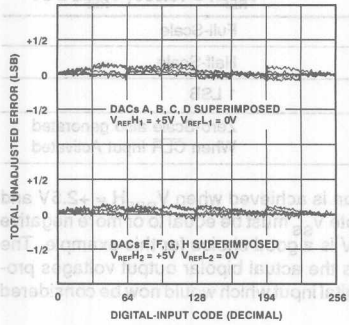
MSB D_7	D_6	D_5	D_4	D_3	D_2	D_1	LSB D_0	DAC OUTPUT VOLTAGE (K = $V_{REF}H - V_{REF}L$)
0	0	0	0	0	0	0	0	$V_{REF}L$
0	0	0	0	0	0	0	1	(1/256) x K + $V_{REF}L$
⋮								
0	1	1	1	1	1	1	1	(127/256) x K + $V_{REF}L$
1	0	0	0	0	0	0	0	(128/256) x K + $V_{REF}L$
1	0	0	0	0	0	0	1	(129/256) x K + $V_{REF}L$
⋮								
1	1	1	1	1	1	1	1	(255/256) x K + $V_{REF}L$

MSB A_2	A_1	LSB A_0	DAC UPDATED
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	0	0	DAC E
1	0	1	DAC F
1	1	0	DAC G
1	1	1	DAC H

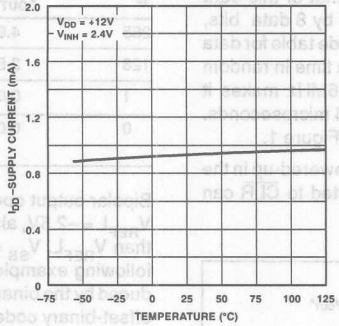
TABLE 3: Logic Control Input Truth Table

CLK	$\overline{CLK}$	INPUT SHIFT REGISTER OPERATON
↑	L	Shift Data
H	↓	Shift Data
L	X	No Operation
X	H	No Operation

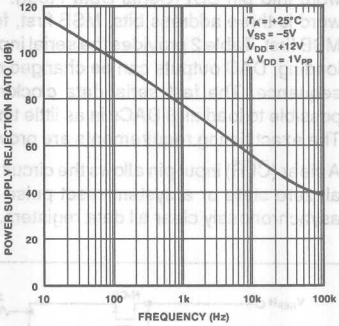
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT CODE



SUPPLY CURRENT vs TEMPERATURE

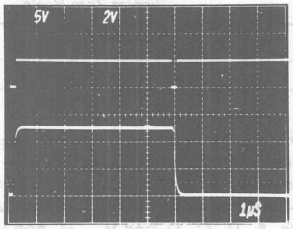


POWER SUPPLY REJECTION RATIO vs FREQUENCY



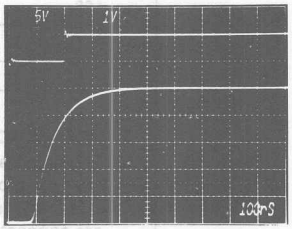
2

DAC OUTPUT SETTLING TIME POSITIVE & NEGATIVE TRANSITIONS



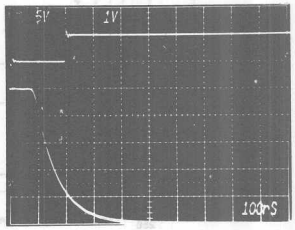
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (2V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME POSITIVE TRANSITION



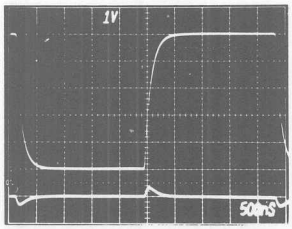
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME NEGATIVE TRANSITION



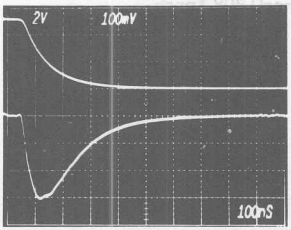
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

DAC OUTPUT CHANNEL-TO-CHANNEL CROSSTALK BOTH TRANSITIONS



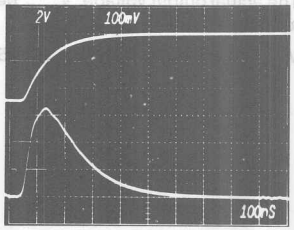
UPPER TRACE: V_{OUT}A 0 TO +5V CHANGE
LOWER TRACE: V_{OUT}B (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK NEGATIVE TRANSITION



UPPER TRACE: V_{OUT}A +5V TO 0V CHANGE
LOWER TRACE: V_{OUT}B (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK POSITIVE TRANSITION



UPPER TRACE: V_{OUT}A 0 TO +5V CHANGE
LOWER TRACE: V_{OUT}B (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

CIRCUIT OPERATION

The DAC-8800 provides a programmable voltage output adjustment capability. Changing the programmed output voltage of each DAC is accomplished by clocking in an 11-bit serial data word into pin SDI (Serial Data Input). The format of this data word is three address bits, MSB first, followed by 8 data bits, MSB first. Table 2 provides the serial input decode table for data loading. DAC outputs can be changed one at a time in random sequence. The fast serial-data clocking of 6.6MHz makes it possible to load all 8 DACs in as little time as 14 microseconds. The exact timing requirements are provided in Figure 1.

A clear ($\overline{CLR}$) input pin allows the circuit to be powered-up in the all zero state or a system reset pulse connected to $\overline{CLR}$ can asynchronously clear all data registers.

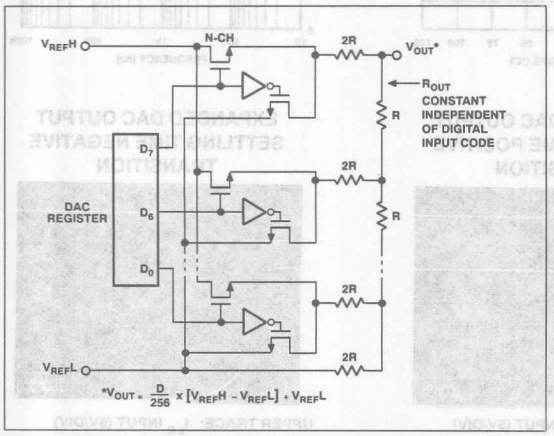


FIGURE 2: *DAC-8800 TrimDAC™ Equivalent DAC Circuit*

The output voltage range is determined by the external input voltages applied to $V_{REF}H$ and $V_{REF}L$. See Figure 2 for a simplified equivalent DAC circuit. If a negative supply is used on V_{SS} then $V_{REF}L$ may be set negative resulting in a programmable bipolar output voltage swing.

The actual output voltage, V_{OUT}, depends on $V_{REF}H$ and $V_{REF}L$ as follows:

$$V_{OUT}(D) = D \times (V_{REF}H - V_{REF}L)/256 + V_{REF}L$$

where D is a whole number binary digital input word loaded into the DAC register. For example, when $V_{REF}H = +5V$ and $V_{REF}L = 0V$ unipolar output operation results with the following binary digital inputs:

D	$V_{OUT}(D)$	$V_{REF}H = +5.00V$; $V_{REF}L = 0V$
255	4.98V	Full-Scale
128	2.50V	Half-Scale
1	0.02V	1 LSB
0	0.00V	Zero-Scale also generated When $\overline{CLR}$ Input Activated

Bipolar output operation is achieved when $V_{REF}H = +2.5V$ and $V_{REF}L = -2.5V$, also note V_{SS} must be equal to or more negative than $V_{REF}L$. $V_{SS} = -5V$ is a good choice for this example. The following example lists the actual bipolar output voltages produced by the binary digital input which would now be considered offset-binary coded:

D	$V_{OUT}(D)$	$V_{REF}H = +2.50V$; $V_{REF}L = -2.50V$
255	2.48V	Positive Full-Scale
129	0.02V	Positive 1 LSB
128	0.00V	Bipolar Zero-Scale
127	–0.02V	Negative 1 LSB
0	–2.50V	Negative Full-Scale

REFERENCE INPUTS ($V_{REF}H_1$, $V_{REF}L_1$, $V_{REF}H_2$, $V_{REF}L_2$)

The external voltages connected to the V_{REF} input pins determine the programmable output voltage ranges of the two sets of four DACs in the DAC-8800. Specifically, $V_{REF}H_1$ and $V_{REF}L_1$ are connected to DACs, A, B, C, D, and $V_{REF}H_2$ and $V_{REF}L_2$ are connected to DACs E, F, G, H.

Inspection of the DAC-8800 equivalent DAC circuit (Figure 2) shows the external $V_{REF}H$ and $V_{REF}L$ inputs connected to the internal DAC switches. During updating, the DAC switches produce transient current flowing from $V_{REF}H$ to $V_{REF}L$. It is recommended to place 0.01µF bypass capacitors across the $V_{REF}H$ and $V_{REF}L$ inputs to minimize the voltage transients.

A wide range of external voltage references can be used subject to the reference input voltage range boundary conditions. First $V_{REF}H$ should always be more positive than $V_{REF}L$. DC voltages are recommended. $V_{REF}L$ can be equal to the negative power supply V_{SS}. This feature results in single supply operation when V_{SS} is at ground. $V_{REF}H$ should not be closer than four volts to V_{DD}. This is due to the DAC-8800 NMOS only DAC switches which will no longer operate properly if $V_{REF}H$ is closer to V_{DD} than four volts. Total unadjusted error degrades when ($V_{DD} - V_{REF}H$) is less than four volts as shown in Figure 3.

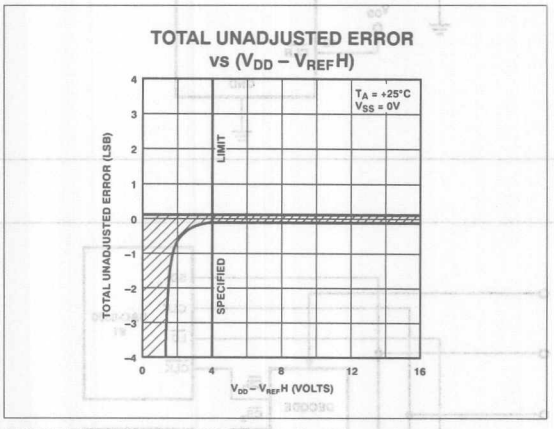


FIGURE 3: *Effect on TUE Operating Beyond ($V_{DD} - V_{REF}H$) > 4V Limit*

RECOMMENDED OPERATING POWER SUPPLY VOLTAGE RANGES

Although the DAC-8800 is thoroughly specified for operation with V_{DD} = +12V and V_{SS} = 0V or–5V, it will still function with the following recommended boundary conditions:

- $(V_{DD} - V_{SS}) < 18V$
- $4.5V < V_{DD} < 16V$
- $0V > V_{SS} > -12V$

In all cases the reference voltage boundary conditions still apply. The boundary conditions described here make it possible to use DAC-8800 with a wide variety of readily available supply voltages. Some choices include, but are not limited to:

V_{DD}/V_{SS} = +15V/0V; +12V/0V; +12V/–5V; +5V/–5V; +5V/–12V

DAC OUTPUTS (V_{OUT} A, B, C, D, E, F, G, H)

The eight D/A converter voltage outputs have a constant output resistance independent of digital input code. The distribution of R_{OUT} from DAC to DAC within the DAC-8800 typically matches by 0.5%. Device to device R_{OUT} matching is process-lot to process-lot dependent having a ±20% variation. The change in R_{OUT} with temperature is very small as a result of PMI's low temperature coefficient SiCr thin-film resistor process.

The nominal DAC output capacitance measures three picofarads and has little variation with temperature.

One aspect of the nominal 12.5kΩ DAC output resistance is channel-to-channel crosstalk. Under a worst case condition of adjacent DAC outputs when DAC A makes a five volt output voltage change DAC B exhibits a 300mV voltage transient. See photograph in typical characteristics section of data sheet.

The channel-to-channel crosstalk is due to the 0.15pF inter-pin package capacitance. A FET probe with 3.4pF input capacitance was used to measure the DAC output channel-to-channel crosstalk characteristics shown. In voltage transient sensitive applications, minimization of crosstalk can be accomplished by placing ground traces between adjacent DAC output pins. DAC output bypass capacitors will also minimize voltage transients.

Output settling time has a dominant pole response as the photograph in the typical characteristics section shows. The output settling time characteristic consists of an 80 nanosecond propagation delay followed by a single RC decay waveform determined by the nominal R_{OUT} of 12.5kΩ times C_{OUT} plus C_{LOAD} which includes the oscilloscope probe.

The digital feedthrough from the serial data inputs (CLK, and SDI) to the DAC outputs measures less than 20mV.

DIGITAL INTERFACING

The DAC-8800 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), load ($\overline{LD}$), and serial data input (SDI). A $\overline{CLK}$ input pin is available for negative edge triggered data loading. The edge sensitive clock input pin requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means.

The logic control input truth table (Table 3) defines operation of the serial data input register.

The CLK input is used to place data in the serial data input register. The unused clock input (CLK or $\overline{CLK}$) should be tied to the active state (CLK = 1 or $\overline{CLK}$ = 0 for active). The load strobe ($\overline{LD}$) which must follow the eleventh active CLK edge transfers the

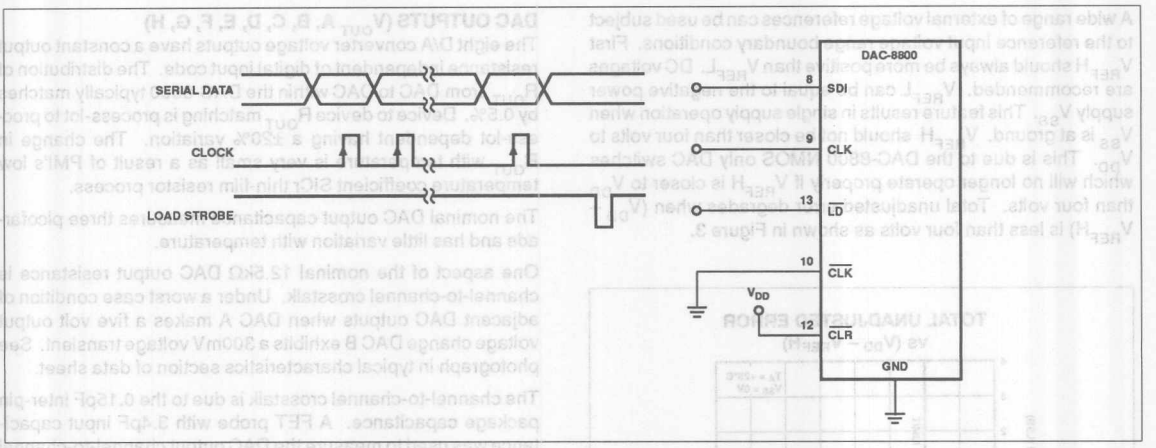


FIGURE 4: *Three-Wire Serial Interface Connections*

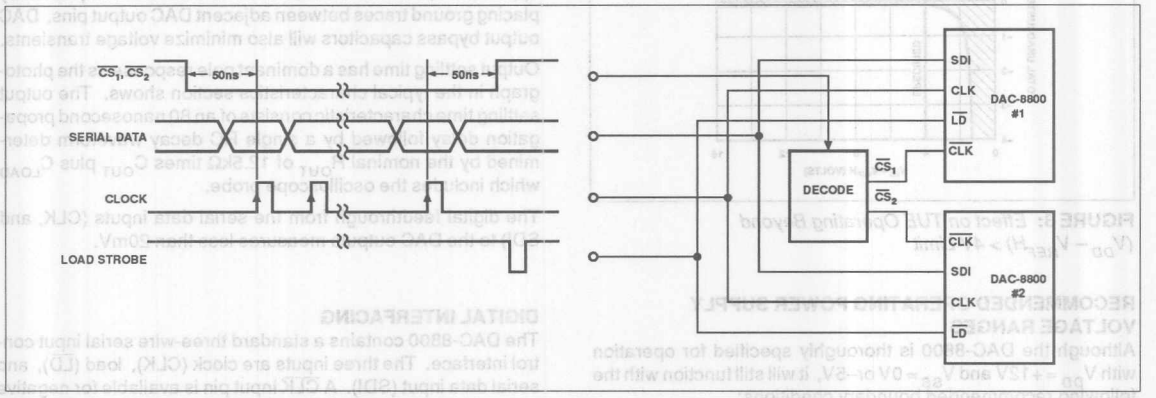


FIGURE 5a: *Decoding Multiple DAC-8800s*

data from the serial data input register to the DAC register decoded from the first three address bits clocked into the input register. Any extra CLK edges after the eleventh edge looses the first bits shifted in. See Table 2 for a complete description. See Figure 4 for an example using the CLK input pin to clock data into the SDI.

The unused clock input of Figure 4 can be used to provide a chip select ($\overline{CS}$) feature for applications using more than one DAC-8800. Figure 5a shows the proper connection and timing of the CLK inputs which assures that the $\overline{CLK}$ acting as a chip select ($\overline{CS}$) is taken to the active low state selecting the desired DAC-8800.

Another method of decoding multiple DAC-8800s is shown in Figure 5b. Here all the DAC serial input registers receive the same input data; however, only one of DAC's $\overline{LD}$ input is activated to transfer its serial input register contents into the destination DAC register. In this circuit the $\overline{LD}$ timing generated by the address decoder should follow the DAC-8800 standard timing requirements. Note the address decoder should not be activated by its $\overline{WR}$ input while the coded address inputs are changing.

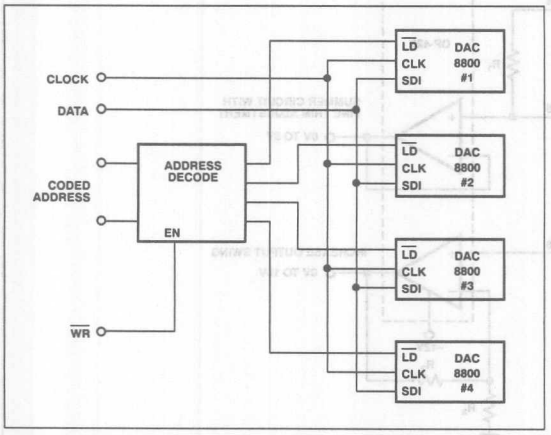


FIGURE 5b: *Decoding Multiple DAC-8800s Using the $\overline{LD}$ Input Pin*

APPLICATIONS

DIGITALLY PROGRAMMABLE AUDIO AMPLIFIER

The DAC-8800 is well suited to digitally control the gain or attenuation settings of eight voltage controlled amplifiers (VCAs). In professional audio mixing consoles, music synthesizers and other audio processor's VCAs, such as the SSM-2014, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of audio level when the slew rate of the analog input control voltage (V_C) is properly chosen. Taking advantage of the 12.5kΩ nominal output resistance of the DAC-8800 it is very easy to control the slew rate of V_{OUT} by appropriate selection of C_{OUT}. Figure 6 shows one channel of a digitally programmable audio amplifier.

The reference high ($V_{REF}H$) and reference low ($V_{REF}L$) input voltages of the DAC-8800 provide a digitally programmable output voltage of –1.2V to +1.2V which is connected to the control voltage (V_C) input terminal of the SSM-2014 VCA. The gain of the SSM-2014 is guaranteed to change from –15dB to + 15dB for 1.2 to –1.2V input V_C voltage. A C_{OUT} of 0.1μF provides a control voltage transition time of 1.2ms which generates a click free change in audio channel gain.

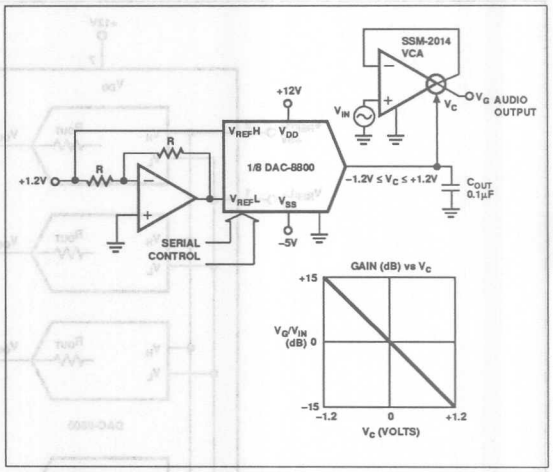


FIGURE 6: *Digitally Programmable Amplifier*

BUFFERING THE DAC-8800 OUTPUT

External op amps can be used to buffer the output of the DAC-8800's nominal 12.5kΩ output resistance. In Figure 7 a variety of possibilities are shown. The quad low power OP-420 is used as a simple buffer to reduce the output resistance of DAC A. The OP-420 was chosen for its wide operating supply range, both single and dual, low power consumption, and low cost.

The next two DACs, B and C, are configured in a summing arrangement where DAC C provides the course output voltage setting and DAC B can be used for fine adjustment. The insertion of R_1 in series with DAC B attenuates its contribution to the voltage sum node at the DAC C output.

DAC D in Figure 7 is in a noninverting gain of two configuration increasing the available output swing to 10V. Appropriate choice of external op amp gain can achieve output voltage swings beyond the range of the DAC-8800 if the external op amp power supply voltages are sufficiently high. In addition, the op amp feedback network termination could be a bias voltage which would provide an offset to the output signal swing.

SETTING COMPARATOR TRIP POINTS

The DAC-8800 is ideal to provide setpoints for voltage input comparators. In Figure 8 the very low power CMP-404 detects whether input voltage (V_{IN}) is higher or lower than the programmed limit values providing TTL compatible output signals. The compactness of the DAC-8800 makes it ideal for high density testing applications found in pin head electronics.

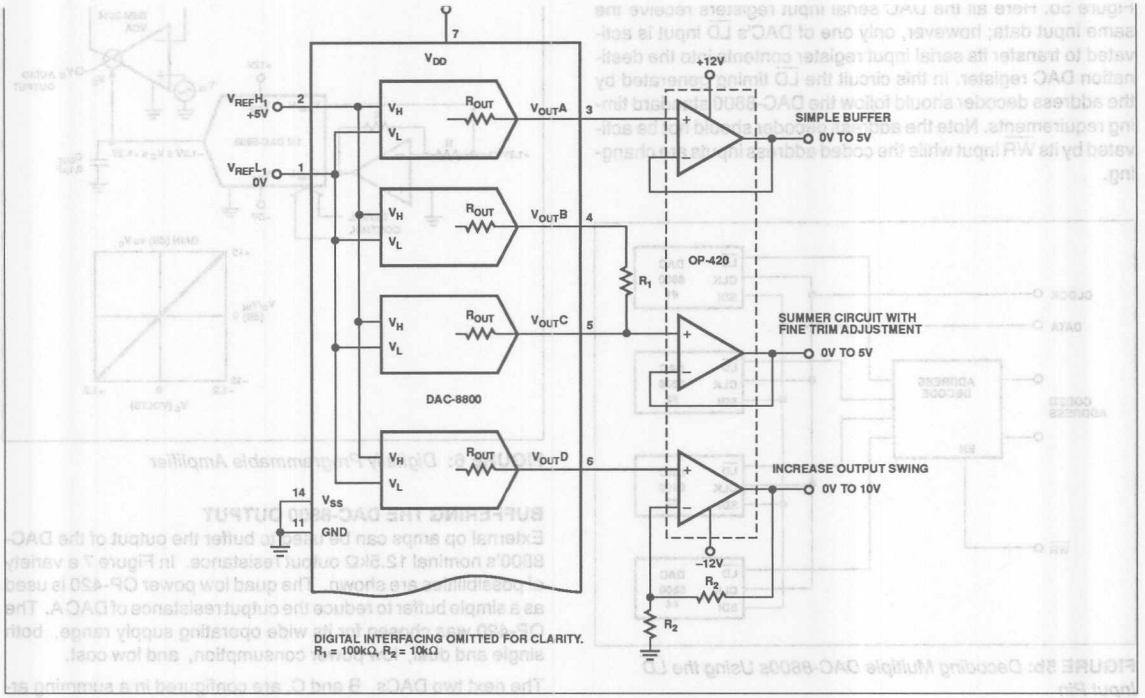


FIGURE 7: *Buffering the DAC-8800 Output*

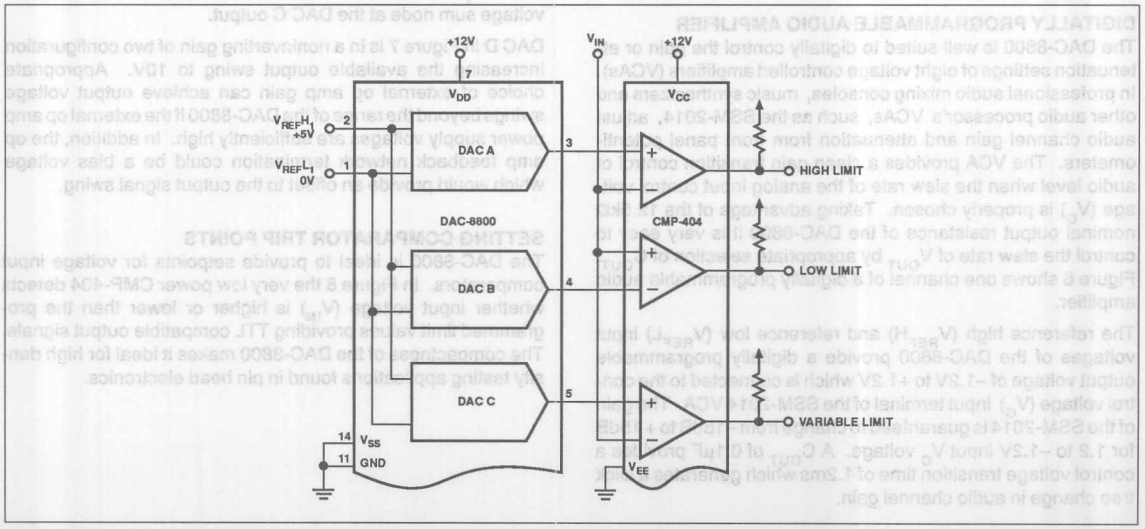


FIGURE 8: *Setting the Comparator Trip Points*

Since the DAC-8800 has a constant output resistance regardless of digital input code, it can be used in a current summing application. Figure 9 depicts the DAC output connected to the inverting input of an OP-20 low power consumption op amp. An external feedback resistor sets the output signal swing according to the formula given. The gain accuracy of this circuit has a wide variation due to the 30% output tolerance of the DAC-8800 R_{OUT} specification. A second DAC in the DAC-8800 could be used with an external resistor summed into the OP-20 current summing node to digitally adjust the full-scale swing.

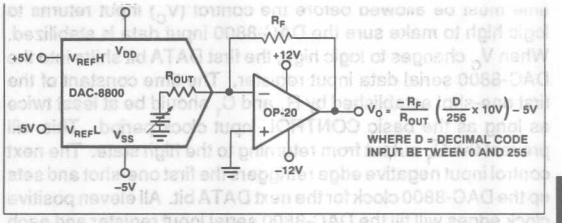


FIGURE 9: *Current Summing Output Operation*

OPTICALLY ISOLATED TWO-WIRE INTERFACE

Two-wire signal interfacing is often found in process control applications where electrical isolation of hazardous environments and minimization of wiring is necessary. Isolation transformers or optocouplers provide the high voltage isolation. Normally the DAC-8800 requires a three-wire interface to update the DAC contents. One technique which translates a two-wire interface into the three-wire signal control required by the DAC-8800 is shown in Figure 10. A single package CMOS-logic dual-retriggerable one-shot MC14538 provides the solution. At rest the optocouplers are both OFF allowing the pull-up resistors to sit at logic high. No undefined transients should occur on the control input line V_C to avoid inadvertently clocking incorrect data into the DAC-8800 serial input register. When it is time to update one of the DAC-8800 DACs, the CONTROL line will go

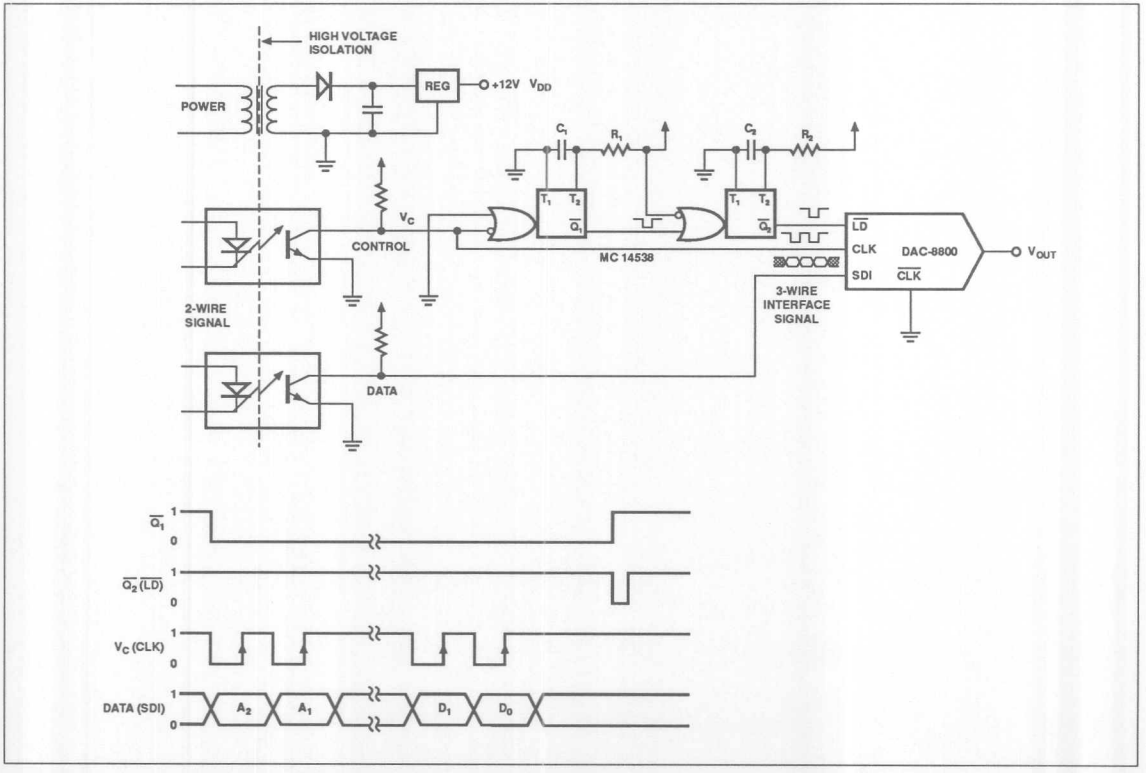
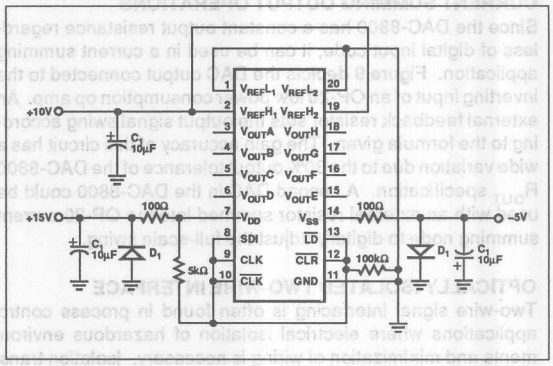


FIGURE 10: *Isolated Two-Wire Signal Interface for Serial Input DAC*

low, triggering the first one-shot ($\overline{Q_1}$). At this time valid data should also be applied to the DATA input optocoupler. Sufficient time must be allowed before the control (V_C) input returns to logic high to make sure the DAC-8800 input data is stabilized. When V_C changes to logic high, the first DATA bit shifts into the DAC-8800 serial data input register. The time constant of the first one-shot established by R_1 and C_1 should be at least twice as long as the basic CONTROL input clock period. This will prevent the $\overline{Q_1}$ output from returning to the high state. The next control input negative edge retriggers the first one-shot and sets up the DAC-8800 clock for the next DATA bit. All eleven positive clock edges will fill the DAC-8800 serial input register and each negative clock edge will retrigger the first one shot. As soon as the CONTROL line returns to the passive state, the first one shot will time out, triggering the second one shot ($\overline{Q_2}$), which will produce the required load $\overline{LD}$ pulse for the DAC-8800 to transfer its serial input register contents to the internal DAC register completing the DAC update. The R_1C_1 and R_2C_2 times need to be designed based on the system's CONTROL-input clock rate. The optocoupler clocking rate must also be considered in setting the system clock rate.

BURN-IN CIRCUIT



8-Bit, Octal, 4-Quadrant Multiplying, CMOS TrimDAC

DAC-8840

2

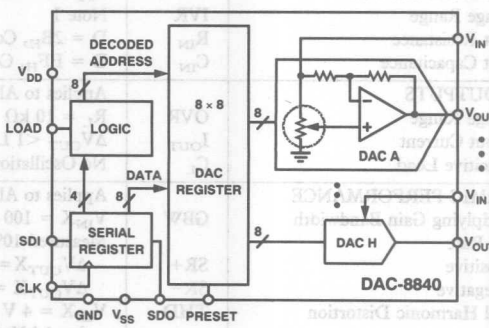
FEATURES

Replaces 8 Potentiometers
1 MHz 4-Quadrant Multiplying Bandwidth
No Signal Inversion
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 Volt Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS

Automatic Adjustment
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8840 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability allows replacement of the mechanical trimmer function in new designs. The DAC-8840 is ideal for ac or dc gain control of up to 1 MHz bandwidth signals. The 4-quadrant multiplying capability is useful for signal inversion and modulation often found in video convergence circuitry.

Internally the DAC-8840 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

The DAC-8840 consumes only 190 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841.

The DAC-8840 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. A separate MIL-STD/883 data sheet for −55°C to +125°C operation is available on request.

DAC-8840—SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic			±1	LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		3	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		10		μV/°C
REFERENCE INPUTS		Applies to All Inputs $V_{IN}X$				
Voltage Range	IVR	Note 1	±3			V
Input Resistance	R_{IN}	D = $2B_H$, Code Dependent	3	6		kΩ
Input Capacitance	C_{IN}	D = FF_H, Code Dependent		19	30	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	±3			V
Output Current	I_{OUT}	ΔV_{OUT} <1 LSB	±5	±10		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p–p	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}X$= +6 V	1.3	4.0		V/μs
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	2.5		V/μs
Total Harmonic Distortion	THD	$V_{IN}X$ = 4 V p–p, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		μV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 0 to FF_H		3.5	6	μs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	80		dB
Digital Feedthrough	Q	V_{INX} = 0 V, D = 0 to 255_{10}		6		nVs
POWER SUPPLIES						
Power Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			190	260	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0002	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS}\rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	μA
Input Capacitance	C_{IL}			7	10	pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V

NOTE
[1]Maximum input voltage is always 2 V less than V_{DD}.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Clock Pulse Width	t_{CH}, t_{CL}	80		ns
Data Setup Time	t_{DS}	40		ns
Data Hold Time	t_{DH}	20		ns
CLK to SDO Propagation Delay	t_{PD}		120	ns
DAC Register Load Pulse Width	t_{LD}	70		ns
Preset Pulse Width	t_{PR}	50		ns
Clock Edge to Load Time	t_{CKLD}	30		ns
Load Edge to Next Clock Edge	t_{LDCK}	60		ns

WAFER TEST LIMITS: (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	DAC8840GBC Limits	Units
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic	±1	LSB max
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H	25	mV max
Input Resistance ($V_{IN}X$)	R_{IN}	D = $2B_H$; Code Dependent	3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	±3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 1 LSB	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +6 V	1.3	V/µs min
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	V/µs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	µA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

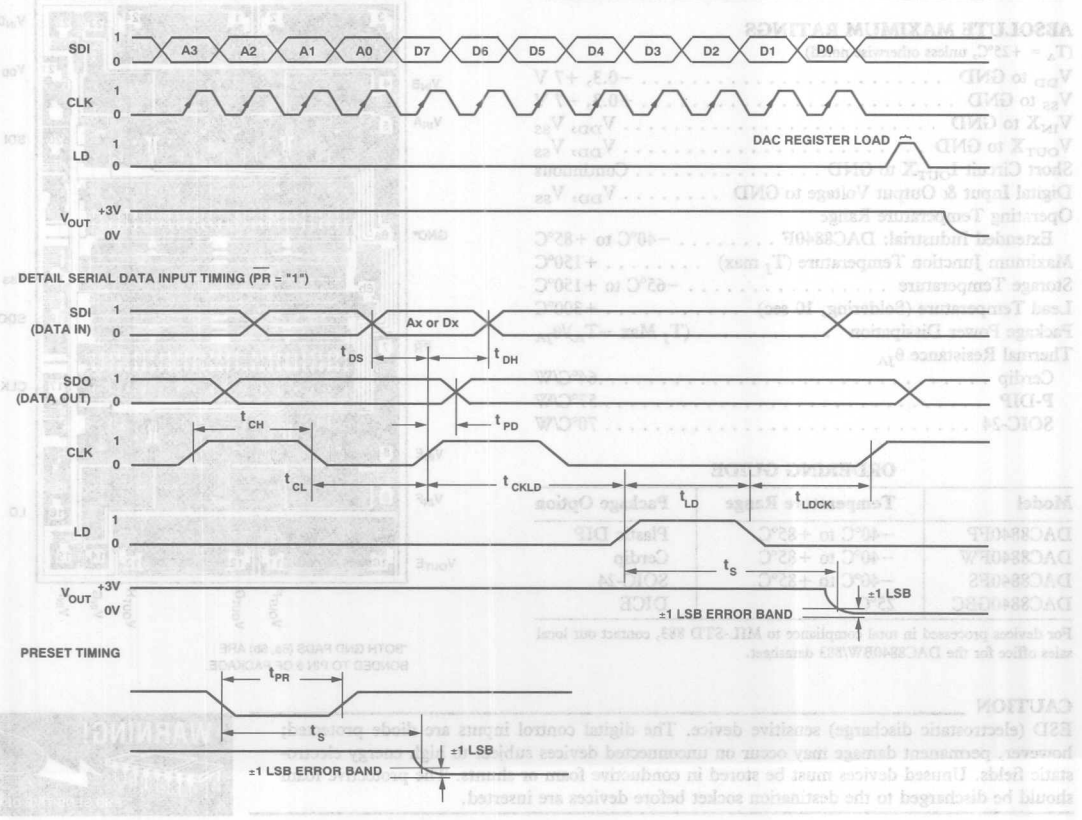
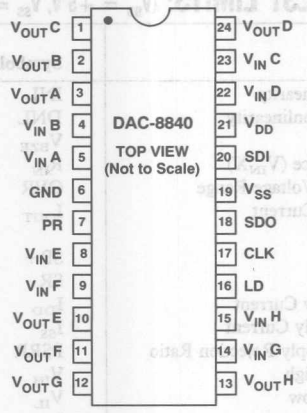


Figure 1. Timing Diagram

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input That Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I.
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . . −0.3, +7 V
V_{SS} to GND . . . . . +0.3, −7 V
$V_{IN}X$ to GND . . . . . V_{DD}, V_{SS}
$V_{OUT}X$ to GND . . . . . V_{DD}, V_{SS}
Short Circuit $I_{OUT}X$ to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}, V_{SS}
Operating Temperature Range
Extended Industrial: DAC8840F . . . . . −40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J Max $-T_A$)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip . . . . . 64°C/W
P-DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C/W

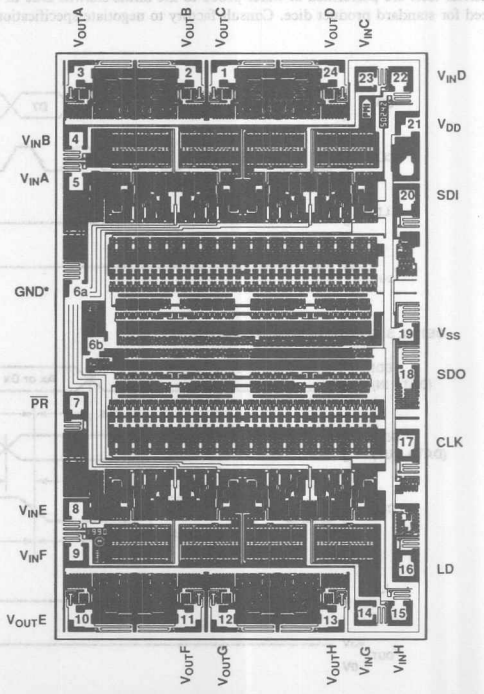
ORDERING GUIDE

Model	Temperature Range	Package Option
DAC8840FP	−40°C to +85°C	Plastic DIP
DAC8840FW	−40°C to +85°C	Cerdip
DAC8840FS	−40°C to +85°C	SOIC-24
DAC8840GBC	25°C	DICE

For devices processed in total compliance to MIL-STD 883, contact our local sales office for the DAC8840BW/883 datasheet.

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.



*BOTH GND PADS (6a, 6b) ARE BONDED TO PIN 6 OF PACKAGE.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



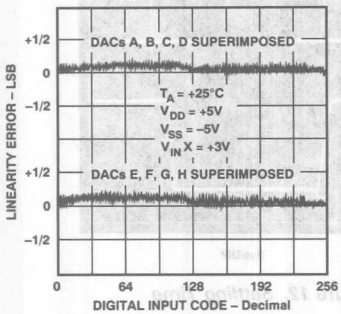


Figure 2. Linearity Error vs. Digital Input Code

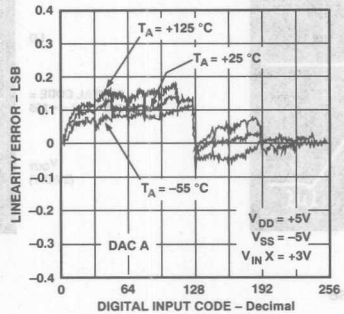


Figure 3. Linearity Error vs. Digital Code vs. Temperature

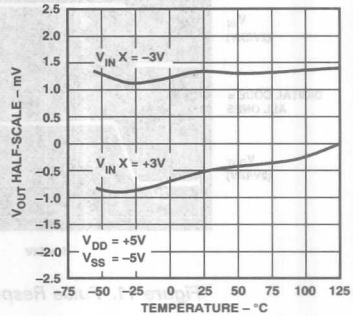


Figure 4. V_{OUT} Half-Scale (80_H) vs. Temperature

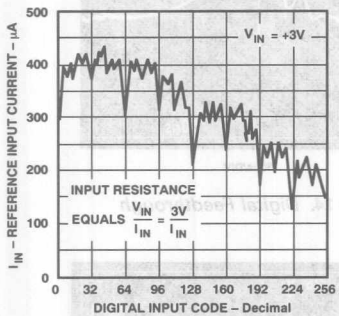


Figure 5. Input Resistance vs. Code

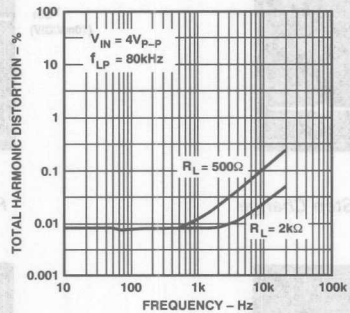


Figure 6. Total Harmonic Distortion vs. Frequency

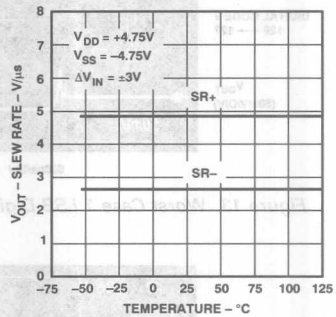


Figure 7. V_{OUT} Slew Rate vs. Temperature

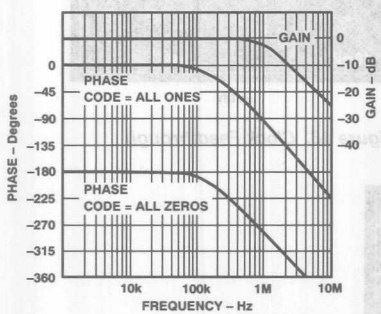


Figure 8. Gain and Phase vs. Frequency (Digital Input = 0 or 255_{10})

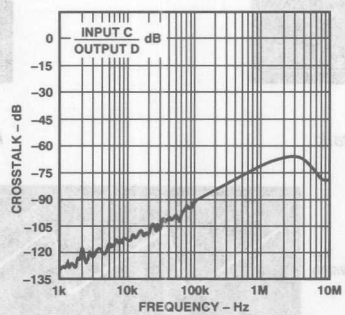


Figure 9. DAC Crosstalk vs. Frequency

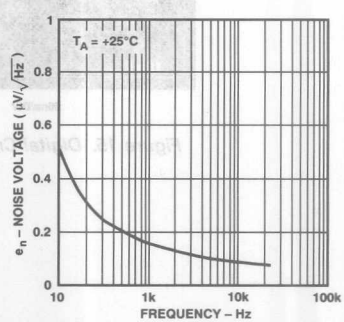


Figure 10. Voltage Noise Density vs. Frequency

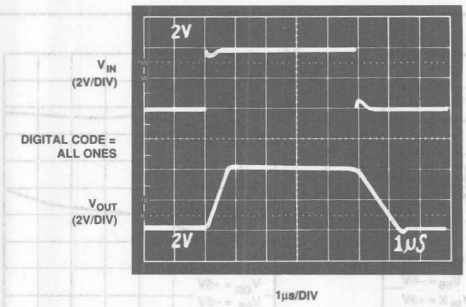


Figure 11. Pulse Response

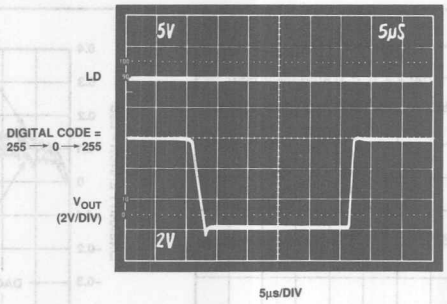


Figure 12. Settling Time

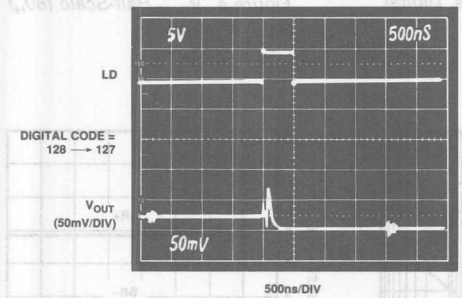


Figure 13. Worst Case 1 LSB Digital Step Change

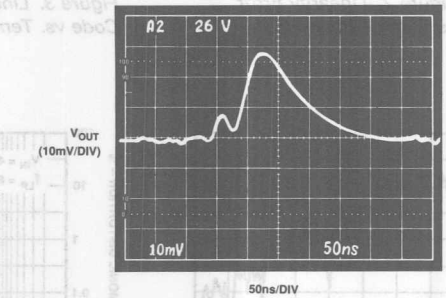


Figure 14. Digital Feedthrough

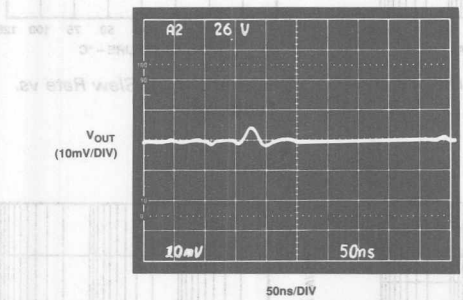


Figure 15. Digital Crosstalk

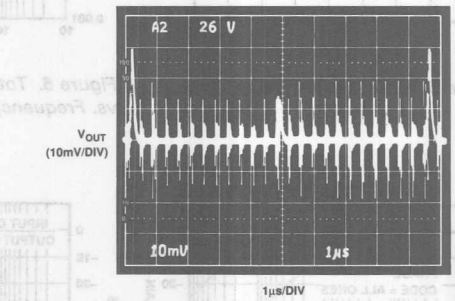


Figure 16. Clock Feedthrough

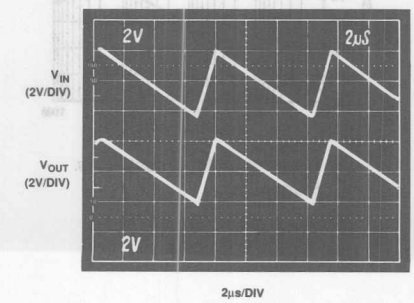


Figure 17. 128 kHz Sawtooth Waveform

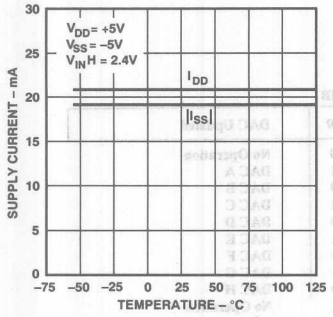


Figure 18. Supply Current vs. Temperature

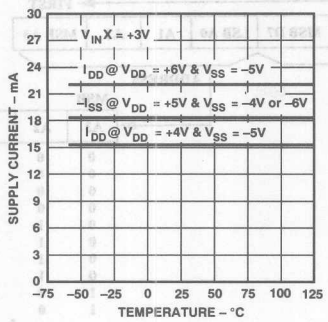


Figure 19. Supply Current vs. Supply Voltage vs. Temperature

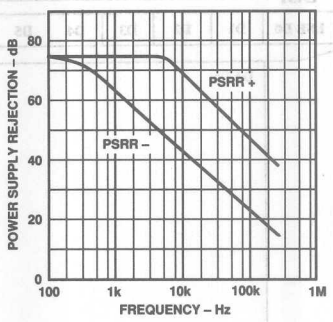


Figure 20. PSRR vs. Frequency

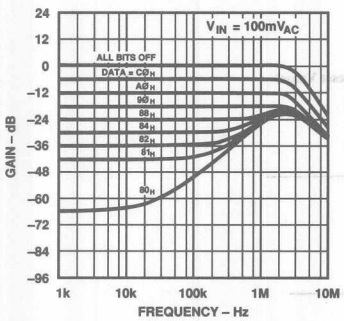


Figure 21. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

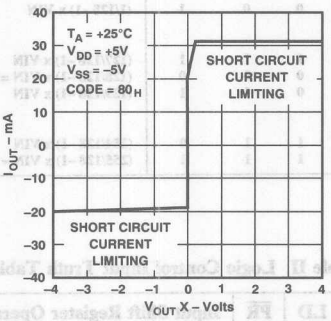


Figure 22. DAC Output Current vs. $V_{OUT}X$

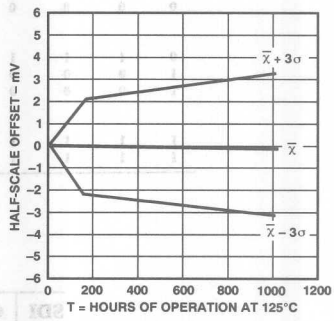


Figure 23. Output Drift Delta Accelerated by Burn-In

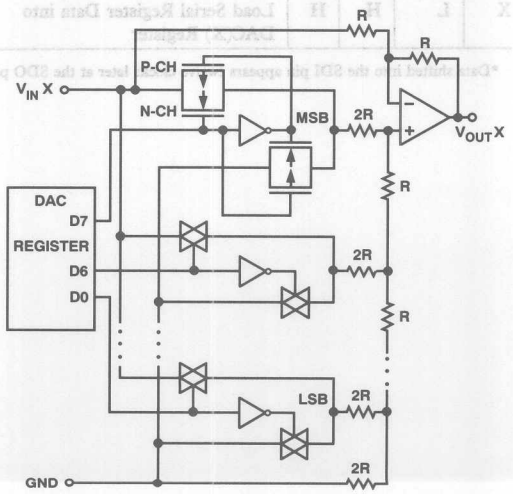
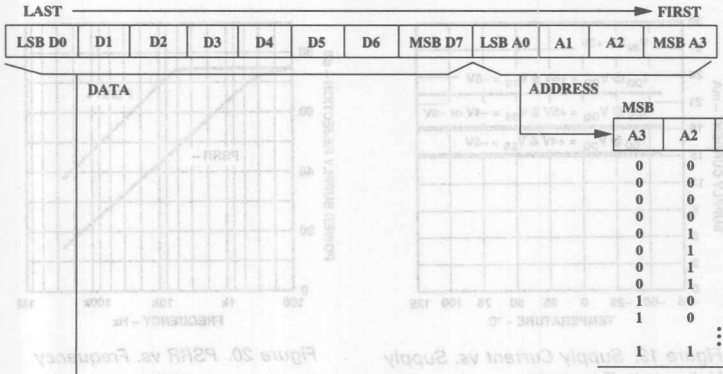


Figure 24. DAC-8840 TrimDAC Equivalent Circuit

Table I. Serial Input Decode



MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
⋮				⋮
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage VOUT = (D/128 –1) x VIN
0	0	0	0	0	0	0	0	–VIN
0	0	0	0	0	0	0	1	(1/128 –1) x VIN
				⋮				
0	1	1	1	1	1	1	1	(127/128 –1) x VIN
1	0	0	0	0	0	0	0	(128/128 –1) x VIN = 0V, (Preset Value)
1	0	0	0	0	0	0	1	(129/128 –1) x VIN
				⋮				
1	1	1	1	1	1	1	0	(254/128 –1) x VIN
1	1	1	1	1	1	1	1	(255/128 –1) x VIN ~ VIN

Table II. Logic Control Input Truth Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X		L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

CIRCUIT OPERATION

The DAC-8840 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of output drive-current to drive external loads. The DAC and amplifier combination shown in Figure 25 produces four-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition, the DAC-8840 provides a 1 MHz gain-bandwidth product in the four-quadrant multiplying channel. Operating from plus and minus 5 V power supplies, analog inputs and outputs of ±3 V are easily accommodated.

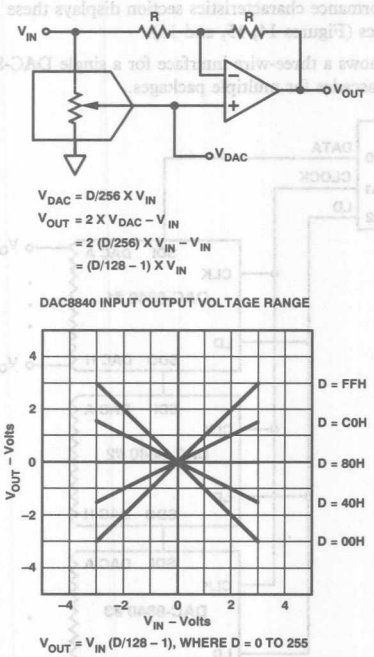


Figure 25. DAC Plus Amplifier Combine to Produce Four Quadrant Multiplication

In order to simplify use with a controlling microprocessor, a simple layout-efficient three-wire serial-data-interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8 bits of data. Using this word combination any DAC register can be changed at a given time without disturbing the other channels. A serial data output SDO pin simplifies cascading multiple DAC-8840s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to zero volts. This asynchronous input pin $\overline{PR}$ can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start general purpose adjustment procedures.

ADJUSTING AC OR DC SIGNAL LEVELS

The four quadrant multiplication operation of the DAC-8840 is shown in Figure 25. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128 - 1) \times V_{IN} \quad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 3V dc input applied to V_{IN} are summarized in this table.

Table III.

Decimal Input (D)	V_{OUT}(D)	Comments (V_{IN} = 3 V)
0	−3.00 V	Inverted FS
1	−2.98	
127	−0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal the input voltage. This is a result of the R-2R ladder DAC architecture chosen. When the DAC register is loaded with 0, the output polarity is inverted and exactly equals the magnitude of the input voltage V_{IN}. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8840. The calculated voltage error would be ±0.023 V (= ±3 V/128).

If V_{IN} is an ac signal such as a sine wave then we can use equation 2 to describe circuit performance.

$$V_{OUT}(t,D) = (D/128 - 1) \times A \sin(\omega t) \quad (2)$$

where $\omega = 2\pi f$, A = sine wave amplitude, and D = decimal input code.

This transfer characteristic Equation 2 lends itself to amplitude and phase control of the incoming signal V_{IN}. When the DAC is loaded with all zeros, the output sine wave is shifted by 180° with respect to the input sine wave. This powerful multiplying capability can be used for a wide variety of modulation, waveform adjustment and amplitude control.

the electrical characteristics table. The graph (Figure 5) titled "Reference Input Current versus Code" shown in the typical performance characteristics section displays the incremental changes. Use a suitable amplifier capable of driving this input resistance in parallel with the specified 19 pF typical input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design (see Figure 24). The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from near the negative supply (V_{SS}) to within 2 V of the positive supply (V_{DD}). That is, the operating input voltage range is:

$$V_{SS} + 0.5\ V < V_{IN}X < (V_{DD}-2\ V) \quad (3)$$

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8840's internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 100 pF. However, in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation.

The low output impedance of the buffers minimizes crosstalk between analog input channels. A graph (Figure 9) of analog crosstalk between channels is provided in the typical performance characteristics section. At 1 MHz, 72 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8840 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8840s.

The Logic Control input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge sensitive input. If mechanical switches are used for breadboarding product evaluation, they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the serial input decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8840 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. The packages not requiring data changes would receive the NOP address, that is, all zeros. It takes 12 clocks on the CLK pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse the processor needs to activate the LD strobe to have the DAC-8840 decode the serial register contents and update the target DAC register with the 8-bit data twelve clock edges, data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels. Measurements of DAC switch feedthrough shown in the electrical characteristics table were accomplished by grounding the $V_{IN}X$ inputs and cycling the data codes between all zeros and all ones. Under this condition 6 nVs of feedthrough was measured on the output of the switched DAC channel. An adjacent channel measured less than 1 nVs of digital crosstalk. The digital feedthrough photographs shown in the typical performance characteristics section displays these characteristics (Figures 14, 15, and 16).

Figure 26 shows a three-wire interface for a single DAC-8840 that easily cascades for multiple packages.

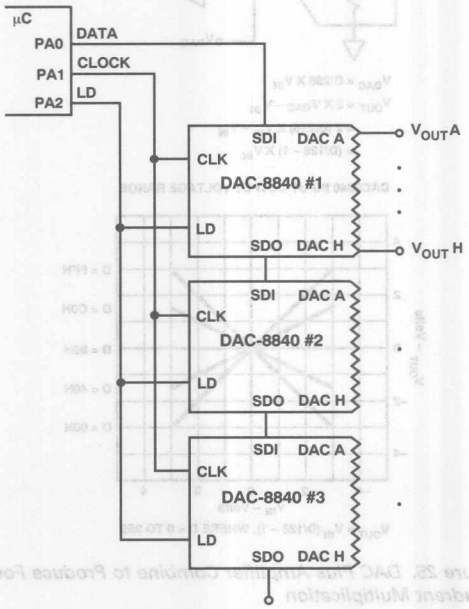
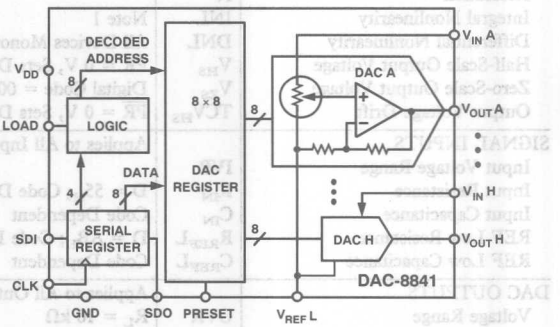


Figure 26. Three-Wire Interface Updates Multiple DAC-8840s

FEATURES
Replaces 8 Potentiometers
Operates From Single +5 V Supply
1 MHz 2-Quadrant Multiplying Bandwidth
No Signal Inversion
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
+3 Volt Output Swing
Midscale Preset
Low 95 mW Power Dissipation

APPLICATIONS
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation
Programmable Gain Amplifiers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8841 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability replaces the mechanical trimmer function in new designs. It is ideal for ac or dc gain control of up to 1 MHz bandwidth signals.

Internally the DAC-8841 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

The DAC-8841 consumes only 95 mW from a +5 V power supply. For dual polarity applications see the DAC-8840 which provides full 4-quadrant-multiplying ±3 V signal capability while operating from ±5 V power supplies.

The DAC-8841 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. For MIL-STD/883 applications, contact ADI sales for the DAC-8841BW/883 data sheet which specifies operation over −55°C to +125°C.

DAC-8841—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0V, T_A = −40°C to +85°C apply for DAC-8841F, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL	Note 1		±1/2	±1.5	LSB
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1			±1	LSB
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475	1.500	1.525	V
Zero-Scale Output Voltage	V_{ZS}	Digital Code = 00_H		20	100	mV
Output Voltage Drift	TCV_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H		10		µV/°C
SIGNAL INPUTS		Applies to All Inputs $V_{IN}X$ or $V_{REF}L$				
Input Voltage Range	IVR		0		1.5	V
Input Resistance	R_{IN}	D = 55_H; Code Dependent	4	10		kΩ
Input Capacitance	C_{IN}	Code Dependent		19	30	pF
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	0.75		kΩ
REF Low Capacitance	$C_{REF}L$	Code Dependent		190	250	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	0		3	V
Output Current	I_{OUT}	ΔV_{OUT} < 25 mV, $V_{IN}X$ = 1.375V, $\overline{PR}$ = 0 V	±5	7		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p–p + 1.0 V dc	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
	+SR	$\Delta V_{OUT}X$ = +3 V	1.3	4.0		V/µs
	−SR	$\Delta V_{OUT}X$ = −3 V	1.3	2.5		V/µs
Total Harmonic Distortion	THD	$V_{IN}X$ = 1 V p–p + 1.0 V dc, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		µV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, 8_{10} to 255_{10}		3.5	6	µs
Channel to Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	70		dB
Digital Feedthrough	Q	$V_{REF}L$ = +1.5 V, D = 0 to FF_H		6		nVs
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			95	130	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V			0.01	%/%
Power Supply Range	PSR	V_{DD}	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}				8	pF
Input Coding				Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS						
Input Clock Pulse Width	t_{CH}, t_{CL}		80			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				120	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTE

[1]INL and DNL tests do not include operation at codes 0 thru 7 due to zero-scale output voltage. For bias voltages above 100 mV on $V_{REF}L$, INL and DNL are maintained over all codes.

Specifications subject to change without notice.

WAFER TEST LIMITS: V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0 V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	DAC-8841GBC Limits	Units
Integral Nonlinearity	INL	Note 1	±1.5	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1	±1	LSB max
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475/1.525	V min/max
Input Resistance ($V_{IN}X$)	R_{IN}	D = 55_H; Code Dependent	4	kΩ min
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 25 mV	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +3 V	1.3	V/µs min
Negative	SR−	$\Delta V_{OUT}X$ = −3 V	1.3	V/µs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	µA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

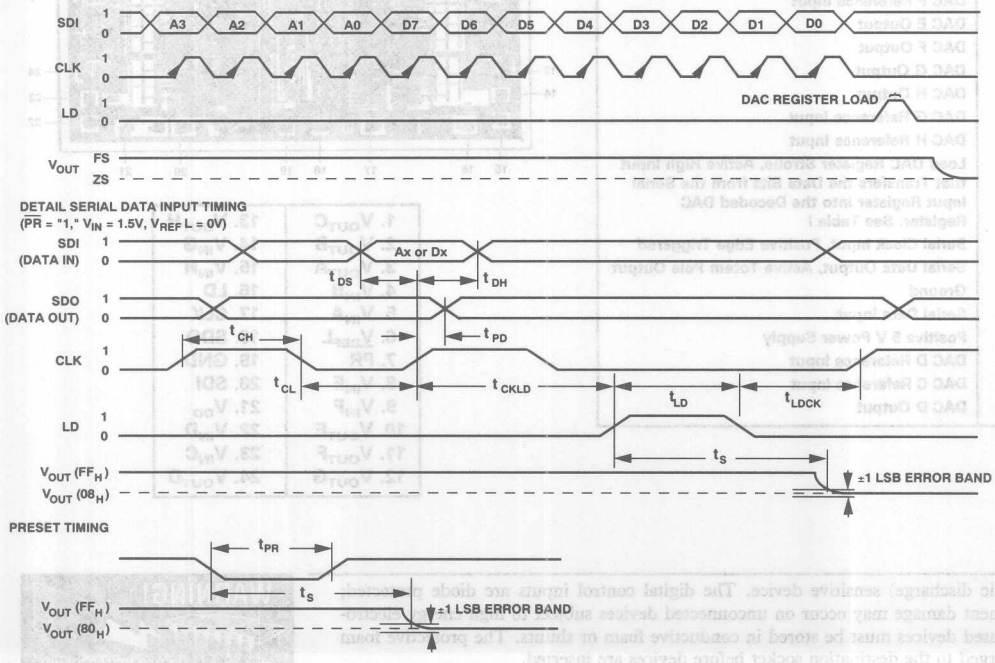


Figure 1. Timing Diagram

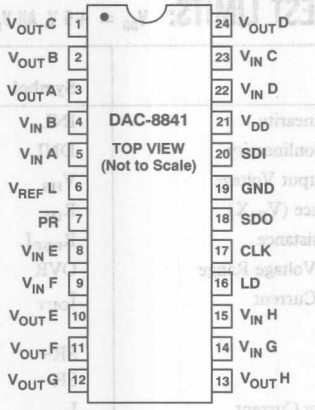
DAC-8841

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . . −0.3 V, +7 V
V_{IN}X to GND . . . . . V_{DD}
V_{REF}L to GND . . . . . V_{DD}
V_{OUT}X to GND . . . . . V_{DD}
Short Circuit I_{OUT}X to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}
Operating Temperature Range
  Extended Industrial: DAC-8841F . . . . . −40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J Max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
  Cerdip . . . . . 64°C/W
  P-DIP . . . . . 57°C/W
  SOIC-24 . . . . . 70°C/W

PIN CONFIGURATIONS

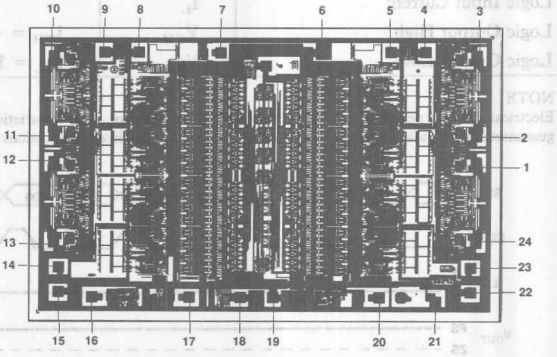


DAC-8841 PIN DESCRIPTION

Pin	Mnemonic	Description
1	V_{OUT}C	DAC C Output
2	V_{OUT}B	DAC B Output
3	V_{OUT}A	DAC A Output
4	V_{IN}B	DAC B Reference Input
5	V_{IN}A	DAC A Reference Input
6	V_{REF}L	DAC Input Reference Low
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	V_{IN}E	DAC E Reference Input
9	V_{IN}F	DAC F Reference Input
10	V_{OUT}E	DAC E Output
11	V_{OUT}F	DAC F Output
12	V_{OUT}G	DAC G Output
13	V_{OUT}H	DAC H Output
14	V_{IN}G	DAC G Reference Input
15	V_{IN}H	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input that Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	GND	Ground
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	V_{IN}D	DAC D Reference Input
23	V_{IN}C	DAC C Reference Input
24	V_{OUT}D	DAC D Output

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.



1. V_{OUT}C	13. V_{OUT}H
2. V_{OUT}B	14. V_{IN}G
3. V_{OUT}A	15. V_{IN}H
4. V_{IN}B	16. LD
5. V_{IN}A	17. CLK
6. V_{REF}L	18. SDO
7. PR	19. GND
8. V_{IN}E	20. SDI
9. V_{IN}F	21. V_{DD}
10. V_{OUT}E	22. V_{IN}D
11. V_{OUT}F	23. V_{IN}C
12. V_{OUT}G	24. V_{OUT}D

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model	Temperature Range	Package Option
DAC8841FP	−40°C to +85°C	Plastic DIP
DAC8841FW	−40°C to +85°C	Cerdip
DAC8841FS	−40°C to +85°C	SOIC
DAC8841GBC	−25°C	Dice

For devices processed in total compliance to MIL-STD 883, contact your local sales office for the DAC8841BW/883 data sheet.

Table I. Serial Input Decode Table

LAST → FIRST

LSB D0	D1	D2	D3	D4	D5	D6	MSB D7	LSB A0	A1	A2	MSB A3

DATA — ADDRESS

MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
⋮				⋮
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage VOUT = D/128 (VIN – VREFL) + VREFL
0	0	0	0	0	0	0	0	VREFL
0	0	0	0	0	0	0	1	1/128 (VIN – VREFL) + VREFL
				⋮				⋮
0	1	1	1	1	1	1	1	127/128 (VIN – VREFL) + VREFL
1	0	0	0	0	0	0	0	VIN (Preset Value)
1	0	0	0	0	0	0	1	129/128 (VIN – VREFL) + VREFL
				⋮				⋮
1	1	1	1	1	1	1	0	254/128 (VIN – VREFL) + VREFL
1	1	1	1	1	1	1	1	255/128 (VIN – VREFL) + VREFL

Table II. Logic Control Input Truth Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X		L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

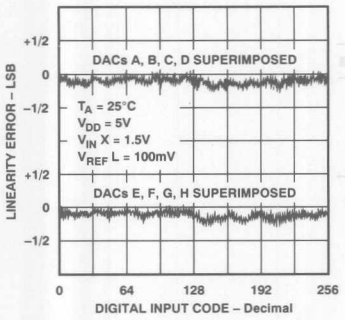


Figure 2. Linearity Error vs. Digital Input Code

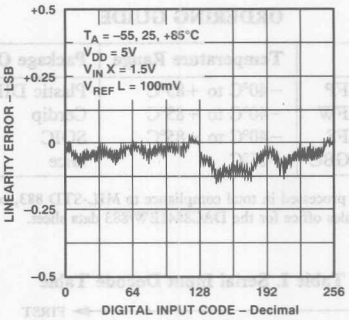


Figure 3. Linearity Error vs. Digital Code vs. Temperature

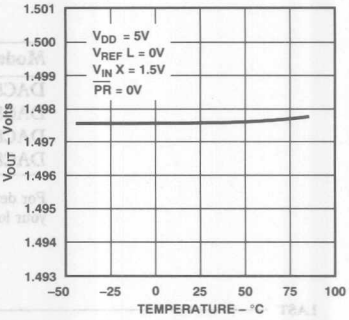


Figure 4. Half Scale vs. Temperature

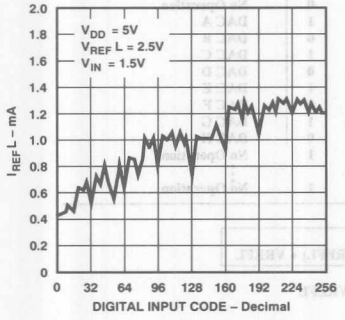


Figure 5. I_{REF}L Input Current vs. Digital Code

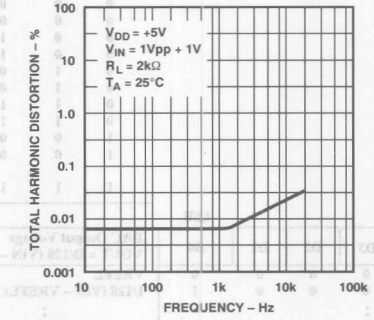


Figure 6. Total Harmonic Distortion vs. Frequency

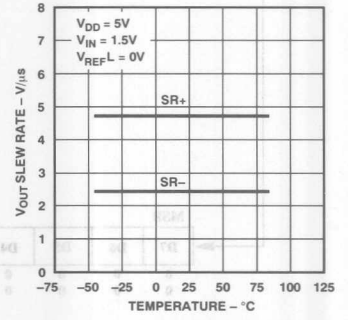


Figure 7. V_{OUT} Slew Rate vs. Temperature

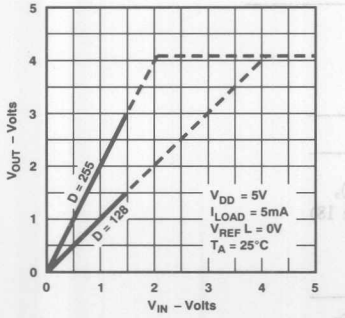


Figure 8. Full-Scale Output to Positive Saturation

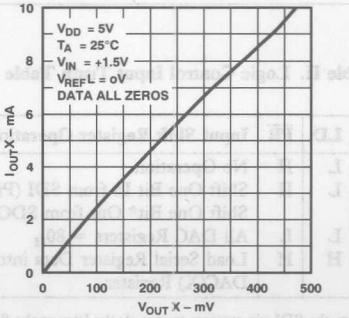


Figure 9. Zero-Scale Output Detail

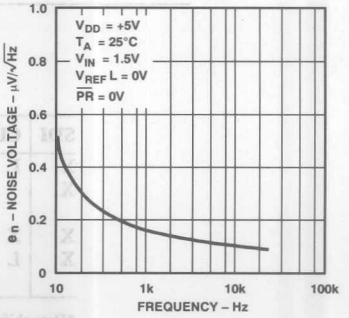


Figure 10. Voltage Noise Density vs. Frequency

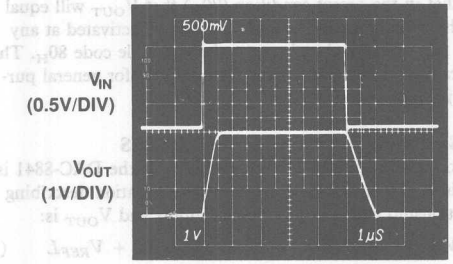
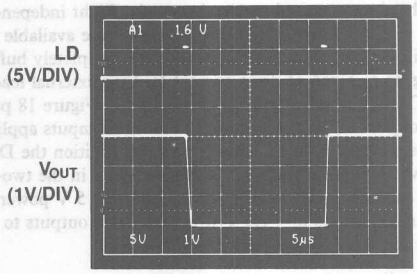
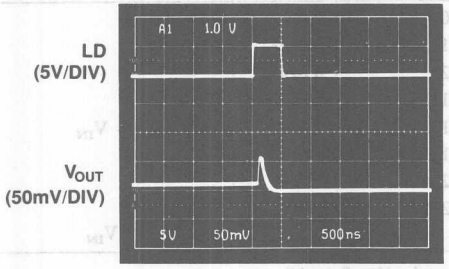


Figure 11. Pulse Response



DIGITAL CODE = 255 → 8 → 255

Figure 12. Settling Time



DIGITAL CODE = 128 → 127

Figure 13. Worst Case 1 LSB Digital Step Change

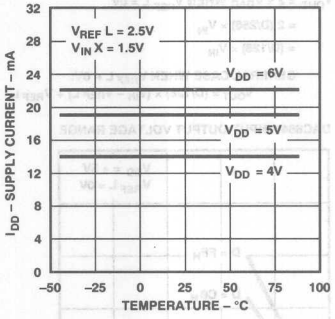


Figure 14. Supply Current vs. Temperature

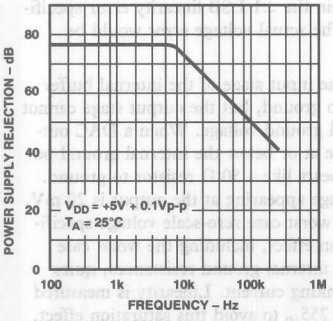


Figure 15. PSRR vs. Frequency

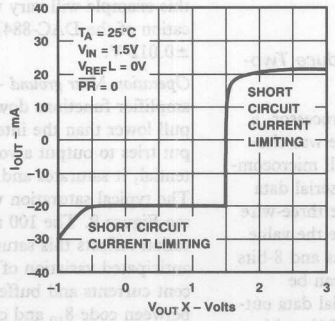


Figure 16. DAC Output Current vs. $V_{OUT}X$

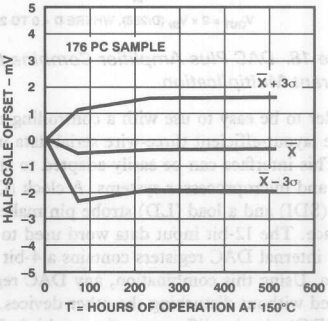


Figure 17. Output Drift Delta Accelerated by Burn-In

CIRCUIT OPERATION

The DAC-8841 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of drive current to drive external loads. The DAC and amplifier combination shown in Figure 18 produces two-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition the DAC-8841 provides a 1 MHz gain-bandwidth product in the two-quadrant multiplying channel. Operating from a 5 V power supply, analog inputs to +1.5 V which generate outputs to +3 V are easily accommodated.

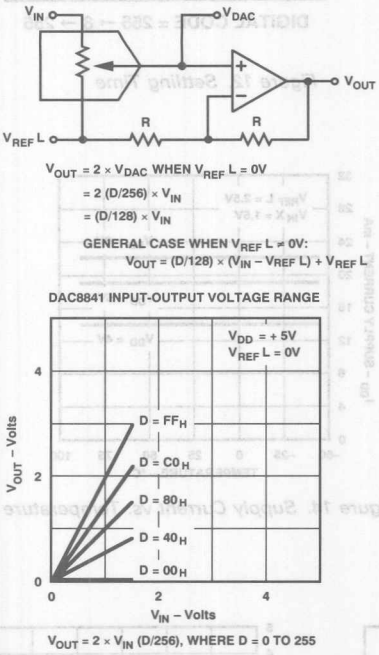


Figure 18. DAC Plus Amplifier Combine to Produce Two-Quadrant Multiplication

In order to be easy to use with a controlling microprocessor, a simple layout-efficient three-wire serial data interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8-bits of data. Using this combination, any DAC register can be changed without disturbing the other devices. A serial data output (SDO) pin simplifies cascading multiple DAC-8841s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to equal half-scale. The transfer equation (1) shows that in the preset condition (80_H) that V_{OUT} will equal V_{IN}. The asynchronous $\overline{PR}$ input pin can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start for general purpose adjustment applications.

ADJUSTING AC OR DC SIGNAL LEVELS

The two-quadrant multiplication operation of the DAC-8841 is shown in Figure 18. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128) \times (V_{IN} - V_{REF}L) + V_{REF}L \qquad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 1.5 V dc input on V_{IN} and $V_{REF}L$ = 0 V are summarized in this table.

Decimal Input (D)	V_{OUT}(D)	Comments (V_{IN} = 1.5 V, $V_{REF}L$ = 0 V)
0	0.000 V*	Zero Scale
1	0.012*	
2	0.024*	
127	1.488	
128	1.500	Half Scale = V_{IN}
129	1.512	
254	2.976	
255	2.988	Full Scale (FS) ≈ 2 × V_{IN}

*See "Operation Near Ground."

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal two times the input voltage. This is a result of the R-2R ladder DAC chosen. When the DAC register is loaded with 0, the output is $V_{REF}L$. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8841. The actual voltage error would be ±0.012 V.

Operation Near ground – The input stage of the internal buffer amplifier functions down to ground, but the output stage cannot pull lower than the internal ground voltage. When a DAC output tries to output a voltage at or below the internal ground potential, it saturates and appears like a 50 Ω resistor to ground. The typical saturation voltage appearing at the output is 20 mV, see Figure 9. The 100 mV worst case zero-scale voltage specification reflects this saturation effect, including the worst case anticipated variation of the internal ground resistances, quiescent currents and buffer sinking current. Linearity is measured between code 8_{10} and code 255_{10} to avoid this saturation effect. In summary, the transfer function of each DAC will be a straight line from code 8 to code 255 when $V_{REF}L$ = 0 V. For input codes 0 to 7, some DAC outputs will be saturated in the zero-scale output voltage region; therefore, changing digital code 0 to 1 may not change the output voltage when $V_{REF}L$ = 0 V.

SIGNAL INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value is specified in the electrical characteristics table. Use a suitable amplifier capable of driving this input resistance in parallel with the specified input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design, see Figure 19. The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from ground (GND) to 1.5 V. That is, the operating input voltage range, when $V_{REF}L = 0$ V, is:

$$0\ V < V_{IN}X < 1.5\ V \tag{2}$$

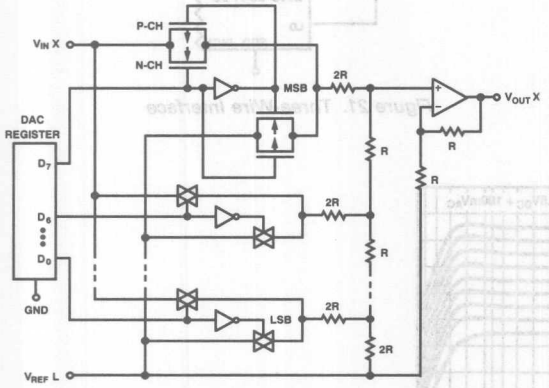


Figure 19. DAC-8841 TrimDAC Equivalent Circuit (One Channel)

The reference inputs can withstand input voltages up to V_{DD}; however due to the internal amplifier's gain of two configuration, the output voltage of the circuit reaches its maximum specified value of 3 V when the input voltage equals 1.5 V and $V_{REF}L = 0$ V; see Figure 18.

The reference low input $V_{REF}L$ is the bottom end of the DAC (see Figure 18). This input is normally tied to ground; however it can be biased above ground. When $V_{REF}L$ is biased above ground, its value and that of $V_{IN}X$ should be chosen in agreement with Equation 3.

$$V_{OUT} \leq V_{DD} - 2\ V \tag{3}$$

Also for the general case the headroom restriction to V_{DD} for $V_{IN}X$ and $V_{REF}L$ is given by Equation 4.

$$V_{IN}X,\ V_{REF}L \leq V_{DD} - 2\ V \tag{4}$$

According to the above equations, the DAC-8841 can only be operated under certain combinations of $V_{IN}X$ and $V_{REF}L$. The shaded area in Figure 20 defines the theoretical allowable ranges of operation. Note that $V_{REF}L$ can be biased higher than $V_{IN}X$. Linearity will vary with the reference voltages and supply conditions. If a symmetrical output ac signal is desired, then the symmetrical ac input on $V_{IN}X$ should be offset to $V_{REF}L$. The output signal will then be with respect to $V_{REF}L$.

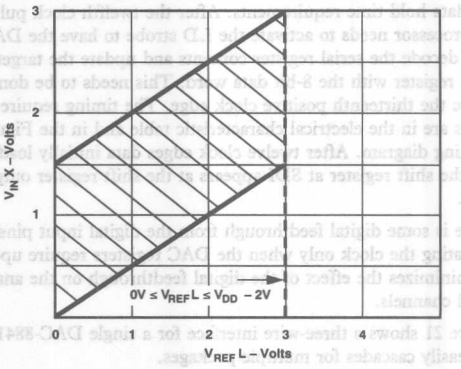


Figure 20. DAC-8841 Input Voltage Operating Boundaries

For example, biasing $V_{REF}L$ equal to one volt would accept a 1 V p–p ac input signal on V_{IN}. This input signal could then be attenuated or given a gain-of-two depending on the DAC data setting.

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8841s internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 200 pF. However in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation. See Figure 16 "DAC output current versus $V_{OUT}X$" graph.

The amplifier output is guaranteed to operate to within 2 V of V_{DD} under all load conditions and temperature. Figure 8 shows typical operation to positive output saturation with a 5 mA load.

The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz 70 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8841 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8841s.

The Logic Control Input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge-sensitive input. If mechanical switches are used for breadboard, product evaluation they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the Serial Input Decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8841 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. It takes 12 clocks on the CLK

and data hold time requirements. After the twelfth clock pulse, the processor needs to activate the LD strobe to have the DAC-8841 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels.

Figure 21 shows a three-wire interface for a single DAC-8841 that easily cascades for multiple packages.

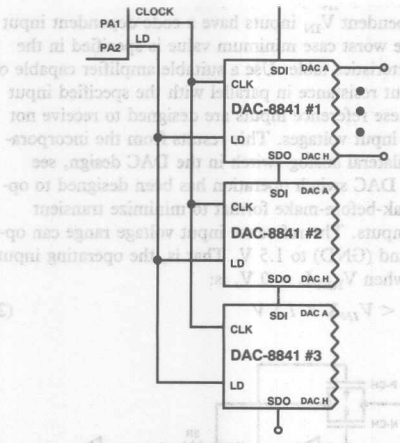


Figure 21. Three-Wire Interface

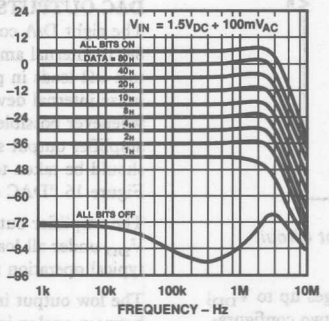


Figure 22. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

12-Bit High-Speed Multiplying D/A Converter

PM-6012

FEATURES

- **Differential Nonlinearity ..... ±1/2LSB**
- **Nonlinearity 0.05%**
- **Fast Settling Time 250ns**
- **High Compliance ..... –5V to +10V**
- **Differential Outputs ..... 0 to 4mA**
- **Guaranteed Monotonicity ..... 12 Bits**
- **Low Full-Scale Tempco ..... 10ppm/°C**
- **Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS**
- **Low Power Consumption 225mW**
- **Industry Standard AM6012 Pinout**

ORDERING INFORMATION †

DNL	PACKAGE: CERDIP 8-PIN	PACKAGE: PLASTIC 20-PIN	OPERATING TEMPERATURE RANGE
±1/2LSB	PM6012ER*		COM
±1LSB	PM6012FR	PM6012HS	XIND
±1LSB	PM6012HR	PM6012HP	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

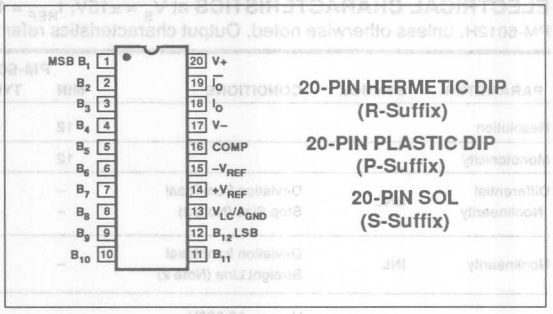
The PM-6012 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commerical operating temperature range.

The PM-6012 combines a 9-bit master D/A converter with a 3-bit (MSBs) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

Continued

PIN CONNECTIONS

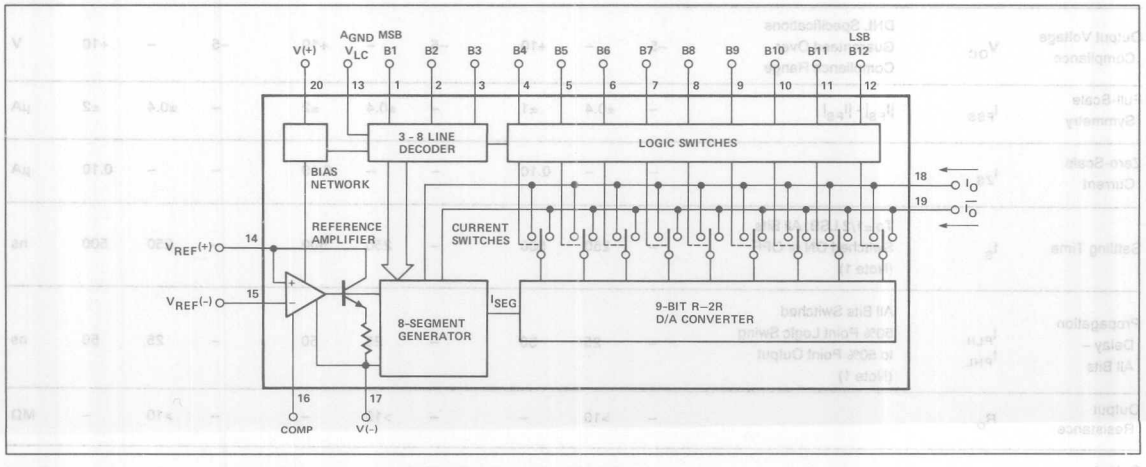


20-PIN HERMETIC DIP (R-Suffix)

20-PIN PLASTIC DIP (P-Suffix)

20-PIN SOL (S-Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639.

GENERAL DESCRIPTION *Continued*

High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the PM-6012 along with an excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/–11V to ±18V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the PM6012 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
- PM-6012E ..... 0°C to +70°C
- PM-6012F, PM-6012H ..... –40°C to +85°C

Junction Temperature ..... –65°C to + 150°C

Storage Temperature (T_j) ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Power Supply Voltage ..... ±18V
Logic Inputs ..... –5V to +18V
Analog Current Outputs ..... –8V to +12V
Reference Inputs V_{14}, V_{15} ..... V– to V+
Reference Input Differential Voltage (V_{14}, V_{15}) ..... ±18V
Reference Input Current(I_{14}) 1.25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 1.0mA, 0°C≤T_A≤70°C for PM-6012E and –40°C≤T_A≤+85°C for PM-6012F, PM-6012H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			PM-6012E			PM-6012F			PM6012H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			12	–	–	12	–	–	12	–	–	Bits
Monotonicity			12	–	–	12	–	–	12	–	–	Bits
Differential Nonlinearity	DNL	Deviation from Ideal Step Size (Note 2)	–	–	±0.0125	–	–	±0.0250	–	–	±0.0250	%FS
			–	–	±0.5	–	–	±1	–	–	±1	LSB
Nonlinearity	INL	Deviation from Ideal Straight Line (Note 2)	–	–	±0.05	–	–	±0.05	–	–	±0.05	%FS
Full-Scale Current	I_{FS}	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ (Note 2)	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}		–	±5	±20	–	±10	±40	–	±80	–	ppm/°C
			–	±0.0005	±0.002	–	±0.001	±0.004	–	±0.008	–	%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specifications Guaranteed Over Compliance Range	–5	–	+10	–5	–	+10	–5	–	+10	V
Full-Scale Symmetry	I_{FSS}	$\|I_{FS}\| - \|\overline{I_{FS}}\|$	–	±0.4	±1	–	±0.4	±2	–	±0.4	±2	µA
Zero-Scale Current	I_{ZS}		–	–	0.10	–	–	0.10	–	–	0.10	µA
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF (Note 1)	–	250	500	–	250	500	–	250	500	ns
Propagation Delay – All Bits	t_{PLH} t_{PHL}	All Bits Switched 50% Point Logic Swing to 50% Point Output (Note 1)	–	25	50	–	25	50	–	25	50	ns
Output Resistance	R_O		–	>10	–	–	>10	–	–	>10	–	MΩ
Output Capacitance	C_{OUT}		–	20	–	–	20	–	–	20	–	pF

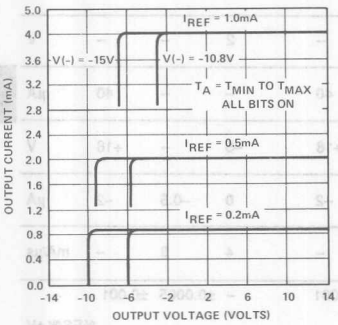
ELECTRICAL CHARACTERISTICS at V_S=±15V, I_{REF}=1.0mA, 0°C≤T_A≤70°C for PM-6012E and –40°C<T_A<+85°C for PM-6012F, PM-6012H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-6012E MIN	PM-6012E TYP	PM-6012E MAX	PM-6012F MIN	PM-6012F TYP	PM-6012F MAX	PM-6012H MIN	PM-6012H TYP	PM-6012H MAX	UNITS
Logic Input Levels "0"	V_{IL}	V_{LC} = GND	–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2	–	–	2	–	–	2	–	–	V
Logic Input Current	I_{IN}	V_{IN} = –5 to +18V	–	–	40	–	–	40	–	–	40	µA
Logic Input Swing	V_{IS}		–5	–	+18	–5	–	+18	–5	–	+18	V
Reference Bias Current	I_{15}		0	–0.5	–2	0	–0.5	–2	0	–0.5	–2	µA
Reference Input Slew Rate	dI/dt	$R_{14(eq)}$ = 800Ω C_C = 0pF (Note 1)	4	8	–	4	8	–	4	8	–	mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = +13.5V to +16.5V, V– = –15V V– = –13.5V to –16.5V, V+ = +15V	– ±0.0002	±0.0005 ±0.001	±0.001	– ±0.00025	±0.0005 ±0.001	±0.001	– ±0.00025	±0.0005 ±0.001	±0.001	%FS/%ΔV
Power Supply Range	V+ V–	V_{OUT} = 0V	4.5 –18	–	18 –10.8	4.5 –18	–	18 –10.8	4.5 –18	–	18 –10.8	V
Power Supply Current	I+ I– I+ I–	V+ = +5V, V– = –15V V+ = +15V, V– = –15V	– – – –	3.3 –13.9 3.9 –13.9	7 –18 7 –18	– – – –	3.3 –13.9 3.9 –13.9	7 –18 7 –18	– – – –	3.3 –13.9 3.9 13.9	7 –18 7 –18	mA
Power Dissipation	P_d	V+ = +5V, V– = –15V V+ = +15V, V– = –15V	– –	225 267	305 375	– –	225 267	305 375	– –	225 267	305 375	mW

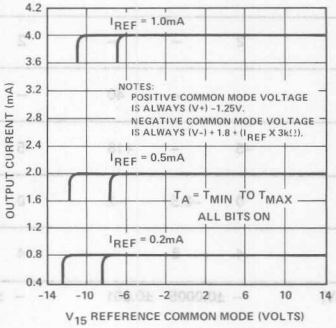
NOTES:
1. Guaranteed by design.
2. T_A = 25°c for PM-6012H grade only.

TYPICAL PERFORMANCE CHARACTERISTICS

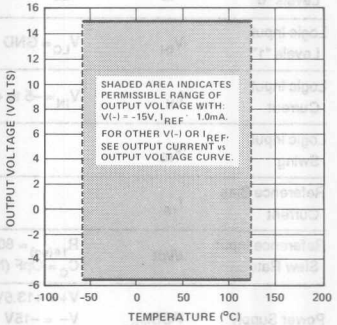
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



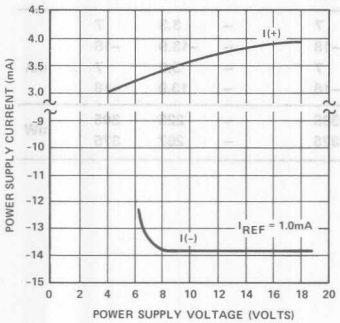
REFERENCE AMPLIFIER COMMON-MODE RANGE



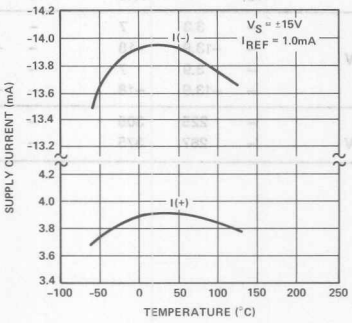
OUTPUT COMPLIANCE vs TEMPERATURE



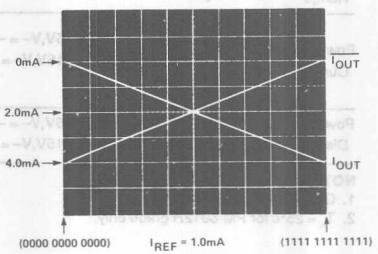
POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



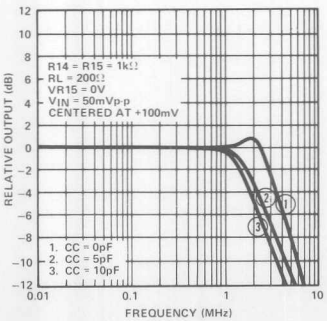
POWER SUPPLY CURRENT vs TEMPERATURE



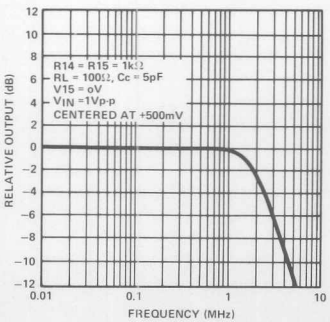
TRUE AND COMPLEMENTARY OUTPUT OPERATION



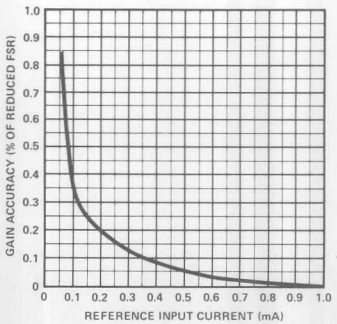
REFERENCE AMPLIFIER SMALL-SIGNAL FREQUENCY RESPONSE



REFERENCE AMPLIFIER LARGE-SIGNAL FREQUENCY RESPONSE

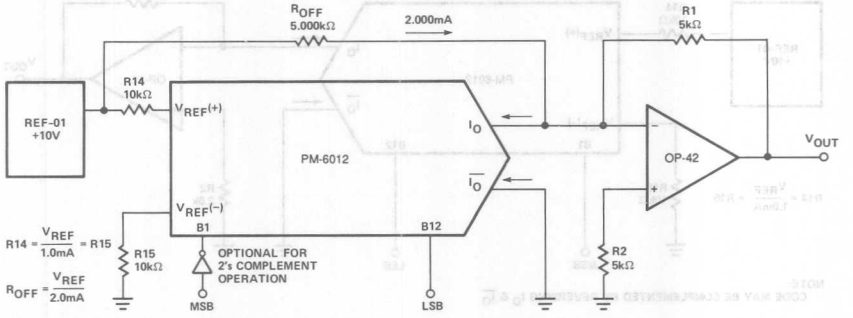


GAIN ACCURACY vs REFERENCE CURRENT



BASIC CONNECTIONS

BIPOLAR OFFSET (TRUE ZERO)

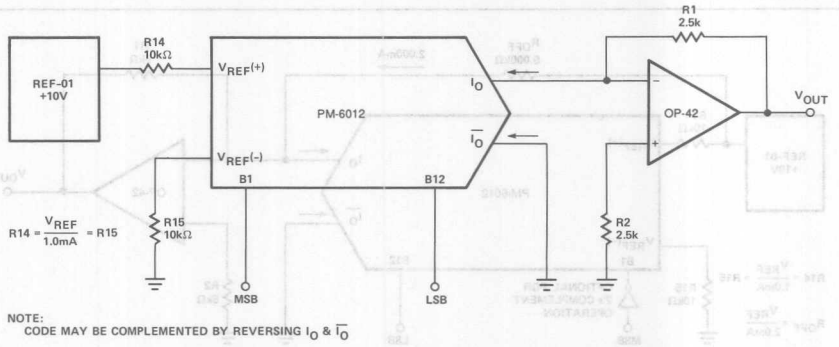


NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Offset binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output.	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	– LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
	Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
	Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000
2's complement;	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
MSB complemented	+ 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
(need inverter at B1).	Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	– 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
	Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
	Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000

BASIC CONNECTIONS

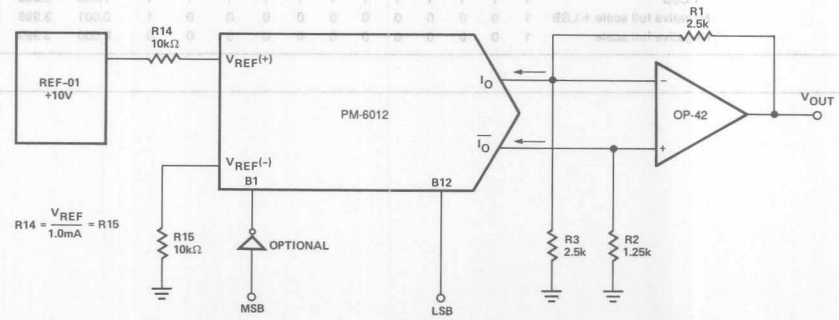
BASIC UNIPOLAR OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
unipolar with true input	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
code, true zero output.	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary binary;	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
unipolar with	Positive full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
complementary input	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
code, true zero output.	Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION



CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight offset binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
	Negative full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
1's complement;	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output	(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
MSB complemented	(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
(need inverter at B1).	Negative full scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The PM-6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = I_{REF}$$

Where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $+V_{REF}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $-V_{REF}$ at pin 15. Reference current flows from ground through R_{14} into $+V_{REF}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin14 is equal to and tracks the voltage at pin15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM}– = V– plus (I_{REF} x 3kΩ) plus 1.23V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1µF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01µF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The PM-6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1µA. Monotonic operation is maintained over a typical range of I_{REF} from 100µA to 1.0 mA. Although some degradation of gain accuracy will be realized at reduced values of I_{REF} (see Gain Accuracy vs. Reference Current graph).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14 for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5,10 and 25pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/µs enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/µs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

For V– = –15V, the logic inputs may swing between –5 and +10V. This enables direct interface with +15V CMOS logic, even when the PM-6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} x 3kΩ) plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 13. When interfacing ECL, an I_{REF} ≤ 1mA is recommended. For general setup of the logic control circuit, it should be noted that pin 13 will sink 7mA typical; external circuitry should be designed to accommodate this current.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V– and is independent of the positive supply. Negative compliance is +10 above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The PM-6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with I_{REF} = 1mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however, at least 8V total must be applied to ensure turn-on of the internal bias network.

Symmetrical supplies are not required, as the PM-6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to ensure logic swings, etc., remain between acceptable limits.

SETTLING TIME

The PM-6012 is capable of extremely fast settling times, typically 250ns at I_{REF} = 1.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the PM-6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if RL > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

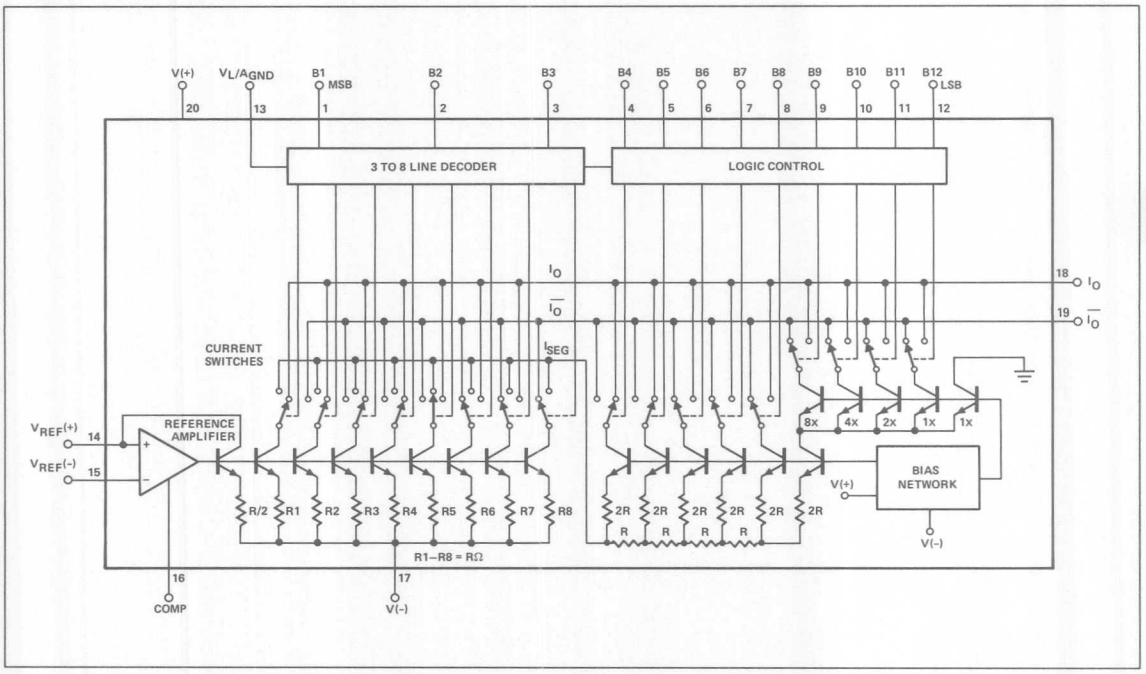
Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

DESCRIPTION OF OPERATION

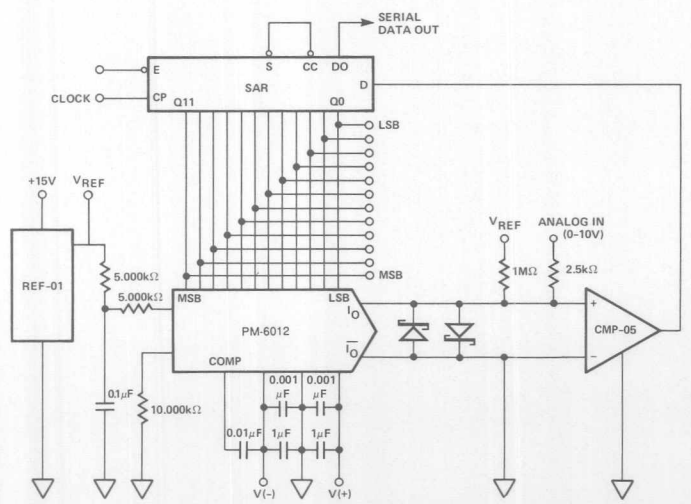
The PM-6012 is divided into two major sections, an 8-segment generator and a 9-bit master/slave D/A converter. In operation the device performs as follows (see Simplified Schematic).

The three most significant bits (MSBs) are inputs to a 3-to-8 line decoder. The selected resistor (R_5 in the figure) is connected to the master/slave 9-bit D/A converter. All lower order resistors (R_1 through R_4) are summed into the I_O line, while all higher order resistors (R_6 through R_8) are summed into the $\overline{I_O}$ line. The R_5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or $\overline{I_O}$ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2mA (4 x 0.5mA/segment) +0.375mA (from master/slave D/A converter) are summed into I_O giving an I_O of 2.375mA. $\overline{I_O}$ has a current of 1.625mA with this code. As the three MSBs are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from $\overline{I_O}$, with the selected resistor feeding its current to the master/slave D/A converter; thus each increment of the 3 MSBs allows the current in the 9-bit D/A converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

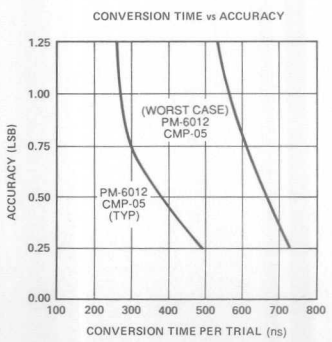
SIMPLIFIED SCHEMATIC



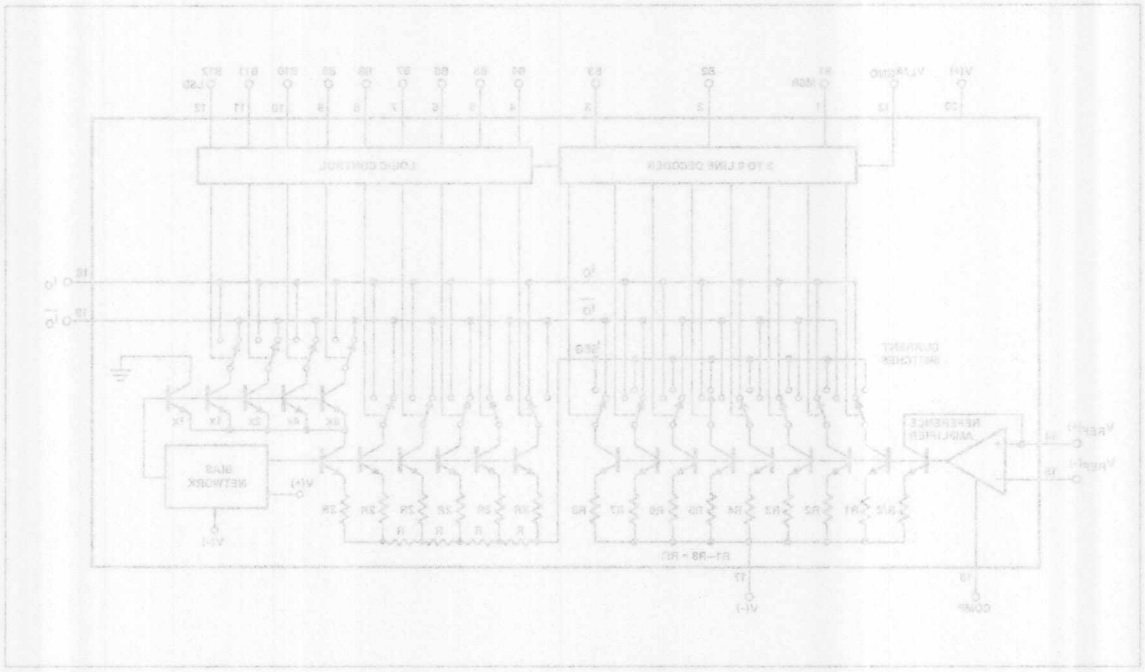
12-BIT FAST A/D CONVERTER

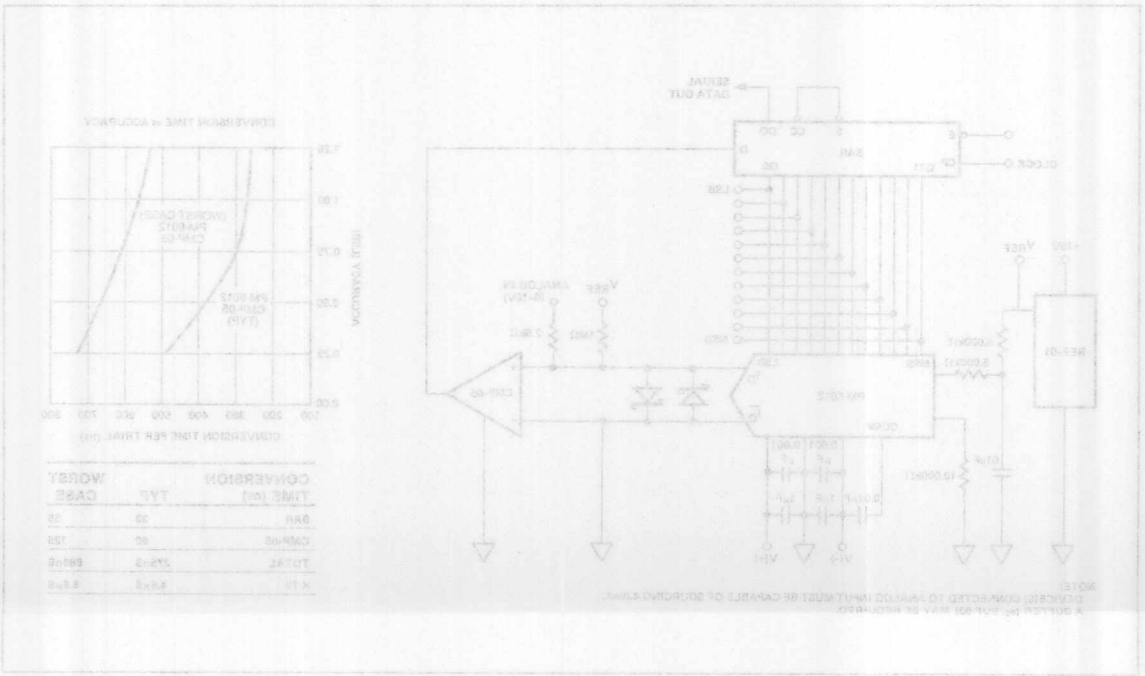


NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375nS	680nS
× 13	4.9μS	8.8μS

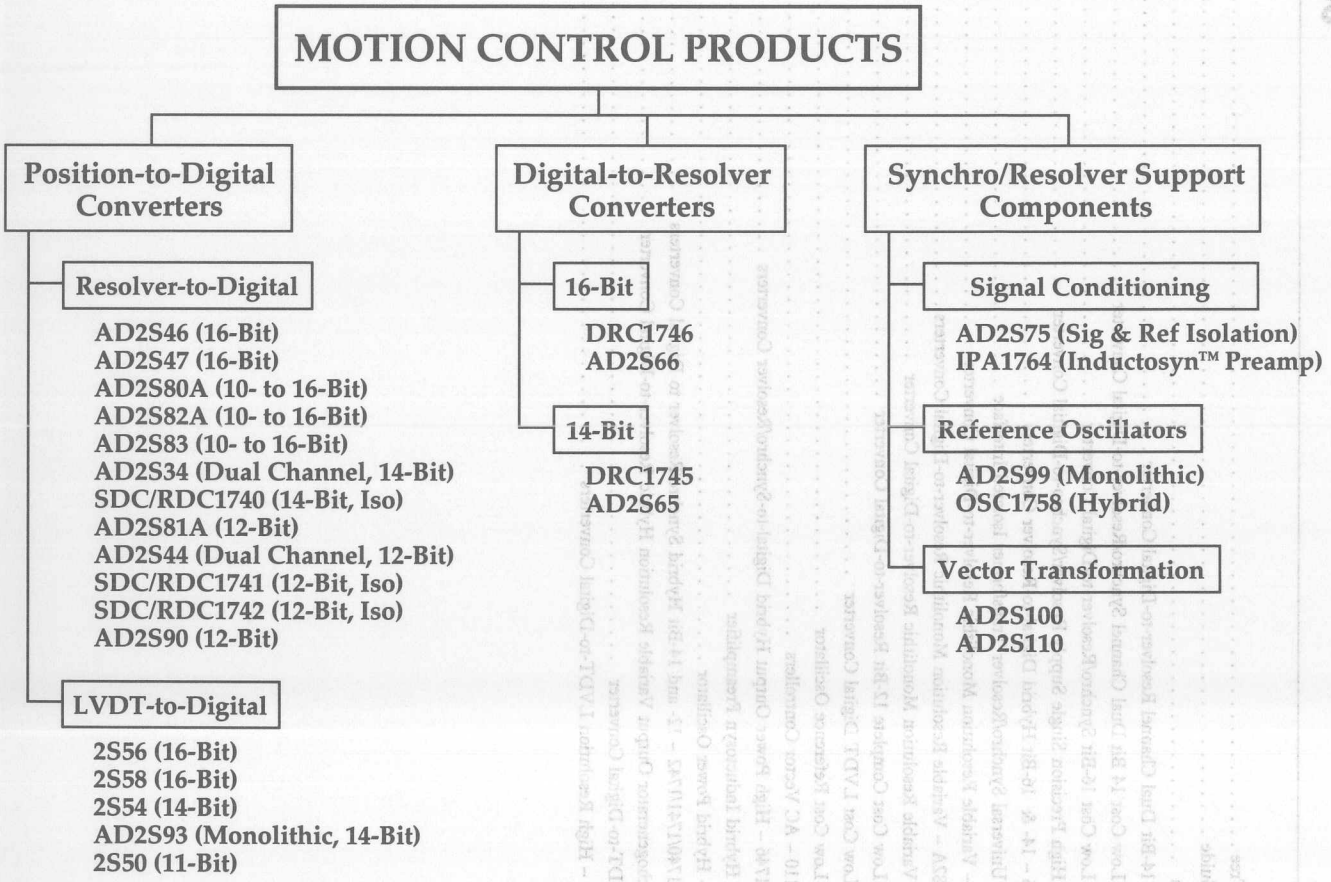




S/D Converters
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Selection Tree
S/D Converters



Selection Guide
Synchro and Resolver Converters

Digital-to-Synchro and Resolver Converters

Model	Res Bits	Output Format[1]	Accuracy arc mins	Load Driving Capability	Reference Frequency Options Hz	Reference Input Volt Options V rms	Signal Output Volt Options V rms	Transformer Output Isolations	Package Options[2]	Temp Range[3]	Page	Comments
DRC1745	14	R[4]	±2, ±4[5]	2.0VA[6]	dc→2600	0→3.4	0→6.8	Use Ext. STM 1680 and STM 1683 Transformer	8	M	C I 3–107	Digital-to-Resolver Converter with Int. 2 VA Power Amplifier. Optional Int. TransZorb† Protection. 2 Byte Latched Inputs
*AD2S65	14	R	±2, ±4[5]	–	dc→2600	0→3.4	0→6.8	–	8	C, M	C I 3–35	Digital-to-Resolver Converter. Autonulling (AN) Option
DRC1746	16	R[4]	±2, ±4[5]	2.0VA[6]	dc→2600	0→3.4	0→6.8	Use Ext. STM 1680 and STM 1683 Transformer	8	M	C I 3–107	16-Bit Version of DRC1745
*AD2S66	16	R	±1, ±2, ±4[5]	–	dc→2600	0→3.4	0→6.8	–	8	C, M	C I 3–35	Digital-to-Resolver Converter. Autonulling (AN) Option

Motor Control

Model	Description	Package Options[2]	Temp Range[3]	Page	Comments
*AD2S100	AC Vector Controller	15	I	C I 3–105	Vector Coordinate Transformation, 15 arc min, 2 µs Settling Time

Synchro/Resolver Support Components

Model	Description	Package Options[2]	Temp Range[3]	Page	Comments
*AD2S75	Signal and Reference Isolation for AD2S80/81/82	8	C, M	C I 3–43	56–20,000 Hz Freq, 11.8–115 V rms Ref, 11.8/26/90 V rms Input
*AD2S99	Monolithic Sine Wave Oscillator Reference	5	I	C I 3–101	2.0–20 kHz Frequency range, Phase Shift Compensation
*OSC1758	Hybrid Sine/Cosine Power Oscillator	8	C, M	C I 3–117	0.0–10 kHz Frequency Range, In-phase and Quadrature Outputs, 1.5 W Output Power
*IPA1764	Inductosyn Preamplifier	8	C, M	C I 3–115	Gain of 1250 ±5%

[1]S = Synchro; R = Resolver; I = Inductosyn.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[4]Synchro format output with external output transformer STM1683.
[5]Depends on option.
[6]Can be used with pulsating power supply for reduced dissipation.
Boldface type: product recommended for new design.
*New product since the publication of the most recent Databooks.
†TransZorb is a trademark of General Semiconductor Industries, Inc.

Selection Guide
Synchro and Resolver Converters

Synchro, Resolver, Inductosyn† and LVDT-to-Digital Converters

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Range[4]	Page	Comments
SDC/RDC1741	12	S, R	±15.3	18	400, 2.6 k	Yes	8	C, M	C I 3–119	Tristate, Latched Output Internal Transformer Isolation
SDC/RDC1742	12	S, R	±8.5	18	400, 2.6 k	Yes	8	C, M	C I 3–119	Tristate, Latched Output Internal Transformer Isolation
*AD2S81A[5]	12	I, R	±30[6]	260	400→20 k	No	1	C	C I 3–71	Monolithic, User Selectable Dynamic Characteristics, High Tracking Rate, Quality Velocity Output, Class 2 ESD
SDC/RDC1740	14	S, R	±5.3	12	400, 2.6 k	Yes	8	C, M	C I 3–119	Tristate, Latched Output Internal Transformer Isolation
2S54	14	LVDT	±0.006[7]	360 LSB/ms[8]	360→5 k	No	8	C, M	C I 3–137	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
2S56	16	LVDT	±0.006[6]	360 LSB/ms[8]	360→5 k	No	8	C, M	C I 3–137	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
2S58	16	LVDT	±0.003[7]	680 LSB/ms[8]	7 k→11 k	No	8	C, M	C I 3–137	Direct Ratiometric Conversion of LVDT Signal, High Gain, Ultra-Linear
*AD2S80A[5]	16, 14, 12, 10[9]	I, R	±2, ±4, ±8	1040[10]	50–20 k	No	1, 4	C, I, M	C I 3–55	Monolithic, User Selectable Dynamic Characteristics, and Resolution High Tracking Rate and Quality Velocity Output, Class 2 ESD
*AD2S82A[5]	16, 14, 12, 10[7]	I, R	±2, ±4, ±8	1040[10]	50–20 k	No	5	C	C I 3–71	Monolithic, User Selectable Dynamic Characteristics, and Resolution High Tracking Rate and Quality Velocity Output, Class 2 ESD
*AD2S83	16, 14, 12, 10	R	±8	1040	50–20 k	No	5	I	C I 3–87	Monolithic, User Selectable Dynamic Characteristics, and Resolution High Tracking Rate and ±0.25% Linearity Velocity Output
*AD2S34	14	R	±2.6, ±4.0	20, 48	0.4, 2.6, 4.0 k	No	12	M	C I 3–7	Dual Channel Resolver-to-Digital Converter with Onboard Oscillator. No External Trims
*AD2S46	16	S, R	±1.3, ±2.6	12	0.4→2.6 k	No	1	M	C I 3–23	16 Bit Resolver/Synchro-to-Digital Converter, 1.3 arc min in a 28-Pin DIP Ceramic Package. No External Trims

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Range[4]	Page	Comments
*AD2S44	12	S, R	±2.6,[11] ±4.0, ±5.2	20	0.4→2.6 k	No	8	M	C I 3–15	Dual Channel Resolver/ Synchro-to-Digital Converter with Loss of Track Detection. No External Trims
*AD2S90	12, 10	R	±8	375, 1500	2.0→10.0 k	No	5	C, I	C I 3–93	Low Cost RDC, Encoder-Like Output
*AD2S47	16, 14	S, R	±1.3, ±2.6	5, 20	200, 400	No	8	M	C I 3–31	Second Source for NATEL HSRDC 1006/56, 75 mW Power Consumption, MIL-STD-883
*AD2S93	14	LVDT	0.1, 0.05%	TBD	2.0–10.0 k	No	5	I	C I 3–97	14-Bit LVDT-to-Digital Converter

[1]S = Synchro; R = Resolver; I = Inductosyn.
[2]Revs/sec equivalent to pitches/sec in the case of an Inductosyn; in general, higher reference frequency options have higher tracking rates.
[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Pac
7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic C
Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[5]Die Revision.
[6]Consult data sheet.
[7]LVDT converter accuracy given as % full-scale linearity.
[8]Slew Rate (min).
[9]Resolution is user selectable.
[10]Depends on resolution selected.
[11]±2.6 arc min only available over 0°C to 70°C.
*New product since the publication of the most recent Databooks.
†Inductosyn is a registered trademark of Farrand Industries, Inc.

Orientation
S/D Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, Inductosyn®, and LVDT transducers.

All use the tracking conversion technique whereby the digital output follows the transducer shaft angle automatically without the need for convert commands or wait loops. Apart from producing near instantaneous digital angular data, this inherently ratiometric conversion method is very tolerant of noise on the signal inputs as well as voltage drops between the transducer and the converter.

In addition to the monolithic integrated circuits and hybrids that perform the conversions, the line also includes support components such as power oscillators, transformers and preamplifiers.

The range of products now available covers a wide spectrum of applications. Synchro and resolver transducers are used in a wide variety of commercial, industrial, and military applications where extreme reliability, ruggedness, and absolute angular position information are desirable. These transducers have a number of advantages over potentiometers and optical encoder based systems. The combination of an ac excited transducer with the technique of synchronous demodulation of the error signal by the converter inherently guarantees repeatability to 1 LSB of the stated resolution of the converter. In addition, the location of the electronics may be many hundreds of feet from the transducer, allowing use in electronically hostile environments unsuitable for other types of transducers.

In this section, the word "synchro" appears frequently. In many cases, the word "resolver" can be used in its place. The monolithic and some of the hybrid converters (options ×10, ×13, ×14, ×18) accept resolver format input. If the input signals are 3-wire synchro format, a "Scott-T" transformation converts it to resolver format. For our monolithic devices, this can be easily accomplished using the AD2S75 universal transformer isolated interface.

In this introductory section, there is a brief set of device definitions. Detailed data and applications information are given in the individual data sheets. For complete information about the synchro/resolver-to-digital converters and their applications, Analog Devices has a 208-page book, *Synchro and Resolver Conversion Handbook*, edited by G. Boyes (1980).

Resolver & Synchro-to-Digital Converters
These devices accept 4-wire resolver format (SIN, COS) signals or 3-wire synchro format (S1, S2, S3) signals together with a 2-wire reference signal, and output a digital binary word that represents the absolute shaft angle of the transducer. All standard resolver and synchro voltages are supported.

LVDT-to-Digital Converters
Linear Variable Displacement Transducer-to-digital converters provide conversion to 12-, 14- or 16-bit digital words of an ac modulated input, referenced to a second fixed signal input. The tracking loop technique employed ensures 1 LSB repeatability and input flexibility. The 2S54/56/58 series converters have been optimized for use in very high precision applications such as metrology.

Digital-to-Resolver Converters
These devices accept parallel binary digital inputs and an ac reference signal. The output is a 4-wire resolver format signal. For 3-wire synchro format output, use our STM1683 resolver-to-synchro output transformer, and for references >3.4 V rms, use the STM1680 input reference conditioning transformer. All standard resolver and synchro voltages are supported.

AC Vector Controller
This device combines the function of Park and Clarke transforms along with coordinate conversion on a single monolithic chip. These constitute a key element in vector control of ac asynchronous and brushless dc motors.

Velocity Output
The resolver & synchro-to-digital converters (RDCs & SDCs) not only provide absolute angular position information, but also provide an analog dc voltage proportional to the transducer's shaft speed. This can be used to exert second order control in a speed and position loop motion control system.

Transformer Isolation
Our input signal conditioning circuits for synchro and resolver inputs >2 V rms are either solid state or transformer based (e.g., 1740, 41, 42 series). Our transformer based hybrids utilize a unique, patented miniature transformer technology and provide input isolation to 350 V dc. This protects and isolates the electronics of a system from the hostile and electromagnetically noisy environments. The AD2S75 is a universal transformer isolated (1,000 V dc) interface and covers all standard synchro and resolver voltages. The AD2S75 is particularly well suited for use with all our monolithic RDCs (AD2S80 series) and some hybrid RDCs.

Support Devices
We also offer support components such as power oscillators (OSC1758), transformer based synchro/resolver signal conditioning (AD2S75) resolver-to-synchro output transformer (STM1683), and Inductosyn preamplifiers (IPA1764).

BIT WEIGHT TABLE
The most common method of representing angles in digital form is simple natural binary weighting, where the most significant bit (MSB) represents 180°, the next represents 90°, etc. The following table shows bit weights in degrees, minutes, seconds, and radians.

# Bits	Degrees	Arc Minutes	Arc Seconds	Radians	Milli-radians
1	180.0000	10800.0000	648000.00	3.1416	3141.5900
2	90.0000	5400.0000	324000.00	1.5708	1570.7950
3	45.0000	2700.0000	162000.00	0.7854	785.3975
4	22.5000	1350.0000	81000.00	0.3927	392.6988
5	11.2500	675.0000	40500.00	0.1963	196.3494
6	5.6250	337.5000	20250.00	0.0982	98.1747
7	2.8125	168.7500	10125.00	0.0491	49.0873
8	1.4063	84.3750	5062.50	0.0245	24.5437
9	0.7031	42.1875	2531.25	0.0123	12.2718
10	0.3516	21.0938	1265.63	0.0061	6.1359
11	0.1758	10.5469	632.81	0.0031	3.0680
12	0.0879	5.2734	316.41	0.0015	1.5340
13	0.0439	2.6367	158.20	0.0008	0.7670
14	0.0220	1.3184	79.10	0.0004	0.3835
15	0.0110	0.6592	39.55	0.0002	0.1917
16	0.0055	0.3296	19.78	0.0001	0.0959
17	0.0027	0.1648	9.89	0.0000	0.0479
18	0.0014	0.0824	4.94	0.0000	0.0240
19	0.0007	0.0412	2.47	0.0000	0.0120
20	0.0003	0.0206	1.24	0.0000	0.0060

14-Bit, Dual Channel Resolver-to-Digital Converter

AD2S34

FEATURES
1 in², 32-Pin Flatpack
2.6 Arc Minute Accuracy
14-Bit Resolution
On-Board Oscillator
Independent Reference Inputs
Independent Velocity Outputs
High Tracking Rate

APPLICATIONS
Gimbal/Gyro Control Systems
Radar/Sonar
Engine Controllers
Coordinate Conversion
Military Servo Control Systems
Fire Control Systems
Avionic Systems
Missile Systems
Antenna Monitoring
CNC Machine Tools

GENERAL DESCRIPTION

The AD2S34 series are 14-bit dual channel, continuous tracking resolver-to-digital converters. They have been designed specifically for applications where space and weight are at a premium. Each 32-pin hybrid device contains two independent Type II servo loop tracking converters and a power oscillator suitable for exciting resolvers. The ratiometric conversion technique employed by the converters provides excellent noise immunity, repeatability and tolerance of long lead lengths. The core of each conversion is performed by state-of-the-art monolithic integrated circuits manufactured in Analog Devices' proprietary BiMOS II process which combines the advantages of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low and ensures high reliability.

The converter interfaces directly to 2 V rms output resolvers. A simple voltage divider circuit of resistors can be used to derive the 2 V rms from other standard resolver voltages.

An on-board oscillator provides a reference excitation for resolvers operating at either 400 Hz, 2.6 kHz or 4 kHz. Each channel has an independent reference input, allowing the user to compensate for any resolver phase shift between induced signals (sin, cos) and reference.

The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation. The $\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$ control lines select the channel and present the digital position to the common data output pins. A $\overline{\text{DATA VALID}}$ flag is provided to assist with data transfer.

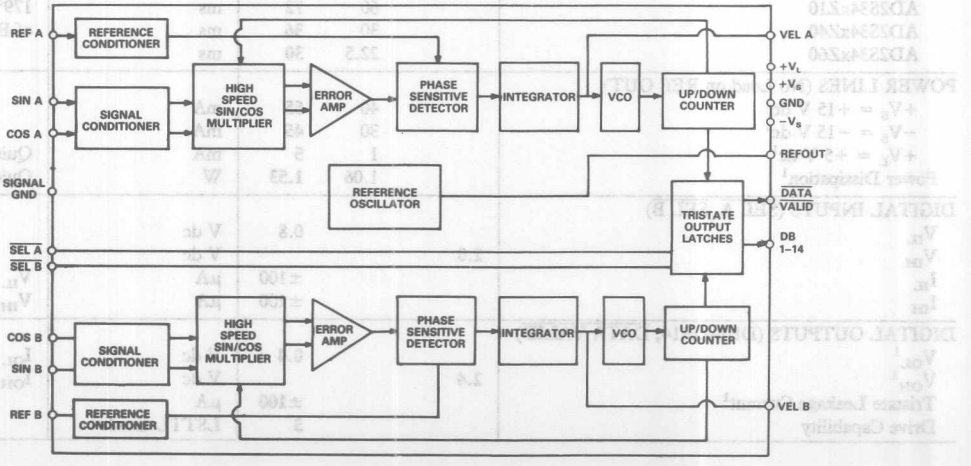
The AD2S34 also features two velocity outputs, one for each channel; these continuously generate analog signals proportional to the rotational velocity of the resolver shafts. These signals can be used in place of velocity transducers in many applications to provide loop stabilization and velocity feedback data.

MODELS AVAILABLE

The AD2S34 series is available in 2 accuracy grades:

AD2S34TZ 14-Bits	2.6 arc mins	−55°C to +125°C
AD2S34SZ 14-Bits	4.0 arc mins	−55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



PERFORMANCE					
Accuracy[1]					
AD2S34TZ			±2.6	arc min	−55°C to +125°C
AD2S34SZ			±4.0	arc min	−55°C to +125°C
Max Tracking Rate					
AD2S34xZ10	20			revs/s	
AD2S34xZ40	48			revs/s	
AD2S34xZ60	20			revs/s	
Resolution			14	Bits	Output Coding Parallel
	(1 LSB = 1.3 arc min)				Natural Binary
Repeatability			1	LSB	
Signal/Reference Frequency					
AD2S34xZ10	360	400	440	Hz	
AD2S34xZ40	2340	2600	2860	Hz	
AD2S34xZ60	3600	4000	4400	Hz	
Tracking Bandwidth					
AD2S34xZ10	90			Hz	
AD2S34xZ40	370			Hz	
AD2S34xZ60	650			Hz	
SIGNAL INPUTS (SIN, COS)					
Signal Voltage	1.8	2.0	2.2	V rms	
Allowable Phase Shift					
(Signal to Reference)			±10	Degrees	
Input Impedance	1			MΩ	
REFERENCE INPUTS (REF A, REF B)					
Reference Voltage	1.8	2.0	2.2	V rms	
Tolerance	1.4		8.0	V peak	
Input Impedance	1			MΩ	
ACCELERATION CONSTANT					
AD2S34xZ10	53000			sec^{-2}	
AD2S34xZ40	695000			sec^{-2}	
AD2S34xZ60	2164000			sec^{-2}	
STEP RESPONSE					
Large Step[1]					
AD2S34xZ10		60	72	ms	179° to 1 LSB
AD2S34xZ40		30	36	ms	of Error
AD2S34xZ60		22.5	30	ms	
POWER LINES (No Load on REF OUT)					
$+V_S$ = +15 V dc[1]		40	55	mA	
$-V_S$ = −15 V dc[1]		30	45	mA	
$+V_L$ = +5 V dc[1]		1	5	mA	Quiescent Condition
Power Dissipation[1]		1.06	1.53	W	Quiescent Condition
DIGITAL INPUTS ($\overline{SEL\ A}$, $\overline{SEL\ B}$)					
V_{IL}			0.8	V dc	
V_{IH}	2.0			V dc	
I_{IL}			±100	μA	V_{IL} = 0 V
I_{IH}			±100	μA	V_{IH} = 5 V
DIGITAL OUTPUTS (DB1–DB14, $\overline{DATA\ VALID}$)					
V_{OL}[1]			0.4	V dc	I_{OL} = 1.2 mA
V_{OH}[1]	2.4			V dc	I_{OH} = 100 μA
Tristate Leakage Current[1]			±100	μA	
Drive Capability			3	LSTTL Loads	

Parameter	AD2S34 Min	Typ	Max	Units	Comments
VELOCITY OUTPUTS (VEL A, VEL B)					
Voltage[1]	±7.5			V dc	At Max Tracking Rate
Linearity[1]					
AD2S34xZ10			±1	% of Output	
AD2S34xZ40			±3	% of Output	
AD2S34xZ60			±1	% of Output	
Reversion Error[1]			±3	%	
DC Zero Offset @ +25°C					
AD2S34xZ10		22	55	mV	
AD2S34xZ40		9	23	mV	
AD2S34xZ60		22	55	mV	
DC Zero Offset Temperature Coefficient					
AD2S34xZ10			−100	μV/°C	
AD2S34xZ40			−42	μV/°C	
AD2S34xZ60			−100	μV/°C	
Gain Scaling Accuracy			±10	% of FSD	
Noise and Ripple at LSB Rate			2	mV	
Dynamic Ripple (Peak)			1.5	% of Mean Output	
REFERENCE OUTPUT (REF OUT)					
Frequency[1]					
AD2S34xZ10	360	400	440	Hz	
AD2S34xZ40	2340	2600	2860	Hz	
AD2S34xZ60	3600	4000	4400	Hz	
Voltage[1]	5.5	6.0	6.5	V rms @ 50 mA	Min 120 Ω Load
DATA TRANSFER (See Figure 3)					
Time to Data Stable (After Negative Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)			1000	ns	t_S
Time to Data in High Impedance State (After Positive Edge of SEL A or SEL B)			50	ns	t_R
Time to DATA VALID High (After Negative Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)	1050			ns	t_P
Time to DATA VALID Low (After Positive Edge of $\overline{SEL\ A}$ or $\overline{SEL\ B}$)	40			ns	t_Q
DIMENSIONS	1.00 × 1.00 × 0.155 25.4 × 25.4 × 3.9			inch mm	See Package Information
WEIGHT			0.254 7.2	oz grams	
THERMAL RESISTANCE[2]					
θ_{JC} Worst Case Component			35	°C/W	
θ_{CA}			31	°C/W	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) 10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) 5% power supply variation; (d) 10% variation in reference frequency.

[2]To ensure that the junction temperature of the hottest component within the hybrid does not exceed the rated maximum of 150°C, the case temperature must not exceed 130°C.

Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages, and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17.25 V dc
$-V_S$ to GND . . . . . −17.25 V dc
$+V_L$ to GND . . . . . 0 to +7.0 V dc
Any Logic Input to GND (max) . . . . . +7.0 V dc
Any Logic Input to GND (min) . . . . . −0.4 V dc
SIN, COS to SIGNAL GND . . . . . ±12 V dc
REF A, REF B to SIGNAL GND . . . . . ±12 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −55°C to +125°C

CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference frequency and voltage. All the standard options and their option codes are shown below. For options not shown, please contact Analog Devices.

AD2S34 x Z y 0 B

- B — High-Reliability Processing (Optional)
- 0 — Signal 2 V Reference 2 V Resolver
- y — Base Part Number
  - y = 1 400 Hz Reference Frequency
  - y = 4 2.6 kHz Reference Frequency
  - y = 6 4.0 kHz Reference Frequency
- Z = Leaded Chip Carrier
- x = "T" −55°C to +125°C Operating Temperature Range 2.6 Arc Min Accuracy
- x = "S" −55°C to +125°C Operating Temperature Range 4.0 Arc Min Accuracy

For example, the correct part number for a component to operate with 400 Hz reference frequency and have a 2.6 arc minute accuracy over the −55°C to +125°C temperature range and processed to high reliability standards would be AD2S34TZ10B.

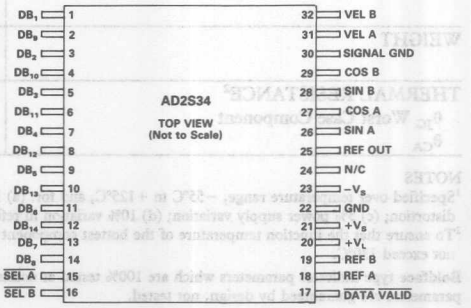
All components are 100% tested at −55°C, +25°C and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to GND) . . . . . +15 V dc ±5%
Power Supply Voltage ($-V_S$ to GND) . . . . . −15 V dc ±5%
Power Supply Voltage V_L . . . . . +5 V dc ±5%
Analog Input Voltage (SIN, COS to SIGNAL GND) . . . . . 2 V rms ±10%
Analog Input Voltage (REF A, REF B to SIGNAL GND) . . . . . 1.0 V to 8.0 V Peak
Signal and Reference Harmonic Distortion . . . . . ±10%
Phase Shift Between Signal and Reference . . . . . ±10 Degrees
Ambient Operating Temperature Range . . . . −55°C to +125°C

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1–14	DB1–DB14	PARALLEL OUTPUT DATA
15	$\overline{\text{SEL A}}$	SELECT CHANNEL A
16	$\overline{\text{SEL B}}$	SELECT CHANNEL B
17	$\overline{\text{DATA VALID}}$	DATA VALID
18	REF A	REFERENCE INPUT CHANNEL A
19	REF B	REFERENCE INPUT CHANNEL B
20	$+V_L$	LOGIC POWER SUPPLY
21	$+V_S$	POSITIVE POWER SUPPLY
22	GND	POWER SUPPLY GROUND (NOTE: THIS PIN IS ELECTRICALLY CONNECTED TO CASE.)
23	$-V_S$	NEGATIVE POWER SUPPLY
24	N/C	NOT CONNECTED
25	REF OUT	REFERENCE OUTPUT
26	SIN A	SINE INPUT CHANNEL A
27	COS A	COSINE INPUT CHANNEL A
28	SIN B	SINE INPUT CHANNEL B
29	COS B	COSINE INPUT CHANNEL B
30	SIGNAL GND	GROUND PIN FOR SIGNALS FROM RESOLVERS
31	VEL A	VELOCITY OUTPUT CHANNEL A
32	VEL B	VELOCITY OUTPUT CHANNEL B



AD2S34 Terminal Connections

ESD SENSITIVITY

The AD2S34 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (human body model) and fast, low energy pulses (charged device model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.



PRINCIPLES OF OPERATION

The AD2S34 series operate on a Type 2 tracking closed-loop principle. The output digital word continually tracks the position of the resolver shaft without the need for external convert commands and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated by one LSB.

Each channel is identical in operation, sharing power supply and digital position output pins.

Both channels operate continuously and independently of each other. The shared digital output from either channel is available as selected by switching the channel select inputs.

To illustrate the conversion process, the resolver format input signals are represented by:

$$V_1 = K E_0 \sin \omega t \sin \theta$$
$$V_2 = K E_0 \sin \omega t \cos \theta$$

where θ is the angle of the resolver shaft.

Assume that the current word state of the up-down counter is ϕ. V1 is multiplied by cos ϕ and V2 is multiplied by sin ϕ to give:

$$K E_0 \sin \omega t \sin \theta \cos \phi$$
$$K E_0 \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give:

$$K E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K E_0 \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed-loop system which seeks to null sin (θ–ϕ). When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the resolver shaft angle, θ.

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +15 V dc and −15 V dc, respectively, and must not be reversed. The voltage applied to V_L should be +5 V nominally. It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the three supply pins to GND.

The pin marked GND is connected electrically to the case and should be taken to the zero volt potential in the system.

The digital output is taken from Pins 1–14. Pin 1 is the MSB, Pin 12 the LSB. Please see terminal connections diagram.

The internal oscillator output (REF OUT) should be connected to each resolver and via an optional phase shift compensation circuit to the reference inputs (REF A & REF B). See Figure 1 for suitable phase compensation circuits.

The signals applied to REF A and REF B should be ac coupled as shown in Figure 1. This ac coupling can be included in the optional phase compensation circuit.

NOTE: For the 400 Hz option (AD2S34xZ10), in addition to the phase shift compensation referred to above, an extra 3.8 degrees of phase lead should be included to compensate for the internal phase shift within the hybrid. For higher frequency options this extra lead is not necessary as the internal phase shift does not affect the stated accuracy.

The signals are connected to sin and cos according to the following convention:

$$E_{SIN} = E_{RLO\text{-}RHI} \sin \omega t \sin \theta$$
$$E_{COS} = E_{RLO\text{-}RHI} \sin \omega t \cos \theta$$

The two signal ground wires from each resolver should be connected at the SIGNAL GND pin of the converter to minimize the coupling between the sine and cosine signals. For the same reason it is also recommended that the resolvers are connected using individual twisted pair cables with the sine, cosine and reference signals twisted separately.

See Figure 1 for the recommended connection circuit.

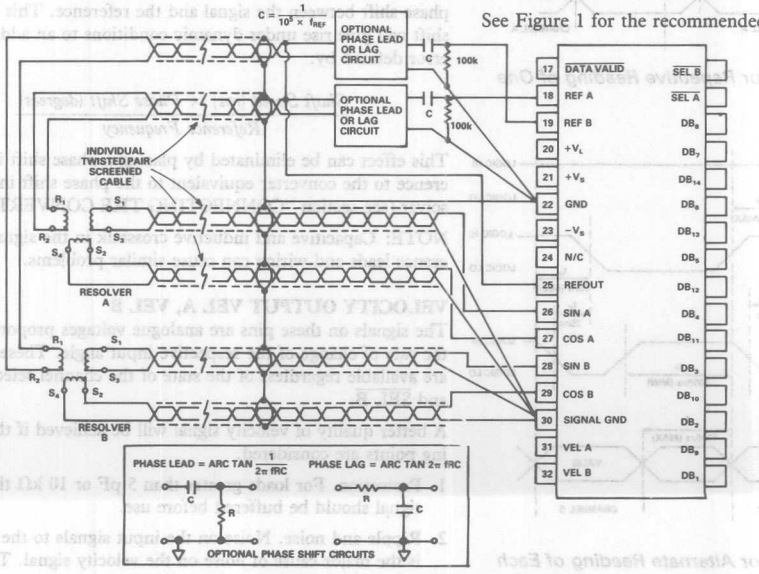


Figure 1. Connecting the 2S34 to Resolvers

SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. It is critical that the value of the resistors on the sine signals be precisely matched to the cosine signals. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common-mode rejection ratio of the signal inputs.

CHANNEL SELECT $\overline{\text{SEL A}}$, $\overline{\text{SEL B}}$

$\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$ are the channel select inputs. A logic low on $\overline{\text{SEL A}}$ selects Channel A and a logic low on $\overline{\text{SEL B}}$ selects Channel B. Both channels must not be selected at the same time.

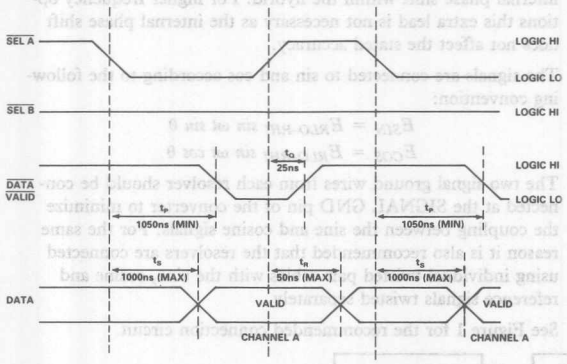


Figure 2a. Timing Diagram for Repetitive Reading of One Channel

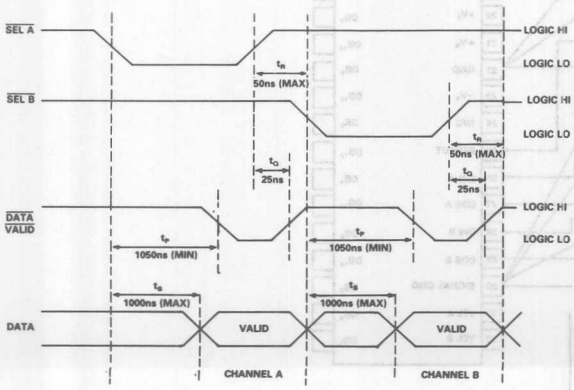


Figure 2b. Timing Diagram for Alternate Reading of Each Channel

Data becomes valid 1 μs after the negative edge of $\overline{\text{SEL A}}$ or $\overline{\text{SEL B}}$. Timing information is shown in Figure 2.

$\overline{\text{DATA VALID}}$

The $\overline{\text{DATA VALID}}$ output is a logic output which switches low 1 μs after the negative edge of either channel select indicating that the output latches have valid data for transfer.

REFERENCE OUTPUT REF OUT

The reference output provides a 6 V rms reference signal of 400 Hz, 2.6 kHz or 4.0 kHz frequency which can be used to excite the two resolvers and also to be used as the reference to the converter.

CAUSES OF ERROR

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers being a transducer characteristic. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are routed differently. For instance, different cable lengths or different capacitive loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$Error = 0.53 \times a \times b \text{ arc minutes}$$

where a = differential phase shift in degrees and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section on "CONNECTING THE CONVERTER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's stated accuracy. However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (degrees)}{Reference\ Frequency}$$

This effect can be eliminated by placing a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE CONVERTER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY OUTPUT VEL A, VEL B

The signals on these pins are analogue voltages proportional to the rate of change of the respective input angle. These signals are available regardless of the state of the channel selects $\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$.

A better quality of velocity signal will be achieved if the following points are considered.

1. Protection. For loads greater than 5 pF or 10 kΩ the velocity signal should be buffered before use.
2. Ripple and noise. Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

The resolvers are connected to the converter using separate screened twisted pair cable of equal lengths for the sine, cosine and reference signals.

Care is taken to reduce the external noise wherever possible.

A resolver with low residual voltage is chosen, i.e., one with small quadrature signals.

Feedthrough of the reference frequency can be removed by a filter on the velocity signal. Care must to be taken when setting the filter not to impede speed loop bandwidth.

Reference to signal phase shift should be minimized to reduce quadrature effects and larger ripple.

If the above precautions are taken, a very good noise and ripple performance can be achieved allowing the AD2S34 velocity signals to be used in very noisy environments.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

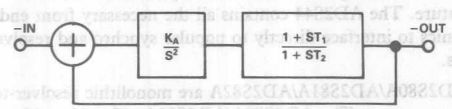


Figure 3. Transfer Function of AD2S34

Open-loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_A\ (1 + sT_1)}{s^2\ (1 + sT_2)}$$

Closed-loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_A + s^3\ T_2/K_A}$$

Where:

Option xZ10	Option xZ40	Option xZ60
K_A = 53000 sec^{-2}	K_A = 695000 sec^{-2}	K_A = 2164000 sec^{-2}
T_1 = 0.0062 sec	T_1 = 0.0019 sec	T_1 = 0.0011 sec
T_2 = 0.00079 sec	T_2 = 0.0003 sec	T_2 = 0.00017 sec

The gain and phase diagrams are shown in Figures 4 through 9.

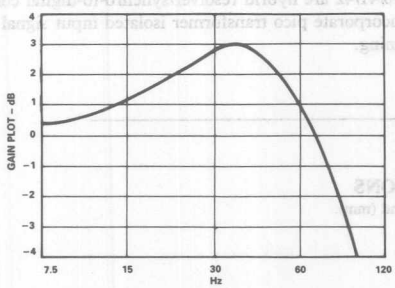


Figure 4. AD2S34xZ10 Gain Plot

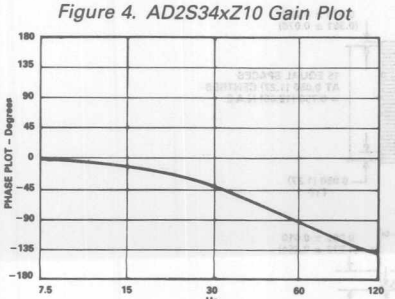


Figure 5. AD2S34xZ10 Phase Plot

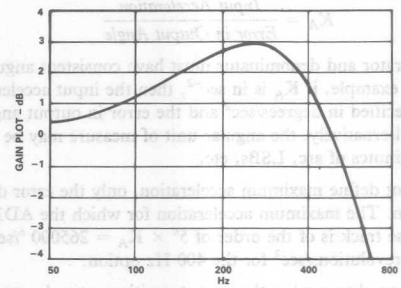


Figure 6. AD2S34xZ40 Gain Plot

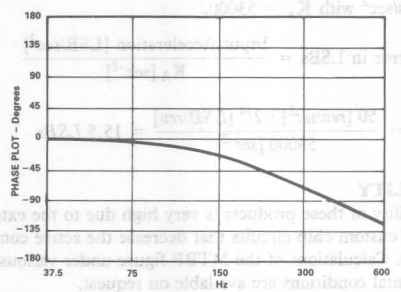


Figure 7. AD2S34xZ40 Phase Plot

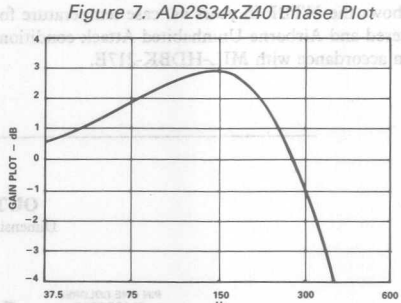


Figure 8. AD2S34xZ60 Gain Plot

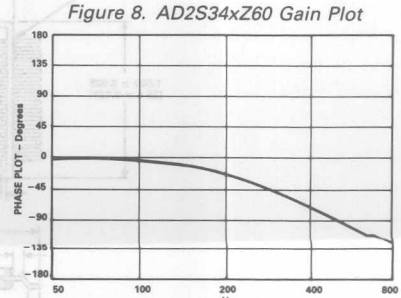


Figure 9. AD2S34xZ60 Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration.

This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_A does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S34 will not lose track is of the order of $5° \times K_A = 265000$ °/sec^2 or about 730 revolutions/sec^2 for the 400 Hz option.

K_A can be used to predict the output position error due to input acceleration. For example, for an acceleration of 50 revolutions/sec^2 with $K_A = 53000$,

$$\text{Error in LSBs} = \frac{\text{Input Acceleration [LSB/sec}^2\text{]}}{K_A\ [sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \cdot 2^{14}\ [LSB/rev]}{53000\ [sec^{-2}]} = 15.5\ LSBs$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 10 shows the MTBF in years vs. case temperature for Naval Sheltered and Airborne Uninhabited Attack conditions calculated in accordance with MIL-HDBK-217E.

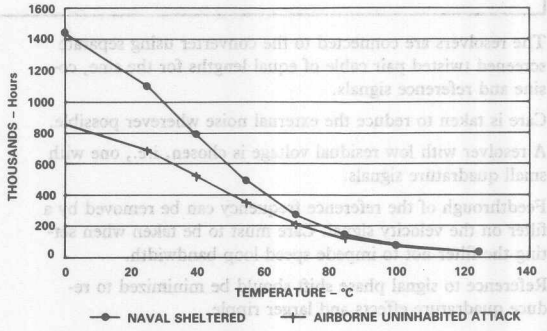


Figure 10. AD2S34 MTBF vs. Temperature

OTHER PRODUCTS

The AD2S44 is a low cost dual channel synchro or resolver converter with independent reference inputs and a built in test feature. The AD2S44 contains all the necessary front end electronics to interface directly to popular synchro and resolver options.

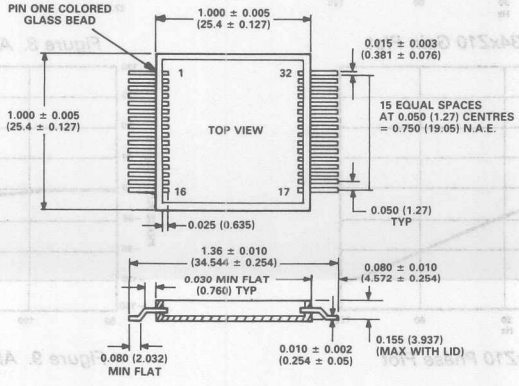
The AD2S80A/AD2S81A/AD2S82A are monolithic resolver-to-digital converters. The AD2S80A/AD2S82A offer selectable 10–16 bits of resolution. The AD2S81A has 12-bit resolution. All devices have user selectable dynamics. The AD2S80A is available in 40-pin DIP, 44-pin LCC and is qualified to MIL-STD-883B, Rev C. The 2S82A is available in a 44-pin PLCC, and the AD2S81A in a 28-pin DIP.

The AD2S46 is a highly integrated hybrid resolver/synchro-to-digital converter packaged in a 28-pin DIP. The part offers the user 1.3 arc minutes of accuracy over the full military temperature range.

The 1740/41/42 are hybrid resolver/synchro-to-digital converters which incorporate pico transformer isolated input signal conditioning.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



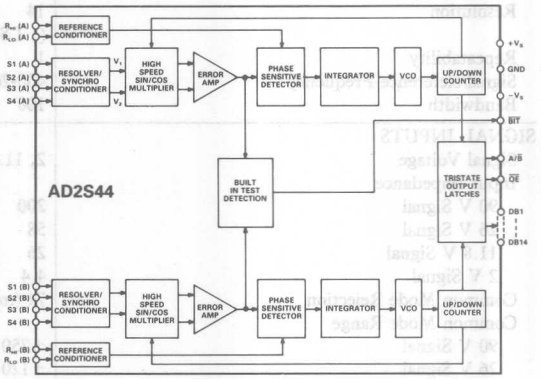
Low Cost, 14-Bit, Dual Channel Synchro/Resolver-to-Digital Converter

AD2S44

FEATURES
Low Cost/Channel
32-Pin DIL Hybrid Package
2.6 Arc Minute Accuracy
14-Bit Resolution
Built-In Test
Independent Reference Inputs
High Tracking Rate

APPLICATIONS
Gimbal/Gyro Control Systems
Robotics
Engine Controllers
Coordinate Conversion
Military Servo Control Systems
Fire Control Systems
Avionic Systems
Antenna Monitoring
CNC Machine Tooling

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S44 series are 14-bit dual channel, continuous tracking synchro/resolver-to-digital converters. They have been designed specifically for applications where space, weight and cost are at a premium. Each 32-pin hybrid device contains two independent Type II servo loop tracking converters. The ratiometric conversion technique employed provides excellent noise immunity and tolerance of long lead lengths.

The core of each conversion is performed by state-of-the-art monolithic integrated circuits manufactured in Analog Devices' proprietary BiMOS II process which combines the advantages of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low and ensures high reliability.

The built-in test ($\overline{BIT}$) facility can be used in failsafe systems to provide an indication of whether the converter is tracking accurately.

Each channel incorporates a high accuracy differential conditioning circuit for signal inputs providing more than 74 dB of common mode rejection. Options are available for both synchro and resolver format inputs. The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation. The A/$\overline{B}$ and $\overline{OE}$ control lines select the channel and present the digital position to the common data outputs.

The AD2S44 also features independent reference inputs. Consequently, different reference frequencies may be used for each channel.

MODELS AVAILABLE

The AD2S44 series is available in three accuracy grades:

AD2S44UM	14-Bits	±4.0 Arc Mins −55°C to +125°C (±2.6 Arc Mins −25°C to +85°C)
AD2S44TM	14-Bits	±4.0 Arc Mins −55°C to +125°C
AD2S44SM	14-Bits	±5.2 Arc Mins −55°C to +125°C

Each grade has options available which will interface to synchros and resolvers of standard voltage and frequency.

All components are 100% tested at −55°C, +25°C, and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability. Full ordering information is given on the back page of this data sheet.

AD2S44—SPECIFICATIONS (typical @ +25°C unless specified otherwise)

Parameter		AD2S44	Units	Comments
PERFORMANCE				
Accuracy[1]	AD2S44UM	**±4.0 (max)**	Arc Min	−55°C to +125°C
		±2.6 (max)	Arc Min	−25°C to +85°C
	AD2S44TM	**±4.0 (max)**	Arc Min	−55°C to +125°C
	AD2S44SM	**±5.2 (max)**	Arc Min	−55°C to +125°C
Tracking Rate		20	rev/s	
Resolution		14	Bits	Output Coding Parallel
		(1 LSB = 1.3 arc mins)		Natural Binary
Repeatability		1	LSB	
Signal/Reference Frequency		400-2600	Hz	
Bandwidth		100	Hz	
SIGNAL INPUTS				
Signal Voltage		2, 11.8, 26, 90	V rms	See Ordering Information
Input Impedance				
90 V Signal		200	kΩ	Resistive, Tolerance ±2%
26 V Signal		58	kΩ	
11.8 V Signal		26	kΩ	
2 V Signal		4.4	kΩ	
Common Mode Rejection		74 (min)	dB	
Common Mode Range				
90 V Signal		±250	V dc	
26 V Signal		±120	V dc	
11.8 V Signal		±60	V dc	
2 V Signal		±12	V dc	
REFERENCE INPUTS				
Reference Voltage		2, 11.8, 26, 115	V rms	See Ordering Information
Input Impedance				
115 V Reference		270	kΩ	Resistive, Tolerance ±5%
26 V Reference		270	kΩ	
11.8 V Reference		25	kΩ	
2 V Reference		25	kΩ	
Common Mode Range				
115 V Reference		±210	V dc	
26 V Reference		±210	V dc	
11.8 V Reference		±35	V dc	
2 V Reference		±35	V dc	
ACCELERATION CONSTANT		62000	sec^{-2}	

Parameter	AD2S44	Units	Comments
STEP RESPONSE			
Large Step[1]	63 (typ), **75 (max)**	ms	179° to 1 LSB of Error
Small Step[1]	25 (typ), **30 (max)**	ms	2° to 1 LSB of Error
POWER LINES			
$+V_S = +15\ V^1$	85 (typ), **100 (max)**	mA	Quiescent Condition
$-V_S = -15\ V^1$	55 (typ), **70 (max)**	mA	Quiescent Condition
Power Dissipation	2.1 (typ), 2.6 (max)	W	Quiescent Condition
DIGITAL INPUTS			
$\overline{OE}$ V_{IL}	0.7 (max)	V dc	$I_{IL} = 5\ \mu A$
V_{IH}	2.0 (min)	V dc	$I_{IH} = 5\ \mu A$
A/$\overline{B}$ V_{IL}	0.7 (max)	V dc	$I_{IL} = 1.2$ mA
V_{IH}	2.0 (min)	V dc	$I_{IH} = -60\ \mu A$
DIGITAL OUTPUTS (DB1–DB14)			
V_{OL}[1]	**0.4 (max)**	V dc	$I_{IL} = 1.2$ mA
V_{OH}[1]	**2.4 (min)**	V dc	$I_{OH} = 60\ \mu A$
Tristate Leakage Current	±40	μA	
Drive Capability	3 (max)	LSTTL Loads	
DATA TRANSFER			See Figure 3
Time to Data Stable (After Negative Edge of $\overline{OE}$ or Change of Level of A/$\overline{B}$)	640 (max)	ns	t_S
Time to Data in High Impedance State (After Positive Edge of $\overline{OE}$)	200 (max)	ns	t_R
Time for Repetitive Strobing of Selected Channel	200 (min)	ns	t_P
BUILT-IN TEST OUTPUT (BIT)			
Sense	Active Low		Low = Error Condition
V_{OL}	0.4 (max)	V dc	$I_{OL} = 3.2$ mA
V_{OH}	2.4 (min)	V dc	$I_{OH} = -160\ \mu A$
Drive Capability	8 (max)	LSTTL Loads	
Error Condition Set	55 (max)	LSB	
Error Condition Cleared	45 (min)	LSB	
DIMENSIONS	1.75 × 1.05 × 0.225	inch	See Package Information
	44.45 × 28.07 × 5.72	mm	
WEIGHT	0.65 (max)	oz	
	18.2 (max)	grams	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

Bold face type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17.25 V dc
$-V_S$ to GND . . . . . −17.25 V dc
Any Logic Input to GND (max) . . . . . +6.0 V dc
Any Logic Input to GND (min) . . . . . −0.4 V dc
Maximum Junction Temperature . . . . . +150°C
S1, S2, S3, S4 (Line to Line)[1]
  90 V Option . . . . . ±600 V dc
  26 V Option . . . . . ±160 V dc
  11.8 V Option . . . . . ± 80 V dc
  2 V Option . . . . . ±14 V dc
S1, S2, S3, S4 to GND
  90 V Option . . . . . ±600 V dc
  26 V Option . . . . . ±160 V dc
  11.8 V Option . . . . . ±80 V dc
  2 V Option . . . . . ±14 V dc
R_{HI} to R_{LO}
  26 V, 115 V Options . . . . . ±600 V dc
  2 V, 11.8 V Options . . . . . ±50 V dc
R_{HI}, R_{LO} to GND
  26 V, 115 V Options . . . . . ±600 V dc
  2 V, 11.8 V Options . . . . . ±50 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −55°C to +125°C

NOTE
[1]On synchro input options, line-to-line voltage refers to the S2–S1, S1–S3 and S3–S2 differential voltages. On resolver input options line-to-line levels refer to the S1–S3 and S2–S4 voltages.

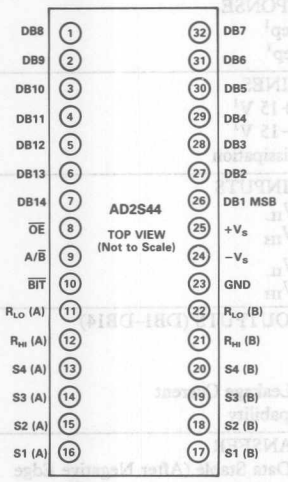
CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. The +15 V power supply must never go below GND.

Table I. Bit Weight Table

Bit Number	Weight (Degrees)
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB for 2S44)	0.0220

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Pin	Mnemonic	Description
1–7	DB8–DB14	Parallel Output Data Bits
26–32	DB1–DB7	Parallel Output Data Bits
8	$\overline{OE}$	Output Enable Input
9	A/$\overline{B}$	Channel A or B Select Input
10	$\overline{BIT}$	Built-In Test Error Output
11	R_{LO} (A)	Input Pin for Channel A Reference Low
12	R_{HI} (A)	Input Pin for Channel A Reference High
13–16	S4–S1 (A)	Channel A Input Signal
17–20	S1–S4 (B)	Channel B Input Signal
21	R_{HI} (B)	Input Pin for Channel B Reference High
22	R_{LO} (B)	Input Pin for Channel B Reference Low
23	GND	Power Supply Ground (Note: This Pin Is Electrically Connected to the Case.)
24	$-V_S$	Negative Power Supply
25	$+V_S$	Positive Power Supply

ESD SENSITIVITY

The AD2S44 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.



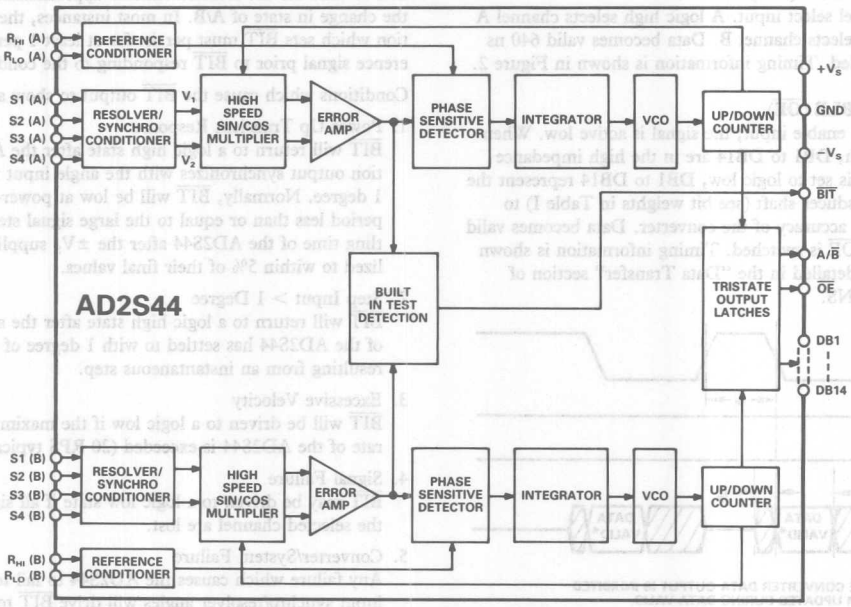


Figure 1. Functional Block Diagram of AD2S44

PRINCIPLES OF OPERATION

The AD2S44 series operate on a tracking principle. The output digital word continually tracks the position of the resolver/synchro shaft without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated.

A functional diagram of the AD2S44 is shown in Figure 1.

Each channel is identical in operation, sharing power supply and output pins. Both channels operate continuously and independently of each other–the digital output from either channel is available after switching the channel select and output enable inputs.

If the device is a synchro-to-digital converter, the 3-wire synchro output will be connected to S1, S2 and S3 on the unit, and a solid-state Scott-T input conditioner will convert these signals into resolver format, i.e.,

$$V_1 = K\,E_0\,sin\,\omega\tau\,sin\,\theta$$
$$V_2 = K\,E_0\,sin\,\omega\tau\,cos\,\theta$$

Where θ is the angle of the synchro shaft, $E_0 \sin \omega\tau$ is the reference signal and K is the transformation ratio of the input signal conditioner. If the unit is a resolver-to digital converter, the 4-wire resolver output will be connected directly to S1, S2, S3 and S4 on the unit.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ. V_1 is multiplied by $\cos\phi$ and V_2 is multiplied by $\sin\phi$ to give:

$$K\,E_0\,sin\,\omega\tau\,sin\,\theta\,cos\,\phi$$
$$K\,E_0\,sin\,\omega\tau\,cos\,\theta\,sin\,\phi.$$

These signals are subtracted by the error amplifier to give:

$$K\,E_0\,sin\,\omega\tau\,(sin\,\theta\,cos\,\phi - cos\,\theta\,sin\,\phi)$$

or

$$K\,E_0\,sin\,\omega\tau\,sin\,(\theta-\phi).$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null $\sin(\theta-\phi)$. When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the synchro-resolver shaft angle, θ.

CONNECTING THE CONVERTER

The power supply voltages connected to $-V_S$ and $+V_S$ pins should be ±15 V and must not be reversed.

It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the supply pins to GND.

The pin marked GND is connected electrically to the case and should be taken to the zero volt potential in the system.

The digital output is taken from Pins 26–32 and Pins 1–7. Pin 26 is the MSB, Pin 7 the LSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI}\,sin\,\omega\tau\,sin\,\theta$$
$$E_{S3-S2} = E_{RLO-RHI}\,sin\,\omega\tau\,sin\,(\theta-120°)$$
$$E_{S2-S1} = E_{RLO-RHI}\,sin\,\omega\tau\,sin\,(\theta-240°).$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

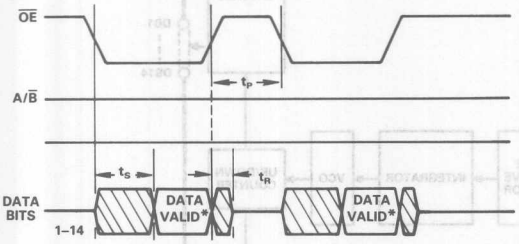
$$E_{S1-S3} = E_{RLO-RHI}\,sin\,\omega\tau\,sin\,\theta$$
$$E_{S2-S4} = E_{RLO-RHI}\,sin\,\omega\tau\,cos\,\theta$$

CHANNEL SELECT (A/$\overline{B}$)

A/$\overline{B}$ is the channel select input. A logic high selects channel A and a logic low selects channel B. Data becomes valid 640 ns after A/$\overline{B}$ is toggled. Timing information is shown in Figure 2.

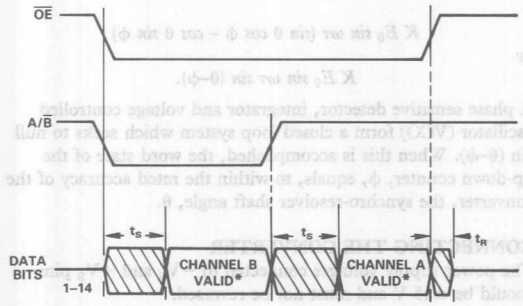
OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is the output enable input; the signal is active low. When set to a logic high, DB1 to DB14 are in the high impedance state. When $\overline{OE}$ is set to logic low, DB1 to DB14 represent the angle of the transducer shaft (see bit weights in Table I) to within the stated accuracy of the converter. Data becomes valid 640 ns after the $\overline{OE}$ is switched. Timing information is shown in Figure 2 and detailed in the "Data Transfer" section of SPECIFICATIONS.



*NOTE CONVERTER DATA OUTPUT IS INHIBITED FROM UPDATES DURING DATA VALID.

a. Repetitive Reading of One Channel



*NOTE CONVERTER DATA OUTPUT IS INHIBITED FROM UPDATES DURING CHANNEL VALID

b. Alternate Reading of Each Channel

Figure 2. AD2S44 Timing Diagrams

BUILT-IN TEST ($\overline{BIT}$)

$\overline{BIT}$ is the built-in test error output. This provides an over velocity or fault indication signal for the channel selected via A/$\overline{B}$. The error voltage of each channel is continuously monitored; and when the error exceeds ±50 bits for the currently selected channel, the $\overline{BIT}$ output goes low indicating that an error greater than approximately 1 angular degree exists and that the data is therefore invalid.

The $\overline{BIT}$ signal has a built-in hysterisis, i.e., the error required to set $\overline{BIT}$ is greater than that required for it to be cleared. $\overline{BIT}$ is set when the error exceeds 55 LSBs and is cleared when the error goes below 45 LSBs. This mode of operation guarantees that $\overline{BIT}$ will not flicker when the error threshold is crossed.

$\overline{BIT}$ is valid for the selected channel approximately 50 ns after the change in state of A/$\overline{B}$. In most instances, the error condition which sets $\overline{BIT}$ must persist for at least 1 period of the reference signal prior to $\overline{BIT}$ responding to the condition.

Conditions which cause the $\overline{BIT}$ output to show a fault are:

1. Power-Up Transient Response
   $\overline{BIT}$ will return to a logic high state after the AD2S44 position output synchronizes with the angle input to within 1 degree. Normally, $\overline{BIT}$ will be low at power-up for a period less than or equal to the large signal step response settling time of the AD2S44 after the $\pm V_S$ supplies have stabilized to within 5% of their final values.
2. Step Input > 1 Degree
   $\overline{BIT}$ will return to a logic high state after the selected channel of the AD2S44 has settled to with 1 degree of the input angle resulting from an instantaneous step.
3. Excessive Velocity
   $\overline{BIT}$ will be driven to a logic low if the maximum tracking rate of the AD2S44 is exceeded (20 RPS typical).
4. Signal Failure
   $\overline{BIT}$ may be driven to a logic low state if all signal voltages to the selected channel are lost.
5. Converter/System Failure
   Any failure which causes the AD2S44 to fail to track the input synchro/resolver angles will drive $\overline{BIT}$ to a logic low. This may include, but is not necessarily limited to, acceleration conditions, poor supply voltage regulation or excessive noise on the signal connections.

SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. For resolver format options, it is critical that the value of the resistors on the S1–S3 signal input pair be precisely matched to the S4–S2 input pair. For synchro options, the three resistors on S1, S2, S3 must be matched. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common mode rejection ratio of the signal inputs.

To calculate the values of the external scaling resistors add 2.222 kΩ extra per volt of signal in series with S1, S2, S3 and S4 (no resistor required on S4 for synchro options), and 3 kΩ in extra per volt of reference in series with R_{LO} and R_{HI}.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

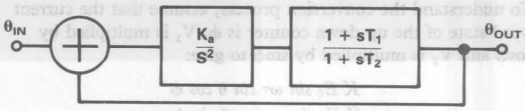


Figure 3. Transfer Function of AD2S44

Open loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2}$$

Closed loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_a + s^3\,T_2/K_a}$$

where $K_a = 62000\ sec^{-2}$
$T_1 = 0.0061$ sec
$T_2 = 0.001$ sec.

The gain and phase diagrams are shown in Figures 4 and 5.

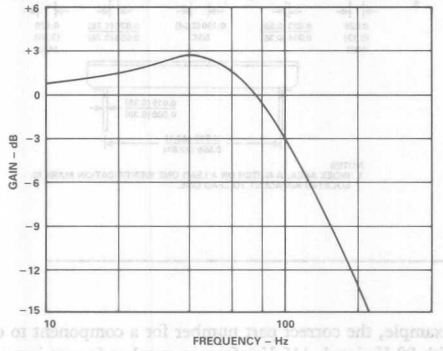


Figure 4. AD2S44 Gain Plot

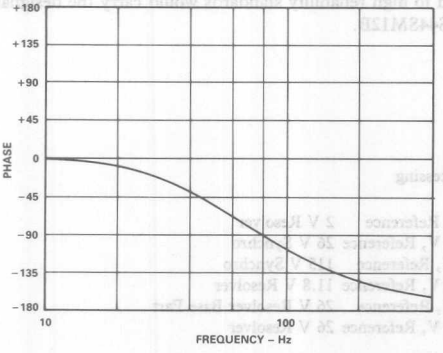


Figure 5. AD2S44 Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_a is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_a does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S44 will not lose track is on the order of $5° \times K_a = 310{,}000\ °/sec^2$ or about 800 revolutions/sec^2.

K_a can be used to predict the output position error due to input acceleration. For example, for an acceleration of 50 revolutions/sec^2 with $K_a = 62000$,

$$\text{Error in LSBs} = \frac{\text{Input Acceleration [LSB/sec}^2\text{]}}{K_a\,[sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \cdot 2^{14}\ [LSB/rev]}{62000\ [sec^{-2}]} = 13.2\ LSBs.$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 6 shows the MTBF in years vs. case temperature for Naval Sheltered conditions calculated in accordance with MIL-HDBK-217E.

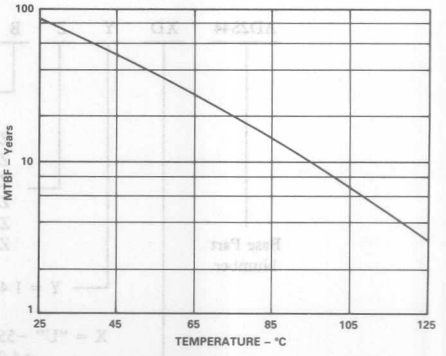


Figure 6. 2S44 MTBF vs. Temperature

OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below.

The SDC/RDC1740/41/42 are hybrid synchro/resolver to digital converters with internal isolating micro transformers.

The SDC/RDC1767/68 are identical to the SDC/RDC1740 series but with the additional features of analog velocity output and dc error output.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts. The device operates over a frequency range of 1 kHz to 10 kHz.

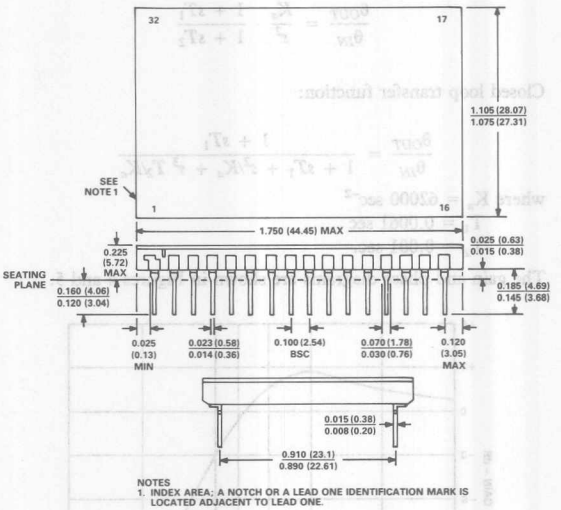
The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched output high power hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc minutes, and the outputs can supply 2 VA at 7 V rms. Transformers are available to convert the output to synchro or resolver format at high voltage levels.

The AD2S65/66 are similar to the DRC1745/46 but do not include the power output stage. These devices are available in accuracy grades to 1 arc minute.

The 2S80 series are monolithic ICs performing resolver to digital conversion with accuracies up to ±2 arc minutes and 16-bit resolution.

OUTLINE DIMENSION

Dimensions shown in inches and (mm).



NOTES
1. INDEX AREA: A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference voltage and frequency. All the standard options and their option codes are shown below. For nonstandard configurations, please contact Analog Devices.

For example, the correct part number for a component to operate with 90 V signal, 115 V reference synchro format inputs and yield a ±5.2 arc minute accuracy over the −55°C to +125° temperature range would be AD2S44SM12. The same part, processed to high reliability standards would carry the designator AD2S44SM12B.

AD2S44 XD Y Z B

- AD2S44 — Base Part Number
- B — High-Rel Processing
- Z — Signal / Reference / Resolver
  - Z = 0, Signal 2 V, Reference 2 V Resolver
  - Z = 1, Signal 11.8 V, Reference 26 V Synchro
  - Z = 2, Signal 90 V, Reference 115 V Synchro
  - Z = 3, Signal 11.8 V, Reference 11.8 V Resolver
  - Z = 4, Signal 26 V, Reference 26 V Resolver Base Part
  - Z = 8, Signal 11.8 V, Reference 26 V Resolver
- Y — Reference Frequency
  - Y = 1 400 Hz to 2.6 kHz Reference Frequency
- XD — Temperature Range / Accuracy
  - X = "U" −55°C to +125°C Operating Temperature Range ±4.0 arc min Accuracy
  - ±2.6 arc min Accuracy (−25°C to +85°C)
  - X = "T" −55°C to +125°C Operating Temperature Range ±4.0 arc min Accuracy
  - X = "S" −55°C to +125°C Operating Temperature Range ±5.2 arc min Accuracy

Low Cost, 16-Bit Synchro/ Resolver-to-Digital Converter

AD2S46

FEATURES
- 1.3 Arc Minute Accuracy
- 16-Bit Resolution
- Small 28-Pin Ceramic DIP
- Low Cost

APPLICATIONS
- Gimbal/Gyro Control Systems
- Radar System
- Engine Controllers
- Sonar
- Military Servo Control Systems
- Fire Control Systems
- Avionic Systems
- Antenna Monitoring
- CNC Machine Tooling

GENERAL DESCRIPTION

The AD2S46 series are 16-bit, continuous tracking synchro/ resolver-to-digital converters. They have been designed specifically for applications where space and performance are at a premium. Each 28-pin hybrid device uses a Type 2 servo loop tracking converter with a ratiometric conversion technique to provide excellent noise immunity, repeatability and tolerance of long lead lengths.

The core of each conversion is performed by a state of the art monolithic integrated circuit manufactured in Analog Devices' proprietary BiMOS II process which combines the advantage of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low providing both packaging which reflects LSI monolithic standards and ensures high reliability.

The device incorporates a high accuracy differential conditioning circuit for signal inputs providing more than 74 dB of common-mode rejection. Options are available for both synchro and resolver format inputs. The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation.

Digital data transfer is accommodated by an $\overline{\text{ENABLE}}$ input which controls the tristate outputs and presents the data to the bus when taking from a HI to a LO state.

An $\overline{\text{INHIBIT}}$ precedes the $\overline{\text{ENABLE}}$ input and freezes the data transfer from the up-down counter to the output latches. This action does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a data refresh. A BYTE SELECT input provides the facility for interfacing to an 8- or 16-bit bus system.

MODELS AVAILABLE

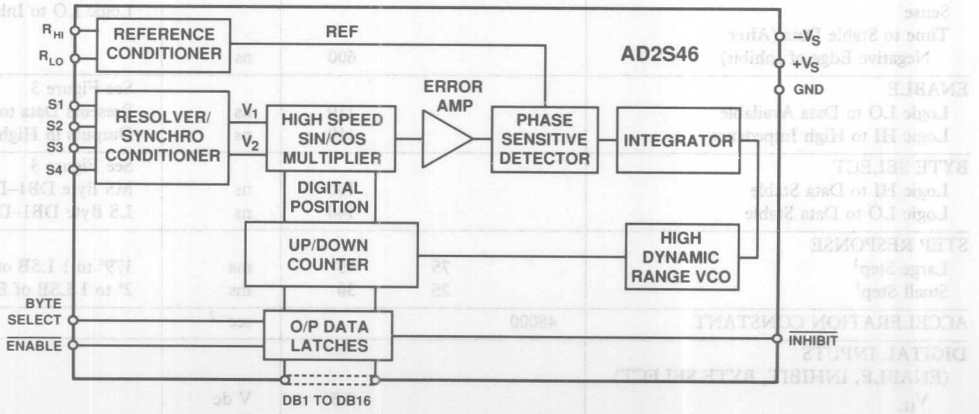
The AD2S46 series is available in 2 accuracy grades:

AD2S46TD	16 Bits	± 1.3 arc mins	−55°C to +125°C
AD2S46SD	16 Bits	± 2.6 arc mins	−55°C to +125°C

Each grade has options available which will interface to standard synchros and resolvers.

All components are 100% tested at −55°C, +25°C, and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability. Full ordering information is given on the back page of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



AD2S46—SPECIFICATIONS (typical at +25°C unless specified otherwise)

Parameter	AD2S46 Min	Typ	Max	Units	Comments
PERFORMANCE					
Accuracy[1]					
AD2S46TD			±1.3	arc min	
AD2S46SD			±2.6	arc min	
Tracking Rate			12	rev/s	
Resolution			16	Bits	Parallel Natural Binary
		(1 LSB = 20 arc sec)			1 IN65356
Repeatability			1	LSB	
Signal/Reference					
Frequency	360		2860	Hz	
Bandwidth			85	Hz	
SIGNAL INPUTS					
Signal Voltage		2, 11.8, 26, 90 ±10%		V rms	See Ordering Information
Impedance					
90 V Signal		200		kΩ	Resistive Tolerance ±2%
26 V Signal		58		kΩ	
11.8 V Signal		26		kΩ	
2 V Signal		4.4		kΩ	
Common-Mode Rejection	74			dB	
Common-Mode Range					
90 V Signal			±250	V dc	
26 V Signal			±120	V dc	
11.8 V Signal			±60	V dc	
2 V Signal			±12	V dc	
REFERENCE INPUTS					
Reference Voltage		2, 11.8, 26, 115 ±10%		V rms	See Ordering Information
Impedance					
115 V Reference		275		kΩ	Resistive Tolerance ±5%
26 V Reference		275		kΩ	
11.8 V Reference		25		kΩ	
2 V Reference		25		kΩ	
Common-Mode Range					
115 V Reference			±210	V dc	
26 V Reference			±210	V dc	
11.8 V Reference			±35	V dc	
2 V Reference			±35	V dc	
INHIBIT					See Figure 3
Sense					Logic LO to Inhibit
Time to Stable Data (After Negative Edge of Inhibit)			600	ns	
ENABLE					See Figure 3
Logic LO to Data Available			110	ns	Presents Data to Output
Logic HI to High Impedance			110	ns	Outputs in High Impedance State
BYTE SELECT					See Figure 3
Logic HI to Data Stable			130	ns	MS Byte DB1–DB8
Logic LO to Data Stable			140	ns	LS Byte DB1–DB8
STEP RESPONSE					
Large Step[1]		75	95	ms	179° to 1 LSB of Error
Small Step[1]		25	30	ms	2° to 1 LSB of Error
ACCELERATION CONSTANT	48000			sec^{-2}	
DIGITAL INPUTS (ENABLE, INHIBIT, BYTE SELECT)					
V_{IL}			0.8	V dc	
V_{IH}	2.0			V dc	
I_{IL}			±100	μA	V_{IL} = 0 V
I_{IH}			±100	μA	V_{IH} = 5 V

Parameter	AD2S46 Min	Typ	Max	Units	Comments
DIGITAL OUTPUTS (DB1–DB16)					
V_{OL}[1]			0.4	V dc	I_{OL} = 1.2 mA
V_{OH}[1]	2.4			V dc	I_{OH} = 100 μA
Tristate Leakage Current			±100	μA	
Drive Capability			3	LSTTL	
POWER SUPPLIES					
Voltage Levels					
$+V_S$[1]	+14.25	+15	+15.75	V dc	
$-V_S$[1]	−14.25	−15	−15.75	V dc	
Current					
$+I_S$		30	35	mA	
$-I_S$		15	20	mA	
Power Dissipation		675	825	mW	
DIMENSIONS	1.4 × 0.6 × 0.135			inch	See Package Information
	35.6 × 15.2 × 3.4			mm	
WEIGHT			0.25	Oz	
			6.3	Grams	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal ± and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages, and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17.25 V dc
$-V_S$ to GND . . . . . −17.25 V dc
Any Logic Input to GND (max) . . . . . +5.5 V dc
Any Logic Input to GND (min) . . . . . −0.4 V dc
Maximum Junction Temperature . . . . . 150°C
S1, S2, S3, S4 (Line to Line)[1]
(90 V Option) . . . . . ±600 V dc
(26 V Option) . . . . . ±160 V dc
(11.8 V Option) . . . . . ±80 V dc
(2 V Option) . . . . . ±14 V dc
S1, S2, S3, S4 to GND
(90 V Option) . . . . . ±250 V dc
(26 V Option) . . . . . ±120 V dc
(11.8 V Option) . . . . . ±60 V dc
(2 V Option) . . . . . ±12 V dc
R_{HI} to R_{LO}
(26 V, 115 V Options) . . . . . ±600 V dc
(2 V, 11.8 V Options) . . . . . ±50 V dc
R_{HI} and R_{LO} to GND
(26 V, 115 V Options) . . . . . ±210 V dc
(2 V, 11.8 V Options) . . . . . ±35 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range[2] . . . . . −55°C to +125°C

NOTE

[1]On synchro input options, line to line voltage refers to the S2–S1, S1–S3 and S3–S2 differential voltages. On resolver input options line to line levels refer to the S1–S3 and S2–S4 voltages.

[2]Thermal Resistance: To ensure that the junction temperature of the hottest component within the hybrid does not exceed the rated maximum of 150°C, the case temperature must not exceed 130°C.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to GND) . . . . . +15 V dc ±5%
Power Supply Voltage ($-V_S$ to GND) . . . . . −15 V dc ±5%
Analog Input Voltage (S1, S2, S3, S4 Line to Line)
(90 V Option) . . . . . 90 V rms ±10%
(26 V Option) . . . . . 26 V rms ±10%
(11.8 V Option) . . . . . 11.8 V rms ±10%
(2 V Option) . . . . . 2 V rms ±10%
Analog Input Voltage (R_{HI} to R_{LO})
(26 V Option) . . . . . 26 V rms ±10%
(115 V Option) . . . . . 115 V rms ±10%
(11.8 V Option) . . . . . 11.8 V rms ±10%
(2 V Option) . . . . . 2 V rms ±10%
Signal and Reference Harmonic Distortion . . . . . ±10%
Phase Shift Between Signal and Reference . . . . . ±10 Degrees
Ambient Operating Temperature Range . . . . −55°C to +125°C

CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

ESD SENSITIVITY

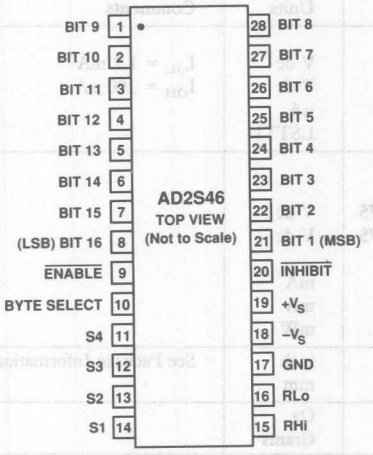
The AD2S46 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.



AD2S46

PIN CONFIGURATION



AD2S46 PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1–8	DB9–DB16	PARALLEL OUTPUT DATA BITS
21–28	DB1–DB8	PARALLEL OUTPUT DATA BITS
9	$\overline{\text{ENABLE}}$	OUTPUT ENABLE INPUT
10	BYTE SELECT	BYTE SELECT INPUT SIGNAL
11–14	S4–S1	SYNCHRO/RESOLVER SIGNAL INPUTS
15	R_{HI}	INPUT PIN FOR REFERENCE HIGH
16	R_{LO}	INPUT PIN FOR REFERENCE LOW
17	GND	POWER SUPPLY GROUND
18	$-V_S$	NEGATIVE POWER SUPPLY
19	$+V_S$	POSITIVE POWER SUPPLY
20	$\overline{\text{INHIBIT}}$	INPUT PIN TO INHIBIT CONVERTER

PRINCIPLES OF OPERATION

The AD2S46 series operate on a Type 2 tracking closed-loop principle. The output digital word continually tracks the position of the resolver/synchro shaft without the need for external convert commands and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated by one LSB.

If the device is a synchro-to-digital converter, the 3-wire synchro output will be connected to S1, S2 and S3 on the unit and a solid-state Scott-T input conditioner will convert these signals into resolver format, i.e.,

$V_1 = K\,E_0 \sin \omega t \sin \theta$ (sin)
$V_2 = K\,E_0 \sin \omega t \cos \theta$ (cos)

Where θ is the angle of the synchro shaft, $E_0 \sin \omega t$ is the reference signal, and K is the transformation ratio of the input signal conditioner. If the unit is a resolver-to digital converter, the 4-wire resolver output will be connected directly to S1, S2, S3 and S4 on the unit.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ. V_1 is multiplied by $\cos \phi$ and V_2 is multiplied by $\sin \phi$ to give:

$K\,E_0 \sin \omega t \sin \theta \cos \phi$
$K\,E_0 \sin \omega t \cos \theta \sin \phi$

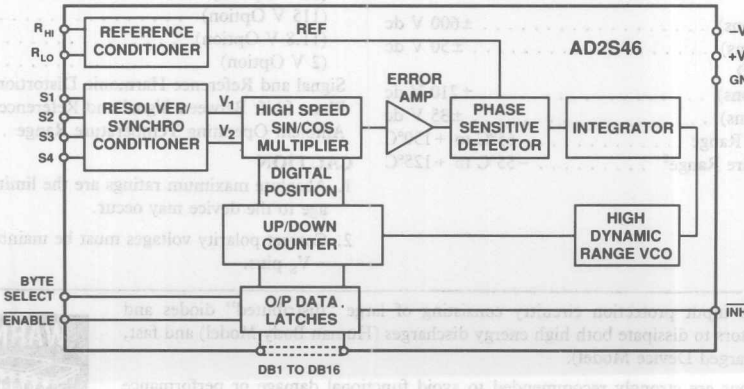
These signals are subtracted by the error amplifier to give:

$K\,E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$

or

$K\,E_0 \sin \omega t \sin (\theta - \phi)$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed-loop system which seeks to null sin $(\theta - \phi)$. When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the synchro/resolver shaft angle, θ.



AD2S46 Functional Block Diagram

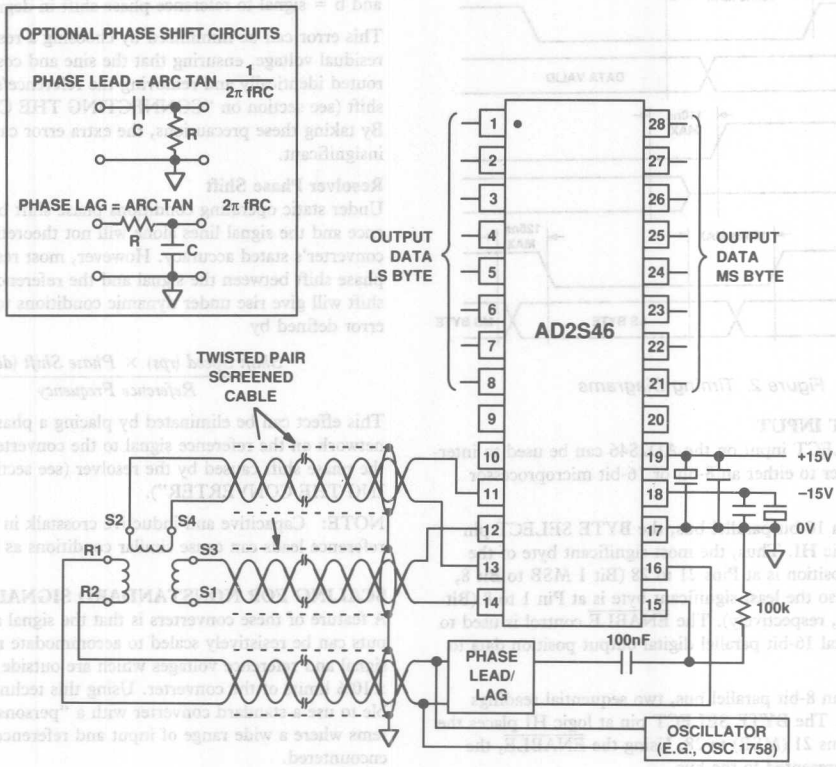


Figure 1. Connection Diagram

CONNECTING THE CONVERTER

The power supply voltages connected to $-V_S$ and $+V_S$ pins should be −15 V and +15 V and must not be reversed.

It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the supply pins to GND.

The digital output is taken from Pins 21–28 and Pins 1–8. Pin 21 is the MSB, Pin 8 the LSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120°)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240°)$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RLO-RHI} \sin \omega t \cos \theta$$

It is recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to $\overline{\text{INHIBIT}}$. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

$\overline{\text{INHIBIT}}$ INPUT

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a refresh of the output data.

$\overline{\text{ENABLE}}$ INPUT

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance state, and application of a logic "LO" presents the data of the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process. Timing information is shown in Figure 2.

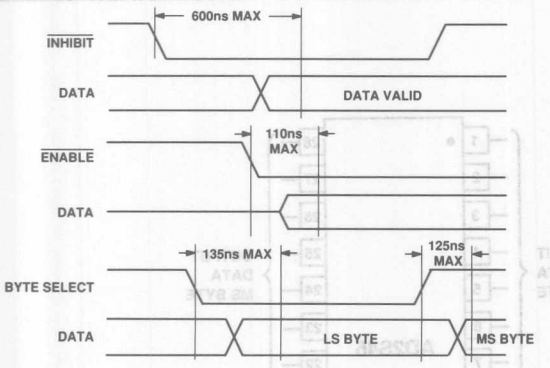


Figure 2. Timing Diagrams

BYTE SELECT INPUT

The BYTE SELECT input on the AD2S46 can be used to interface the converter to either an 8-bit or 16-bit microprocessor bus.

To interface to a 16-bit parallel bus, the BYTE SELECT pin should be at logic HI. Thus, the most significant byte of the digital output position is at Pins 21 to 28 (Bit 1 MSB to Bit 8, respectively). Also the least significant byte is at Pin 1 to 8 (Bit 9 to Bit 16 LSB, respectively). The $\overline{\text{ENABLE}}$ control is used to present the digital 16-bit parallel digital output position data to the pins.

To interface to an 8-bit parallel bus, two sequential readings must take place. The BYTE SELECT pin at logic HI places the MS BYTE at Pins 21 (MSB) to 28. Using the $\overline{\text{ENABLE}}$, the parallel data is presented to the bus.

A logic LO on the BYTE SELECT place the LS BYTE at Pins 21 to 28 (LSB). Using the $\overline{\text{ENABLE}}$, the parallel data is presented to the bus.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is within the recommended operating conditions.

The AD2S46 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

CAUSES OF ERROR

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static errors. Some differential phase shift will be present on all resolvers being a characteristic of the transducer. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different capactive loads could cause differential phase shift. The additional error caused by differential phase shift on the input signals approximates to:

$$Error = 0.53 \times a \times b \text{ arc minutes}$$

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are routed identically and removing the reference/signals phase shift (see section on "CONNECTING THE CONVERTER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's stated accuracy. However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (degrees)}{Reference\ Frequency}$$

This effect can be eliminated by placing a phase lead/lag network on the reference signal to the converter equivalent to the phase shift caused by the resolver (see section "CONNECTING THE CONVERTER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads can cause similar conditions as described above.

SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. For resolver format options, it is critical that the value of the resistors on the S1-S3 signal input pair be precisely matched to the S4–S2 input pair. For synchro options, the three resistors on S1, S2, S3 must be matched. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common-mode rejection ratio of the signal inputs.

Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

Bit Weight Table

To calculate the values of the external scaling resistors add 1.111 kΩ extra per volt of signal in series with S1, S2, S3 and S4 (resolver options only), and 3 kΩ in extra per volt of reference in series with R_{LO} and R_{HI}.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

Open-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_A (1 + sT_1)}{S^2 (1 + sT_2)}$$

Closed-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_A + s^3 T_2/K_A}$$

where $K_A = 48000\ sec^{-2}$
$T_1 = 0.0071$ sec
$T_2 = 0.00125$ sec

The gain and phase diagrams are shown in Figures 3 and 4.

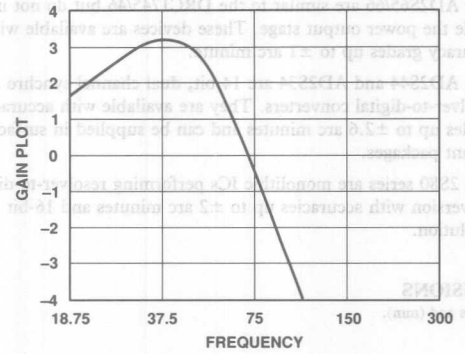


Figure 3. AD2S46 Gain Plot

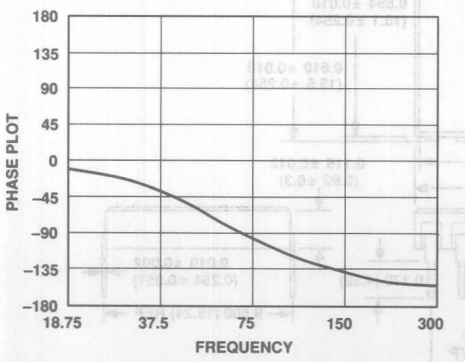


Figure 4. AD2S46 Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_A does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S46 will not lose track is in the order of $5° \times K_A = 238{,}000\ °/sec^2$ or about 660 revolutions/sec^2.

K_A can be used to predict the output position error due to input acceleration. For example, for an acceleration of 50 revolutions/sec^2 with $K_A = 48000$,

$$Error\ in\ LSBs = \frac{Input\ Acceleration\ [LSB/sec^2]}{K_A\ [sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \times 2^{16}\ [LSB/sec^2]}{47662\ [sec^{-2}]}$$

$$= 68\ LSBs$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 5 shows the MTBF in years vs. case temperature for Naval Sheltered conditions and airborne uninhabited cargo calculated in accordance with MIL-HDBK-217E.

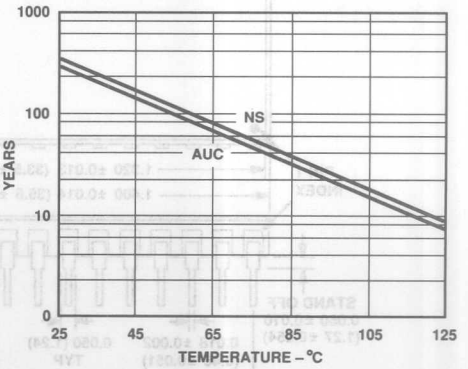
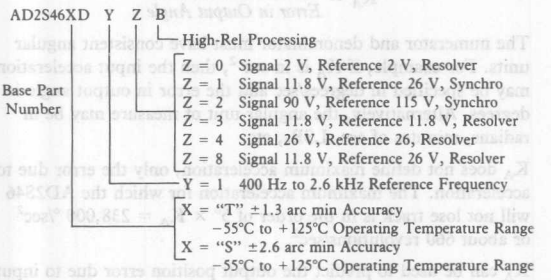


Figure 5. AD2S46 MTBF vs. Temperature

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference voltage and frequency. All the standard options and their option codes are shown below. For options not shown, please contact Analog Devices, Inc.



For example, the correct part number for a component to operate with a 90 V signal, 115 V reference synchro format inputs and yield a ±1.3 arc minute accuracy over the −55°C to +125°C temperature range would be AD2S46TD12. The same part processed to high reliability standards would carry the designator B, i.e., AD2S46TD12B.

OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application please contact our Applications Engineering Department.

The SDC/RDC1740/41/42 are hybrid synchro/resolver-to-digital converters with internal isolating micro transformers.

The SDC/RDC1767/1768 are identical to the SDC/RDC1740 series but with the additional features of analog velocity output and dc error output.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts. The device operates over a frequency range of 1 to 10 kHz.

The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched output high power hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc minutes and the outputs can supply 2 VA at 7 V rms. Transformers are available to convert the output to synchro or resolver format at high voltage levels.

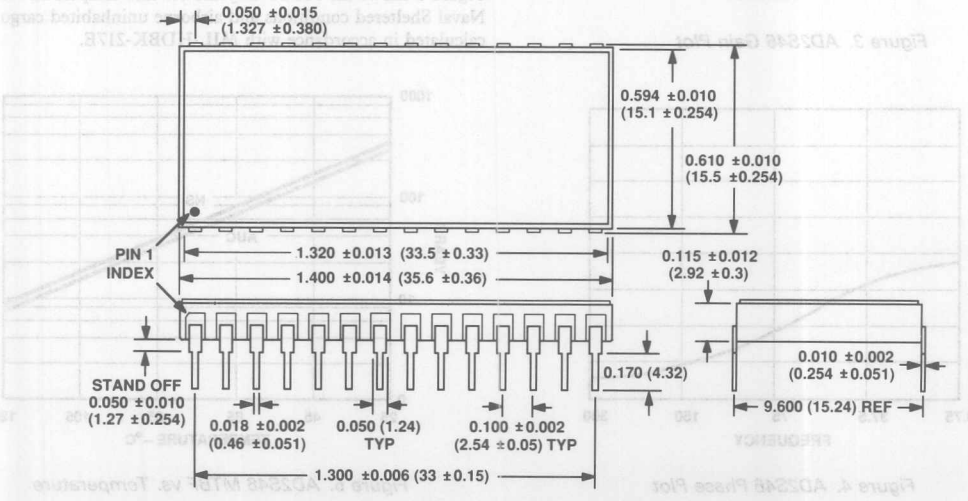
The AD2S65/66 are similar to the DRC1745/46 but do not include the power output stage. These devices are available with accuracy grades up to ±1 arc minute.

The AD2S44 and AD2S34 are 14 bit, dual channel synchro and resolver-to-digital converters. They are available with accuracy grades up to ±2.6 arc minutes and can be supplied in surface mount packages.

The 2S80 series are monolithic ICs performing resolver-to-digital conversion with accuracies up to ±2 arc minutes and 16-bit resolution.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



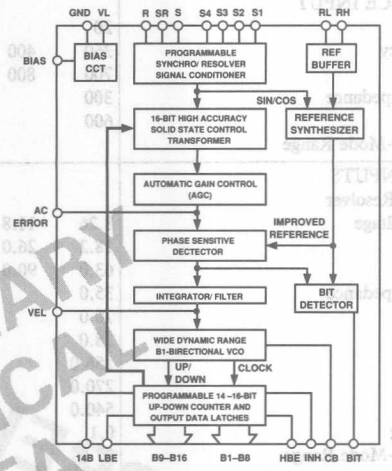
High Precision, Single Supply Resolver/Synchro-to-Digital Converter

AD2S47

FEATURES
- Single 5 V Supply Operation
- High Accuracy (1.3 arc min)
- 8-/16-Bit Bus Compatible
- 14-/16-Bit Resolution
- Built-in Test Features
- Internal Reference Synthesis Function
- Automatic Gain Control Circuit
- Pin Programmable for 14-/16-Bit Operation
- High Tracking Rate (7200°/sec – 14-Bit Mode)
- Analog Velocity and AC Error Outputs
- NATEL/DDC Second Source
- Manufactured to MIL STD 1772
- 36-Pin DDIP

APPLICATIONS
- Natel/DDC Second Source
- Avionics Systems
- Servo Systems
- Robotics
- Fire Control Systems
- Radar Systems
- Stabilization Systems

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S47 is a high accuracy 14-/16-bit resolution synchro/resolver-to-digital converter (S/RDC).

Options are available that will accept 90, 26 or 11.8 volt signal levels in synchro or resolver formats. The reference input accepts voltages in the range 20 to 115 V rms. Internal reference conditioning match the reference phase to the signal input phase. This eliminates errors due to signal to reference phase shifts in the transducer.

The AD2S47 operates at reference frequencies of either 400 Hz or 800 Hz (see Ordering Guide).

The AD2S47 operates on the type 2 tracking loop principle, resulting in the digital output continuously tracking the input angle. The converter does not require conversion instructions or wait states. The converter operates a ratiometric conversion technique which shows excellent noise immunity and repeatability. Using proprietary designed full custom integrated circuits, the AD2S47 achieves high accuracy over the full operating temperature range. The use of custom designed circuits inside the device allows high grade performance to be achieved at a competitive cost.

AD2S47 provides a cost competitive solution to S/RDC requirements. Internal circuits fabricated on Analog Devices linear compatible CMOS (LC^2MOS) process minimize component count and power requirements. The AD2S47 uses a proprietary designed custom digital circuit to control all interfacing to the device. The output from the AD247 is via a 16-bit bus which can be placed in a high impedance state, allowing connection of the device directly to an 8- or 16-bit data bus.

PRODUCT HIGHLIGHTS

Second Source for Natel HSRD1006 & 1056
Second Source for DDC SDC-14531

Single 5 V Power Supply Operation. Single power supply operation with low current consumption reduces system power supply requirements.

8- and 16-Bit Processor Bus Compatible. Separate HI and LO byte enable pins allow direct, simple interfacing to either 8- or 16-bit data buses.

Pin Programmable Selectable Resolution. Connecting the 14B pin to 0 V selects 16-bit resolution.

Pin Programmable for Synchro or Resolver Signals. Connecting the S pin to SR pin formats the device for synchro operation. Connecting the R pin to the SR pin formats the device for resolver operation.

High Tracking Rate. Tracking rate up to 20 rps (7200°/sec in 14-bit mode (800 Hz option).

Excellent Dynamic Performance. Acceleration constant up to 768000, bandwidth up to 400 Hz.

Small Package. 36-pin DDIP (1.9″ × 0.775″ × 0.21″).

Full Internal Reference Synthesis. Internal circuits compensate for static and dynamic transducer reference to signal phase shifts.

Analog Velocity Output. Analog signal which accurately represents the angular velocity of the input signals.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S47—SPECIFICATIONS

Parameter	AD2S47 Min	Typ	Max	Units	Conditions
ACCURACY					
Resolution		14		Bits	
		16		Bits	
Error (Accuracy)			2.6	arc min	S Options
			1.3	arc min	T Options
REFERENCE INPUT					
Voltage	20		130	V rms	
Frequency	360	400	1000	Hz	400 Hz Options
	700	800	3000	Hz	800 Hz Options
Input Impedance	300			kΩ	Single Ended
	600			kΩ	Differential
Common-Mode Range			250	V dc	Includes Recurrent AC Peak
SIGNAL INPUTS					
Synchro/Resolver					
Input Voltage	8.26	11.8	15.34	V rms	11.8 V Options to Rated Accuracy
	18.2	26.0	33.8	V rms	26.0 V Options to Rated Accuracy
	63.0	90.0	117.0	V rms	90.0 V Options to Rated Accuracy
Input Impedance	35.0			kΩ	11.8 V Options, Single Ended
	70.0			kΩ	11.8 V Options, Differential
	78.0			kΩ	26.0 V Options, Single Ended
	156.0			kΩ	26.0 V Options, Differential
	270.0			kΩ	90.0 V Options, Single Ended
	540.0			kΩ	90.0 V Options, Differential
Matching	0.1			%	All Options
Common-Mode Range	27.0			V peak	11.8 V Options
	60.0			V peak	26.0 V Options
			200.0	V peak	90.0 V Options
Common-Mode Rejection	70			dB	DC to 1 kHz
Harmonic Distortion			10	%	To Full Rated Accuracy
REFERENCE SYNTHESIZER					
Maximum Phase Shift					
Reference to Signal	±45	±60		Degrees	To Full Rated Accuracy
DIGITAL INPUTS					
Logic Levels					
V_{INL}	−0.3		0.8	V dc	V_L = 5 V
V_{INH}	2.4		5.0	V dc	V_L = 5 V
Input Currents					
HBE, LBE		−20		μA	Pulled Down to GND Internally May Be Left Unconnected When Not in Use.
		20		μA	Pulled Up to V_L Internally, May Be Left Unconnected When Not in Use.
DIGITAL OUTPUTS					
(B1–B16, CB, BIT)					
Drive Capability	1			LSTTL Load	
Logic '0'	1.6			mA	@ 0.4 V dc (Sink Current)
Logic '1'	−1.6			mA	@ 3.0 V dc (Source Current)
High 'Z' Output Leakage Current (B1–B16)			±10	μA	
ANALOG OUTPUTS					
V (Bias Voltage)	1.93	2.15	2.37	V dc	V_L = 5 V
E (AC Error)		750		mV rms/°	Referenced to V
Drive Capability	±1			mA	All Analog Outputs

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Min	Typ	Max	Units	Conditions
VELOCITY OUTPUT					
Polarity					Negative for Increasing Input Angle
Scale Factor		0.209		mV/°/sec	800 Hz, 14-Bit Mode (@ +25°C)
		0.835		mV/°/sec	800 Hz, 16-Bit Mode (@ +25°C)
		0.305		mV/°/sec	400 Hz, 14-Bit Mode (@ +25°C)
		1.220		mV/°/sec	400 Hz, 16-Bit Mode (@ +25°C)
Scale Factor Tempco	±500			ppm/°C	
Scale Factor Power Supply Sensitivity			−1	% per %	
Full Scale Output		1.5		V dc @ 7200°/sec	800 Hz, 14-Bit Mode (@ +25°C)
		1.5		V dc @ 1800°/sec	800 Hz, 16-Bit Mode (@ +25°C)
		1.5		V dc @ 5000°/sec	800 Hz, 14-Bit Mode (@ +25°C)
		1.5		V dc @ 1250°/sec	800 Hz, 16-Bit Mode (@ +25°C)
Nonlinearity			±5	% of Full Scale	800 Hz Options
			±2	% of Full Scale	400 Hz Options
			±200	ppm/°C	
Nonlinearity Tempco		0.1		% per %	
Power Supply Sensitivity		±20	±20	mV dc	@ +25°C
Output Offset		±10	±10	%	All Options
Reversion Error					
AUTOMATIC GAIN CONTROL (AGC)					
Range	0.66		1.33	V/V	Converter Performance Is Maintained with ±30% Signal Amplitude Variation
DYNAMIC CHARACTERISTICS					
Tracking Rate	7200			°/sec	800 Hz, 14-Bit Mode
	1800			°/sec	800 Hz, 16-Bit Mode
	5000			°/sec	400 Hz, 14-Bit Mode
	1250			°/sec	400 Hz, 16-Bit Mode
Acceleration Constant (Ka)		768000		/sec	800 Hz, 14-Bit Mode
		192000		/sec	800 Hz, 16-Bit Mode
		192000		/sec	400 Hz, 14-Bit Mode
		48000		/sec	400 Hz, 16-Bit Mode
Bandwidth		400		Hz	800 Hz, 14-Bit Mode
		200		Hz	800 Hz, 16-Bit Mode
		200		Hz	400 Hz, 14-Bit Mode
		100		Hz	400 Hz, 16-Bit Mode
Small Step Settling Time (<1.4°C)			8	ms	800 Hz, 14-Bit Mode
			25	ms	800 Hz, 16-Bit Mode
			16	ms	400 Hz, 14-Bit Mode
			50	ms	400 Hz, 16-Bit Mode
Large Step Settling Time (179°C)			50	ms	800 Hz, 14-Bit Mode
			150	ms	800 Hz, 16-Bit Mode
			100	ms	400 Hz, 14-Bit Mode
			300	ms	400 Hz, 16-Bit Mode
POWER SUPPLY					
Voltage	4.5	5.0	5.5	V dc	To Rated Accuracy
Current		14	32	mA	All Options
Power Dissipation		70	160	mW	All Options
PHYSICAL CHARACTERISTICS	36-Pin Hermetic DDIP				
Dimensions	0.78 × 1.9 × 0.21 Inches (20 × 48 × 5.3 mm)				
Weight	0.6 oz (17 g) Maximum				

Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_L to GND)[1] . . . . . +5 V dc ± 10%

Reference and Single Frequency[2, 3]

400 Hz Options . . . . . 400 Hz ± 10%

800 Hz Options . . . . . 800 Hz ± 10%

Signal Voltage

11.8 V Options . . . . . 11.8 V rms ± 30%

26.0 V Options . . . . . 26.0 V rms ± 30%

90.0 V Options . . . . . 90.0 V rms ± 30%

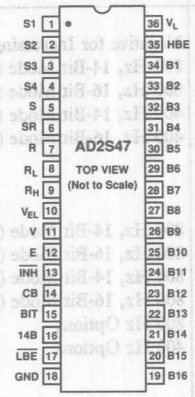
Reference Voltage . . . . . 20 to 130 V rms

Ambient Temperature . . . . . −55°C to +125°C

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PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[4]

Power Supply Voltage (V_L to GND) . . . . . +5.75 V dc
Any Logic Input to GND (Positive) . . . . . +5.50 V dc
Any Logic Input to GND (Negative) . . . . . −0.40 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −55°C to +125°C
Signal Voltage
11.8 V Options . . . . . 18.8 V rms
26.0 V Options . . . . . 41.6 V rms
90.0 V Options . . . . . 144.0 V rms
Reference Voltage . . . . . 180.0 V rms

NOTES
[1]Correct polarity must be maintained on the V_L pin with respect to the ground pin (GND).
[2]Signal and reference harmonic distortion <10%.
[3]Phase shift between reference and signals ±45°C.
[4]Absolute maximum ratings are values beyond which damage to the device will occur.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	S1	Signal input, connect to synchro S1 for synchro operation, connect to resolver Sine Lo for resolver operation.
2	S2	Signal input, connect to synchro S2 for synchro operation connect to resolver Cosine High for resolver operation.
3	S3	Signal input, connect to synchro S3 for synchro operation, connect to resolver Sine Low for resolver operation.
4	S4	Signal input, do not connect for synchro operation, connect to resolver Cosine Low for resolver operation.
5	S	Synchro/Resolver programming pin, connect to SR (Pin 6) for synchro operation, do not connect for resolver operation.
6	SR	Synchro/Resolver programming pin, connect to S (Pin 5) for synchro operation connect to R (Pin 7) for resolver operation.
7	R	Synchro/Resolver programming pin, connect to SR (Pin 6) for resolver operation, do not connect for synchro operation.
8	R_L	Reference low input, connect to reference signal low (ground) side.
9	R_H	Reference high input, connect to reference signal high.
10	V_{EL}	Velocity output dc voltage proportional to the speed of rotation of the input signals. *Negative voltage output for increasing input angle.* Note: Measurement reference for this signal is V, Pin 11.
11	V	Bias signal, measurement reference for velocity and ac error output.
12	E	Error voltage, ac signal at reference frequency proportional to the instantaneous error of the converter. Note: Measurement reference for this signal is V, Pin 11.
13	$\overline{INH}$	Inhibit input. Logic low applied to this pin latches the digital output word and prevents further updates. Does not affect the operation of the tracking loop. Internally pulled high, can be left unconnected for continuous output.
14	CB	Converter Busy. 450 ns wide positive going pulse indicating that an LSB update is occuring. Output data may be read on the trailing (falling) edge of CB.
15	BIT	Build-In-Test. Logic high output indicates either a tracking error of greater the ±1° or a loss of signal or reference connections.
16	14B	Output resolution control, allows operation of the converter in 14-bit mode. Internally pulled high, logic "1" results in the converter operating in 14-bit mode.
17	$\overline{LBE}$	Low Byte Enable. Data output bits DB9 to DB16 enabled when a logic "0" is applied to LBE, internally pulled to ground, so may be left unconnected if the bits DB9 to DB16 are to be permanently enabled.
18	GND	Power supply ground.
19 to 34	DB16 to DB1	Digital output data. Bit 1 (MSB) to Bit 16 (LSB). In 14-bit mode, Bits 15 and 16 will be logic low.
35	$\overline{HBE}$	High Byte Enable. Data output bits DB1 to DB8 enabled when a logic "0" is applied to HBE. HBE is internally pulled to ground and so may be left unconnected if the bits DB1 to DB9 are to be permanently enabled.
36	V_L	Positive power supply, +5 V dc ± 10%

PRELIMINARY TECHNICAL DATA

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14- & 16-Bit, Hybrid Digital-to-Resolver Converters

AD2S65/AD2S66

FEATURES

- Single Rank Transparent TTL or CMOS Compatible Latched Input Registers With High and Low Byte ENABLE
- Accuracy ±1, ±2 or ±4 Arc Minutes
- Resolution 14- or 16-Bit
- Very Low DC Offset Voltage
- Autonulling Option Available (Extremely Low DC Offset Voltage)
- Output Drive Capability 4.3 mA Peak into Resistive, Inductive or Capacitive Loads
- Low Radius Vector Variation 0.03% (Transformation Ratio)
- ±15 V DC Power Supplies Only
- DC to 2.6 kHz Depending on Option (to 10 kHz with Reduced Accuracy)
- Low Power Dissipation
- 32-Pin Welded Metal Package
- Hermetically Sealed
- Protection Against +200% Overload on Analog Input
- Microprocessor Compatible (8 or 16 Bits)

APPLICATIONS

- Polar to Rectangular Coordinate Conversion
- Missile and Fire Control Systems
- Simulation Systems
- Low Frequency Oscillators
- PPI Displays
- Radar and Navigational Systems
- Avionics
- Axis Rotation
- Flight Instrumentation
- Wrap-Around Resolver-to-Digital Converter Tests
- ATE Systems

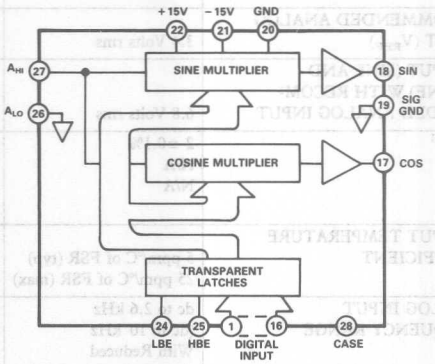
GENERAL DESCRIPTION

The AD2S65 and AD2S66 are hybrid digital-to-resolver converters which accept a 14-bit or 16-bit digital, natural binary input word representing angle, and output sine and cosine voltages.

The AD2S65 and AD2S66 are pin compatible replacements for the previous generation DRC1765 and DRC1766 digital-to-resolver converters, respectively.

The SIN and COS output voltage signals are internally multiplied by the analog input reference voltage, thus the SIN and COS outputs are amplitude modulated at the input reference frequency.

FUNCTIONAL BLOCK DIAGRAM



NOTE: A_{LO}, GND, AND SIG GND ARE INTERNALLY CONNECTED.

The analog input reference voltage can either be dc or ac voltage of frequency up to 10 kHz. For the extremely low dc offset autonulling part, the frequency range is covered by two options, 50 Hz to 2.6 kHz and 360 Hz to 2.6 kHz (both to 10 kHz with reduced accuracy).

The digital input word to the converter is latched with transparent high and low byte ENABLE commands to facilitate easy interface to microprocessor systems. The input latches are TTL and CMOS compatible utilizing components of HCT series.

The devices are available in accuracy grades of ±1, ±2 and ±4 arc minutes. Please see ordering information.

A particularly useful feature of the converters is their low dc output offset voltage (±2.5 mV typ). The autonulling option (see ordering information) offers an extremely low output offset voltage (±0.5 mV typ). The output voltage dc offset remains constant over the frequency range and operating temperature of the converter. The low offset voltage characteristic of this range means that external trim adjustments are not required, particularly important in display and test applications.

The converters have a closed loop bandwidth of 300 kHz and are capable to drive into a load which can be inductive, resistive, capacitive (to the extent of 15 nF) or a combination of above.

A further feature of the converters is that the radius vector variation (Transformation Ratio) is very low at 0.03%. This means that the individual SIN and COS outputs are both independently accurate which is important in coordinate conversion, display applications, simulation and test of resolver-to-digital converters.

	[illegible]	[illegible]	[illegible]	[illegible]	Comments
DIGITAL INPUT RESOLUTION	**14 Bits (1.3 arc min Per Bit)**	**16 Bits (19 arc sec Per Bit)**	**14 Bits (1.3 arc min Per Bit)**	**16 Bits (19 arc sec Per Bit)**	
DIGITAL INPUT FORMAT	Parallel Natural Binary	*	*	*	TTL and CMOS Compatible
RECOMMENDED ANALOG INPUT (V_{REF})	3.4 Volts rms	*	*	*	
OUTPUT (SINE AND COSINE) WITH RECOMMENDED ANALOG INPUT	6.8 Volts rms	*	*	*	Refer to Gain Section
GAIN[1]	2 ±0.1% N/A N/A	* N/A N/A	N/A 1.98 ±0.1% 1.98 ±0.1%	N/A ** **	Option X1Z dc to 2.6 kHz Option X2Z 50 Hz to 2.6 kHz Option X3Z 360 Hz to 2.6 kHz See Figure 4
OUTPUT TEMPERATURE COEFFICIENT	5 ppm/°C of FSR (typ) 25 ppm/°C of FSR (max)	* *	* *	* *	
ANALOG INPUT FREQUENCY RANGE	dc to 2.6 kHz (dc to 10 kHz With Reduced Accuracy) N/A N/A	* * N/A N/A	N/A N/A 50 Hz to 2.6 kHz 360 Hz to 2.6 kHz (to 10 kHz With Reduced Accuracy)	N/A N/A ** **	Option X1Z Option X2Z Option X3Z
ANALOG INPUT IMPEDANCE	10.2 kΩ	*	*	*	±5% Resistive
ANALOG OUTPUT IMPEDANCE	2 mΩ (typ) 20 mΩ (max)	* *	* *	* *	
ANALOG OFFSET VOLTAGE	**±2.5 mV (typ)** **±12 mV (max)**	* *	**±0.5 (typ)** **±2.5 (max)**	*	
OUTPUT DRIVE CAPABILITY	**4.3 mA peak @ ±10 V peak**	*	*	*	
OUTPUT PROTECTION	Outputs May Be Grounded Indefinitely				
RESPONSE TO A STEP INPUT	20 µs (max) to Within Accuracy of Converter. Any Size Step Input	*	*	*	
VECTOR ACCURACY Radius Error Angular Error	 0.03% ±2, ±4 arc min	 * ±1, ±2, ±4 arc min	 * ±2, ±4 arc min	 * ±1, ±2, ±4 arc min	 Refer to Frequency Option. See Figure 3
DIGITAL INPUTS (BIT 1–BIT 16) V_{IH} V_{IL}	 2.0 V dc min 0.8 V dc max	 *	 *	 *	+15 V = 15 V dc I_{IH} = 1 µA I_{IL} = 1 µA
DIGITAL INPUTS (ENABLE M, ENABLE L)[2] V_{IH} V_{IL}	 2.0 V dc min 0.8 V dc max	 *	 *	 *	+15 V = 15 V dc I_{IH} = 1.5 µA I_{IL} = 1.5 µA
DIGITAL INPUTS LEAKAGE CURRENT	±1 µA max	*	*	*	+15 V = 15 V dc
DATA SETUP TIME[2] (DATA TO ENABLE M, L)	40 ns min	*	*	*	+15 V = 15 V dc
HOLD TIME (DATA[2] TO ENABLE M, L)	25 ns min	*	*	*	+15 V = 15 V dc
MINIMUM PULSE WIDTH[2] (DATA TO ENABLE M, L)	40 ns min	*	*	*	+15 V = 15 V dc

POWER SUPPLIES					
+15 Volts	**26 mA (typ) 32 mA (max)**	*	*	*	
−15 Volts	**15 mA (typ) 23 mA (max)**	*	*	*	
TEMPERATURE RANGE					
Operating	−55°C to +125°C	*	*	*	Option 4YZ
	0 to +70°C	*	*	*	Option 5YZ
Storage	−65°C to +150°C	*	*	*	
DIMENSIONS	1.75″ × 1.1″ × 0.225″	*	*	*	
PACKAGE TYPE	32-Pin Bottom Brazed Ceramic T DIP	*	*	*	
WEIGHT	15 Grams (typ)	*	*	*	
	20 Grams (max)	*	*	*	

NOTES
[1]See Figure 4.
[2]ENABLE M enables most significant 8 bits.
ENABLE L enables least significant 6 bits in case of AD2S65, 8 bits in case of AD2S66.
*Specifications same as AD2S65.
**Specifications same as AD2S65AN.
Specifications subject to change without notice.
Specifications shown in **bold face** are tested on all production units at nominal values of power supply, signal voltage and operating frequency.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply
+15 V[2] to GND . . . . . +17 V dc
−15 V[2] to GND . . . . . −17 V dc
Analog Input A_{HI} to A_{LO} (Peak) . . . . . $\pm V_{SUPPLY}$
Common Mode Range . . . . . $\pm V_{SUPPLY}$
Any Logical Input to GND . . . . . −0.4 V dc to +5.5 V dc
Case to GND . . . . . ±20 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
Extended Temperature . . . . . −55°C to +125°C
Commercial Temperature . . . . . 0 to +70°C

NOTES
[1]Absolute maximum ratings are those values beyond which damage to the device may occur.
[2]Correct polarity voltages must be maintained on the +15 V and −15 V pins.

RECOMMENDED OPERATING CONDITIONS

Power Supply
+15 V[1] . . . . . +15 V dc
−15 V[1] . . . . . −15 V dc
Analog Input[2] A_{HI} to A_{LO} . . . . . 3.4 V rms
Analog Input Frequency Range
Option X1Z . . . . . dc to 2.6 kHz
Option X2Z (Autonulling) . . . . . 50 Hz to 2.6 kHz
Option X3Z (Autonulling) . . . . . 360 Hz to 2.6 kHz
Digital Input Format . . . . . Parallel Natural Binary
Operating Temperature Range
Option 4YZ (Extended) . . . . . −55°C to +125°C
Option 5YZ (Commercial) . . . . . 0 to +70°C

NOTES
[1]Power supply tolerance (+15 V, −15 V) ±5%.
[2]The analog input voltage may vary to user's requirements from below 1 V rms to 4.2 V rms in simulation and test applications where the required output voltage is in the range of 2 V rms to 8.4 V rms (11.9 V peak).

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB AD2S65)	0.0220
15	0.0110
16 (LSB AD2S66)	0.0055

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



The power consumption of the AD2S65 and AD2S66 is particularly low by utilizing HCT series latches and only requires ±15 volt power supply rails.

An additional feature of the converters is the extended operating frequency range, dc to 10 kHz for the standard products, 50 Hz, 360 Hz to 10 kHz for the autonulling options; please see the appropriate graphs for accuracy and gain versus frequency.

Separate ENABLE inputs for the high and low bytes facilitate easy interface to any 8- or 16-bit microprocessor system bus.

The converters are housed in a 32-pin DIP solid sidewall hybrid metal package and are hermetically sealed.

MODELS AVAILABLE

The AD2S65 has a resolution of 14 bits (1.3 arc min) and is available with accuracies of ±2 and ±4 arc minutes. The AD2S66 has a resolution of 16 bits (19 arc sec) and is available with accuracies of ±1, ±2 and ±4 arc minutes. Both models operate over the frequency range dc to 2.6 kHz and with reduced accuracy to 10 kHz.

There is the autonulling option available to both models; the accuracies are the same as above, but the operating frequency range is 50 Hz to 2.6 kHz and 360 Hz to 2.6 kHz, both with reduced accuracy to 10 kHz.

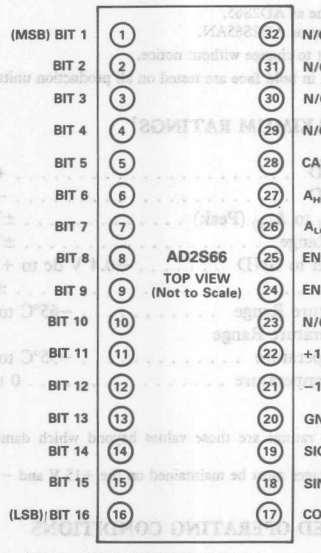
Models are available to operate over the military temperature range (−55°C to +125°C) and also the commercial temperature range (0 to +70°C).

All models are available processed with high reliability screening standards (Suffix B) which receive further levels of testing and screening to ensure high levels of reliability. More information about the option codes is given under the heading Ordering Information.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1–16	Bit 1–16 (AD2S66)	Parallel digital input angle.
1–14	Bit 1–14 (AD2S65)	Bit 15 and Bit 16 are N/C.
17	COS	Cosine signal output.
18	SIN	Sine signal output.
19	SIG GND	Output signals ground connection (0 V).
20	GND	Power supply 0 V connection.
21	−15 V	Main negative power supply.
22	+15 V	Main positive power supply.
23	N/C	No connection.
24	ENABLE L	Input latch enables the 8 (AD2S66) or 6 (AD2S65) least significant bits.
25	ENABLE M	Input latch enables the 8 most significant bits. Logic HI causes the input to appear transparent, the converter output follows the changes on the digital input. Logic LO the converter output will be latched at the level of previous digital input.
26	A_{LO}	Input pin for the reference signal.
27	A_{HI}	Input pin for the reference signal.
28	CASE	Should be connected to 0 V (GND).
29	N/C	No connection.
30	N/C	No connection.
31	N/C	No connection.
32	N/C	No connection.

PIN CONFIGURATION



NOTE: FOR AD2S65, BIT 14 IS LSB.
BIT 15 AND BIT 16 ARE NOT CONNECTED.

THEORY OF OPERATION

The analog input reference voltage signal ($V_i \sin \omega t$) applied between A_{HI} (analog input HI) and A_{LO} (analog input LO), is multiplied by both $\sin\theta$ and $\cos\theta$, where θ is the angle represented by the digital input word.

The resultant resolver format output voltages at pins sin and cos are:

$V_O \sin = GV_i \sin \omega t \sin \theta$ (sine output)
$V_O \cos = GV_i \cos \omega t \cos \theta$ (cosine output).

Note: Converter Gain G is typically ×2 (input to output). There is a reduction of 1% due to autonull circuit (see relevant options). Please see specifications section and graphs of gain versus frequency.

All the signal inputs and outputs are with reference to SIG GND (Signal Ground).

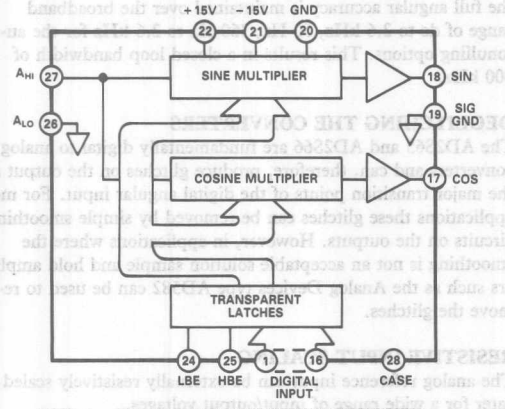


Figure 1. AD2S65/AD2S66 Functional Block Diagram

CONNECTING THE CONVERTER

The connections to the AD2S65 and AD2S66 are very straightforward.

The digital inputs should be connected to the converter using Pins 1 (MSB) through 14 (LSB) in the case of the AD2S65 and through 16 (LSB) in the case of the AD2S66. The format of the digital angular input is shown at the "Bit Weight Table" section.

The digital input control lines should be connected as described under the "Digital Data Input" section.

The analog input reference voltage (V_{REF}, A_{HI} to A_{LO}) should be connected to A_{HI}. It should be noted that this is a single ended amplifier input where A_{LO} is grounded internally (also connected to GND and SIG GND). If it is desired, the V_{REF} signal input can be externally isolated using the STM1680 or 5S72 series of reference input step down transformers.

Alternatively the analog input reference voltage, V_{REF}, can be externally resistively scaled to cater for a wide range of input voltages. Please see the section on "Resistive Input Sealing."

The CASE pin is joined to the case which is isolated and should be connected to a convenient zero potential (GND) point in the system.

The sine and cosine voltage outputs are taken from the SIN and COS pins with SIG GND as the common connection.

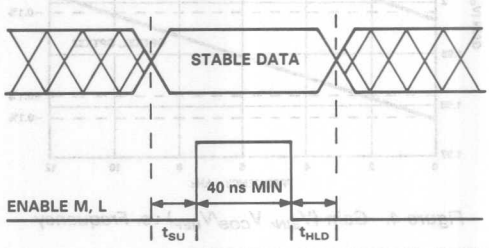
DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches are both CMOS and TTL compatible (type 54HCT373).

The ENABLE M input controls the input of the most significant 8 bits, and the ENABLE L input controls the input of the least significant 6 bits in the case of AD2S65, 8 least significant bits in the case of AD2S66.

A logic HI on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital inputs. When ENABLE M and ENABLE L are taken to a logic LO, the converter output will be latched at the SIN, COS voltage levels (angle) represented by the digital input data at the low going edge of the ENABLE L, M. The SIN, COS voltage outputs will remain constant until the ENABLE L, M are taken to a HI logic state again.

If the latches are not required, ENABLE M and ENABLE L can be left open circuit, as they are internally pulled up by 12.5 kΩ resistors. The timing diagram in Figure 2 illustrates the use of ENABLE M and ENABLE L control inputs.



NOTE: INTERNAL LATCHES ARE TYPE 54HCT373.

Figure 2. Data Transfer Diagram

Internal resistive pull ups are employed only on the ENABLE M, ENABLE L digital inputs and are not necessary for the digital control angular data inputs as the HCT series latches are both TTL and CMOS compatible.

DEGRADATION OF ACCURACY OVER FREQUENCY

The AD2S65 and AD2S66 have guaranteed accuracies as stated in the specifications section from dc to 2.6 kHz and 50 Hz, 360 Hz to 2.6 kHz for the autonull options. However all devices operate satisfactorily to 10 kHz with reduced accuracy.

Figure 3 represents typically the angular accuracy degradation over the range of frequencies dc to 10 kHz for the standard part (Option X1Z) and the autonull parts (Options X2Z and X3Z).

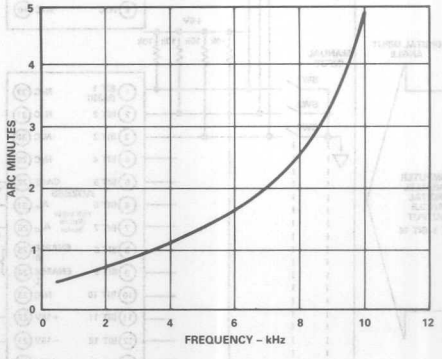


Figure 3. Accuracy vs. Frequency

GAIN VARIATION OVER FREQUENCY

The gain (input to output SIN, COS voltages) of the standard part is ×2 ±0.1% (Option X1Z) over the frequency range dc to 2.6 kHz. As can be seen from Figure 4, the gain at 10 kHz is ×2.02 ±0.1%.

2.6 kHz. From Figure 4 can be seen that the gain for the autonull part is typically ×2 + 0.1% at 10 kHz.

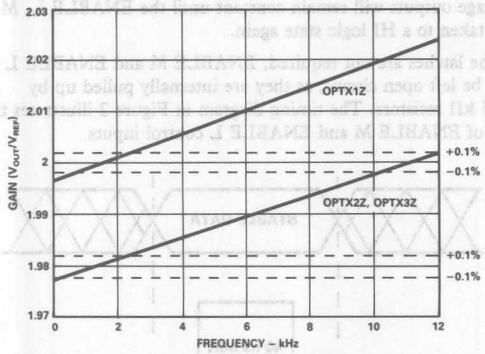


Figure 4. Gain (V_{SIN}, V_{COS}/V_{REF}) vs. Frequency

VECTOR ERRORS AND EFFECTS

The error law used in the converter has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the internal components used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays and resolver-to-digital converter testing.

BANDWIDTH

The dynamic characteristics of the AD2S65 and AD2S66, including the autonulling option, have been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6 kHz, 50 Hz, 360 Hz to 2.6 kHz for the autonulling options. This results in a closed loop bandwidth of 300 kHz.

DEGLITCHING THE CONVERTERS

The AD2S65 and AD2S66 are fundamentally digital to analog converters and can, therefore, produce glitches on the output at the major transition points of the digital angular input. For most applications these glitches can be removed by simple smoothing circuits on the outputs. However, in applications where the smoothing is not an acceptable solution sample and hold amplifiers such as the Analog Devices type AD582 can be used to remove the glitches.

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of input/output voltages.

A resistance of value 3 kΩ per extra volt required (in excess of 3.4 V rms) should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI} to A_{LO}) does not exceed 4.2 V rms (8.4 V rms, 11.9 V peak at SIN, COS outputs) otherwise clipping may occur due to lack of voltage supply headroom for the internal output amplifiers.

The recommended input is 3.4 V rms for a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and therefore the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} input pins.

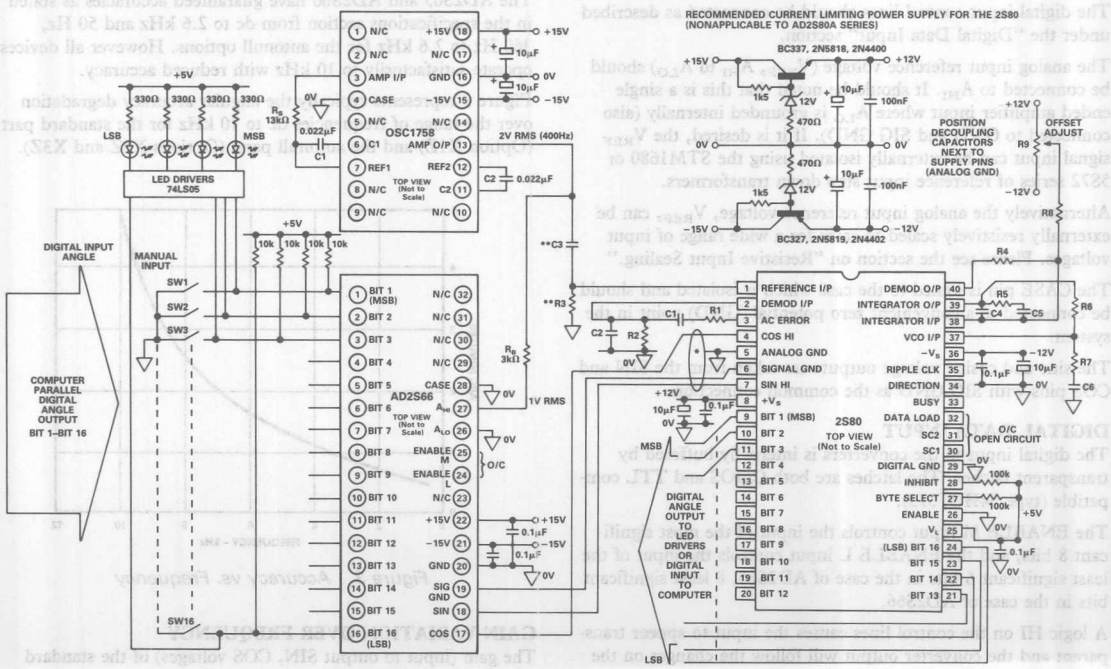


Figure 5. Application Circuit: Resolver-to-Digital Converter (2S80) Testing Using the AD2S66

The diagram Figure 5 shows a "hookup" for resolver-to-digital converter testing, with the digital-to-resolver converter (AD2S66), power oscillator (OSC1758) and the resolver-to-digital converter (2S80). Using a similar circuit, 2S81, 2S82, 1S20, 1S40, 1S60, 1S24, 1S44, 1S64 and 1S74 R/D converters can be tested.

Current Set Resistor (R_S)
This resistor is used to reduce the voltage output of the oscillator to 2 V rms so it can be used as the reference input to the 2S80.

$$R_S = \frac{37.5 \times 10^3}{V_{OUT}\,(rms)} - 5350\ \Omega$$

for 2 V rms output R_S = 13 k Ohms

Frequency of Oscillation
The frequency of oscillation for the OSC1758 is determined by the two external capacitors, C1 and C2. These should be calculated as follows:

$$C1 = C2 = \frac{1}{F_{OSC} \times 10^5}\ F$$

where F_{OSC} = frequency of oscillation in Hz for 400 Hz frequency C1 = C2 = 0.022 μF.

Decoupling
The DRC and oscillator have internal high frequency decoupling capacitors on the supply lines. However, it is recommended that electrolytic decoupling capacitors are connected close to the hybrid power supply pins. Please see decoupling recommendations in relevant data sheets.

Circuit Description
The OSC1758 generates 2 V rms, of nominal frequency 400 Hz, to be applied at the REFERENCE I/P of the 2S80. The signal is further attenuated by resistor R_B and applied to A_{HI} input of the AD2S66 (V_{REF}) which generates SIN and COS signals, as per digital input angle, at 400 Hz.

The digital input angle can be set either manually by selection of the switches SW1 (MSB) to SW16 (LSB) or by the digital parallel outputs of a computer or by means of a 16-bit counter which consists of 74LS193 and driven by a square wave oscillator. The digital input angle may be displayed, if so desired, by means of LEDs and visually compared with the digital outputs of the 2S80 RDC also displayed by LEDs.

Alternatively, the digital angle position outputs of the 2S80 may be connected to a 16-bit parallel input port of a computer, which can compare digital input angle to digital output angle and compute the error.

2S80 R-to-D Converter External Components
Please consult the appropriate date sheet as the external components which set the dynamic performance characteristics of the converter are user selectable. There is available, on request, PC compatible software to help users select the optimum values of the external components for the desired application.

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

MTBF in hours versus case temperature in naval sheltered conditions for AD2S65/AD2S66.

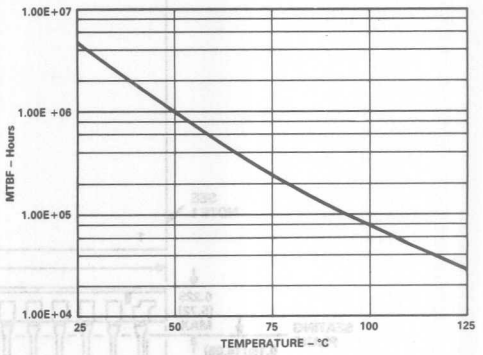


Figure 6. AD2S65/AD2S66 MTBF Curve

OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The DRC1745 (14 bit) and DRC1746 (16 bit) are hybrid resolver-to-digital converters with internal power amplifiers capable of driving a 2 VA load.

The STM1683 series are output transformers used in conjunction with the DRC1745 and DRC1746, operate over the frequency range of 360 Hz to 2.6 kHz and can be Scott T connected to provide all the standard synchro output formats over the frequency range dc to 2.6 kHz.

The 2S80 and 2S82 are monolithic, variable resolution 10-, 12-, 14- and 16-bit tracking resolver-to-digital converters that feature user selectable dynamic performance and operate over the reference frequency range 50 Hz to 20 kHz, with accuracies of ±2, ±4, ±8 arc min (2S80 and 2S82) and 22 arc min (2S82).

The 2S81 is a low cost, monolithic tracking resolver-to-digital converter with fixed 12-bit resolution, user selectable dynamic performance over the frequency range 50 Hz to 20 kHz and accuracy 30 arc min.

The AD2S75 is a transformer isolated universal synchro and resolver pin programmable interface. All standard synchro and resolver signal and reference voltages are accepted and transformed to 2 V rms, resolver format signals for use with the 2S80 series monolithic resolver-to-digital converters.

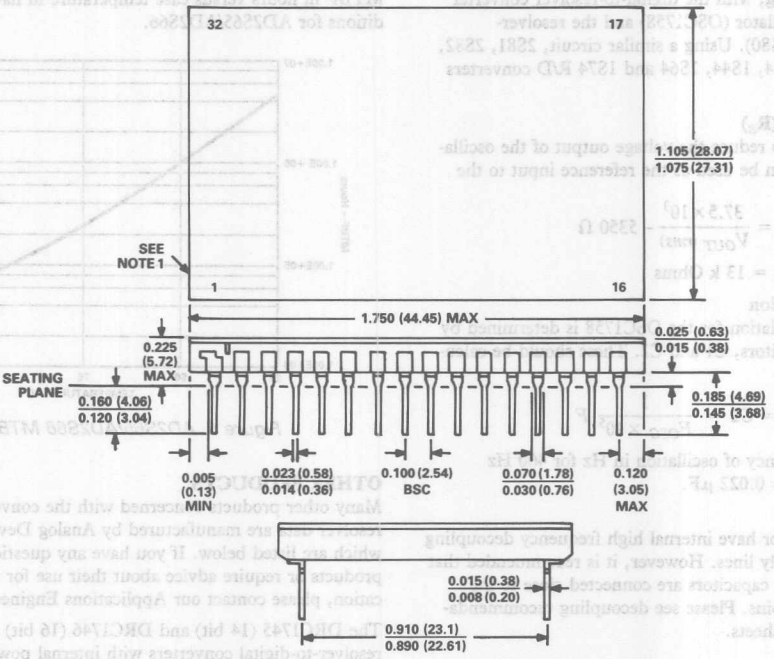
The 1740 series are hybrid 14- or 12-bit continuous tracking synchro or resolver-to-digital converters featuring internal microtransformers for signal isolation.

The OSC1758 is an excitation oscillator for supplying reference signals to synchros, resolvers and Inductosyns* and associated converters.

*Inductosyn is a registered trademark of Farrand Industries, Inc.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.

AD2S6N/ X Y Z B

- B — High-Rel Processing (Applicable X = 4)
- Z = 1 ±1 arc min Accuracy (AD2S66 Only)
- Z = 2 ±2 arc min Accuracy
- Z = 4 ±4 arc min Accuracy
- Y = 1 Bandwidth dc–2.6 kHz
- Y = 2 Bandwidth 50 Hz–2.6 kHz (Autonull Option)
- Y = 3 Bandwidth 360 Hz–2.6 kHz (Autonull Option)
- X = 4 −55°C to +125°C Operating Temperature Range
- X = 5 0 to +70°C Operating Temperature Range

AD2S65 = 14-Bit Resolution
Accuracy Z = ±2, ±4 arc min

AD2S66 = 16-Bit Resolution
Accuracy Z = ±1, ±2, ±4 arc min

Universal Synchro/Resolver Transformer Isolated Interface

AD2S75

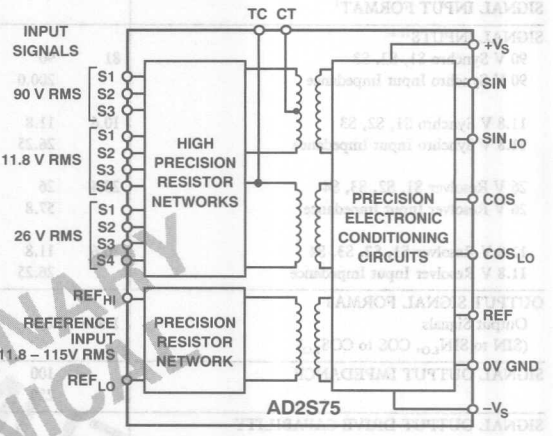
FEATURES

Universal Transformer Isolated Synchro/Resolver Interface
Supports All the Standard Synchro/Resolver Voltages
High Accuracy over Full Military Temperature Range
Wideband Performance: 56 Hz to 20,000 Hz
Not Achievable with Conventional Transformers
Wide Power Supply Range: ±4.75 to ±15.75 V DC
1000 V DC Transformer Isolation
Dimensions: 1.37 × 1.1 × 0.3 inch
(35 × 27.7 × 7.6 mm)

APPLICATIONS

Universal Synchro/Resolver Interface
Military Systems/Equipment
Avionics
Naval Systems
Factory Automation
Interfaces to the Following R/DCs 2S80/81/82, AD2S80A/81A/82A, AD2S46, AD2S44, AD2S34
Transformer Isolator, Signal Buffer, Signal Conditioning

BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S75 is a functionally complete, analog signal conditioning transformer interface for all the standard synchro/resolver format signals.

The AD2S75 performs synchro-to-resolver and resolver-to-resolver signal transformations. The device features signal inputs for 90 V rms, 26 V rms and 11.8 V rms, and outputs 2 V rms resolver format signals (sine and cosine). The reference frequency input accepts sinusoidal signals in the range 11.8 V rms to 115 V rms and outputs a nominal voltage of 2 V rms with enhanced zero crossing definition.

All inputs are isolated from the outputs and power supply lines by use of patent design miniature transformers thus providing true galvanic isolation. On the secondary (low side) of the isolation transformers, analog signal conditioning circuits are used to sustain the performance and stabilize the device over the wide operating temperature range as well as over the broad range of reference frequency.

The AD2S75 is a wide bandwidth device which operates over a reference frequency range of 56 Hz to 20,000 Hz. This covers the majority of commercially available synchros and resolvers for military and industrial use, thus providing the isolated interface for these types of transducers. The AD2S75 operates over the wide range of ±5 V dc to ±15 V dc nominal power supplies without degradation in accuracy or a reduction in the range of reference frequency.

The AD2S75 is designed to operate over the full military temperature range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

Complete Synchro/Resolver Interface. The AD2S75 is a universal synchro/resolver interface for resolver-to-digital converters that accept 2 V rms resolver format signals. All the standard synchro/resolver voltages are catered for, thus eliminating the need for different voltage option devices to be ordered and to be held in stock.

1000 V DC Transformer Isolation. The AD2S75 continues the transformer isolated SDC/RDC tradition from Analog Devices. The internal miniature transformers present a balanced input regardless of other equipment that may be connected to the synchro, or resolver.

True Galvanic Isolation. 1000 V dc input to output isolation regardless of input voltage amplitude level. The galvanic isolation completely eliminates ground loops between the transducer and the converter, thus minimizing errors.

High Common-Mode Voltage consistent across all input voltage ranges. Electronic solid state conditioning circuits are input voltage amplitude dependent.

Isolating Transformers in conjunction with the high common-mode voltage range, allow compliance with lightening strike protection requirements.

Ratiometric Inputs. Eliminate errors due to parasitic capacitance effects and enhance the accuracy performance of synchros and resolvers.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S75—SPECIFICATIONS (typical at +25°C unless specified otherwise)

Parameter	Min	Typ	Max	Units	Comments/Test Conditions
ACCURACY[1]					
60–209 Hz		1.3	**2.0**	arc min	Reference Frequency, Accuracy Tested at 60,
210–4099 Hz		0.5	**0.66**	arc min	400, 2600 and 10,000 Hz
4100 Hz–11.000 Hz			**1.0**	arc min	
11000 Hz–20000 Hz			2.0	arc min	
ACCURACY TEMPCO[1]		0.0033		arc min/°C	
SIGNAL INPUT FORMAT[1]					Either Synchro or Resolver
SIGNAL INPUTS[1, 2]					
90 V Synchro S1, S2, S3	81	90	99	V rms	Line to Line
90 V Synchro Input Impedance		200.0		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
11.8 V Synchro S1, S2, S3	10.6	11.8	13	V rms	Line to Line
11.8 V Synchro Input Impedance		26.25		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
26 V Resolver S1, S2, S3, S4	23.4	26	28.6	V rms	Line to Line
26 V Resolver Input Impedance		57.8		kΩ	Resistive, Tolerance ±0.1% (Including Transformer Winding Resistance)
11.8 V Resolver S1, S2, S3, S4	10.6	11.8	13	V rms	Line to Line
11.8 V Resolver Input Impedance		26.25		kΩ	
OUTPUT SIGNAL FORMAT					Resolver Format 2 V rms
Output Signals (SIN to SIN_{LO}, COS to COS_{LO})	**1.990**	2	**2.010**	V rms	Tested with Nominal Input Voltage at 400 Hz
SIGNAL OUTPUT IMPEDANCE		100	200	mΩ	at 400 Hz
		250	450	mΩ	at 10,000 Hz
SIGNAL OUTPUT DRIVE CAPABILITY			100	pF	
SIGNAL CURRENT OUTPUT DRIVE	4.3	20		mA peak	Minimum Refers to Operation with Supplies $\pm V_S = \pm 5$ V dc
SIGNAL OUTPUT OFFSET SIN, COS		2	5	mV dc	Measured across SIN, SIN_{LO} and COS, COS_{LO}
OUTPUT SIGNAL PHASE SHIFT					SIN, COS with Respect to Reference,
60–200 Hz		0.66	1.0	degrees	Measured at Zero Crossings,
201–2700 Hz		0.25	0.5	degrees	Average of Both Alignments.
2701–20000 Hz		150	450	ns	Propagation Delay
OUTPUT SIGNALS DIFFERENTIAL PHASE SHIFT					SIN with Respect to COS, Measured at
60–200 Hz		0.66	0.88	degrees	Zero Crossings, Average of Both
201–2700 Hz		0.25	0.33	degrees	Alignments.
2701–20000 Hz		80	120	ns	Propagation Delay
REFERENCE INPUT SIGNAL VOLTAGE[1, 2]	8.0	11.8–115	130	V rms	Reference Frequency = 60 Hz to 20000 Hz
Reference Input Impedance		81		kΩ	Resistive, Tolerance ±2%
REFERENCE OUTPUT VOLTAGE SIGNAL					Zero Crossing Transition Enhanced Waveform
I/P 11.8 V rms	**1.2**	1.4	**1.6**	V peak	(See Figure 8). Output Signal Consists of a
I/P 26 V rms	**1.5**	1.8	**2.0**	V peak	1.1 V Square Wave (at Reference Frequency)
I/P 115 V rms	**3.0**	3.4	**3.7**	V peak	on Which Is Superimposed a Sinusoid of Amplitude 1/75 of Reference Input Amplitude.
REFERENCE OUTPUT VOLTAGE TEMPCO		4.4		mV/°C	
REFERENCE OUTPUT IMPEDANCE		400	860	mΩ	at 400 Hz
		550	1200	mΩ	at 10,000 Hz
REFERENCE OUTPUT DRIVE CAPABILITY			100	pF	See Load Considerations
REFERENCE CURRENT OUTPUT DRIVE	**3**	10		mA peak	Minimum Refers to Operation with Supplies $\pm V_S = \pm 5$ V dc
TRANSFORMER ISOLATION[3]					
Input to Output	**±1000**			V dc	With Respect to Grounded Secondary
Common-Mode Range	600			V rms	
Input to Case (GND)	**±1000**			V dc	
POWER SUPPLIES					
Voltage Levels					
$+V_S$	+4.75		+15.75	V dc	
$-V_S$	−4.75		−15.75	V dc	

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Min	Typ	Max	Units	Comments/Test Conditions
Quiescent Current					
$+I_S$		13	18	mA	$+V_S$ = +5 V dc
$-I_S$		13	18	mA	$-V_S$ = −5 V dc
$+I_S$		15	20	mA	$+V_S$ = +15 V dc
$-I_S$		15	20	mA	$-V_S$ = −15 V dc
Power Dissipation			180	mW	$\pm V_S$ = ±5 V dc
			600	mW	$\pm V_S$ = ±15 V dc
POWER SUPPLY REJECTION RATIO		0.05	0.1	arc min	See Note 4
DIMENSIONS		1.37 × 1.1 × 0.3		inch	See Package Information
		34.8 × 27.7 × 7.6		mm	
WEIGHT		20	21	gm	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) 10% reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

[2]For power supply voltages $\pm V_S$ less than ±6 V dc, signal and reference input voltage overdrive should be constrained to ±5% maximum.

[3]The primary (high voltage) winding(s) of the transformer(s) are floating. There is ±1000 V dc galvanic isolation between primary and secondary (low voltage) windings. All active components are located on the secondary side of the transformers. This guarantees ±1000 V dc galvanic isolation between the primary windings and the signal(s), power supply connections on the secondary side.

[4]The figure above is not an additional error. It represents the worst case contribution to the angular error caused by variation of power supplies over the range ±5 V dc to ±15 V dc, with nominal signal input voltages.

Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal and reference voltage amplitude and operating frequency. All other parameters are guaranteed by design and are not tested.

Specifications subject to change without notice.

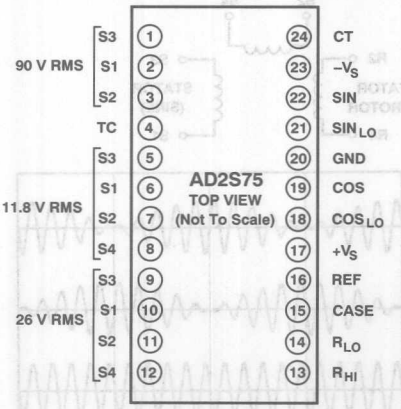
ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND[1] . . . . . +17.25 V dc
$-V_S$ to GND[1] . . . . . −17.25 V dc
Reference Input HI to GND . . . . . ±1000 V dc
Reference Input LO to GND . . . . . ±1000 V dc
Common-Mode Range . . . . . 700 V rms
S1, S2, S3, S4 to GND . . . . . ±1000 V dc
Case to GND . . . . . ±1000 V dc
Case Operating Temperature Range . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C

CAUTION

[1]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins and must not be reversed.

PIN CONFIGURATION



ORDERING GUIDE

Model	Operating Temperature Range	Package Option
AD2S75AM	−40°C to +85°C	M-24
AD2S75SMB	−55°C to +125°C	M-24

PIN DESCRIPTION

Pin	Mnemonic	Description
1, 2, 3	S3, S1, S2	90 V rms Synchro Signal Inputs
4	TC	"TEASER" winding-connect to CT, Pin 24, for Synchro input signals. Do not connect for Resolver signals.
5 6 7 8	S3 S1 S2 S4	11.8 V rms Synchro signal inputs to S3, S1, S2. (S4 not connected) 11.8 V rms Resolver signal inputs (SINE) to S3, S1, (COSINE) to S2, S4. For Resolver, S3–S1 is the effective SINE signal, S2–S4 is the effective COSINE signal.
9 10 11 12	S3 S1 S2 S4	26 V rms Resolver signal inputs (SINE) to S3, S1, (COSINE), to S2, S4. For Resolver, S3–S1 is the effective SINE signal, S2–S4 is the effective COSINE signal. 26 V rms Synchro signal inputs (non standard) to S3, S1, S2, do not connect S4.
13	R_{HI}	Reference Input HI Synchro and Resolver.
14	R_{LO}	Reference Input LO Synchro and Resolver.
15	CASE	Connect to 0 V, GND Pin 20.
16	REF	Reference output signal connect to R/DC. Reference output measured with respect to 0 V, GND Pin 20.
17	$+V_S$	Positive power supply line +5 V dc to +15 V dc
18	COS_{LO}	Cosine output signal return.
19	COS	Cosine output signal. Connect to COS Input of R/DC.
20	GND	Analog ground, 0 V power supplies common.
21	SIN_{LO}	Sine output signal return.
22	SIN	Sine output signal. Connect to SIN input of R/DC.
23	$-V_S$	Negative power supply line −5 V dc to −15 V dc.
24	CT	Center tap of primary windings. Synchro input signals only—connect to TC Pin 4. Resolver signals do not connect. See connection diagrams.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

A synchro is an electromagnetic rotational transducer (forerunner of the resolver) that detects angular displacement. The synchro consists of a fixed stator, which houses three pickup windings which are star connected, 120° apart. The rotor contains the ac excitation (Reference) winding which is connected to terminals via slip rings and brushes.

The voltage induced in any stator winding, by the rotor, will be proportional to the sine of the angle θ between the rotor coil axis and the stator coil axis.

The voltage induced across any pair of stator terminals will be the sum or the difference, depending on the phase of the voltages across the two coils concerned.

The excitation voltage of the rotor, applied across R1 and R2, is of the form:

A sin ωt

The voltages which would appear across the stator terminals will be:

S3 to S1 = AR sin ωt sin θ
S2 to S3 = AR sin ωt sin (θ + 120°)
S1 to S2 = AR sin ωt sin (θ + 240°)

where:

R = transformation ratio of the transducer.
A = amplitude of the excitation voltage signal.
sin ωt = excitation frequency.
θ = the synchro shaft angle.

Note: The S1, S2 and S3 outputs for synchros are **phase coherent signals**.

An equivalent electrical representation and diagram of the typical output signal formats for a synchro are shown in Figure 1.

Note: Standard notation for the rotation of synchros is counter clockwise (CCW) shaft movement for an increasing angle as viewed from the transducer shaft end.

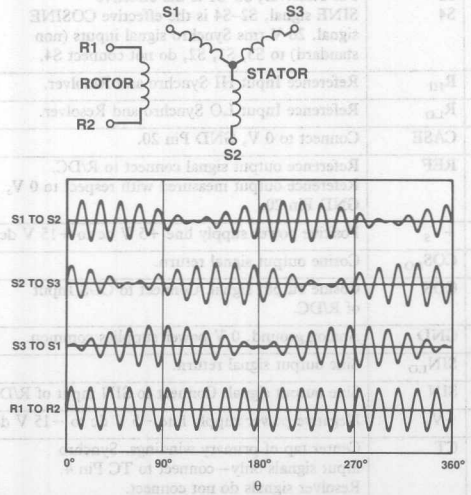


Figure 1. Electrical Representation and Typical Synchro Signals

A resolver is an electromagnetic, rotational transducer that detects angular displacement. Most modern resolvers are "brushless." An ac excitation (reference) signal is applied to the stator (primary reference winding); in turn a voltage is induced in the rotor which subsequently induces a voltage in two pickup windings sine and cosine, which are also located in the stator (secondaries), spaced 90° apart.

The induced voltages (secondaries) ratios are amplitude modulated by the sine and the cosine of the angle θ of the rotor relative to the stator.

The excitation voltage is of the form:

A sin ωt

The voltages which would appear across the stator terminals will be:

Sine: S3 to S1 = AR sin ωt sin θ
Cosine: S2 to S4 = AR sin ωt cos θ

where:

A = amplitude of the excitation voltage signal
R = transformation ratio of the transducer
sin ωt = excitation frequency
θ = the resolver shaft angle

Note: the S1, S2, S3 and S4 outputs for resolvers are **phase coherent signals**.

An equivalent electrical representation and diagram of the typical output signals format for a resolver are shown in Figure 2.

Note: Standard notation for the rotation of resolvers is clockwise (CW) shaft movement for an increasing angle as viewed from the transducer shaft end.

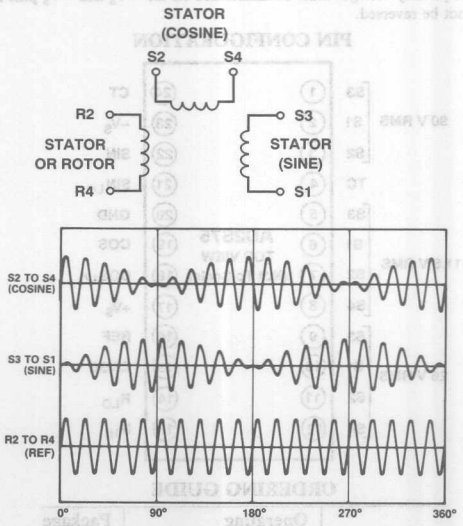


Figure 2. Electrical Representation and Typical Resolver Signals

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AD2S75 USER BENEFITS

The AD2S75 is a user friendly interface device which minimizes many potential sources of error. However errors can occur due to the nonideal generation of the transducer signals and their subsequent distribution, limitations such as:

- Finite output impedance of the transducer.
- Imbalance between transducer impedances.
- Imbalance in chassis wiring impedances.

These errors are minimized by the use of the AD2S75 which employs balanced, high precision, high impedance, transformer isolated, input networks. This allows system accuracies to be maintained, even when long chassis wiring runs are required between synchro/resolver transducer and the AD2S75. Accuracy is maintained by the simple control of resistive balance of the transducer signals. This overall balance requirement is dominated by the precision input resistor network; which greatly reduces the balance requirements placed on the transducer and associated chassis wiring. When using the AD2S75, the sensitivities to signal distribution imbalance (mismatch) are of the order:

Synchro	90 V	87.3 Ω/arc min or 28.8 Ω/bit in 16
	11.8 V	11.4 Ω/arc min or 3.8 Ω/bit in 16
Resolver	26 V	16.8 Ω/arc min or 5.5 Ω/bit in 16
	11.8 V	7.6 Ω/arc min or 2.5 Ω/bit in 16

Thus 22 AWG wire at 17 mΩ per foot and PCB tracking using 0.012 inch 1 oz. Cu at 400 mΩ per foot will not introduce significant errors provided simple control of resistive balance is maintained.

The use of the AD2S75 eliminates errors due to ill defined ground loop currents. This is achieved by the galvanic isolation of the internal transformers and strict adherence to analog star point sensing internal to the AD2S75, and between the AD2S75 and the RDC as shown in the following connection diagrams.

Errors due to signal loading effects on the SIN and COS outputs are minimized by providing balanced, low output impedances, together with distinct and separate four wire transmission for SIN, SIN_{LO} and COS, COS_{LO}. Full angular accuracy is maintained from zero to maximum output current drive capability.

Capacitive loading considerations (100 pF maximum) indicate that the AD2S75 should be sited close to its load, often a 2S80. Provided the capacitive loading limits are met, then the AD2S75 can be sited in accordance with user preference.

CONNECTING THE TRANSDUCERS TO THE AD2S75 INTERFACE

Synchro

Synchros are available in two standard voltage ranges:

(a) 90 V rms line-to-line signals, 115 V rms reference, nominal frequency 400 Hz or 60 Hz.

(b) 11.8 V rms line-to-line signals, 26 V rms reference, nominal frequency 400 Hz.

For nonstandard voltages, please see section "Resistive Scaling of Inputs."

The signals from the synchro should be connected to the appropriate inputs. Refer to pin configuration diagram.

90 V: connect S3 to Pin 1, S1 to Pin 2, S2 to Pin 3.
11.8: connect S3 to Pin 5, S1 to Pin 6, S2 to Pin 7.

Note: S4 (Pin 8) should be left unconnected for synchro signals and connected for use with 11.8 V resolver signals only.

TC, Pin 4 should be connected to CT, Pin 24.

The reference input signal, either 115 V or 26 V, should be connected to R_{HI} and R_{LO}, Pins 13 and 14, respectively.

After the synchro output signals have been connected and the devices have been powered up, the synchro signals transformed to resolver signals should be as shown in Figures 1 and 2, respectively.

Note that the standard notation for the rotation of a synchro, for increasing angle is counter clockwise (CCW) as viewed from the transducer's shaft end.

Resolver

Resolvers are available in a variety of voltages. The three standard voltage ranges (most common) are:

(a) 11.8 V rms, line-to-line signals, 11.8 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

(b) 26 V rms, line-to-line signals, 26 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

(c) 11.8 V rms, line-to-line signals, 26 V rms reference, various frequencies between 400 Hz to 10,000 Hz.

For nonstandard voltages, please refer to section "Resistive Scaling of Inputs."

The signals from the resolver should be connected to appropriate inputs. Refer to pin configuration diagram.

11.8 V: Connect the Sine signal to S3, S1, Pins 5 and 6, S1 being the voltage measurement reference point. Connect the Cosine signal to S2, S4, Pins 7 and 8, S4 being the voltage measurement reference point.

26 V: Connect the Sine signal to S3, S1, Pins 9 and 10, S1 being the voltage measurement reference point. Connect the Cosine signal to S2, S4, Pins 11 and 12, S4 being the voltage measurement reference point.

TC Pin 4 and CT Pin 24 should not be connected.

The reference input signal should be connected to R_{HI} and R_{LO}, Pins 13 and 14, respectively.

After the connections have been completed and the devices have been powered up, the output signals from the AS2S75 should be as shown in Figure 2.

Note that the standard notation for the rotation of a resolver, for increasing angle is clockwise (CW), as viewed from the transducer's shaft end.

PRELIMINARY TECHNICAL DATA

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GENERAL GOOD ENGINEERING PRACTICE

The AD2S75 offers the user numerous benefits. This section describes techniques which will enable the user to achieve the specified performance of the device.

Wiring Practice

The recommended cable for interconnecting synchros to equipment is a three-way twisted cable. Such a cable will eliminate any radiated electromagnetic interference, and will have minimum capacitance as there is no need for an earthed screen. This will also present a balanced load to the transducer.

The recommended cable for interconnecting resolvers to equipment would be three separate screened twisted pair cables for the sine, cosine and reference signals. Further information should be obtained by consulting with the synchro and resolver suppliers.

Layout Considerations

The high voltage input signals, including reference, should be kept physically remote from the precision low voltage output signals.

Input signal track pairs, i.e., S3, S1 should be routed using parallel, physically adjacent PCB tracks that employ the same PCB layer. This minimizes external radiation that could corrupt low level precision analog signals. Distinct signal track pairs, i.e., R_{HI}–R_{LO} and S3–S1 should be routed physically separate. This minimizes mutual interference coupling whereby large amplitude signals can corrupt low level signals. This is angle dependent as shown in Figures 1 and 2, e.g., Cosine or Reference coupling to Sine at 0° (Figure 2).

A ground/power plane should not be sited underneath these high voltage input signal tracks as these signals can corrupt the noise integrity of the plane.

Errors due to ill defined ground loop currents should be avoided. The use of the AD2S75 enables the complete elimination of these errors using galvanic isolation within the internal transformers while retaining rigid adherence to analog star point sensing internal to the AD2S75 and between the AD2S75 and the RDC, as shown in the following connection diagrams. Note that the signal grounds have been connected to 0 V at the source of the signal.

CONNECTING THE AD2S75 TO A RESOLVER-TO-DIGITAL CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$, Pins 17 and 23, should be within the range of +5 V dc to +15 V dc and −5 V dc to −15 V dc, respectively, with respect to 0 V, (GND Pin 20), and must not be reversed.

It is recommended that a 100 nF (ceramic) decoupling capacitor should be connected between each of the supply pins and GND. The decoupling capacitors should be placed as near to the device as possible.

The metal package CASE, Pin 15, should be connected to 0 V, GND, Pin 20, to screen the internal circuits from any external noise and aid the operation of the magnetic circuits within the device.

The AD2S75 is a universal synchro/resolver interface for resolver-to-digital converters that accept 2 V rms input signals. The following converters from the Analog Devices range can be used directly with the AD2S75 and benefit from the transformer isolated interface:

2S80 series—monolithic, variable resolution RDC, all accuracy grades, including the 2S81 and 2S82. Please see Figure 3.

AD2S80A series—monolithic, variable resolution RDC all accuracy grades, including the AD2S81A and AD2S82A. For connections, please see Figure 3.

AD2S46TD10, AD2S46SD10—16-bit, high accuracy S/R/DC. Please use the 2 V input signals resolver option as shown above. For connections, please see Figure 4.

AD2S44UM10, AD2S44TM10, AD2S44SM10—14-bit, dual channel S/R/DC. Please use the 2 V input signals resolver option as shown above. For connections, please see Figure 5.

AD2S34TZ10, AD2S34SZ10, AD2S34TZ40, AD2S34SZ40, AD2S34TZ60, AD2S34SZ60—14-bit, dual channel RDC. For connections, please see Figure 6.

General

The Sine signal output from the AD2S75 is from SIN and SIN_{LO}, Pins 22 and 21, respectively.

The Cosine signal output from the AD2S75 is from COS and COS_{LO}, Pins 19 and 18, respectively.

The Reference signal output from the AD2S75 is from REF and GND, Pins 16 and 20 respectively.

The above signals should be connected to the appropriate input pins of the RDC.

The following should be noted:

Place the AD2S75 near to the RDC to minimize any external noise pickup.

Connect the signals from the AD2S75 to the RDC using equal lengths of pcb track so as to minimize differential phase shifts. The tracks should be routed in close proximity, parallel to each other on the same side of the pcb. Avoid the use of ground/power planes near the route of the ac signals so to avoid ac coupling and phase shifts caused by parasitic capacitance.

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Connecting the AD2S75 to 2S80/AD2S80A Series of RDCs
The following information also applies to 2S81, 2S82 and AD2S81A, AD2S82A.

The above resolver-to-digital converters (RDCs) have single ended amplifier inputs for the SIN and COS signals. It is recommended that SIN_{LO} and COS_{LO} are connected individually to a "star" point at SIGNAL GND, Pin 6 of the RDC. This eliminates any errors due to movement of the measurement reference point (SIGNAL GND).

The above is particularly important when the RDC is used at 14- to 16-bit resolution, medium to high accuracy applications.

For detailed information on the 2S80/AD2S80A series of RDC, please see the relevant data sheets.

Please see Figure 3.

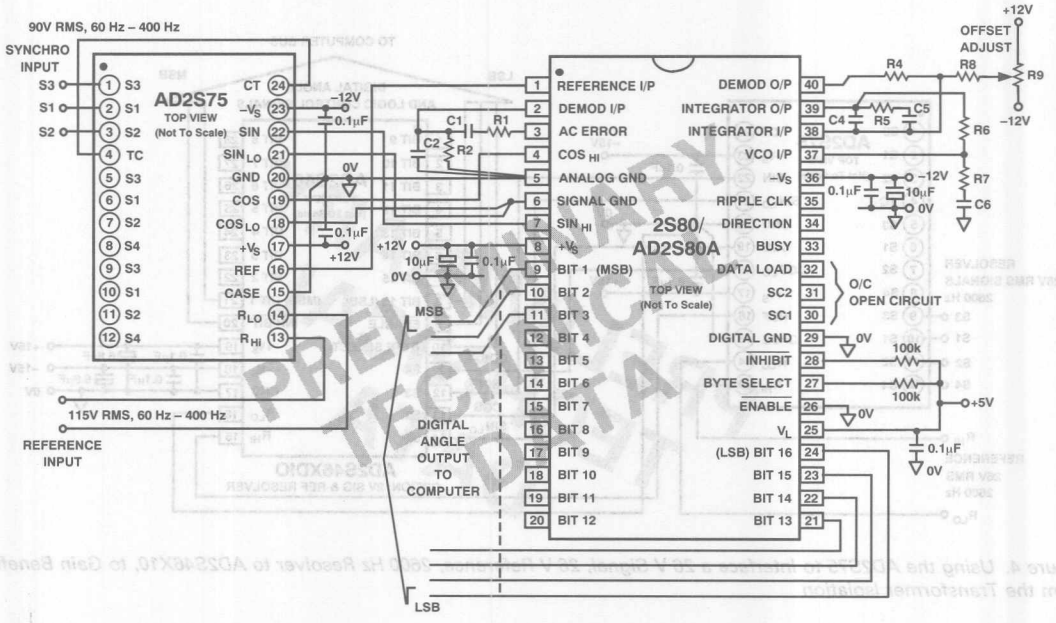


Figure 3. Using the AD2S75 to Interface a 90 V Signal, 115 V Reference, 60 Hz–400 Hz, Synchro to 2S80/AD2S80A Resolver-to-Digital Converter

PRELIMINARY TECHNICAL DATA

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Connecting the AD2S75 to the AD2S46

The AD2S46 series feature high accuracy differential inputs. It is recommended that the AD2S75 is connected to AD2S46XD10 as shown below in Figure 4.

Note that the SIN_{LO}, Pin 21, COS_{LO}, Pin 18, from AD2S75 are individually connected to S1 and S4, Pins 14 and 11, of AD2S46, respectively, in order to minimize any amplitude variation of the SIN and COS signals, thus maintaining the high accuracy of the AD2S46. (1.3 arc min over the operating temperature range −55°C to +125°C.)

The reference signals from the AD2S75 are also connected individually to AD2S46.

It is permissible to separate the RDC from the AS2S75 interface, as long as good wiring practice is employed by routing all cables together to avoid differential phase shifts.

As mentioned previously, the use of ground/power planes near the routing of the signals on the pcb is not recommended. For detailed information, please consult the AD2S46 data sheet.

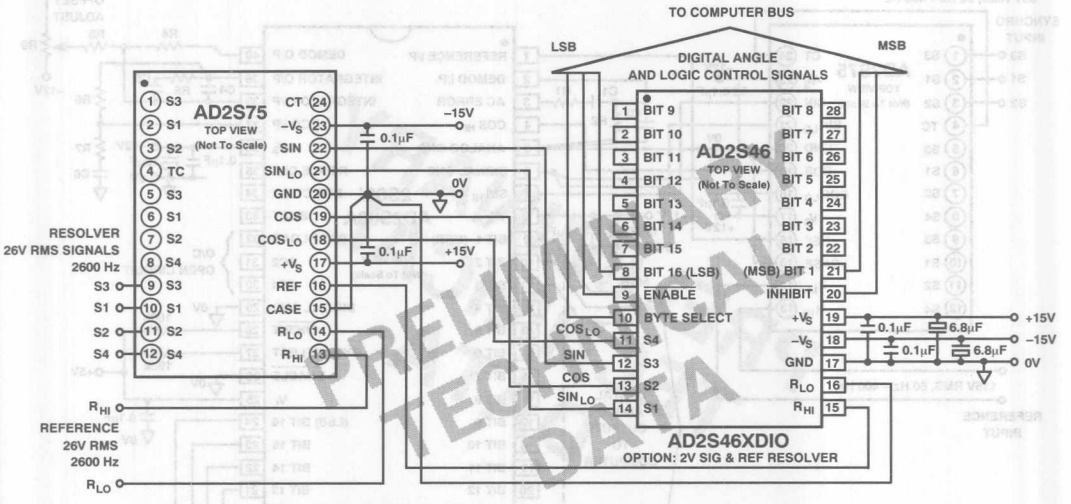


Figure 4. Using the AD2S75 to Interface a 26 V Signal, 26 V Reference, 2600 Hz Resolver to AD2S46X10, to Gain Benefit from the Transformer Isolation

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Connecting the AD2S75 to the AD2S44

The AD2S44 is a 14-bit, dual channel S/R/DC which features differential inputs and a separate individual reference input for each channel. This means that one single AD2S44XM10 (2 V resolver input option) can be used with the AD2S75 to interface to two completely different transducers in terms of signal configuration and reference frequency. The flexibility of the AD2S44 in combination with the AD2S75 is shown below in Figure 5. For detailed information, please consult the AD2S44 data sheet.

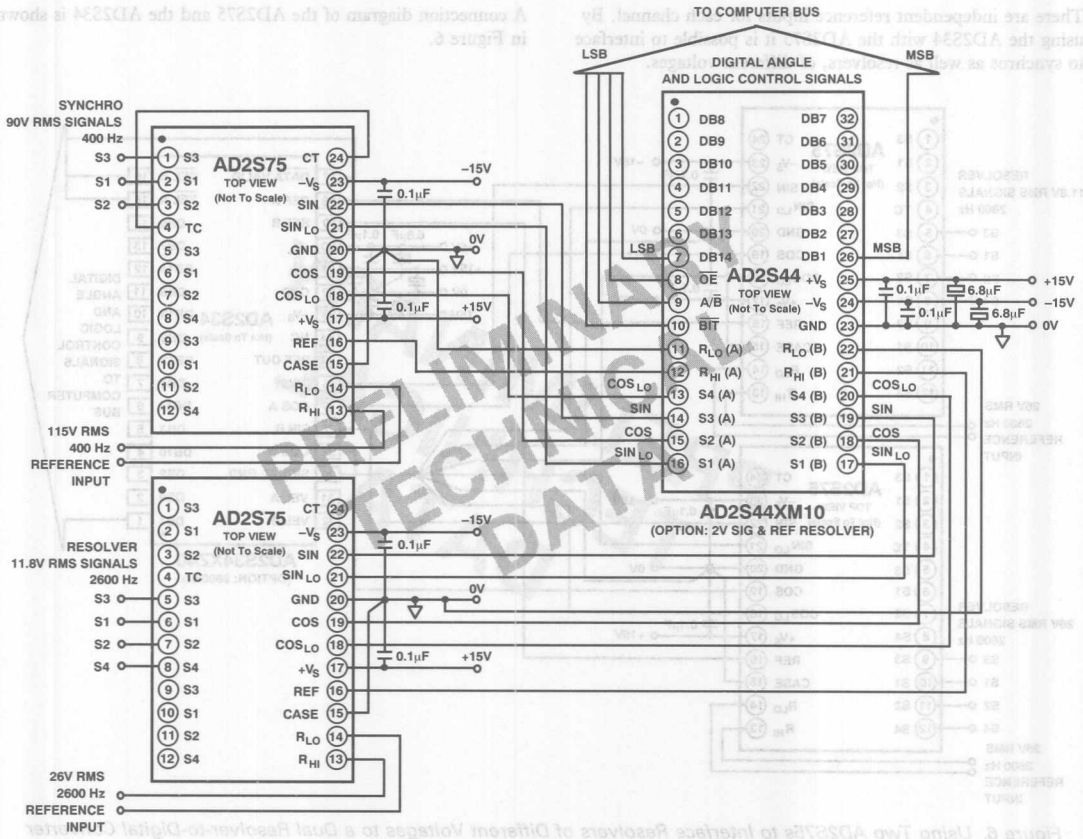


Figure 5. Using Two AD2S75s to Interface Synchro and Resolver Signals of Different Reference Frequencies to a Dual Resolver-to-Digital Converter AD2S44XM10

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Connecting the AD2S75 to the AD2S34

The AD2S34 is a 14-bit, dual channel, R/DC that accepts 2 V rms sine and cosine signals and reference input voltage. Some of the features of this converter are:

Small 1 inch^2 surface mount package.

On-board reference oscillator which can be used to provide excitation to a transducer(s).

There are independent reference inputs for each channel. By using the AD2S34 with the AD2S75 it is possible to interface to synchros as well as resolvers, of different voltages.

However, both transducers should be excited at similar frequencies up to 4400 Hz.

Due to limits imposed by the package size, the design of the dynamics of the AD2S34 are not as wideband as the design of the dynamics of the AD2S44.

For further detailed information, please see the AD2S34 data sheet.

A connection diagram of the AD2S75 and the AD2S34 is shown in Figure 6.

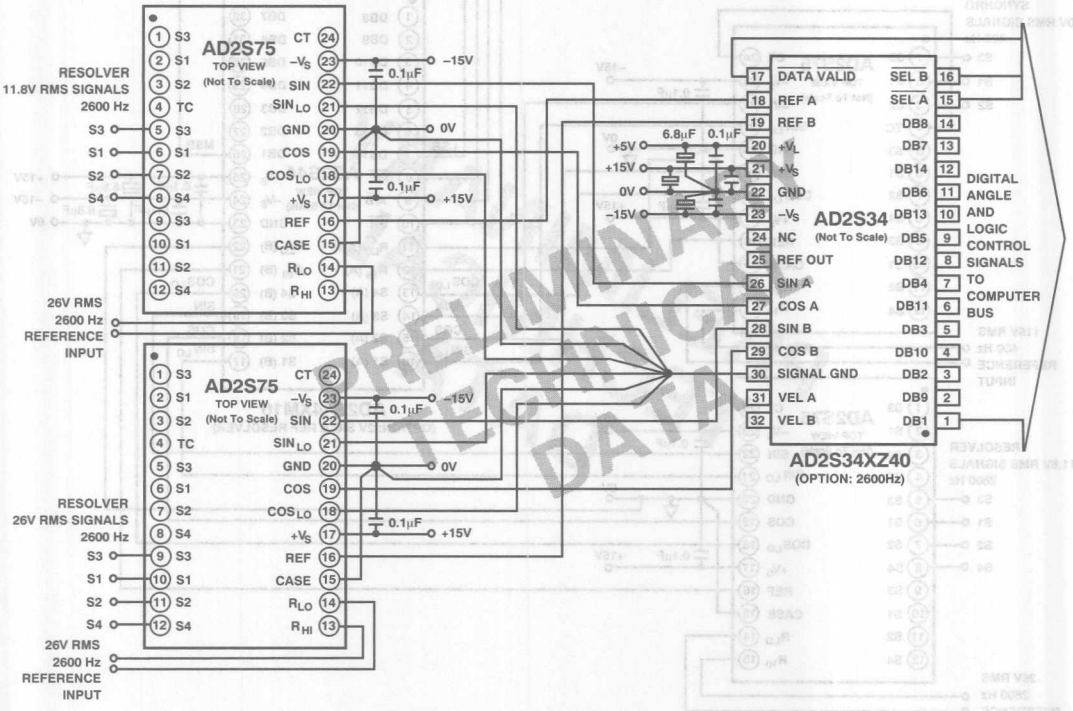


Figure 6. Using Two AD2S75s to Interface Resolvers of Different Voltages to a Dual Resolver-to-Digital Converter AD2S34XZ40

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

The AD2S75 signal and reference inputs can be scaled by using resistors to accommodate any voltage input (above 10.6 V rms).

Note: The accuracy of the interface and subsequently the accuracy of an R/DC, will be affected by the matching accuracies of the resistors used for the external scaling.

The current into any of the S1, S2, S3 and S4 inputs is very precisely controlled to 0.450 mA.

The total resistance in series with the signal inputs should be 2.222 kΩ per extra volt of signal. To calculate the values of the external scaling input resistors, add 1.111 kΩ per extra volt of input signal in series with S1, S2, S3 for a synchro, and S1, S2, S3, S4 for a resolver. For example to interface a 57.5 V rms line to line Magslip to the AD2S75 either:

(a) Into 26 V Inputs; use 35,000 Ω in series with each input; S1 Pin 10, S2 Pin 11 and S3 Pin 9. Leave S4 Pin 12 unconnected.

or

(b) Into 11.8 V Inputs; use 50,777.8 Ω in series with each input; S1 Pin 6, S2 Pin 7, S3 Pin 5. Leave S4 Pin 8 unconnected.

For example to interface a 48 V rms line-to-line resolver to the AD2S75 either:

(a) Into 26 V Inputs; use 24,444.4 Ω in series with S1 Pin 10, S2 Pin 11, S3 Pin 9 and S4 Pin 12.

or

(b) Into 11.8 V Inputs; use 40,222.2 Ω in series with S1 Pin 6, S2 Pin 7, S3 Pin 5 and S4 Pin 8.

The current into the reference input is controlled to 1.42 mA. For reference signals in excess of 115 V rms, please add 707 Ω per extra volt of input signal in series with R_{HI}, Pin 13, and R_{LO}, Pin 14.

External Resistor tolerance requirements are reduced by employing the highest standard internal voltage input available.

DYNAMIC PERFORMANCE

The closed-loop frequency response of the AD2S75 is shown

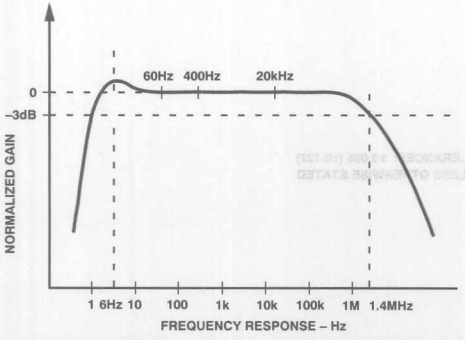


Figure 7. AD2S75 Closed-Loop Frequency Response

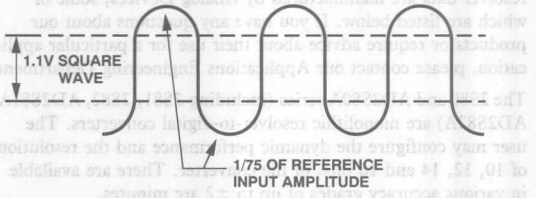


Figure 8. AD2S75 Reference Output Waveform

RELIABILITY

Figure 9 shows the MTBF in years versus case temperature for conditions, calculated in accordance with MIL-HDBK-217E.

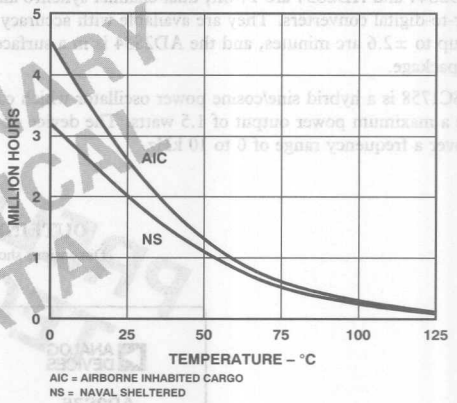


Figure 9. 2S75 vs. Temperature

PRELIMINARY TECHNICAL DATA

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OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The 2S80 and AD2S80A series (including 2S81, 2S82, AD2S81A, AD2S82A) are monolithic resolver-to-digital converters. The user may configure the dynamic performance and the resolution of 10, 12, 14 and 16 bits, of the converter. There are available in various accuracy grades of up to ±2 arc minutes.

The AD2S46 is a 16-bit resolution synchro or resolver-to-digital converter. Two accuracy grades are available with ±1.3 arc minutes and ±2.6 arc minutes, over the temperature range of −55°C to +125°C.

The AD2S44 and AD2S34 are 14-bit, dual channel synchro and resolver-to-digital converters. They are available with accuracy grades up to ±2.6 arc minutes, and the AD2S34 is in a surface mount package.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts. The device operates over a frequency range of 0 to 10 kHz.

The SDC/RDC1740/41/42 are hybrid synchro/resolver-to-digital converters with internal isolating microtransformers, with resolution of 14 and 12 bits, respectively. They are available in accuracy grades of ±5.3 arc minutes, ±8.5 arc minutes, ±15.3 arc minutes.

The SDC/RDC1768 is identical to the SDC/RDC1740 but with the additional features of analog velocity output and dc error output.

The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched input hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc minutes and the outputs can supply 2 VA at 7 V rms. Transformers are available to convert the output to synchro or resolver format at high voltage levels.

The AD2S65/AD2S66 are similar to the DRC1745/DRC1746 but do not include the power output stage. These devices are available with accuracy grades up to ±1 arc minute.

The AD2S75AM, industrial grade product operates over the temperature range of −40°C to +85°C.

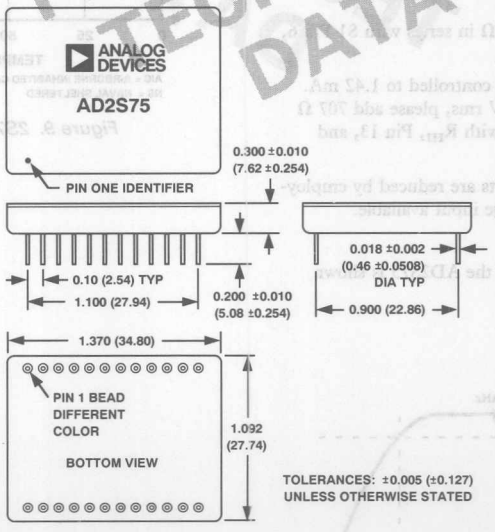
The AD2S75SMB receives additional environmental testing and processing and operates over the extended temperature range of −55°C to +125°C.

For further information, please contact Analog Devices.

PRELIMINARY TECHNICAL DATA

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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Variable Resolution, Monolithic Resolver-to-Digital Converter

AD2S80A

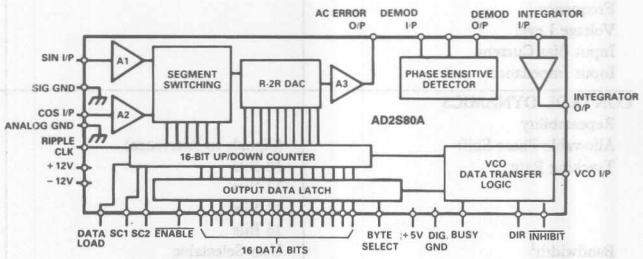
FEATURES

Monolithic (BiMOS II) Tracking R/D Converter
40-Pin DIP Package
44-Pin LCC Package
10-, 12-, 14- and 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
Velocity Output
Industrial Temperature Range Versions
Military Temperature Range Versions
ESD Class 2 Protection (2,000 V min)
/883 B Parts Available

APPLICATIONS

DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control
Military Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S80A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 40-pin DIP or 44-pin LCC ceramic package. It is manufactured on a BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip.

The converter allows users *to select their own resolution and dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S80A converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is in a three-state digital logic available in 2 bytes on the 16 output data lines. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

The AD2S80A operates over 50 Hz to 20,000 Hz reference frequency.

PRODUCT HIGHLIGHTS

Monolithic. A one chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S80A to be 10, 12, 14 or 16 bits allowing the user to use the AD2S80A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

Military Product. The AD2S80A is available processed in accordance with MIL-STD-883B, Class B.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Guide."

AD2S80A— SPECIFICATIONS (typical at +25°C unless otherwise specified)

Parameter	Conditions	AD2S80A Min	Typ	Max	Units
SIGNAL INPUTS					
Frequency		50		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
Maximum Voltage				8	V pk
REFERENCE INPUT					
Frequency		50		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
CONTROL DYNAMICS					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10	Degrees
Tracking Rate	10 Bits			1040	rps
	12 Bits			260	rps
	14 Bits			65	rps
	16 Bits			16.25	rps
Bandwidth[1]	User Selectable				
ACCURACY					
Angular Accuracy	A, J, S			**±8 +1 LSB**	arc min
	B, K, T			**±4 +1 LSB**	arc min
	L, U			**±2 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A, B, J, K, S, T			4	Codes
	L, U			1	Code
VELOCITY SIGNAL					
Linearity	Over Full Range		±1	±3	% FSD
Reversion Error			±1	±2	% FSD
DC Zero Offset[2]				6	mV
DC Zero Offset Tempco			−22		µV/°C
Gain Scaling Accuracy				±10	% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	V
Dynamic Ripple	Mean Value			1.5	% rms O/P
Output Load				1.0	kΩ
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				
Output Format	Bidirectional Natural Binary				
Load				3	LSTTL
$\overline{\text{INHIBIT}}$[3]					
Sense	Logic LO to Inhibit				
Time to Stable Data				600	ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs in High Impedance State				
$\overline{\text{ENABLE}}$ Time		35		110	ns
BYTE SELECT[3]					
Sense					
Logic HI	MS Byte DB1–DB8, LS Byte DB9–DB16				
Logic LO	LS Byte DB1–DB8, LS Byte DB9–DB16				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High (100 kΩ) to $+V_S$				
SC1 SC2					
0 *0*	10 Bit				
0 1	12 Bit				
1 0	14 Bit				
1 1	16 Bit				

Parameter	Conditions	AD2S80A Min	Typ	Max	Units
DATA LOAD					
Sense	Internally Pulled High (100 kΩ) to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[3]					
Sense	Logic HI When Position O/P Changing				
Width		200		600	ns
Load	Use Additional Pull-Up			1	LSTTL
DIRECTION[3]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[3]					
Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	300			
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS					
High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	2.0			V
Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			0.8	V
DIGITAL INPUTS					
High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100	μA
Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100	μA
DIGITAL INPUTS					
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			−400	μA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ μA	2.4			V
Low Voltage, V_{OL}	DB1– DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4	V
THREE STATE LEAKAGE	DB1–DB16 Only				
Current I_L	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			±100	μA
	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±100	μA

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

Parameter	Conditions	Min	Typ	Max	Units
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				12	mV
Gain					
In Phase	w.r.t. REF	−0.882	−0.9	−0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	150	nA
Input Impedance		1			MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57		63	dB
Dead Zone Current (Hysteresis)			100		nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	150	nA
Output Voltage Range	$\pm V_S = \pm 10.8$ V dc	±7			V
VCO					
Maximum Rate	$\pm V_S = \pm 12$ V dc	1.0	1.1		MHz
VCO Rate	Positive Direction	7.1	7.9	8.7	kHz/μA
	Negative Direction	7.1	7.9	8.7	kHz/μA
VCO Power Supply Sensitivity					
Increase	$+V_S$		+0.5		%/V
	$-V_S$		−8.0		%/V
Decrease	$+V_S$		−8.0		%/V
	$-V_S$		+2.0		%/V
Input Offset Voltage			1	5	mV
Input Bias Current			70	380	nA
Input Bias Current Tempco			−1.22		nA/°C
Input Voltage Range				±8	V
Linearity of Absolute Rate					
Full Range				<2	% FSD
Over 0% to 50% of Full Range				<1	% FSD
Reversion Error				1.5	% FSD
Sensitivity of Reversion Error to Symmetry of Power Supplies			±8		%/V of Assymetry
POWER SUPPLIES					
Voltage Levels					
$+V_S$		+10.8		+13.2	V
$-V_S$		−10.8		−13.2	V
$+V_L$		+5		+13.2	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	±23	mA
$\pm I_S$	$\pm Vs$ @ ±13.2 V		±19	±30	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	±1.5	mA

Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** and tested on all production units at final electrical test.

ESD SENSITIVITY

The AD2S80A features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

The AD2S80A is ESD protection Class II (2000 V min). Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual*.



RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$) . . . . . ±12 V dc ±10%
Power Supply Voltage V_L . . . . . +5 V dc ±10%
Analog Input Voltage (SIN and COS) . . . . . 2V rms ±10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . ±10 Degrees (max)
Ambient Operating Temperature Range
- Commercial (JD, KD, LD) . . . . . 0°C to +70°C
- Industrial (AD, BD) . . . . . −40°C to +85°C
- Extended (SD, SE, TD, TE, UD, UE) . . . −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2] . . . . . +14 V dc
$-V_S$ . . . . . −14 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +14 V to $-V_S$
SIN . . . . . +14 V to $-V_S$
COS . . . . . +14 V to $-V_S$
Any Logical Input . . . . . −0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +14 V to $-V_S$
Integrator Input . . . . . +14 V to $-V_S$
VCO Input . . . . . +14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
- Commercial (JD, KD, LD) . . . . . 0°C to +70°C
- Industrial (AD, BD) . . . . . −40°C to +85°C
- Extended (SD, SE, TD, TE, UD, UE) . . . −55°C to +125°C

θ_{JC}[3] (40-Pin DIP 883 Parts Only) . . . . . 11°C/W
θ_{JC}[3] (44-Pin LCC 883 Parts Only) . . . . . 10°C/W
Storage Temperature (All Grades) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

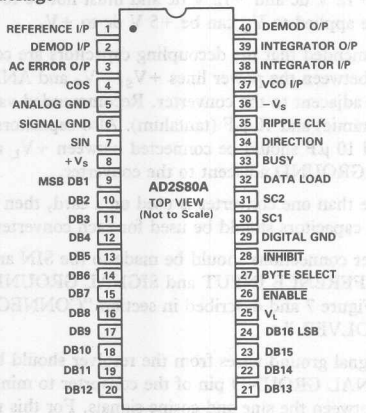
CAUTION:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. With reference to Appendix C of MIL-M-38510.

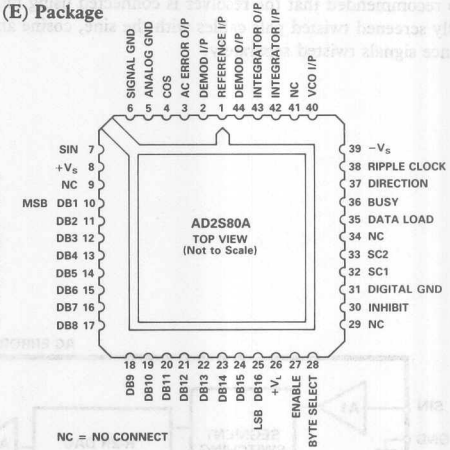
Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

Bit Weight Table

DIP (D) Package



LCC (E) Package



NC = NO CONNECT

PIN DESIGNATIONS

MNEMONIC	DESCRIPTION
REFERENCE I/P	REFERENCE SIGNAL INPUT
DEMOD I/P	DEMODULATOR INPUT
AC ERROR O/P	RATIO MULTIPLIER OUTPUT
COS	COSINE INPUT
ANALOG GROUND	POWER GROUND
SIGNAL GROUND	RESOLVER SIGNAL GROUND
SIN	SINE INPUT
$+V_S$	POSITIVE POWER SUPPLY
DB1–DB16	PARALLEL OUTPUT DATA
V_L	LOGIC POWER SUPPLY
$\overline{\text{ENABLE}}$	LOGIC HI-OUTPUT DATA IN HIGH IMPEDANCE STATE, LOGIC LO PRESENTS DATA TO THE OUTPUT LATCHES.
BYTE SELECT	LOGIC HI-MOST SIGNIFICANT BYTE TO DB1–DB8 LOGIC LO-LEAST SIGNIFICANT BYTE TO DB1–DB8.
$\overline{\text{INHIBIT}}$	LOGIC LO INHIBITS DATA TRANSFER TO OUTPUT LATCHES.
DIGITAL GROUND	DIGITAL GROUND
SC1–SC2	SELECT CONVERTER RESOLUTION
DATA LOAD	LOGIC LO DB1–D16 INPUTS LOGIC HI DB1–D16 OUTPUTS
BUSY	CONVERTER BUSY, DATA NOT VALID WHILE BUSY HI
DIRECTION	LOGIC STATE DEFINES DIRECTION OF INPUT SIGNAL ROTATION
RIPPLE CLOCK	POSITIVE PULSE WHEN CONVERTER OUTPUT CHANGES FROM 1S TO ALL 0S OR VICE VERSA
$-V_S$	NEGATIVE POWER SUPPLY
VCO I/P	VCO INPUT
INTEGRATOR I/P	INTEGRATOR INPUT
INTEGRATOR O/P	INTEGRATOR OUTPUT
DEMOD O/P	DEMODULATOR OUTPUT

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and −12 V dc and must not be reversed. The voltage applied to V_L can be +5 V dc to $+V_S$.

It is recommended that the decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 μF (tantalum). Also capacitors of 100 nF and 10 μF should be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER."

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figure 1.

CONVERTER RESOLUTION

Two major areas of the AD2S80A specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits; and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section COMPONENT SELECTION). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do it when the BUSY is low, i.e., when Data is not changing.

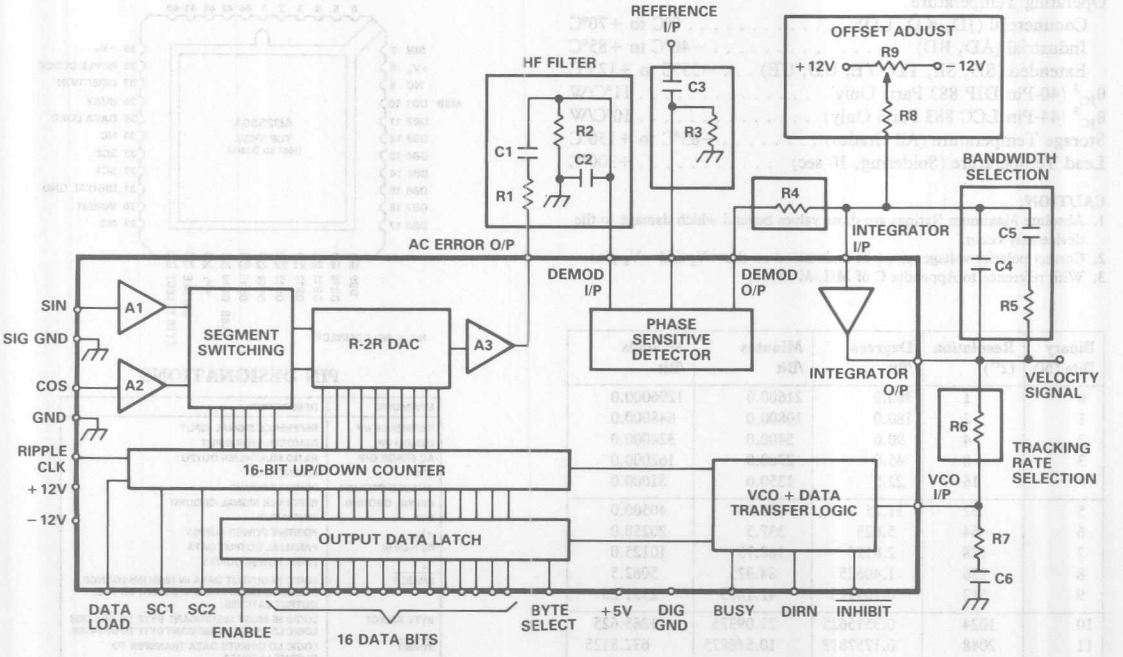


Figure 1. AD2S80A Connection Diagram

CONVERTER OPERATION

When connected in a circuit such as shown in Figure 1 the AD2S80A operates as a tracking resolver to digital converter and forms a Type 2 closed-loop system. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S80A is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING

The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S80A will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S80A will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak.) Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word. As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changing state (1 LSB min change) with a corresponding change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$. The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR INPUT (which can be trimmed out – see Figure 1), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S80A can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

In many applications it is possible to use the velocity signal of the AD2S80A to replace a conventional tachogenerator.

DC ERROR SIGNAL

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. This is the dc error of the converter; and as the converter is a Type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in-test."

COMPONENT SELECTION

The following instructions describe how to select the external components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used, and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

PC compatible software is available to help users select the optimum component values for the AD2S80A, and display the transfer gain, phase and small step response.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S80A, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.

   Values should be chosen so that

   $$15\ k\Omega \leq R1 = R2 \leq 56\ k\Omega$$

   $$C1 = C2 = \frac{1}{2\,\pi\,R1\,f_{REF}}$$

   and f_{REF} = Reference frequency (Hz)

   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\ \Omega$$

   where 100×10^{-9} = current/LSB
   If R1, C2 are not fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\ \Omega$$

   where $E_{DC} = 160 \times 10^{-3}$ for 10 bits resolution
   $= 40 \times 10^{-3}$ for 12 bits
   $= 10 \times 10^{-3}$ for 14 bits
   $= 2.5 \times 10^{-3}$ for 16 bits
   = Scaling of the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

   $$R3 = 100\ k\Omega$$

   $$C3 > \frac{1}{R3 \times f_{REF}}\ F$$

   with R3 in Ω.

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate, the velocity output will be 8 V.

   Decide on your maximum tracking rate, "T," in revolutions per second. Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.

   $$R6 = \frac{6.32 \times 10^{10}}{T \times n}\ \Omega$$

   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does not exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100Hz for a 400Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.

   b. Select C4 so that

   $$C4 = \frac{21}{R6 \times f_{BW}^2}\ F$$

   with R6 in Ω and f_{BW} in Hz selected above.

   c. C5 is given by

   $$C5 = 5 \times C4$$

   d. R5 is given by

   $$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

   $C6 = 470\ pF,\ R7 = 68\ \Omega$

7. Offset Adjust
   Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

   If fitted, the following values of R8 and R9 should be used:

   $R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega$ *potentiometer*

   To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

   The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL level. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input selects the byte of the position data to be presented at the data output DB1 to DB8. The least significant byte will be presented on data output DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S80A is used with a resolution less than 16 bits the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output DB1 and DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK

As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulse width of the ripple clock is 300 ns. RIPPLE CLOCK is normally set high before a BUSY pulse and resets before the next positive going edge of the next consecutive pulse.

The only exception to this is when DIR changes whilst the RIPPLE CLOCK is high. Resetting of the RIPPLE clock will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

If the AD2S80A is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2).

RIPPLE CLOCK is unaffected by $\overline{\text{INHIBIT}}$.

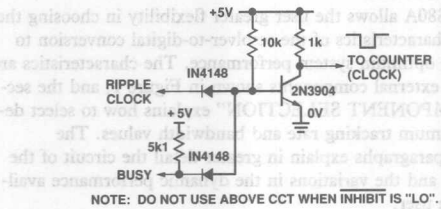
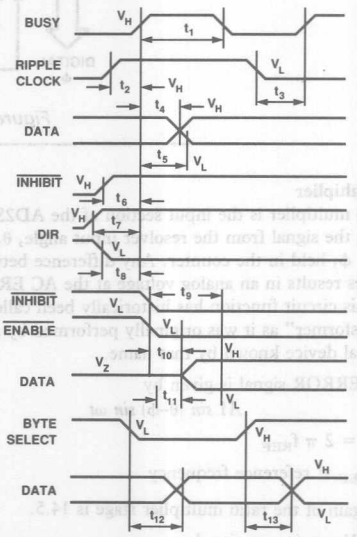


Figure 2. Diode Transistor Logic Nand Gate

DIRECTION Output

The DIRECTION (DIR) logic output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA and RIPPLE CLOCK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This corresponds to a change in input rotation direction but less than 1 LSB.

DIGITAL TIMING



PARAMETER	T_{MIN}	T_{MAX}	CONDITION
t_1	200	600	BUSY WIDTH V_H– V_H
t_2	10	25	RIPPLE CLOCK V_H TO BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L TO NEXT BUSY V_H
t_4	16	45	BUSY V_H TO DATA V_H
t_5	3	25	BUSY V_H TO DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H TO BUSY V_H
t_7	485	625	MIN DIR V_H TO BUSY V_H
t_8	515	670	MIN DIR V_H TO BUSY V_H
t_9	–	600	$\overline{\text{INHIBIT}}$ V_L TO DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_L
t_{12}	60	140	BYTE SELECT V_L TO DATA STABLE
t_{13}	60	125	BYTE SELECT V_H TO DATA STABLE

The AD2S80A allows the user greater flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the AD2S80A and the variations in the dynamic performance available to the user.

Loop Compensation

The AD2S80A (connected as shown in Figure 1) operates as a Type 2 tracking servo loop where the VCO/counter combination and Integrator perform the two integration functions inherent in a Type 2 loop.

acteristic crossing the 0 dB axis with 180° of additional phase lag, as shown in Figure 5.

This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The AD2S80A does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer (see Application Note).

A block diagram of the AD2S80A is given in Figure 3.

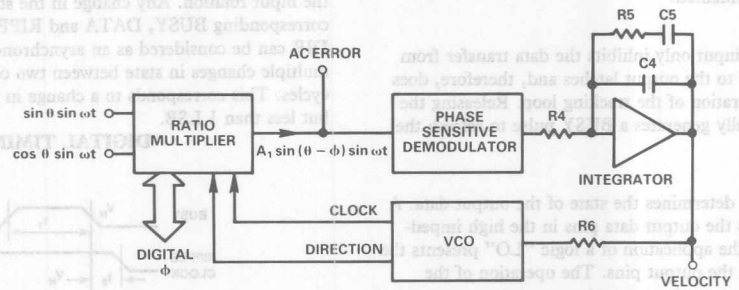


Figure 3. AD2S80A Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the AD2S80A and compares the signal from the resolver input angle, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a electromechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta-\phi) \sin \omega t$$

where $\omega = 2 \pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5.

So for 2 V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{n}\right) \times A1$$

where n = bits per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

giving an AC ERROR output
= 178 mV/bit @ 10 bits resolution
= 44.5 mV/bit @ 12 bits
= 11.125 mV/bit @ 14 bits
= 2.78 mV/bit @ 16 bits

The ratio multiplier will work in exactly the same way whether the AD2S80A is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the AD2S80A is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (DEMODULATOR\ INPUT\ rms\ voltage)$$

(for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160 mV/bit (10 bits resolution)
= 40 mV/bit (12 bits resolution)
= 10 mV/bit (14 bits resolution)
= 2.5 mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the AD2S80A to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 LSB. In order to ensure that this feedback "hysteresis" is set to 1 LSB the input current to the integrator must be scaled to be 100 nA/bit. Therefore,

$$R4 = \frac{DC\ Error\ Scaling\ (mV/bit)}{100\ (nA/bit)}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100 nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocking either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated, the reset period is constant at 400 ns.

The VCO rate is fixed for a given input current by the VCO scaling factor:

$$= 7.9\ kHz/\mu A$$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT

100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$$(100 \times 4096)/(7900) = 51.8\ \mu A$$

Thus, R6 would be set to: $5/(51.8 \times 10^{-6}) = 96\ k\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

$$Velocity\ Offset\ Voltage = R6 \times (VCO\ bias\ current)$$

The temperature coefficient of this offset is given by

$$Velocity\ Offset\ Tempco = R6 \times (VCO\ bias\ current\ tempco)$$

where the VCO bias current tempco is typically −1.22 nA/°C.

The maximum recommended rate for the VCO is 1.1 MHz which sets the maximum possible tracking rate.

Since the minimum voltage swing available at the integrator output is ±8 V, this implies that the minimum value for R6 is 57 kΩ. As

$$Max\ Current = \frac{1.1 \times 10^6}{7.9 \times 10^3} = 139\ \mu A$$

$$Min\ Value\ R6\ \frac{8}{139 \times 10^{-6}} = 57\ k\Omega$$

Transfer Function

By selecting components using the method outlined in the section "Component Selection," the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\ (1 + s_N)}{(s_N + 2.4)\ (s_N^2 + 3.4\ s_N + 5.8)}$$

where, s_N, the normalized frequency variable is:

$$s_N = \frac{2}{\pi}\ \frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3 dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2\ sec^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

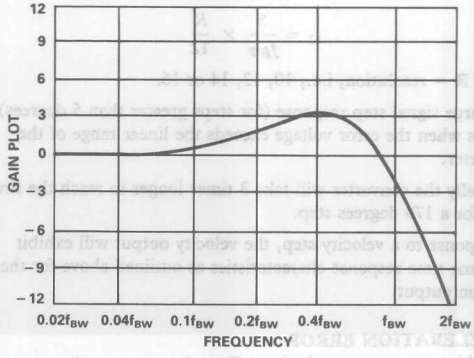


Figure 4. AD2S80A Gain Plot

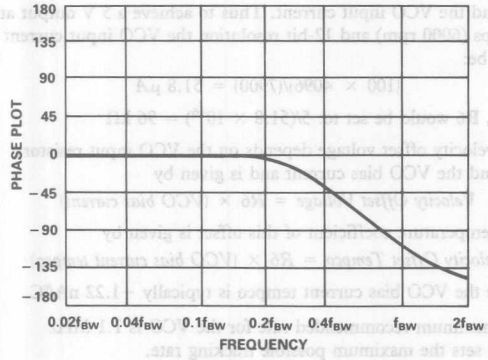


Figure 5. AD2S80A Phase Plot

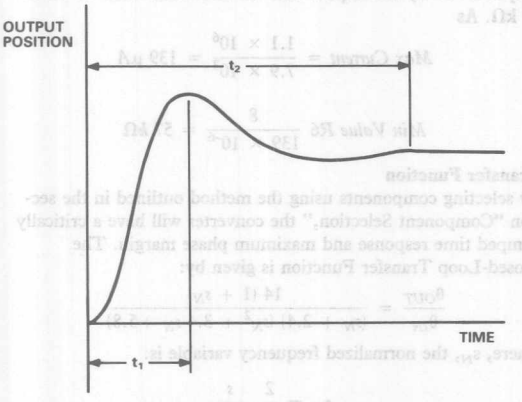


Figure 6. AD2S80A Small Step Response

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter is settled to 1 LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

The large signal step response (for steps greater than 5 degrees) applies when the error voltage exceeds the linear range of the converter.

Typically the converter will take 3 times longer to reach the first peak for a 179 degrees step.

In response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{\textit{Input Acceleration}}{\textit{Error in Output Angle}}$$

The numerator and denominator must have consistent angular units. For example if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error output in degrees. Angular measurement may also be specified using radians, minutes of arc, LSBs, etc.

K_A does not define maximum input acceleration, only the error due to it's acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$\textit{Angular Accuracy} \times K_A = \textit{Degrees/sec}^2$$

K_A can be used to predict the output position error for a given input acceleration. For example for an acceleration of 100 revs/sec^2, $K_A = 2.7 \times 10^6$ sec^{-2} and 12-bit resolution.

$$\textit{Error in LSBs} = \frac{\textit{Input acceleration [LSB/sec}^2\textit{]}}{K_A\,[sec^{-2}]}$$

$$= \frac{100\ [rev/sec^2] \times 2^{12}}{2.7 \times 10^6} = 0.15\ \textit{LSBs or } 47.5\ \textit{seconds of arc}$$

To determine the value of K_A based on the passive components used to define the dynamics of the converter the following should be used.

$$K_A = \frac{4.04 \times 10^{11}}{2^n \cdot R6 \cdot R4 \cdot (C4 + C5)}$$

Where n = resolution of the converter.
R4, R6 in ohms
C5, C4 in farads

SOURCES OF ERRORS

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will typically be 1 arc minute over the operating temperature range.

A description of how to adjust from zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$\textit{Error} = 0.53\ a \times b\ \textit{arc minutes}$$

where a = differential phase shift (degrees).
b = signal to reference phase shift (degrees).

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see

section "CONNECTING THE RESOLVER"). By taking these precautions the extra error can be made insignificant.

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\textit{Shaft Speed (rps)} \times \textit{Phase Shift (Degrees)}}{\textit{Reference Frequency}}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5 kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \textit{ Degrees}$$

This effect can be eliminated by placing a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY ERRORS

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in the place of a velocity transducer. Although the conversion loop of the AD2S80A includes a digital section there is an additional analog feedback loop around the velocity signal. This ensures against flicker in the digital positional output in both dynamic and static states.

A better quality velocity signal will be achieved if the following points are considered:

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion error.[1]
   The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).
   A resolver is chosen that has low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the AD2S80A with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   Maintenance of the input signal voltages at 2 V rms will prevent LSB flicker at the positional output. The analog feedback or hysteresis employed around the VCO and the intergrator is a function of the input signal levels (see section "INTEGRATOR").

Following the preceding precautions will allow the user to use the velocity signal in very noisy environments, for example, PWM motor drive applications. Resolver/converter error curves may exhibit apparent acceleration/deceleration at a constant velocity. This results in ripple on the velocity signal of frequency twice the input rotation.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 7.

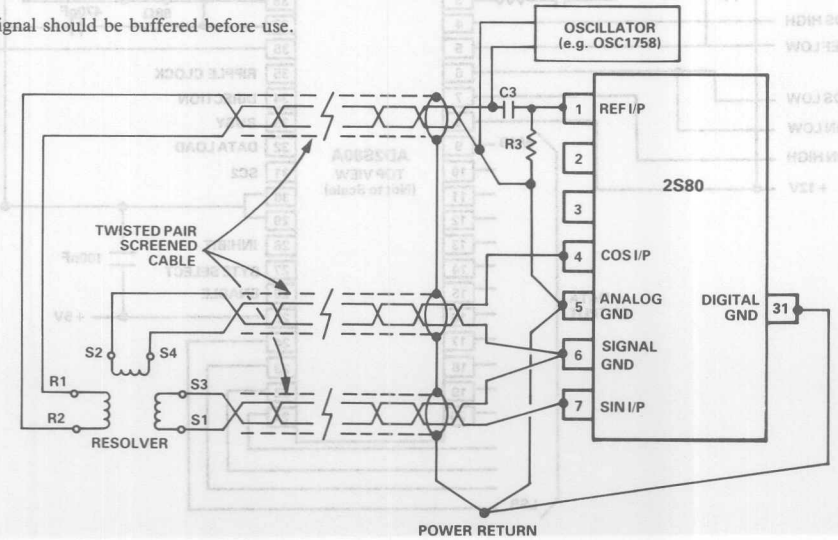


Figure 7. Connecting the AD2S80A to a Resolver

[1]Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO.

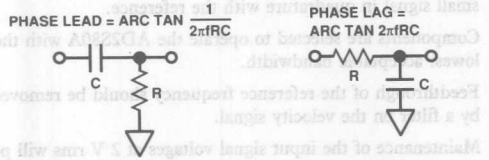
from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency = $\frac{1}{2\pi RC}$

by altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.



Phase Shift Circuits

TYPICAL CIRCUIT CONFIGURATION

Figure 8 shows a typical circuit configuration for the AD2S80A in a 12-bit resolution mode. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 2.7×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

For more information on resistive scaling of SIN, COS and REFERENCE converter inputs refer to the application note, "Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters."

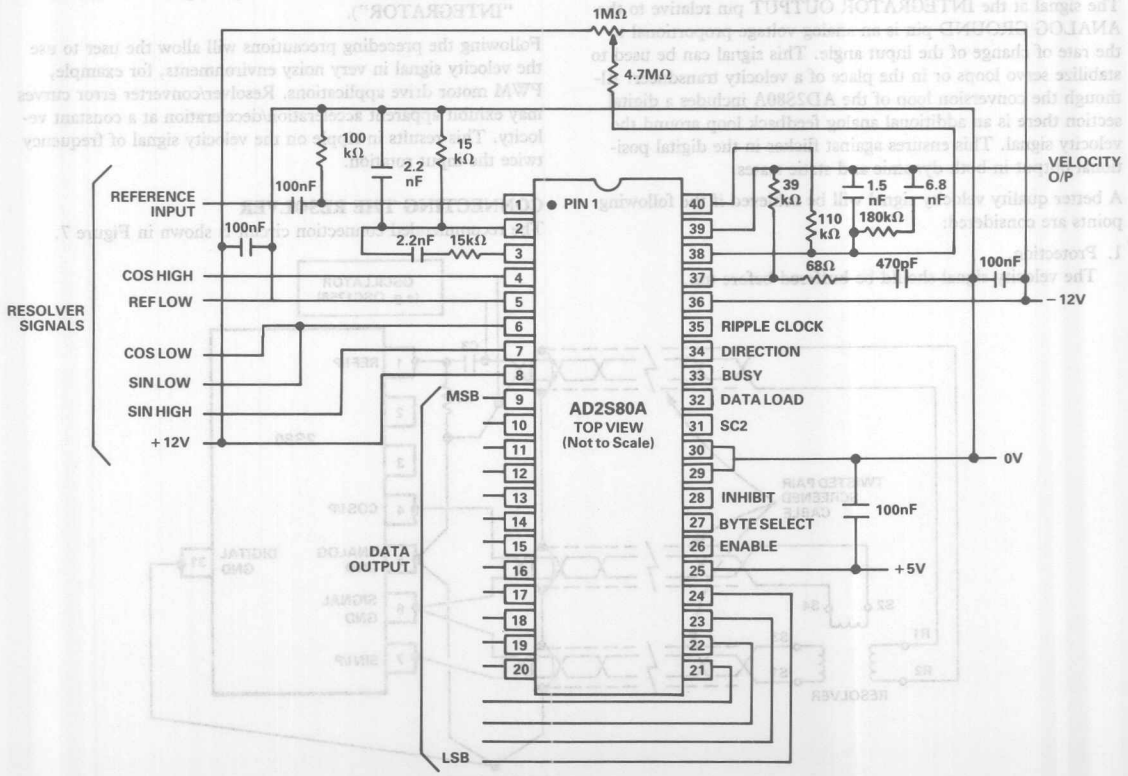


Figure 8. Typical Circuit Configuration

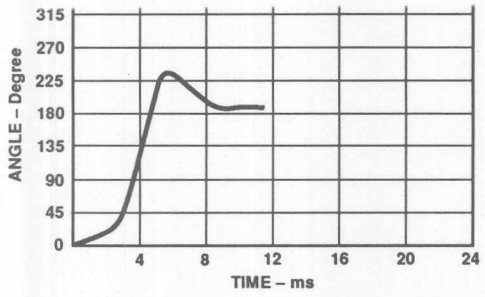


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 8

RELIABILITY

The AD2S80A Mean Time Between Failures (MTBF) has been calculated according to MIL-HDBK-217E, Figure 10 shows the MTBF in hours in naval sheltered conditions for AD2S80A/883B only.

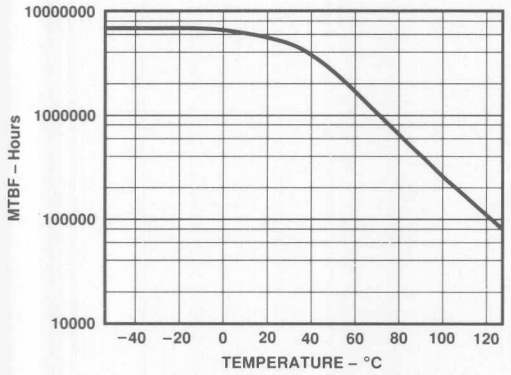


Figure 10. AD2S80A MTBF Curve

Control Transformer

The ratio multiplier of the AD2S80A can be used independently of the loop integrators as a control transformer. In this mode the resolver inputs θ are multiplied by a digital angle ϕ, any difference between ϕ and θ will be represented by the AC ERROR output as SIN ωt sin (θ–ϕ) or the DEMOD output as sin (θ–ϕ). To use the AD2S80A in this mode refer to the "Control Transformer" application note.

Dynamic Switching

In applications where the user requires wide band response from the converter, for example 100 rpm to 6000 rpm, superior performance is achieved if the converters control characteristics are switched dynamically. This reduces velocity offset levels at low tracking rates. For more information on the technique refer to "Dynamic Resolution Switching Using the Variable Resolution Monolithic Resolver-to-Digital Converters."

3

OTHER PRODUCTS

The AD2S82A is a monolithic, variable resolution 10-, 12-, 14- and 16-bit resolver to digital converter in a 44-pin J-leaded PLCC package. In addition to the AD2S80A functions it has a VCO OUTPUT which is a measure of position within a LSB, and a COMPLEMENT Data Output.

The AD2S81A is a low cost, monolithic, 12-bit resolver-to-digital converter in a 28-pin ceramic DIP package.

ORDERING GUIDE

Model	Operating Temperature Range	Accuracy	Package Option*
AD2S80AJD	0°C to +70°C	8 arc min	D-40
AD2S80AKD	0°C to +70°C	4 arc min	D-40
AD2S80ALD	0°C to +70°C	2 arc min	D-40
AD2S80AAD	−40°C to +85°C	8 arc min	D-40
AD2S80ABD	−40°C to +85°C	4 arc min	D-40
AD2S80ASD	−55°C to +125°C	8 arc min	D-40
AD2S80ATD	−55°C to +125°C	4 arc min	D-40
AD2S80AUD	−55°C to +125°C	2 arc min	D-40
AD2S80ASE	−55°C to +125°C	8 arc min	E-44A
AD2S80ATE	−55°C to +125°C	4 arc min	E-44A
AD2S80AUE	−55°C to +125°C	2 arc min	E-44A
AD2S80ASD/883B	−55°C to +125°C	8 arc min	D-40
AD2S80ATD/883B	−55°C to +125°C	4 arc min	D-40
AD2S80ASE/883B	−55°C to +125°C	8 arc min	E-44A
AD2S80ATE/883B	−55°C to +125°C	4 arc min	E-44A

*D = Ceramic DIP Package; E = Leadless Ceramic Chip Carrier Package. For outline information see Package Information section.

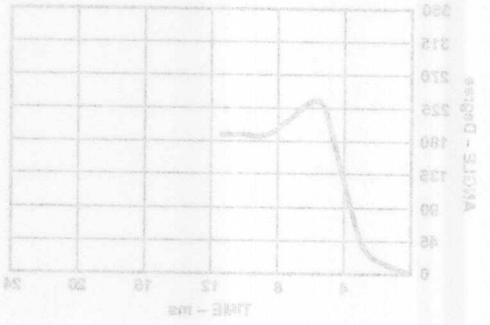


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 9

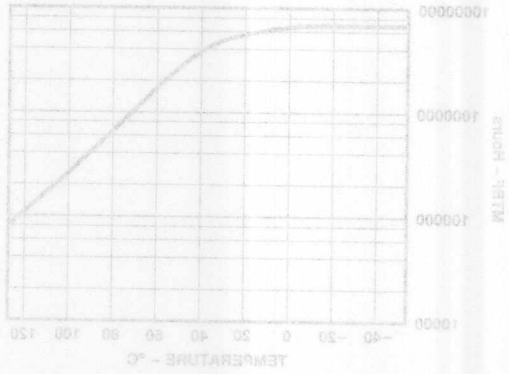


Figure 10. AD2S80A MTBF Curve

Variable Resolution, Monolithic Resolver-to-Digital Converters

AD2S81A/AD2S82A

FEATURES

Monolithic (BiMOS II) Tracking R/D Converter
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
Velocity Output
ESD Class 2 Protection (2,000 V min)

AD2S81A
28-Pin DIP Package
Low Cost

AD2S82A
44-Pin PLCC Package
10-, 12-, 14- and 16-Bit Resolution Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
VCO Output (Inter LSB Output)
Data Complement Facility

APPLICATIONS

DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

GENERAL DESCRIPTION

The AD2S82A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin J leaded PLCC package. Two extra functions are provided in the new surface mount package – COMPLEMENT and VCO output.

The AD2S81A is a monolithic 12-bit fixed resolution tracking resolver-to-digital converter packaged in a 28-pin DIP.

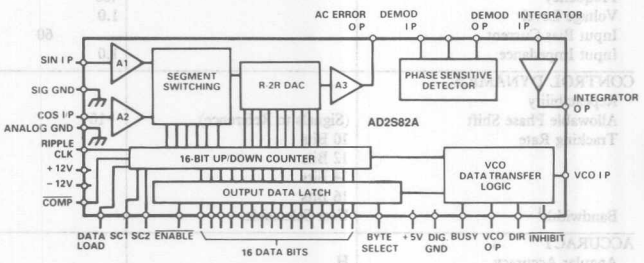
The converters allow users to *select their own dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The AD2S82A allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S81A and AD2S82A convert resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The output word is in a three-state digital logic form available in 2 bytes on the 16 output data lines for the AD2S82A and on 8 output data lines for the AD2S81A. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

AD2S82A FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

Monolithic. A one-chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S82A to be 10, 12, 14 or 16 bits allowing the user to use the AD2S82A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

SIGNAL INPUTS							
Frequency		400		20,000	50	20,000	Hz
Voltage Level		1.8	2.0	2.2	*		V rms
Input Bias Current			60	150	*		nA
Input Impedance		1.0			*		MΩ
Maximum Voltage				±8	*		V pk
REFERENCE INPUT							
Frequency		400		20,000	50	20,000	Hz
Voltage Level		1.0		8.0	*		V pk
Input Bias Current			60	150	*		nA
Input Impedance		1.0			*		MΩ
CONTROL DYNAMICS							
Repeatability				1		1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10	*		Degrees
Tracking Rate	10 Bits					1040	rps
	12 Bits			260		260	rps
	14 Bits					65	rps
	16 Bits					16.25	rps
Bandwidth[1]	User Selectable						
ACCURACY							
Angular Accuracy	H					**±22 + 1 LSB**	arc min
	J			**±30 +1 LSB**		**±8 + 1 LSB**	arc min
	K					**±4 + 1 LSB**	arc min
	L					**±2 + 1 LSB**	arc min
Monotonicity	Guaranteed Monotonic						
Missing Codes (16-Bit Resolution)	J, K					4	Codes
	L					1	Code
VELOCITY SIGNAL							
Linearity	Over Full Range		±1	±3	*		% FSD
Reversion Error				±2	*		% FSD
DC Zero Offset[2]				6	*		mV
DC Zero Offset Tempco			−22		*		µV/°C
Gain Scaling Accuracy				±10	*		% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	*		V
Dynamic Ripple	Mean Value			1.5	*		% rms O/P
Output Load				1.0	*		kΩ
INPUT/OUTPUT PROTECTION							
Analog Inputs	Overvoltage Protection		±8		*		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	*		mA
DIGITAL POSITION							
Resolution	10, 12, 14, and 16						
Output Format	Bidirectional Natural Binary						
Load				3	*		LSTTL
$\overline{\text{INHIBIT}}$[3]							
Sense	Logic LO to Inhibit						
Time to Stable Data				600	*		ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs in High Impedance State						
$\overline{\text{ENABLE}}$/Disable Time		35		110	*		ns
BYTE SELECT[3]							
Sense							
Logic HI	MS Byte DB1–DB8, (LS Byte DB9–DB16)[4]						
Logic LO	LS Byte DB1–DB8, (LS Byte DB9–DB16)[4]						
Time to Data Available		60		140	*		ns
SHORT CYCLE INPUTS[4]	Internally Pulled High (100 kΩ) to $+V_S$						
SC1 SC2							
0 0	10 Bit						
0 1	12 Bit						
1 0	14 Bit						
1 1	16 Bit						
DATA LOAD[4]							
Sense	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO Allows Data to Be Loaded into the Counters from the Data Lines				150	300	ns

Parameter	Conditions	AD28S1A Min	AD28S1A Typ	AD28S1A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
COMPLEMENT[4]	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO to Activate; No Connect for Normal Operation							
BUSY[3]								
Sense	Logic HI When Position O/P Changing							
Width		200		600		*		ns
Load	Use Additional Pull-Up			1		*		LSTTL
DIRECTION[3]								
Sense	Logic HI Counting Up Logic LO Counting Down							
Max Load				3		*		LSTTL
RIPPLE CLOCK[3]								
Sense	Logic HI All 1s to all 0s All 0s to All 1s							
Width	Dependent On Input Velocity	300				*		
Reset	Before Next Busy							
Load				3		*		LSTTL
DIGITAL INPUTS								
High Voltage, V_{IH}	$\overline{INHIBIT}$, $\overline{ENABLE}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	2.0				*		V
Low Voltage, V_{IL}	$\overline{INHIBIT}$, $\overline{ENABLE}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			0.8		*		V
DIGITAL INPUTS								
High Current, I_{IH}	$\overline{INHIBIT}$, $\overline{ENABLE}$ DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100		*		μA
Low Current, I_{IL}	$\overline{INHIBIT}$, $\overline{ENABLE}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100		*		μA
DIGITAL INPUTS								
Low Voltage, V_{IL}	$\overline{ENABLE}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0		*		V
Low Current, I_{IL}	$\overline{ENABLE}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			−400		*		μA
DIGITAL OUTPUTS								
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ μA	2.4				*		V
Low Voltage, V_{OL}	DB1– DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4		*		V
THREE-STATE LEAKAGE Current I_L	DB1–DB16 Only $+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			±100		*		μA
	$+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±100		*		μA

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.
[4]AD2S82A only.

*Specifications same as AD2S81A.
Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

AD2S81A/AD2S82A—SPECIFICATIONS (typical at +25°C unless otherwise specified)

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
RATIO MULTIPLIER								
AC Error Output Scaling	10 Bit					177.6		mV/Bit
	12 Bit		**			44.4		mV/Bit
	14 Bit					11.1		mV/Bit
	16 Bit					2.775		mV/Bit
PHASE SENSITIVE DETECTOR								
Output Offset Voltage				12		*		mV
Gain								
In Phase	w.r.t. REF	−0.882	−0.9	−0.918		*		V rms/V dc
In Quadrature	w.r.t. REF			0.04		*		V rms/V dc
Input Bias Current			60	150		*		nA
Input Impedance		1				*		MΩ
Input Voltage				±8		*		V
INTEGRATOR								
Open-Loop Gain	At 10 kHz	57		63		*		dB
Dead Zone Current (Hysteresis)			100			*		nA/LSB
Input Offset Voltage			1	5		*		mV
Input Bias Current			60	150		*		nA
Output Voltage Range	$\pm V_S$ = ±10.8 V dc,	±7						V
VCO	$\pm V_S$ = ±12 V dc							
Maximum Rate		1.0	1.1			*		MHz
VCO Rate	Positive DIR	7.1	7.9	8.7		*		kHz/μA
	Negative DIR	7.1	7.9	8.7		*		kHz/μA
VCO Power Supply Sensitivity								
Increase	$+V_S$		+0.5			*		%/V
	$-V_S$		−8.0			*		%/V
Decrease	$+V_S$		−8.0			*		%/V
	$-V_S$		+2.0			*		%/V
Input Offset Voltage			1	5		*		mV
Input Bias Current			70	380		*		nA
Input Bias Current Tempco			−1.22			*		nA/°C
Input Voltage Range				±8		*		V
Linearity of Absolute Rate								
Full Range				<2		*		% FSD
Over 0% to 50% of Full Range				<1		*		% FSD
Reversion Error				1.5		*		% FSD
Sensitivity of Reversion Error to Symmetry of Power Supplies			±8			*		%/V of Asymmetry
VCO Output[1, 2]					±2.7	±3.0	±3.3	V/LSB
POWER SUPPLIES								
Voltage Levels								
$+V_S$		+10.8		+13.2		*		V
$-V_S$		−10.8		−13.2		*		V
$+V_L$		+5		+13.2		*		V
Current								
$+I_S$	$\pm V_S$ @ ±12 V		±12	±23		*		mA
$+I_S$	$\pm V_S$ @ ±13.2 V		±19	±30		*		mA
$+I_L$	$\pm V_L$ @ ±5.0 V		±0.5	±1.5		*		mA

NOTE
[1]The VCO output swings between ±3 V depending on the resolver direction.
[2]AD2882A only.

*Specifications same asAD2S81A.
**Specifications same as AD2S82A.

Specifications subject to change without notice.

ESD SENSITIVITY

The AD2S81A and AD2S82A feature input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

The AD2S81A and AD2S82A are ESD protection Class II (2000 V min). Proper ESD precautions *are strongly recommended to avoid* functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*



RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to $-V_S$) . . . . . ±12 V dc ±10%
Power Supply Voltage V_L . . . . . +5 V dc ±10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . ±10 Degrees (max)
Ambient Operating Temperature
Commercial (JD, HP, JP, KP, LP) . . . . . 0 to +70°C

PIN DESIGNATIONS

MNEMONIC	DESCRIPTION
REFERENCE I/P	REFERENCE SIGNAL INPUT
DEMOD I/P	DEMODULATOR INPUT
AC ERROR O/P	RATIO MULTIPLIER OUTPUT
COS I/P	COSINE INPUT
ANALOG GROUND	POWER GROUND
SIGNAL GROUND	RESOLVER SIGNAL GROUND
SIN I/P	SINE INPUT
$+V_S$	POSITIVE POWER SUPPLY
DB1–DB16	PARALLEL OUTPUT DATA
V_L	LOGIC POWER SUPPLY
$\overline{\text{ENABLE}}$	LOGIC HI–OUTPUT DATA IN HIGH IMPEDANCE STATE, LOGIC, LO PRESENTS DATA TO THE OUTPUT LATCHES.
BYTE SELECT	LOGIC HI–MOST SIGNIFICANT BYTE TO DB1–DB8 LOGIC LO–LEAST SIGNIFICANT BYTE TO DB1–DB8.
$\overline{\text{INHIBIT}}$	LOGIC LO INHIBITS DATA TRANSFER TO OUTPUT LATCHES.
DIGITAL GROUND	DIGITAL GROUND
SC1–SC2*	SELECT CONVERTER RESOLUTION
DATA LOAD*	LOGIC LO DB1–D16 INPUTS LOGIC HI DB1–D16 OUTPUTS
BUSY	CONVERTER BUSY, DATA NOT VALID WHILE BUSY HI
DIRECTION	LOGIC STATE DEFINES DIRECTION OF INPUT SIGNAL ROTATION
RIPPLE CLOCK	POSITIVE PULSE WHEN CONVERTER OUTPUT CHANGES FROM 1S TO ALL 0S OR VICA VERSA
$-V_S$	NEGATIVE POWER SUPPLY
VCO I/P	VCO INPUT
INTEGRATOR I/P	INTEGRATOR INPUT
INTEGRATOR O/P	INTEGRATOR OUTPUT
DEMOD O/P	DEMODULATOR OUTPUT
$\overline{\text{COMPLEMENT}}$*	ACTIVE LOGIC LO
VCO O/P*	VCO OUTPUT

*AD2S82A ONLY.

Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

Bit Weight Table

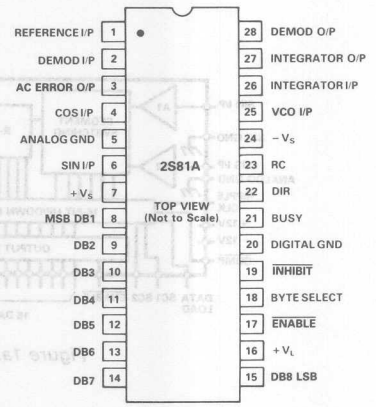
ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

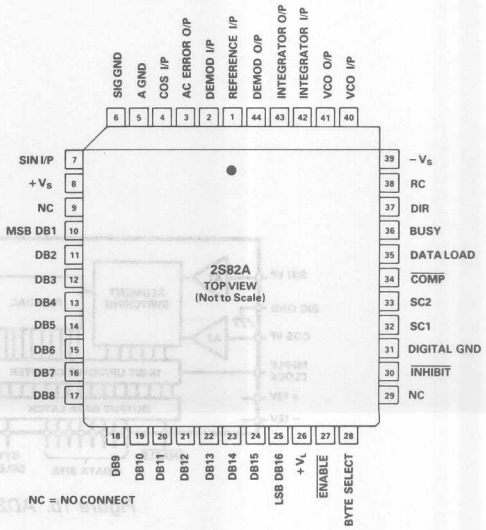
$+V_S$[2] . . . . . +14 V dc
$-V_S$ . . . . . −14 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +14 V to $-V_S$
SIN . . . . . +14 V to $-V_S$
COS . . . . . +14 V to $-V_S$
Any Logical Input . . . . . −0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +14 V to $-V_S$
Integrator Input . . . . . +14 V to $-V_S$
VCO Input . . . . . +14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
Commercial (JD, HP, JP, KP, LP) . . . . . 0 to +70°C
Storage Temperature (All Grades) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

CAUTION:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

AD2S81A/2S82A PIN CONFIGURATIONS





CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and −12 V dc and must not be reversed. The voltage applied to V_L can be +5 V dc to $+V_S$.

It is recommended that the decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 μF (tantalum). Also capacitors of 100 nF and 10 μF should be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER."

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the resolver to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figures 1a and 1b.

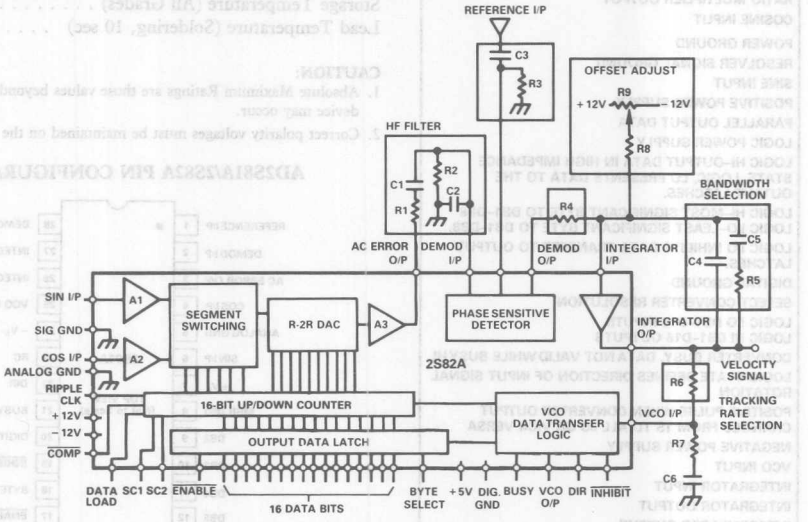


Figure 1a. AD2S82A Connection Diagram

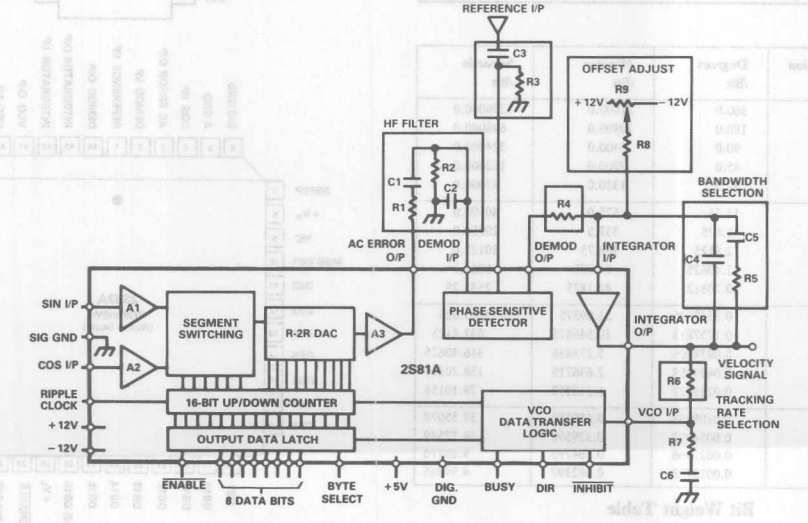


Figure 1b. AD2S81A Connection Diagram

CONVERTER RESOLUTION (AD2S82A ONLY)

Two major areas of the AD2S82A specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO, respectively (see section COMPONENT SELECTION). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do it when the BUSY is low, i.e., when Data is not changing.

CONVERTER OPERATION

When connected in a circuit such as shown in Figure 1, the AD2S81A/AD2S82A operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S81A/AD2S82A is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING

The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S81A/AD2S82A will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S81A/AD2S82A will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak). Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changing state (1 LSB min change) with a corresponding change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$.

The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR INPUT (which can be trimmed out – see Figures 1a and 1b), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S81A/AD2S82A can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

In many applications it is possible to use the velocity signal of the AD2S81A/AD2S82A to replace a conventional tachogenerator.

DC ERROR SIGNAL

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. This is the dc error of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in-test."

The following instructions describe how to select the external components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

PC compatible software is available to help users select the optimum component values for the AD2S81A and AD2S82A, and display the transfer gain, phase and small step response.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S81A/AD2S82A, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.
   Values should be chosen so that

$$15\ k\Omega \leq R1 = R2 \leq 56\ k\Omega$$

$$C1 = C2 = \frac{1}{2\ \pi\ R1\ f_{REF}}$$

   and f_{REF} = Reference Frequency (Hz)
   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted, then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\ \Omega$$

   where 100×10^{-9} = current/LSB
   If R1, C2 are not fitted, then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\ \Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling of the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100\ k\Omega$$

$$C3 > \frac{1}{R3 \times f_{REF}}\ F$$

   with R3 in Ω.

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter, and hence the velocity scaling as at the max tracking rate the velocity output will be 8 V.
   per second. Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{6.32 \times 10^{10}}{T \times n}\ \Omega$$

   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does not exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100 Hz for a 400 Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.
   b. Select C4 so that

$$C4 = \frac{21}{R6 \times f_{BW}^2}\ F$$

   with R6 in Ω and f_{BW} in Hz selected above.
   c. C5 is given by

$$C5 = 5 \times C4\ F$$

   d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted:

$$C6 = 470\ pF \quad R7 = 68\ \Omega$$

7. Offset Adjust
   Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.
   If fitted, the following values of R8 and R9 should be used:

$$R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega\ potentiometer$$

   To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.
   The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL level. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input on the AD2S82A selects the byte of the position data to be presented at the data output DB1 to DB8. The least significant byte will be presented on data output DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S82A is used with a resolution less than 16 bits, the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output DB1 and DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

When the BYTE select pin is a logic "HI" on the AD2S81A, the most significant byte is presented on Pins 8 to 15 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO"). A logic "HI" presents the 4 least significant bits on Pins 8 to 11 and places a logic "LO" on Pins 12 to 15 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO").

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK

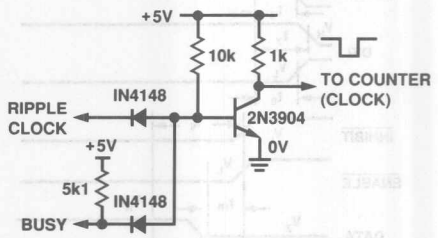
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulse width of the ripple clock is 300 ns. RIPPLE CLOCK is normally set high before a BUSY pulse and resets before the next positive going edge of the next consecutive pulse.

The only exception to this is when DIR changes while the RIPPLE CLOCK is high. Resetting of the RIPPLE clock will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

If the AD2S81A/AD2S82A is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2).

RIPPLE CLOCK is unaffected by $\overline{\text{INHIBIT}}$.



NOTE: DO NOT USE ABOVE CCT WHEN $\overline{\text{INHIBIT}}$ IS "LO."

Figure 2. Diode Transistor Logic Nand Gate

DIRECTION Output

The DIRECTION (DIR) logic output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA, and RIPPLE CLOCK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This corresponds to a change in input rotation direction but less than 1 LSB.

$\overline{\text{COMPLEMENT}}$ (AD2S82A Only)

The $\overline{\text{COMPLEMENT}}$ input is internally pulled to +12 V in the INACTIVE STATE. It is pulled down to DIGITAL GROUND (100 μA) to ACTIVATE.

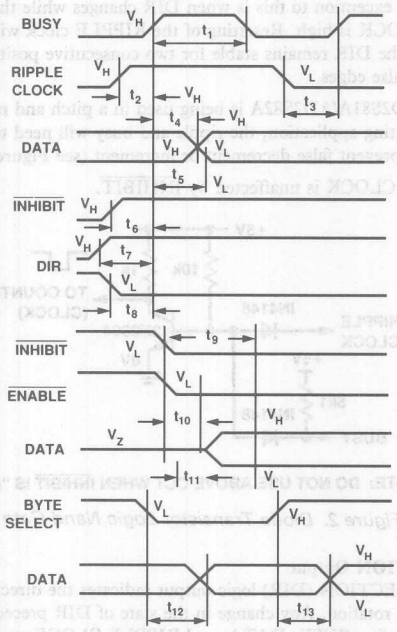
When used in conjunction with DATA LOAD, strobing DATA LOAD and $\overline{\text{COMPLEMENT}}$ pins to logic LO, will set the logic HIGH bits of the AD2S82A counter to a LO state. Those bits of the applied data which are logic LO will not change the corresponding bits in the AD2S82A counter:

For Example:	
Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after Data Load	1 1 0 0 0
Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after Data Load and Complement	0 0 1 0 1

In order to read the output the following procedures should be followed:

1. Place Outputs in high impedance state ($\overline{\text{ENABLE}}$ = HI).
2. Present data to pins.
3. Pull DATA LOAD and $\overline{\text{COMPLEMENT}}$ pins to ground.
4. Wait 100 ns.
5. Remove data from pins.
6. Remove outputs from high impedance state ($\overline{\text{ENABLE}}$ = LO).
7. Read outputs.

DIGITAL TIMING



PARAMETER	T_{MIN}	T_{MAX}	CONDITION
t_1	200	600	BUSY WIDTH $V_H - V_H$
t_2	10	25	RIPPLE CLOCK V_H TO BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L TO NEXT BUSY V_H
t_4	16	45	BUSY V_H TO DATA V_H
t_5	3	25	BUSY V_H TO DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H TO BUSY V_H
t_7	485	625	MIN DIR V_H TO BUSY V_H
t_8	515	670	MIN DIR V_H TO BUSY V_H
t_9	–	600	$\overline{\text{INHIBIT}}$ V_L TO DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_L
t_{12}	60	140	BYTE SELECT V_L TO DATA STABLE
t_{13}	60	125	BYTE SELECT V_H TO DATA STABLE

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The AD2S81A/AD2S82A allows the user greater flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the AD2S81A/AD2S82A and the variations in the dynamic performance available to the user.

Loop Compensation

The AD2S81A and AD2S82A (connected as shown in Figure 1a and 1b) operates as a type 2 tracking servo loop where the VCO/counter combination and integrator perform the two integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0 dB axis with 180° of additional phase lag, as shown in Figure 5. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The AD2S81A/AD2S82A does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer (see Application Note).

A block diagram of the AD2S81A/AD2S82A is given in Figure 3.

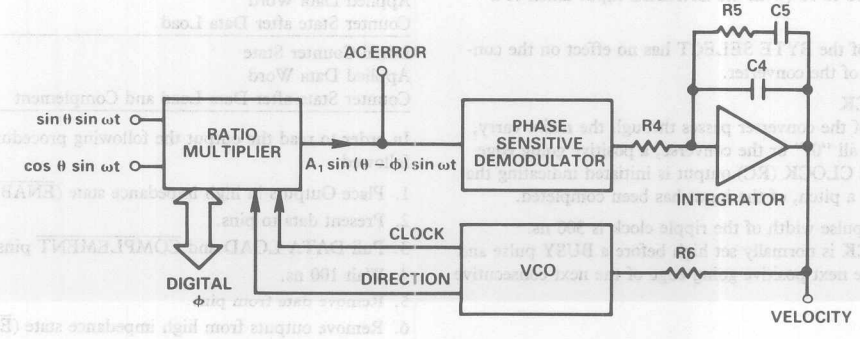


Figure 3. AD2S81A/AD2S82A Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the AD2S81A/AD2S82A and compares the signal from the resolver input angle, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by an electromechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin \omega t$$

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5.

So for 2 V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{n}\right) \times A1$$

Where n = bits per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

Giving an AC ERROR output
= 178 mV/bit @ 10 bits resolution
= 44.5 mV/bit @ 12 bits
= 11.125 mV/bit @ 14 bits
= 2.78 mV/bit @ 16 bits

The ratio multiplier will work in exactly the same way whether the AD2S81A/AD2S82A is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the AD2S81A/AD2S82A is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (DEMODULATOR\ INPUT\ rms\ voltage)$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160 mV/bit (10 bits resolution)
= 40 mV/bit (12 bits resolution)
= 10 mV/bit (14 bits resolution)
= 2.5 mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the AD2S81A/AD2S82A to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ), feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 LSB. In order to ensure that this feedback "hysteresis" is set to 1 LSB the input current to the integrator must be scaled to be 100 nA/bit. Therefore,

$$R4 = \frac{DC\ Error\ Scaling\ (mV/bit)}{100\ (nA/bit)}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100 nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocking either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

The VCO rate is fixed for a given input current by the VCO scaling factor:

$$= 7.9\ kHz/\mu A$$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5 V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$$(100 \times 4096)/(7900) = 51.8\ \mu A$$

Thus, R6 would be set to: $5/(51.8 \times 10^{-6}) = 96\ k\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

$$Velocity\ Offset\ Voltage = R6 \times (VCO\ bias\ current)$$

The temperature coefficient of this offset is given by

$$Velocity\ Offset\ Tempco = R6 \times (VCO\ bias\ current\ tempco)$$

where the VCO bias current tempco is typically −1.22 nA/°C.

The maximum recommended rate for the VCO is 1.1 MHz which sets the maximum possible tracking rate.

Since the minimum voltage swing available at the integrator output is ±8 V, this implies that the minimum value for R6 is 57 kΩ. As

$$Max\ Current = \frac{1.1 \times 10^6}{7.9 \times 10^3} = 139\ \mu A$$

$$Min\ Value\ R6\ \frac{8}{139 \times 10^{-6}} = 57\ k\Omega$$

VCO OUTPUT

In order to overcome the "freeplay" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of digital angle output.

The converter updates the output if the error is an LSB or greater and the VCO output gives the positional error smaller than 1 LSB.

Figure 4 illustrates how the VCO output compensates for instances where, due to hysteresis, there is no change in the digital count output for 1 LSB change in input angle. The sum of the digital count output and VCO output equals the actual input angle.

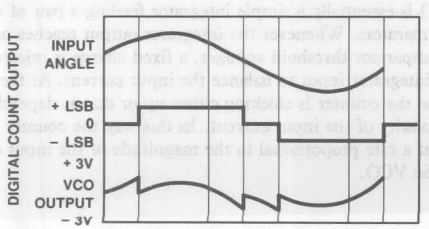


Figure 4.

tion "Component Selection," the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\ (1 + s_N)}{(s_N + 2.4)\ (s_N^2 + 3.4\ s_N + 5.8)}$$

where, s_N, the normalized frequency variable is:

$$s_N = \frac{2}{\pi}\ \frac{s}{f_{BW}}$$

and f_{BW} is the closed loop 3 dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2\ sec^{-2}$$

The normalized gain and phase diagrams are given in Figures 5 and 6.

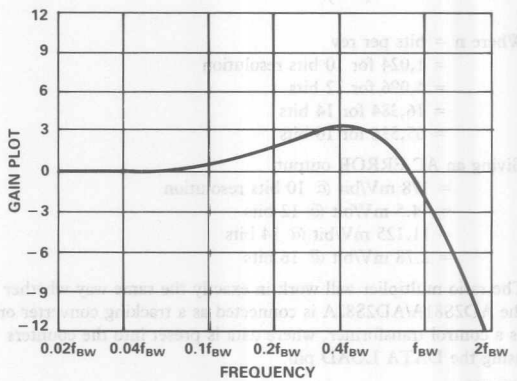


Figure 5. AD2S81A/AD2S82A Gain Plot

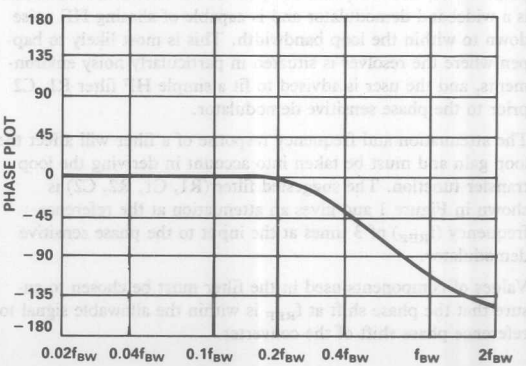


Figure 6. AD2S81A/AD2S82A Phase Plot

The small signal step response is shown in Figure 7. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter is settled to 1 LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

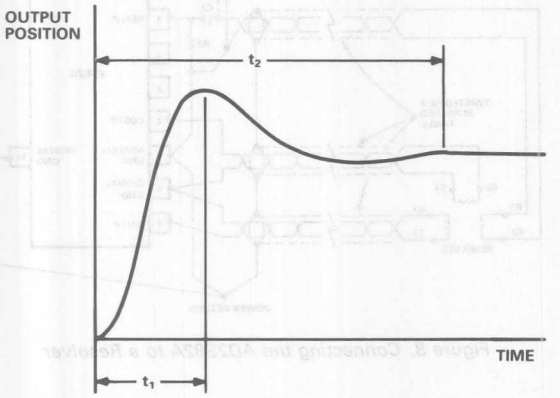


Figure 7. AD2S81A/AD2S82A Small Step Response

The large signal step response (for steps greater than 5 degrees) applies when the error voltage exceeds the linear range of the converter.

Typically the converter will take three times longer to reach the first peak for a 179 degrees step.

In response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error output in degrees. Angular measurement may also be specified using radians, minutes of arc, LSBs, etc.

K_A does not define maximum input acceleration, only the error due to it's acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$Angular\ Accuracy \times K_A = degrees/sec^2$$

K_A can be used to predict the output position error for a given input acceleration. For example for an acceleration of 100 revs/sec^2, $K_A = 2.7 \times 10^6$ sec^{-2} and 12-bit resolution.

$$Error\ in\ LSBs = \frac{Input\ acceleration\ [LSB/sec^2]}{K_A\ [sec^{-2}]}$$

$$= \frac{100\ [rev/sec^2] \times 2^{12}}{2.7 \times 10^6} = 0.15\ LSBs\ or\ 47.5\ seconds\ of\ arc$$

To determine the value of K_A based on the passive components used to define the dynamics of the converter the following should be used:

$$K_A = \frac{4.04 \times 10^{11}}{2^n \cdot R6 \cdot R4 \cdot (C4 + C5)}$$

Where n = resolution of the converter
R4, R6 in ohms
C5, C4 in farads

SOURCES OF ERRORS

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will typically be 1 arc minute over the operating temperature range.

A description of how to adjust from zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1a, b.

Differential Phase Shift

Phase shift between the sine and cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

Error = 0.53 a × b arc minutes

where a = differential phase shift (degrees).
b = signal to reference phase shift (degrees).

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions the extra error can be made insignificant.

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (Degrees)}{Reference\ Frequency}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5 kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \text{ degrees}$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY ERRORS

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in the place of a velocity transducer. Although the conversion loop of the AD2S81A/AD2S82A includes a digital section, there is an additional analog feedback loop around the velocity signal. This ensures against flicker in the digital positional output in both dynamic and static states.

A better quality velocity signal will be achieved if the following points are considered:

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion error.[1]
   The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the AD2S81A/AD2S82A with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   Maintenance of the input signal voltages at 2 V rms will prevent LSB flicker at the positional output. The analog feedback or hysteresis employed around the VCO and the integrator is a function of the input signal levels (see section "INTEGRATOR").

Following the preceding precautions will allow the user to use the velocity signal in very noisy environments for example PWM motor drive applications. Resolver/converter error curves may exhibit apparent acceleration/deceleration at a constant velocity. This results in ripple on the velocity signal of frequency twice the input rotation.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 8.

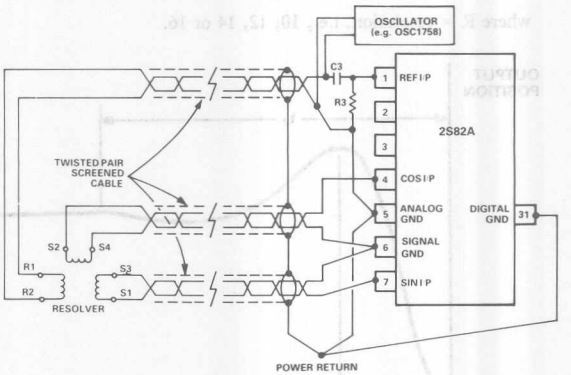


Figure 8. Connecting the AD2S82A to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1a, b).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $\frac{1}{2\pi RC}$

by altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

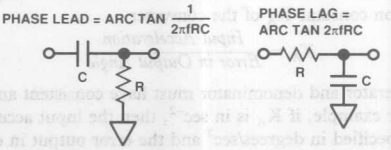


Figure 9. Phase Shift Circuits

[1]Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO.

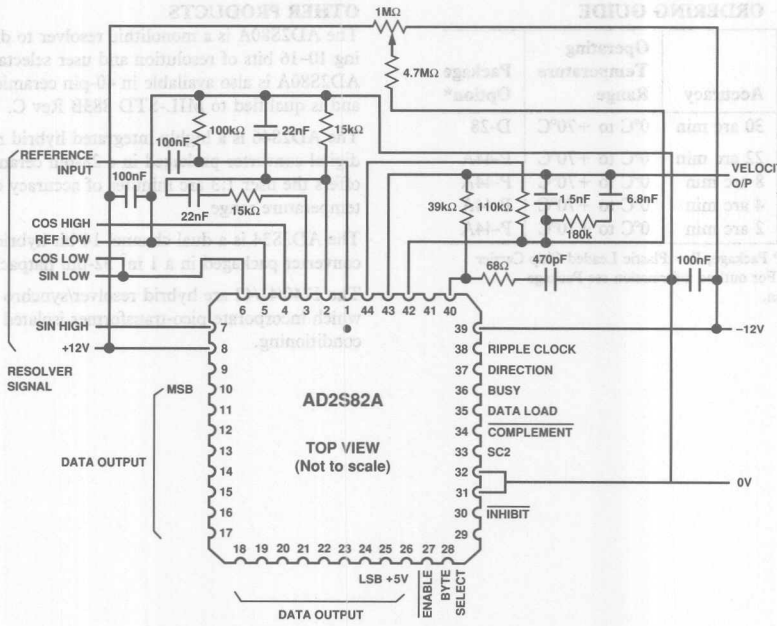


Figure 10. Typical Circuit Configuration

TYPICAL CIRCUIT CONFIGURATION

Figure 10 shows a typical circuit configuration for the AD2S81A/AD2S82A in a 12-bit resolution mode. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 2.7×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

For more information on resistive scaling of SIN, COS and REFERENCE converter inputs, refer to the application note "Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters."

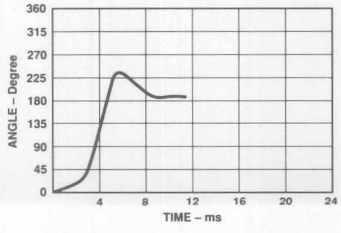


Figure 11. Large Step Response Curves for Typical Circuit Shown in Figure 10

APPLICATIONS

Control Transformer

The ratio multiplier of the AD2S82A can be used independently of the loop integrators as a *control transformer*. In this mode the resolver inputs θ are multiplied by a digital angle ϕ, any difference between ϕ and θ will be represented by the AC ERROR output as SIN ωt sin (θ–ϕ) or the DEMOD output as sin (θ–ϕ). To use the AD2S81A/AD2S82A in this mode refer to the "Control Transformer" application note.

Dynamic Switching

In applications where the user requires wide band response from the converter, for example 100 rpm to 6000 rpm, superior performance is achieved if the converters control characteristics are switched dynamically. This reduces velocity offset levels at low tracking rates. For more information on the technique refer to "Dynamic Resolution Switching Using the Variable Resolution Monolithic Resolver-to-Digital Converters."

ORDERING GUIDE

	Accuracy	Operating Temperature Range	Package Option*
AD2S81AJD	30 arc min	0°C to +70°C	D-28
AD2S82AHP	22 arc min	0°C to +70°C	P-44A
AD2S82AJP	8 arc min	0°C to +70°C	P-44A
AD2S82AKP	4 arc min	0°C to +70°C	P-44A
AD2S82ALP	2 arc min	0°C to +70°C	P-44A

*D = Ceramic DIP Package; P = Plastic Leaded Chip Carrier (PLCC) Package. For outline information see Package Information section.

OTHER PRODUCTS

The AD2S80A is a monolithic resolver to digital converter offering 10–16 bits of resolution and user selectable dynamics. The AD2S80A is also available in 40-pin ceramic DIP, 44-pin LCC and is qualified to MIL-STD 883B Rev C.

The AD2S46 is a highly integrated hybrid resolver/synchro to digital converter packaged in a 28-pin ceramic DIP. The part offers the user 1.3 arc minutes of accuracy over the full military temperature range.

The AD2S34 is a dual channel 14-bit hybrid resolver to digital converter packaged in a 1 in^2 32-pin flatpack.

The 1740/41/42 are hybrid resolver/synchro to digital converters which incorporate pico-transformer isolated input signal conditioning.

Variable Resolution, Monolithic Resolver-to-Digital Converter

AD2S83

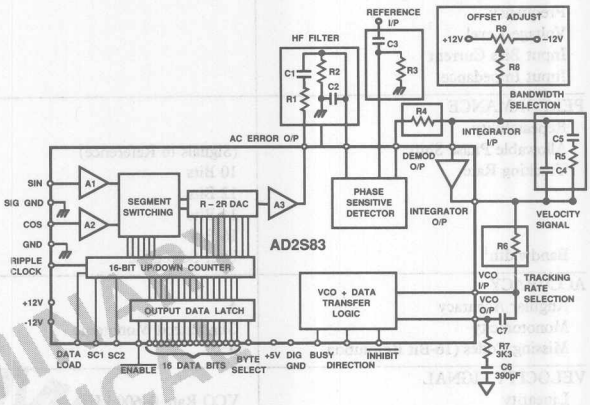
FEATURES

Monolithic Tracking R/D Converter
44-Pin PLCC Package
10-, 12-, 14- or 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
High Accuracy Velocity Output
Industrial Temperature Range Versions
ESD Class 2 Protection (2,000 V min)

APPLICATIONS

DC and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control
Military Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S83 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin PLCC ceramic package. It is manufactured on Analog Devices' BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip.

The converter allows users *to select their own resolution and dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S83 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long leads allowing the converter to be located remote from the resolver.

The position output from the converter is presented via 3-state output pins which can be configured for operations with 8- or 16-bit busses. BYTE SELECT, ENABLE and INHIBIT pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

The AD2S83 operates over reference frequencies in the range 50 Hz to 20,000 Hz.

PRODUCT HIGHLIGHTS

High Accuracy Velocity Output. A precision analog velocity signal with a typical linearity of ±0.25% and reversion error less than ±0.5% is generated by the AD2S83. The provision of this signal removes the need for mechanical tachogenerators used in servo systems to provide loop stabilization and speed control.

Monolithic. A one-chip solution reduces the package size and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S83 to be 10, 12, 14 or 16 bits allowing the user to use the AD2S83 with the optimum resolution for each application.

Ratiometric Tracking Conversion. This technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the free component selection software.

Low Power Consumption. Typically only 300 mW.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S83—SPECIFICATIONS (typical at +25°C unless otherwise specified)

Parameter	Conditions	AD2S83J Min	Typ	Max	Units
SIGNAL INPUTS (SIN, COS)					
Frequency		50		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
REFERENCE INPUT (REF)					
Frequency		50		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
PERFORMANCE					
Repeatability				±1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10	Degrees
Tracking Rate	10 Bits			1040	rps
	12 Bits			260	rps
	14 Bits			65	rps
	16 Bits			16.25	rps
Bandwidth[1]	User Selectable				
ACCURACY					
Angular Accuracy	A			**±8 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A			**4**	Codes
VELOCITY SIGNAL					
Linearity	VCO Rate 0–600 kHz		0.25	**0.4**	% FSD
	VCO Rate 600 kHz–1100 kHz		0.5	0.8	% FSD
Reversion Error			0.25	0.5	% FSD
DC Zero Offset[2]				**6**	mV
DC Zero Offset Tempco			−22		µV/°C
Gain Scaling Accuracy					% FSD
Output Voltage	1 mA Load	±8			V
Dynamic Ripple	Mean Value				% rms O/P
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				Bits
Output Format	Bidirectional Natural Binary				
Load				**3**	LSTTL
$\overline{\text{INHIBIT}}$[3]					
Sense	Logic LO to $\overline{\text{INHIBIT}}$				
Time to Stable Data				600	ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output				
	Logic HI Outputs in High				
$\overline{\text{ENABLE}}$[3]/Disable Time	Impedance State	35		110	ns
BYTE SELECT[3]					
Sense					
Logic HI	MS Byte DB1–DB8				
Logic LO	LS Byte DB1–DB8				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High via 100 kΩ				
	100 kΩ to $+V_S$				
SC1 SC2					
0 0	10-Bit Resolution				
0 1	12-Bit Resolution				
1 0	14-Bit Resolution				
1 1	16-Bit Resolution				

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Conditions	AD2S83 Min	Typ	Max	Units
$\overline{\text{COMPLEMENT}}$	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO to Activate; No Connect for Normal Operation				
$\overline{\text{DATA LOAD}}$					
Sense	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[3]					
Sense	Logic HI When Position O/P Changing				
Width		**200**		**600**	ns
Load	Use Additional Pull-Up (See Figure 2)			1	LSTTL
DIRECTION[3]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[3]					
Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	**300**			
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS					
Input High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	**2.0**			V
Input Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			**0.8**	V
DIGITAL INPUTS					
Input High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			**±100**	μA
Input Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			**±100**	μA
DIGITAL INPUTS					
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**1.0**	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**−400**	μA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ μA	**2.4**			V
Low Voltage, V_{OL}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			**0.4**	V

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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Current I_L	DB1-DB16 Only $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±50 ±50	µA µA
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Gain					
In Phase	w.r.t. REF	−0.882	−0.9	−0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	**150**	nA
Input Impedance			1		MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57	60	63	dB
Dead Zone Current (Hysteresis)			100		nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	**150**	nA
Output Voltage Range		±8			V
VCO					
Maximum Rate		1.0	1.1		MHz
VCO Rate	+ve DIR	8.1	8.3	8.5	kHz/µA
	−ve DIR	8.1	8.3	8.5	kHz/µA
VCO Power Supply Sensitivity					
Increase	$+V_S$			−0.5	%/V
	$-V_S$			+0.5	%/V
Input Offset Voltage				0.6	mV
Input Bias Current			12	55	nA
Input Bias Current Tempco			−1.22		nA/°C
Input Voltage Range				±8	V
Linearity of Absolute Rate					
Full Range			0.5	**0.8**	% FSD
Over 0% to 50% of Full Range			0.25	**0.4**	% FSD
Reversion Error			0.25	0.5	% FSD
POWER SUPPLIES					
Voltage Levels					
$+V_S$		**+10.8**		**+13.2**	V
$-V_S$		**−10.8**		**−13.2**	V
$+V_L$		**+5**		**$+V_S$**	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	**±23**	mA
$\pm I_S$	$\pm V_S$ @ ±13.2 V		±19	**±30**	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	**±1.5**	mA

All min and max specifications are guaranteed. Specifications in **boldface** and tested on all production units at final electrical test.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2]	+14 V dc
$-V_S$	−14 V dc
$+V_L$[2]	$+V_S$
Reference	+14 V to $-V_S$
SIN	+14 V to $-V_S$
COS	+14 V to $-V_S$
Any Logic Input	−0.4 V dc to $+V_L$ dc
Demodulator Input	+14 V to $-V_S$
Integrator Input	+14 V to $-V_S$
VCO Input	+14 V to $-V_S$
Power Dissipation	860 mW
Operating Temperature	
Industrial (AP)	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

CAUTION:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$)	±12 V dc ± 10%
Power Supply Voltage V_L	+5 V dc ± 10%
Analog Input Voltage (SIN and COS)	2 V rms ± 10%
Analog Input Voltage (REF)	1 V to 8 V peak
Signal and Reference Harmonic Distortion	10% (max)
Phase Shift Between Signal and Reference	±10 Degrees (max)
Ambient Operating Temperature Range	
Industrial (AP)	−40°C to +85°C

3

PRELIMINARY TECHNICAL DATA

ESD SENSITIVITY

The AD2S83 features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

The AD2S83 is ESD protection Class II (2000 V min). Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual.*



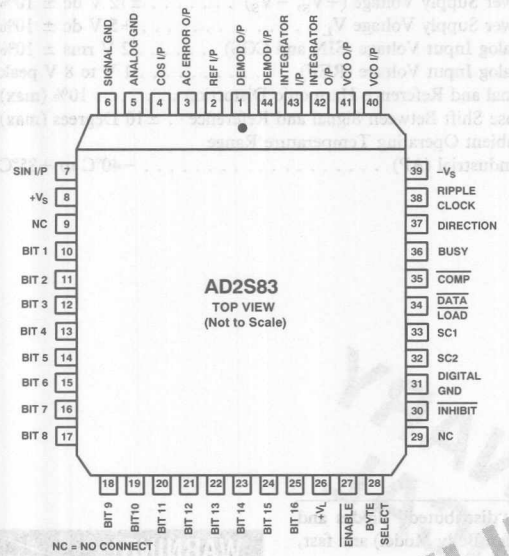
ORDERING GUIDE

Model	Temperature Range	Package Accuracy	Option*
AD2S83AP	−40°C to +85°C	8 arc min	P-44A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN CONFIGURATION



PIN DESIGNATIONS

Pin Nos.	Mnemonic	Description
1	REFERENCE I/P	Reference Signal Input
2	DEMOD I/P	Demodulator Input
3	AC ERROR O/P	Ratio Multiplier Output
4	COS	Cosine Input
5	ANALOG GND	Power Ground
6	SIGNAL GND	Resolver Signal Ground
7	SIN	Sine Input
8	$+V_S$	Positive Power Supply
10–25	BIT 1–BIT 16	Parallel Output Data
26	$+V_L$	Logic Power Supply
27	$\overline{\text{ENABLE}}$	Logic HI–Output Data in High Impedance State Logic LO–Presents Data to the Output Latches
28	BYTE SELECT	Logic HI–Most Significant Byte to DB1–DB8 Logic LO–Least Significant Byte to DB1–DB8
30	$\overline{\text{INHIBIT}}$	Logic LO Inhibits Data Transfer to Output Latches
31	DIGITAL GND	Digital Ground
32, 33	SC1–SC2	Select Converter Resolution
34	$\overline{\text{DATA LOAD}}$	Logic LO DB1–DB16 Inputs
35	$\overline{\text{COMPLEMENT}}$	Logic HI DB1–D16 Outputs
36	BUSY	Converter Busy, Data not Valid While Busy HI
37	DIRECTION	Logic State Defines Direction of Input Signal Rotation
38	RIPPLE CLOCK	Positive Pulse when Converter. Output Changes from 1s to All 0s or Vice Versa
39	$-V_S$	Negative Power Supply
40	VCO I/P	VCO Input
41	VCO O/P	VCO Output
42	INTEGRATOR O/P	Integrator Output
43	INTEGRATOR I/P	Integrator Input
44	DEMOD I/P	Demodulator Output

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Cost, Complete 12-Bit Resolver-to-Digital Converter

AD2S90

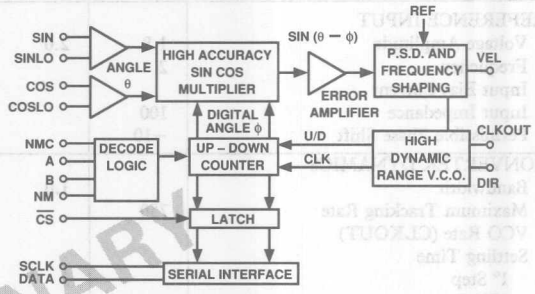
FEATURES

Complete Monolithic Resolver-to-Digital Converter
Incremental Encoder Emulation (1024-Line)
Absolute Serial Data (12-Bit)
Differential Inputs
12-Bit Resolution
Analog Velocity Output
Industrial Temperature Range
20-Pin PLCC
Low Power

APPLICATIONS

Industrial Motor Control
Servo Motor Control
Industrial Gauging
Encoder Emulation
Automotive Motion Sensing and Control
Factory Automation
Limit Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S90 is a complete 12-bit resolution tracking resolver-to-digital converter. No external components are required to operate the device.

The converter accepts 2 V rms ± 10% input signals in the range 2–10 kHz on the SIN, COS and REF inputs. A Type II servo loop is employed to track the inputs and convert the input SIN and COS information into a digital representation of the input angle. The bandwidth of the converter is set internally at 1 kHz. The maximum tracking rate is 750 rps at 12-bit resolution.

Angular position output information is available in two forms, absolute serial binary and incremental A quad B.

The absolute serial binary output is 12-bit (1 in 4096). The data output pin is high impedance when Chip Select $\overline{CS}$ is logic HI. This allows the connection of multiple converters onto a common bus. Absolute angular information in serial pure binary form is accessed by $\overline{CS}$ followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz

The encoder emulation outputs A, B and NM continuously produce signals equivalent to a 1024 line encoder. When decoded this corresponds to 12-bits resolution. Three common north marker pulse widths are selected via a single pin (NMC).

An analog velocity output signal provides an accurate representation of input angular velocity of the input signals, in either a clockwise or counterclockwise direction. The velocity full scale is ±2.5 V dc equivalent to ±300 rps/V dc.

The AD2S90 operates on a ±5 V dc ±5% power supplies and is fabricated on Analog Devices' Linear Compatible CMOS process (LC^2MOS). LC^2MOS is a mixed technology process that combines precision bipolar circuits with low power CMOS logic circuits.

PRODUCT HIGHLIGHTS

Complete Resolver–Digital Interface. The AD2S90 provides the complete solution for digitizing resolver signals (12-bit resolution) without the need for external components.

Dual Format Position Data. Incremental encoder emulation in standard A QUAD B format with selectable North Marker width. Absolute serial 12-bit angular binary position data accessed via simple 3-wire interface.

Single High Accuracy Grade in Low Cost Package. ±8 arc minutes of angular accuracy available in a 20-pin PLCC.

Low Power. 50 mW power consumption.

Analog Velocity Output. Analog output which represents the input velocity of a resolver shaft.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S90—SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, T_A = −40°C to +85°C unless otherwise stated)

Parameter	Min	Typ	Max	Units	Test Condition
SIGNAL INPUTS					
Voltage Amplitude	1.8	2.0	2.2	V rms	Differential SIN to SIN LO, COS to COS LO
Frequency	2		10	kHz	
Input Bias Current			100	nA	V_{IN} = 2 ± 10% V rms
Input Impedance	1.0			MΩ	V_{IN} = 2 ± 10% V rms
Common-Mode Volts[1]			100	mV peak	CMV @ SINLO, COSLO w.r.t.
CMRR	60			dB	AGND @ 10 kHz
REFERENCE INPUT					
Voltage Amplitude	1.8	2.0	2.2	V rms	
Frequency	2		10	kHz	
Input Bias Current			100	nA	
Input Impedance	100			kΩ	
Permissible Phase Shift	−10		+10	Degrees	Relative to SIN, COS Inputs
CONVERTER DYNAMICS					
Bandwidth		1.0		kHz	
Maximum Tracking Rate	750			rps	
VCO Rate (CLKOUT)			2.0	MHz	
Settling Time					
1° Step		5		ms	
179° Step		20		ms	
ACCURACY					
Angular Accuracy			±8 +1 LSB[2]	arc min	
Repeatability[3]			1	LSB	
VELOCITY OUTPUT					
Scaling	285	300	315	rps/V dc	
Max Output Voltage	±2.375	±2.500	±2.625	V dc	
Reversion Error			±0.5	% FS	V_{OUT} = ±2.5 V dc
Linearity			1.0	% FS	
Offset			±10	mV dc	
Load Drive Capability			±250	μA	V_{OUT} = ±2.5 V dc
LOGIC INPUTS SCLK, CS					
Input High Voltage (V_{INH})	3.5			V dc	V_{DD} = +5 V dc, V_{SS} = −5 V dc
Input Low Voltage (V_{INL})			1.5	V dc	V_{DD} = +5 V dc, V_{SS} = −5 V dc
Input Current (I_{IN})			10	μA	
Input Capacitance			10	pF	
LOGIC OUTPUTS DATA, A, B, NM, CLKOUT, DIR					V_{DD} = +5 V dc, V_{SS} = −5 V dc
Output High Voltage	4.0			V dc	I_{OH} = 1 mA
Output Low Voltage			1.0	V dc	I_{OL} = 1 mA
SERIAL CLOCK (SCLK)					
SCLK Input Rate			2	MHz	1:1 Mark Space Ratio
Rise/Fall Time			10	ns	
NORTH MARKER CONTROL (NMC)					
90°	+4.75	+5.0	+5.25	V dc	North Marker Width Relative to
180°	−0.75	0.0	+0.75	V dc	to "A" Cycle
360°	−4.75	−5.0	−5.25	V dc	
POWER SUPPLIES					
V_{DD}	+4.75	+5.00	+5.25	V dc	
V_{SS}	−4.75	−5.00	−5.25	V dc	
I_{DD}			8.0	mA	
I_{SS}			8.0	mA	

NOTES
[1]If the tolerance on signal inputs = ±5%, then CMV = 200 mV.
[2]1 LSB = 5.3 arc minute.
[3]Specified at constant temperature.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($V_{DD}-V_{SS}$) . . . . . ±5 V dc ± 5%
Analog Input Voltage (SIN, COS & REF) . . . 2 V rms ± 10%
Signal and Reference Harmonic Distortion 10%
Phase Shift between Signal and Reference . . . . . ±10°
Ambient Operating Temperature Range
Industrial (AP) . . . . . −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

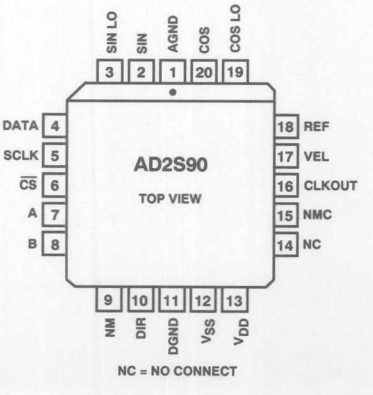
V_{DD} to AGND . . . . . −0.3 V dc to +7.0 V dc
V_{SS} to AGND . . . . . +0.3 V dc to −7.0 V dc
AGND to DGND . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND
REF . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
SIN, SIN LO . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
COS, COS LO . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
Analog Output to AGND
VEL . . . . . V_{SS} to V_{DD}
Digital Inputs to DGND, CSB,
SCLK, RES . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Digital Outputs to DGND, NM, A,B,
DIR, CLKOUT DATA . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Operating Temperature Range
Industrial (AP) . . . . . −40°C to +85°C
Lead Temperature (Soldering 10 secs) . . . . . 300°C
Power Dissipation to +75°C . . . . . 300 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Option*
AD2S90AP	−40°C to +85°C	8 arc min	P-20A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.



NC = NO CONNECT

PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	AGND	Analog ground, reference ground.
2	SIN	SIN channel noninverting input connect to resolver SIN HI output. SIN to SIN LO = 2 V rms ± 10%.
3	SIN LO	SIN channel inverting input connect to resolver SIN LO.
4	DATA	Serial interface data output. High impedance with $\overline{CS}$ = HI. Enabled by $\overline{CS}$ = 0.
5	SCLK	Serial interface clock. Data is clocked out on "first" negative edge of SCLK after a LO transition on $\overline{CS}$. 12 SCLK pulses to clock data out.
6	$\overline{CS}$	Chip select. Active LO. Logic LO transition enables DATA output.
7	A	Encoder A output. A leads B for increasing angular rotation.
8	B	Encoder B output.
9	NM	Encoder North Marker emulation output. Pulse triggered as code passes through zero. Three common pulse widths available.
10	DIR	Indicates direction of rotation of input. Logic HI = increasing angular rotation. Logic LO = decreasing angular rotation.
11	DGND	Digital power ground return.
12	V_{SS}	Negative power supply, −5 V dc ± 5%.
13	V_{DD}	Positive power supply, +5 V dc ± 5%.
14	NC	Not connected.
15	NMC	North marker width control. Internally pulled HI via 50 kΩ nominal.
16	CLKOUT	Internal VCO clock output. Indicates angular velocity of input signals. Max rate = 2 MHz. CLKOUT is a 200 ns positive pulse.
17	VEL	Bipolar analog velocity output. Indicates angular velocity of input signals. Positive voltage w.r.t. AGND indicates increasing angle. FSD = 750 rps.
18	REF	Converter reference input. Normally derived from resolver primary excitation. REF = 2 V rms ± 10%. Phase shift w.r.t. COS and SIN = ±10° max.
19	COS LO	COS channel inverting input. Connect to resolver COS LO.
20	COS	COS channel noninverting input. Connect to resolver COS HI output. COS = 2 V rms ± 10%.

PRELIMINARY TECHNICAL DATA

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Pin No.	Mnemonic	Function
1	AGND	Analog ground, reference ground.
2	SIN	SIN channel noninverting input connect to resolver SIN HI output. SIN to SIN L.O = 2 V rms ± 10%.
3	SIN L.O	SIN channel inverting input connect to resolver SIN L.O.
4	DATA	Serial interface data output. High impedance with $\overline{CS}$ = HI. Enabled by $\overline{CS}$ = 0.
5	SCLK	Serial interface clock. Data is clocked out on "first" negative edge of SCLK after a L.O transition on $\overline{CS}$. 12 SCLK pulses to clock data out.
6	$\overline{CS}$	Chip select. Active L.O. Logic L.O transition enables DATA output.
7	A	Encoder A output. A leads B for increasing angular rotation.
8	B	Encoder B output.
9	NM	Encoder North Marker emulation output. Pulse triggered as code passes through zero. Three common pulse widths available.
10	DIR	Indicate direction of rotation of input. Logic HI = increasing angular rotation. Logic LO = decreasing angular rotation.
11	DGND	Digital power ground return.
12	V_{SS}	Negative power supply, −5 V dc ± 5%.
13	V_{DD}	Positive power supply, +5 V dc ± 5%.
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17	VEL	Bipolar analog velocity output. Indicates angular velocity of input signals. Positive voltage w.r.t. AGND indicates increasing angle. FSD = 750 rps.
18	REF	Converter reference input. Normally derived from resolver primary excitation. REF = 2 V rms ± 10%. Phase shift w.r.t. COS and SIN = ± 10° max.
19	COS L.O	COS channel inverting input. Connect to resolver COS L.O.
20	COS	COS channel noninverting input. Connect to resolver COS HI output. COS = 2 V rms ± 10%.

PRELIMINARY DATA

Low Cost LVDT-to-Digital Converter

AD2S93

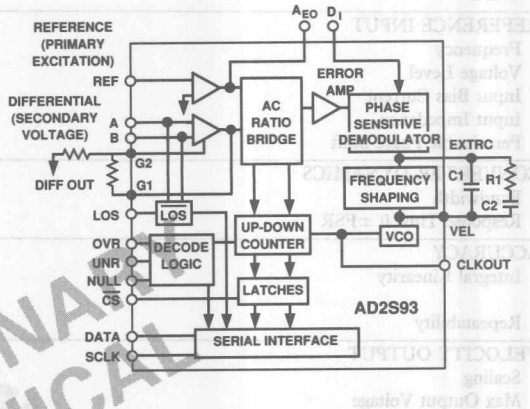
FEATURES

Full Function Monolithic LVDT-to-Digital Converter
Absolute Serial Data Output
Uncommitted Differential Input
14-Bits Repeatability
Loss of Signal Detection
14-Bit Resolution
Analog Velocity Output
Industrial Temperature Range
28-Pin PLCC
Low Power

APPLICATIONS

Industrial Gauging
Industrial Process Control
Linear Positioning Systems
Linear Actuator Control
Automotive Motion Sensing and Control
Factory Automation

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S93 is a complete 14-bit resolution tracking LVDT-to-digital converter.

A Type II servo loop is employed to track the A–B input and produce a digital output equal to (A–B)/REF, where REF is a fixed amplitude ac reference phase coherent with the A–B input. This allows the measurement of any 2-, 3-, 4- and 5-wire LVDTs or alternative amplitude modulated input. The bandwidth of the converter is set by the user externally between a range of 500 Hz–1000 Hz.

The AD2S93 has a 16-bit serial output. The MSB (LOS), read first, indicates loss of the A, B or reference inputs to the converter or transducer. The second and third MSBs are flags indicating whether $-(A-B) \leq -REF$ (UNR) or $A-B \leq +REF$ (OVR). The displacement data is presented as 13-bit offset binary giving a ±12 bits operating range. LOS, OVR and UNR are pinned out on the device. In addition, NULL is available; this flags when A – B = 0.

Absolute displacement information is accessed when $\overline{CS}$ is taken LO followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz. Data is read MSB first. When $\overline{CS}$ is high, the DATA output is high impedance; this allows daisy chaining of more than one converter onto a common bus.

The A, B differential input allows the user to scale the A, B input between 1 and 10. This enables the user to accurately set up the inputs matching the REF input to the DIFF output. The DIFF output is the resultant A–B.

An analog velocity output is provided which accurately indicates the input velocity of the input signals. The full-scale output is ±2.5 V dc equivalent to a maximum 130 Hz full stroke constant velocity displacement.

The AD2S93 operates on a ±5 V ±5% power supplies and is fabricated on Analog Devices' linear compatible CMOS process (LC^2CMOS). (LC^2CMOS) is a mixed technology process that combines precision bipolar circuits with low power logic.

PRODUCT HIGHLIGHTS

Complete LVDT-to-Digital Interface. The AD2S93 provides the complete solution for digitizing LVDT signals to 14-bit resolution.

Serial 16-Bit Output Data. One 16-bit read from the AD2S93 determines input signal continuity (LOS), over and underrange detection and 13 bits of offset binary displacement information.

High Accuracy Grade in Low Cost Package. 0.05% and 0.1% integral linearity over the full −40°C to 85°C operating temperature range.

Uncommitted Differential Input. Allows configuration of 2-, 3-, 4- and 5-wire LVDTs.

Multiple Converter Interfacing. High impedance data output and a simple three-wire interface, reduces cabling and eliminates bus contention.

Low Power. 50 mW power consumption.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S93—SPECIFICATIONS (V_{DD} = 5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, T_A = −40°C to +85°C unless otherwise stated)

Parameter	Min	Typ	Max	Units	Test Conditions
SIGNAL INPUTS					
Frequency	2		10	kHz	
Voltage Level	1.8	2.0	2.2	V rms	
Input Bias Current			500	nA	
Input Impedance	1.0			MΩ	
CMRR	60			dB	
REFERENCE INPUT					
Frequency	2		10	kHz	
Voltage Level	1.8	2.0	2.2	V rms	
Input Bias Current			500	nA	
Input Impedance	1.0			MΩ	
Permissible Phase Shift	−10		+10	Degrees	
CONVERTER DYNAMICS					
Bandwidth	500		1000	Hz	Set by User
Response Time 0 ±FSR			20	ms	
ACCURACY					
Integral Linearity			0.1	% FSD	AP
			0.05	% FSD	BP
Repeatability			±1	LSB	
VELOCITY OUTPUT					
Scaling		50		Hz/V dc	
Max Output Voltage	±2.375	±2.500	±2.625	V dc	
Reversion Error			±0.5	% FS	
Linearity			1.0	% FS	
Offset			±10	mV dc	
Load Drive Capability			±250	μA	
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage, V_{INH}	3.5			V dc	
Input Low Voltage, V_{INL}			1.5	V dc	
Input Current I_{IN}			10	μA	
Input Capacitance			10	pF	
LOGIC OUTPUTS OVR, UNR, LOS, NULL, DATA, A, B, CLKOUT					
Output High Voltage	4.0			V dc	
Output Low Voltage			1.0	V dc	
SERIAL CLOCK (SCLK)					
SCK Input Rate			2	MHz	

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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RECOMMENDED OPERATING CONDITIONS

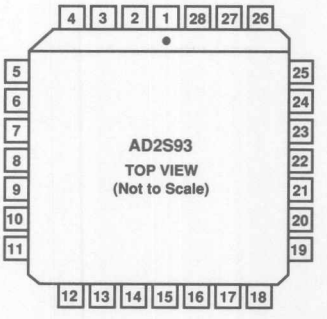
Power Supply Voltage (V_{DD} – V_{SS}) . . . . . ±5 V dc ±5%
Analog Input Voltage (A, B and REF) . . . . . 2 V rms ±10%
Signal and Reference Harmonic Distortion 10%
Phase Shift between Signal and Reference . . . . . ±10°
Ambient Operating Temperature Range
Industrial (AP, BP) . . . . . −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7.0 V dc
V_{SS} to AGND . . . . . +0.3 V to −7.0V dc
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V dc
Analog Inputs to AGND REF . . . V_{SS} −0.3 V to V_{DD} +0.3 V
A, B . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Analog Output to AGND VEL . . . . . V_{SS} to V_{DD}
Digital Inputs to DGND
$\overline{CS}$, SCLK . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
NULL, A, B, DIR,
CLKOUT, DATA . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (A, B) . . . . . −40°C to +85°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Power Dissipation to +75°C . . . . . 300 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed in "Absolute Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



Pin	Description
A, B	Uncommitted differential inputs for the A–B signal inputs.
REF	Single ended input for fixed amplitude reference.
DIFF OUT	Output of signal input preamplifier.
GAIN	Connect GAIN pin to DIFF OUT for nominal × 1. Gains greater than 1 can be resistively scaled. Do not leave unconnected.
DATA	16-bit serial data output. Thirteen bits of absolute position information + over- and under-range + LOS.
SCLK	Serial Clock. Maximum rate = 2 MHz.
$\overline{CS}$	Chip Select. Loads serial interface with current positional information. Enables output.
CLKOUT	Clocks a pulse every corresponding LSB increment. Mark space ratio indicates input velocity.
DIR	Indicates direction. DIR HI for positive displacement and LO for negative displacement.
NULL	Denotes null position.
LOS	Denotes A or B lines loss of connection and loss of reference to transducer or converter.
OVR, UNR	Two pins that denote whether the input signals are underrange, −ve posn, +ve posn or overrange.
VEL	Analog Velocity Output.
EXTRC	Determines system dynamics. Connect C and RC (serial) parallel combination across EXTRC and VEL to define loop dynamics.
AGND	Analog Ground.
DGND	Digital Ground.
AEO, DI	AC couple output of AC bridge with a capacitor placed between AEO and DI.
V_{SS}	Negative power supply −5.0 V dc ±5%.
V_{DD}	Positive power supply +5.0 V dc ±5%.

PRELIMINARY TECHNICAL DATA

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Principle of Operation

The AD2S93 is based on a Type 2 tracking loop. Three external passive components are required to set the dynamics of the loop. The input format is one fixed signal ac reference and an amplitude modulated reference; this is decoded into a ±12-bit serial offset binary output. The output word is complemented with the inclusion of input state detection and an additional loss of transducer or converter reference and loss of signal detection. The total word length is 16 bits (see Figure 1) with the MSB denoting the loss of an input and the second and third MSBs determining whether the transducer signal is either over- or underrange. (Over- and underrange refers to when the signal input to the converter exceeds the reference.)

Data Output Format

The operating range of the converter is 14 bits. This gives a bipolar resolution of 12 bits in both positive and negative directions, i.e., +4096 (positive) and −4096 (negative). The thirteenth bit is used to denote the sign of the data. An additional bit indicates the span limit or overrange of the transducer input. Overrange signifies that the A, B input is larger than the REF input. The addition of overrange increases the converter's resolution to 14 bits (12 bits underrange + 12 bits negative position + 12 bits positive position + 12 bits overrange). The underrange and overrange states are decoded prior to a read.

	DB0	DB1	DB2	DB3	DATA DB–D15
FUNCTION	LOS	UNR	OVR	SIGN	12 BITS OF DATA

WHERE UNR = UNDERRANGE AND OVR = OVERRANGE

Figure 1. Data Output Format

The null point of operation is denoted by half full-scale code, the NULL output produces a positive going as the count passes through zero.

Interfacing to the AD2S93

Accessing the serial interface is by a three-wire interface DATA, SCLK and $\overline{CS}$. The data is loaded into the serial interface from the internal counters when $\overline{CS}$ goes LO. SCLK can then be applied (a minimum of 600 ns after $\overline{CS}$ = LO) and the data retrieved from the DATA output pin, MSB first. The maximum clock rate is 2 MHz.

Built-in Diagnostics

The first three bits read from the serial interface preceding the data can be used to determine whether the data is valid or not. The 2nd and 3rd MSB tell the user whether the inputs to the converter are within the linear operating range of the converter, either overrange (positive) or underrange (negative). The MSB is a continuity flag, LOS, which will be HI if one of the following statements are true.

1. Either or both of the signal inputs, A and B, have become disconnected from the converter.
2. The reference has become disconnected from the converter.
3. The reference has become disconnected from the transducer.

PRELIMINARY TECHNICAL DATA



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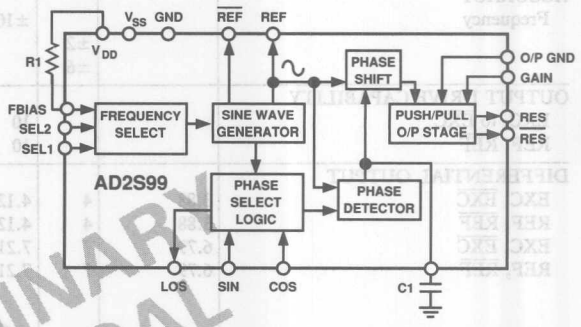
Low Cost Reference Oscillator

AD2S99

FEATURES
- Sine Wave Oscillator
- Two Phase-locked Sine Wave Outputs
- Programmable Output Frequency Range 2 kHz–20 kHz
- Programmable Output Amplitude
- Wide Power Supply Range
- "Loss-of-Signal" Indicator
- Small 20-Pin PLCC Package
- Low Cost

APPLICATIONS
- Primary Winding Excitation of
  - Resolvers
  - Synchros
  - LVDTs
  - RVDTs
  - Pressure Transducers
  - Load Cells
  - Inductosyns*
  - AC Bridges

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S99 is a programmable sine wave oscillator contained in a 20-pin PLCC package, with an operating temperature range of −40°C to +85°C.

The main use of the AD2S99 is to provide two signals. An excitation signal is provided for an ac transducer, also, a reference signal, phase locked to the transducer outputs, which can be used to demodulate the transducer outputs. The AD2S99 requires only two external components, one resistor and one capacitor.

The AD2S99 operates on resolver format SINE and COSINE signals. These are dynamically phase compensated by varying the transducer excitation, producing complete alignment between the SINE, COSINE and Reference signal.

Elimination of the temperature dependent phase shifts found with inductive transducers, and their resultant errors is therefore achieved.

The AD2S99 is manufactured on a LC^2MOS process which combines high density and low power CMOS logic with high accuracy bipolar linear circuitry.

PRODUCT HIGHLIGHTS

Dynamic Phase Compensation
The AD2S99 dynamically compensates for any phase variation in the transducer by phase locking the outputs of the transducer to the reference output of the AD2S99.

Programmable Frequency
The oscillator frequency is easily programmed to 2 kHz, 5 kHz, 10 kHz or 20 kHz by using the frequency select pins.

Programmable Output Amplitude
Pin programmable to 4 V rms or 7 V rms output amplitudes.

Loss of Signal Pin
The "LOS" output indicates a signal failure if both the sensor outputs feeding back to the AD2S99 are lost.

*Inductosyn is a registered trademark of Farrand, Industries, Inc.

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AD2S99—SPECIFICATIONS (T_A = −40°C to +85°C, V_S = ±15 V dc, R_1 = 345K [1%] unless otherwise specified)

Parameter	Min	Typ	Max	Units	Conditions
ANALOG INPUTS SIN, COS[1]					
Maximum Amplitude	0.7		2.2	V rms	
FREQUENCY OUTPUT RANGE					SEL1 SEL2
	1800	2000	2200	Hz	0 0
	4500	5000	5500	Hz	0 1
	9000	10000	11000	Hz	1 0
	18000	20000	22000	Hz	1 1
ACCURACY					
Frequency			±10	%	V_S = ±4.75 to ±15.75 V @ −40°C to +85°C
		±2		%	V_S = ±15 V @ +25°C
		±6		%	V_S = ±15 V @ −40°C to +85°C
OUTPUT DRIVE CAPABILITY					
EXC, to $\overline{EXC}$			10	mA rms	Max Capacitive Load (C_L) = 30 pF
REF, $\overline{REF}$			10	mA rms	Max Capacitive Load (C_L) = 30 pF
DIFFERENTIAL OUTPUT					
EXC, $\overline{EXC}$	3.88	4	4.12	V rms	GAIN = 0; R_{LOAD} = 200 Ω to GND
REF, $\overline{REF}$	3.88	4	4.12	V rms	
EXC, $\overline{EXC}$	6.79	7	7.21	V rms	GAIN = 1; R_{LOAD} = 350 Ω to GND
REF, $\overline{REF}$	6.79	7	7.21	V rms	7 V rms Obtained Only @ $V_S \geq \pm 8$ V (Single Ended Output Gives Half the Voltage Range)
PHASE SENSITIVE DETECTOR					
Phase Range	0		180	Degrees	
Detector Threshold	0.4	0.5	0.6	V rms	
PHASE CONTROL RANGE					
SIN Input to REF Output	1°		180°		
HARMONIC DISTORTION					
REF, $\overline{REF}$, EXC, $\overline{EXC}$		−30		dB	
POWER DISSIPATION		100		mW	
POWER SUPPLIES					
V_{DD}	+4.75		+15.75	V	
V_{SS}	−4.75		−15.75	V	
Quiescent Current		4		mA	
TEMPERATURE RANGE	−40		+85	°C	Operating
	−65		+150	°C	Storage
POWER SUPPLY REJECTION RATIO					V_{SS}/V_{DD} to REF, $\overline{REF}$ EXC, $\overline{EXC}$
SEL1, SEL2 INPUTS					
Input High Voltage (V_{INH})	AGND −0.4		AGND +0.4	V dc	Logic 1
Input Low Voltage (V_{INL})	V_{SS}−0.25		V_{SS}+0.4	V dc	Logic 0
GAIN INPUTS					
Input High Voltage (V_{INH})	V_{DD}−0.4		V_{DD}+0.25	V dc	Logic 1
Input Low Voltage (V_{INL})	V_{SS}−0.25		V_{SS}+0.4	V dc	Logic 0
LOS OUTPUT					
LOS Output High Voltage (V_{OH})	V_{DD}−0.4	V_{DD}	V_{DD}+0.25	V dc	Logic 1
LOS Output Low Voltage (V_{OL})	V_{SS}+0.4	V_{SS}	V_{SS}−0.4	V	Logic 0

NOTES

[1]Either SIN or COS input must not exceed input limits. Worst Case sinθ = cosθ where θ = 45°.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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RECOMMENDED OPERATING CONDITIONS

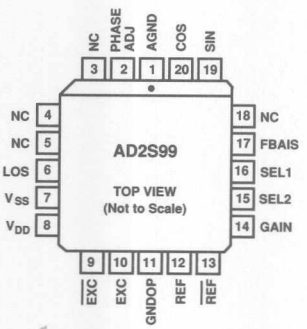
Power Supply Voltage (V_{DD} to V_{SS}) . . . ±4.75 V to ±15.75 V
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Frequency Select (SEL1 and SEL2) . . . . . V_{SS} to AGND
Operating Temperature Range . . . . . −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . 0 V to +16.5 V
V_{SS} . . . . . 0 V to −16.5 V
Operating Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Outputs (EXC, $\overline{EXC}$, REF, $\overline{REF}$ and LOS)
. . . . . V_{SS} −0.4 V to V_{DD} +0.4 V
Analog Input Voltages (SIN and COS) . . . . . ±5 V rms
Output Amplitude Control (GAIN)
. . . . . V_{SS} −0.4 V to V_{DD} +0.4 V
Frequency Select (SEL1, SEL2)
. . . . . V_{SS} −0.4 V to AGND +0.4 V

CAUTION:
*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Reversal of power supplies may damage the device.

PIN CONFIGURATION



NOTE:
THE AD2S99 WILL BE AVAILABLE IN A CERAMIC PACKAGE.

3

PRELIMINARY TECHNICAL DATA

PIN DESCRIPTION

1	AGND	Analog ground pin. Measure SIN and COS inputs with reference to AGND.
2	PHASE ADJ	Input with a voltage range of ±2 volts with respect to AGND. Phase shifts the EXC output relative to the REF output from 0 to 180 degrees.
3	NC	Not Connected.
4	NC	Not Connected.
5	NC	Not Connected.
6	LOS	LOS signal is a logic output which swings between V_{SS} and V_{DD}. Logic high when both SIN and COS signals are below the input detector threshold of 0.5 ± 0.1 volts.
7	V_{SS}	Negative power supply pin. −4.75 V to −15.75 V dc.
8	V_{DD}	Positive power supply pin. +4.75 V to +15.75 V dc.
9	$\overline{EXC}$	Complement of the signal found on the EXC pin.
10	EXC	Excitation output. Can drive 10 mA with a 30 pF capacative load, with an output voltage of 2 V or 3.5 V rms.
11	GNDOP	Ground pin for reference outputs EXC, $\overline{EXC}$, REF, and $\overline{REF}$. Internally connected to AGND.
12	REF	Converter reference output sine wave can drive 10 mA with a 30 pF load, with an amplitude of 2 V or 3.5 V rms.
13	$\overline{REF}$	Complement of the signal found on REF pin.
14	GAIN	Controls the output voltages of EXC, $\overline{EXC}$, REF, $\overline{REF}$.
15	SEL2	Selects output frequency. Connect to GND or V_{SS}.
16	SEL1	Selects output frequency. Connect to GND or V_{SS}.
17	FBIAS	Connect to V_{DD} via resistor to trim oscillator frequency.
18	NC	Not Connected.
19	SIN	Input for the SIN signal from the transducer.
20	COS	Input for the COS signal from the transducer.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN CONFIGURATION

NOTE:
THE ADS99 WILL BE AVAILABLE IN SOIC/HMC PACKAGE.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD} to V_{SS}) . . . . . ±4.75 V to ±15.75 V
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ± 10%
Frequency Select (SEL1 and SEL2) . . . . . V_{SS} to AGND
Operating Temperature Range . . . . . −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . 0 V to +16.5 V
V_{SS} . . . . . 0 V to −16.5 V
Operating Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Outputs (EXC, $\overline{EXC}$, REF, $\overline{REF}$ and LOS)
. . . . . V_{SS} −0.4 V to V_{DD} +0.4 V
Analog Input Voltage (SIN and COS) . . . . . ±5 V rms
Output Amplitude Control (GAIN)
. . . . . V_{SS} −0.4 V to V_{DD} +0.4 V
Frequency Select (SEL1, SEL2)
. . . . . V_{SS} −0.4 V to AGND +0.4 V

CAUTION.
*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Reversal of power supplies may damage the device.

PIN DESCRIPTION

1	AGND	Analog ground pin. Monitors SIN and COS inputs with reference to AGND.
2	PHASE ADJ	Input with a voltage range of ±2 volts with respect to AGND. Phase shifts the EXC output relative to the REF output from 0 to 180 degrees.
3	NC	Not Connected.
4	NC	Not Connected.
5	NC	Not Connected.
6	LOS	LOS signal is a logic output which swings between V_{SS} and V_{DD}. Logic high when both SIN and COS signals are below the input detector threshold of 0.5 ± 0.1 volts.
7	V_{SS}	Negative power supply pin. −4.75 V to −15.75 V dc.
8	V_{DD}	Positive power supply pin. +4.75 V to +15.75 V dc.
9	$\overline{EXC}$	Complement of the signal found on the EXC pin.
10	EXC	Excitation output. Can drive 10 mA with a 30 pF capacitive load, with an output voltage of 2 V or 3.5 V rms.
11	GNDOP	Ground pin for reference outputs EXC, $\overline{EXC}$, REF, and $\overline{REF}$. Internally connected to AGND.
12	REF	Converter reference output sine wave can drive 10 mA with a 30 pF load, with an amplitude of 2 V or 3.5 V rms.
13	$\overline{REF}$	Complement of the signal found on REF pin.
14	GAIN	Controls the output voltages of EXC, $\overline{EXC}$, REF, $\overline{REF}$.
15	SEL2	Selects output frequency. Connect to GND or V_{SS}.
16	SEL1	Selects output frequency. Connect to GND or V_{SS}.
17	FBIAS	Connect to V_{DD} via resistor to trim oscillator frequency.
18	NC	Not Connected.
19	SIN	Input for the SIN signal from the transducer.
20	COS	Input for the COS signal from the transducer.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

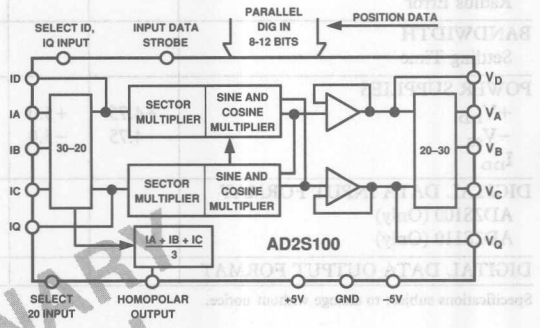
AC Vector Controllers

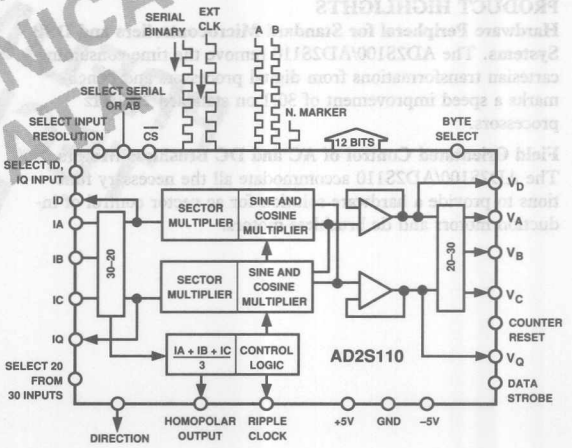
AD2S100/AD2S110

FEATURES
- Complete Clarke and Park Transformations
- Real-Time Computation
- Homopolar Output
- 8- to 12-Bit Digital Interface

APPLICATIONS
- AC Vector Control
- AC Induction and DC Permanent Magnet Motors
- HVAC, Pump, Fan Control
  - Material Handling
  - Robotics
  - Spindle Drives
  - Gyroscopes
- Stabilization Platforms
- Three Phase Power Measurement

FUNCTIONAL BLOCK DIAGRAMS





PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S100 performs the vector rotation of two 90 degree orthogonal ac signals and rotates them into a reference frame related to the update frequency of the digital input port.

Two transforms are included in this single silicon system. The first is the Clarke transform which converts three phase 120 degree signals into their two phase 90 degree equivalents. These signals represent real and imaginary currents which can be computed to give the vector current magnitude.

The Park transform rotates these currents at the update speed of the applied digital input. This digital input is normally provided from a resolver-to-digital converter, or in the case of the AD2S110 an optical encoder position sensor.

If the input current signals are represented by I_{DS} and I_{QS}, respectively, the transformation can be mathematically described as follows:

$$I_{DS}' = I_{DS}\ Cos\ \theta - I_{QS}\ Sin\ \theta$$

$$I_{QS}' = I_{DS}\ Sin\ \theta + I_{QS}\ Cos\ \theta$$

Where I_{DS}' and I_{QS}' are the output of the Park transform and Sin θ and Cos θ the trigonometric values of the input rotor position.

The input section of the device can be configured to accept either three phase inputs, two phase inputs of a three phase system, or two 90 degree separated input signals. A three phase input selection is the only input type which will record the correct homopolar output. This output identifies the situation where an imbalance between the three phase currents exists. In normal conditions this output will normally be zero.

The digital input section will accept a variable resolution from 8 to 12 bits (AD2S100). An input data strobe signal is required to freeze the position data and load this information into the device counters.

Two analog output formats are available. A two phase rotated output facilitates concatenation where a derotation is required. The other output provides three phase signals which can be used as an input to a dc, or, ac motor controller.

The AD2S100 optical encoder version provides the functions above with the addition of a parallel digital port which can be used to extract real-time absolute position data. The AD2S100/AD2S110 are fabricated on LC^2MOS and operate on ±5 volt power supplies.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD2S100/AD2S110—SPECIFICATIONS (typical at +25°C unless otherwise stated)

Parameter	Min	Typ	Max	Units	Conditions
ANALOG INPUTS					
Voltage Level	0		±5	V dc	
ANALOG OUTPUTS					
Output Voltage Offset			3	mV dc	
ANGULAR ERROR	0		±30	arc min	
Radius Error			0.2	%	
BANDWIDTH			150	Hz	
Settling Time			2	μs	0°C–180°C Step
POWER SUPPLIES					
$+V_{DD}$	+4.75	+5.0	+5.25	V dc	
$-V_{SS}$	−4.75	−5.0	−5.25	V dc	
I_{DD}			8	mA	
DIGITAL DATA INPUT FORMAT					
AD2S100 (Only)					10- or 12-Bit Absolute Parallel Binary
AD2S110 (Only)					12-Bit Absolute Serial or 1000 Line A Quad B
DIGITAL DATA OUTPUT FORMAT					12-Bit Absolute Parallel Binary

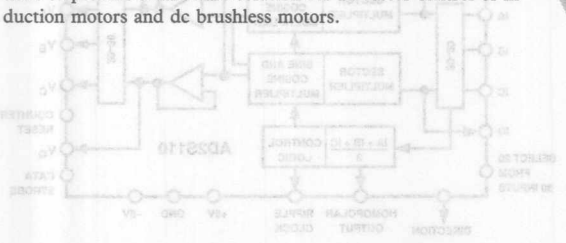
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

Hardware Peripheral for Standard Microcontrollers and DSP Systems. The AD2S100/AD2S110 remove the time consuming cartesian transformations from digital processors and benchmarks a speed improvement of 30:1 on standard 20 MHz processors.

Field Orientated Control of AC and DC Brushless Motors. The AD2S100/AD2S110 accommodate all the necessary functions to provide a hardware solution for ac vector control of induction motors and dc brushless motors.



Three Phase Peak Current Measurement. The AD2S100/AD2S110 calculates the peak time current and can be used to sense overcurrent situations, or, imbalances in a three phase system via the homopolar output.

Resolver or Optical Encoder Interface. The AD2S100/AD2S110 provide these general purpose interfaces which will allow direct application of these circuits without changing the rotor position sensor.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

High Power Output, Hybrid Digital-to-Synchro/Resolver Converters

DRC1745/DRC1746

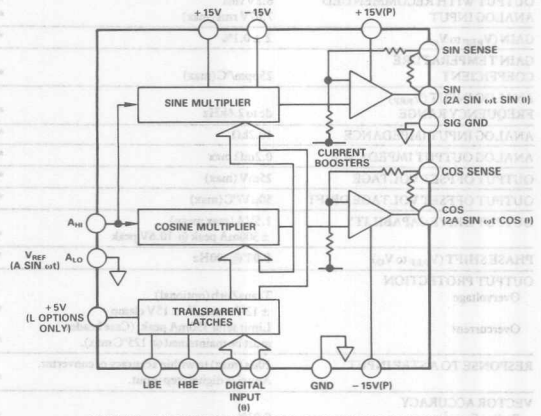
FEATURES

- 14- or 16-Bit Resolution
- 2 or 4 Arc-Minutes Accuracy
- 2VA max Mean Output Drive Capability
- Full Accuracy for dc to 2.6kHz Reference
- Full Accuracy with dc or Pulsating Power Supplies (PPS)
- Guaranteed Operation With 3V dc Pedestal on PPS
- Can Drive Pure Inductive, Resistive or Highly Capacitive Loads
- LS or CMOS Latched Inputs With Separate High/Low Byte Enable
- Low Radius Vector Variation (0.03%)
- Optional TransZorb™ Protection Against Inductive Spikes on Output
- Protected Against +200% Overvoltage on Analog Input
- Remote Output Sensing Facility
- No Trims or External Adjustments
- Full Output Short Circuit Protection
- Single 40-Pin Package
- Hi Rel, MIL-STD 883B Versions Available

APPLICATIONS

- Driving Synchro and Resolver Control Transformers
- Avionic Equipment (e.g., Air Data Computers)
- Interfacing With Servo Systems
- Fire Control System Outputs
- Naval Retransmission Unit Outputs
- Outputs to Radars and Navigational Aids
- Aircraft and Naval Simulators

FUNCTIONAL BLOCK DIAGRAM



NOTE: "A_{LO}", "GND", AND "SIG GND" ARE INTERNALLY CONNECTED IN STAR POINT.

GENERAL DESCRIPTION

The DRC1745 and DRC1746 are hybrid packaged Digital-to-Resolver converters. They accept a 14-bit or 16-bit digital input word representing angle and output sine and cosine voltages multiplied by an analog input. The converters maintain full accuracy when the analog input frequency is in the range dc to 2.6kHz.

The units have internal power amplifiers capable of driving a 2VA load which can be pure inductive, resistive or highly capacitive. The output is fully short-circuit protected against overcurrent. The output of the converter can be used to drive directly into resolver control transformers or in conjunction with an external transformer module to drive synchro control transformers. The power available is more than adequate to drive all standard synchro control transformers.

The separately powered output stage is compatible with conventional ±15V dc power supplies or pulsating power supplies with pedestal components as low as 3V dc.

TransZorb is a registered trademark of General Semiconductor Industries, Inc.

The use of pulsating power supplies greatly reduces the internal power dissipation in the hybrid package which in turn maximizes the converter's Mean Time Between Failures (MTBF).

A particular feature of the converters is that they have a remote sensing facility which means that output accuracy can be maintained even when long lines have to be driven.

The converter's data inputs are latched and the latches can be CMOS or Low Power Schottky (LS). The former gives advantages in terms of power dissipation and the latter in terms of glitch performance when used in fast dynamic update modes. The latches are transparent and have a separate high and low byte enable.

As an option, the output stage can be fitted with internal TransZorb™ protection. This gives full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. This condition can occur at switch off or as a consequence of external power supply fault conditions.

The units are packaged in 40-pin dual in line hybrid packages and require no external trims or adjustments.

MODELS AVAILABLE

The DRC1745 (14-bit resolution) and DRC1746 (16-bit resolution) are available with accuracies of ±2 or ±4 arc-minutes. Both units have optional TransZorb protection and a choice of either LS or CMOS inputs (see Ordering Information).

Two sets of reference and output transformers are available. The STM1660/STM1663 operates over 47Hz to 440Hz while the STM1680/STM1683 operates over 360Hz to 2.6kHz. The transformers can be Scott T connected to provide a synchro output format.

DRC1745/DRC1746—SPECIFICATIONS (typical @ +25°C and ±15V power supplies, unless otherwise noted)

Models	DRC1745	DRC1746
DIGITAL INPUT RESOLUTION	14 Bits (1.32 arc-minutes)	16 Bits (0.33 arc-minutes)
DIGITAL INPUT FORMAT	Parallel natural binary, TTL compatible. Includes internal 27kΩ pull-up resistors.	*
RECOMMENDED ANALOG INPUT (V_{REF})[1]	3.4V rms (single ended input) 3.53V rms (max)	*
OUTPUT WITH RECOMMENDED ANALOG INPUT	6.8V rms 7.07V rms (max)	* *
GAIN (V_{REF} to V_O)	2 ± 0.1%	*
GAIN TEMPERATURE COEFFICIENT	25ppm/°C (max)	*
ANALOG INPUT (V_{REF}) FREQUENCY RANGE	dc to 2.6kHz	*
ANALOG INPUT IMPEDANCE	10.2kΩ	*
ANALOG OUTPUT IMPEDANCE	0.2mΩ max	*
OUTPUT OFFSET VOLTAGE	25mV (max)	*
OUTPUT OFFSET VOLTAGE DRIFT	50µV/°C (max)	*
OUTPUT DRIVE CAPABILITY	1.5VA (max mean) ± 300mA peak @ 10.6V peak	*
PHASE SHIFT (V_{REF} to V_O)	0.08°@400Hz	*
OUTPUT PROTECTION		
Overvoltage	TransZorb (optional) ± 12V standoff, ± 15V clamp	*
Overcurrent	Limit set@ 550mA peak. (Case header must be maintained @ 125°C max).	*
RESPONSE TO A STEP INPUT	20µs (max) to within accuracy of converter. Any size digital step input.	*
VECTOR ACCURACY		
Radius Error[2]	0.03%	*
Angular Error	± 2 or ± 4 arc-minutes	*
POWER SUPPLY (NO LOAD)[3,4,5]		
LS Latch Options + 15 Volts	15mA (typ) 22mA (max)	*
− 15 Volts	15mA (typ) 22mA (max)	*
+ 15(P) Volts	20mA (typ) 34mA (max)	*
− 15(P) Volts	20mA (typ) 34mA (max)	*
+ 5 Volts	44mA (typ) 72mA (max)	*
CMOS Latch Options + 15 Volts	24mA (typ) 30mA (max)	*
− 15 Volts	15mA (typ) 22mA (max)	*
+ 15(P) Volts	20mA (typ) 34mA (max)	*
− 15(P) Volts	20mA (typ) 34mA (max)	*
Additional Current (Load Dependent) + 15(P) Volts	400mA Peak (max)	*
− 15(P) Volts	400mA Peak (max)	*
PULSATING POWER SUPPLY PEDESTAL	3V dc (min)	*
POWER DISSIPATION	See Power Dissipation section of this data sheet.	*
CASE TEMPERATURE RANGE[6]	− 55°C to + 125°C Operating − 65°C to + 150°C Storage	* *
SIZE	40-Pin DIL 1.14 × 2.14 × 0.18" (29.0 × 54.4 × 4.6mm)	* *
WEIGHT	0.9 oz (25 grams)	*

Model	Reference Input Transformer STM1680	Output Transformer STM1683
INPUT VOLTAGE	11.8, 26, 115V rms depending on option R_{HI}, R_{LO}	6.8V rms Sin, Cos
OUTPUT VOLTAGES	3.4V rms ± 1% A_{HI}, A_{LO}	11.8, 26, 90V rms ± 5% S1, S2, S3, (S4)
OUTPUT FORMAT	N/A	Synchro or resolver depending on option
FREQUENCY RANGE		
STM1680	360Hz–2.6kHz	
STM1683		360Hz–2.6kHz
INPUT IMPEDANCE		
11.8V Input	50kΩ(min)	N/A
26V Input	30kΩ(min)	N/A
115V Input	800kΩ(min)	N/A
ACCURACY		
0.1VA Load	N/A	± 1.0 arc-min (max)
1.4VA Load	N/A	± 2.0 arc-min (max)
2.0VA Load	N/A	± 3.0 arc-min (max)
Temperature Coefficient	N/A	± 0.02 arc-min/°C (max)
OUTPUT IMPEDANCE		
11.8 V Output	N/A	2.9Ω (typ)
26V Output	N/A	13.6Ω (typ)
90V Output	N/A	156Ω (typ)
DC ISOLATION		
Voltage	1000V	1000V
SIZE		
STM1680	1.12 × 1.12 × 0.4" (28.5 × 28.5 × 10.2mm)	
STM1683		2.25 × 1.12 × 0.4" (57.1 × 28.5 × 10.2mm)
TEMPERATURE RANGE		
Operating	− 55°C to + 125°C	− 55°C to + 125°C
Storage	− 60°C to + 150°C	− 60°C to + 150°C
WEIGHT (max)		
STM1680	1.5 oz (42 grams)	
STM1683		2.5 oz (70 grams)

N/A means not applicable.

NOTES
[1]V_{REF} is internally clamped to ± 15V power supplies. Input current should not exceed 10mA.
[2]Worst case error over operating temperature range.
[3]The +5 volt power supply must never go more than 0.3V below GND potential.
[4]Correct polarity voltages must be maintained on the ± 15V and the ± 15V(P) pins.
[5]Tracking of the ± 15V and ± 15(P) supplies must be maintained.
[6]Adequate heat sinking must be provided to keep the case temperature less than 125°C.
*Specifications same as DRC1745.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS

+15V to GND	+17V
−15V to GND	−17V
+5V to GND	+5.5V, −0.3V
+15(P) to −15(P)	+40V
Digital Inputs GND	+5.5V, −0.3V

THEORY OF OPERATION

The operation of the DRC1745 and DRC1746 is illustrated in the block diagram shown in Figure 1.

The reference voltage, V_{REF}, (A sin ωt) is multiplied by both Sin θ and Cos θ where θ is the digital angle. The resultant outputs then pass through the current booster output stage to provide the resolver format output voltages viz:

$2A \sin \omega t \sin \theta$ (Sine output)
and $2A \sin \omega t \cos \theta$ (Cos output)

(Note: Converter has a gain of 2 from input to output.)

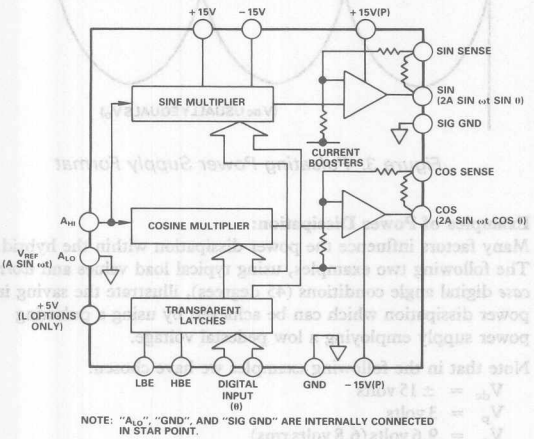


Figure 1. Theory of Operation

CONNECTING THE CONVERTER

The connections to the DRC1745 and DRC1746 are very straightforward.

The digital inputs should be connected to the converter using pins 1 (MSB) through 14 (LSB) in the case of the DRC1745 and through 16 (LSB) in the case of the DRC1746. The format of the digital angular input is shown under the "Bit Weight Table" section on this page.

The digital input control lines should be connected as described under the "Digital Data Input" section.

A_{LO} and A_{HI} are for the analog input reference voltage (V_{REF}). It should be noted that this is a single ended input where A_{LO} is grounded internally. If it is desired, the V_{REF} input can be externally isolated using the STM1680 or STM1660 transformer. See the section on "Output and Reference Transformers".

The converters have separate power supply inputs for the output amplifier stage (+15V(P) and −15V(P)) and for the remainder of the converter (+15V and −15V). When dc power supplies are used for the output stage, the supplies may be linked. However, when pulsating power supplies are used for the output stage, a separate dc supply must be provided for the +15V and −15V requirement. The converters have internal capacitive decoupling of 47nF on both power stage and converter supply but it is recommended that 6.8μF capacitors are taken from the +15V and −15V pin to "GND".

The "Case" pin is joined to the case which is isolated and should be connected to a convenient zero potential point in the system.

The sine and cosine outputs are taken from the "Sin" and "Cos" pins with "SIG GND" as the common connection.

The remote sense facility using "Cos Sense" and "Sin Sense" connections should be used as described under the "Remote Output Sensing" heading. If not used, the sense outputs should be connected to the corresponding Sin and Cos outputs.

DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches will be CMOS (type 54C373) or low power Schottky (LS)(type 54LS373) depending on the option.

The "HBE" input controls the input of the most significant 8 bits and the "LBE" input controls the input of the least significant bits (6 in the case of the DRC1745 and 8 in the case of the DRC1746).

A logic "Hi" on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital input. When "HBE" and "LBE" are taken to a logic "Lo" state, the converter output will be latched at the level of the data present on the input at the low going edge and remains constant until "HBE" and "LBE" are taken to a "Hi" state again. If the latches are not required, "HBE" and "LBE" can be left open circuit. The timing diagram in Figure 2 illustrates the use of "HBE" and "LBE".

Internal resistive pull-ups (to +5V using 27k resistors) are employed on all digital inputs. This ensures full TTL compatibility for either latch option even when sourcing 50μA of leakage current into each external digital driver.

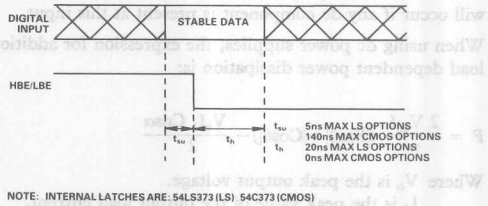


Figure 2. Data Transfer Diagram

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB DRC1745)	0.0220
15	0.0110
16 (LSB DRC1746)	0.0055

The DRC1745 and the DRC1746 can be used with conventional dc power supplies or a pulsating power supply on the output stage (see Figure 3). The latter gives significant reductions in power dissipation within the hybrid package without any attendant loss of accuracy.

When using a pulsating power supply, full advantage can be taken of the special design which allows the power supply to have a very low dc pedestal voltage. This results in minimized power dissipation. The pedestal voltage can in fact be as low as 3 volts. The combined pedestal plus peak supply voltage must not exceed the absolute maximum rating.

Full accuracy is retained during operation on pulsating power supplies because the output stage employing these supplies is only used to provide current gain. Overall operational loop gain is independently powered. There are no special switch-on/switch-off power supply sequencing requirements, and full internal protection is provided.

The section below demonstrates the power dissipation differences for different load conditions when using dc supplies and pulsating power supplies.

DC Power Supplies:
With inductive loads, the dc resistance is low compared with ac impedance; therefore care should be taken to ensure that no dc offset occurs at the sin and cos outputs. Note that under external current limit conditions asymmetry of the power supplies could occur, forcing a large dc offset to be present at the sin and cos outputs causing heavy power dissipation in the device. Case temperature must be maintained below 125°C.

As the reference input, A_{HI}, is directly coupled, output offset will occur if any dc component is present at this input.

When using dc power supplies, the expression for additional load dependent power dissipation is:

$$P = \frac{2\,V_{dc}I_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) - \frac{V_o I_1\,\mathrm{Cos}\alpha}{2} \qquad (1)$$

Where V_o is the peak output voltage.
I_1 is the peak value of the output load current.
θ is the digital angle.
α is the load phase angle.
V_{dc} is the dc power supply voltage (usually ±15 volts).

Pulsating Power Supplies:
When using a pulsating power supply, the expression for additional load dependent power dissipation within the hybrid is:

$$P = \frac{2\,V_p I_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) + \frac{V_{ac}I_1}{\pi}\,(\mathrm{Sin}\alpha - \alpha\mathrm{Cos}\alpha) \qquad (2)$$

Where V_{ac} is the peak ac component of the pulsating power supply assumed equal to the peak output voltage, V_o.
I_1 is the peak value of the output load current.
θ is the digital angle.
α is the load phase angle.
V_p is the dc pedestal voltage of the pulsating power supply.

Note that $I_1 = \frac{V_o}{|Z|}$ where V_o = Peak output voltage
$= 2 \times V_{REF}$
$|Z|$ = output load

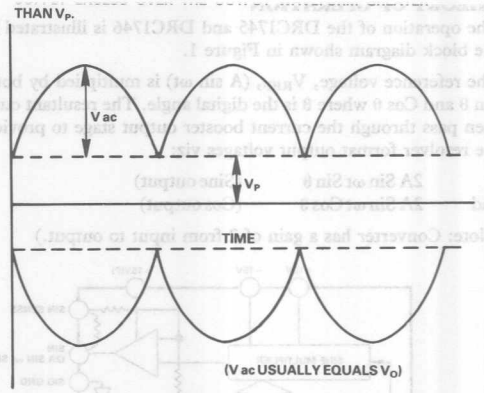


Figure 3. Pulsating Power Supply Format

Examples of Power Dissipation:
Many factors influence the power dissipation within the hybrid. The following two examples, using typical load values and *worst case* digital angle conditions (45 degrees), illustrate the saving in power dissipation which can be achieved by using a pulsating power supply employing a low pedestal voltage.

Note that in the following examples we have chosen:
V_{dc} = ±15 volts
V_p = 3 volts
V_o = 9.6 volts (6.8 volts rms)
V_{ac} = 9.6 volts (should be chosen to equal V_o)
I_1 = 292mA (equivalent to a 1.4VA mean load)

1) DC power supply, $\theta = 45°$ resistive load.

$$P = \frac{2 \times 15 \times 0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} - \frac{9.6 \times 0.292 \times 1}{2}$$
$$= 3.943 - 1.402$$
$$= \underline{2.54\ \text{Watts}}$$

2) As example (1) but with a 3 volt pedestal pulsating power supply.

From equation (2):

$$P = \frac{2 \times 3 \times 0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} + \frac{9.6 \times 0.292 \times 0}{\pi}$$
$$= \underline{0.79\ \text{Watts}}$$

Thus the pulsating power supply has cut down the internal dissipation by 1.75 watts, a ratio of 3.2:1.

A similar calculation using an inductive load shows a reduction from 3.94 Watts, using a dc power supply, to 1.68 Watts, when a 3 volt pedestal pulsating power supply is used. Thus the pulsating power supply has cut down the internal dissipation by 2.26 Watts, a ratio of 2.3:1.

The graph shown in Figure 4 shows the temperature at the hottest part of the base of the hybrid (in the middle of the base between "+15V(P)" and the opposite "N/C" pin) for resistive loads up to 2VA using dc supplies and pulsating supplies with pedestals of 3 volts and 5 volts.

Figure 5 shows a similar graph for inductive loads up to 1VA.

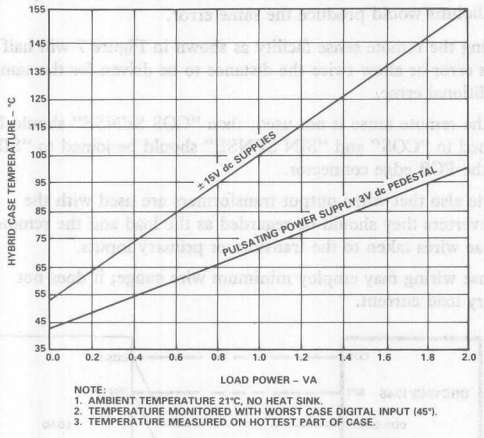


Figure 4. Case Temperature for Resistive Loads

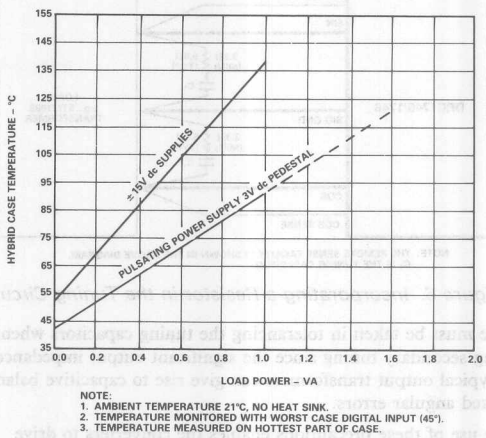


Figure 5. Case Temperature for Inductive Loads

As can be seen from Figures 4 and 5, it will be necessary to provide heat sinking when driving significant loads in order to keep the temperature of the case below its 125°C maximum.

The converters have been designed with a flat metal base to facilitate mounting on heat sinking materials. Special thermal management, utilizing direct eutectic bonding, has been employed in the output stage to minimize thermal resistance to:

Angle

0°, 90° θJunction/case = less than 12°C/watt
45°, 135° θJunction/case = less than 6°C/watt

Consequently the internal junction temperatures do not exceed case header temperature by more than 20°C when using pulsating power (even under worst case pure inductive load conditions. The maximum permitted junction temperature is 155°C).

CALCULATING THE LOAD

The following describes how to calculate the load.

In the case of synchro control transformers, first determine the value of Z_{so}. This impedance is normally quoted by the synchro manufacturer.

The load presented by the control transformer will be:

$$\frac{3}{4} \times \frac{V^2}{|Z_{so}|}$$

where V^2 is the rms signal input voltage.

When the STM1683 output transformer pair is used, it is necessary to add 0.25VA to the calculated figure to allow for transformer magnetizing current. For the STM1663 output transformer a figure of 0.30VA should be added.

For example, assume that a 90V rms signal, 400Hz synchro control transformer is to be driven by the DRC1745 in conjunction with the STM1683/412 output transformer pair. (The STM1683/412 boosts the 6.8V rms signal from the DRC1745 to the 90V rms required by the control transformer.)

Z_{so} for the control transformer is quoted as:

$700 + j4900$

Therefore

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

Therefore, the load presented by the control transformer is:

$$\frac{90^2}{4950} \times \frac{3}{4} = 1.23\text{VA}$$

Adding to this value 0.25VA for the STM1683 gives a figure of 1.48VA total.

In the case of a resolver control transformer the same exercise must be performed but it is not necessary to multiply by 3/4. Some resolver manufacturers quote rms input current and in this case the load will be the product of the input current and the rms voltage used to drive it. The 0.25VA must be added if the STM1683 transformer pair is used.

DRIVING CAPACITIVE LOADS

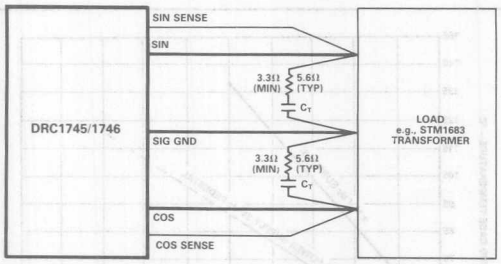
Synchros and resolvers often employ capacitive tuning to minimize power dissipation. This tuning can be on the load itself or (preferably for best accuracy) on the primary of the transformer driving the load. Full tuning modifies the load to appear resistive at the reference frequency, but it appears progressively more capacitive at all frequencies above.

Since the converter is an active negative feedback device, it is essential to include a low value resistor in series with each tuning capacitor to prevent highly dissipative output stage oscillation. This resistor must not be less than 3.3Ω. A value of 5.6Ω is recommended when referred to the output of the DRC1745/DRC1746.

The DRC1745 and DRC1746 can readily drive capacitive inputs up to 100nF at the converter output terminals without special precautions. However, please consult the factory when extreme lengths of screened cable or any other cases of high capacitance are to be driven. For example in the case of step-up transformers where the effective capacitance to be driven is:

$$C_{eff} = n^2 C_L$$

Where C_L is the capacitive load.



NOTE: THE REMOTE SENSE FACILITY IS SHOWN IN THE ABOVE DIAGRAM. C_T IS THE TUNING CAPACITOR.

Figure 6. Incorporating a Resistor in the Tuning Circuit

Care must be taken in tolerancing the tuning capacitors when using secondary tuning since the significant output impedance of typical output transformers can give rise to capacitive balance related angular errors.

The use of these precautions enables the converters to drive fully tuned 2VA loads.

For more information please send for relevant application note.

SHORT CIRCUIT PROTECTION

The short circuit current limit is set at <600mA maximum.

Under short circuit or excessive current conditions, the overcurrent protection circuit will trip and reduce the output current to zero. In order to minimize power dissipated under current limit conditions the device goes into a switching mode, testing the load condition at a high frequency.

When the overload conditions are removed, the output is automatically restored to its normal condition.

VECTOR ERRORS AND EFFECTS

The error law used in the converter has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the thin-film resistor networks used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays, or metal cutting control where perfect circles have to be generated.

BANDWIDTH

The open loop gain bandwidth product of the DRC1745 and DRC1746 has been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6kHz. This results in a closed loop bandwidth of 300kHz.

REMOTE SENSE FACILITY AND ADDITIONAL OUTPUT ERRORS

A remote sense facility is included in the DRC1745 and DRC1746 in order to reduce errors caused by the output interconnection wiring when driving large loads. The magnitude of this error is illustrated by two examples below.

Assume that the sine and cosine load impedances are perfectly matched and the sine output wiring resistance matches the cosine output wiring resistance to within 5%. Then for a resistive load of 1.4VA (33 ohms) and the worst case angle of 45 degrees, there will be 1.3 arc-minutes of extra error introduced for every 250 milliohms of resistance for the loop wiring between the converter and the load. (AWG22 = 17mΩ/ft, 1 oz PCB copper = 400mΩ/ft.)

In the case of an inductive load under similar conditions, 500 milliohms would produce the same error.

Using the remote sense facility as shown in Figure 7 will half this error or allow twice the distance to be driven for the same additional error.

If the remote sense is not used, then "COS SENSE" should be joined to "COS" and "SIN SENSE" should be joined to "SIN" at the PCB edge connector.

Note also that when output transformers are used with the converters they should be regarded as the load and the remote sense wires taken to the transformer primary inputs.

Sense wiring may employ minimum wire gauge; it does not carry load current.

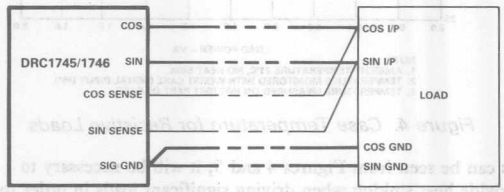


Figure 7. Using the Remote Sense Facility

The ground returns from the load should be individually wired and star-point connected at the converter's signal ground. Any common resistance in the signal returns will produce errors due to the summation of the sin and cos outputs. With a resistive load of 33 ohms at 1.4VA, and at the worst angles of 0 and 90°, there will be 1.3 arc-minutes of extra error introduced for every 12.5 milliohms of common signal return resistance.

TRANSZORB™ OUTPUT PROTECTION

As an option, the output stages of the converter can be internally fitted with TransZorb protection. This form of protection can be advantageous and significantly increase the Mean Time Between Failures when driving inductive loads. The TransZorbs, which are effectively back to back zener diodes, give full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. Such a change can occur at switch off or as a consequence of external power supply fault conditions. The TransZorbs are rated to give protection against worst case transients corresponding to an instantaneous interruption of the converter when driving into a full 2VA pure inductive load with the converter operating at the maximum case temperature of 125°C.

Figure 8 shows a simplified diagram of the converter output stage indicating the action of the TransZorb when the 15 volt supply is interrupted.

It is important to appreciate that destructively high voltages can be generated (given by E = Ldi/dt) even for modest inductive loading, under many fault conditions, since di/dt is effectively uncontrolled. Internal TransZorb protection is a better and more direct solution to the problem than employing a pair of reverse biased diodes to the output stage power supplies. This is because the transient is contained within the specific load disturbed and does not escape into the power supply wiring and hence cause possible damage to other equipments and devices. A domino effect of catastrophic failure is therefore prevented.

TransZorb is a registered trademark of General Semiconductor Industries, Inc.

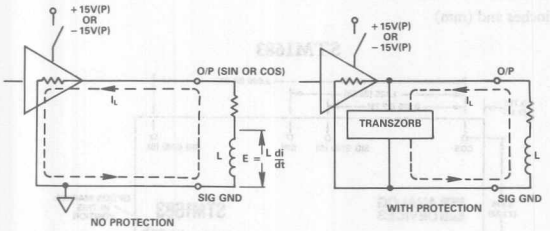


Figure 8. DRC1745/DRC1746 Output Stage Showing TransZorb Protection

Figure 9 shows the nature of transient waveforms where by the very large transient voltage generated by the inductive load is limited to a safe clamp level when it is applied to the output stage.

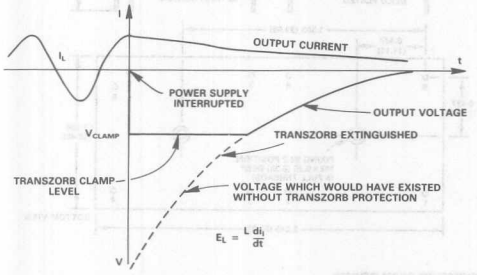


Figure 9. Transient Waveforms and TransZorb Clamping

In addition, there are conventional diode clamps on the ±15V(P) power supplies.

OUTPUT AND REFERENCE TRANSFORMERS

A set of low profile (0.4" high) reference and output transformers (which are capable of handling the full drive capability of the DRC1745 and DRC1746 over a frequency range of 360Hz to 2.6kHz) are available in order to accept the standard voltage formats of synchros and resolvers.

The reference transformer, STM1680, can accept voltages of 11.8 volts, 26 volts or 115 volts depending on the option and its output is 3.4 volts rms which is suitable for connecting to A_{HI} and A_{LO} on the converter.

The output transformer pair, STM1683, accepts the 6.8 volts rms output of the converter and provides a synchro or resolver format depending on the option.

Note: For resolver option for the STM1683 transformer, part number is RTM1683.

The pin out and dimensions of the STM1680 and STM1683 are shown on the next page, and the connection to the converter in Figure 10.

Note: For operation over the frequency range 47Hz to 440Hz a similar set of transformers are available (1.0" profile height). Part numbers are STM1660 (reference transformer) and STM1663 (output transformer).

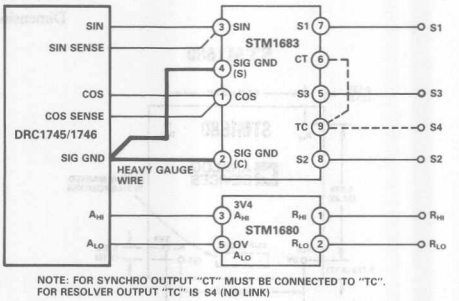


Figure 10. Connecting the DRC1745 to the STM1680 and STM1683 Transformers

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of voltage both when used with or without the reference transformer, STM1680/STM1660.

When the converters are used with the STM1680/STM1660 transformer, a resistance of value 3kΩ per extra volt required should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI}, A_{LO}) is 3.4 volts rms in order to provide a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and therefore the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} pins. Note that the input to the reference transformer should not exceed the rated max.

Note that the best dc output offset performance is achieved when the STM1680/STM1660 transformer is used. However the use of resistive scaling can never cause an additional offset of greater than 6.5mV (max), 2.6mV (typ).

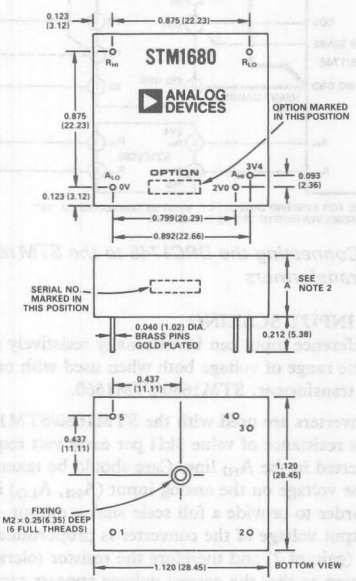
OTHER PRODUCTS

We manufacture a wide range of hybrid and modular circuits for processing synchro and resolver information. Please ask for our comprehensive literature.

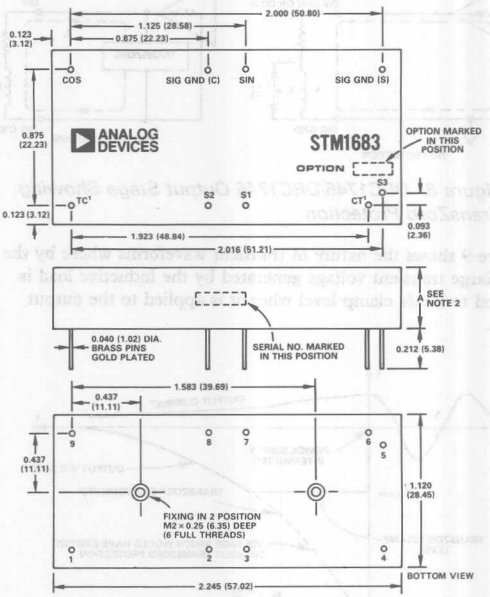
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).

STM1680

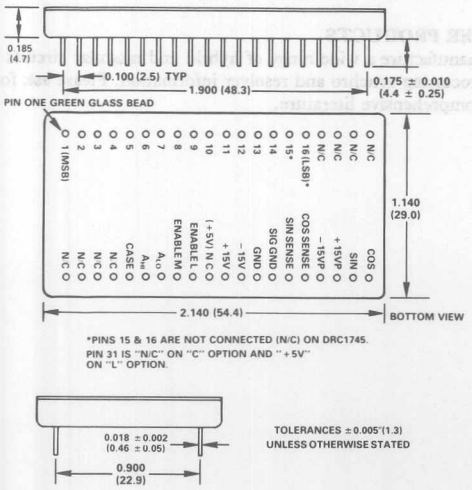


STM1683



NOTES
1. "TC" READS "S4" and "CT" READS "NC" ON RESOLVER DEVICE (RTM1683).
2. DIMENSION "A" IS 0.4 (10.2) FOR STM1680 AND STM1683. THE TOLERANCES ARE +0.010", −0.005" OR +0.25mm, −0.13mm.

DRC1745/1746



ORDERING INFORMATION

DRC1745/LT4/B

- 1745 = 14-Bit Resolution
- 1746 = 16-Bit Resolution
- Add B after part number if high reliability processing required.
- 2 = ±2 Arc-Mins Accuracy
- 4 = ±4 Arc-Mins Accuracy
- L = Low power Schottky input latches
- C = CMOS input latches
- T = Internal TransZorb protection
- O = Without TransZorb protection

STM1680.A

- 1680 = 360Hz – 2.6kHz
- A = 26V (26V reference, synchro)
- A = 115V (115V reference, synchro)
- A = 11V8 (11.8V reference, resolver)
- A = 26V (26V reference, resolver)

STM1683.4YZ

- STM for synchro output options
- RTM for resolver output options
- Z = 1 (11.8V rms synchro output)
- Z = 2 (90V rms synchro output)
- Z = 3 (11.8V rms resolver output)
- Z = 4 (26V rms resolver output)
- Z = 8 (11.8V rms resolver output)
- 1683 = 360Hz – 2.6kHz
- Y = 1 360Hz to 2.6kHz (STM1683 only)
- Y = 2 47Hz to 440Hz (STM1663 only)
- 4 = −55°C to +125°C operating temperature range.

Hybrid Inductosyn Preamplifier

IPA1764

FEATURES

Hybrid Construction
Phase Shift <5°
Phase Match <1°
Load Capacity 10,000pF
Full Military Temperature Range

APPLICATIONS

The IPA1764 is recommended for use with the 1S10/20, 1S14/24 and other 10- and 12-bit Inductosyn*/Resolver-to-Digital Converters.

GENERAL DESCRIPTION

The output signals from an Inductosyn slider are at a low level of the order millivolts and require amplification and buffering before transmission to an Inductosyn-to-digital converter. The IPA1764 provides the necessary gain and output impedance for this purpose.

Any gain mismatch in the two channels amplifying the sine and cosine outputs of the Inductosyn slider contributes to the system error. The IPA1764 with a 0.15% gain match over the temperature range only contributes an error of 0.23 micron using a 2mm pitch Inductosyn. By carefully controlling phase mismatch to less than 1°, the error contribution is only 0.2 micron in a 2mm pitch Inductosyn.

The IPA1764 with an output resistance of less than 3 ohms and a capability of driving a cable capacity of 10,000pF is totally suited to machine tool applications where the Inductosyn-to-digital converter is remote from the measuring Inductosyn.

The IPA1764 is of hybrid manufacturing techniques, and available in two temperature range versions–industrial temperature range (0 to +70°C) and extended temperature range (−55°C to +125°C).

Both versions of the IPA1764 are housed in an 18-pin metal case.

APPLICATION

The diagram below shows a "hookup" with the preamplifier, power oscillator and a 1S60 with an Inductosyn. Precise application information is not possible as the Inductosyn in its application has many variables.

Current Set Resistor

This resistor is used to match the voltage output of the oscillator to the Inductosyn track resistance and provide the manufacturer's recommended current. By variation of the voltage outputs and current resistance, track by this up to approximately 10 feet (3 meters) can be accommodated.

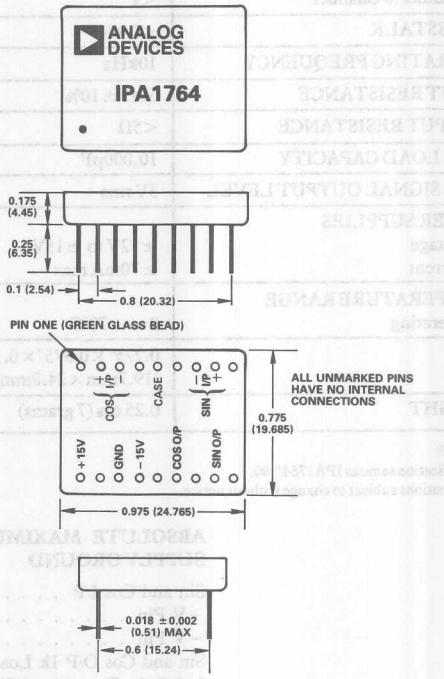
Decoupling

The preamplifier and oscillator have internal high frequency decoupling capacitors on the supply lines, however, it is recommended that electrolytic decoupling capacitors are connected close to the hybrid pins.

*Inductosyn is a registered trademark of Farrand Industries, Inc.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ORDERING INFORMATION

IPA1764 X 60 B

- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

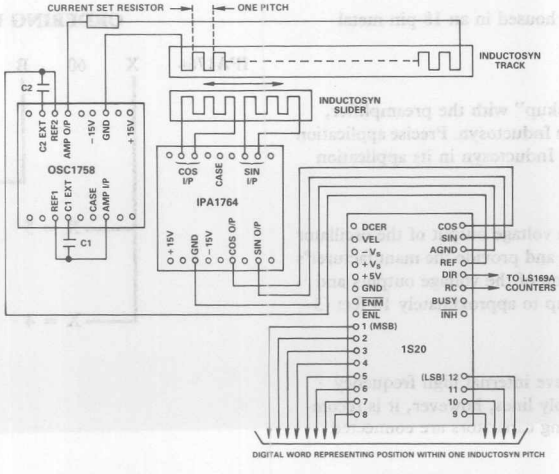
IPA1764 – SPECIFICATIONS (typical @ +25°C over full range of power supply inputs unless otherwise noted)

Model	IPA1764/560	IPA1764/460
GAIN	1250 ± 5%	*
GAIN MISMATCH Channel to Channel Over Full Temperature Range	± 0.15% (equivalent to 2.5 arc mins)	± 0.3%
PHASE SHIFT	<5°	*
PHASE MISMATCH Channel to Channel	<1°	*
CROSSTALK	<0.1%	*
OPERATING FREQUENCY	10kHz	*
INPUT RESISTANCE	5kΩ ± 10%	*
OUTPUT RESISTANCE	<5Ω	*
MAX LOAD CAPACITY	10,000pF	*
MAX SIGNAL OUTPUT LEVEL	3V rms	*
POWER SUPPLIES Voltage Current	 ± 12V to ± 15V ± 70mA max	 * *
TEMPERATURE RANGE Operating	0 to + 70°C	− 55°C to + 125°C
SIZE	0.775″ × 0.975″ × 0.175″ (19.7mm × 24.8mm × 4.5mm)	*
WEIGHT	0.25 ozs (7 grams)	*

NOTES
*Specification same as IPA1764/560.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

Sin and Cos I/P . . . . . +V
+V Pin . . . . . +17V
−V Pin . . . . . −17V
Sin and Cos O/P 1k Load . . . . . +10V
Indefinite Short Circuit Proof



Use of 1S20 with Inductosyn Preamplifier IPA1764, Hybrid Power Oscillator OSC1758

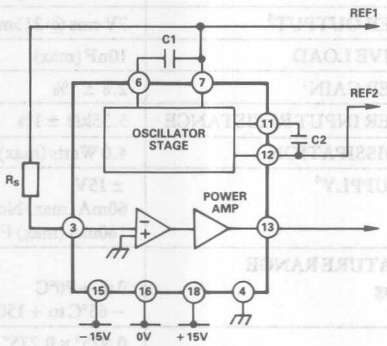
Hybrid Power Oscillator

OSC1758

FEATURES
- Full Military Temperature Range
- Hybrid Construction
- 18-Pin DIL Package
- 0-10kHz Frequency Range
- In-Phase and Quadrature Outputs

APPLICATIONS
- Synchro Resolver, and Inductosyn® Excitation
- LVDT Drive

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over 0 to 10kHz.

The device comprises two independent parts–an oscillator and a power amplifier.

The oscillator stage has two signal outputs, one 90° in phase advance with respect to the other.

The oscillator frequency is programmable in the range of 0 to 10kHz by two identical external capacitors.

The power amplifier stage is externally short circuit protected and has a gain of 2.8 ±1%. The maximum output current this stage can produce is 215mA rms (at 7V rms).

Connecting either of the oscillator stage outputs to the power amplifier input, using an external link, will give a nominal output of 7 volts rms. Lower voltages can be obtained by connecting an external resistor in series with the amplifier's inputs.

The OSC1758 is housed in an hermetically-sealed 18-pin DIL metal case, and operates over full military temperature range (−55°C to +125°C), as well as the industrial (0 to +70°C) temperature range.

MODELS AVAILABLE

The OSC1758 is available in both industrial and military temperature ranges. For details of how to specify the required part, see "Ordering Information".

CONNECTING THE OSC1758

The block diagram shows the output configuration, when using the power amplifier stage. If only the oscillator stage is required, the connection between pin 3 and pin 7 is not included.

The frequency of oscillation for the OSC1758 in the block diagram is determined by the two identical capacitors C1 and C2. For the frequency required, the value of C1 and C2 should be calculated using the following equation.

$$C_1 = C_2 = \frac{1}{F_{OSC} \times 10^5} \quad \text{Farads}$$

Where F_{OSC} = Frequency of oscillation in Hz.

For a reduced output a series resistor, R_S, must be added.

For the required output voltage R_S should be calculated as follows:

$$R_S = \frac{37.5 \times 10^3}{V_{OUT}\,(rms)} - 5350 \text{ Ohms}$$

STABILITY

To ensure stability of both frequency and voltage level outputs it is essential that good quality external capacitors are used, e.g., Silver Mica or Polystyrene.

The tolerance quoted in the specification applies if high grade Silver Mica capacitors, with a temperature coefficient of less than 50ppm/°C, and a low loss factor, are used.

POWER DISSIPATION

The thermal dissipation characteristics for the OSC1758 are as follows:

θ junction – case = 15°C/W
θ junction – ambient = 40°C/W
θ j (max) = 150°C.

Total Power Dissipation =

$(V_{SUPPLY} \times I_{SUPPLY}) - (V_{OUT} \times I_{OUT} \times \text{cosine } \phi)$

where ϕ = load phase angle

NOTE: Although the power amplifier stage has internal short circuit protection, a heat sink should be employed for protection against continuous short circuit conditions.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

Inductosyn® is a registered trademark of Farrand Industries, Inc.

OSC1758—SPECIFICATIONS (typical @ +25°C with ±15V power supplies unless otherwise noted.)

Model	OSC1758/500	OSC1758/400
FREQUENCY RANGE	0-10kHz	*
FREQUENCY STABILITY[1,2]	±5%	*
REFERENCE 1 OUTPUT[1]	2.5V rms ±5% @ 3mA rms	*
REFERENCE 2 OUTPUT[1]	2.5V rms ±5% @ 3mA rms 90° Phase Advanced with Respect to Ref. 1 Output	*
AMPLIFIER OUTPUT[3]	7V rms @ 215mA max	*
CAPACITIVE LOAD	10nF (max)	*
AMPLIFIER GAIN[1]	2.8 ± 1%	*
AMPLIFIER INPUT RESISTANCE	5.35kΩ ± 1%	*
POWER DISSIPATION	4.0 Watts (max)	*
POWER SUPPLY[4]	±15V 60mA (max) No Load 160mA (max) Full Load	* *
TEMPERATURE RANGE Operating Storage	 0 to +70°C −65°C to +150°C	 −55°C to +125°C *
SIZE	0.975" × 0.775" × 0.175" (24.8mm × 19.7mm × 4.5mm)	*
WEIGHT	0.25 ozs. 7 grams	*

NOTES
[1]Over full operating temperature range.
[2]See section on "Stability".
[3]Derated to 5V rms @ 215mA if using ±12 volt power supply.
[4]Will operate with ±12 volt power supply with derated output voltage.
*Specifications same as OSC1758/500

Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

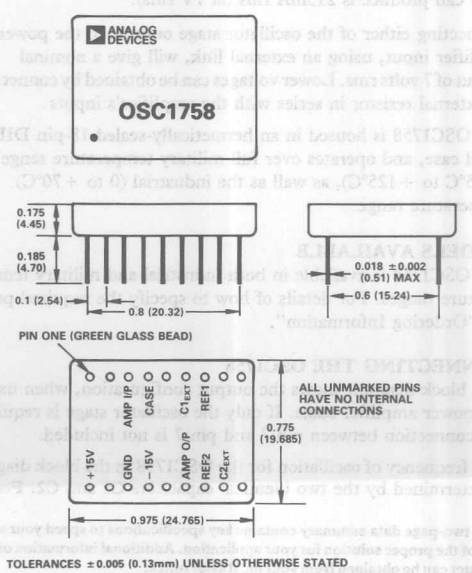
$+V_S$ . . . . . −0.3V to +18V
$-V_S$ . . . . . +0.3V to −18V

ORDERING INFORMATION

OSC1758 X 00 B
- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



TOLERANCES ±0.005 (0.13mm) UNLESS OTHERWISE STATED

12- and 14-Bit Hybrid Synchro/ Resolver-to-Digital Converters

SDC/RDC1740/1741/1742

FEATURES

- Internal Isolating Transformers
- Military Temperature Range
- Three Accuracy Options
- 14-Bit or 12-Bit Resolution
- High, Continuous Tracking Rate
- 32-Pin Welded Metal Package
- Hermetically Sealed
- Ratiometric Conversion
- Laser Trimmed – No External Adjustment
- Three-State Latched Outputs

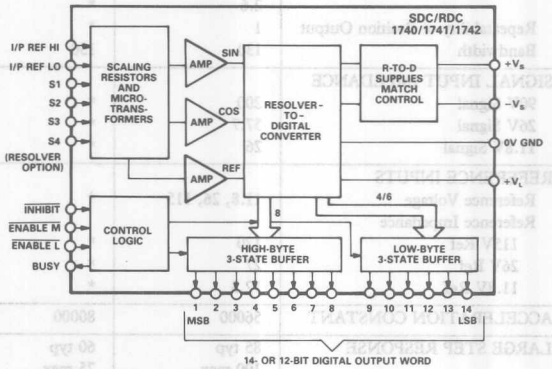
APPLICATIONS

- Flight Instrumentation Systems
- Military Servo Control Systems
- Artillery Fire Control Systems
- Avionic Systems
- Antenna Monitoring
- Robotics
- Engine Controllers
- Coordinate Conversion
- Axis Transformation
- CNC Machine Tooling
- Process Control

GENERAL DESCRIPTION

The SDC/RDC1740/1741/1742 are hybrid 14- or 12-bit continous tracking synchro or resolver to digital converters contained in 32-pin welded metal packages. In the core of this hybrid the conversion process is performed by a monolithic IC manufactured in Analog Devices proprietary BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip. Internal isolating microtransformers are used to provide true isolation of the signal and reference inputs. The 14- or 12-bit digital word is in a three-state digital form available in two bytes. Using separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 6 or 4 bits not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ input to be used without interrupting the operation of the tracking loop. The converters are hermetically sealed in a 32-pin welded metal package.

FUNCTIONAL BLOCK DIAGRAM



MODELS AVAILABLE

The three synchro/resolver-to-digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±5.3 arc minutes and a resolution of 1.3 arc minutes.

Model SDC1741XYZ is a 12-bit converter with an overall accuracy of ±15.3 arc minutes and a resolution of 5.3 arc minutes.

Model SDC1742XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc minutes and a resolution of 5.3 arc minutes.

Each model has two operating temperature range versions, those covering the industrial temperature range (0 to +70°C) and the military temperature range (−55°C to +125°C). The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage whether it will accept synchro or resolver format. To ensure a high level of reliability each converter receives stringent precap visual inspection, environmental screening and final electrical test.

Military temperature range devices and those processed to high reliability screening standards (suffix B) receive further levels of testing and screening to ensure high levels of reliability. More information about the option codes is given under the heading Ordering Information.

SDC/RDC1740/1741/1742—SPECIFICATIONS (typical at 25°C unless otherwise specified)

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
CONVERTER PERFORMANCE						
Accuracy	±5.3 max	±15.3 max	±8.5 max	arc min		1, 3
Tracking Rate	27 min	18 min	**	rev/s		4
Resolution	14	12	**	Bits	Output Coding Parallel Natural Binary	
	(1 LSB = 1.3 arc min)	(1 LSB = 5.3 arc min)	**			
Signal & Reference Frequency	400	*	*	Hz	Option X1Z	
	2.6	*	*	kHz	Option X4Z	
Repeatability of Position Output	1	*	*	LSB		4
Bandwidth	130	150	**	Hz		4
SIGNAL INPUT IMPEDANCE						
90V Signal	200	*	*	kΩ	Resistive Tolerance ±2%	4
26V Signal	57.7	*	*	kΩ		4
11.8V Signal	26	*	*	kΩ		4
REFERENCE INPUTS						
Reference Voltage	11.8, 26, 115	*	*	V rms	See Ordering Information	
Reference Impedance						
115V Ref	120	*	*	kΩ	Resistive Tolerance ±5%	4
26V Ref	27	*	*	kΩ		4
11.8V Ref	12.3	*	*	kΩ		4
ACCELERATION CONSTANT	56000	80000	**	sec^{-2}	Symbol K_a	4
LARGE STEP RESPONSE	85 typ	60 typ	**	ms	179° Step for Settling to	1, 3
	100 max	75 max	**	ms	1 LSB of Error	
POWER LINES						
$+V_S$=+15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
$-V_S$=−15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
V_L=+5V	35 typ 56 max	*	*	mA	Quiescent Condition	1, 3
Power Dissipation	1.4 max	*	*	W		
DIGITAL INPUTS (INHIBIT, ENABLE L, ENABLE M)						
V (Input High)	2 min	*	*	V dc	V_L=+5V	1, 3
V (Input Low)	0.7 max	*	*	V dc	V_L=+5V	1, 3
I (Input High)	20 max	*	*	µA	V_{IH}=2.4V	1, 3
I (Input Low)	−400 max	*	*	µA	V_{IL}=0.4V	1, 3
ENABLE AND DISABLE TIME	80 max	*	*	ns		2, 4
INHIBIT						
Sense	Logic Low	*	*			
	to INHIBIT	*	*			
Time to Data Stable (after Negative-Going Edge of INHIBIT)	640 max	*	*	ns		4
BUSY OUTPUT						
Sense	Active Logic High when converter position output changing.					
Timing	Positive going edge 50ns before change in position output.					
Width						
	400 typ	*	*	ns		4
	200 min	*	*	ns		4
	600 max	*	*	ns		4
Load	2 min	*	*	TTL		4
DIGITAL OUTPUTS						
Voltage Levels						
Logic High	2.4 min	*	*	V dc	V_L=+5V, I_{OH}=−240µA	1, 3
Logic Low	0.4 max	*	*	V dc	V_L=+5V I_{OL}=9.6mA	1, 3
Load	6 max	*	*	TTL		

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
OPERATING TEMPERATURE RANGE						
Option 5YZ	0 to + 70	*	*	°C		
Option 4YZ	−55 to +125	*	*	°C		
DIMENSIONS	1.74×1.14×0.28	*	*	Inch	See Package	4
	(44.2×28.9×7.1)	*	*	mm	Information	
WEIGHT	0.86 max	*	*	oz		4
	25 max	*	*	grams		

NOTES
[1]Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.
[2]ENABLE M enables most significant 8 bits.
ENABLE L enables least significant 4 bits (or 6 bits for SDC/RDC1740).
[3]100% tested at nominal values of power supplies, input signal voltages and operating frequency.
[4]Guaranteed by design.

*Specifications same as SDC/RDC1740.
**Specifications same as SDC/RDC1741.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

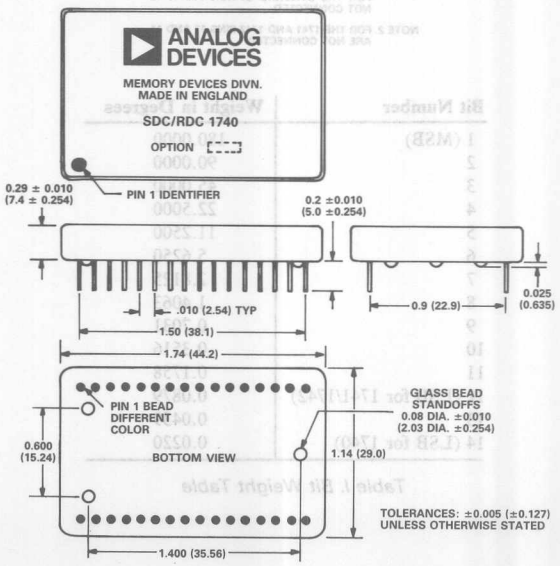
$+V_S$[1] to GND . . . . . +17.25V dc
$-V_S$ to GND . . . . . −17.25V dc
$+V_L$[2] to GND . . . . . +7V dc
Reference Input HI to GND . . . . . ±350V dc
Reference Input LO to GND . . . . . ±350V dc
Common Mode Range . . . . . 175V rms
S1, S2, S3, S4 to GND . . . . . ±350V dc
Any Logical Input to GND . . . . . −0.4V to $+V_L$
Case to GND . . . . . ±20V dc
Storage Temperature Range . . . . . −65°C to +150°C

CAUTION:
[1]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
[2]The +5V power supply must never go below GND potential.

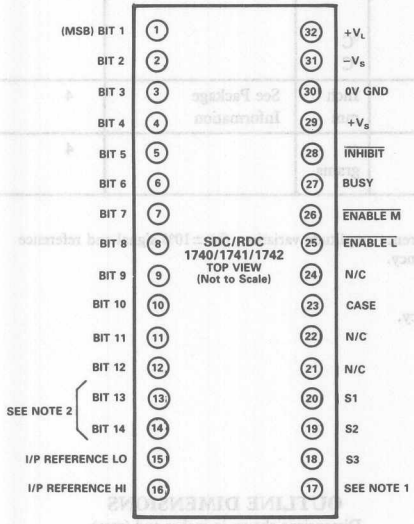
NOTE
Absolute maximum ratings are those values beyond which damage to the device may occur.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN CONFIGURATION



NOTE 1. FOR THE RESOLVER OPTION PIN 17 IS S4. FOR THE SYNCHRO OPTION PIN 17 IS NOT CONNECTED.

NOTE 2. FOR THE 1741 AND 1742 PINS 13 AND 14 ARE NOT CONNECTED.

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for 1741/1742)	0.0879
13	0.0439
14 (LSB for 1740)	0.0220

Table I. Bit Weight Table

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1-14	Bit 1-14 (1740)	Parallel output data bits.
1-12	Bit 1-12 (1741/1742)	
15	REF LO	Input pins for the reference signal.
16	REF HI	
17	S4 OR N/C	S4 signal input for Resolver option. N/C for Synchro option.
18	S3	
19	S2	Synchro/Resolver input signals.
20	S1	
21	N/C	No Connection.
22	N/C	No Connection.
23	CASE	Should be connected to 0V GND.
24	N/C	No Connection.
25	$\overline{\text{ENABLE L}}$	$\overline{\text{ENABLE L}}$ enables the 6 or 4 least significant bits.
26	$\overline{\text{ENABLE M}}$	$\overline{\text{ENABLE M}}$ enables the 8 most significant bits. Logic High sets the output data bits to a high impedance state; a Logic Low presents the data in the latches to the output pins.
27	BUSY	Converter busy. A Logic High output indicates that the output latches are being updated and data should not be transferred.
28	$\overline{\text{INHIBIT}}$	Logic Low inhibits the data transfer from the counter to the output latches.
29	$+V_S$	Main positive power supply.
30	0V GND	Power supply ground.
31	$-V_S$	Main negative power supply.
32	$+V_L$	Logic power supply.

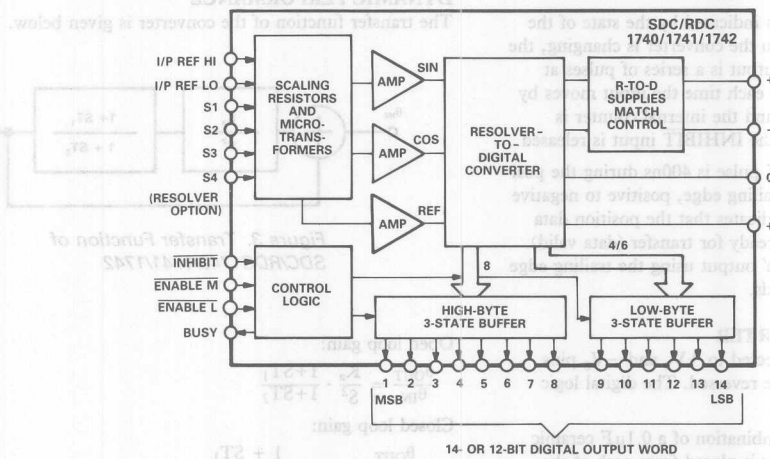


Figure 1. Functional Diagram of the SDC/RDC1740/1741/1742

THEORY OF OPERATION

In the synchro-to-digital converter configuration, the 3-wire synchro output should be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format, i.e.,

$V_1 = K\,E_O \sin \omega t \sin \theta$ (SIN)
$V_2 = K\,E_O \sin \omega t \cos \theta$ (COS)

where θ is the angle of the synchro shaft.

In the resolver-to-digital converter configuration, the 4-wire resolver output should be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by COSϕ and V_2 is multiplied by SINϕ to give:

$K\,E_O \sin \omega t \sin \theta \cos \phi$
and $K\,E_O \sin \omega t \cos \theta \sin \phi$.

These signals are subtracted by the error amplifier to give:

$K\,E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$
or $K\,E_O \sin \omega t \sin (\theta - \phi)$.

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null $\sin(\theta - \phi)$. The digital output (counter ϕ), then represents the synchro/resolver shaft angle θ within the specified accuracy of the converter.

$\overline{\text{INHIBIT}}$ INPUT

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a busy pulse to refresh the output data.

$\overline{\text{ENABLE}}$ INPUTS

The $\overline{\text{ENABLE}}$ inputs determine the state of the output data. A Logic High maintains the output data pins in the high impedance condition, and application of a Logic Low presents the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits, while $\overline{\text{ENABLE L}}$, enables the least significant 4 bits (6 bits in the SDC/RDC1740). The operation of the $\overline{\text{ENABLE}}$ inputs has no effect on the conversion process.

DATA TRANSFER

Data transfer can be accomplished using either the $\overline{\text{INHIBIT}}$ input or the trailing edge, positive to negative transition of the BUSY pulse output.

The data will be valid 640ns after the application of a Logic Lo to the $\overline{\text{INHIBIT}}$ input. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active busy pulse to clear. By using the $\overline{\text{ENABLE M}}$ and $\overline{\text{ENABLE L}}$ inputs the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a Logic Hi state to enable the output latches to be updated.

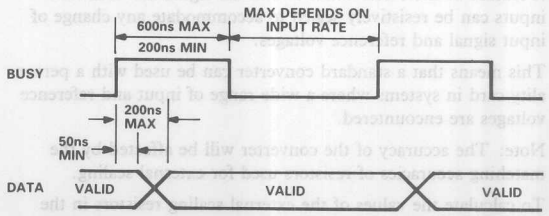


Figure 2. Timing Diagram

BUSY OUTPUT

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY is initiated each time the input moves by an analog equivalent of an LSB and the internal counter is incremented or decremented or the $\overline{\text{INHIBIT}}$ input is released.

Typically the width of the BUSY pulse is 400ns during the position data output updates. The trailing edge, positive to negative transition, of the BUSY pulse indicates that the position data output has been updated and is ready for transfer (data valid). The maximum load on the BUSY output using the trailing edge of the BUSY pulse is 2 TTL loads.

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm 15V$ and must not be reversed. The digital logic supply V_L is connected to $+5V$.

It is suggested that a parallel combination of a $0.1\mu F$ ceramic and a $6.8\mu F$ electrolytic capacitor is placed from each of the three supply pins to GND.

The pin marked CASE is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin 1 through to Pin 12 for the SDC/RDC1741/1742 and Pin 1 through to Pin 14 for the SDC/RDC1740 where Pin 1 is the MSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega t \sin \theta$$

$$E_{S3\text{-}S2} = E_{RLO\text{-}RHI} \sin \omega t \sin (\theta + 120°)$$

$$E_{S2\text{-}S1} = E_{RLO\text{-}RHI} \sin \omega t \sin (\theta + 240°)$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

$$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega t \sin \theta$$
$$E_{S2\text{-}S4} = E_{RHI\text{-}RLO} \sin \omega t \cos \theta$$

The BUSY, $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins should be connected as described under the heading Data Transfer.

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any change of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

Note: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling.

To calculate the values of the external scaling resistors in the case of a synchro converter, add $1.11k\Omega$ per extra volt of signal in series with S1, S2 and S3 and $1k\Omega$ per extra volt of reference in series with RHI. In the case of a resolver-to-digital converter, add $2.22k\Omega$ in series with S1 and S2 per extra volt of signal and $1k\Omega$ per extra volt of reference in series with RHI.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

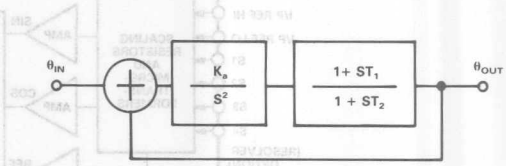


Figure 3. Transfer Function of SDC/RDC1740/1741/1742

Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1+ST_1}{1+ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3T_2}{K_a}}$$

Model SDC/RDC1740

Where $K_a = 56{,}000$
T1=0.01
T2=0.001525

The gain and phase diagrams are shown in Figures 4 and 5.

Model SDC/RDC1741/1742

Where $K_a = 80{,}000$
T1=0.0087
T2=0.001569

The gain and phase diagrams are shown in Figures 6 and 7.

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input Acceleration}}{\text{Error in Output Angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration, only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure. The following is an example using the K_a of the SDC1740.

Acceleration of 50 revolutions sec^{-2} with $K_a = 56000$

$$\text{Error in LSBs} = \frac{50 \times 16384}{56000} = 14.62\text{LSBs}$$

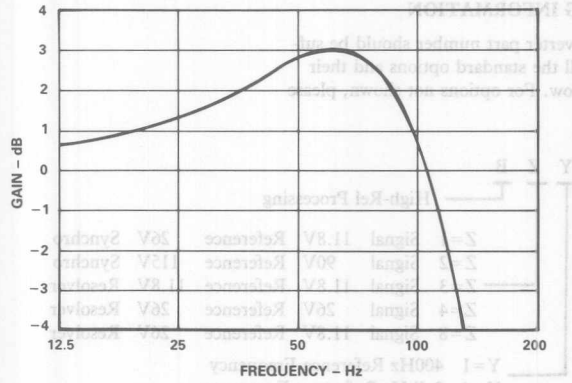


Figure 4. SDC/RDC1740 Gain Plot

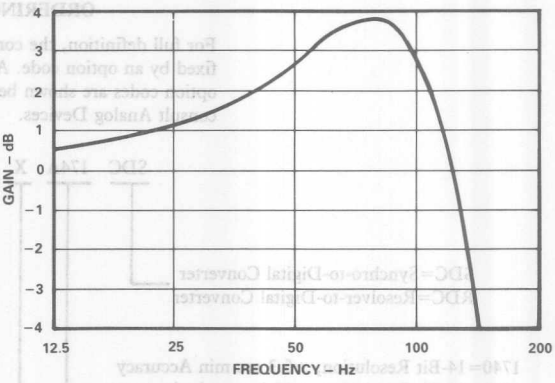


Figure 6. SDC/RDC1741/1742 Gain Plot

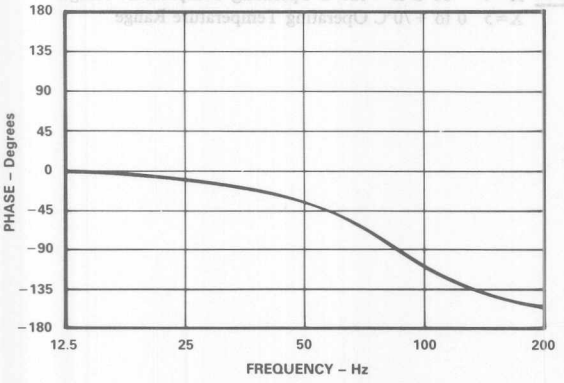


Figure 5. SDC/RDC1740 Phase Plot

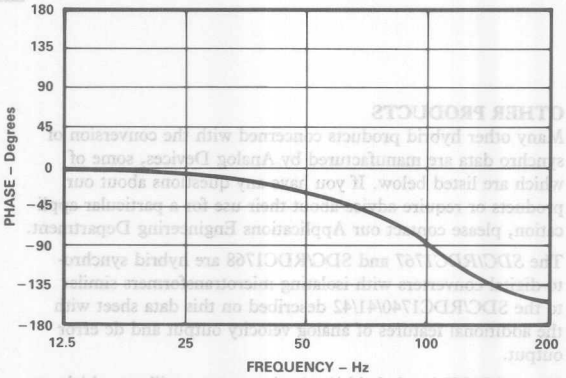


Figure 7. SDC/RDC1741/1742 Phase Plot

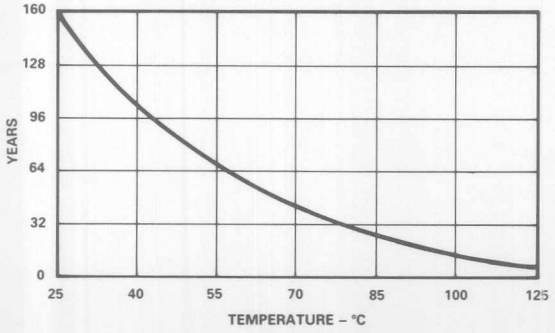


Figure 8. SDC/RDC1740/41/42 MTBF Curve

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217E, Figure 8 shows the MTBF in years versus case temperature in naval sheltered conditions for SDC/RDC1740/41/42.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.

SDC 174A X Y Z B

- B: High-Rel Processing
- Z: Signal / Reference / Synchro or Resolver
  - Z=1 Signal 11.8V Reference 26V Synchro
  - Z=2 Signal 90V Reference 115V Synchro
  - Z=3 Signal 11.8V Reference 11.8V Resolver
  - Z=4 Signal 26V Reference 26V Resolver
  - Z=8 Signal 11.8V Reference 26V Resolver
- Y: Reference Frequency
  - Y=1 400Hz Reference Frequency
  - Y=4 2.6kHz Reference Frequency
- X: Operating Temperature Range
  - X=4 −55°C to +125°C Operating Temperature Range
  - X=5 0 to +70°C Operating Temperature Range
- 174A: Resolution / Accuracy
  - 1740=14-Bit Resolution, ±5.3 arc min Accuracy
  - 1741=12-Bit Resolution, ±15.3 arc min Accuracy
  - 1742=12-Bit Resolution, ±8.5 arc min Accuracy
- SDC/RDC: Converter Type
  - SDC=Synchro-to-Digital Converter
  - RDC=Resolver-to-Digital Converter

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The *SDC/RDC1767* and SDC/RDC1768 are hybrid synchro-to-digital converters with isolating microtransformers similar to the SDC/RDC1740/41/42 described on this data sheet with the additional features of analog velocity output and dc error output.

The *OSC1758* is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over a frequency range of 0 to 10kHz.

The *DRC1745* and *DRC1746* are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins, and the outputs can supply 2VA at 7V rms.

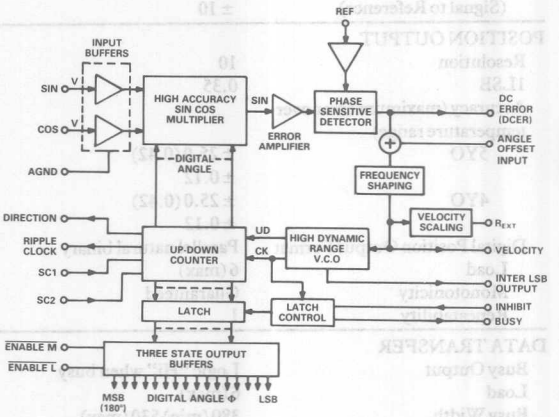
Tachogenerator Output, Variable Resolution, Hybrid, Resolver-to-Digital Converter

1S74

FEATURES
- 40-Pin Hybrid
- Tachogenerator Velocity Output
- User Selectable Resolution
- DC Error Output
- Sub LSB Output
- Angle Offset Input
- Reference Frequency of 2kHz to 10kHz
- Logic Outputs for Extension Pitch Counter

APPLICATIONS
- Numerical Control of Machine Tools
- Feed Forward Velocity Stabilizing Loops
- Robotics
- Closed Loop Motor Drives
- Brushless Tachometry
- Single Board Controllers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1S74 is a hybrid device that converts standard resolver inputs to digital position and analog velocity outputs. All the essential features of multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically, the input signal would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S74 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

In conjunction with the IPA1764 preamplifier, the 1S74 is also suitable for use with Inductosyns®.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the user's chosen volts/rpm relationship.

Repeatability is 1LSB under constant temperature conditions.

The resolution of the 1S74 converter is user selectable by means of applying a specific binary code to two of the converter's pins.

Four resolutions can be selected, all operating over a frequency range of 2kHz to 10kHz.

10 bit up to 40,800 revolutions per minute.
12 bit up to 10,200 revolutions per minute.
14 bit up to 2,550 revolutions per minute.
16 bit up to 630 revolutions per minute.

APPLICATIONS

The 1S74 has been designed for motor position control in the CNC, robotic and military fields. The use of a type 2 tracking servo loop circuit with high inherent noise immunity, makes the product ideally suited to these applications.

USER BENEFITS

Allows both velocity and position measurement from a single, low cost, standard, brushless resolver.

80dB dynamic range of velocity output.

0.5% ripple on velocity signal.

0.1% linearity of velocity signal.

Cost effective tachogenerator/encoder replacement.

Tracks at 5 to 10 times the rate of equivalent resolution encoders.

Analog output for interpolation between digital codes.

Direction and Ripple Clock (Datum) outputs facilitate revolution counting.

Hybrid construction offering small size and MTBF of >200 years at 50°C GB.

MIL operating temperature range and spec. options available.

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RESOLVER INPUTS					
Signal Voltage	2.0 (±5%)	*	*	*	V rms
Reference Voltage	2.0 (+50% −20%)	*	*	*	V rms
Signal & Reference Frequency	2k – 10k	*	*	*	Hz
Signal Input Impedance	10 (min)	*	*	*	MΩ
Reference Input Impedance	125	*	*	*	kΩ
Allowable Phase Shift (Signal to Reference)	±10	*	*	*	Degrees
POSITION OUTPUT					
Resolution	10	12	14	16	Bits
1LSB	0.35	0.088	0.022	0.0055	Degrees
Accuracy (maximum error over temperature range)					
5YO	±25.0 (0.42)	±8.5 (0.14)	±5.3 (0.09)	±4.0 (0.07)	arc-mins (degrees)
	±0.12	±0.04	±0.025	±0.019	% F.S.
4YO	±25.0 (0.42)	±8.5 (0.14)	±5.3 (0.09)	±2.6 (0.04)	arc-mins (degrees)
	±0.12	±0.04	±0.025	±0.012	% F.S.
Digital Position Output Format	Parallel natural binary	*	*	*	
Load	6 (max)	*	*	*	LSTTL
Monotonicity	Guaranteed	*	*	*	
Repeatability	1	*	*	*	LSB
DATA TRANSFER					
Busy Output	Logic "Hi" when busy	*	*	*	
Load	6 (max)	*	*	*	LSTTL
Busy Width	380 (min) 530 (max)	*	*	*	ns
ENABLE INPUTS	Logic "Lo" to enable	*	*	*	
Load	1	*	*	*	LSTTL
Enable & Disable Times	250 (max)	*	*	*	ns
INHIBIT INPUT	Logic "Lo" to inhibit	*	*	*	
Load	1	*	*	*	LSTTL
Direction Output (DIR)	Logic "Hi" when counting up, logic "Lo" when counting down.				
Load	6 (max)	*	*	*	LSTTL
Ripple Clock (RC)	Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.				
Load	6 (max)	*	*	*	LSTTL
Width	1μ (max) 850n (min)	*	*	*	secs
DYNAMIC CHARACTERISTICS					
Tracking Rate					
with ±15V Supplies	40,800 (min)	10,200 (min)	2,550 (min)	630 (min)	rpm
with ±12V Supplies	34,680 (min)	8,670 (min)	2,168 (min)	536 (min)	rpm
Acceleration Constant K_a	220,000	*	*	*	sec^{-2}
Settling Time (179° step input)	25 (max)	35 (max)	60 (max)	120 (max)	ms
Bandwidth	230	*	*	*	Hz
VELOCITY OUTPUT					
Polarity	Positive for increasing angle	*	*	*	
Tachogenerator Voltage Scaling	0.25	1.00	4	16	V/K rpm
Scale Factor Accuracy	±1 (max)	*	*	*	% of output
Scale Factor Tempco	200 (max)	*	*	*	ppm/°C
Reversion Error	±0.2 (max)	*	*	*	%
Reversion Error Tempco	50 (max)	*	*	*	ppm/°C
Linearity	0.1	*	*	*	% of output
Over Full Temperature Range	0.25 (max)	*	*	*	% of output
Ripple and Noise					
Steady State (200Hz B/W)	100	150	300	1300	μV rms
Dynamic Ripple (av-pk)	0.5 (max)	*	*	*	% of output
Zero Offset	±500	*	*	*	μV
Zero Offset Tempco	50 (max)	*	*	*	μV/°C
Output Load	5 (min)	*	*	*	KΩ

SPECIAL FUNCTIONS					
dc Error Output Voltage	450	*	*	*	mV/deg
Inter LSB Output	±1 (±20%)	*	*	*	V/LSB
Load	1k (min)	*	*	*	Ω
Angle Offset Input (over operating temperature range)	320 (±10%)	*	*	*	nA/LSB
Maximum Input	32	*	*	*	LSB
POWER REQUIREMENTS					
Power Supplies					
$\pm V_S$	±15 (±5%) or ±12 (±5%)	*	*	*	V dc
+5V	+4.75 to +5.25	*	*	*	V dc
Power Supply Consumption					
$+V_S$	30 (max)	*	*	*	mA
$-V_S$	30 (max)	*	*	*	mA
+5V	125 (max)	*	*	*	mA
Power Dissipation	1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating 5YO Option	0 to +70	*	*	*	°C
4YO Option	−55 to +125	*	*	*	°C
Storage 5YO Option	−55 to +125	*	*	*	°C
4YO Option	−60 to +150	*	*	*	°C
DIMENSIONS					
5YO Option	2.1×1.1×0.195	*	*	*	Inches
	(53.5×28×4.95)	*	*	*	(mm)
4YO Option	2.14×1.14×0.18	*	*	*	Inches
	(54.5×29×4.6)	*	*	*	(mm)
WEIGHT	1 (28)	*	*	*	oz. (grams)

Specifications subject to change without notice.

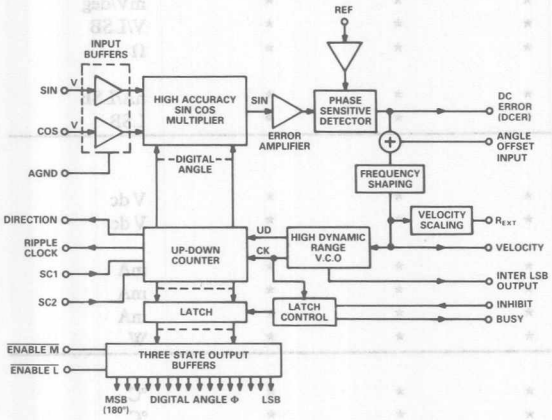
ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
+5V[2]	0V to +6.0V dc
Reference	±17V dc
Sine	±17V dc
Cosine	±17V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

FUNCTIONAL DIAGRAM



OPERATION OF THE CONVERTER

The 1S74 is a tracking converter, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the resolution option. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

The static angular accuracy quoted for each converter type is the worst case error that can occur over the full operating temperature range with the following input conditions:

a) Signal input amplitudes within 5% of the nominal values.

b) Signal and reference frequency within the specified operating range.

c) Phase shift between signal and reference less than 10 degrees.

d) Signal and reference waveform harmonic distortion less than 10 percent.

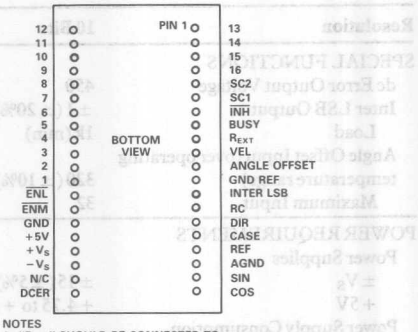
These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the converters can be used well outside these operating conditions providing the following points are observed.

SIGNAL AMPLITUDE (SINE AND COSINE INPUTS)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the analog outputs and inputs of the converter such as velocity, inter LSB position and angle offset.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value the angular error will increase by an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the K_a is proportional to signal level.

PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" FOR UNITY GAIN.
2. CASE PIN CONNECTED ON 460 OPTION ONLY

SIGNAL AND REFERENCE FREQUENCY

Any frequency within the specified range of the converter may be used. It should be noted that the signal and reference input voltages must be in resolver format.

REFERENCE VOLTAGE LEVEL

The amplitude and waveform of the reference signal applied to the converter's input is not critical, however it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square and triangle waveforms can be used but the input levels should be adjusted so that the average value after rectification is 1.9 volts. (For example – a square wave should be 1.9V peak.)

NOTE: The figure specified of 10% harmonic distortion is for calibration convenience only.

PHASE SHIFT (BETWEEN SIGNAL AND REFERENCE)

See Section on "Dynamic Accuracy vs. Resolver Phase Shift".

RESOLUTION PROGRAMMING

The 1S74 converter can be programmed for resolutions of 10, 12, 14, and 16 bit by applying a binary code to the pins "SC1" and "SC2".

The dc error output and maximum revolutions per minute for full scale are scaled internally according to the particular resolution selected.

Table I gives the binary code, dc error output and maximum tracking rate for the resolutions available.

Resolution	Binary Code SC1	SC2	DC Error (mV/Bit)	Tracking Rate for FS (±10V) rpm
10 Bit	0	0	160	40,800
12 Bit	0	1	40	10,200
14 Bit	1	0	10	2,550
16 Bit	1	1	2.5	630

Table I.

NOTE: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

For more information ask for the relevant application note.

DATA TRANSFER

BUSY Output:

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

NOTE: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

$\overline{\text{ENABLE}}$ Inputs:

Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the most significant 8-bits and $\overline{\text{ENABLE L}}$ for the least significant remainder. These $\overline{\text{ENABLES}}$ determine the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins. The operation of these $\overline{\text{ENABLES}}$ has no effect on the conversion process.

Two methods are available for transferring data, by using the inputs and outputs described.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

RIPPLE CLOCK (RC) AND DIRECTION (DIR) OUTPUTS:

As the digital output of the converter passes through the major carry, i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

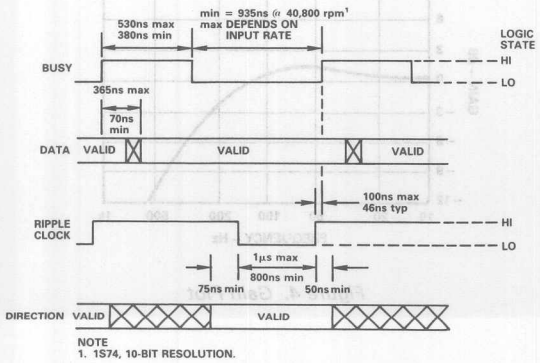


Figure 1. Timing Diagram

The DIRECTION (DIR) logic output indicates the direction of input rotation and this data is always valid in advance of the RIPPLE CLOCK pulse, and stays valid until the direction changes (see Timing Diagram).

These two logic outputs are provided so that the user can count the input revolutions or pitches. An external extension counter is required. Figure 2 shows the application circuit which should be used to perform this counting function.

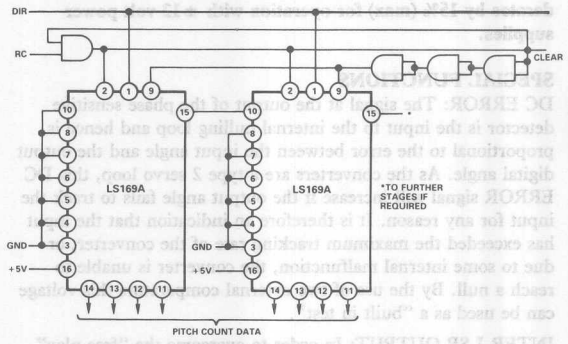


Figure 2. Connections for Use with LS Extension Counters

VELOCITY OUTPUT

The tracking conversion technique produces an internal signal at the input to the voltage controlled oscillator (VCO) that is proportional to the rate of the input angle. In the 1S74 additional circuitry is included to linearize this signal, which is closely characterized, producing a high quality tachogenerator velocity output at the VELOCITY (VEL) pin.

This analog tachogenerator velocity output is resistively scaled internally to give a full scale output of ±10V dc at the specified tracking rate for the converter.

However, a full scale output of ±10V dc can be obtained for lower speeds by changing the gain of the internal scaling amplifier using only an external resistor. The external resistor, R_{EXT}, should be connected between "R_{EXT}" pin and ground, and calculated using the following equation.

$$R_{EXT} = \frac{10 \times A}{B - A} \text{ k ohms}$$

Where A = required rpm to be represented by ±10V FS

B = specified rpm for the converter.

NOTE: A cannot be greater than B and for unity gain "VEL" and "R_{EXT}" pins should be linked.

Ripple and noise on the velocity signal consists of two components—steady state noise and dynamic noise.

Steady state noise—this is internally generated noise produced by the converter's circuitry and is the only noise signal present under static input conditions.

Dynamic noise—this is the noise produced, in addition to steady state noise, under dynamic operating conditions.

The two main components of the dynamic noise signal are due to the "non-zero" angular error of the resolver/converter combination. The figures given in the specification are typical for a size 11, 7 arc-minutes, brushless resolver.

It should be noted that when operating at low tracking rates it is critical to maintain the signal input voltage at its nominal value in order to keep the noise level on the velocity signal to an absolute minimum. The effect of variation in signal voltage at low tracking rates is to produce low energy spikes on the velocity output on the rising edge of the BUSY pulse. The amplitude of these spikes will be in the region of 30μV per percent variation in signal input voltage level.

NOTE: The velocity signal output and max tracking rate derates by 15% (max) for operation with ±12 volt power supplies.

SPECIAL FUNCTIONS

DC ERROR: The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converters are a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason. It is therefore an indication that the input has exceeded the maximum tracking rate of the converter, or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

INTER LSB OUTPUT: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

The output is therefore proportional to the inter LSB resolved position with a maximum output representing 1LSB.

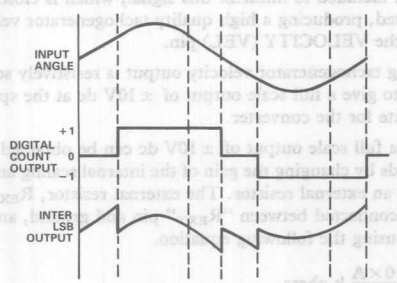


Figure 3.

Figure 3 illustrates how the INTER LSB output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and INTER LSB output equals the actual input angle.

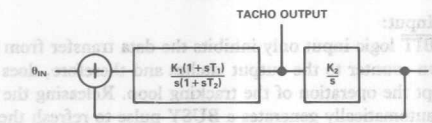
ANGLE OFFSET: A unique feature of the 1S74 converter is the angle offset input which allows the user to electrically "rotate" the input shaft of the resolver.

Injecting a current of 320nA into the angle offset input pin will offset the digital output of the converter by 1LSB relative to the angle defined by the resolver inputs. It is recommended that an offset equivalent to no greater than 30LSB's be applied to this input.

This input is a virtual ground, therefore a current source can be generated by a voltage source connected by a single resistor.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below:



Positional Transfer Function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1 K_2}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2} \text{ open loop}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_1 K_2} + \frac{s^3 T_2}{K_1 K_2}} \text{ closed loop}$$

where $K_1K_2 = K_a$

Tachogenerator Transfer Function:

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{K_1(1 + sT_1)}{s(1 + sT_2)} \text{ open loop}$$

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{s(1 + sT_1)}{K_2(1 + sT_1) + \frac{s^2}{K_1} + \frac{s^3 T_2}{K_1}} \text{ closed loop}$$

Where: $K_1 = 3.23$
$K_2 = 68.2 \times 10^3$
$K_a = 220 \times 10^3$
$T_1 = 4.46\text{ms}$
$T_2 = 0.21\text{ms}$

Refer: Figures 4 and 5

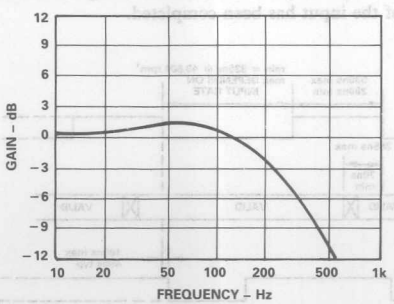


Figure 4. Gain Plot

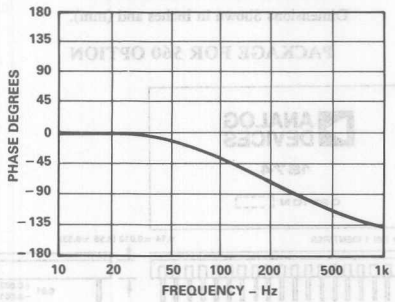


Figure 5. Phase Plot

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Under static operating conditions phase shift between signal and reference lines theoretically does not affect the converter's static accuracy:

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions, to an additional error defined by:

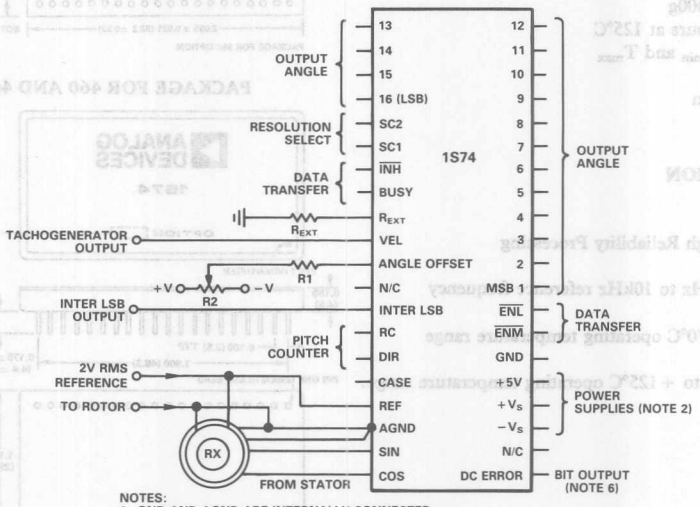
$$\frac{\text{SHAFT SPEED (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.



NOTES:
1. GND AND AGND ARE INTERNALLY CONNECTED.
2. EACH SUPPLY SHOULD BE DECOUPLED WITH 100nF CERAMIC CAPACITOR IN PARALLEL WITH A 6μF TANTALUM CAPACITOR.
3. REXT IS EXTERNAL TACHOGENERATOR SENSITIVITY SCALING RESISTOR (IF REQUIRED) – SEE TEXT UNDER HEADING "VELOCITY OUTPUT".
4. R1 AND R2 ARE ANGLE OFFSET INPUT SCALING RESISTORS (IF REQUIRED) – SEE TEXT.
5. CASE PIN CONNECTED ON 460 OPTION ONLY.
6. POSSIBLE USE AS BUILT-IN TEST EQUIPMENT. (SEE HEADING "SPECIAL FUNCTIONS".)

Figure 6. Electrical Connections

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to +V, and −V, pins can be ±12V to ±15V but must not be reversed. The +5V supply connects to the +5V pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors are connected in parallel between the power lines ($+V_s$, $-V_s$ and +5V) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 6). The 2V rms reference supply, which can be provided by the OSC1758 oscillator, should be connected to the resolver rotor.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

HI-REL PROCESSING

All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 5000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{min} and T_{max}
7. Seal test, fine and gross
8. External visual inspection

ORDERING INFORMATION

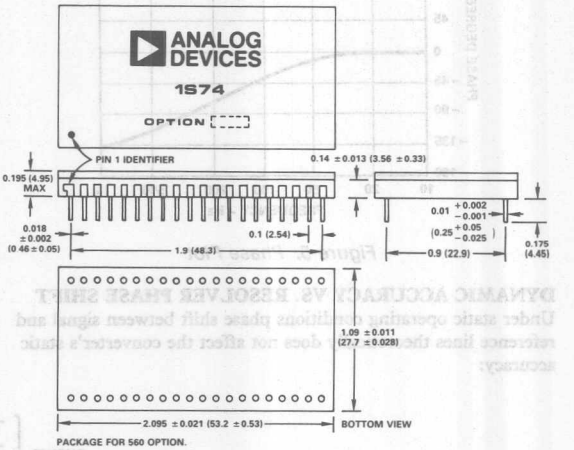
1S74 X60 B

- B — High Reliability Processing
- X60 — 2kHz to 10kHz reference frequency
- X=5 0 to +70°C operating temperature range
- X=4 −55°C to +125°C operating temperature range.

OUTLINE DIMENSIONS

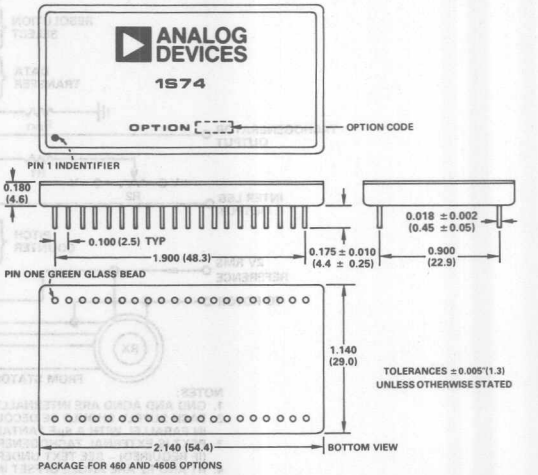
Dimensions Shown in inches and (mm).

PACKAGE FOR 560 OPTION



PACKAGE FOR 560 OPTION.

PACKAGE FOR 460 AND 460B OPTIONS



PACKAGE FOR 460 AND 460B OPTIONS

OTHER PRODUCTS

1S14/1S24/1S44/1S64–	10-, 12-, 14- and 16-Bit Hybrid Resolver-to-Digital Converters with High Specification Tachometer Output.
1S10/1S20/1S40/1S60/1S61–	10-, 12-, 14- and two 16-Bit Inductosyn™/ Resolver-to-Digital Converters (Hybrid)
IRDC1732–	Inductosyn™/Resolver-to-Digital Converter (Hybrid), Low Cost
IPA1751–	Inductosyn™ Pre-Amplifier
OSC1754–	Power Oscillator
OSC1758–	Power Oscillator (Hybrid)
IPA1764–	Inductosyn™ Pre-Amplifier (Hybrid)
MCI1794–	3 Channel Inductosyn™/Resolver-to-Digital Converter (Multibus Compatible Card)

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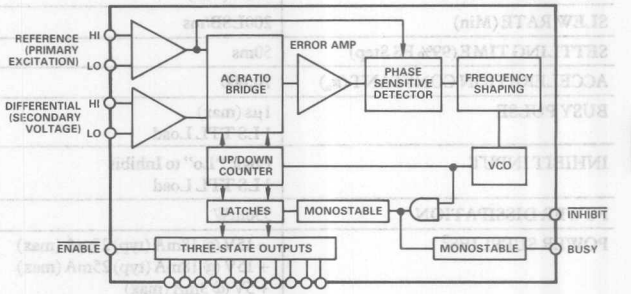
LVDT-to-Digital Converter

2S50

FEATURES
- Internal Signal Conditioning
- Direct Conversion to Digits
- Reference Frequency 400Hz or 1kHz to 10kHz
- High MTBF
- No External Trims
- Absolute Encoding

APPLICATIONS
- Industrial Measurement and Gauging
- Numerical Control
- Avionic Control Systems
- Valves and Actuators
- Limit Sensing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S50 series converters translate the outputs from LVDT and RVDT transducers into digits directly. No signal conditioning, trims, preamplifiers, demodulators or filters are required. The 2S50 series can also be used as general purpose ratiometric A-to-D converters; very compatible with load cells, strain gauge bridges, some pressure transducers and interferometers.

The 2S50 linearly converts ac signals into an 11-bit parallel digital word. The digital output is an offset binary word which is the ratio of the signal and reference inputs. When used with LVDT and RVDT transducers, the digital output represents the linear or rotary displacements of the transducer. The converter is a continuous tracking type using a type 2 servo loop.

PRINCIPLE OF OPERATION

The 2S50 is a tracking converter. This means that the output automatically follows the input without the necessity of a convert command.

A conversion is initiated by a change of input signal equivalent to 1LSB of the output.

Each LSB increment of the output is indicated by a "Busy" pulse.

With an LVDT connected to give a null at center position, the output will track the input from digital "1 + all zeroes" to digital "all ones" for plus full scale, and digital "1 + all zeroes" to digital "all zeroes" for negative full scale.

The 2S50 operates only on the ratio of the two inputs for the conversion process. As such the whole system, consisting of excitation oscillator, LVDT and converter, is insensitive to change in excitation voltage, amplitude, frequency and waveshape.

Since a phase sensitive demodulator is included with the conversion loop of the 2S50, the system has a high rejection to signals that are not phase and frequency coherent with the excitation voltage. This feature, combined with ratiometric conversion gives a very high standard of integrity to digitized LVDT and RVDT systems.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply − 15V dc.
$+V_S$	Main positive power supply + 15V dc.
+5V	Logic supply.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-11	Parallel output data bits.
Ref Hi	Analog reference input (Hi).
Diff Hi	Analog difference input (Hi).
Ref Lo	Analog reference input (Lo).
Diff Lo	Analog difference input (Lo).
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "Lo".
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ±20V.
N/C	Pins designated N/C not connected internally.

ORDERING INFORMATION

2S50/ X Y 0 B

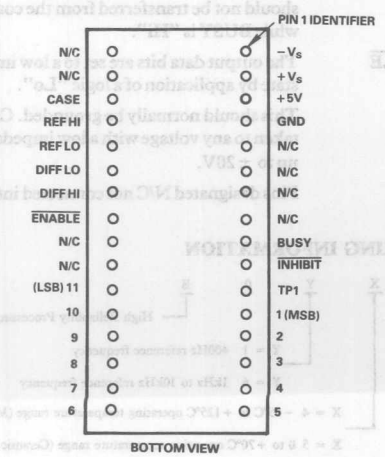
- B — High Reliability Processing
- Y = 1 400Hz reference frequency
- Y = 6 1kHz to 10kHz reference frequency
- X = 4 −55°C to +125°C operating temperature range (Metal Package)
- X = 5 0 to +70°C operating temperature range (Ceramic Package)

2S50—SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	2S50/510	2S50/560	2S50/410	2S50/460
RESOLUTION	11 Bits	*	*	*
ACCURACY[1]	0.1% (Full Scale)	0.1%	0.2%	0.2%
LINEARITY	±1/2LSB	*	*	*
REFERENCE FREQUENCY	400Hz	1kHz–10kHz	400Hz	1kHz–10kHz
SIGNAL INPUTS[2]	2.5V rms	*	*	*
INPUT IMPEDANCE	5MΩ (min)	*	*	*
SLEW RATE (Min)	200LSB/ms	400LSB/ms	200LSB/ms	400LSB/ms
SETTLING TIME (99% FS Step)	50ms	25ms	50ms	25ms
ACCELERATION CONSTANT (k_a)	70,000	650,000	70,000	650,000
BUSY PULSE	1μs (max) 1 LS TTL Load	* *	* *	* *
INHIBIT INPUT	Logic "Lo" to Inhibit 1 LS TTL Load	* *	* *	* *
POWER DISSIPATION	550mW	*	*	*
POWER SUPPLIES[3]	−15V @ 18mA (typ) 25mA (max) +15V @ 18mA (typ) 25mA (max) +5V @ 3mA (max)	* * *	* * *	* * *
TEMPERATURE RANGE Operating Storage	 0 to +70°C −60°C to +150°C	 * *	 −55°C to +125°C *	 ** *
DIMENSIONS	1.72″ × 1.1″ × 0.205″ (43.5 × 28.0 × 5.2mm)	* *	1.74″ × 1.14″ × 0.28″ (44.2 × 28.9 × 7.1mm)	** **
WEIGHT	1 oz. (28g)	*	*	*
PACKAGE OPTIONS[4]	DH-32E	DH-32E	M-32	M-32

NOTES
[1]Accuracy applies over ±20% signal voltage, ±20% excitation frequency and full temperature range, and for not greater than 3° phase error between reference and difference inputs.
[2]This is a nominal value.
[3]±12 volts to ±17 volts.
[4]DH-32E = Bottom Brazed Ceramic DIP; M = Metal Platform DIP. For outline information see Package Information section.
*Specifications same as 2S50/510.
**Specifications same as 2S50/410.
Specifications subject to change without notice.

PIN CONFIGURATION



BOTTOM VIEW

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$	0V to +17V dc
$-V_S$	0V to −17V dc
+5V	0V to +5.5V dc
Ref, Hi to Lo	±20V dc
Diff, Hi to Lo	±20V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc

High Resolution LVDT to Digital Converters

2S54/2S56/2S58

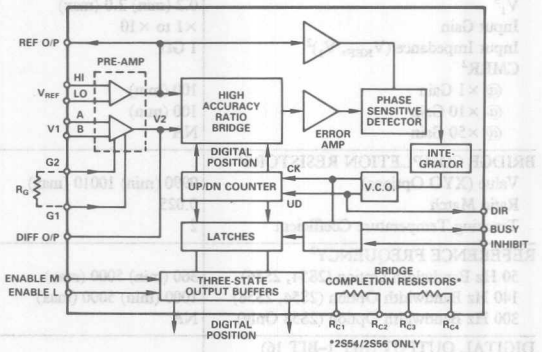
FEATURES

- Direct Conversion of LVDT and RVDT Outputs into Digital Format
- Ratiometric Conversion for Extremely High Stability
- High Resolution (14-16 Bit) Parallel Digital Output
- User Definable Input Gain
- Quadrature Rejection
- Operation Over 360 Hz to 11 kHz Frequency Range
- Linearity Better than ±0.01%
- Internal Bridge Completion Resistors
- 1 LSB Repeatability
- 75% Overrange Capability
- Extended Temperature Range Versions

APPLICATIONS

- Direct LVDT/RVDT-to-Digital Conversion
- Industrial Measurement and Gauging
- Valve and Actuator Control
- Limit Sensing
- Aircraft Control Systems
- Semiconductor Wafer Profiling
- AC-to-Digital Conversion

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S56 series of converters linearly converts the outputs of ac energized Linear and Rotary Variable Differential Transformers (LVDTs, RVDTs) directly into a high resolution digital format. For example, with a ±1 mm stroke LVDT, the least significant bit (LSB) of the 2S56 will represent 0.061 microns.

The 2S58, a high gain variant of the 2S56, can offer even higher positional resolution. Using the same ±1 mm stroke LVDT over a reduced range, the 2S58 can realize an LSB weighting of 1.22 nm.

The ratiometric conversion technique employed by the converters obviates the need for high stability oscillators. The performance quoted for the devices can be achieved with as much as a ±10% variation in reference amplitude.

The converters are complete – no signal conditioning, preamplifiers or filters are required. The user need only supply a suitable reference oscillator.

The converters operate on a Type II, tracking, servo loop principle which means that the digital output continuously follows the transducer input without the need for external convert commands as in conventional A-to-D converters. The conversion technique also ensures that there is no lag between digital output and transducer input under constant velocity conditions.

To facilitate interfacing with various types of LVDTs and RVDTs, all inputs are fully differential. In addition, the converters have the flexibility of setting the input gain with a single external resistor or link. In order to simplify the transducer interface, both the output of the gain stage as well as the reference voltage are brought out to enable simplified measurement.

The parallel digital output word is through tri-state drivers to enable direct connection to system data buses. Included is a High/Low byte enable which allows communication on both 8 and 16-bit busses. A separate line is provided to indicate the direction of transducer travel. A BUSY pulse is provided indicating that data is changing and not valid for transfer.

APPLICATIONS/USER BENEFITS

Because the 2S56 series of converters operates on the ratio of the transducer output signal to the excitation (reference) voltage, the entire measurement system is insensitive to changes in reference voltage, frequency and wave shape. The resulting stability makes conversion technique unrivaled, particularly in applications with poor voltage regulation.

The converters can also be connected in a mode which allows the 2S54/56/58 to be galvanically isolated from the excitation source. This configuration has the added benefit of minimizing the effect of phase shifts and signal input quadrature.

Because of the use of a phase sensitive demodulator in the tracking loop, the system has extremely high rejection of signals which are not phase and frequency coherent with the excitation voltage. The resulting noise immunity makes the converters an ideal choice for industrial and airborne applications.

The high precision of the conversion, together with the stability offered by ratiometric conversion, make the 2S56 series good candidates for applications previously beyond the capability of LVDTs. For example, the 2S58 can realize performance competitive with optical interferometric measurement systems.

Format Overrange[2]	14-Bit Binary 75% of FS	16-Bit Binary *	16-Bit Binary *	Output Coding Parallel Natural Binary	
INPUTS (DIFFERENTIAL)					
V_{REF}	2	*	*		V rms
V_2	2	*	*		V rms
V_1[3]	0.2 (min) 2.0 (max)	*	0.04 (min) 0.2 (max)	See "INPUT GAIN" and	V rms
Input Gain	×1 to ×10	*	×10 to ×50	"SCALING INPUTS"	
Input Impedance (V_{REF}, V_1)[2]	1 GΩ	*	6 MΩ		
CMRR[2]					
@ ×1 Gain	100 (min)	*	NA		dB
@ ×10 Gain	100 (min)	*	120 (min)		dB
@ ×50 Gain	NA	NA	120 (min)		dB
BRIDGE COMPLETION RESISTORS[2]				(Only in 2S54/2S56)	
Value (XYO Options)	9990 (min) 10010 (max)	*	NA		Ω
Ratio Match	0.025	*	NA		%
Tracking Temperature Coefficient	2	*	NA		ppm/°C
REFERENCE FREQUENCY[2]					
50 Hz Bandwidth Option (2S54, 2S56)	360 (min) 5000 (max)	*	NA		Hz
140 Hz Bandwidth Option (2S54, 2S56)	1000 (min) 5000 (max)	*	NA		Hz
300 Hz Bandwidth Option (2S58 Only)	NA	NA	7000 (min) 11000 (max)		Hz
DIGITAL OUTPUT (BIT 1–BIT 16)					
Output Voltage				V_L = +5 V dc	
(Logic Low I_{OL}=8.0 mA)	0.4 (max)	*	*	Logic Low I_{OL} = 8.0 mA	V dc
(Logic High I_{OH}=−0.4 mA)	2.4 (min)	*	*	Logic High I_{OH} = −0.4 mA	V dc
Tristate Leakage Current				V_L = +5 V dc	
(V_{OZL}=0.4 V dc)	±20 (max)	*	*	Logic Low V_{OZL} = 0.4 V dc	µA
(V_{OZH}=2.4 V dc)	±20 (max)	*	*	Logic High V_{OZH} = 2.4V dc	µA
DIGITAL INPUT (INHIBIT, ENABLE M, ENABLE L)					
Low Input Voltage	0.7 (max)	*	*	V_L = +5 V dc	V dc
High Input Voltage	2.0 (min)	*	*	V_L = +5 V dc	V dc
Low Input Current	−400 (max)	*	*	V_{IL} = 0.4 V dc	µA
High Input Current	20 (max)	*	*	V_{IH} = +2.4 V dc	µA
DATA TRANSFER[2]				See Figure 12	
BUSY Pulse Width	380 (min) 530 (max)	*	*		ns
BUSY Pulse Load[4]	6	*	*	BUSY Is "Hi" When Output Is Changing	LSTTL Loads
Enable/Disable Time	120 (typ) 220 (max)	*	*		ns
Data Setup Time	600	*	*		ns
ACCURACY[5]					
Conversion Accuracy	±0.7	±2.5	±1		LSB
Gain Accuracy[6, 7]					
@ ×1 Gain					
0 to +70°C (5Y0)	±0.03 (max)	*	NA	2S54/2S56 Only	% FSR
−55°C to +125°C (4Y0)	±0.03 (max)	*	NA		% FSR
@ ×10 Gain					
0 to +70°C (5Y0)	±0.07 (max)	*	*	2S54/2S56 and 2S58	% FSR
−55°C to +125°C (4Y0)	±0.10 (max)	*	*		% FSR
@ ×50 Gain					
0 to +70°C (5Y0)	NA	NA	±0.09 (max)	2S58 Only	% FSR
−55°C to +125°C (4Y0)	NA	NA	±0.12 (max)		% FSR

Models	2S54	2S56	2S58	Comments	Units
Integral Linearity[6, 7]					
0° Phase Shift, V_{REF} to V_1	±0.006 (max)	*	±0.00312 (max)	See "PHASE SHIFT	% FSR
1° Phase Shift, V_{REF} to V_1	±0.008 (max)	*	±0.00437 (max)	AND QUADRATURE	% FSR
5° Phase Shift, V_{REF} to V_1	±0.01 (max)	*	±0.00625 (max)	EFFECTS"	% FSR
Differential Linearity[6]	±0.5 (max)	*	*		LSB
Temperature Dependent Position Offset[2]	±0.04 (max)	*	*		% FSR
REPEATABILITY[5]					
Over 0 to +70°C[2]	±1	*	*		LSB
Hysterisis	0.5 (min) 1 (max)	*	*		LSB
DYNAMIC CHARACTERISTICS[5]					
Slew Rate[2]					
50 Hz Bandwidth Option (2S54, 2S56)	150	*	NA		LSB/ms
140 Hz Bandwidth Option (2S54, 2S56)	360	*	NA		LSB/ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	688		LSB/ms
Settling Time (Half FS Step)					
50 Hz Bandwidth Option (2S54, 2S56)	160	300	NA	Half FS Step	ms
140 Hz Bandwidth Option (2S54, 2S56)	70	160	NA	Half FS Step	ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	65	Step From +FSR to −FSR	ms
ANALOG OUTPUTS					
DIFF O/P (Max Allowable Swing)	10	*	*		V p-p
REF O/P (Max Allowable Swing)	10	*	*		V p-p
POWER REQUIREMENTS					
$+V_S$	+15 ±5%	*	*		V dc
$-V_S$	−15 ±5%	*	*		V dc
+5 V	+5 ±5%	*	*		V dc
Supply Currents					
$\pm V_S$	25 (typ) 40 (max)	*	*	Quiescent Condition	mA
+5 V	105 (typ) 125 (max)	*	*		mA
Power Dissipation	1.3 (typ) 1.8 (max)	*	*		Watts
TEMPERATURE RANGE					
Operating	0 to +70 (5Y0 Option)	*	*		°C
	−55 to +125 (4Y0 Option)	*	*		°C
Storage	−55 to +125	*	*		°C
DIMENSIONS	2.145 × 1.145 × 0.227 (max)	*	*	See Packaging	Inches
	54.5 × 29.1 × 5.76 (max)	*	*	Specifications	mm
WEIGHT	1	*	*		Ounces
	28	*	*		Grams
PACKAGE OPTIONS[8]	DH-40A	DH-40A	DH-40A		

NOTES

[1]Tested with nominal supply (±15 V dc, +5 V dc), reference/signal voltages and frequency.

[2]Guaranteed by design, test not required.

[3]V_1 is the signal input to the converter directly from the transducer. V_2 is the output of the internal gain stage. Because V_2 needs to be maintained at 2 V ±10% in order to meet the converter accuracy (see Note 5), the gain and the maximum value of V_1 should be carefully chosen. Furthermore, because the converter operates on the ratio of V_2 and V_{REF}, care should be taken to see these voltages are matched in order to achieve the full dynamic range of the converter.

[4]Maximum output current is 2.4 mA.

[5]Specified over the operating temperature range of the option and for:

a. ±10% difference in both V_{REF} and V_2 amplitudes

b. 10% harmonic distortion in V_{REF} and V_1.

c. The accuracy is specified for the preset gains of ×1, ×10, and ×50. For accuracy in the intermediate range, see Section "PHASE SHIFT AND QUADRATURE EFFECTS."

[6]Tested with input gains 1, 10 and 50 with V_1 attenuated by 1, 10 and 50, respectively.

[7]Full-Scale Range (FSR) is defined as $V_2 = +V_{REF}$ to $V_2 = -V_{REF}$. This would usually correspond to the utilized LVDT stroke.

[8]DH-40A = Hermetic Metal Can DIP.

*Specifications the same as the 2S54.

Specifications subject to change without notice.

MODELS AVAILABLE

The 2S56 series is available in three versions:

2S54	14-Bits	Input Gain 1–10
2S56	16-Bits	Input Gain 1–10
2S58	16-Bits	Input Gain 10–50

The 2S54 and 2S56 are available in two bandwidth options. The 50 Hz bandwidth option operates over the reference frequency range of 360 Hz to 5 kHz, while the 140 Hz bandwidth option operates over the range of 1 kHz to 5 kHz. The 2S58 is available only in a 300 Hz bandwidth version which operates with reference frequencies between 7 kHz and 11 kHz.

All three devices are available in both commercial (0 to +70°C) and military (−50°C to +125°C) operating temperature versions.

Full ordering information is given on the back page of this data sheet.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND	+17 V dc
$-V_S$ to GND	−17 V dc
V_{REF}	35 V p-p
$+V_L$ to GND	+7 V dc
V1	35 V p-p
Logical Input to GND (max)	+5.5 V dc
Logical Input to GND (min)	−0.4 V dc
Case to GND	±20 V dc
Power Dissipation	1.8 Watts
Junction Temperature	+150°C

CAUTION:

1. Absolute Maximum Ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. The +5 V power supply must never go below GND.

PRINCIPLES OF OPERATION

The principle of operation is shown in Figure 1.

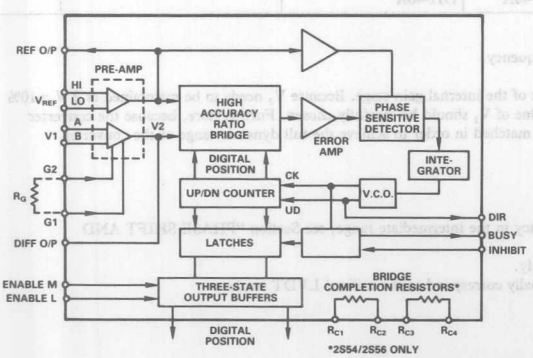


Figure 1. Principle of Operation of the 2S56 Series Converters

USING THE 2S56 SERIES CONVERTERS

The 2S56 series of converters operates on a tracking principle. This means that the output digital word always automatically represents the position of the LVDT or RVDT without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to 1 Least Significant Bit (LSB) on the output, the output digital word is automatically updated. Each LSB update initiates a BUSY pulse.

INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage is typically in the order of 1:0.15, provision for gain scaling has been provided. The gain can, therefore, be selected to ensure that the full-scale output of the converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by means of Pins 21 and 22 (G1 and G2). A link between the two pins gives a preset gain of ×10 (×50 on the 2S58) whereas no connections between them gives a preset gain of ×1 (×10 on the 2S58).

$$G = \frac{R_1}{R_G + R_2} + G\infty$$

where R_G is the value of the external resistor in kΩ and G is the realized gain.

For the 2S54 and 2S56:

$R_1 = 27$ [kΩ]

$R_2 = 3$ [kΩ]

$G\infty = 1$

For the 2S58:

$R_1 = 108$ [kΩ]

$R_2 = 2.7$ [kΩ]

$G\infty = 10$

The internal resistors each have absolute accuracies of 0.02% at 25°C. Their absolute temperature coefficient is ±25 ppm/°C. Therefore, if the temperature coefficient and absolute accuracy of the external gain setting resistor, R_G, is known, the accuracy of the input gain stage can be calculated. This additional inaccuracy must be added to the gain error of the converter.

DIGITAL OUTPUT CODES

The 2S56 series of converters employs an offset binary output code, the null position of the LVDT being represented by the MSB being high and all other bits low. Representative digital output codes are shown in Figure 2. For the 2S54 (14-bit resolution), the two least significant bits are unused.

NOTE: A negative position is defined as being when the V1 and V_{REF} are out of phase. A positive position is when they are in phase.

OVERRANGE

The digital output code format shown in Figure 2 enables the user to determine if the LVDT has exceeded the negative or positive full-scale position and has gone into overrange. An indication of overrange can be obtained by performing an "exclusive OR" on Bits 1 and 2 (MSB and 2nd MSB). Alternatively this function can be performed in software.

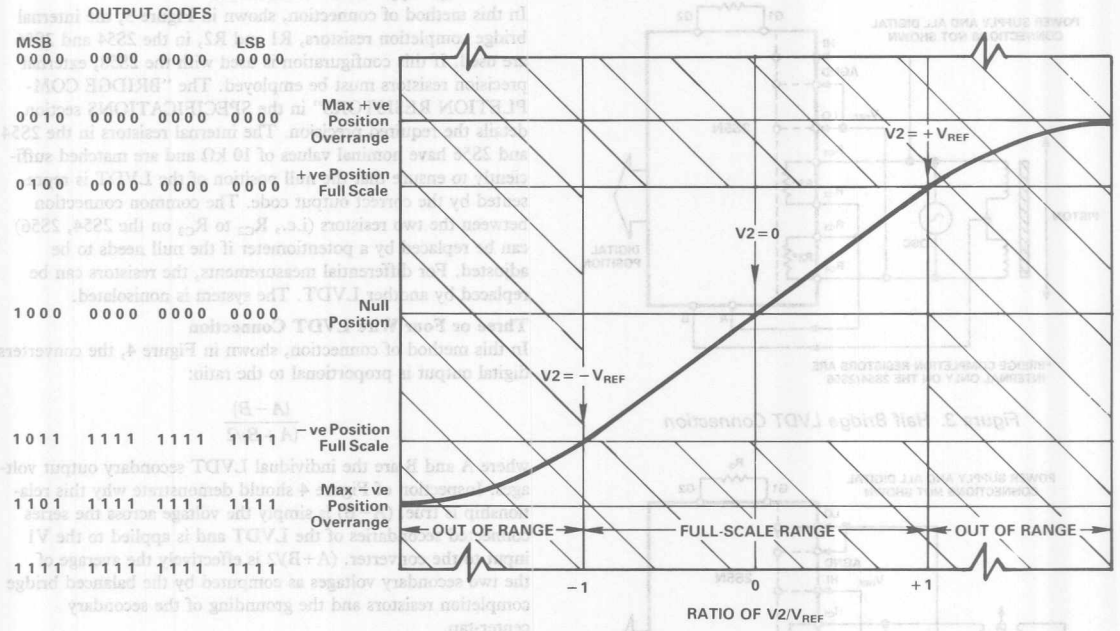


Figure 2. Output Code Format

PHASE SHIFT AND QUADRATURE EFFECTS

Reference to signal phase shift can be high in LVDTs, sometimes in the order of 70 degrees. If the converter is connected as in Figures 3 and 4, any effects due to this phase shift are minimized. This connection method, therefore, provides outstanding benefits.

The additional gain error caused by reference to signal phase shifts is given by:

$$(1 - cos\theta) \times 100\% \; of \; FSR$$

where

θ = phase shift between V_{REF} and V1.

When the phase shift between V_{REF} and V1 is zero, additional quadrature on the signal will have no effect on the converter. This is another benefit of the conversion method.

CONNECTING LVDTS

Since all input connections to 2S56 converters are truly differential, there is great flexibility in the input sensor connection configuration. Some of the various methods are shown in Figures 3, 4 and 5.

(It should be noted that a ground reference point should always be included and connected to either the V_{REF} or V1 inputs.)

It is suggested that decoupling capacitors be connected in parallel between the power supply lines ($+V_S$, $-V_S$, +5 V) and GND, adjacent to the converter. Suggested values are: 6.8 µF tantalum and 47 nF disc capacitors connected in parallel. When more than one converter is on a card, separate decoupling should be used for each converter, particularly the 47 nF capacitors.

The $+V_S$ and the $-V_S$ pins should be connected to dc power supplies of the appropriate polarity in the range of ±15 V ±5%. Care should be taken to ensure that the polarity can never become reversed. The +5 V pins should be connected to a +5 V ±5% dc supply. The +5 V supply must never be allowed to go negative with respect to ground.

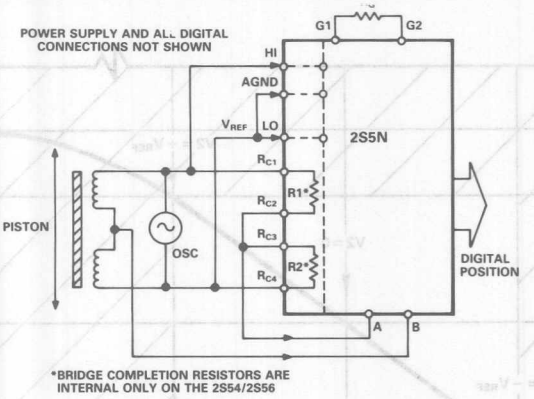


Figure 3. Half Bridge LVDT Connection

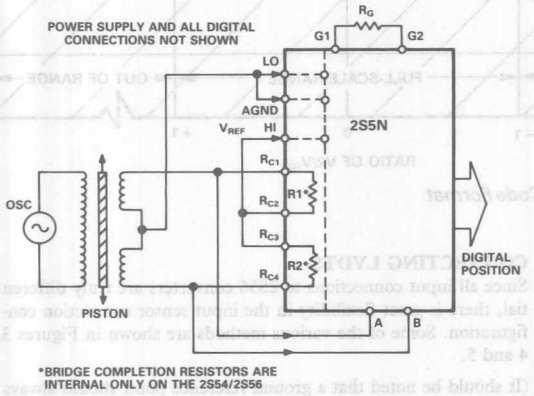


Figure 4. Three- or Four-Wire LVDT Connection

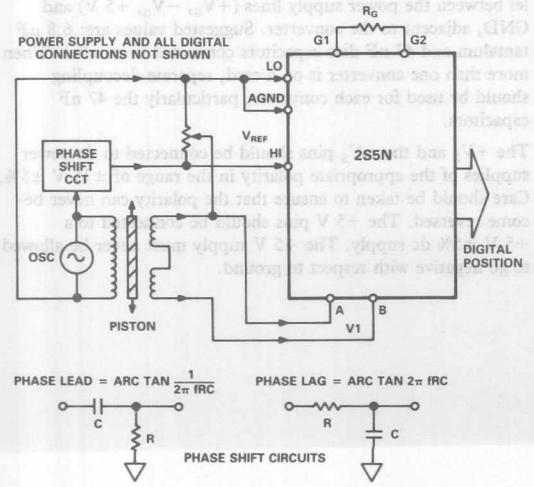


Figure 5. Two-Wire LVDT Connection

Half Bridge Type LVDT Connection

In this method of connection, shown in Figure 3, the internal bridge completion resistors, R1 and R2, in the 2S54 and 2S56 are used. If this configuration is used with the 2S58, external precision resistors must be employed. The "BRIDGE COMPLETION RESISTORS" in the SPECIFICATIONS section details the required precision. The internal resistors in the 2S54 and 2S56 have nominal values of 10 kΩ and are matched sufficiently to ensure that the null position of the LVDT is represented by the correct output code. The common connection between the two resistors (i.e., R_{C2} to R_{C3} on the 2S54, 2S56) can be replaced by a potentiometer if the null needs to be adjusted. For differential measurements, the resistors can be replaced by another LVDT. The system is nonisolated.

Three or Four Wire LVDT Connection

In this method of connection, shown in Figure 4, the converters digital output is proportional to the ratio:

$$\frac{(A-B)}{(A+B)/2}$$

where A and B are the individual LVDT secondary output voltages. Inspection of Figure 4 should demonstrate why this relationship is true. (A−B) is simply the voltage across the series connected secondaries of the LVDT and is applied to the V1 input to the converter. (A+B)/2 is effectively the average of the two secondary voltages as computed by the balanced bridge completion resistors and the grounding of the secondary center-tap.

Note: This method of connection is appropriate only for where (A+B) is a constant, independent of LVDT position. Any lack of constancy in (A+B) will be reflected as an additional non-linearity in the output. It is up to the user to determine if (A+B) is sufficiently constant over the particular stroke length employed. (A+B)/2 can be monitored on the "REF O/P" pin.

This method will usually restrict the usable LVDT range to half of its full range. The restriction can be eliminated, however, by attenuating V1 by a factor of 2 or increasing V_{REF} by a factor of 2.

This connection method has the tremendous advantage of being insensitive to temperature related phase shifts and excitation oscillator instabililty effects usually associated with more conventional LVDT conversion systems.

As in the case of the Half Bridge Type LVDT Connection, R1 and R2 are the bridge completion resistors (internal on the 2S54, 2S56; external on the 2S58) and are matched to a degree sufficient to ensure that the digital output representing the null position does not vary from the LVDT's natural null position. If null adjustment is required, a potentiometer can be used in place of the common connection between the two resistors.

Two-Wire LVDT Connection

This method should be used in cases where the sum of the LVDT secondary output voltages (A+B) is not constant with LVDT displacement over the desired stroke length. The method of connection, shown in Figure 5, still maintains the ratiometric operation and the insensitivity to variations in reference amplitude and frequency. However, the phase shift between V_{REF} and V1 should be minimized to maintain accuracy (see Section "PHASE SHIFT AND QUADRATURE EFFECTS"). Suggested phase compensation circuits are shown in Figure 5.

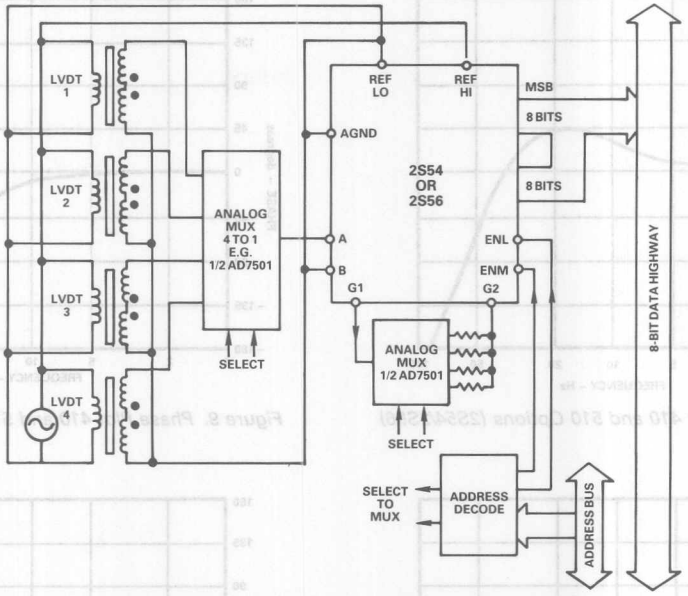


Figure 6. Multiplexing 4 LVDTs into the 2S54/2S56

MULTIPLEXING THE CONVERTERS

Although the 2S56 series of converters are primarily intended for use as single channel, continuous conversion devices, they can also be used in small multiplexed systems as shown in Figure 6. However, when switching between LVDT channels, ample time must be allowed for the converters to settle prior to transferring data.

Using the 2S54/X40 as in Figure 6 and allowing a time between samples of 70 ms, the maximum settling time of the converter can yield four 14-bit results from the 4 LVDTs in 280 ms. The gain can be programmed, as shown, to accommodate various transformation rations of dissimilar LVDTs. Note, however, that the finite "ON" resistance of the analog switch used with the gain setting resistor can introduce gain inaccuracies. This error is minimized for lower gains as the "ON" resistance of the switch will be negligible compared to the gain setting resistor. The error introduced can be calculated from the equation for the preamplifier gain in the "INPUT GAIN" section.

SCALING THE INPUTS

In cases where there is a requirement for a particular LVDT stroke length to correspond to full-scale on the digital output, the input gain must be chosen accordingly. It is important to remember that it is the relationship between V2 and V_{REF}, not V1 and V_{REF}, which determines the full-scale digital output. Furthermore, it should be ensured that these voltages are each 2 V rms ±10%, respectively. For monitoring purposes, V2 is brought to the "DIFF O/P" pin and V_{REF} is brought to the "REF O/P" pin.

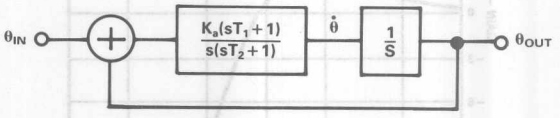


Figure 7. Transfer Function

DYNAMIC PERFORMANCE

The transfer function of the converters, shown in Figure 7 is given by:

Open Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1+sT_1}{1+sT_2}$$

Closed Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{1+sT_1}{1+sT_1+s^2/K_a+s^3T_2/K_a}$$

where:

	k_a	T1	T2
2S54/56 X10 options	12000 sec^{-2}	14.7 ms	2.3 ms
2S54/56 X40 options	93600 sec^{-2}	5.9 ms	1.0 ms
2S58	450000 sec^{-2}	2.4 ms	0.4 ms

The gain and phase response of each of the three options is shown in Figures 8, 9, 10, 11, 12 and 13.

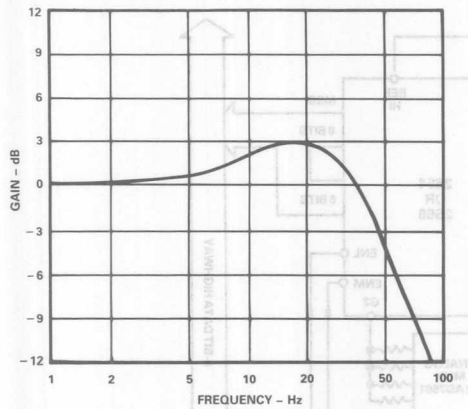


Figure 8. Gain Plot 410 and 510 Options (2S54/2S56)

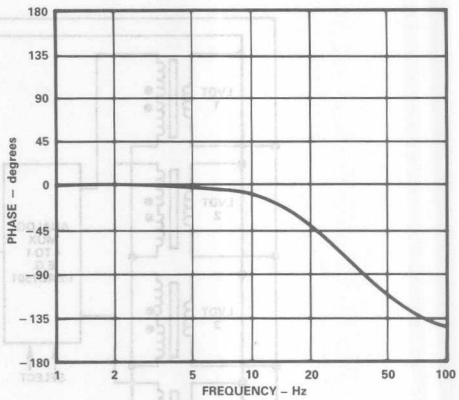


Figure 9. Phase Plot 410 and 510 Options (2S54/2S56)

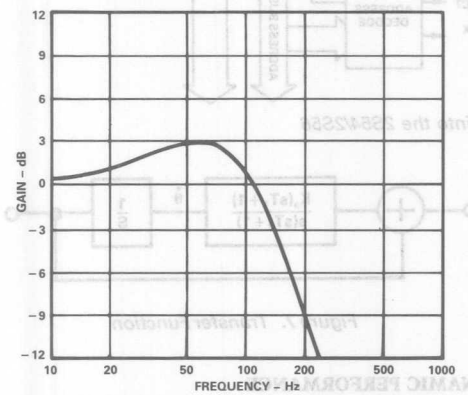


Figure 10. Gain Plot 440 and 540 Options (2S54/2S56)

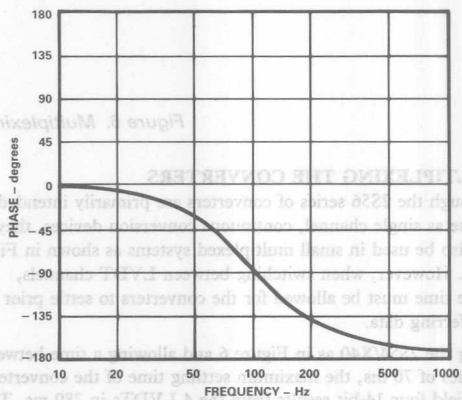


Figure 11. Phase Plot 440 and 540 Options (2S54/2S56)

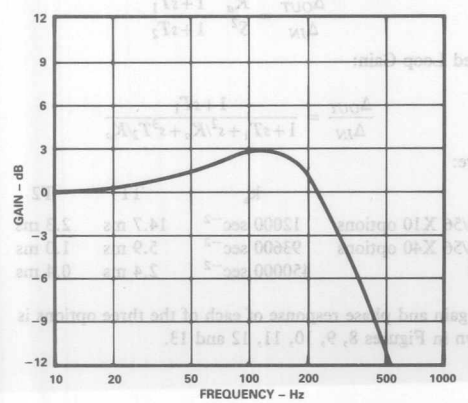


Figure 12. Gain Plot for 2S58

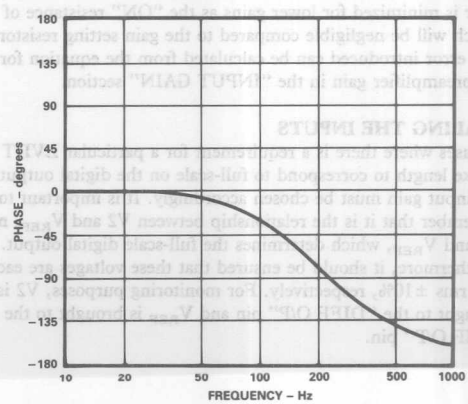


Figure 13. Phase Plot for 2S58

ACCELERATION ERROR

Tracking converters such as the 2S56 series, employing a type 2 servo loop, do not suffer any velocity lag. However, there is an additional error when the LVDT is undergoing periods of acceleration.

The additional error can be defined using the K_a constant of the converter (see DYNAMIC PERFORMANCE section) as follows:

$$K_a = \frac{\textit{Input acceleration}}{\textit{Error in output position}}$$

where the numerator and the denominator are defined in the same units.

K_a does not define the maximum acceleration, only the error due to the acceleration.

DATA TRANSFER

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, due to a change in displacement of the LVDT, the signal appearing on the converter's BUSY output pin is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the equivalent of an LSB and the internal up-down counter is incremented or decremented.

With the INHIBIT input pin in the "Hi" state, data will be transferred automatically to the output latches.

The two three-state enable inputs, ENABLE L and ENABLE M, allow the digital input to be transferred on to a data bus in two separate bytes. ENABLE M enables the most significant 8 bits of the output word while ENABLE L enables the remaining least significant bits.

Figure 14 shows the timing diagram.

There are two methods of transferring the output data. The first is to detect the state of the "BUSY" which is 'Hi" for 1 μs max and then transfer the data when the BUSY is "Lo". Both INHIBIT, ENABLE M and ENABLE L must be in their correct state of "Hi" and "Lo" respectively, in order that the data is presented to the output.

The alternative method is to use the INHIBIT input. Taking this input to a "Lo" state prevents the internal monostable circuits being triggered and consequently the latches being updated. Data will always be valid 1 μs after the application of a logic "Lo" to the INHIBIT. However, if INHIBIT is applied while BUSY is in the "Lo" state (with ENABLE M and ENABLE L also "Lo"), data is valid instantaneously.

The internal tracking operation of the converter cannot in any way be affected by the logic state present on either the INHIBIT or the ENABLE pins.

OTHER INPUTS AND OUTPUTS

Differential Output (DIFF O/P)

This signal is in fact V2 and is brought out to a pin in order to simplify scaling of the V1 signal.

Direction (DIR)

This TTL output signal indicates the direction of the transducer. It is a logic "Hi" when counting up and a logic "Lo" when counting down.

Reference Output (REF O/P)

This is the reference signal after the input buffer stage. It can be used as a single ended measurement point for the V_{REF} input.

It can also be used as a BITE (Built in Test Equipment) signal to detect if the LVDT has become disconnected or the reference supply has failed.

SUPPORT OSCILLATOR

A power oscillator, OSC1758, is available for use as a reference generator for LVDT and RVDT transducers. It is capable of providing up to 7 volts rms at 1.4 VA.

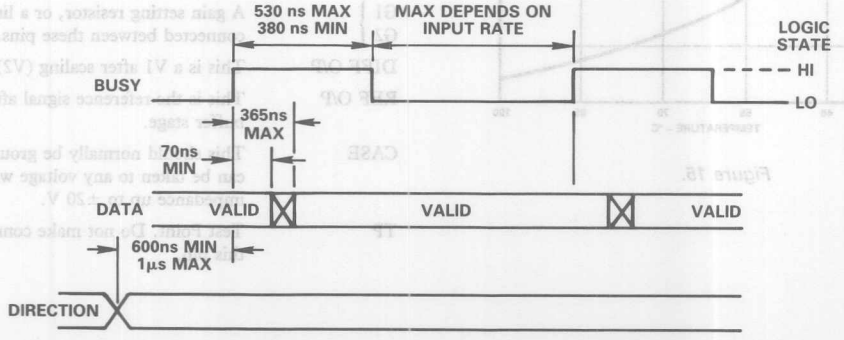
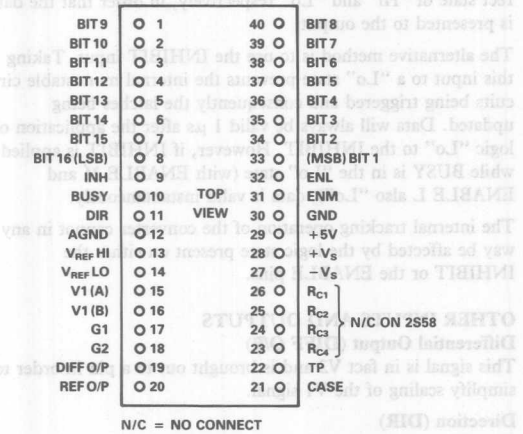


Figure 14. 2S56 Data Transfer Timing Diagram



N/C = NO CONNECT

MEAN TIME BETWEEN FAILURES (MTBF)

The predicted reliability of these converters is exceptionally high due to the extensive uses of LSI custom circuitry. Figure 15 shows the MTBF of the 4YZ options as calculated according to MIL HDBK 217D at various temperatures under ground benign environment. For MTBF calculations under other environments, please consult the factory.

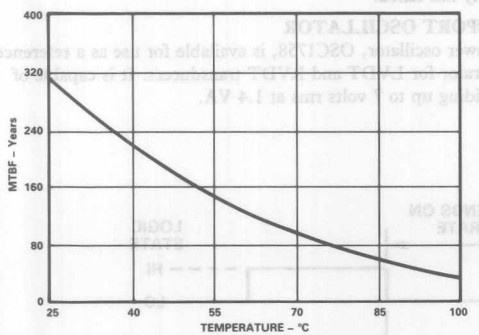


Figure 15.

$-V_S$	Main negative power supply.
$+V_S$	Main positive power supply.
+5 V	Logic power supply.
GND	Power supply ground. Digital ground.
Bit 1–14 (2S54) Bit 1–16	Parallel output data bits. (2S56, 2S58))
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi."
$\overline{\text{ENABLE M}}$	The 8 most significant output data bits are set to a high impedance state by application of a logic "Hi."
$\overline{\text{ENABLE L}}$	The 6 least significant bits of a 2S54, or the 8 least significant bits of a 2S56 "and 2S58," are set to a high impedance state by application of a logic "Hi."
R_{C1} R_{C2}	Connections to R1, internal bridge completion resistor (2S54/2S56 only).
R_{C3} R_{C4}	Connections to R2, internal bridge completion resistor (2S54/2S56 only).
DIR	TTL output indicating the direction of movement of the transducer.
AGND	Analog ground.
V_{REF} HI V_{REF} LO	Input pins for the Reference signal.
V1 (A) V1 (B)	Input pins for the Signal.
G1 G2	A gain setting resistor, or a link, can be connected between these pins.
DIFF O/P	This is a V1 after scaling (V2).
REF O/P	This is the reference signal after the input buffer stage.
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ±20 V.
TP	Test Point. Do not make connections to this pin.

receive the following processing:

Process	Condition
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	In-House Criteria
3. Seal Test, Fine and Gross	In-House Criteria
4. Final Electrical Test	

Extended temperature range versions receive additional processing as follows:

4. Final Electrical Test	Performed at Maximum and Minimum Operating Temperatures

PROCESSING FOR HIGH RELIABILITY

All extended temperature range models are available with high reliability screening. The parts are identified with a B suffix, and will receive the following processing.

Process	Conditions
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	MIL-STD-883, Method 2017
3. Temperature Cycling	10 Cycles, −65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 Hours at +125°C
7. Seal Test, Fine and Gross	MIL-STD-883, Method 1014
8. Final Electrical Testing (Group A)	Performed at T_{min}, T_{AMB}, and T_{max}
9. External Visual Inspection	MIL-STD-883, Method 2009

NOTE: Test and screening data can be supplied. Further information on request.

2S50	Digital Converter (Monolithic IC)
	10 Bit + Sign, LVDT to Digital Converter (Hybrid)
OSC1758	Power Oscillator (Hybrid)
IPA1764	Inductosyn Pre-Amplifier (Hybrid)

3

ORDERING INFORMATION

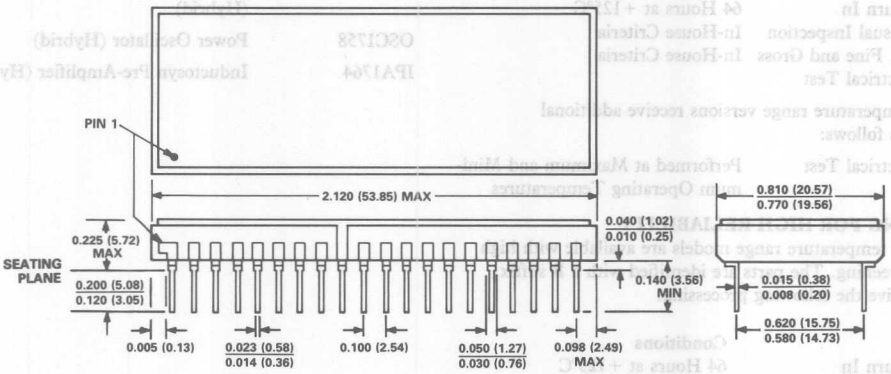
2S5N/ X Y 0 B

- B — High Reliability Process
- Y = 1 — 50 Hz Bandwidth (2S54, 2S56 Only) (Ref 360 Hz–5 kHz)
- Y = 4 — 140 Hz Bandwidth (2S54, 2S56 Only) (Ref 1 kHz–5 kHz)
- Y = 0 — 300 Hz Bandwidth (2S58 Only)
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range
- N = 4 — 14-Bit Binary
- N = 6 — 16-Bit Binary
- N = 8 — 16-Bit Binary High Precision

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

40-Pin Bottom Brazed Ceramic DIP (DH-40A)



Communications Products
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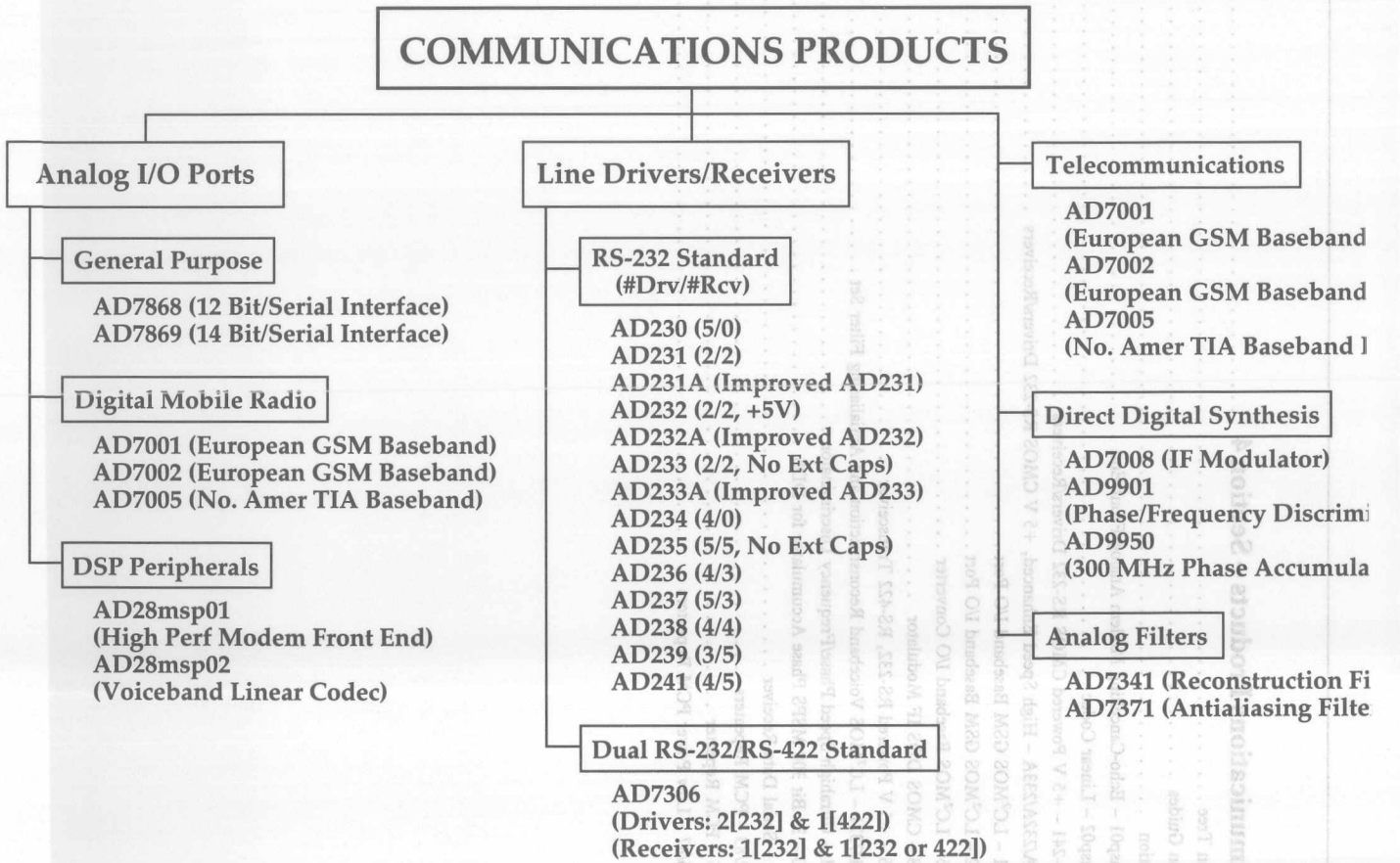
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4

Selection Tree
Communications Products



Selection Guide
Communications Products

Analog I/O Ports

Model	DAC/ADC Resolution Bits	DAC/ADC SNR + THD dB	Through-put kSPS	Ref. Volt Int/Ext	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
*AD7001	10/8	56/44	2170	2.5 V, Int	10, 8, Serial, µP	10	C[3]	C I 4–47	GSM Baseband I/O Port
*AD7002	10/12	—/62	4333 (DAC) 541.7 (ADC)	2.5 V, Int	Serial, µP	10	C[3]	C I 4–59	GSM Baseband I/O Port with On-Board GMSK Modulation
*AD7005	10/12	—/62	97.2 (DAC) 194.4 (ADC)	2.3 V, Int	Serial, µP	10	C[3]	C I 4–75	TIA Baseband I/O Port
*AD7868	12/12	72/72	83	3.0 V, Int	Serial, µP	2, 3, 6	I, M	C II 8–79	Complete 12-Bit Analog I/O System
*AD7869	14/14	78/78	83	3.0 V, Int	Serial, µP	2, 3, 6	I, M	C II 8–95	Complete 14-Bit Analog I/O System
*AD28msp02	16/16	65/65	8	2.5 V, Int	Serial, µP	6	C	C I 4–25	Complete Voice Band Linear Codec with On-Chip Filtering
*AD28msp01	16/16	80/80	7.2/8.0/9.6	2.5 V, Int	Serial, µP	6	C	C I 4–9	Complete Analog Front End for High Performance DSP-Based Modems

Analog Filters

Model	SNR (typ) dB	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
AD7341	75	Parallel, µP	2, 5	C	C I 4–99	Voiceband Reconstruction Filter
AD7371	75	Parallel, µP	2, 5	C	C I 4–99	Voiceband Antialiasing Filter

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]Operates to −25°C.
*Boldface type: Product recommended for new design.
*New product since the publication of the most recent Databooks.

Selection Guide
Communications Products

Direct Digital Synthesis

Model	Bus Interface	Package Options[1]	Temp Range[2]	Comments	Page
*AD7008	8/16 µP	10	C[3]	DDS IF Modulator with 32-Bit Phase Accumulator and 10-bit DAC, 20 MHz Output Capability, Single 5 V Supply, Low Power	C I 4–91
AD9901		3, 4, 5	C, M	Ultrahigh Speed Digital Phase/Frequency Discriminator, No "Dead Zone," Linear Transfer Function up to 200 MHz	C I 4–115
*AD9950	8/16 µP	14	C, M	32-Bit, 300 MSPS Phase Accumulator for DDS, On-Board Quad Logic	C I 4–123

Telecommunications

Model	Description	Package Options[1]	Temp Range[2]	Page
LIU-01	Serial Data Receiver Reconstructs Clock and Data	2, 3, 6	I	C I 4–135
RPT-82	T1/E1 PCM Repeater Featuring Automatic ALBO	3, 6	I	C I 4–147
RPT-83	T1/E1 PCM Repeater with ALBO and Clock Shutdown Circuit	3, 6	I	C I 4–147
RPT-85	T1/E1 PCM Repeater with XR-T445 Pinout	3, 6	I	C I 4–155
RPT-86	T1/E1 Low Power PCM Repeater with ALBO	2, 3, 6	I	C I 4–163
RPT-87	T1/E1 Low Power PCM Repeater with ALBO and Clock Shutdown Circuit	2, 3, 6	I	C I 4–163

Line Drivers/Receivers

Model	Power Supply Voltage	No. of Drivers	No. of Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins	Package Options[1]	Temp Range[2]	Page
***AD230**	**+5 V**	**5 (232)**	**0**	**4**	**Yes**	**No**	**20**	**2, 3, 6**	**C, I**	**C I 4–29**
***AD231**	**+5 V & 7.5 V to 13.2 V**	**2 (232)**	**2 (232)**	**2**	**No**	**No**	**14**	**2, 3, 6**	**C, I, M**	**C I 4–29**
***AD231A**	**+5 V & 7.5 V to 13.2 V**	**2 (232)**	**2 (232)**	**2**	**No**	**No**	**14**	**2, 3, 6**	**C, I, M**	**C I 4–41**
***AD232**	**+5 V**	**2 (232)**	**2 (232)**	**4**	**No**	**No**	**16**	**2, 3, 6**	**C, I, M**	**C I 4–29**
***AD232A**	**+5 V**	**2 (232)**	**2 (232)**	**4**	**No**	**No**	**16**	**2, 3, 6**	**C, I, M**	**C I 4–41**
***AD233**	**+5 V**	**2 (232)**	**2 (232)**	**None**	**No**	**No**	**20**	**2**	**C, I**	**C I 4–29**
***AD233A**	**+5 V**	**2 (232)**	**2 (232)**	**None**	**No**	**No**	**20**	**2**	**C, I**	**C I 4–41**
***AD234**	**+5 V**	**4 (232)**	**0**	**4**	**No**	**No**	**16**	**2, 3, 6**	**C, I**	**C I 4–29**
***AD235**	**+5 V**	**5 (232)**	**5 (232)**	**None**	**Yes**	**Yes**	**24**	**2, 3**	**C, I**	**C I 4–29**
***AD236**	**+5 V**	**4 (232)**	**3 (232)**	**4**	**Yes**	**Yes**	**24**	**2, 3, 6**	**C, I, M**	**C I 4–29**
***AD237**	**+5 V**	**5 (232)**	**3 (232)**	**4**	**No**	**No**	**24**	**2, 3, 6**	**C, I**	**C I 4–29**
***AD238**	**+5 V**	**4 (232)**	**4 (232)**	**4**	**No**	**No**	**24**	**2, 3, 6**	**C, I, M**	**C I 4–29**
***AD239**	**+5 V & 12 V**	**3 (232)**	**5 (232)**	**2**	**No**	**Yes**	**24**	**2, 3, 6**	**C, I, M**	**C I 4–29**
***AD241**	**+5 V**	**4 (232)**	**5 (232)**	**4**	**Yes**	**Yes**	**28**	**6**	**C, I**	**C I 4–29**
***AD7306**	**+5 V**	**2 (232)**	**1 (232)**	**4**	**No**	**No**	**24**	**6**	**C, I**	**C I 4–93**
		1 (422)	**1 (232/422)**							

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[3]Operates to −25°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Orientation
Communications Products

Analog Devices produces a wide range of products serving the needs of the communications industry. Our product portfolio contains devices designed for such applications as digital mobile radio, radar, telecommunications, LANs, and other serial data transmission applications. A brief description of our communications product portfolios along with their respective applications is given below.

ANALOG I/O PORTS

The Analog I/O Ports product portfolio displayed in this section contains application specific devices used in telecommunication and digital mobile radio applications. The AD7001, AD7002, are baseband modulators designed specifically to meet the requirements of the European Groupe Speciale Mobile (GSM) digital cellular telephone system. The AD7005 meets the requirements of the North American Telecommunications Industries Association (TIA) standard for its digital cellular telephone system.

The AD7001 provides two 10-bit DACs and filters to generate a Gaussian Minimum Shift Keyed (GSMK) modulated bit-stream at 220 Kbits/sec. This modulated bit-stream is guaranteed to meet the requirements of the GSM specification. The receive channel provides an IQ amplifier, a programmable gain amplifier and a sample-and-hold circuit mixing for necessary signal preconditioning. The circuit features independent shutdown control of the transmit and receive functions for low power operation and also includes an 8-bit DAC for control of functions such as AFC or AGC.

The AD7002 is also designed for GSM but includes the ROM and logic to produce the GMSK modulated digital inputs to the DACs. The transmit path consists of an on-board ROM, and two high accuracy, fast 10-bit DACs with output reconstruction filters. The receive path is composed of two high performance sigma-delta ADCs with digital filtering. Three control DACs ranging from 8- to 10-bit accuracy are also included for AFC, AGC, and carrier signal shaping functions. The device also features power shutdown capabilities.

The AD7005 is designed for the North American TIA standard. It features two 10-bit transmit DACs and filtering required for the TIA standard. Two sigma-delta 12-bit ADCs are provided for the receive channel along with digital FIR filtering. Three auxiliary DACs are also provided. This device also has power shutdown capabilities.

The AD28msp01 is a complete analog front-end for high performance modems and the AD28msp02 is a voiceband codec providing a complete analog front end for high performance voiceband DSP applications. Both devices have similar architectures and contain a 16-bit sigma-delta ADC and DAC with on-chip antialiasing and smoothing filters.

The AD7868 and AD7869 are 12- and 14-bit 83 kSPS I/O ports designed for modems and other communications equipment. Both devices provide simple interfaces to the serial ports of standard DSP processors such as the ADSP-2101 and are fully specified in terms of ac and dc performance. Both devices have an analog input/output range of ±3 V and have low power consumption (130 mW typical).

The specifications pertaining to the Analog I/O Ports are similar to the ADC and DAC specifications, and the definitions to these specifications may be found in the orientation segments of each respective product section.

VOICEBAND FILTERS

The AD7341 and AD7371 are a switched capacitor voiceband reconstruction and antialiasing filter chipset, respectively. These devices are designed to be used in conjunction with the AD7871/AD7872 and AD7840 14-bit A/D and D/A converters or the 14-bit AD7869 analog I/O port to form a complete analog front-end for voiceband DSP applications. This chipset substitutes for discrete active filters and/or digital filtering used on high performance DSP front-ends thus reducing design time, component cost, and PCB real estate. Specifications along with definitions are provided on the data sheets.

DIRECT DIGITAL SYNTHESIS/PHASE LOCK LOOP

The AD7008 and AD9950 are designed for direct digital synthesis (DDS) applications used for dynamic sine waveform synthesis. The AD7008 is a numerically controlled oscillator employing a 32-bit phase accumulator and a 10-bit DAC integrated on a single CMOS chip. The device is capable of phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for SSB generation. Clock rates up to 50 MHz are supported, thus providing for usable analog outputs up to about 20 MHz. The AD9950 is a 32-bit, 300 MHz phase accumulator used as a building block for higher speed DDS applications. This device supports DDS applications using clock rates between 100 MHz and 300 MHz. The AD9901 is a digital phase/frequency discriminator used in phase-lock loop applications and is capable of directly comparing phase/frequency inputs up to 200 MHz. Specifications along with definitions are provided on the data sheets.

SERIAL COMMUNICATIONS

The AD232 family of parts consists of low power, high performance driver/receiver products for the RS-232 transmission standard. The parts are designed to meet the requirements of EIA-232-C, EIA-232-D and CCITT V.28. The AD231, AD232, AD233 support the basic RTS-CTS and XON-XOFF protocols, while the AD230, AD234, AD235, AD236, AD237, AD238, AD239 and AD241 provide a selection of different receiver and driver combinations that can be used to implement a wide variety of interface types. The AD241 is particularly suited to the standard PC serial interface. This part has been designed to meet the specific needs of a PC environment and provides ample driver current to directly drive a mouse.

The AD231A, AD232A, AD233A are enhanced pin-compatible versions of the AD231, AD232, and AD233 offering 116 Kbaud operation while using 0.1 μF charge pump capacitors.

The parts feature single 5 V supply operation and low operating current. A selection of features including tri-stateable outputs, on-board capacitors and a 1 μA shutdown mode are available. On-board slew rate control ensures compliance to the standards with no requirement for external slew rate control capacitors. Under power-off conditions, driver output impedance is greater than 300 ohms and the receivers are designed to reject any noise impulses on the line that are faster than about 1 μs.

The AD7306 is a multiprotocol driver that supports both RS-232 and RS-422 standards. This is the industry's first single 5 V supply, multiprotocol part. It operates on-board-saving 0.1 μF capacitors and provides RS-422 transmission rates up to 10 MHz. It also features very low output driver skew.

TELECOMMUNICATIONS

Our repeater and receiver line of communications products serves the needs of the serial data transmission networks used in telecommunications and LANs. These products perform the difficult interfacing function between the analog nature of a transmission line and the digital world of the microprocessor. The repeater products regenerate data which has been attenuated and distorted along the transmission line and retransmit the information synchronized to the original clock rate. The receiver products terminate the transmission line and separate the incoming clock and data information into microprocessor-compatible signals. Both are compatible with NRZ and RZ data transmissions, and both operate transparent to data formatting.

The RPT-82/RPT-83 are monolithic PCM repeaters used to regenerate alternate-mark-inversion pulses in PCM carrier systems at T1 (1.544 Mbps) and T148 (2.048 Mbps) data rates. These repeaters contain a high gain preamplifier and ALBO circuitry to achieve over 40 dB of input signal dynamic range. RPT-86/RPT-87 are next generation PCM repeaters similar to the RPT-82/RPT-83 with many additional performance enhancements. These repeaters operate from a single 5.6 V supply and are compatible with T1, T148, and the higher data rate T1C (3.152 Mbit) systems. The RPT-86/RPT-87 both contain dual ALBO ports for an increased dynamic range of over 50 dB. They also exhibit greatly improved stability versus temperature and supply voltage fluctuations. Both the RPT-83 and RPT-87 also contain a clock shutdown function to prevent the transmission of false data when the incoming signal falls below a usable level.

The LIU-01 is a versatile serial data receiver. It also contains dual ALBO ports for over 60 dB of dynamic range and operates at data rates from 300 bps to over 6 Mbps. Unlike the repeaters, the LIU-01 presents both data and clock as TTL-CMOS compatible outputs. It also outputs a LOSS OF CARRIER signal indicating that the incoming signal has fallen below a usable level.

DEFINITIONS OF SPECIFICATIONS (REPEATER/RECEIVER PRODUCTS)

ALBO Diode Impedance—The small-signal impedance of the ALBO diode measured from the ALBO input to ground. The ac impedance is the parallel combination of two diode-connected transistors and approximately 3 pF of stray capacitance. The impedance of the transistors is inversely proportional to the current flowing through them, $R_D = 13/I_D$, where R_D is the ALBO diode impedance in ohms and I_D is the ALBO diode current in mA.

ALBO Threshold—The differential voltage, measured between the preamp outputs, that is required to activate the internal peak detector which drives current through the ALBO diodes.

AMI—Alternate Mark Inversion. A form of digital signal transmission where each successive 1-bit is of opposite polarity.

Automatic Line Build Out, ALBO—An automatic-gain-control circuit which operates by simulating the attenuation and frequency distortion of an extension of the transmission line.

Bipolar Violation, BPV—The transmission of two consecutive pulses of the same polarity.

Bit Error Rate, BER—A count of the errored data bits received per second of transmission.

Clock Threshold—The differential voltage, measured between the preamp outputs, that is required to activate the clock synchronization circuitry.

Data Threshold—The differential voltage, measured between the preamp outputs, that is required to activate the data detection circuitry.

Equalizing Network—A network which compensates for the attenuation and frequency response of the transmission cable over the operating bandwidth.

Eye Pattern—The trace obtained on an oscilloscope by viewing a serial data receiver's/repeater's preamplifier output while receiving a QRSS input signal.

Interference Margin—The ratio of the signal amplitude to the maximum noise amplitude that a system can tolerate without errors. Interference Margin = 20 Log (S/N) dB.

Loss of Carrier, LOC—An output indicating that the incoming signal has fallen below a usable level. This signal is active low.

Maximum Density—An input signal pattern consisting of all 1s.

Minimum Density—For T1 format, this is a repeating signal pattern consisting of two 1s followed by fourteen 0s.

Oscillator Bias Voltage—A dc level used to set the center point of an LC oscillator tank's operation.

Output-Pulse Rise (Fall) Time—Measured from the 10% to 90% points.

Output-Pulse-Width Differential—In a T1 carrier system, a typical transmitted data pulse width is 324 ns. The pulse-width differential is the difference in pulse width of two successive outputs.

Preamplifier Bandwidth—3 dB bandwidth of the preamplifier circuit.

Quasi-Random Signal Source, QRSS—A signal consisting of random 1s and 0s.

RCLK—Received clock data extracted from the incoming data signal.

RNEG—Received data extracted from negative incoming signal levels.

RPOS—Received data extracted from positive incoming signal levels.

Echo-Cancelling Modem Analog Front End

AD28msp01

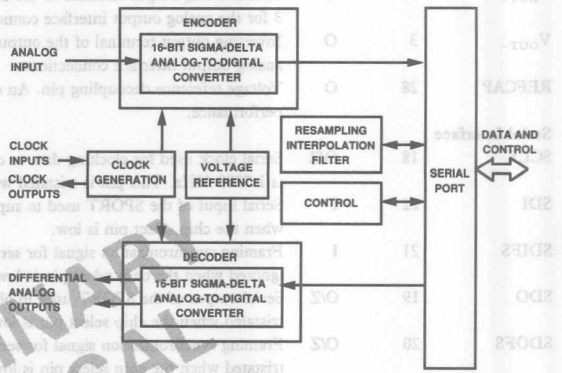
FEATURES

- 16-Bit Sigma-Delta A/D Converter
- 16-Bit Sigma-Delta D/A Converter
- 80-dB SNR and THD
- Linear Phase Antialias and Anti-Image Filters
- Digital Resampling/Interpolation Filter
- On-Chip Voltage Reference
- 7.2 kHz, 8.0 kHz, and 9.6 kHz Sampling Rates
- 8/7 Mode for 8.23 kHz, 9.14 kHz, and 10.97 kHz Sampling
- Synchronous and Asynchronous DAC/ADC Modes
- Bit and Baud Clock Generation
- Transmit Digital Phase-Locked Loop for Terminal Synchronization
- Independent Transmit and Receive Phase Adjustment
- DSP-Compatible Serial Port
- Single +5 V Supply with Power-Down Mode
- 28-Pin DIP

APPLICATIONS

- High Performance DSP-Based Modems
  V.32ter, V.32bis, V.32, V.22bis, V.22, V.21, Bell 212A, 103
- Fax and Cellular-Compatible Modems
  V.33, V.29, V.27ter, V.27bis, V.27, V.26bis
- Integrated Fax, Modem, and Speech Processing

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

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GENERAL DESCRIPTION

The AD28msp01 is a complete analog front end for high performance DSP-based modems. The device includes all data conversion, filtering, and clock generation circuitry needed to implement an echo-cancelling modem with one companion digital signal processor. Software-programmable sample rates and clocking modes support all established modem standards.

The AD28msp01 utilizes advanced sigma-delta technology to move the entire echo-cancelling modem implementation into the digital domain. The device maintains 80 dB SNR and THD throughout all filtering and data conversion. Purely DSP-based echo cancellation algorithms can thereby maintain robust bit error rates under worst case signal attenuation and echo amplitude conditions. The AD28msp01's on-chip interpolation filter resamples the received signal after echo cancellation in the DSP, freeing the processor for other voice or data communications tasks.

On-chip bit and baud clock generation circuitry allows either synchronous or asynchronous operation of the transmit (DAC) and receive (ADC) paths. Each path features independent phase advance and retard adjustments via software control. The AD28msp01 can also synchronize modem operation to an external terminal bit clock.

Packaged in a 28-pin DIP, the AD28msp01 provides a compact solution for space-constrained environments. The device operates from a single +5 V supply and offers a low power sleep mode for battery-powered systems.

A detailed block diagram of the AD28msp01 is shown in Figure 1.

The following abbreviations are used in this data sheet:

DAC—Digital-to-Analog Converter
ADC—Analog-to-Digital Converter
SPORT—Serial Port
soft reset—in a soft reset, the AD28msp01 is reset but the control register values do not change.

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PIN DESCRIPTION

Name	Pin #	Type	Description
Analog Interface			
V_{IN}	27	I	Inverting terminal of the input amplifier to the receiver (ADC). Refer to Figure 2 for the analog input interface connections.
V_{FB}	26	O	Feedback terminal of the input amplifier to the receiver. Refer to Figure 2 for the analog input interface connections.
V_{OUT+}	2	O	Noninverting output terminal of the output differential amplifier, from the transmitter (DAC). Refer to Figure 3 for the analog output interface connections.
V_{OUT-}	3	O	Inverting output terminal of the output differential amplifier from the transmitter. Refer to Figure 3 for analog output interface connections.
REFCAP	28	O	Voltage reference decoupling pin. An external 0.1 μF capacitor is recommended on this pin for optimum noise performance.
Serial Interface			
SCLK	18	O/Z	Serial clock used for clocking data or control bits to/from the serial port (SPORT). The frequency of this clock is 1.7280 MHz. This pin is tristated when the chip select pin is low.
SDI	22	I	Serial input of the SPORT used to supply data or control information to the AD28msp01. This pin is ignored when the chip select pin is low.
SDIFS	21	I	Framing synchronization signal for serial data transfers to the AD28msp01 (via the SDI pin). This pin is ignored when the chip select pin is low.
SDO	19	O/Z	Serial output of the SPORT used to obtain data or control information from the AD28msp01. This pin is tristated when the chip select pin is low.
SDOFS	20	O/Z	Framing synchronization signal for serial data transfers from the AD28msp01 (via the SDO pin). This pin is tristated when the chip select pin is low.
Clock Generation			
TSYNC	7	I	Transmit Synchronization Clock. This signal is used to synchronize the transmit clocks and the converter clocks to an external terminal/bit-rate clock. It is used in the V.32 TSYNC and asynchronous TSYNC modes and is ignored in other operating modes. The frequency of the external clock must be programmed in Control Register 0. This pin must be tied high or low if it is not being used.
TBIT	9	O	Transmit Bit Rate Clock. This is an output clock whose frequency is programmable via Control Register 3. It is synchronized to the TCONV clock.
TBAUD	10	O	Transmit Baud Rate Clock. This is an output clock whose frequency is programmable via Control Register 3. It is synchronized to the TCONV clock.
TCONV	8	O	Transmit Conversion Clock. This clock indicates when the ADC has finished a sampling cycle. The frequency of TCONV is programmed by setting the sample rate field in Control Register 0. The programmed TCONV rate can be scaled by a factor of 8/7 by setting Bit 9 in Control Register 1. The phase of TCONV can be adjusted by writing the Transmit Phase Adjust Register.
RBIT	12	O	Receive Bit Rate Clock. This is an output clock whose frequency is programmable via Control Register 2. It is synchronized to the RCONV clock.
RBAUD	13	O	Receive Baud Rate Clock. This is an output clock whose frequency is programmable via Control Register 2. It is synchronized to the RCONV clock.
RCONV	11	O	Receive Conversion Clock. This clock indicates when the DAC has finished a sampling cycle. The frequency of RCONV is programmed by setting the sample rate field in Control Register 0. The programmed RCONV rate can be scaled by a factor of 8/7 by setting Bit 9 in Control Register 1. The phase of RCONV can be adjusted by writing the Receive Phase Adjust Register.
Miscellaneous			
MCLK	14	I	AD28msp01 Master Clock Input. The frequency of this clock must be exactly 13.824 MHz to guarantee the correct frequency response for the device's digital filters.
$\overline{\text{RESET}}$	6	I	Active-Low Chip Reset. This signal sets all AD28msp01 control registers to their default values and clears the device's digital filters. SPORT output pins are tristated when $\overline{\text{RESET}}$ is active. SPORT input pins are ignored when $\overline{\text{RESET}}$ is active.
CS	23	I	Active-high chip select. This signal tristates all SPORT output pins and forces the AD28msp01 to ignore all SPORT input pins. Note that the AD28msp01's ADC, DAC, and digital filters continue operating when CS is de-asserted.
Power Supplies			
V_{DDA}	1		Analog Supply Voltage (Nominally +5 V).
GNDA	4, 25		Analog Ground.
V_{DDD}	16, 17		Digital Supply Voltage (Nominally +5 V).
GNDD	5, 15, 24		Digital Ground.

PRELIMINARY TECHNICAL DATA

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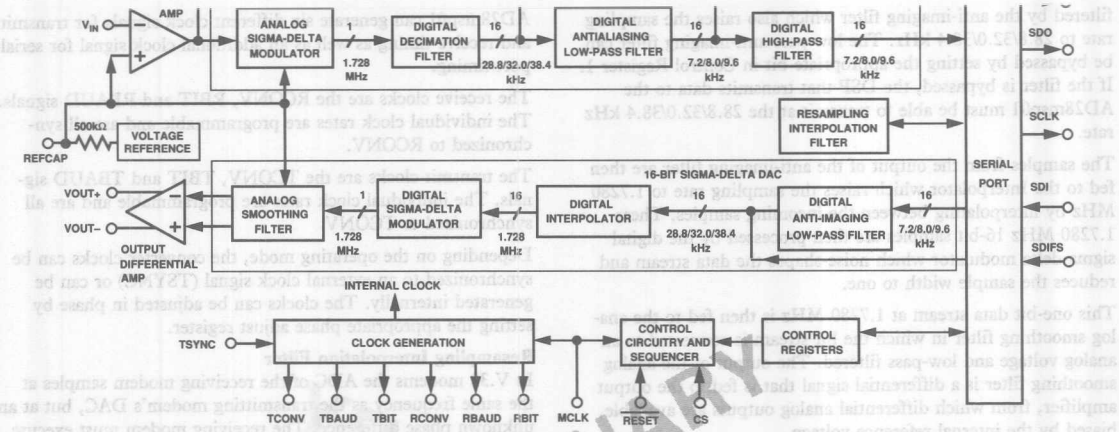


Figure 1. AD28msp01 Block Diagram

PRELIMINARY TECHNICAL DATA

FUNCTIONAL DESCRIPTION

ADC

The analog input is applied to the input amplifier via external gain setting resistors (see Figure 2, which can be found on the following page). The output of this amplifier, now biased by the on-chip voltage reference, is applied to an analog sigma-delta modulator which noise-shapes it and produces 1-bit samples at a 1.7280 MHz rate. The spectral content of this bit stream is noise-shaped such that in-band noise supports 80-dB SNR. Out-of-band noise is rejected in subsequent filtering.

This bit stream is fed to a decimation filter which has a Sinc^4 transfer function. The output of this decimation filter consists of a parallel data stream with a reduced sampling rate of 28.8 kHz, 32.0 kHz or 38.4 kHz (depending on the input sample rate), which is now processed by the digital antialiasing low-pass filter. This filter low-pass filters the data stream and further reduces the sampling rate by a factor of four. Finally the high-pass filter removes input frequency components at the low end of the spectrum.

Either the high-pass filter alone or the high-pass/low-pass filter combination can be bypassed by setting the appropriate bit in Control Register 1, thus producing samples at 7.2/8.0/9.6 kHz or 28.8/32.0/38.4 kHz, respectively. The frequency response of the AD28msp01 is altered when these filters are bypassed. The DSP processor that receives samples from the AD28msp01 may need to compensate for this change.

Each resultant sample is then loaded into the SPORT for transmission.

Analog Input Interface

The recommended analog input interface is shown in Figure 2. Since the AD28msp01 operates from a single 5 V power supply, an arbitrary analog input signal with 0 V dc bias must be offset and scaled appropriately to avoid clipping and to ensure successful conversion. The scaling of the analog input is achieved by the resistors R_{IN} and R_{FB}. The gain $-R_{FB}/R_{IN}$ should be selected to ensure that a full-scale analog input signal at A_{IN} does not exceed a 3.156 V peak-to-peak signal at the output of the input amplifier (monitored at V_{FB}). The dc offsetting of the analog input is performed with an on-chip generated reference voltage of 2.5 V (nominal). The A_{IN} signal must be ac-coupled with a capacitor (C_{AC}).

Since the receiver uses a highly oversampled implementation approach which transfers the bulk of the antialiasing filtering requirement into the digital domain, the analog input antialiasing filter need only be of low order. This first stage of antialiasing is performed by the R_{FB}/C_{FB} combination, allowing the user to arbitrarily set the input 3 dB point. An acceptable 3 dB point range is 20 kHz ±10%, which should be achieved using components in the ranges indicated. See Figure 2. Note that all frequency response specifications given in this data sheet do not include the slight in-band rolloff caused by the use of a feedback capacitor (C_{FB}).

This input structure also allows the easy combination of a number of analog inputs before conversion via the summing node (V_{IN}), as indicated in Figure 2.

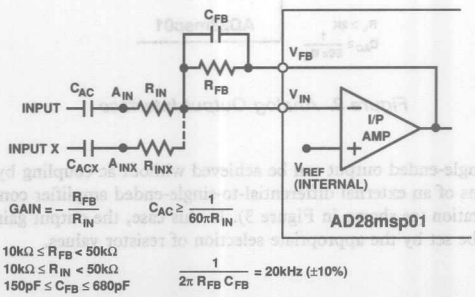


Figure 2. Analog Input Interface

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

or 9.6 kHz rate from the SPORT. These samples are low-pass filtered by the anti-imaging filter which also raises the sampling rate to 28.8/32.0/38.4 kHz. The low-pass anti-imaging filter can be bypassed by setting the appropriate bit in Control Register 1. If the filter is bypassed, the DSP that transmits data to the AD28msp01 must be able to transmit at the 28.8/32.0/38.4 kHz rate.

The samples from the output of the anti-imaging filter are then fed to the Interpolator which raises the sampling rate to 1.7280 MHz by interpolating between the incoming samples. These 1.7280 MHz 16-bit samples are then processed by the digital sigma-delta modulator which noise-shapes the data stream and reduces the sample width to one.

This one-bit data stream at 1.7280 MHz is then fed to the analog smoothing filter in which the bit stream is converted to an analog voltage and low-pass filtered. The output of the analog smoothing filter is a differential signal that is fed to the output amplifier, from which differential analog outputs are available, biased by the internal reference voltage.

Analog Output Interface

The differential analog output signal will be dc-biased at the internal reference voltage and, therefore, should be ac-coupled using C_{AC+} and C_{AC-} before applying to a load as shown in Figure 3. Load resistances in the range 2 kΩ to ∝ can be accommodated.

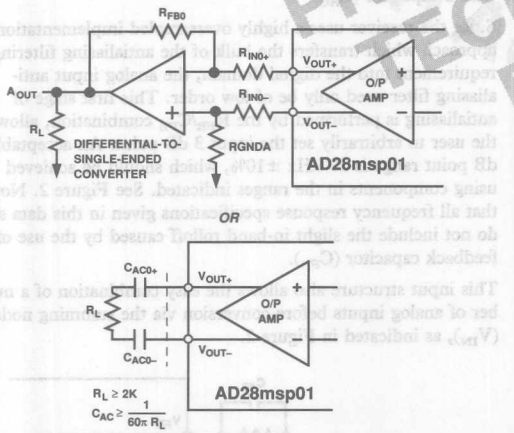


Figure 3. Analog Output Interface

A single-ended output can be achieved without ac coupling by means of an external differential-to-single-ended amplifier configuration (as shown in Figure 3). In this case, the output gain can be set by the appropriate selection of resistor values.

The AD28msp01 generates all transmit and receive clocks necessary to implement standard voice-grade modems. The AD28msp01 can generate six different clock signals for transmit and receive timing as well as an additional clock signal for serial port timing.

The receive clocks are the RCONV, RBIT and RBAUD signals. The individual clock rates are programmable and are all synchronized to RCONV.

The transmit clocks are the TCONV, TBIT and TBAUD signals. The individual clock rates are programmable and are all synchronized to TCONV.

Depending on the operating mode, the converter clocks can be synchronized to an external clock signal (TSYNC) or can be generated internally. The clocks can be adjusted in phase by setting the appropriate phase adjust register.

Resampling Interpolation Filter

In V.32 modems the ADC of the receiving modem samples at the same frequency as the transmitting modem's DAC, but at an unknown phase difference. The receiving modem must execute a timing recovery algorithm to force the received data to be sampled in phase with the received signal. The AD28msp01 includes a digital resampling interpolation filter to resample the received signal at the correct phase.

The resampling interpolation filter interpolates the data to a 1.7280 MHz rate. The data is then resampled (decimated) at the sample rate but in phase with the RCONV clock. The frequency response characteristics of the resampling interpolation filter are identical to the frequency response characteristics of the DAC.

Since the resample phase is locked to RCONV, it can be advanced or slipped by writing a signed-magnitude value to the Receive Phase Adjust Register (Control Register 2). The register decrements or increments to zero to determine the phase shift. The AD28msp01 implements the phase shift by adjusting the phase of an internal clock signal, the oversampling clock. The amount of time added or subtracted is relative to one period of the master clock (MCLK). The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 4 (or 5).

The change in phase requires a maximum of two RCONV cycles to complete. If the value written to Control Register 4 is less than the oversampling ratio, then the change will complete in one RCONV cycle.

Control Registers

The AD28msp01 contains six control registers which configure various modes of device operation—sampling rate, phase shift, clock rate, etc. All of the control registers are read and written via the serial port. Unused bits in the control registers should always be set to zero.

The control registers should be set up for the desired mode of operation before bringing the AD28msp01 out of power down (by writing ones to the power-down analog and power-down digital bits in Control Register 1).

PRELIMINARY TECHNICAL DATA

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The sampling rate should be set before writing ones to the power-down bits. Changing the sampling rate at any other time will force a soft reset. Changing from an asynchronous operating mode to a V.32 mode or vice versa will also force a soft reset (see the Operating Modes section of this data sheet).

In a **soft reset**, the AD28msp01 is reset but the control register values do not change.

The table below shows when a soft reset is caused by changing the values of certain control register bits while the device is operating. When these bits are modified, the AD28msp01 will perform a soft reset and start up again in the new configuration.

Bits	*Configures*
Control Register 0, SR1–SR0	Sampling rate
Control Register 0, OP2–OP0	Clock generation operating modes (async-to-V.32 or V.32-to-async)
Control Register 0, TS3–TS0	TSYNC rate
Control Register 1, FB2–FB0	Filter bypass configuration
Control Register 1, SA87	Sampling rate scaling by 8/7

Control Register 0 **address = 0x00**
This register is used to:

- Enable/disable the resampling interpolation filter
- Set the external TSYNC clock rate
- Select the sampling rate
- Select the operating mode

Control Register 1 **address = 0x01**
This register is used to:

- Increase the sampling rate to 8/7 the rate selected in Control Register 0
- Power down the device
- Bypass the digital filters

If any low-pass filter is bypassed, the resampling interpolation filter should be disabled (in Control Register 0.)

Control Register 2 **address = 0x02**
This register is used to:

- Select the frequency of the Receive baud clock (RBAUD)
- Select the frequency of the Receive bit clock (RBIT)

Control Register 3 **address = 0x03**
This register is used to:

- Select the frequency of the Transmit baud clock (TBAUD)
- Select the frequency of the Transmit bit clock (TBIT)

Control Register 4 **address = 0x04**
This register is used to:

- Change the phase of the Receive clocks (RBAUD, RBIT, RCONV)

This register must be equal to zero before its value can be changed. Once you have written a value to the register, subsequent writes are ignored until the register is finished incrementing/decrementing to zero. If the register is read while incrementing/ decrementing, its current value is returned (not the value originally loaded).

Any value written to this register prior to the first rising edge of the conversion clock (RCONV) is ignored.

The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 4. The AD28msp01 decrements Control Register 4 as it adjusts the phase of RCONV. Control Register 4 will equal zero when the phase shift is complete.

Control Register 5 **address = 0x05**
This register is used to:

- Change the phase of the Transmit clocks (TBAUD, TBIT, TCONV)

This register must be equal to zero before its value can be changed. Once you have written a value to the register, subsequent writes are ignored until the register is finished incrementing/decrementing to zero. If the register is read while incrementing/decrementing, its current value is returned (not the value originally loaded).

Any value written to this register prior to the first rising edge of the conversion clock (TCONV) is ignored.

The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 5. The AD28msp01 decrements Control Register 5 as it adjusts the phase of TCONV. Control Register 5 will equal zero when the phase shift is complete.

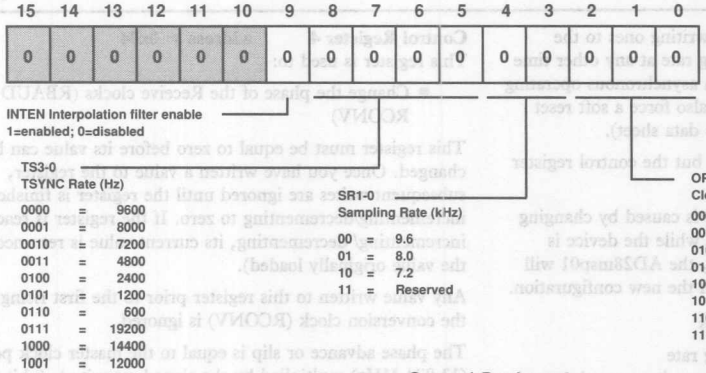


Address Word

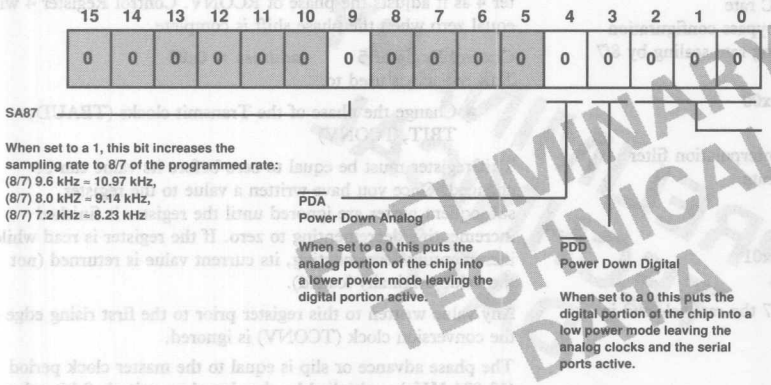
PRELIMINARY TECHNICAL DATA

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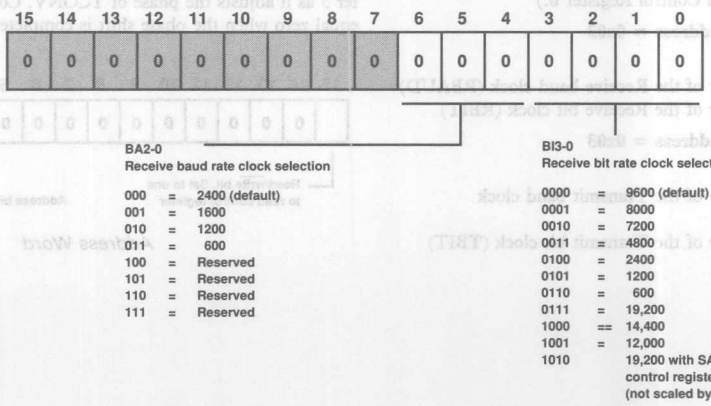


Control Register 0



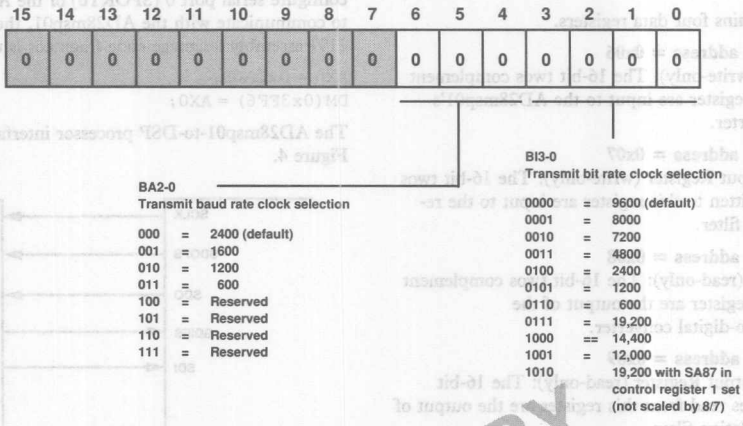
PRELIMINARY TECHNICAL DATA

Control Register 1

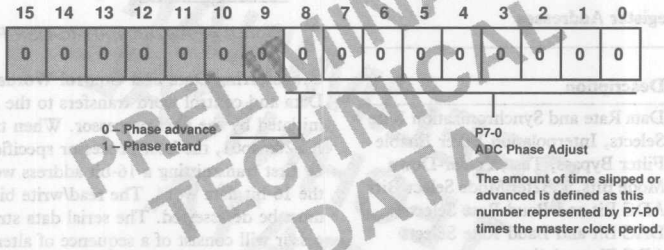


Control Register 2 (Receive Bit and Baud Rate Selection)

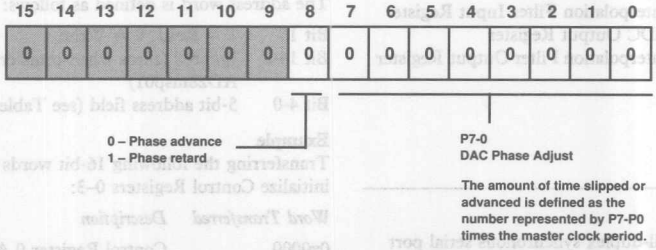
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Control Register 3 (Transmit Bit and Baud Rate Selection)



Control Register 4 (ADC Phase Adjust)



Control Register 5 (DAC Phase Adjust)

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DATA REGISTERS

The AD28msp01 contains four data registers.

Data Register 0 address = 0x06
DAC Input Register (write-only): The 16-bit twos complement values written to this register are input to the AD28msp01's digital-to-analog converter.

Data Register 1 address = 0x07
Interpolation Filter Input Register (write-only): The 16-bit twos complement values written to this register are input to the re-sampling interpolation filter.

Data Register 2 address = 0x08
ADC Output Register (read-only): The 16-bit twos complement values read from this register are the output of the AD28msp01's analog-to-digital converter.

Data Register 3 address = 0x09
Interpolation Filter Output Register (read-only): The 16-bit twos complement values read from this register are the output of the resampling interpolation filter.

Addresses 0x0A–0x1F are reserved.

Table I. Register Addresses

Address Bits 4-0	Register	Description
00000	Control Register 0	Data Rate and Synchronization Rate Selects, Interpolation Filter Enable
00001	Control Register 1	Filter Bypass, Test, Power-Down Mode Bits, V.32ter Mode Select Bits
00010	Control Register 2	ADC Bit and Baud Rate Selects
00011	Control Register 3	DAC Bit and Baud Rate Selects
00100	Control Register 4	ADC Phase Adjust
00101	Control Register 5	DAC Phase Adjust
00110	Data Register 0	DAC Input Register
00111	Data Register 1	Interpolation Filter Input Register
01000	Data Register 2	ADC Output Register
01001	Data Register 3	Interpolation Filter Output Register
01010	Reserved	
. . . . .	. . . . .	
. . . . .	. . . . .	
. . . . .	. . . . .	
11111	Reserved	

Serial Port

The AD28msp01 includes a full-duplex synchronous serial port (SPORT) used to communicate with a host processor. The SPORT is used to read and write all data and control registers in the AD28msp01. The SPORT transfers 16-bit words, MSB first, at a serial clock rate of 1.7280 MHz.

When the AD28msp01 exits reset, both the analog circuitry and the digital circuitry are powered down. The serial port will not transmit data to the host until the host sets the power-down bits in Control Register 1 to 1. All control registers should be initialized before these bits are set.

The SPORT is configured for an externally generated receive frame sync (SDIFS), and an internally generated serial clock (SCLK) and transmit frame sync (SDOFS). The host processor should be configured for an external serial clock and receive frame sync and an internal transmit frame sync. For example, to configure serial port 0 (SPORT0) of the ADSP-2101 processor to communicate with the AD28msp01, the following ADSP-2101 assembly language code fragment is used:

```
AX0 = 0x2A0F;
DM(0x3FF6) = AX0;
```

The AD28msp01-to-DSP processor interface is shown in Figure 4.

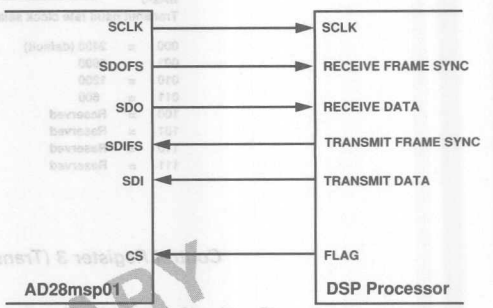


Figure 4. AD28msp01-to-DSP Processor Interface

Transferring Data and Control Words to the AD28msp01

Data and control word transfers to the AD28msp01 can only be initiated by the host processor. When transferring data to the AD28msp01, the host processor specifies the destination register by first transmitting a 16-bit address word and then transmitting the 16-bit data word. The read/write bit in the address word must be de-asserted. The serial data stream from the host processor will consist of a sequence of alternating address and data words. The AD28msp01 will not write the target register until both the address word and data word are completely transferred.

The address word is defined as follows:

Bit 15 1 = Read, 0 = Write
Bit 14-5 Ignored (zeros when transfers originate from the AD28msp01)
Bit 4-0 5-bit address field (see Table I)

Example

Transferring the following 16-bit words to the AD28msp01 will initialize Control Registers 0–3:

Word Transferred	*Description*
0x0000	Control Register 0 Address Word
0x0254	Write this value to Control Register 0
0x0002	Control Register 2 Address Word
0x0031	Write this value to Control Register 2
0x0003	Control Register 3 Address Word
0x0032	Write this value to Control Register 3
0x0001	Control Register 1 Address Word
0x0018	Write this value to Control Register 1

Note that the power-down bits in Control Register 1 are released (set to 1) only after the AD28msp01 is fully configured by writing to Control Registers 0, 2, and 3.

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Transferring Data from the AD28msp01 to the Host
Data transfers to the host processor can only be initiated by the AD28msp01. When transferring data the AD28msp01 first specifies the source register by transferring a 16-bit address word and then transfers the contents of the source register. Bits 14–5 of the address word will always be forced to zero. When transferring data, the serial data stream from the AD28msp01 will consist of a sequence of alternating address and data words.

Transferring Control Words from the AD28msp01 to the Host
All control registers in the AD28msp01 are host readable. To read a control register, the host must transmit a 16-bit address word with the Read/Write bit set, then transmit a dummy data word. The AD28msp01 will respond by first completing any AD28msp01-to-Host transfer in progress. As soon as the dummy data word is received, the device will transfer a 16-bit word with the control register address and then transmit the contents of the control register.

Example
The following data streams show how a host can read the contents of an AD28msp01 control register:

Host Transfer	*AD28msp01 Transfer*	*Description*
0x8001		Read Control Register 0
0x1234		Dummy Data Word
	0x——	AD28msp01 completes data
	0x——	Transfer in progress
	0x0001	Address word
	0x0023	Contents of Control Register 1

Serial Port Timing
All serial transfers are synchronous. The receive data (SDI) and receive frame sync (SDIFS) are clocked into the device on the falling edge of SCLK. The receive frame sync (SDIFS) must be asserted one SCLK cycle before the first data bit is transferred. When receiving data, the AD28msp01 ignores the receive frame sync pin until the least significant bit is being received.

When transmitting data, the AD28msp01 asserts transmit frame sync (SDOFS) and transmit data (SDO) synchronous with the rising edge of SCLK. Transmit frame sync is transmitted one SCLK cycle before the first data bit is transferred.

All input signals to the serial port must meet setup and hold times as specified in this data sheet.

OPERATING MODES
The AD28msp01 is capable of operating in several different modes, as described below.

V.32 TSYNC Mode
In V.32 TSYNC Mode, the AD28msp01's transmit circuitry is synchronized to an external TSYNC signal. The AD28msp01's receive circuitry is sampled synchronous to the transmit circuitry, but the data can be resampled at a different phase through the resampling interpolation filter.

TCONV, TBIT and TBAUD are generated internally but are phase-locked to the external TSYNC input signal with the digital phase-locked loop. RCONV, RBIT and RBAUD are generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

TCONV initiates a new DAC sample update and loads the ADC register (Data Register 2) with a new sample.

The digital resampling interpolation filter can be used for digital resampling of the received signal. Enable this function by setting Bit 9 in Control Register 0. The phase of the resampled signal is adjusted with the Receive Phase Adjust Register. Samples are loaded into the interpolator at the TCONV rate and are resampled at the RCONV rate.

When entering V.32 TSYNC Mode, RCONV is locked to TCONV before TCONV is locked to TSYNC. If this mode is entered from a non-V.32 mode, the device performs a soft reset. The time required to lock TCONV to RCONV is dependent on the phase difference between RCONV and TCONV when entering the mode.

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in

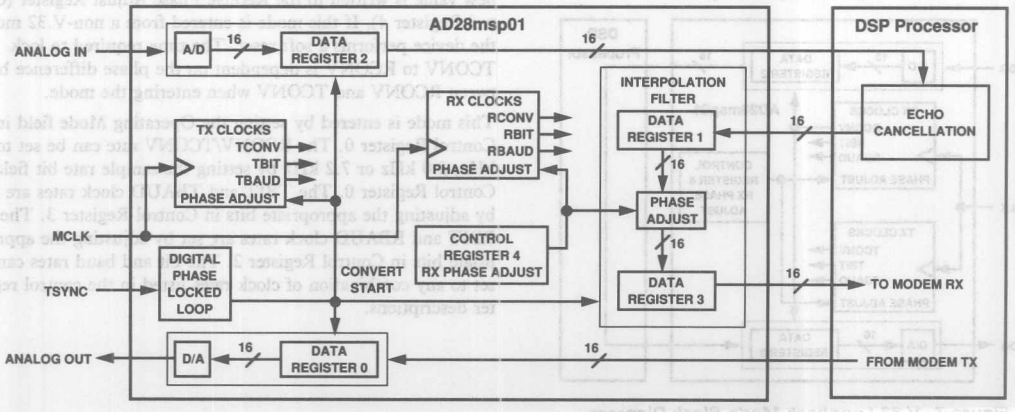


Figure 5. V.32 TSYNC Mode Block Diagram

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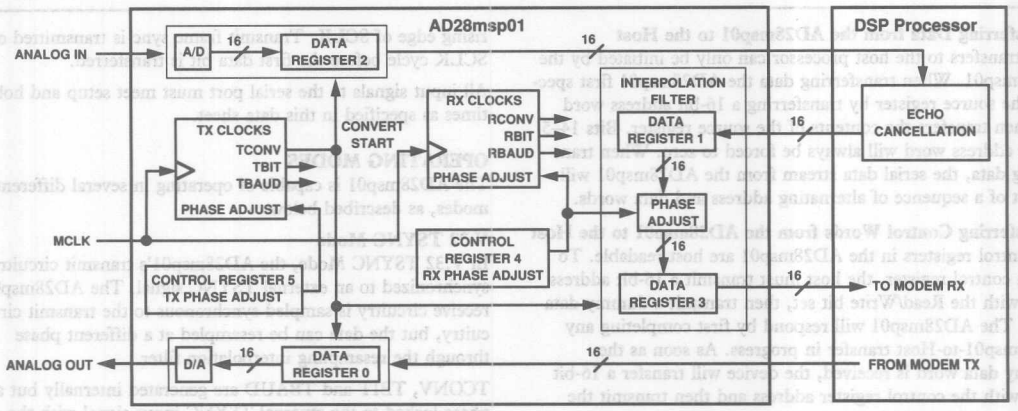


Figure 6. V.32 Internal Sync Mode Block Diagram

Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit rates, baud rates and TSYNC rate can be set to any combination of clock rates listed in the control register descriptions. The TSYNC field on Control Register 0 must be set to the frequency of the input pin.

Example

Transferring the following word sequence to the AD28msp01 will configure the device for V.32 TSYNC Mode at the clock rates indicated:

Word Transferred	*Description*
0x0000	Control Register 0 address word
0x0254	Enable interpolation filter, TSYNC = 7200, sample rate = 7200, mode = V.32 TSYNC
0x0002	Control Register 2 address word
0x0002	RBAUD = 2400, RBIT = 7200
0x0003	Control Register 3 address word
0x0023	TBAUD = 1200, TBIT = 4800
0x0001	Control Register 1 address word
0x0018	Configure and power-up device

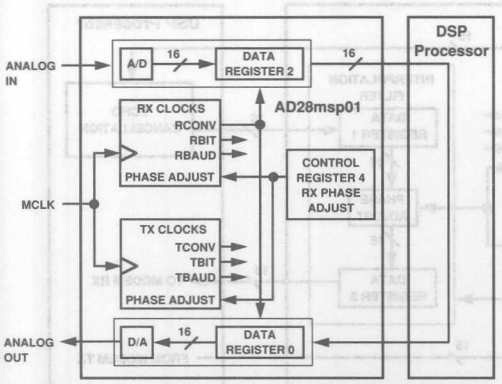


Figure 7. V.32 Loopback Mode Block Diagram

V.32 Internal Sync Mode

In V.32 Internal Sync Mode, the AD28msp01's transmit clocks are generated internally. The receive circuitry operates synchronous to the transmit circuitry, but the data can be resampled at a different phase through the resampling interpolation filter.

TCONV, TBIT and TBAUD are generated internally and can be phase adjusted with the Transmit Phase Adjust Register (Control Register 5). RCONV, RBIT and RBAUD are also generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

TCONV initiates a new DAC sample update and loads the ADC register (Data Register 2) with a new sample.

The digital resampling interpolation filter can be used for digital resampling of the received signal. Enable this function by setting Bit 9 in Control Register 0. The phase of the resampled signal is adjusted with the Receive Phase Adjust Register. Samples are loaded into the interpolator at the TCONV rate and are resampled at the RCONV rate.

When entering V.32 Internal Sync Mode, RCONV is first locked to TCONV. RCONV is then phase adjusted whenever a new value is written to the Receive Phase Adjust Register (Control Register 4). If this mode is entered from a non-V.32 mode, the device performs a soft reset. The time required to lock TCONV to RCONV is dependent on the phase difference between RCONV and TCONV when entering the mode.

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

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V.32 Loopback Mode

In V.32 Loopback Mode, the AD28msp01's receive circuitry and transmit circuitry are locked together.

RCONV is generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4). RBIT, RBAUD, TCONV, TBIT and TBAUD are all locked to RCONV.

RCONV initiates a new DAC sample update and loads the ADC register (Data Register 2) with a new sample. The RCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

V.32ter TSYNC Mode

This mode is identical to V.32 TSYNC Mode except all clocks are scaled by a factor of 8/7 over the corresponding V.32 TSYNC rate. In this mode, the maximum value to which the phase adjust registers (Control Registers 4 and 5) may be set is +192.

Both TBIT and RBIT can be set to a 19,200 Hz rate that will not be scaled by a factor of 8/7, by setting the appropriate fields in Control Registers 2 and 3.

V.32ter Internal Sync Mode

This mode is identical to V.32 TSYNC Mode except all clocks are scaled by a factor of 8/7 over the corresponding V.32 TSYNC rate. In this mode, the maximum value to which the phase adjust registers (Control Registers 4 and 5) may be set is +192.

Both TBIT and RBIT can be set to a 19,200 Hz rate that will not be scaled by a factor of 8/7, by setting the appropriate fields in Control Registers 2 and 3.

Asynchronous Fallback TSYNC Mode

TCONV, TBIT and TBAUD are generated internally but phase locked to the external TSYNC input signal. RCONV, RBIT and RBAUD are generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit rates, baud rates and TSYNC rate can be set to any combination of clock rates listed in the control register descriptions.

Asynchronous Fallback Mode

TCONV, TBIT and TBAUD are generated internally and can be phase adjusted with the Transmit Phase Adjust Register (Control Register 5). RCONV, RBIT and RBAUD are generated internally and can also be phase adjusted with the Receive Phase Adjust Register (Control Register 4). The digital phase-locked loop is not used in this operating mode

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz , 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

PRELIMINARY TECHNICAL DATA

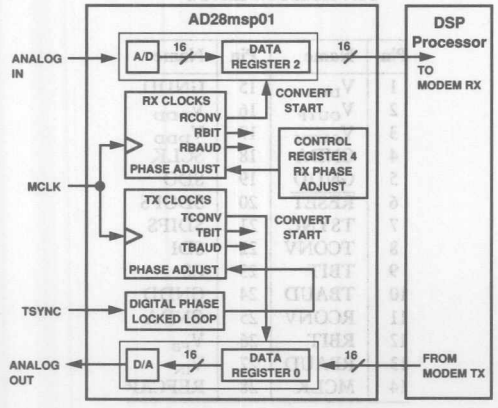


Figure 8. Asynchronous Fallback TSYNC Driven Mode Block Diagram

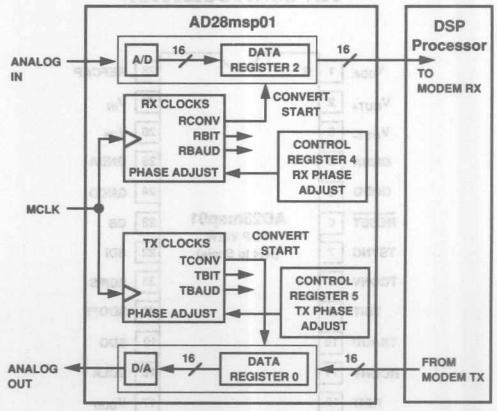


Figure 9. Asynchronous Fallback Mode Block Diagram

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- V.32 Modes to Asynchronous Fallback Modes
- Asynchronous Fallback to V.32 Modes

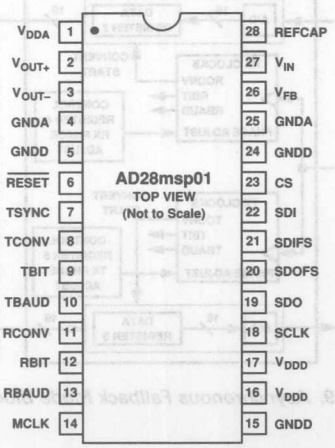
Operating Modes Summary

Mode	Initial Phase Lock After Entering Mode	Normal DPLL* Operation	Phase Register Programmable**	Resampling Interpolator	Internal Filter Operation Synchronous to ADC	Internal Filter Operation Synchronous to DAC	Control Register 0 OP2-0
Async Fallback	No Phase Lock	No Phase Lock	ADC, DAC	Not Used	RCONV	TCONV	000
Async TSYNC	TCONV Lock to TSYNC	TCONV Lock to TSYNC	ADC	Not Used	RCONV	TCONV	111
V.32 TSYNCH	RCONV Lock to TCONV	TCONV Lock to TSYNC	ADC	Input Synchronous and In Phase with TCONV, Output Synchronous and In Phase with RCONV	TCONV	TCONV	100
V.32 Internal Sync	RCONV Lock to TCONV	No Phase Lock	ADC, DAC	Input Synchronous and In Phase with TCONV, Output Synchronous and In Phase with RCONV	TCONV	TCONV	101
V.32 Loopback	TCONV Lock to RCONV	No Phase Lock	ADC†	Not Used	TCONV	TCONV	110

*DPLL—Digital Phase-Locked Loop.
**ADC phase adjusted via Control Register 4, DAC phase adjusted via Control Register 5.
†Adjusting ADC phase also adjusts DAC phase in this mode.
NOTE
All receive clocks: RBIT, RBAUD are synchronous to RCONV. All transmit clocks: TBIT, TBAUD are synchronous to TCONV.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



PIN ASSIGNMENTS

Pin	Name	Pin	Name
1	V_{DDA}	15	GNDD
2	V_{OUTP}	16	V_{DDD}
3	V_{OUTN}	17	V_{DDD}
4	GNDA	18	SCLK
5	GNDD	19	SDO
6	$\overline{RESET}$	20	SDOFS
7	TSYNC	21	SDIFS
8	TCONV	22	SDI
9	TBIT	23	$\overline{CS}$
10	TBAUD	24	GNDD
11	RCONV	25	GNDA
12	RBIT	26	V_{FB}
13	RBAUD	27	V_{IN}
14	MCLK	28	REFCAP

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SPECIFICATIONS

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

Parameter		Test Condition	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	V_{DD} = max	2.0			V
V_{IL}	Input Low Voltage	V_{DD} = min			0.8	V
V_{OH}	Output High Voltage	V_{DD} = min, I_{OH} = −0.5 mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	High Level Input Current	V_{DD} = max, V_{IN} = max			10	µA
I_{IL}	Low Level Input Current	V_{DD} = max, V_{IN} = 0 V			10	µA
I_{OZL}	Low Level Output 3-State Leakage Current	V_{DD} = max, V_{IN} = max			10	µA
I_{OZH}	High Level Output 3-State Leakage Current	V_{DD} = max, V_{IN} = 0 V			10	µA
C_I	Digital Input Capacitance					pF

Parameter		Min	Typ	Max	Unit
Power Dissipation					
V_{DDA}	Analog Operating Voltage		5		V
V_{DDD}	Digital Operating Voltage		5		V
I_{DDA}	V_{DDA} Operating Current Active		40		mA
I_{DDD}	V_{DDD} Operating Current Active				mA
P_1	Power Dissipation (V_{DDA} and V_{DDD} Active)				mW
I_{DDA}	V_{DDA} Operating Current Inactive		0.5		mA
I_{DDD}	V_{DDD} Operating Current Inactive				mA
P_0	Power Dissipation (V_{DDA} and V_{DDD}) Inactive				mW

PRELIMINARY TECHNICAL DATA

RECOMMENDED OPERATING CONDITIONS

Parameter		J Grade Min	J Grade Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	V
T_{AMB}	Ambient Operating Temperature	0	+70	°C

Refer to Environmental Conditions for information on case temperature and thermal specifications.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (5 sec) PLCC . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD28msp01 features proprietary input protection circuitry to dissipate high energy discharges (Human Body Model). Per Method 3015 of MIL-STD-883C, the AD28msp01 has been classified as a Class 1 device.

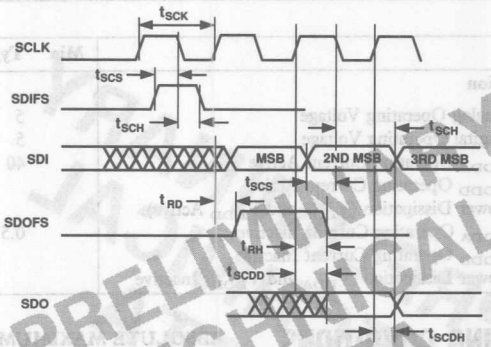


Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

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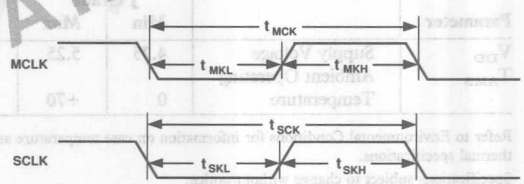
SPECIFICATIONS—AD28msp01

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCS}	SDI/SDIFS Setup before SCLK Low	10		ns
t_{SCH}	SDI/SDIFS Hold after SCLK Low	10		ns
Switching Characteristic				
t_{SCK}	SCLK Period			ns
t_{RD}	SDOFS Delay from SCLK High		15	ns
t_{RH}	SDOFS Hold after SCLK High	0		ns
t_{SCDH}	SDO Hold after SCLK High	0		ns
t_{SCDD}	SDO Delay from SCLK High		30	ns

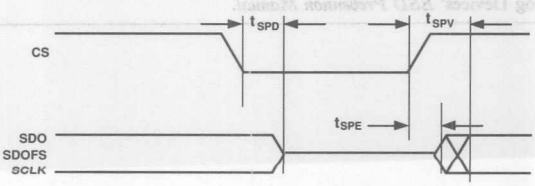


PRELIMINARY TECHNICAL DATA

Parameter		Min	Max	Unit
Clock Signals				
Timing Requirement:				
t_{MCK}	MCLK Frequency	13.824	13.824	MHz ±0.0025%
t_{MKL}	MCLK Width Low			ns
t_{MKH}	MCLK Width High			ns
Switching Characteristic:				
t_{SCK}	SCLK Period			ns
t_{SKL}	SCLK Width Low			ns
t_{SKH}	SCLK Width High			ns



Parameter		Min	Max	Unit
Serial Port Tristate				
Switching Characteristic:				
t_{SPD}	CS Low to SDO, SDOFS, SCLK Disable			ns
t_{SPE}	CS High to SDO, SDOFS, SCLK Enable			ns
t_{SPV}	CS High to SDO, SDOFS, SCLK Valid			ns



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ANALOG INTERFACE CHARACTERISTICS

Parameter		Test Condition	Min	Typ	Max	Unit
ADC:						
I_L	Input Leakage Current at V_{IN}			10		nA
R_I	Input Resistance at V_{IN}			100		MΩ
C_{IL}	Input Load Capacitance at V_{FB}			10		pF
V_{INMAX}	Maximum Input Range at V_{IN}			3.156		V p–p
DAC:						
R_O	Output Resistance for Voice Frequencies*			1		Ω
V_{OOFF}	Output dc Offset Between V_{OUT+} and V_{OUT-}			100		mV
C_{OL}	Output Load Capacitance*				100	pF
V_O	Maximum Voltage Output Swing (p–p) Across R_L Differential			6.312		V
R_L	Load Resistance*		2			kΩ

*At V_{OUT+} and V_{OUT-}

Parameter	Test Conditions	Min	Typ	Max	Unit
Absolute Gain					
ADC Milliwatt Response (ADC Gain Tolerance)	Signal Input = 0.7746 V rms		±0.1		dBm0
Digital Milliwatt Response (DAC Gain Tolerance)	Signal Input = 0.7746 V rms		±0.1		dBm0

Parameter	Test Conditions	Min	Max	Unit
Gain Tracking (Reference Level = 0 dBm0)				
ADC Gain Tracking Error Sinusoidal Input	+3 to −50 dBm0		±0.1	dB
Decoder Gain Tracking Error Sinusoidal Input	+3 to −50 dBm0		±0.1	dB

Typical Frequency Responses
The frequency responses of the ADC and DAC are given below.

	9.6 kHz	8.0 kHz	7.2 kHz
ADC			
Passband Ripple	<0.1 dB	<0.1 dB	<0.1 dB
Low-Pass Passband Cutoff Frequency	3.4 kHz	3.4 kHz	3.3 kHz
Low-Pass Stopband Cutoff Frequency	4.8 kHz	4.0 kHz	3.6 kHz
High-Pass Passband Cutoff Frequency	220 Hz	220 Hz	220 Hz
High-Pass Stopband Cutoff Frequency	60 Hz	60 Hz	60 Hz
Low-Pass Stopband Rejection	−55 dB	−55 dB	−55 dB
High-Pass Stopband Rejection	−50 dB	−50 dB	−50 dB
DAC			
Passband Ripple	<0.1 dB	<0.1 dB	<0.1 dB
Passband Cutoff Frequency	3.4 kHz	3.4 kHz	3.3 kHz
Low-Pass Stopband Cutoff Frequency	4.8 kHz	4.0 kHz	3.6 kHz
Stopband Rejection	−55 dB	−55 dB	−55 dB

PRELIMINARY TECHNICAL DATA

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		Min	Typ	Max	Unit
Noise and Distortion					
ADC Signal to Noise Plus Distortion (Single Tone Test)	Output Level: 0		−80		dB
	Output Level: −20 dBm0				dB
	Output Level: −30 dBm0				dB
	Output Level: −40 dBm0				dB
	Output Level: −50 dBm0				dB
	Output Level: −60 dBm0				dB
	Output Level: −70 dBm0				dB
	Output Level: −80 dBm0				dB
DAC Signal to Noise Plus Distortion (Single Tone Test)	Output Level: 0		−80		dB
	Output Level: −20 dBm0				dB
	Output Level: −30 dBm0				dB
	Output Level: −40 dBm0				dB
	Output Level: −50 dBm0				dB
	Output Level: −60 dBm0				dB
	Output Level: −70 dBm0				dB
	Output Level: −80 dBm0				dB
ADC Intermodulation Distortion			−80		dBm0
DAC Intermodulation Distortion			−80		dBm0
ADC Idle Channel Noise, 0 Hz–4000 Hz Flat			10		dBrn
DAC Idle Channel Noise, 0 Hz–4000 Hz Flat			10		dBrn

PRELIMINARY TECHNICAL

Parameter	Test Conditions	Min	Typ	Max	Unit
PSRR and Crosstalk					
V_{DDA} & V_{DDD} Power Supply Rejection, ADC Channel	100 mV p–p, 1.02 kHz on Supplies		−35		dB
V_{DDA} & V_{DDD} Power Supply Rejection, DAC Channel	100 mV p–p, 1.02 kHz on Supplies		−35		dB
Crosstalk, ADC Channel-to-DAC Channel	ADC Input: 1.02 kHz at 0 dBm0 DAC Input: IDLE CODE Measure V_{OUT} at 1.02 kHz		−80		dB
Crosstalk, DAC Channel-to-ADC Channel	ADC Input: Analog Ground DAC Input: 1.02 kHz at DmW* Measure ADC Output at 1.02 kHz		−80		dB

*DmW = digital milliwatt

	9.6 kHz	8.0 kHz	7.2 kHz	Unit
Typical Group Delay	12	13	15	ms
ADC Low-Pass Filter Group Delay	2	3	5	ms
ADC High-Pass Filter Group Delay	10	10	10	ms
DAC Group Delay	2	3	5	ms
Resampling Filter Group Delay	2	3	5	ms

ORDERING GUIDE

Model	Package Option*
AD28msp01	N-28

*N = Plastic DIP. For outline information see Package Information section.

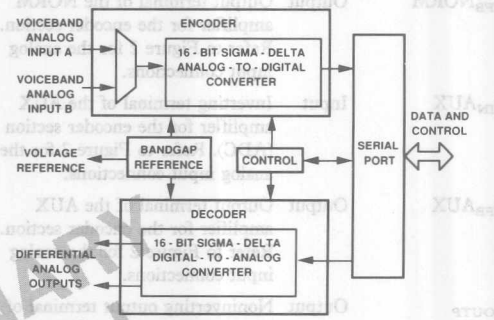
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AD28msp02

FEATURES

Complete Linear Coded Codec
16-Bit Sigma-Delta ADC
16-Bit Sigma-Delta DAC
On-Chip Antialiasing and Anti-Imaging Filters
On-Chip Voltage Reference
8 kHz Sampling Frequency
Twos Complement Coding
65 dB SNR and THD
Programmable Gain on DAC and ADC
DSP Compatible Serial Port
24-Pin (0.3 Inch) DIP/SOIC
Single 5 V Power Supply

SIMPLIFIED BLOCK DIAGRAM



4

GENERAL DESCRIPTION

The AD28msp02, as shown in Figure 1, is a complete analog front end for high performance voiceband DSP applications. Compared to traditional μ-law and A-law codecs, the AD28msp02's linear coded ADC and DAC maintain wide dynamic range throughout the transfer function while maintaining far superior SNR and THD.

A sampling rate of 8.0 kHz coupled with 65 dB SNR and THD performance make the AD28msp02 attractive in many datacom and telecom applications (e.g., cellular radio, telephones, etc.).

The inclusion of on-chip antialiasing and anti-imaging filters, 16-bit ADC, 16-bit DAC and programmable gain amplifiers in a 24-pin DIP/SOIC ensures a highly integrated and compact solution to voiceband analog processing requirements.

The serial I/O port provides easy interface to industry standard DSP processors such as the ADSP-2101, ADSP-2111, ADSP-2105, MC56001 and the TMS320C25.

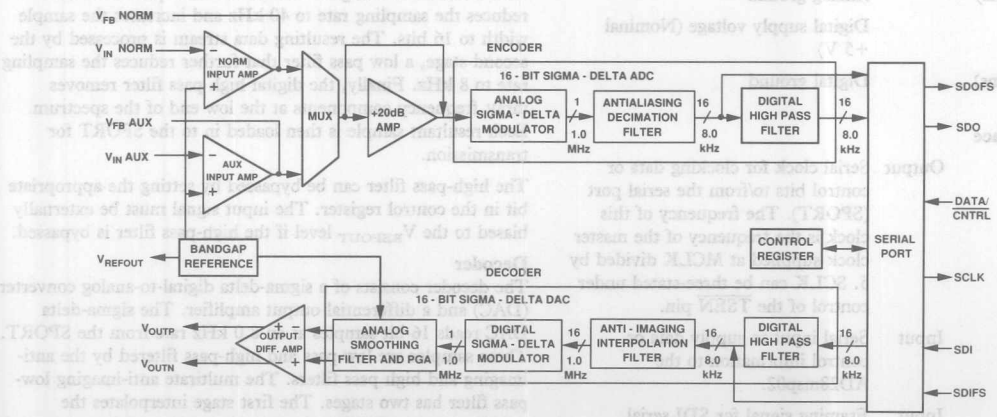


Figure 1. AD28msp02 Block Diagram

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PIN DESCRIPTION

Pin Name	I/O	Function
Analog Interface		
V_{IN}NORM	Input	Inverting terminal of the NORM amplifier for the encoder section (ADC). Refer to Figure 2 for the analog input connections.
V_{FB}NORM	Output	Output terminal of the NORM amplifier for the encoder section. Refer to Figure 2 for the analog input connections.
V_{IN}AUX	Input	Inverting terminal of the AUX amplifier for the encoder section (ADC). Refer to Figure 2 for the analog input connections.
V_{FB}AUX	Output	Output terminal of the AUX amplifier for the encoder section. Refer to Figure 2 for the analog input connections.
V_{OUTP}	Output	Noninverting output terminal of the output differential amplifier, from the decoder (DAC). Refer to Figure 3 for the analog output connections.
V_{OUTN}	Output	Inverting output terminal of the output differential amplifier, from the decoder. Refer to Figure 3 for the analog output connections.
V_{REFOUT}	Output	An output reference voltage of 2.5 V (Nominal).
Power Supplies		
V_{CC}		Analog supply voltage (Nominal +5 V)
GNDA (2 pins)		Analog ground
V_{DD}		Digital supply voltage (Nominal +5 V)
GNDD (2 pins)		Digital ground
Serial Interface		
SCLK	Output	Serial clock for clocking data or control bits to/from the serial port (SPORT). The frequency of this clock is the frequency of the master clock supplied at MCLK divided by 5. SCLK can be three-stated under control of the $\overline{\text{TSEN}}$ pin.
SDI	Input	Serial input to supply data or control information to the AD28msp02.
SDIFS	Input	Framing signal for SDI serial transfers.
SDO	Output	Serial output to obtain data or control information from the AD28msp02. This pin can be three-stated by the $\overline{\text{TSEN}}$ pin.
SDOFS	Output	Framing signal for SDO. This pin can be three-stated by the $\overline{\text{TSEN}}$ pin.
DATA/$\overline{\text{CNTRL}}$	Input	Differentiates between data and control serial transfers for the SPORT.
Miscellaneous		
MCLK	Input	The master clock to the AD28msp02. The clock frequency is 13.0 MHz.
$\overline{\text{RESET}}$	Input	This pin three-states the SPORT pins and clears the digital filter in the modulator.
$\overline{\text{TSEN}}$	Input	This pin should be high to enable the SPORT. When not enabled, SPORT outputs are in a high-impedance state.

FUNCTIONAL DESCRIPTION

Encoder

The encoder consists of two analog input amplifiers and a sigma-delta analog-to-digital converter (ADC). The two analog input amplifiers (NORM, AUX) can be adjusted in gain from −12 dB to +26 dB via external resistors. The amplifiers are biased by an on-chip voltage reference, V_{REFOUT} (see Figure 2). A multiplexer selects one amplifier as the input to the sigma-delta modulator. An optional 20 dB pre-amplifier can be inserted before the modulator. The pre-amplifier and multiplexer are configured by bits in the control register.

The sigma-delta ADC consists of a sigma-delta modulator, an antialiasing decimation filter, and a digital high pass filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a 1.0 MHz rate. This bit stream, representing the analog input, is fed to the antialiasing decimation filter. This filter contains two stages. The first is a low pass filter that reduces the sampling rate to 40 kHz and increases the sample width to 16 bits. The resulting data stream is processed by the second stage, a low pass filter that further reduces the sampling rate to 8 kHz. Finally, the digital high pass filter removes input frequency components at the low end of the spectrum. Each resultant sample is then loaded in to the SPORT for transmission.

The high-pass filter can be bypassed by setting the appropriate bit in the control register. The input signal must be externally biased to the V_{REFOUT} level if the high-pass filter is bypassed.

Decoder

The decoder consists of a sigma-delta digital-to-analog converter (DAC) and a differential output amplifier. The sigma-delta DAC reads 16-bit samples at an 8.0 kHz rate from the SPORT. These samples are low-pass and high-pass filtered by the anti-imaging and high pass filters. The multirate anti-imaging low-pass filter has two stages. The first stage interpolates the sampling rate to 40 kHz; the second stage interpolates to 1.0 MHz. The high pass filter can be bypassed by setting the appropriate bit in the control register.

PRELIMINARY TECHNICAL DATA

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The 1.0 MHz 16-bit samples are processed by the digital sigma-delta modulator which noise-shapes the data stream and reduces the sample width to 1 bit. This 1-bit data stream is fed at a 1.0 MHz rate to the analog smoothing filter in which the bit stream is converted into an analog voltage and low pass filtered. The gain of this smoothing filter can be adjusted via the control register from −15 dB to +6 dB in 3 dB steps. The output of the analog smoothing filter is a differential signal which is fed to the output amplifier.

Serial Port

The serial interface consists of an I/O port which can be used to transmit and receive data or control information to and from the AD28msp02.

Control Register

The control register determines the configuration of the AD28msp02 and can be read and written via the SPORT by driving the DATA/$\overline{\text{CNTRL}}$ pin low. It is possible to program the encoder and decoder gain settings, filter bypass options, power-down option and encoder multiplexer selection using this register.

DETAILED BLOCK DESCRIPTIONS

Analog Input Interface

The recommended analog input interface is shown in Figure 2. Since the AD28msp02 operates from a single 5 V power supply, an arbitrary analog input signal with 0 V dc bias must be offset and scaled appropriately to avoid clipping and to ensure successful conversion. The scaling of the analog input is achieved by the resistors RIN and RFB. The gain −RFB/RIN− should be selected to ensure that a full-scale analog input signal at AIN produces a 3.156 V peak-to-peak signal at the encoder input. The dc offsetting of the analog input is done with an on-chip generated reference voltage V_{REFOUT} . Both the NORM and the AUX inputs must be ac coupled for proper operation. The coupling capacitor, CAC, should be 0.1 μF or greater. The RIN resistors should be chosen to ensure a coupling corner frequency of 30 Hz.

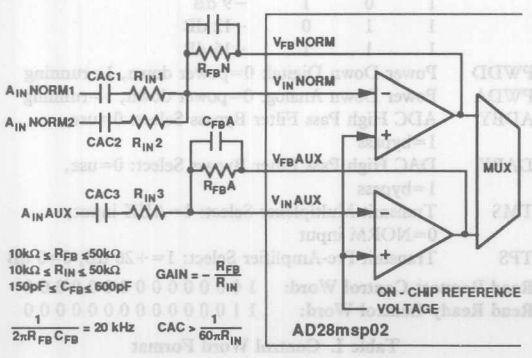


Figure 2. Analog Input Interface

Since the encoder uses a highly oversampled implementation approach which transfers the bulk of the antialiasing filtering requirement into the digital domain, the analog input antialiasing filter need only be of low order. This antialiasing is done by the RFB/CFB combination, allowing the user to arbitrarily set the input 3 dB point. An acceptable 3 dB point range is 20 kHz ± 10% which should be achieved using components in the ranges indicated. (See Figure 2.)

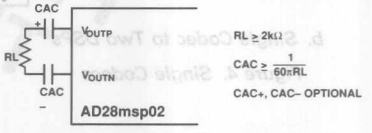
The two separate input amplifiers NORM and AUX can be individually configured to allow for the variations in microphone sensitivity. The 20 dB gain stage can be selected when there is not enough gain in the input amplifier.

This input structure also allows the easy combination of a number of analog inputs before conversion. Figure 2 shows two inputs summed together at the NORM input.

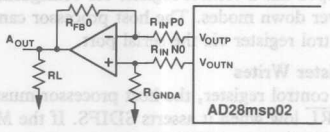
Analog Output Interface

The differential analog output signal is dc biased at the internal reference voltage and therefore can either be ac coupled using CAC+ and CAC− (Figure 3a) or can drive a differential load directly (Figure 3b). Load resistances in the range 2 kΩ to ∞ can be accommodated. The output gain can be programmed via the control register from −15 dB to +6 dB in 3 dB steps. The nominal node differential swing is +3.156 V to −3.156 V.

A single-ended output can be achieved without ac coupling, by means of an external differential-to-single-ended amplifier configuration (Figure 3b). In this case, the output gain can be set by the appropriate selection of resistor values. Alternatively, single-ended outputs may be used directly with degraded performance. Load resistances greater than 2 kΩ can be driven. The nominal maximum single-ended output signal is 3.156 V peak-to-peak (3.17 dBm0).



a. Differential Load with AC Coupling



b. Single-Ended Output

Figure 3. Analog Output Interface

Serial Ports

There is a bidirectional serial port (SPORT) for transmitting data between the AD28msp02 and the host processor, with a minimum of external hardware (Figure 4).

All serial transfers are 16 bits long, MSB first, at the SCLK rate. SCLK is internally set to the master clock frequency divided by 5, exactly 2.6 MHz.

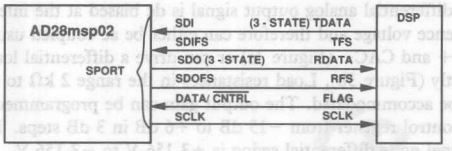
When data is written to the AD28msp02 via the SPORT, the transfer is initiated by the host processor driving the SDIFS input on the SPORT high shortly after the rising edge of SCLK and maintaining SDIFS high for one cycle. The DATA/$\overline{\text{CNTRL}}$ line must be driven high when SDIFS is driven high. Data is then driven from the processor shortly after the rising edge of

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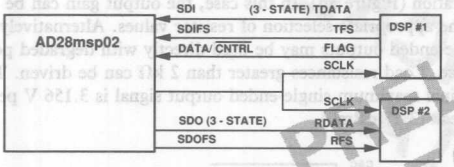
the next clock and clocked into the AD28msp02 on the falling edge of SCLK in that cycle. All data bits are thus clocked into the AD28msp02 on the falling edge of SCLK starting with the MSB first.

If the SDIFS input is driven high again before the end of the present transfer, it is not recognized until the falling edge of SCLK in the LSB cycle.

The $\overline{\text{TSEN}}$ pin can be used to three-state the SPORT pins and disable communication to the host processor. This capability is useful in multi-codec configurations where the host processor can control each $\overline{\text{TSEN}}$ as a memory-mapped pin.



a. Single AD28msp02 to Single-Port DSP



b. Single Codec to Two DSPs

Figure 4. Single Codecs

CONTROL REGISTER

The AD28msp02 has a control register for configuring various gain and power down modes. The host processor can read or write the control register via the serial port.

Control Register Writes

To write the control register, the host processor must assert DATA/$\overline{\text{CNTRL}}$ low when it asserts SDIFS. If the MSB of the bit stream is also low, the SPORT recognizes the incoming serial data as a new control word and copies it to the AD28msp02 control register. The format for the control word is listed in Table I.

Control Register Reads

To read the control register, the host processor must transfer two control words. For each transfer, the DATA/$\overline{\text{CNTRL}}$ pin must be low when SDIFS is asserted. If the MSB of the bit stream is high, the SPORT recognizes the incoming serial data as a request for control information. The protocol for reading the control register is as follows:

a. The host processor sends a "Read Request" control word to the AD28msp02. Since the MSB of this control word is high, the SPORT recognizes the incoming serial data as a read request and does not overwrite the AD28msp02 control register.

b. When the AD28msp02 receives the read request, it finishes any data transfers in progress and waits for a "Read Ready" control word.

c. The host processor then transfers a "Read Ready" control word to the AD28msp02. Upon receiving this control word, the AD28msp02 transfers the control register contents to the host processor via the serial port.

d. When the SPORT completes the control register transfer, it immediately restarts transmitting data at an 8 kHz rate.

This scheme allows any data transfers in progress to complete and resolves any ambiguities between data and control words. The format for the control words is listed in Table I.

Control Register Write:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	RG2	RG1	RG0	0	PWDD	PWDA	ADBY	DABY	TMS	TPS

RG2–RG0 Receive Gain Setting

RG2	RG1	RG0	
0	0	0	+6 dB
0	0	1	+3 dB
0	1	0	0 dB
0	1	1	−3 dB
1	0	0	−6 dB
1	0	1	−9 dB
1	1	0	−12 dB
1	1	1	−15 dB

PWDD Power Down Digital: 0=power down, 1=running
PWDA Power Down Analog: 0=power down, 1=running
ADBY ADC High Pass Filter Bypass Select: 0=use, 1=bypass
DABY DAC High Pass Filter Bypass Select: 0=use, 1=bypass
TMS Transmit Multiplexer Select: 1=AUX input, 0=NORM input
TPS Transmit Pre-Amplifier Select: 1=+20 dB, 0=0 dB

Read Request Control Word: 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Read Ready Control Word: 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Table I. Control Word Format

PRELIMINARY TECHNICAL DATA

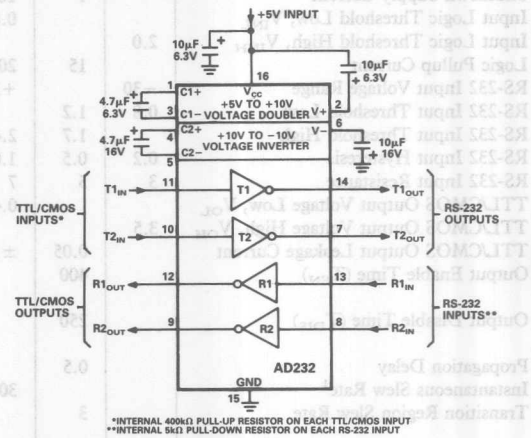
+5 V Powered CMOS RS-232 Drivers/Receivers

AD230–AD241

FEATURES
- Single 5 V Power Supply
- Meets All RS-232-C and V.28 Specifications
- Multiple Drivers and Receivers
- On-Board DC-DC Converters
- ±9 V Output Swing with +5 V Supply
- Low Power CMOS: 5 mA Operation
- Low Power Shutdown ≤1 μA
- 3-State TTL/CMOS Receiver Outputs
- ±30 V Receiver Input Levels
- Plug-In Replacement for MAX230-241

APPLICATIONS
- Computers
- Peripherals
- Modems
- Printers
- Instruments

AD232 TYPICAL OPERATING CIRCUIT



GENERAL DESCRIPTION

The AD230 family of 5 V only, RS-232 line drivers/receivers provides a variety of configurations to fit most communication needs, especially in applications where ±12 V is not available. The AD230, AD235, AD236 and AD241 feature a low power shutdown mode which reduces power dissipation to less than 5 μW making them ideally suited for battery powered equipment. The AD233 and AD235 do not require any external components and are particularly useful in applications where printed circuit board space is critical.

All members of the AD230 family, except the AD231 and the AD239, include two internal charge pump voltage converters which allow operation from a single +5 V supply. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels. The AD231 and AD239 are designed to operate from +5 V and +12 V supplies. An internal +12 V to −12 V charge pump voltage converter generates the −12 V supply.

In order to minimize the package count in all applications, a wide selection of driver/receiver combinations is available (see table below).

SELECTION TABLE

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins
AD230	+5 V	5	0	4	Yes	No	20
AD231	+5 V & +7.5 V to 13.2V	2	2	2	No	No	14
AD232	+5 V	2	2	4	No	No	16
AD233	+5 V	2	2	None	No	No	20
AD234	+5 V	4	0	4	No	No	16
AD235	+5 V	5	5	None	Yes	Yes	24
AD236	+5 V	4	3	4	Yes	Yes	24
AD237	+5 V	5	3	4	No	No	24
AD238	+5 V	4	4	4	No	No	24
AD239	+5 V & +12 V	3	5	2	No	Yes	24
AD241	+5 V	4	5	4	Yes	Yes	28

AD230–AD241—SPECIFICATIONS

(V_{CC} = +5 V ± 10% (AD231, AD232, AD234, AD236, AD238, AD239, AD241); V_{CC} = +5 V ± 5% (AD233, AD235); V+ = 7.5 V to 13.2 V (AD231) & V+ = 12 V ± 10% (AD239); All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		4	10	mA	No Load, T_A = 25°C
		0.4	1	mA	AD231, AD239
V+ Power Supply Current		5	10	mA	No Load, V+ = 12 V AD231 & AD239 Only
Shutdown Supply Current		1	10	μA	T_A = +25°C, V_{SD} = +5 V
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD
Logic Pullup Current		15	200	μA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Threshold High		1.7	2.4	V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	V_{CC} = 5V, T_A = +25°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA (AD231–AD233, I_{OUT} = 3.2 mA)
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
TTL/CMOS Output Leakage Current		0.05	±10	μA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		400		ns	AD235, AD236, AD239, AD241 (Figure 25. C_L = 150 pF)
Output Disable Time (T_{DIS})		250		ns	AD235, AD236, AD239, AD241 (Figure 25. R_L = 1 kΩ)
Propagation Delay		0.5		μs	RS-232 to TTL
Instantaneous Slew Rate[1]			30	V/μs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate		3		V/μs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
V+ . . . . . (V_{CC} −0.3 V) to +13 V
V− . . . . . +0.3 V to −13 V
Input Voltages
T_{IN} . . . . . −0.3 V to (V_{CC} +0.3 V)
R_{IN} . . . . . ±30 V
Output Voltages
T_{OUT} . . . . . (V+, +0.3 V) to (V−, −0.3 V)
R_{OUT} . . . . . −0.3 V to (V_{CC} +0.3 V)
Short Circuit Duration
T_{OUT} . . . . . Continuous

Power Dissipation
Cerdip (Derate 9.5 mW/°C above +70°C) . . . . . 675 mW
Plastic DIP (Derate 7 mW/°C above +70°C) . . . . . 375 mW
SOIC (Derate 7 mW/°C above +70°C) . . . . . 375 mW
Operating Temperature Range
Commercial (J Version) . . . . . 0 to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*
AD230			**AD231**			**AD232**		
AD230JN	0°C to +70°C	N-20	AD231JN	0°C to +70°C	N-14	AD232JN	0°C to +70°C	N-16
AD230JR	0°C to +70°C	R-20	AD231JR	0°C to +70°C	R-16	AD232JR	0°C to +70°C	R-16
AD230AN	−40°C to +85°C	N-20	AD231AN	−40°C to +85°C	N-14	AD232AN	−40°C to +85°C	N-16
AD230AR	−40°C to +85°C	R-20	AD231AR	−40°C to +85°C	R-16	AD232AR	−40°C to +85°C	R-16
AD230AQ	−40°C to +85°C	Q-20	AD231AQ	−40°C to +85°C	Q-14	AD232AQ	−40°C to +85°C	Q-16
			AD231SQ	−55°C to +125°C	Q-14	AD232SQ	−55°C to +125°C	Q-16
AD233			**AD234**			**AD235**		
AD233JN	0°C to +70°C	N-20	AD234JN	0°C to +70°C	N-16	AD235JN	0°C to +70°C	N-24A
AD233AN	−40°C to +85°C	N-20	AD234JR	0°C to +70°C	R-16	AD235AN	−40°C to +85°C	N-24A
			AD234AN	−40°C to +85°C	N-16	AD235AQ	−40°C to +85°C	D-24
			AD234AR	−40°C to +85°C	R-16			
			AD234AQ	−40°C to +85°C	Q-16			
			AD234SQ	−55°C to +125°C	Q-16			
AD236			**AD237**			**AD238**		
AD236JN	0°C to +70°C	N-24	AD237JN	0°C to +70°C	N-24	AD238JN	0°C to +70°C	N-24
AD236JR	0°C to +70°C	R-24	AD237JR	0°C to +70°C	R-24	AD238JR	0°C to +70°C	R-24
AD236AN	−40°C to +85°C	N-24	AD237AN	−40°C to +85°C	N-24	AD238AN	−40°C to +85°C	N-24
AD236AR	−40°C to +85°C	R-24	AD237AR	−40°C to +85°C	R-24	AD238AR	−40°C to +85°C	R-24
AD236AQ	−40°C to +85°C	Q-24	AD237AQ	−40°C to +85°C	Q-24	AD238AQ	−40°C to +85°C	Q-24
AD236SQ	−55°C to +125°C	Q-24				AD238SQ	−55°C to +125°C	Q-24
AD239			**AD241**					
AD239JN	0°C to +70°C	N-24	AD241JR	0°C to +70°C	R-28			
AD239JR	0°C to +70°C	R-24	AD241AR	−40°C to +85°C	R-28			
AD239AN	−40°C to +85°C	N-24						
AD239AR	−40°C to +85°C	R-24						
AD239AQ	−40°C to +85°C	Q-24						
AD239SQ	−55°C to +125°C	Q-24						

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

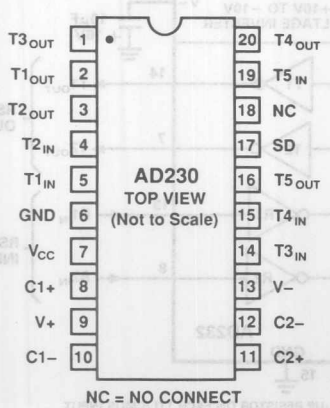


Figure 1. AD230 DIP/SOIC Pin Configuration

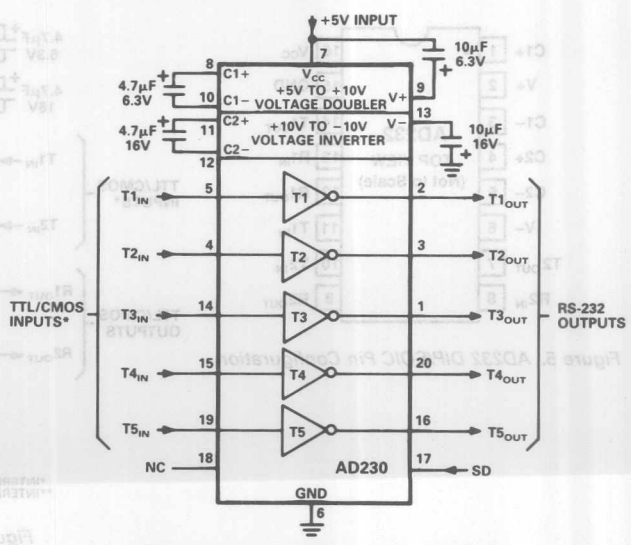
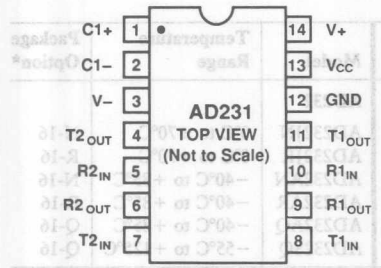


Figure 2. AD230 Typical Operating Circuit



SOIC

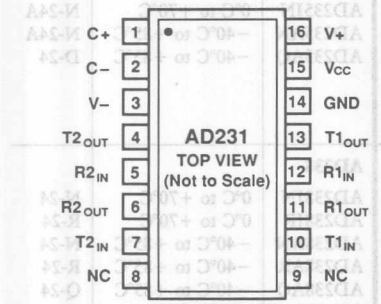


Figure 3. AD231 DIP & SOIC Pin Configurations

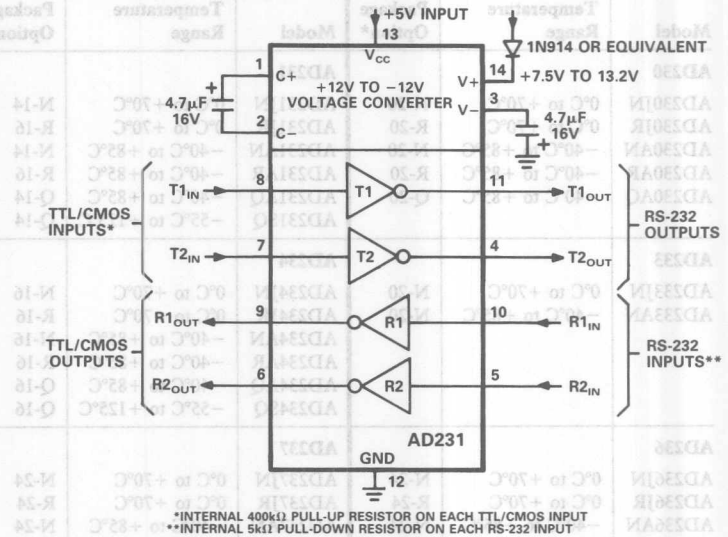


Figure 4. AD231 Typical Operating Circuit

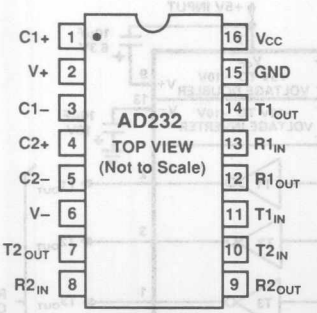


Figure 5. AD232 DIP/SOIC Pin Configuration

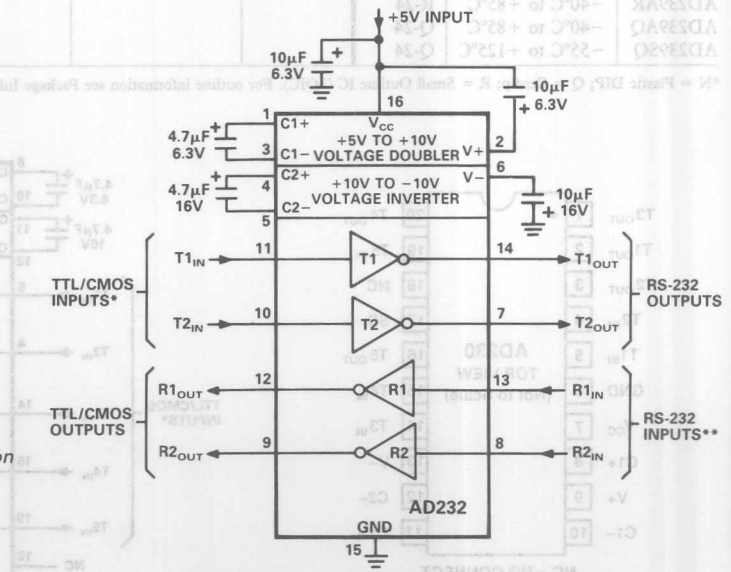


Figure 6. AD232 Typical Operating Circuit

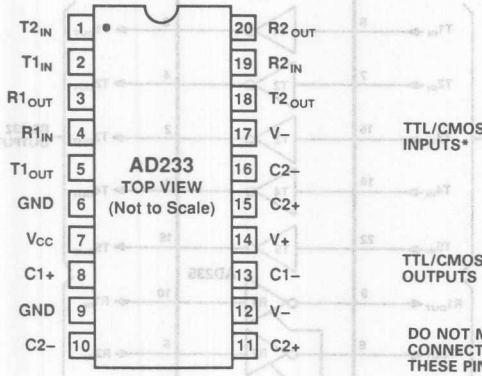


Figure 7. AD233 DIP Pin Configuration

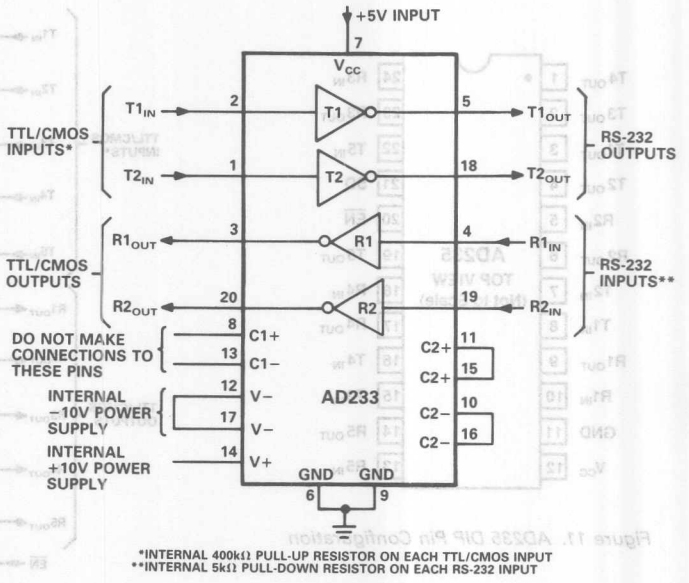


Figure 8. AD233 Typical Operating Circuit

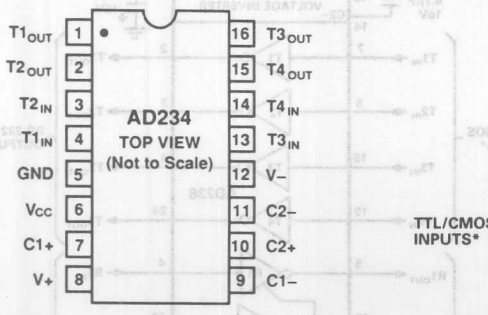


Figure 9. AD234 DIP/SOIC Pin Configuration

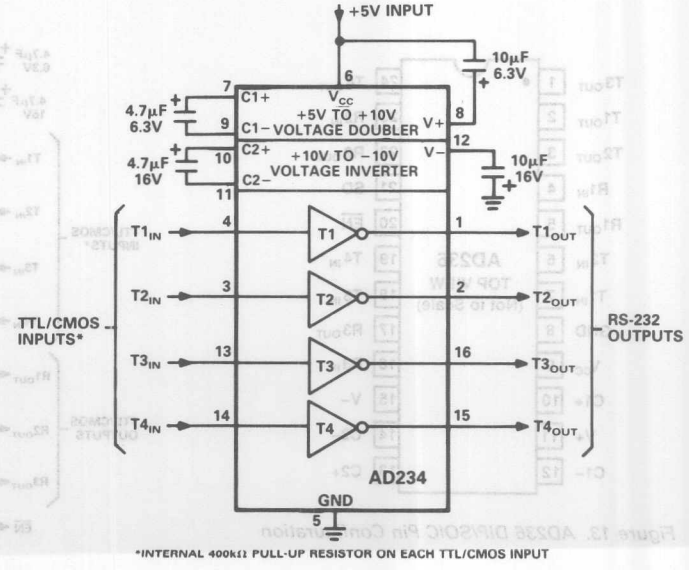


Figure 10. AD234 Typical Operating Circuit

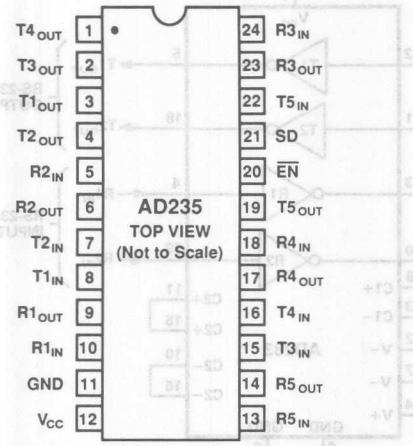


Figure 11. AD235 DIP Pin Configuration

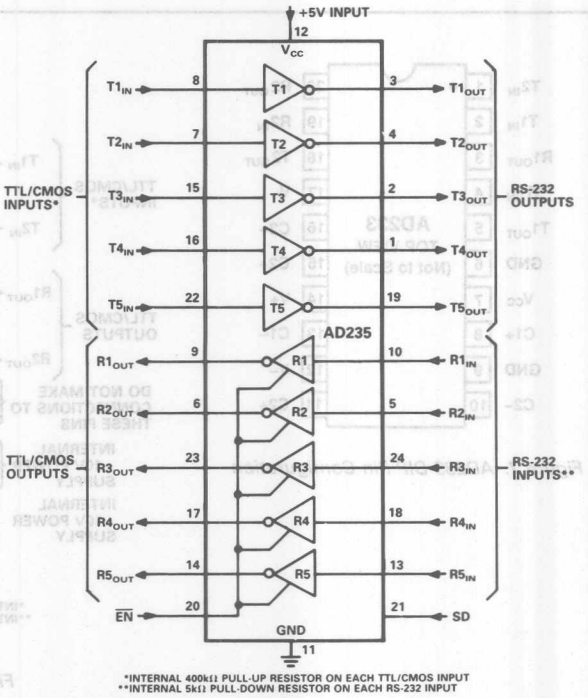


Figure 12. AD235 Typical Operating Circuit

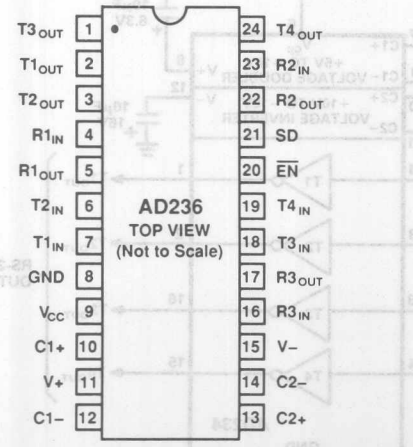


Figure 13. AD236 DIP/SOIC Pin Configuration

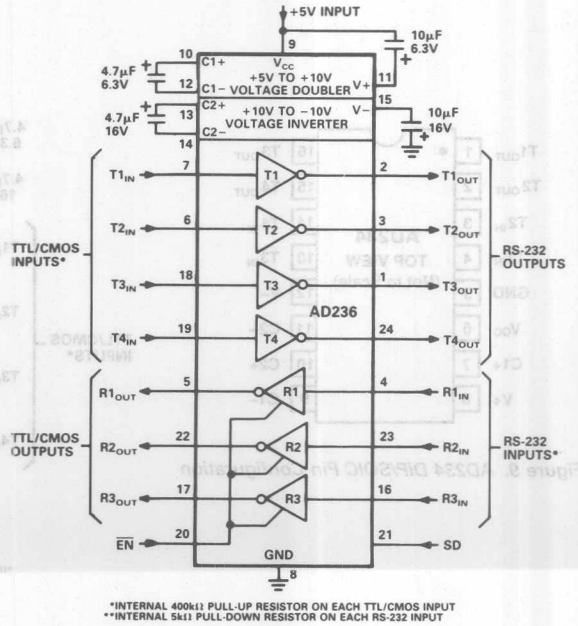


Figure 14. AD236 Typical Operating Circuit



Figure 15. AD237 DIP/SOIC Pin Configuration

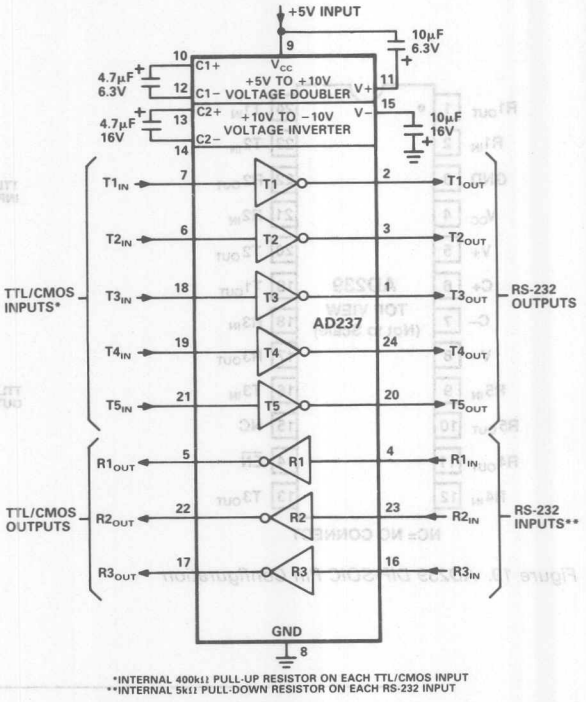


Figure 16. AD237 Typical Operating Circuit

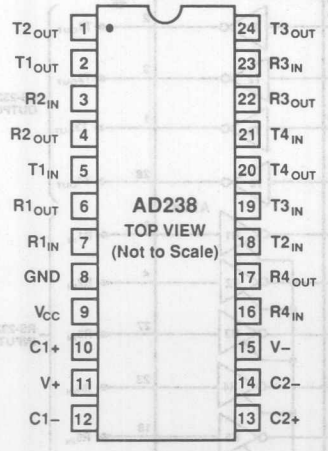


Figure 17. AD238 DIP/SOIC Pin Configuration

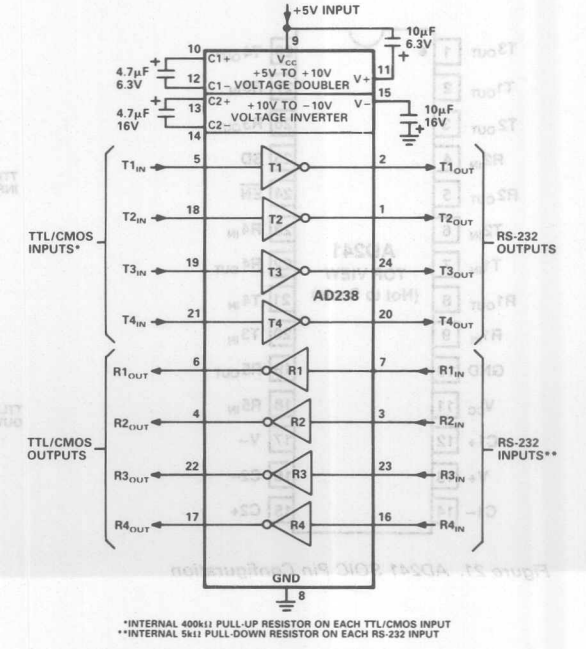


Figure 18. AD238 Typical Operating Circuit

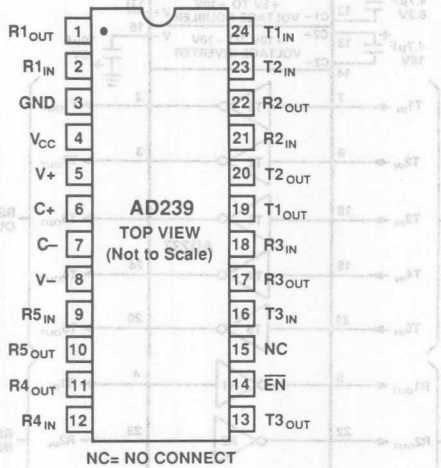


Figure 19. AD239 DIP/SOIC Pin Configuration

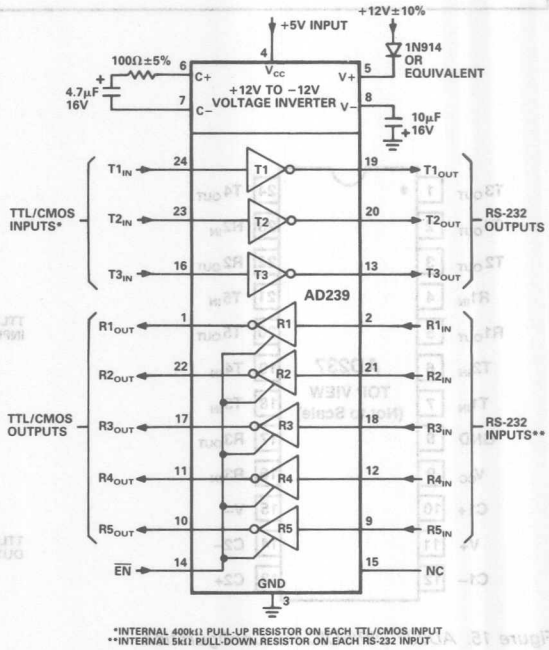


Figure 20. AD239 Typical Operating Circuit

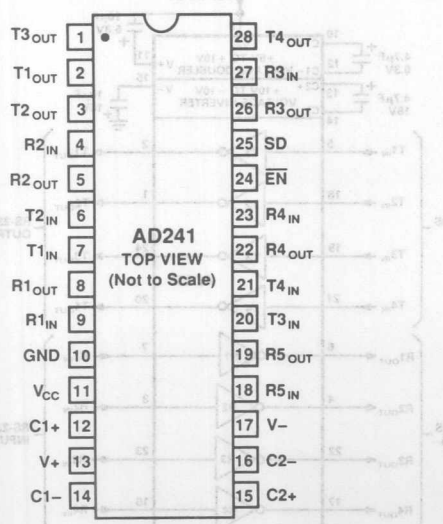


Figure 21. AD241 SOIC Pin Configuration

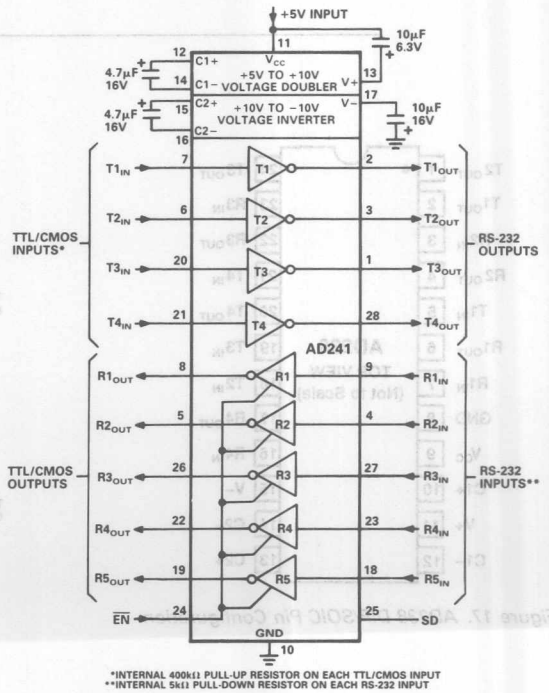


Figure 22. AD241 Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10% (AD231, AD232, AD234, AD236, AD238, AD239, AD241). 5 V± 5% (AD233, AD235).
V+	Internally generated positive supply (+10 V nominal) on all parts except AD231 and AD239. AD231 requires external 7.5 V to 13.2 V supply; AD239 requires external 10.8 V to 13.2 V supply.
V−	Internally generated negative supply (−10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	(AD231 and AD239 only). External capacitor (+ terminal) is connected to this pin.
C−	(AD231 and AD239 only). External capacitor (− terminal) is connected to this pin.
C1+	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (+ terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
C1−	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (− terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
C2+	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (+ terminal) is connected to this pin. (AD233) Internal capacitor connections, Pins 11 and 15 must be connected together.
C2−	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (− terminal) is connected to this pin. (AD233) Internal capacitor connections, Pins 10 and 16 must be connected together.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable Input (AD235, AD236, AD239, AD241). This is an active low input which is used to enable the receiver outputs. With $\overline{EN}$ = 0 V, the receiver outputs are enabled. With $\overline{EN}$ = 5 V, the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD	Shutdown Input. (AD230, AD235, AD236, AD241). With SD = 5 V, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. The supply current reduces to <5 μA making these parts ideally suited for battery operation.
NC	No Connect. No connections are required to this pin.

GENERAL INFORMATION

The AD230–AD241 family of RS-232 drivers/receivers are designed to solve interface problems by meeting the RS-232-C specifications while using a single digital +5 V supply. The RS-232-C standard requires transmitters which will deliver ±5 V minimum on the transmission channel and receivers which can accept signal levels down to ±3 V. The AD230–AD241 meet these requirements by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available to cover most communications needs.

The AD230, AD235, AD236 and AD241 are particularly useful in battery powered systems as they feature a low power shutdown mode which reduces power dissipation to less than 5 μW.

The AD233 and AD235 are designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The AD231 and AD239 include only a negative charge pump converter and are intended for applications where a positive 12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus the AD235, AD236, AD239 and AD241 feature an enable ($\overline{EN}$) function. When disabled, the receiver outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the AD230–AD241 consists of three main sections. These are:

(a) A charge pump voltage converter
(b) RS-232 to TTL/CMOS receivers
(c) TTL/CMOS to RS-232 transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated in Figures 23 and 24. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

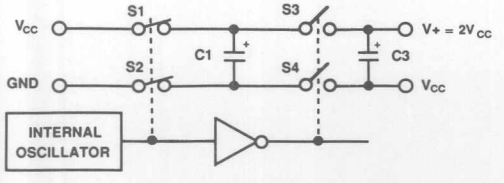


Figure 23. Charge-Pump Voltage Doubler

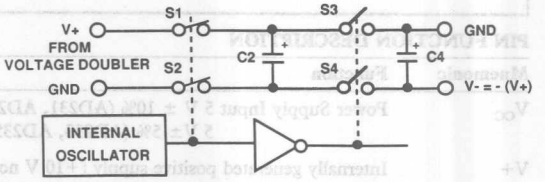


Figure 24. Charge-Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into RS-232-C output levels. With V_{CC} = +5 V and driving a typical RS-232-C load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232-C minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the RS-232-C standard, the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232-C input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

Shutdown (SD)

The AD230, AD235, AD236 and AD241 feature a control input which may be used to disable the part and reduce the power consumption to less than 5 μW. This is very useful in battery operated systems. With SD = 5 V, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off.

Enable Input

The AD235, AD236, AD239 and AD241 feature an enable input ($\overline{EN}$). It is used to enable the receiver outputs. With $\overline{EN}$ = 0 V the outputs are enabled. With $\overline{EN}$ = 5 V the outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 25.

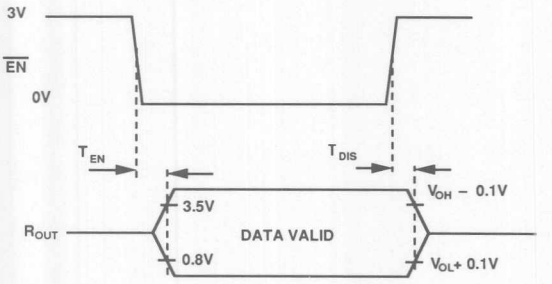


Figure 25. Enable Timing

APPLICATION HINTS

Protection for Shorts to ±15 V Supplies

The driver outputs are internally protected against shorting to ground, to other driver outputs, to V+ or to V−. In practice, these are the highest voltages likely to be encountered in an application. If the possibility exists for shorting to ±15 V, then it is recommended that external protection be provided. This may be done by connecting a series 220 Ω resistor on each transmitter output.

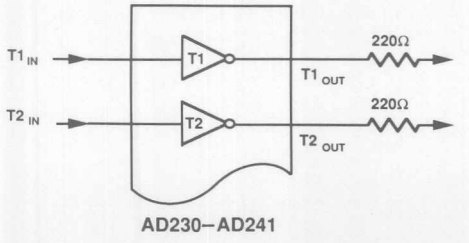


Figure 26. Protection for Shorts to ±15 V

Over-Voltage Protection for AD231, AD239

The AD231 and AD239 require an external +12 V supply as they do not contain an internal V+ generator. It is important that this supply be switched on before the 5 V, V_{CC} supply. If there is a possibility that the V_{CC} supply will be switched on first, or if the 12 V supply may be inadvertently shorted to ground, then it is recommended that a diode (1N914 or equivalent) be connected in series with the 12 V input. This will not affect normal operation but it ensures that under fault conditions, the device will be protected.

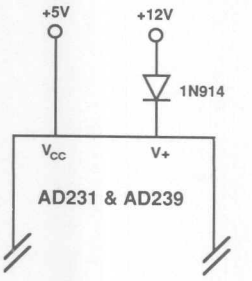


Figure 27. Diode Protection Scheme for AD231 and AD239

High Baud Rate Operation

The RS-232-C standard requires that *"For Data and Timing interchange Circuits, the time for the signal to pass through the transition region shall not exceed one millisecond or four percent of the nominal duration of the signal element on that interchange circuit, whichever is the lesser."* With the maximum transmission rate of 19.2 kbaud, this translates into a minimum slew rate of 3 V/μs. The typical slew rate of the AD230–AD241 is 3 V/μs under maximum loading conditions and therefore meets the standard.

The V.28 standard is more stringent and requires a transition time which will not exceed three percent of the nominal signal duration. This translates into a slew rate of 4 V/μs at the maximum 19.2 kbaud rate. In practice, less than ideal slew rates will have negligible affect on the data transmission. The result is that the valid mark/space duration is slightly shorter than the optimum because the signal spends more time in the transition region. The valid duration remains more than adequate for error-free reception even at maximum transmission rates and under worst case load conditions.

Driving Long Cables

In accordance with the RS-232-C standard, long cables are permissible provided that the total load capacitance does not exceed 2500 pF. For longer cables which do exceed this, then it is possible to trade off baud rate vs. cable length. Large load capacitances cause a reduction in slew rate, and hence the maximum transmission baud rate is decreased. The AD230–AD241 are designed so that the slew rate reduction with increasing load capacitance is minimized.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The AD230–AD241 have 0.5 V of hysteresis to guard against this. This ensures that, even in noisy environments, error-free reception can be achieved.

4

Figure 25. Enable Timing

Figure 26. Protection for Shorts to ±15 V

Figure 27. Diode Protection Scheme for ADM231 and ADM239

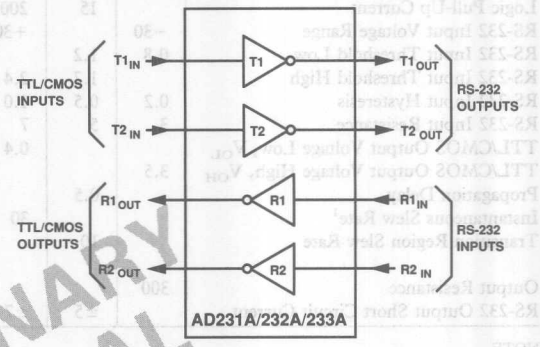
High Speed Enhanced, +5 V CMOS RS-232 Drivers/Receivers

AD231A/AD232A/AD233A

FEATURES
100 kB Transmission Rate
Small Charge Pump Capacitors
Single 5 V Power Supply
Meets All RS-232-C and V.28 Specifications
Two Drivers and Two Receivers
Onboard DC–DC Converters
±9 V Output Swing with +5 V Supply
Low Power CMOS: 10 mA Operation
±30 V Receiver Input Levels

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

4

GENERAL DESCRIPTION

The AD231A/AD232A/AD233A RS-232 line drivers/receivers are enhanced replacements for the AD2XX family offering a much higher transmission rate of 100 kilobaud. A highly efficient charge pump design allows smaller charge pump capacitors (0.1 μF) to be used giving a large reduction in PCB board space. All three parts contain two RS-232 drivers and two RS-232 receivers.

The AD231A is designed to operate from +5 V and +12 V supplies. An internal +12 V to −12 V charge pump voltage converter generates the −12 V supply.

The AD232A contains two internal charge pump voltage converters which make operation from a single +5 V supply possible. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels.

The AD233 does not require any external components and is particularly useful in applications where printed circuit board space is critical. On this part the charge pump capacitors are internally molded into the package.

Table I. Selection Table

Part Number	Power Supply Voltage	External Capacitors
AD231A	+5 V & +7.5 V to 13.2 V	2
AD232A	+5 V	4
AD233A	+5 V	None

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD231A/AD232A/AD233A—SPECIFICATIONS

(V_{CC} = +5 V ± 10%, V+ = 7.5 V to 13.2 V (AD231). All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		10	15	mA	No load, T_A = 25°C
V+ Power Supply Current		5	10	mA	No load, V+ = 12 V (AD231 Only)
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}
Logic Pull-Up Current		15	200	μA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Threshold High		1.7	2.4	V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	T_A = +25°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 3.2 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
Propagation Delay		0.5		μs	RS-232 to TTL
Instantaneous Slew Rate[1]			30	V/μs	C_L = 10 pF, R_L = 3–7kΩ, T_A = +25°C
Transition Region Slew Rate		10		V/μs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±5	±7	mA	

NOTE
[1] Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted.)

V_{CC} . . . . . +6 V
V+ . . . . . (V_{CC} − 0.3 V) to + 13 V
V− . . . . . +0.3 V to −13 V
Input Voltages
  T_{IN} . . . . . −0.3 V to (V_{CC} + 0.3 V)
  R_{IN} . . . . . ±30 V
Output Voltages
  T_{OUT} . . . . . (V+, +0.3 V) to (V−, −0.3 V)
  R_{OUT} . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous

Power Dissipation
  Cerdip . . . . . 675 mW
  (Derate 9.5 mW/°C above +70°C)
Plastic DIP . . . . . 375 mW
  (Derate 7 mW/°C above +70°C)
SOIC . . . . . 375 mW
  (Derate 7 mW/°C above +70°C)
Operating Temperature Range
  Commercial (J Version) . . . . . 0°C to +70°C
  Industrial (A Version) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

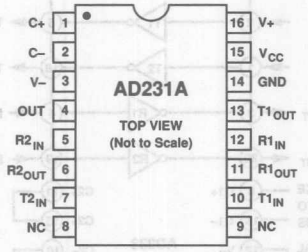


PRELIMINARY TECHNICAL DATA

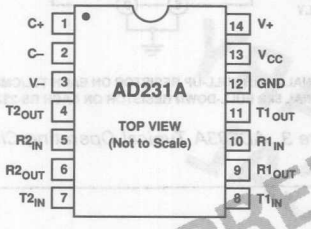
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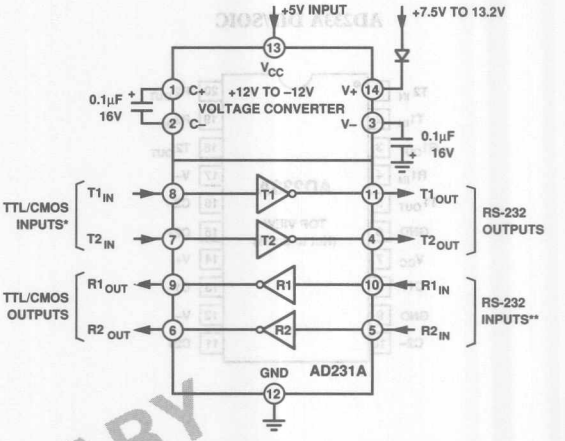
PIN CONFIGURATIONS

AD231A SOIC



AD231A DIP





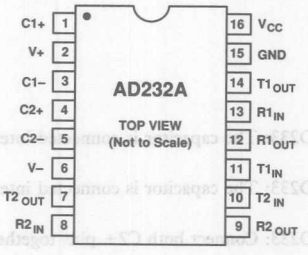
*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

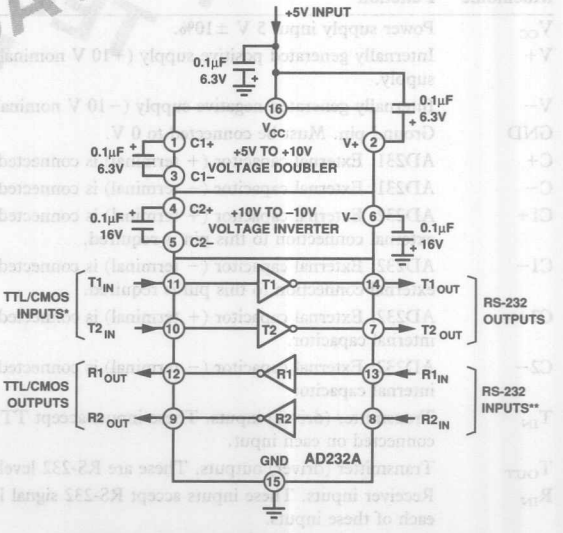
Figure 1. AD231A Typical Operating Circuit

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION

AD232A DIP/SOIC





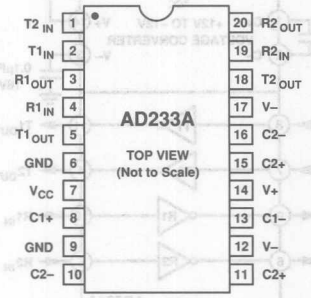
*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

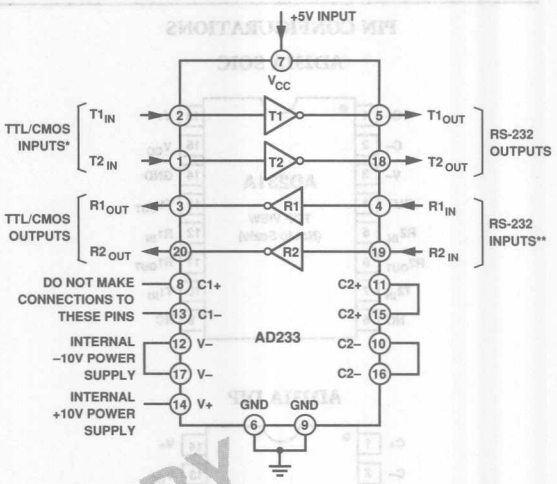
Figure 2. AD232A Typical Operating Circuit

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PIN CONFIGURATION

AD233A DIP/SOIC





*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 3. AD233A Typical Operating Circuit

PRELIMINARY TECHNICAL DATA

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power supply input 5 V ±10%.
V+	Internally generated positive supply (+10 V nominal) on AD232, AD233. AD231 requires external 7.5 V to 13.2 V supply.
V−	Internally generated negative supply (−10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	AD231: External capacitor (+ terminal) is connected to this pin.
C−	AD231: External capacitor (− terminal) is connected to this pin.
C1+	AD232: External capacitor (+ terminal) is connected to this pin. AD233: The capacitor is connected internally and no external connection to this pin is required.
C1−	AD232: External capacitor (− terminal) is connected to this pin. AD233: The capacitor is connected internally and no external connection to this pin is required.
C2+	AD232: External capacitor (+ terminal) is connected to this pin. AD233: Connect both C2+ pins together to use the internal capacitor.
C2−	AD232: External capacitor (− terminal) is connected to this pin. AD233: Connect both C2− pins together to use the internal capacitor.
T_{IN}	Transmitter (driver) inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (driver) outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
R_{OUT}	Receiver outputs. These are TTL/CMOS levels.
NC	No Connect. No connections are required to this pin.

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receivers are designed to solve interface problems by meeting the RS-232-C specifications while using a single digital +5 V supply. The RS-232-C standard requires transmitters which will deliver ±5 V minimum on the transmission channel and receivers which can accept signal levels down to ±3 V. The parts achieve this by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum.

The AD232 contains an internal voltage doubler and a voltage inverter which generates ±10 V from the +5 V input. External 0.1 μF capacitors are required for the internal voltage converter.

The AD233 is designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The AD231 contains only a negative charge pump converter and is intended for applications where a positive 12 V is available.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are:

(a) A charge pump voltage converter
(b) RS-232 to TTL/CMOS receivers
(c) TTL/CMOS to RS-232 transmitters.

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated below. Firstly the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

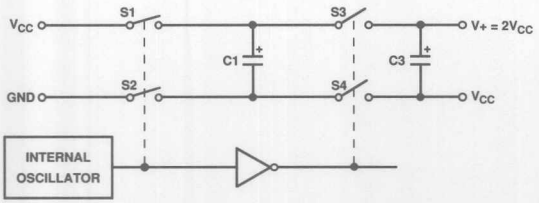


Figure 4. Voltage Doubler

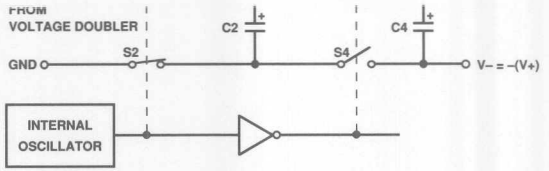


Figure 5. Voltage Inverter

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into RS-232-C output levels. With V_{CC} = +5 V and driving a typical RS-232-C load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232-C minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the RS-232-C standard the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232-C input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

PRELIMINARY TECHNICAL DATA

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Figure 5. Voltage Inverter

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into RS-232-C output levels. With V_{CC} = +5 V and driving a typical RS-232-C load, the output voltage swing is ±5 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232-C minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = +5 V, the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high, forcing the outputs into a low state.

As required by the RS-232-C standard the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232-C input levels (±3 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

ANALOG DEVICES

LC²MOS GSM Baseband I/O Port

AD7001

FEATURES

- Single +5 V Supply
- Single Channel 8-Bit A/D Converter
  - 2.16 MHz Sampling Rate
  - Receive Difference Amplifier
  - Programmable Gain Amplifier
- Two 10-Bit D/A Converters
  - 2 MHz Throughput Rate
  - Simultaneous Update Mode
  - 4th Order Antialias Filters
- Single Serial Auxiliary 8-Bit D/A Converter
- Fast Interface Port
- Power Down Mode(s)
- On-Chip Voltage Reference
- 44-Pin PQFP

APPLICATIONS

- Digital Cellular Telephony
- Private Mobile Telephony
- Satellite Baseband Digitization
- Radar Signal Processing
- Signal Generation and Acquisition

GENERAL DESCRIPTION

The AD7001 is a complete low power, LC²MOS, input/output port with single +5 V power supply. The part is designed to perform the conversion of I and Q signals in the transmit and receive data paths of Pan-European Digital Cellular Telephone (GSM) systems. However, the device can be used in any application requiring fast and accurate signal conversion in the sub-600 kHz band.

Besides providing two high accuracy 10-bit digital-to-analog converters in the transmit path and a single fast analog-to-digital converter in the receive path, the part also provides antialiasing filters and signal conditioning functions. The difference amplifier is usable in the I and Q mixing function.

A single serial 8-bit DAC is included for such functions as AFC, AGC and carrier signal shaping in the IF/RF portion of the system.

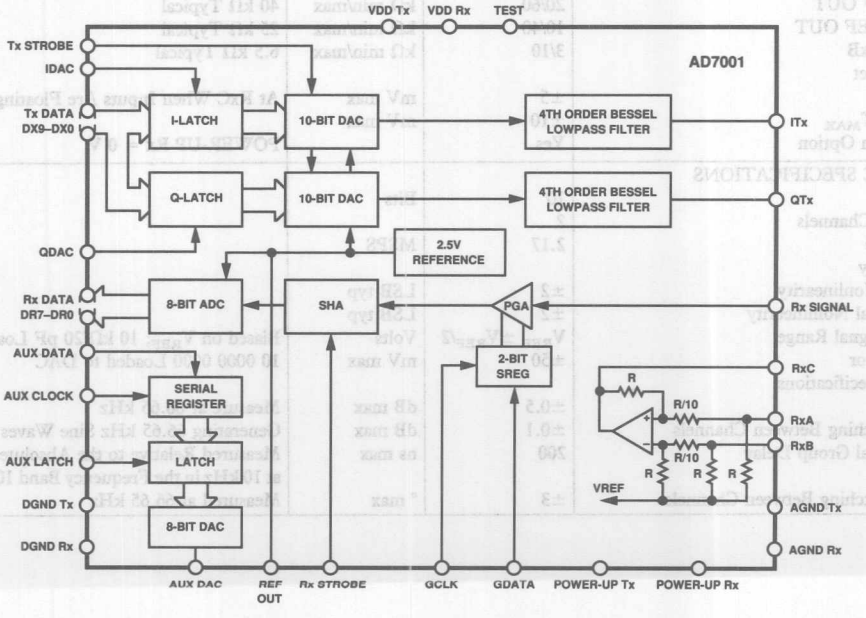
All logic necessary for control of this device is contained on board. A fast data bus allows easy interface with all commonly available microprocessors.

As it is a necessity for all GSM mobile systems to use the lowest possible power, the device has power down options for both the transmit path and the receive path which are independent of each other. The AD7001 is housed in a space efficient 44-pin PQFP (Plastic Quad Flatpack).

PRELIMINARY TECHNICAL DATA

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FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7001—SPECIFICATIONS[1]

(V_{DD} Tx = V_{DD} Rx = +5 V ± 10%; Test = AGNDTx = AGNDRx = DGNDTx = DGNDRx = 0 V; T_A = T_{MIN} to T_{MAX}, POWER-UP Tx = POWER-UP Rx = V_{DD}, unless otherwise stated)

Parameter	AD7001A	Units	Test Conditions/Comments
ADC SPECIFICATIONS			
Resolution	8	Bits	
Signal Input Range	V_{REF} ±V_{REF}/2	Volts	PGA = 1
	V_{REF} ±V_{REF}/4	Volts	PGA = 2
	V_{REF} ±VREF/8	Volts	PGA = 4; All Biased on V_{REF}
Sampling Rate	2.17	MSPS	
DC Accuracy			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	No Missing Codes Guaranteed
Offset Error			
@ +25°C	±1.5	LSB max	PGA = 1
T_{MIN} to T_{MAX}	±3	LSB max	PGA = 1
T_{MIN} to T_{MAX}	TBD	LSB max	PGA = 2 or 4
Full-Scale Error			Positive and Negative
@ +25°C	±2.5	LSB max	PGA = 1
T_{MIN} to T_{MAX}	±3.5	LSB max	PGA = 1
T_{MIN} to T_{MAX}	TBD	LSB max	PGA = 2 or 4
Input Resistance (DC)	5	kΩ min	
Input Capacitance	50	pF max	
Dynamic Specifications			V_{IN} = 500 kHz Full-Scale Sine Wave,
Signal-to-Noise Ratio	44	dB min	f_{SAMPLE} = 2.16 MHz, PGA = 1
Peak Spurious Noise	TBD	dB max	
Total Harmonic Distortion	−46	dB max	
Gain Accuracy	±0.5	dB max	PGA = 1, 2 or 4
Coding	Binary		
Power Down Option	Yes		POWER-UP Rx = 0 V
DIFFERENCE AMPLIFIER SPECIFICATIONS			
Differential Gain	20	dB min	V_{IN} = 474 kHz ± 80 kHz; Biased on V_{REF}
Gain Accuracy	±1	dB max	
Input Common-Mode Rejection Ratio	30	dB min	RxA = RxB = 0.4 V pk–pk @ 500 kHz
Distortion	−40	dB max	V_{OUT} = 1 V pk–pk @ 500 kHz; Biased on V_{REF}
Input Impedance			
RxA to REF OUT	20/60	kΩ min/max	40 kΩ Typical
RxB to REF OUT	10/40	kΩ min/max	25 kΩ Typical
RxA to RxB	3/10	kΩ min/max	6.5 kΩ Typical
Output Offset			
@ +25°C	±5	mV max	At RxC When Inputs Are Floating
T_{MIN} to T_{MAX}	±10	mV max	
Power-Down Option	Yes		POWER-UP Rx = 0 V
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Number of Channels	2		
Update Rate	2.17	MSPS	
DC Accuracy			
Integral Nonlinearity	±2	LSB typ	
Differential Nonlinearity	±2	LSB typ	
Output Signal Range	V_{REF} ±V_{REF}/2	Volts	Biased on V_{REF}; 10 kΩ/20 pF Load
Offset Error	±50	mV max	10 0000 0000 Loaded to DAC
Dynamic Specifications			
Gain	±0.5	dB max	Measure at 66.65 kHz
Gain Matching Between Channels	±0.1	dB max	Generating 66.65 kHz Sine Waves
Differential Group Delay	200	ns max	Measured Relative to the Absolute Group Delay at 10 kHz in the Frequency Band 10 kHz–200 kHz
Phase Matching Between Channels	±3	° max	Measured at 66.65 kHz

PRELIMINARY TECHNICAL DATA

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Parameter	AD7001A	Units	Test Conditions/Comments
GMSK Spectrum Mask			
100 kHz	+0.5	dB min	
200 kHz	−30	dB min	
250 kHz	−33	dB min	
400 kHz	−60	dB min	
600 kHz–1000 kHz	−70	dB min	
>1 MHz	TBD	dB min	
GMSK Phase Trajectory Error	TBD	° rms typ	
	TBD	° Peak typ	
LP Filter Response			
300 kHz	−3	dB typ	
1 MHz	−20	dB typ	
2 MHz	−44	dB typ	
SNR + THD (0 MHz–1.08 MHz)			Producing 66.65 kHz Sine Wave with 2.17 MHz
@ +25°C	54	dB min	Updated Rate
T_{MIN} to T_{MAX}	52	dB min	
Peak Spurious Noise (0 MHz–6.5 MHz)	−70	dB typ	
Coding	Binary		
Power-Down Option	Yes		POWER-UP Tx = 0 V
AUXILIARY DAC SPECIFICATIONS			
Resolution	8	Bits	
DC Accuracy			
Integral Nonlinearity[2]	±2	LSB max	
Differential Nonlinearity[2]	±1	LSB max	Guaranteed Monotonic
Offset Error	1.5 ± 1	LSB max	
Gain Error	±2	LSB max	
Output Signal Range	0 to V_{REF}	Volts	
Output Impedance	2	kΩ max	I_{SINK} = 250 μA
	20	Ω typ	I_{SOURCE} = 250 μA
	850	Ω typ	I_{SINK} = 250 μA
Coding	Binary		
Power-Down Option	Yes		POWER-UP Tx = 0 V
REFERENCE SPECIFICATIONS			
V_{REF}, Reference Output	2.4/2.6	V min/V max	R_L = 10 kΩ, C_L = 10 nF
Reference Variation[3]	5	mV max	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	4.0	V min	$\|I_{OUT}\| \leq 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			
All Sections	55	mA max	
ADC and Bandpass Filter Active[4]	35	mA max	POWER-UP Tx = 0 V
Signal DACs and AUX DAC Active[5]	20	mA max	POWER-UP Rx = 0 V
All Sections Powered Down[4, 5]	2	mA max	POWER-UP Tx = POWER-UP Rx = 0 V

NOTES
[1]Operating temperature ranges as follows: A Version; −25°C to +85°C.
[2]AUX DAC DC linearity is measured between codes 3 and 255, see terminology.
[3]Variation of the Reference between different POWER-UP Tx and POWER-UP Rx modes.
[4]Measured while the digital inputs to the transmit interface are static.
[5]Measured while the digital inputs to the receive interface are static.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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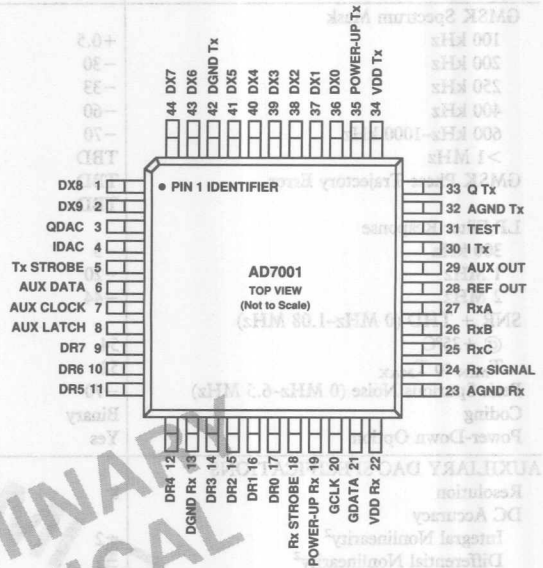
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} Tx, V_{DD} Rx to AGND . . . . . −0.3 V to +6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . −25°C to +85°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PRELIMINARY TECHNICAL DATA

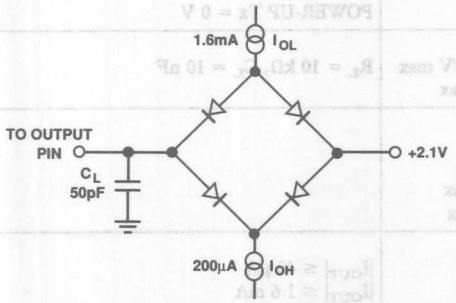


Figure 1. Load Circuit for Access Time Test

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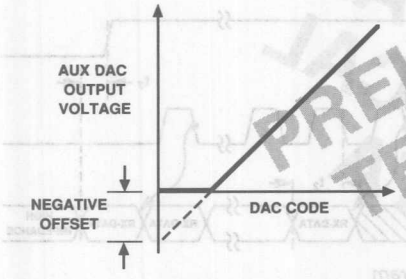
TERMINOLOGY

Signal Input Range
The input signal range for Rx SIGNAL is biased about V_{REF}. It can go $\pm V_{REF}/2$, $\pm V_{REF}/4$ or $\pm V_{REF}/8$ volts (depending on the PGA setting) about this point.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the DAC or ADC transfer function.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and an ideal 1 LSB change between any two adjacent codes.

Auxiliary DAC Linearity
The AUX DAC output amplifier can have an internal negative offset, even though the part operates from a single (5 V) supply. However, because the negative rail is 0 V, the output cannot actually go below ground, resulting in the transfer function shown below. This "Knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.



Effect of Negative Offset

Normally, linearity is measured between zero (all 0s) and full scale (all 1s) after offset and full scale have been adjusted out, but this is not possible with the AD7001 AUX DAC if the offset is negative. Instead, linearity of the AUX DAC is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the AD7001 AUX DAC the linearity is measured between codes 3 and 255.

Bias Offset Error
This is the offset error (in LSBs) in the DAC or ADC and is measured with respect to V_{REF}.

Signal-to-Noise Ratio
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. SNR is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by:

$$SNR = (6.02\ N + 1.76) dB$$

Differential Group Delay
Absolute group delay is the rate of change of phase versus frequency, $d\phi/df$. For the AD7001, differential group delay is the absolute group delay in a specified band relative to the absolute group delay at 10 kHz. The specified band for the AD7001 is 10 kHz–200 kHz.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Output Signal Span
This is the output signal range for the transmit channel section and the auxiliary DAC section. For the transmit channel the span is ± 1.25 volts centered on V_{REF} and for the auxiliary DAC section it is 0 to $+V_{REF}$.

Output Signal Full-Scale Accuracy
This is the accuracy of the full scale output (all 1s loaded to the DACs) on the transmit channel and is expressed in dBs.

DAC Offset Error
This is the amount of offset in the transmit DACs and the auxiliary DACs and is expressed in mVs for the transmit section and in LSBs for the auxiliary section.

DAC Gain Error
This is a measure, expressed in LSBs, of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. In the AD7001, gain error is specified for the auxiliary section.

Output Impedance
This is a measure, expressed in kΩs, of the drive capability of the auxiliary DAC output.

GMSK Spectrum Mask
This is the output spectrum of the I and Q transmit channels when transmitting a random sequence of data bits using GMSK modulation, as specified in the GSM standard, using a bit truncation of ± 4-bit periods.

GMSK Phase Trajectory Error
This is a measure of the phase error between the transmitted phase of an ideal GMSK modulator and the actual phase transmitted by the AD7001, when transmitting a random sequence of data bits. It is specified as a peak phase error and also as a rms phase error.

PRELIMINARY TECHNICAL DATA

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ADC TIMING unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_1	100	100	µs min	POWER-UP Rx to Rx STROBE Setup Time
t_2	380	380	ns min	Rx STROBE to New Rx DATA
	440	440	ns max	
t_3	460	460	ns min	Rx STROBE Period
t_4	200	200	ns min	Rx STROBE High Period
t_5	200	200	ns min	Rx STROBE Low Period
t_6	3680	3680	ns max	ADC Settling Time After Switching from V_{REF} to Rx SIGNAL
t_7	0	0	ns min	POWER-UP Rx Going Low to Rx DATA
	40	40	ns max	3-State

NOTES
[1]All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 1.
[3]t_2 is measured with the load circuit of Figure 1 and is defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

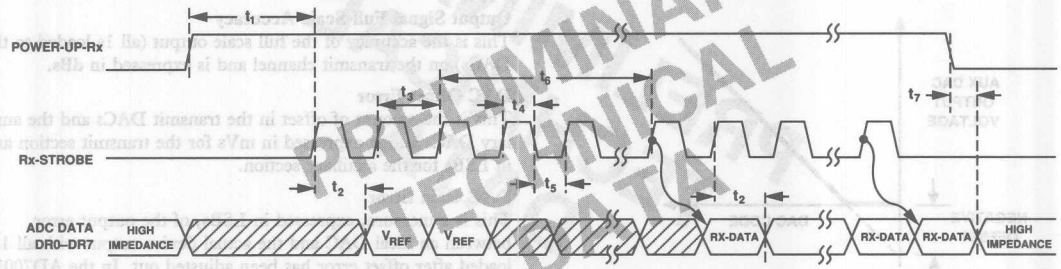


Figure 2. ADC Timing Diagram

PGA TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 10%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0 V; unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_6	150	150	ns min	GCLK Period
t_7	75	75	ns min	GCLK Low Period
t_8	75	75	ns min	GCLK High Period
t_9	40	40	ns min	GDATA to GCLK Setup Time
t_{10}	50	50	ns min	GDATA to GCLK Hold Time

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 10 ns.
[2]Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

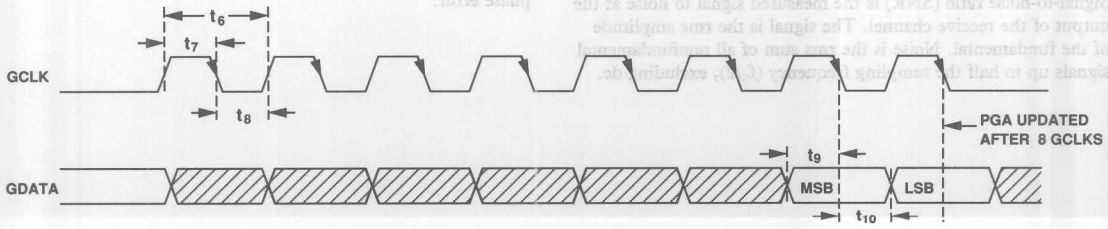


Figure 3. PGA Timing Diagram

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SIGNAL DAC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 10%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0V; unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_{11}	100	100	µs min	POWER-UP Tx to Tx STROBE Setup Time.
t_{12}	100	100	ns min	IDAC, QDAC Pulse Width
t_{13}	40	40	ns min	Tx DATA Setup Time
t_{14}	10	10	ns min	Tx DATA Hold Time
t_{15}	50	50	ns min	IDAC to Tx STROBE Setup Time
t_{16}	50	50	ns min	QDAC to Tx STROBE Setup Time
t_{17}	100	100	ns min	Tx STROBE Pulse Width
t_{18}	400	400	ns min	Tx STROBE Period

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 20 ns.
[2]Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

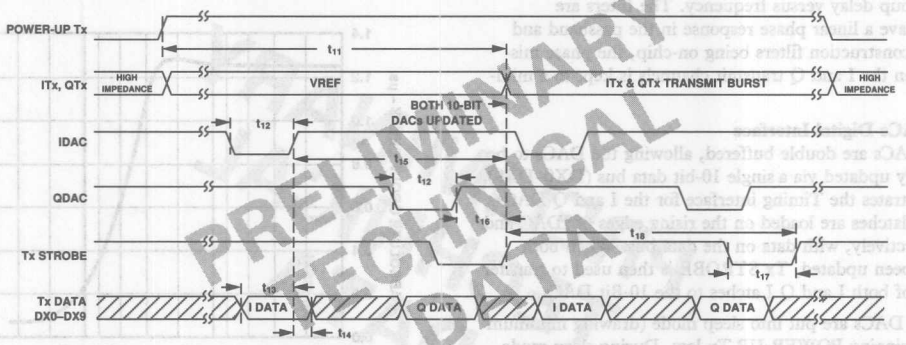


Figure 4. Signal DAC Timing Diagram

AUXILIARY DAC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 10%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0 V; unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_{19}	75	75	ns min	AUX CLOCK Low Duration
t_{20}	75	75	ns min	AUX CLOCK High Duration
t_{21}	40	40	ns min	AUX DATA to AUX CLOCK Setup Time
t_{22}	50	50	ns min	AUX DATA to AUX CLOCK Hold Time
t_{23}	50	50	ns min	AUX LATCH to AUX CLOCK Setup Time
t_{24}	40	40	ns min	AUX LATCH to AUX CLOCK Hold Time
t_{25}	8 $(t_1 + t_2)$	8 $(t_1 + t_2)$	ns min	AUX LATCH Duration

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V; tr = tf = 20 ns.
[2]Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

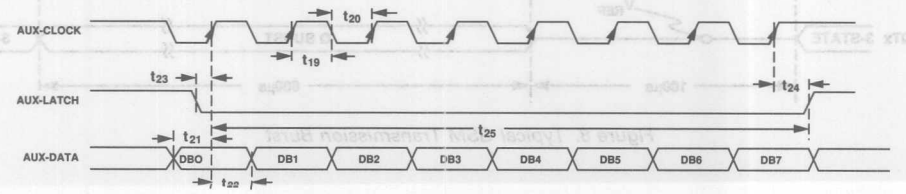


Figure 5. Auxiliary DAC Timing Diagram

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TRANSMIT SECTION

The transmit section of the AD7001 performs the baseband conversion of I and Q (In-phase and Quadrature) waveforms for the GSM Pan-European Digital Cellular Communications system. The transmit channel consists of two 10-bit DACs, followed by 4th order Bessel reconstruction filters. Also included in the transmit channel is a single 8-bit auxiliary DAC.

Transmit DACs

The 10-bit DACs can be used to perform the conversion of I and Q waveforms when implementing GMSK modulation in accordance with the GSM 5.04 standard.

Reconstruction Filters

The reconstruction filters smooth the DAC output signals, providing continuous time I and Q waveforms at the output pins. These are 4th order Bessel low-pass filters with a cutoff frequency of approximately 300 kHz. Figure 6 shows a typical transmit filter frequency response, while Figure 7 shows a typical plot of group delay versus frequency. The filters are designed to have a linear phase response in the passband and due to the reconstruction filters being on-chip, the phase mismatch between the I and Q transmit channels is kept to a minimum.

Transmit DACs Digital Interface

The 10-bit DACs are double buffered, allowing the DACs to be simultaneously updated via a single 10-bit data bus (DX0–DX9). Figure 4 illustrates the Timing interface for the I and Q DACs. The I and Q latches are loaded on the rising edges of IDAC and QDAC, respectively, with data on the data bus. When both latches have been updated, Tx STROBE is then used to transfer the contents of both I and Q Latches to the 10-Bit DACs.

The transmit DACs are put into sleep mode (drawing minimum current) by bringing POWER-UP Tx low. During sleep mode the I Tx and Q Tx outputs go into high impedance. On POWER-UP Tx going high, the I and Q DACs are reset to V_{REF}, which prevents any imbalance between the I and Q channels when the I Tx and Q Tx outputs are ac coupled to the IF/RF modulator. Allow time for the transmit section to fully power-up before updating the I and Q latches. Figure 8 shows a typical GSM transmission burst.

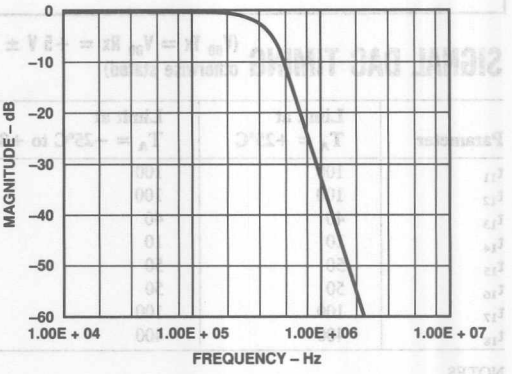


Figure 6. Transmit Filter Frequency Response

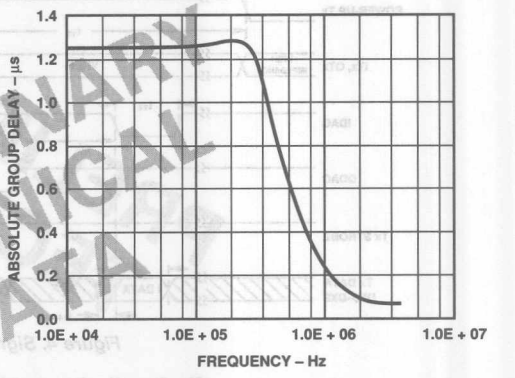


Figure 7. Transmit Filter Group Delay

PRELIMINARY TECHNICAL DATA

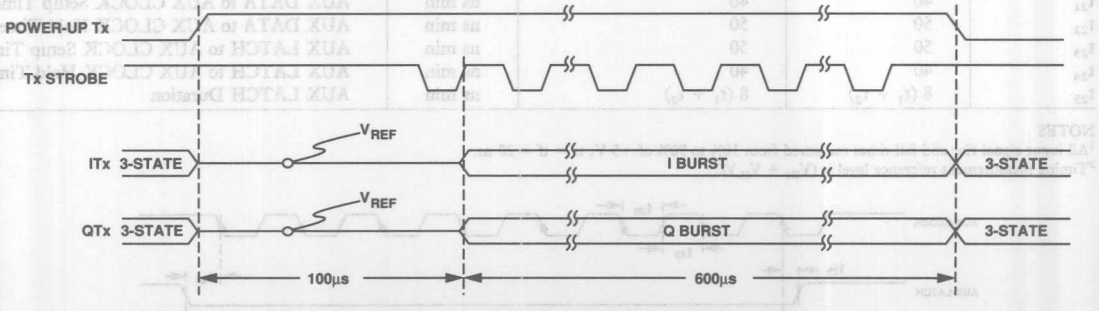


Figure 8. Typical GSM Transmission Burst

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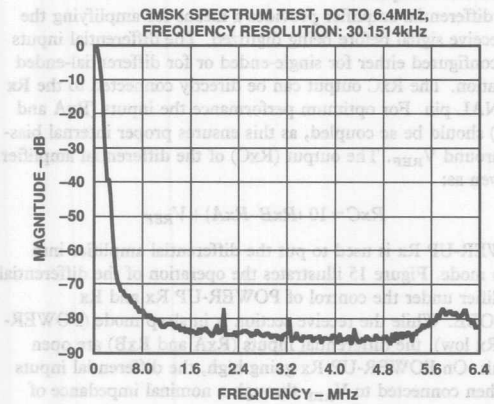


Figure 9. GMSK Spectrum Mask Generated Using the I Transmit Channel

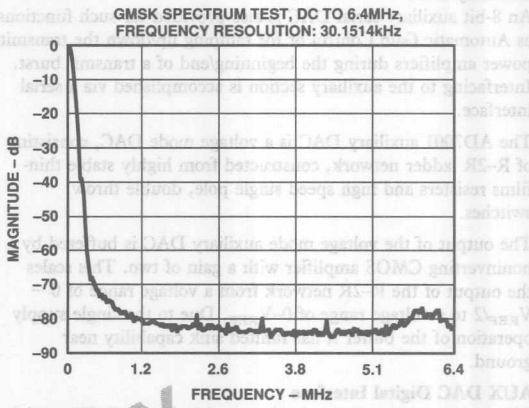


Figure 10. GMSK Spectrum Mask Generated Using the Q Transmit Channel

4

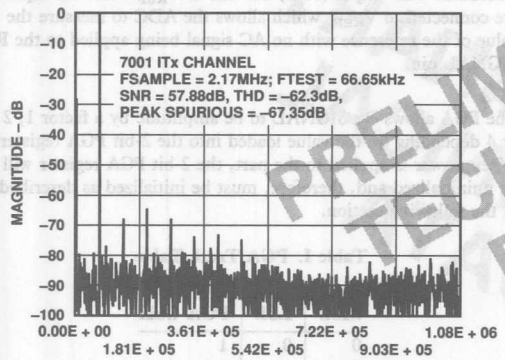


Figure 11. Frequency Plot of the I Channel Generating a Sine Wave at 66.65 kHz

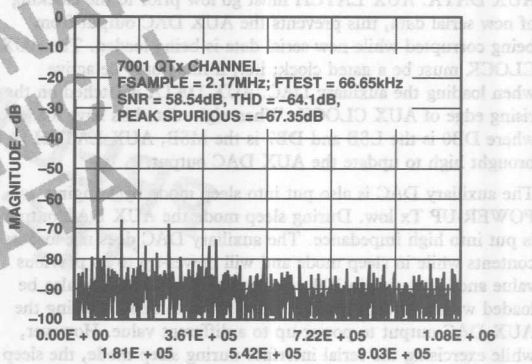


Figure 12. Frequency Plot of the Q Channel Generating a Sine Wave at 66.65 kHz

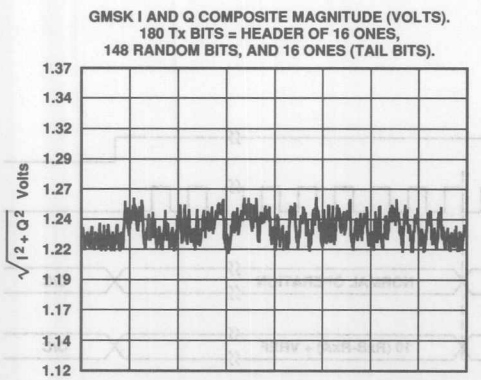


Figure 13. Typical Plot of the GMSK I and Q Waveforms Generated Using the I and Q Transmit Channels

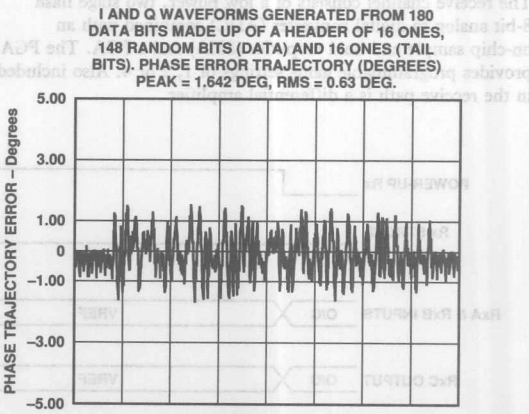


Figure 14. Typical Plot of the GMSK Phase Error Trajectory Generated Using the AD7001 I and Q Transmit Channels

PRELIMINARY TECHNICAL DATA

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Auxiliary DAC

An 8-bit auxiliary serial DAC is also provided for such functions as Automatic Gain Control or for ramping up/down the transmit power amplifiers during the beginning/end of a transmit burst. Interfacing to the auxiliary section is accomplished via a serial interface.

The AD7001 auxiliary DAC is a voltage mode DAC, consisting of R–2R ladder network, constructed from highly stable thin-films resisters and high speed single pole, double throw switches.

The output of the voltage mode auxiliary DAC is buffered by a noninverting CMOS amplifier with a gain of two. This scales the output of the R–2R network from a voltage range of 0 – $V_{REF}/2$ to a voltage range of 0–V_{REF}. Due to the single supply operation of the buffer it has limited sink capability near ground.

AUX DAC Digital Interface

The serial interface timing is illustrated in Figure 5. The serial interface is controlled using AUX CLOCK, AUX LATCH and AUX DATA. AUX LATCH must go low prior to the clocking of new serial data, this prevents the AUX DAC output from being corrupted while new serial data is being loaded. The AUX CLOCK must be a gated clock; i.e., it must only be active when loading the auxiliary DAC. AUX DATA is latched on the rising edge of AUX CLOCK. When eight data bits have loaded, where DB0 is the LSB and DB7 is the MSB, AUX LATCH is brought high to update the AUX DAC output.

The auxiliary DAC is also put into sleep mode by bringing POWER-UP Tx low. During sleep mode the AUX DAC output is put into high impedance. The auxiliary DAC does not lose its contents while in sleep mode and will power-up to its previous value and settle within 100 µs. The auxiliary DAC can also be loaded with new data while in sleep mode thereby allowing the AUX DAC output to power-up to a different value. However, while exercising the serial interface during sleep mode, the sleep current will increase.

RECEIVE SECTION

The receive channel consists of a low power, two stage flash 8-bit analog to digital converter (ADC) combined with an on-chip sample and hold amplifier (SHA) and a PGA. The PGA provides programmable gains settings of 1, 2 or 4. Also included in the receive path is a differential amplifier.

Differential Amplifier

The differential amplifier provides a means for amplifying the IF receive signal before being digitized. The differential inputs can configured either for single-ended or for differential-ended operation. The RxC output can be directly connected to the Rx SIGNAL pin. For optimum performance the inputs (RxA and RxB) should be ac coupled, as this ensures proper internal biasing around V_{REF}. The output (RxC) of the differential amplifier is given as:

$$RxC = 10\ (RxB–RxA) + V_{REF}$$

POWER-UP Rx is used to put the differential amplifier into sleep mode. Figure 15 illustrates the operation of the differential amplifier under the control of POWER-UP Rx and Rx STROBE. While the receive section is in sleep mode (POWER-UP Rx low), the differential inputs (RxA and RxB) are open circuit. On POWER-UP Rx going high, the differential inputs are then connected to V_{REF} through a nominal impedance of 300 Ω. The inputs are connected for normal operation after two Rx STROBE cycles, i.e., on the third rising edge of Rx STROBE. The output (RxC) also sits at V_{REF} while the inputs are connected to V_{REF}, which allows the ADC to measure the value of the reference with no AC signal being applied to the Rx SIGNAL pin.

PGA

The PGA allows Rx SIGNAL to be amplitude by a factor 1, 2 or 4 depending on the value loaded into the 2-bit PGA register. When power is applied to the part, the 2-bit PGA register will be uninitialized and, therefore, must be initialized as described in the following section.

Table I. PGA Truth Table

MSB	LSB	PGA Gain
0	0	1
0	1	2
1	0	2
1	1	4

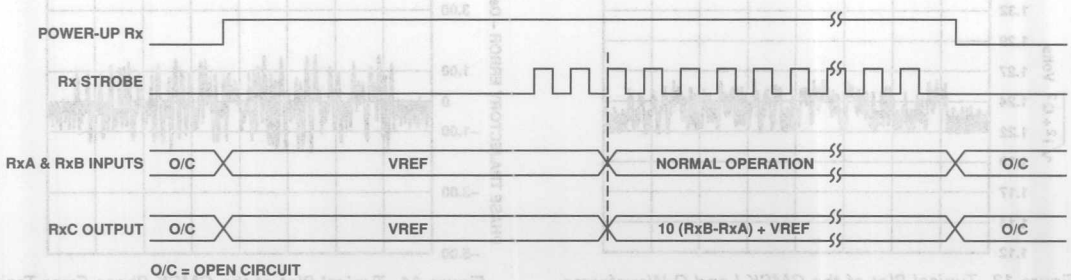


Figure 15. Operation of the Differential Amplifier

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PGA Digital Interface

The receive channel PGA is programmed via a two pin serial interface (GCLK and GDATA). Figure 3 illustrates the serial interface timing diagram for the PGA. GDATA is latched on the falling edge of GCLK. GCLK must be a gated clock, active only when updating the PGA. Eight clock cycles are required to update the PGA setting, where the first six cycles are dummy cycles and only the last two clock cycles load new data into the 2-bit PGA register. These last two data bits are loaded MSB first. On the last falling edge of GCLK the PGA is set to a gain of 1, 2 or 4, depending on the 2-bit value contain in the PGA register. Table I illustrates the truth table for the PGA setting.

On initial power being applied to the part, the PGA serial logic will be in an undetermined state; however, each time the receive section is brought out of sleep mode (POWER-UP Rx brought high) the serial logic is reset. In order to correctly initialize the 2-bit PGA register, one must first reset the serial logic after power has initially been applied to the part. The PGA can be updated at any time, except when the serial logic is being reset. Hence, one should not attempt to update the PGA register immediately before or after POWER-UP Rx goes high. A guard band of 150 ns before and 300 ns after POWER-UP Rx going high is sufficient for correct operation.

SHA and ADC

The 8-bit flash ADC, combined with the on-board Sample and Hold Amplifier (SHA), generates 8-bit samples up to a data rate of 2.17 MHz. When the receive section is brought out of sleep mode the receive path is initially connected to V_{REF} to enable the ADC to measure on-chip offsets. Hence the first two ADC conversions, following POWER-UP Rx going high, are a measurement of the reference. However, the AD7001 does not subtract the offset measurement from subsequent conversions and, if so required, should be carried by the DSP/ASIC following the receive section. As these two conversions may not yield the same offset value, one should average the two conversions to obtain an overall offset value.

ADC Digital Interface

Figure 2 illustrates the receive timing interface. Control of the receive interface is effected through the use of the POWER-UP Rx and Rx STROBE pins with the receive data available on a parallel interface (DR0–DR7).

On POWER-UP Rx going high, time (t_1) must be provided to allow the receive circuitry to become fully powered up. Rx STROBE can now be activated to initial ADC conversions. As described earlier, the first two conversions are of the reference, after which the input to the PGA is switched from the reference to the Rx SIGNAL input pin. Although the ADC will continue to convert, time (t_6) must be allowed for the ADC conversions to settle due to the internal switching from V_{REF} to the Rx SIGNAL input. Conversions are initiated on the rising edge of Rx STROBE and once the conversion is complete, the DR0–DR7 pins are updated.

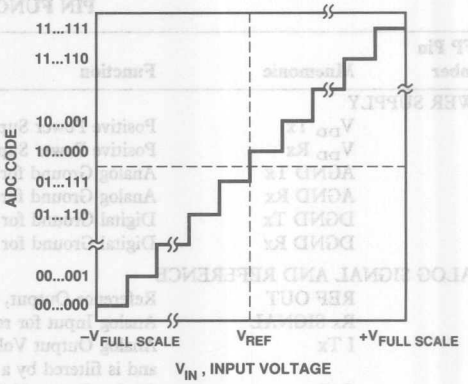


Figure 16. ADC Transfer Function

VOLTAGE REFERENCE

The AD7001 contains an on-chip bandgap reference which provides a low noise, temperature compensated reference to the I/Q transmit DACs and the I/Q receive ADC. The reference is also made available on the REF OUT pin and can be used to bias other analog circuitry in the IF section.

When both the transmit section and the receive section are in sleep mode (POWER-UP Tx and POWER-UP Rx low), the reference output buffer is also powered down by approximately 80%.

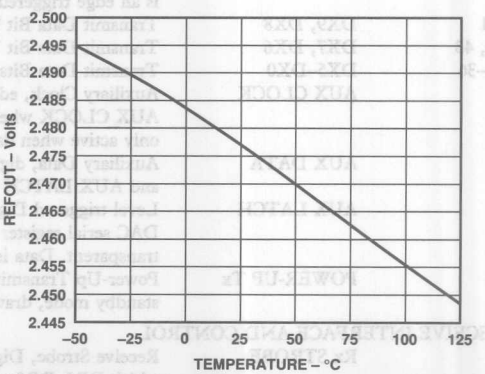


Figure 17. Typical Plot of Reference Variation vs. Temperature

Table II. Truth Table for I_{DD} Control

POWER-UP Tx	POWER-UP Rx	Operation	I_{DD} max
0	0	All Sections Powered Down	2 mA
0	1	Tx Section Powered Down, Rx Section Operational	35 mA
1	0	Tx Section Operational, Rx Section Powered Down	20 mA
1	1	All Sections Operational	50 mA

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Number	Mnemonic	Function
POWER SUPPLY		
34	V_{DD} Tx	Positive Power Supply for transmit section.
22	V_{DD} Rx	Positive Power Supply for receive section. Both V_{DD} pins must be tied together.
32	AGND Tx	Analog Ground for transmit section.
23	AGND Rx	Analog Ground for receive section. Both AGND pins must be tied together.
42	DGND Tx	Digital Ground for transmit section.
13	DGND Rx	Digital Ground for receive section. Both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
28	REF OUT	Reference Output, this is 2.5 V nominal.
24	Rx SIGNAL	Analog Input for receive channel.
30	I Tx	Analog Output Voltage from the I transmit channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
33	Q Tx	Analog Output Voltage from the Q Transmit channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
29	AUX DAC	Analog Output Voltage from the 8-bit Auxiliary DAC. This output comes from a buffer amplifier.
27	RxA	Analog Input for the inverting input of the differential amplifier.
26	RxB	Analog Input for the noninverting input of the differential amplifier.
25	RxC	Analog Output Voltage from the differential amplifier.
TRANSMIT INTERFACE AND CONTROL		
5	Tx STROBE	Transmit Strobe, Digital Input. Tx STROBE transfers the contents of both the I and Q Latches, on a rising edge, to the I and Q 10-bit DACs, respectively. This is used to update both 10-bit DACs simultaneously after the I and Q latches have been loaded via a single 10-bit port.
4	I DAC	I Latch Update, Digital Input. I DAC is used to update the I latch via DX9–DX0. This is an edge triggered latch, DX9–DX0 are latched on the rising edge of I DAC.
3	Q DAC	Q Latch Update, Digital Input. Q DAC is used to update the Q latch via DX9–DX0. This is an edge triggered latch, DX9–DX0 are latched on the rising edge of Q DAC.
2,1	DX9, DX8	Transmit Data Bit 9 and Data Bit 8, digital inputs. DX9 is the most significant bit (MSB).
44, 43	DX7, DX6	Transmit Data Bit 7 and Data Bit 6, digital inputs.
41–36	DX5–DX0	Transmit Data Bits 5 to 0, digital inputs. DX0 is the least significant bit (LSB).
7	AUX CLOCK	Auxiliary Clock, edge triggered digital input. Serial data bits are latched on the rising edge AUX CLOCK when AUX LATCH is low. AUX CLOCK must be a gated clock, which is only active when data is being loaded into the serial register
6	AUX DATA	Auxiliary Data, digital input. This data input is used in conjunction with AUX CLOCK and AUX LATCH to load the 8-bit Auxiliary DAC register.
8	AUX LATCH	Level triggered Digital Input. AUX LATCH controls the transfer of data between the AUX DAC serial register and the AUX DAC latch. When high, the AUX DAC latch is transparent. Data is latched when AUX LATCH is brought low.
35	POWER-UP Tx	Power-Up Transmit, Digital Input. When this goes low the transmit section goes into standby mode, drawing minimum current.
RECEIVE INTERFACE AND CONTROL		
18	Rx STROBE	Receive Strobe, Digital Input. Rx STROBE initiates an ADC conversion, at the end of which DR7–DR0 are updated.
9–12	DR7–DR4	Receive Data Bits 7 to 4, Digital Outputs. DR7 is the most significant bit (MSB).
14–17	DR3–DR0	Receive Data Bits 3 to 0, Digital Outputs. DR0 is the least significant bit (LSB).
20	GCLK	PGA Clock, Digital Input. GDATA bits are latched on the falling edge of GCLK. The PGA must be loaded using 8 GCLKs, the last two bits that are loaded are used to set the PGA.
21	GDATA	Programmable Gain Data, Digital Input. This input is used in conjunction with GCLK to set the gain for the PGA.
19	POWER-UP Rx	Power-Up Receive, Digital Input. When this goes low the receive section goes into standby mode, drawing minimal current.
31	TEST	Test mode, Digital Input. This pin is used to put the device into a special factory test mode. For normal device operation this pin must be tied to DGND.

PRELIMINARY TECHNICAL DATA

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LC²MOS GSM Baseband I/O Port

AD7002

FEATURES
- Single +5 V Supply
- 2-Channel Sigma-Delta ADC
  - 13 MHz Sampling Rate
  - Simultaneous Sampling
  - Digital Filter
- 2-Channel 10-Bit D/A Converter
  - 4 MHz Throughput Rate
  - Simultaneous Update
  - 4th Order Reconstruction Filters
  - GMSK ROM
- 3 Auxiliary D/A Converters
- Fast Interface Port
- Power-Down Modes
- On-Chip Voltage Reference
- 44-Pin PQFP

APPLICATIONS
- GSM
- PCN

GENERAL DESCRIPTION

The AD7002 is a complete low power, two-channel, input/output port with signal conditioning. The device is utilized as a baseband digitization subsystem performing signal conversion between the DSP and the IF/RF sections in the Pan-European telephone system (GSM).

The transmit path consists of an on-board ROM, containing all the code necessary for performing Gaussian Minimum Shift Keying (GMSK), two high accuracy, fast DACs with output reconstruction filters. The receive path is composed of two high performance sigma-delta ADCs with digital filtering. A common bandgap reference feeds the ADCs and signal DACs.

Three control DACs (AUX DAC1 to AUX DAC3) are included for such functions as AFC, AGC and carrier signal shaping. In addition, AUX FLAG is the DAC Shift Register output and may be used for routing digital control information through the device to the IF/RF sections.

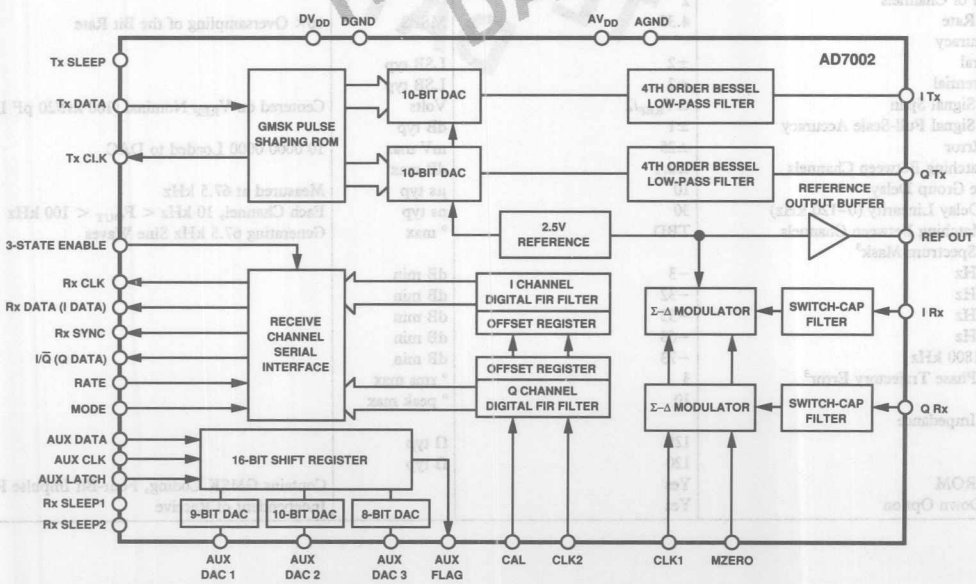
As it is a necessity for all GSM mobile systems to use the lowest power possible, the device has power-down or sleep options for all sections (transmit, receive and auxiliary).

The AD7002 is housed in 44-pin PQFP (Plastic Quad Flatpack).

4

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7002—SPECIFICATIONS[1]

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, f_{CLK1} = f_{CLK2} = 13 MHz; T_A = T_{MIN} to T_{MAX}, Rx $SLEEP_1$ = Rx $SLEEP_2$ = Tx SLEEP = 0 V, unless otherwise stated)

Parameter	AD7002A	Units	Test Conditions/Comments
ADC SPECIFICATIONS			
Resolution	12	Bits	
Signal Input Span	$\pm V_{REF}/2$	Volts	Biased on V_{REF} (2.5 V)
Sampling Rate	13	MSPS	
Output Word Rate	270.8	kHz	RATE 0
	541.7	kHz	RATE 1
Accuracy			
Integral	±1	LSB	
Differential[2]	0		
Bias Offset Error @ +25°C	±5	LSB	After Calibration
T_{MIN} to T_{MAX}	±12	LSB	After Calibration
Input Resistance (DC)	300	kΩ min	
Input Capacitance	10	pF max	
Dynamic Specifications			
Dynamic Range	64	dB min	
Signal to (Noise+Distortion)	62	dB min	
Gain Match Between Channels	0.05	dB max	Input Frequency = 67.5 kHz
Filter Settling Time	46.7	µs typ	
Frequency Response			
0–100 kHz	±0.05	dB max	
110 kHz	−0.8	dB max	
122 kHz	−3.0	dB max	
200 kHz	−66	dB max	
>400 kHz	−72	dB max	
Absolute Group Delay	22.563	µs typ	
Group Delay Between Channels (0–120 kHz)	5	ns typ	
Coding	Twos Complement		
Power Down Option	Yes		Independent of Transmit
TRANSMIT DAC SPECIFICATIONS			
Resolution	10	Bits	
Number of Channels	2		
Update Rate	4.33	MSPS	16× Oversampling of the Bit Rate
DC Accuracy			
Integral	±2	LSB typ	
Differential	±2	LSB typ	
Output Signal Span	$\pm V_{REF}/2$	Volts	Centered on V_{REF} Nominal (100 kΩ/20 pF Load)
Output Signal Full-Scale Accuracy	±1	dB typ	
Offset Error	±25	mV max	10 0000 0000 Loaded to DAC
Gain Matching Between Channels	±0.1	dB max	
Absolute Group Delay	10	µs typ	Measured at 67.5 kHz
Group Delay Linearity (0–120 kHz)	30	ns typ	Each Channel, 10 kHz < F_{OUT} < 100 kHz
Phase Matching Between Channels	TBD	° max	Generating 67.5 kHz Sine Waves
GMSK Spectrum Mask[3]			
100 kHz	−3	dB min	
200 kHz	−32	dB min	
250 kHz	−35	dB min	
400 kHz	−63	dB min	
600–1800 kHz	−73	dB min	
GMSK Phase Trajectory Error[3]	3	° rms max	
	10	° peak max	
Output Impedance			
I Tx	120	Ω typ	
Q Tx	120	Ω typ	
GMSK ROM	Yes		Contains GMSK Coding, Four-Bit Impulse Response
Power Down Option	Yes		Independent of Receive

PRELIMINARY TECHNICAL DATA

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Parameter	AD7002A			Units	Test Conditions/Comments
AUXILIARY DAC SPECIFICATIONS	AUX1	AUX 2	AUX 3		
Resolution	9	11	8	Bits	
DC Accuracy					
Integral	±4	±4	±2	LSB max	
Differential	±1	±1	±1	LSB max	Guaranteed Monotonic
Offset Error	±2	±4	±1	LSB max	
Gain Error	±4	±4	±2	LSB max	
LSB Size	4.88	2.44	9.77	mV typ	
Output Signal Span	0 to V_{REF}	0 to V_{REF}	0 to V_{REF}	Volts	Unloaded Output
Output Impedance	10	10	10	kΩ max	AUX DACs Have Unbuffered Resistive Outputs
	8	8	8	kΩ typ	
Coding	Binary	Binary	Binary		
Power-Down	Yes	Yes	Yes		Power-down Is Implemented by Loading All 1s or All 0s
REFERENCE SPECIFICATIONS					
REF OUT, Reference Output	2.4/2.6			V min/V max	R_L = 100 kΩ, C_L = 1 nF
REF OUT, Reference Output @ +25°C	2.48			V typ	R_L = 100 kΩ, C_L = 1 nF
Reference Temperature Coefficient	TBD			ppm/°C typ	
Reference Variation[4]	±5			mV max	
Output Impedance	60			Ω typ	
LOGIC INPUTS					
V_{INH}, Input High Voltage	3.15			V min	
V_{INL}, Input Low Voltage	0.9			V max	
I_{INH}, Input Current	10			μA max	
C_{IN}, Input Capacitance	10			pF max	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	4.0			V min	$\|I_{OUT}\| \leq 200$ μA
V_{OL}, Output Low Voltage	0.4			V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES					
AV_{DD}	4.75/5.25			V min/V max	
DV_{DD}	4.75/5.25			V min/V max	
I_{DD}					
All Sections Active	25			mA max	
ADC and Auxiliary Paths Active[5]	13			mA max	Tx SLEEP = V_{DD}
Transmit DAC and AUX Paths Active[6]	12			mA max	Rx $SLEEP_1$ = Rx $SLEEP_2$ = V_{DD}
Auxiliary Path only Active[5, 6, 7]	2			mA max	Tx SLEEP = Rx $SLEEP_1$ = Rx $SLEEP_2$ = V_{DD}

NOTES
[1]Operating temperature ranges as follows: A Versions: −25°C to +85°C.
[2]Unmeasurable: sigma-delta conversion is inherently free of differential nonlinearities.
[3]See terminology.
[4]Change in reference voltage due to a change in Tx SLEEP or Rx SLEEP modes.
[5]Measured while the digital inputs to the transmit interface are static.
[6]Measured while the digital inputs to the receive interface are static.
[7]Measured while the digital inputs to the auxiliary interface are static.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

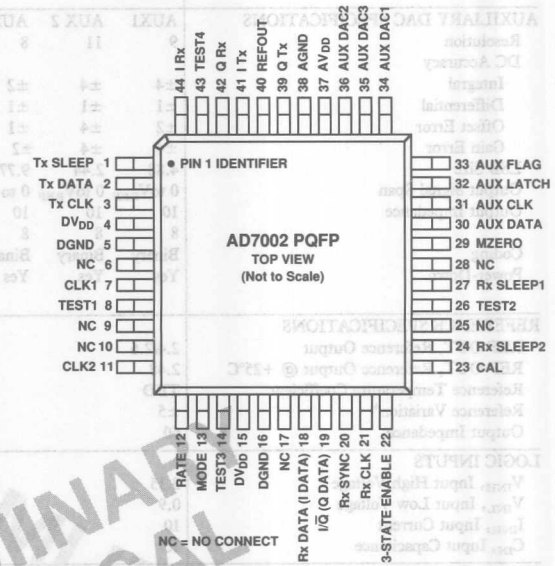
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DV_{DD} to AGND	−0.3 V to +6 V
AV_{DD} to AGND	−0.3 V to +6 V
AGND to DNGD	−0.3 V to +0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Industrial Plastic (A Version)	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates Above +75°C	10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.



PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



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TERMINOLOGY

Signal Input Span
The input signal range for the I and Q channels is biased about V_{REF}. It can go ±1.25 volts about this point.

Sampling Rate
This is the rate at which the modulators on the receive channels sample the analog input.

Output Rate
This is the rate at which data words are made available at the Rx DATA pin (Mode 0) or the I DATA and Q DATA pins (Mode 1). There are two rates depending on whether the device is operated in RATE 0 or RATE 1.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the DAC or ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the DAC or ADC.

Bias Offset Error
This is the offset error (in LSBs) in the ADC section.

Dynamic Range
Dynamic Range is the ratio of the maximum output signal to the smallest output signal the converter can produce (1 LSB), expressed logarithmically, in decibels [(dB = 20 $\log_{10}$ (ratio)]. For an N-bit converter, the ratio is theoretically very nearly equal to 2^N [(in dB, 20N $\log_{10}(2)$ = 6.02N)]. However, this theoretical value is degraded by converter noise and inaccuracies in the LSB weight.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for a sine wave is given by:

Signal to (Noise + Distortion) = (6.02N+1.76)dB

Absolute Group Delay
Absolute group delay is the rate of change of phase versus frequency, dϕ/df. It is expressed in microseconds.

Group Delay Linearity
The group delay linearity or differential group delay is the group delay over the full band relative to the group delay at one particular frequency. The reference frequency for the AD7002 is 1 kHz.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Phase Matching Between Channels
This is a measure of the phase matching characteristics of the I and Q transmit channels. It is obtained by transmitting all ones and then measuring the difference between the actual phase shift between the I and Q outputs and the ideal phase shift of 90°.

Settling Time
This is the digital filter settling time in the AD7002 receive section. On initial power-up or after returning from the sleep mode, it is necessary to wait this amount of time to get useful data.

Output Signal Span
This is the output signal range for the transmit channel section and the auxiliary DAC section. For the transmit channel the span is ±1.25 volts centered on 2.5 volts and for the auxiliary DAC section it is 0 to $+V_{REF}$.

Output Signal Full-Scale Accuracy
This is the accuracy of the full-scale output (all 1s loaded to the DACs) on the transmit channel and is expressed in dBs.

Offset Error
This is the amount of offset in the transmit DACs and the auxiliary DACs and is expressed in mVs for the transmit section and in LSBs for the auxiliary section.

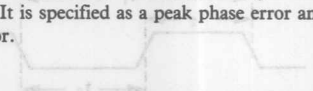
Gain Error
This is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out and is expressed in LSBs. In the AD7002, gain error is specified for the auxiliary section.

Output Impedance
This is a measure of the drive capability of the auxiliary DAC outputs and is expressed in kΩs.

GMSK Spectrum Mask
This is the output spectrum of the I and Q transmit channels, when transmitting a random sequence of data bits using GMSK modulation as specified in GSM 5.04.

GMSK Phase Trajectory Error
This is a measure of the phase error between the transmitted phase of an ideal GMSK modulator and the actual phase transmitted by the AD7002, when transmitting a random sequence of data bits. It is specified as a peak phase error and also as an rms phase error.

PRELIMINARY TECHNICAL DATA



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INPUT CLOCK TIMING SPECIFICATIONS[1]

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_1	76	76	ns min	CLK1, CLK2, AUX CLK Cycle Time
t_2	30	30	ns min	CLK1, CLK2, AUX CLK High Time
t_3	30	30	ns min	CLK1, CLK2, AUX CLK Low Time

TRANSMIT SECTION TIMING SPECIFICATIONS

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, $f_{CLK1} = f_{CLK2}$ = 13 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_4	0	0	ns min	Tx SLEEP Hold Time
t_5	25	25	ns min	Tx SLEEP Setup Time
t_6	24 t_1 + 80	24 t_1 + 80	ns max	Tx CLK Active After CLK1 Rising Edge
t_7	48 t_1	48 t_1	ns	Tx CLK Cycle Time
t_8	24 t_1	24 t_1	ns	Tx CLK High Time
t_9	24 t_1	24 t_1	ns	Tx CLK Low Time
t_{10}	30	30	ns max	Propagation Delay from CLK1 to Tx CLK
t_{11}	25	25	ns max	Data Setup Time
t_{12}	10	10	ns min	Data Hold Time
t_{13}	0	0	ns min	Tx CLK to Tx SLEEP Asserted for Last Tx CLK Cycle[3]
	23 t_1	23 t_1	ns max	
t_{14}	10	10	ns min	Digital Output Rise Time
t_{15}	10	10	ns max	Digital Output Fall Time

AUXILIARY DAC TIMING

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, $f_{AUX\ CLK}$ = 13 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_{16}	15	15	ns min	AUX DATA Setup Time
t_{17}	5	5	ns min	AUX DATA Hold Time
t_{18}	25	25	ns min	AUX LATCH to SCLK Falling Edge Setup Time
t_{19}	20	20	ns min	AUX LATCH to SCLK Falling Edge Hold Time
t_{20}	50	50	ns max	AUX LATCH High to AUX FLAG Valid Delay
t_{21}	10	10	ns max	Digital Output Rise Time
t_{22}	10	10	ns max	Digital Output Fall Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Digital output rise and fall times specify the time required for the output to go between 10% and 90% of 5 V.
[3]t_{13} specifies a window, that Tx SLEEP should be asserted for the current Tx CLK to be the last prior to entering SLEEP mode.
Specifications subject to change without notice.

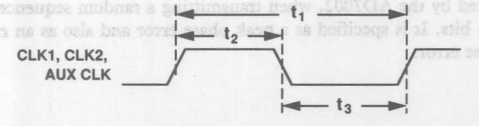


Figure 1. Clock Timing

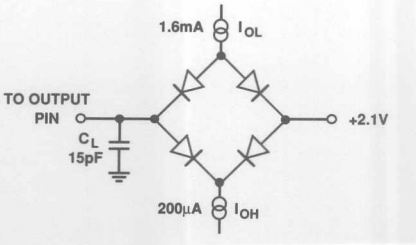


Figure 2. Load Circuit for Timing Specifications

PRELIMINARY TECHNICAL DATA

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RECEIVE SECTION TIMING

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, f_{CLK1} = f_{CLK2} = 13 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_{23}	0	0	ns min	Rx SLEEP Hold Time After CLK1, CLK2 High
t_{24}	25	25	ns min	Rx SLEEP Setup Time Before CLK1, CLK2 High
t_{25}	0	0	ns min	Rx SYNC to Rx SLEEP Asserted; See Note 4
	39 t_1	39 t_1	ns max	RATE 0
	15 t_1	15 t_1	ns max	RATE 1
t_{26}				Rx CLK Active After CLK1 Rising Edge Following Falling Edge of Rx SLEEP
	32 t_1 + t_2	32 t_1 + t_2	ns	Mode 0
	31 t_1 + t_2	31 t_1 + t_2	ns	Mode 1
t_{27}				Rx CLK Cycle Time
	t_1	t_1	ns	MODE 0
	2 t_1	2 t_1	ns	MODE 1
t_{28}				Rx CLK High Pulse Width
	30	30	ns min	MODE 0
	90	90	ns min	MODE 1
t_{29}				Rx CLK Low Pulse Width
	30	30	ns min	MODE 0
	30	30	ns min	MODE 1
t_{30}	25	25	ns max	Propagation Delay from CLK1, CLK2 High to Rx CLK High
t_{31}	20	20	ns min	Rx SYNC Valid Prior to Rx CLK Falling
t_{32}				Rx SYNC High Pulse Width
	t_1	t_1	ns	MODE 0
	2 t_1	2 t_1	ns	MODE 1
t_{33}				Rx SYNC Cycle Time
	24 t_1	24 t_1	ns	MODE 0 RATE 0
	12 t_1	12 t_1	ns	MODE 0 RATE 1
	48 t_1	48 t_1	ns	MODE 1 RATE 0
	24 t_1	24 t_1	ns	MODE 1 RATE 1
t_{34}	15	15	ns min	Rx DATA Valid After Rx CLK Rising Edge
t_{35}	15	15	ns max	Propagation Delay from Rx CLK Rising Edge to I/$\overline{Q}$
t_{36}	10	10	ns max	Digital Output Rise Time[2]
t_{37}	10	10	ns max	Digital Output Fall Time[2]

CALIBRATION AND CONTROL TIMING

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, $f_{AUX\ CLK}$ = 13 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −25°C to +85°C	Units	Description
t_{38}	25	25	ns min	SLEEP to CAL Setup Time
t_{39}	608 t_1	608 t_1	ns min	CAL Pulse Width
t_{40}	25	25	ns min	RATE, MODE or 3-STATE ENABLE Setup Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Digital output rise and fall times specify the time required for the output to go between 10% and 90% of 5 V.

[3]See Figure 4 for test circuit.

[4]t_{25} specifies a window, after Rx SYNC which marks the beginning of I data, that Rx SLEEP should be asserted for the subsequent IQ data pair to be last prior to entering SLEEP mode.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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CIRCUIT DESCRIPTION

TRANSMIT SECTION

The transmit section of the AD7002 generates GMSK I and Q waveforms in accordance with GSM specification 5.04. This is accomplished by a digital GMSK modulator, followed by 10-bit DACs for the I and Q channels and on-chip reconstruction filters. The GMSK (Gaussian Minimum Shift Keying) digital modulator generates I and Q signals, at 16× oversampling, in response to the transmit data stream. The I and Q data streams drive 10-bit DACs, which are filtered by on-chip 4th order Bessel low-pass filters.

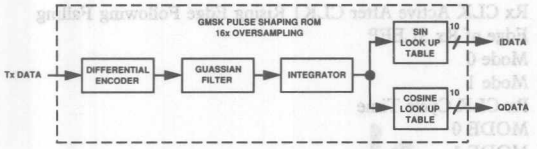


Figure 3. GMSK Functional Block Diagram

Table I. Truth Table for the Differential Encoder

Tx $DATA_i$	Tx $DATA_{i-1}$	Differentially Encoded Data
0	0	0
0	1	1
1	0	1
1	1	0

GMSK Modulator

Figure 3 shows the functional block diagram of the GMSK modulator. This is implemented using control logic with a ROM look up table, to generate I and Q data samples at 16 times the transmit data rate. The transmit data (Tx DATA) is first differentially encoded as specified by GSM 5.04 section 2.3 (Table I). The GMSK modulator generates 10-bit I and Q waveforms (In-phase and Quadrature), in response to the encoded data, which are loaded into the 10-bit, I and Q transmit DACs. The Gaussian filter, in the GMSK modulator, has an impulse response truncated to 4 data bits.

When the transmit section is brought out of sleep mode (Tx SLEEP low), the modulator is reset to a transmitting all 1s state. When Tx SLEEP is asserted (Tx SLEEP high), the transmit section powers down, with the I TX and Q TX outputs connected to V_{REF} through a nominal impedance of 80 kΩ.

Reconstruction Filters

The reconstruction filters smooth the DAC output signals, providing continuous time I and Q waveforms at the output pins. These are 4th order Bessel low-pass filters with a cutoff frequency of approximately 300 kHz. Figure 6 shows a typical transmit filter frequency response, while Figure 7 shows a typical plot of group delay versus frequency. The filters are designed to have a linear phase response in the passband and due to the reconstruction filters being on-chip, the phase mismatch between the I and Q transmit channels is kept to a minimum.

Transmit Section Digital Interface

Figure 4 shows the timing diagram for the transmit interface. Tx SLEEP is sampled on the falling edge of CLK1. When Tx SLEEP is brought low, Tx CLK becomes active after 24 master clock cycles. Tx CLK can be used to clock out the transmit data from the ASIC or DSP on the rising edge and Tx DATA is clocked into the AD7002 on the falling edge of Tx CLK. When Tx SLEEP is asserted the transmit section is immediately put into sleep mode, disabling Tx CLK and powering down the transmit section.

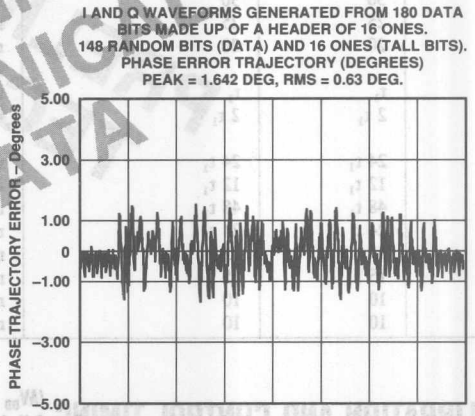


Figure 5. Typical Plot of the Transmit Phase Trajectory Error

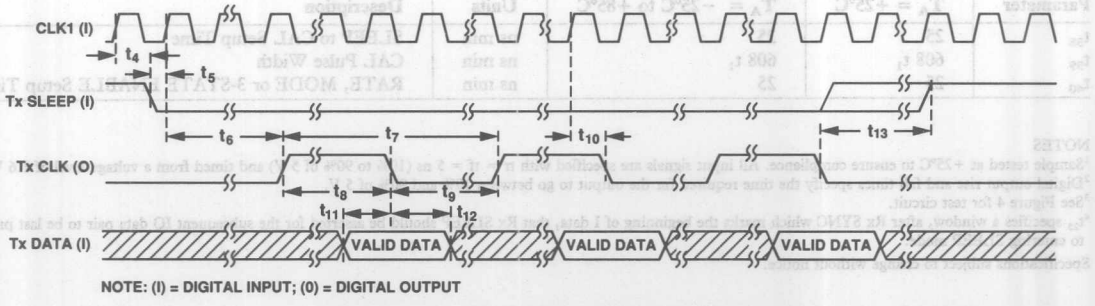


Figure 4. Transmit Section Timing Diagram

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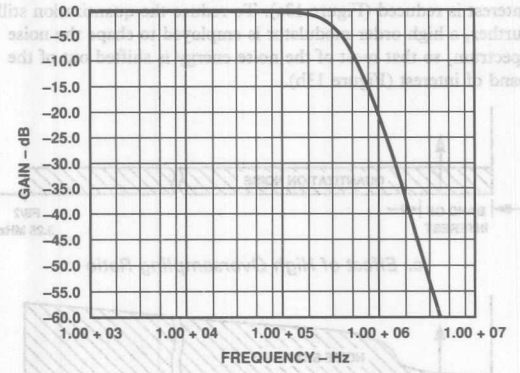


Figure 6. Transmit Filter Frequency Response

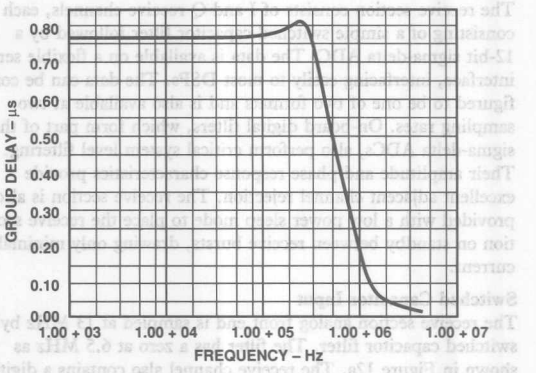


Figure 7. Transmit Filter Group Delay

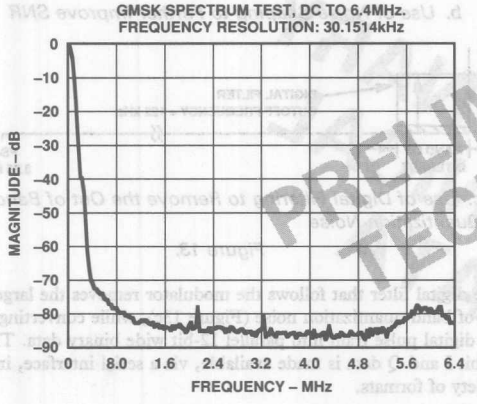


Figure 8. Typical Spectrum Plot of the I Channel When Transmitting Random Data

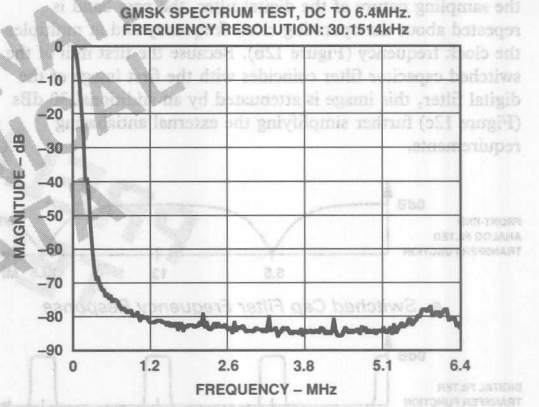


Figure 9. Typical Spectrum Plot of the Q Channel When Transmitting Random Data

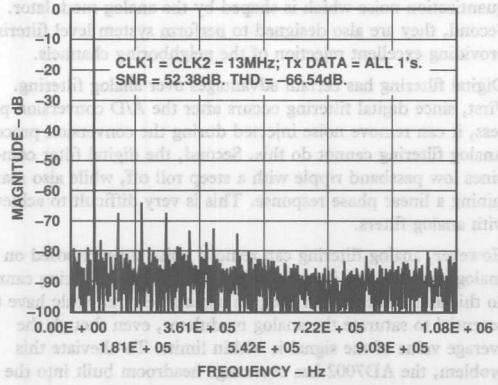


Figure 10. Typical Spectrum Plot of the I Channel When Transmitting All 1s or All 0s

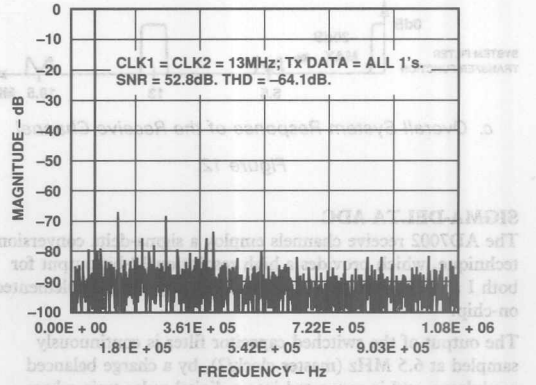


Figure 11. Typical Spectrum Plot of the Q Channel When Transmitting All 1s or All 0s

PRELIMINARY TECHNICAL DATA

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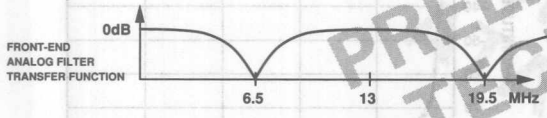
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RECEIVE SECTION

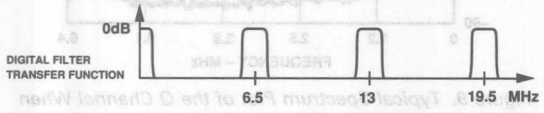
The receive section consists of I and Q receive channels, each consisting of a simple switched capacitor filter followed by a 12-bit sigma-delta ADC. The data is available on a flexible serial interface, interfacing easily to most DSPs. The data can be configured to be one of two formats and is also available at two sampling rates. On-board digital filters, which form part of the sigma-delta ADCs, also perform critical system level filtering. Their amplitude and phase response characteristics provide excellent adjacent channel rejection. The receive section is also provided with a low power sleep mode to place the receive section on standby between receive bursts, drawing only minimal current.

Switched Capacitor Input

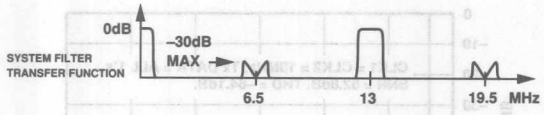
The receive section analog front end is sampled at 13 MHz by a switched capacitor filter. The filter has a zero at 6.5 MHz as shown in Figure 12a. The receive channel also contains a digital low-pass filter (further details are contained in the following section) which operates at a clock frequency of 6.5 MHz. Due to the sampling nature of the digital filter, the pass band is repeated about the operating clock frequency and at multiples of the clock frequency (Figure 12b). Because the first null of the switched capacitor filter coincides with the first image of the digital filter, this image is attenuated by an additional 30 dBs (Figure 12c) further simplifying the external antialiasing requirements.



a. Switched Cap Filter Frequency Response



b. Digital Filter Frequency Response



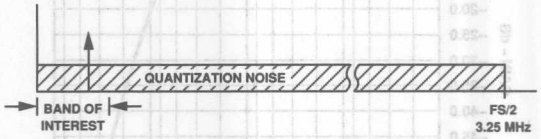
c. Overall System Response of the Receive Channel

Figure 12.

SIGMA-DELTA ADC

The AD7002 receive channels employ a sigma-delta conversion technique, which provides a high resolution 12-bit output for both I and Q channels with system filtering being implemented on-chip.

The output of the switched capacitor filter is continuously sampled at 6.5 MHz (master clock/2), by a charge balanced modulator, and is converted into a digital pulse train whose duty cycle contains the digital information. Due to the high oversampling rate, which spreads the quantization noise from 0 to 3.25 MHz ($F_S/2$), the noise energy contained in the band of interest is reduced (Figure 13a). To reduce the quantization still further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 13b).



a. Effect of High Oversampling Ratio



b. Use of Noise Shaping to Further Improve SNR



c. Use of Digital Filtering to Remove the Out of Band Quantization Noise

Figure 13.

The digital filter that follows the modulator removes the large out of band quantization noise (Figure 13c), while converting the digital pulse train into parallel 12-bit wide binary data. The 12-bit I and Q data is made available, via a serial interface, in a variety of formats.

Digital Filter

The digital filters used in the AD7002 receive section carry out two important functions. First, they remove the out of band quantization noise which is shaped by the analog modulator. Second, they are also designed to perform system level filtering, providing excellent rejection of the neighboring channels.

Digital filtering has certain advantages over analog filtering. First, since digital filtering occurs after the A/D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Second, the digital filter combines low passband ripple with a steep roll off, while also maintaining a linear phase response. This is very difficult to achieve with analog filters.

However, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full-scale have the potential to saturate the analog modulator, even though the average value of the signal is within limits. To alleviate this problem, the AD7002 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV.

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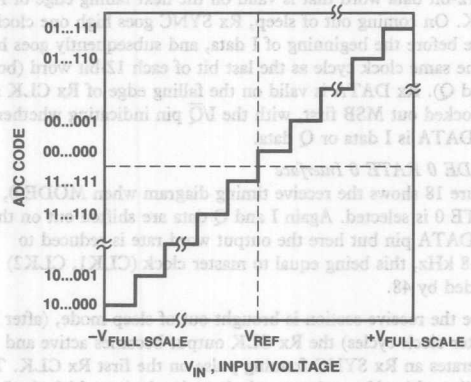


Figure 14. ADC Transfer Function for I and Q Receive Channels

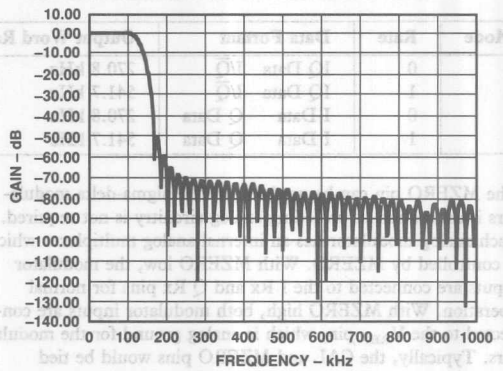


Figure 15. Digital Filter Frequency Response

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Filter Characteristics

The digital filter is a 288-tap FIR filter, clocked at half the master clock frequency. The frequency response is shown in Figure 15. The 3 dB point is at 122 kHz.

Due to the low pass nature of the receive filters, there is a settling time associated with step input functions. Output data will not be meaningful until all the digital filter taps have been loaded with data samples taken after the step change. Hence the AD7002 digital filters have a settling time of 44.7 µs ($288 \times 2\ t_1$).

When coming out of sleep, the digital filter taps are reset. Hence data, initially generated by the digital filters, will not be correct. Not until all 288 taps have loaded with meaningful data from the analog modulator, will the output data be correct. The analog modulator, on coming out of sleep, will generate meaningful data after 21 master clock cycles.

Calibration

Included in the digital filter is a means by which receive signal offsets may be calibrated out. Calibration can be effected through the use of the CAL and MZERO pins.

Each channel of the digital low-pass filter section has an offset register. The offset register can be made to contain a value representing the dc offset of the preceding analog circuitry. In normal operation, the value stored in the offset register is subtracted from the filter output data before the data appears on the serial output pin. By so doing, the dc offset gets cancelled.

In each channel the offset register is cleared (twos complement zero) when CAL is high and becomes loaded with the first digital filter result after CAL falls. This result will be a measure of the channel dc offset if the analog channel is switched to zero prior to CAL falling. Time must be provided for the analog circuitry and the digital filter to settle after the analog circuitry is switched to zero and before CAL falls. The offset register will then be loaded with the a proper representation of the dc offset.

CAL must be high for more than 608 master clock cycles (CLK1, CLK2). If the analog channels are switched to zero coincident with CAL rising, this time is also sufficient to satisfy the settling time of the analog sigma-delta modulators and the digital filters. CAL may be held high for an unlimited time if convenient or necessary. Only the digital result following the fall of CAL will be loaded into each offset register. After CAL falls, normal operation resumes immediately.

The offset registers are static and retain their contents even during sleep mode (Rx $SLEEP_1$ and Rx $SLEEP_2$ high). They need only be updated if drifts in the analog dc offsets are experienced or expected. However, on initial application of power to the digital supply pins the offset registers may contain grossly incorrect values and, therefore, calibration must be activated at least once after power is applied even if the facility of calibration is not regularly used.

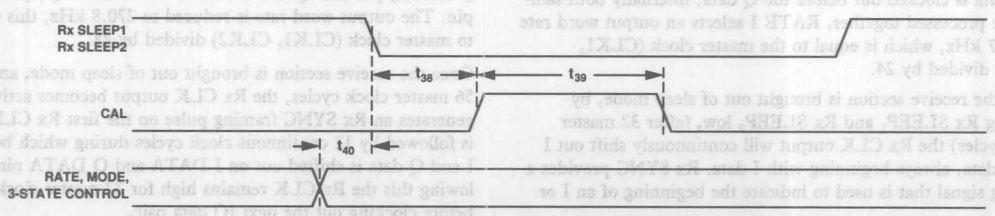


Figure 16. Calibration and Control Timing Diagram

PRELIMINARY TECHNICAL DATA

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Mode	Rate	Data Format		Output Word Rate
0	0	IQ Data	I/$\overline{Q}$	270.8 kHz
0	1	IQ Data	I/$\overline{Q}$	541.7 kHz
1	0	I Data	Q Data	270.8 kHz
1	1	I Data	Q Data	541.7 kHz

The MZERO pin can be used to zero the sigma-delta modulators if calibration of preceding analog circuitry is not required. Each analog modulator has an internal analog multiplexer which is controlled by MZERO. With MZERO low, the modulator inputs are connected to the I Rx and Q Rx pins for normal operation. With MZERO high, both modulator inputs are connected to the V_{REF} pin, which is analog ground for the modulators. Typically, the CAL and MZERO pins would be tied together and driven by the same digital signal. If calibration of external analog circuitry is desired, MZERO should be kept low during the calibration cycle.

The offset registers have enough resolution to hold the value of any dc offset between ±5 V. However, the performance of the sigma-delta modulators will degrade if full scale signals with more that 100 mV of offset are experienced. If large offsets are present, these can be calibrated out, but signal excursions from the offsets should be limited such that the I Rx and Q Rx voltages remain within ±1.35 V of V_{REF}.

Receive Section Digital Interface

A flexible serial interface is provided for the AD7002 receive section. Four basic operating modes are available. Table II shows the truth table for the different serial modes that are available. The MODE pin determines whether the I and Q serial data is made available on two separate pins (MODE 1) or combined on to a single output pin (MODE 0). The RATE pin determines whether I and Q receive data is provided at 541.7 kHz (RATE 1) or at 270.8 kHz (RATE 0).

When the receive section is put into sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ high, the receive interface will complete the current IQ cycle before entering into a low power sleep mode.

MODE 0 RATE 1 Interface

The timing diagram for the MODE 0 RATE 1 receive interface is shown in Figure 17. It can be used to interface to DSP processors requiring only one serial port.

When using MODE 0, the serial data is made available on the Rx DATA pin, with the I/$\overline{Q}$ pin indicating whether the 12-bit word being clocked out is an I sample or a Q sample. Although the I data is clocked out before the Q data, internally both samples are processed together. RATE 1 selects an output word rate of 541.7 kHz, which is equal to the master clock (CLK1, CLK2) divided by 24.

When the receive section is brought out of sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ low, (after 32 master clock cycles) the Rx CLK output will continuously shift out I and Q data, always beginning with I data. Rx SYNC provides a framing signal that is used to indicate the beginning of an I or cycle before the beginning of I data, and subsequently goes high in the same clock cycle as the last bit of each 12-bit word (both I and Q). Rx DATA is valid on the falling edge of Rx CLK and is clocked out MSB first, with the I/$\overline{Q}$ pin indicating whether Rx DATA is I data or Q data.

MODE 0 RATE 0 Interface

Figure 18 shows the receive timing diagram when MODE 0, RATE 0 is selected. Again I and Q data are shifted out on the Rx DATA pin but here the output word rate is reduced to 270.8 kHz, this being equal to master clock (CLK1, CLK2) divided by 48.

Once the receive section is brought out of sleep mode, (after 56 master clock cycles) the Rx CLK output becomes active and generates an Rx SYNC framing pulse on the first Rx CLK. This is followed by 12 continuous clock cycles during which the I data is shifted out on the Rx DATA pin. Following this the Rx CLK remains high for 11 master clock cycles before clocking out the Q data in exactly the same manner.

Rx DATA is valid on the falling edge of Rx CLK with the I/$\overline{Q}$ pin indicating whether Rx DATA is I data or Q data.

MODE 1 RATE 1 Interface

Figure 19 shows the timing for MODE 1 RATE 1 receive digital interface. MODE 1 RATE 1 gives an output word rate of 541.7 kHz, but I and Q data are transferred on separate pins. I data is shifted out on Rx DATA (I DATA) pin and Q data is shifted out on the I/$\overline{Q}$ (Q DATA) pin. RATE 1 selects an output word rate of 541.7 kHz (this is equal to the master clock divided by 24).

When the receive section is brought out of sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ low, (after 32 master clock cycles) the Rx CLK output will continuously shift out I and Q data, on separate pins. Rx SYNC provides a framing signal that is used to indicate the beginning of an I or Q, 12-bit data word that is valid on the next falling edge of Rx CLK. On coming out of sleep, Rx SYNC goes high one clock cycle before the beginning of I data, and subsequently goes high in the same clock cycle as the I and Q LSBs. It takes 24 Rx CLKs (excluding the first framing pulse) to complete a single IQ cycle. I DATA and Q DATA are valid on the falling edge of Rx CLK and are clocked out MSB first.

MODE 1 RATE 0 Interface

Figure 20 shows the receive timing diagram when MODE 1 RATE 0 is selected. MODE 1 RATE 0, again I and Q data are transferred on separate pins. I data is shifted out on Rx DATA (I DATA) pin and Q data is shifted out on the I/$\overline{Q}$ (Q DATA) pin. The output word rate is reduced to 270.8 kHz, this equal to master clock (CLK1, CLK2) divided by 48.

Once the receive section is brought out of sleep mode, and after 56 master clock cycles, the Rx CLK output becomes active and generates an Rx SYNC framing pulse on the first Rx CLK. This is followed by 12 continuous clock cycles during which both the I and Q data is shifted out on I DATA and Q DATA pins. Following this the Rx CLK remains high for 22 master clock cycles before clocking out the next IQ data pair.

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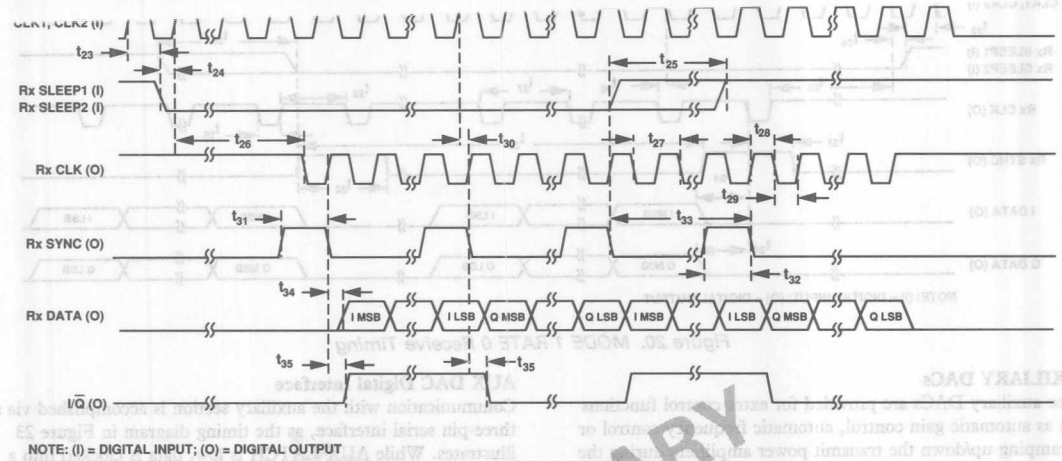


Figure 17. MODE 0 RATE 1 Receive Timing

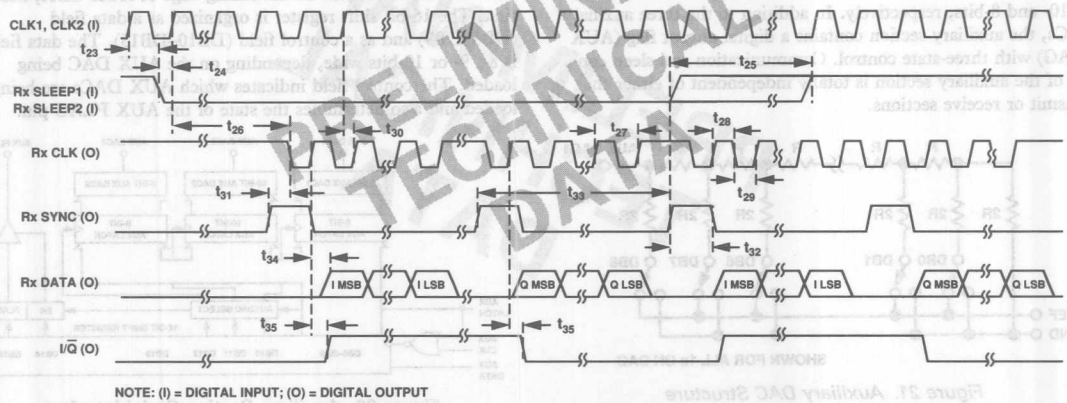


Figure 18. MODE 0 RATE 0 Receive Timing

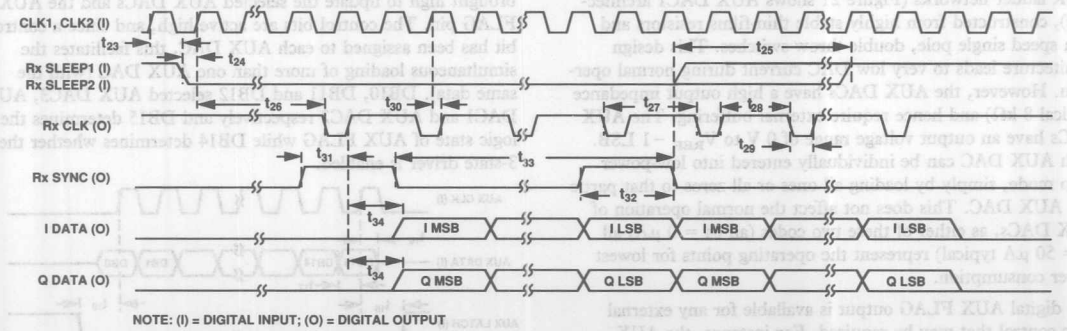


Figure 19. MODE 1 RATE 1, Receive Timing

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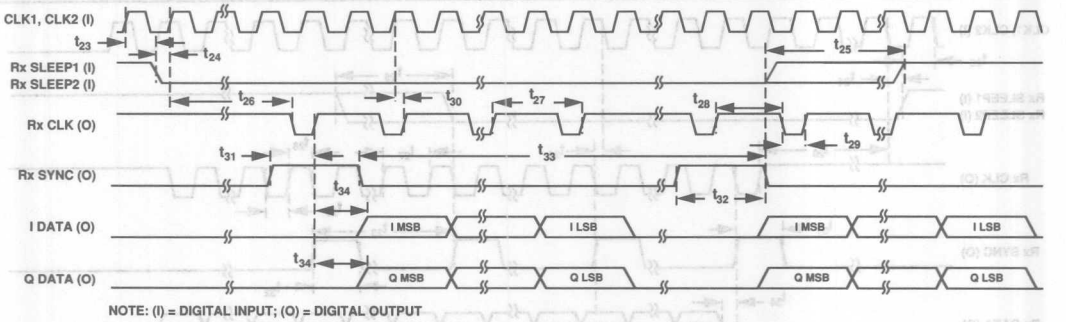


Figure 20. MODE 1 RATE 0 Receive Timing

AUXILIARY DACs

Three auxiliary DACs are provided for extra control functions such as automatic gain control, automatic frequency control or for ramping up/down the transmit power amplifiers during the beginning/end of a transmit burst. The three auxiliary DACs, AUX DAC1, AUX DAC2 and AUX DAC3, have resolutions of 9-, 10- and 8-bits, respectively. In addition to the three auxiliary DACs, the auxiliary section contains a digital output flag (AUX FLAG) with three-state control. Communication and sleep control of the auxiliary section is totally independent of either the transmit or receive sections.

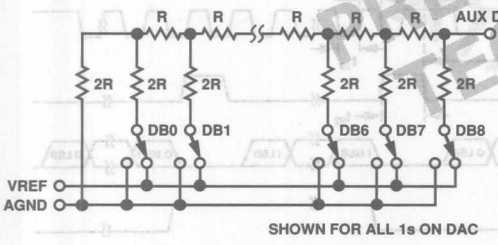


Figure 21. Auxiliary DAC Structure

The AD7002 AUX DACs are voltage mode DACs, consisting of R–2R ladder networks (Figure 21 shows AUX DAC1 architecture), constructed from highly stable thin-films resistors and high speed single pole, double throw switches. This design architecture leads to very low DAC current during normal operation. However, the AUX DACs have a high output impedance (typical 8 kΩ) and hence require external buffering. The AUX DACs have an output voltage range of 0 V to V_{REF} −1 LSB. Each AUX DAC can be individually entered into low-power sleep mode, simply by loading all ones or all zeros to that particular AUX DAC. This does not affect the normal operation of AUX DACs, as either of these two codes (all 0s = 0 μA, all 1s = 50 μA typical) represent the operating points for lowest power consumption.

The digital AUX FLAG output is available for any external logic control that may be required. For instance, the AUX FLAG could be used to control the Tx SLEEP pin, turning on the transmit section prior to ramping up (using one of AUX DACs) the RF amplifiers.

AUX DAC Digital Interface

Communication with the auxiliary section is accomplished via a three-pin serial interface, as the timing diagram in Figure 23 illustrates. While AUX LATCH is low, data is clocked into a 16-bit shift register via the AUX DATA and AUX CLK pins. AUX DATA is clocked on the falling edge of AUX CLK, MSB first. The 16-bit shift register is organized as a data field (DB0–DB9) and as a control field (DB10–DB15). The data field is 8-, 9- or 10-bits wide, depending on the AUX DAC being loaded. The control field indicates which AUX DACs are being loaded and also determines the state of the AUX FLAG pin.

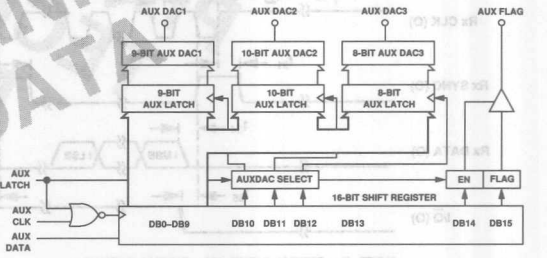


Figure 22. Auxiliary Section Serial Interface

When the shift register has been loaded, AUX LATCH is brought high to update the selected AUX DACs and the AUX FLAG pin. The control bits are active high, and since a control bit has been assigned to each AUX DAC, this facilitates the simultaneous loading of more than one AUX DAC (with the same data). DB10, DB11 and DB12 selected AUX DAC3, AUX DAC1 and AUX DAC2 respectively and DB15 determines the logic state of AUX FLAG while DB14 determines whether the 3-state driver is enabled.

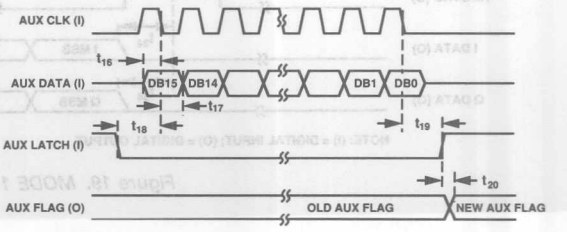


Figure 23. Auxiliary DAC Timing Diagram

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VOLTAGE REFERENCE

The AD7002 contains an on-chip bandgap reference which provides a low noise, temperature compensated reference to the IQ transmit DACs and the IQ receive ADCs. The reference is also made available on the REF OUT pin and can be used to bias other analog circuitry in the IF section.

When both the transmit section and the receive section are in sleep mode (Tx SLEEP and Rx SLEEP asserted), the reference output buffer is also powered down by approximately 80%.

PIN FUNCTION DESCRIPTION

PQFP Pin Number	Mnemonic	Function
POWER SUPPLY		
37	AV_{DD}	Positive power supply for analog section. This is +5 V±5%.
38	AGND	Analog ground.
4, 15	DV_{DD}	Positive power supply for digital section. This is +5 V±5%.
5, 16	DGND	Digital ground.
ANALOG SIGNAL AND REFERENCE		
41	I Tx	Analog output for the I (In-Phase) channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low pass filter. The 10-bit DAC is loaded with I data, which is generated by the GMSK modulator.
39	Q Tx	Analog output for the Q (Quadrature) channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low pass filter. The 10-bit DAC is loaded with Q data, which is generated by the GMSK modulator.
44	I Rx	Analog input for I receive channel.
42	Q Rx	Analog input for Q receive channel.
34	AUX DAC1	Analog output voltage from the 9-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
36	AUX DAC2	Analog output voltage from the 10-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
35	AUX DAC3	Analog output voltage from the 8-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
40	REF OUT	Reference output; this is 2.48 volts nominal.
TRANSMIT INTERFACE AND CONTROL		
7, 11	CLK1, CLK2	Master clock inputs for both the transmit and receive sections. CLK1 and CLK2 must be externally hardwired together and driven from a 13 MHz TTL compatible crystal.
3	Tx CLK	Clock output from the AD7002 which can be used to clock in the data for the transmit section.
2	Tx DATA	Data input for the transmit section, data is clocked on the falling edge of Tx CLK.
1	Tx SLEEP	Sleep control input for transmit section. When it is high, the transmit section goes into standby mode and draws minimal current.

PRELIMINARY TECHNICAL DATA

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PQFP Pin Number	Mnemonic	Function
RECEIVE INTERFACE AND CONTROL		
13	MODE	Digital control input. When High (MODE 1), the I and Q outputs are on separate pins (Q DATA and I DATA). When Low (MODE 0), I and Q are on the same pin (Rx DATA).
12	RATE	Digital control input. This determines whether the receive section interface operates at a word rate of 541.7 kHz or at a word rate of 270.8 kHz. When High (RATE 1), the output word rate is 541.7 kHz. When Low (RATE 0), the output word rate is 270.8 kHz.
18	Rx DATA (I DATA)	This is a dual function digital output. When the device is operating in MODE 0, the Rx DATA (both I and Q) is available at this pin. When the device is operating in MODE 1, only I DATA is available at this pin.
19	I/$\overline{Q}$ (Q DATA)	This is a dual function digital output. When the device is operating in MODE 0, it indicates whether I DATA or Q DATA is present on Rx DATA pin. In MODE 1, Q DATA is available at this pin.
20	Rx SYNC	Synchronization output for framing I and Q data at the receive interface.
21	Rx CLK	Output clock for the receive section interface.
22	3-STATE CONTROL	This digital input controls the output 3-state drivers on the receive section interface. When it is High, the outputs are enabled. When Low, they are in high impedance.
23	CAL	Calibration control pin for digital filter section. When brought high, for a minimum of 608 master clock cycles, the receive section enters a calibration cycle. Where I and Q offset registers are updated, when the CAL pin is brought low again, with offset values which are subtracted out from subsequent ADC conversions. CAL should remain Low during normal operation.
29	MZERO	Digital control input. When high the analog modulator input is internally grounded (i.e., tied to V_{REF}). MZERO, in conjunction with CAL, allows on-chip offsets to be calibrated out. Low for normal operation.
27, 24	Rx $SLEEP_1$, Rx $SLEEP_2$	Power-down control inputs for receive section. When high, the receive section goes into standby mode and draws minimal current. Rx $SLEEP_1$ and Rx $SLEEP_2$ must be externally hardwired together for normal device operation.
AUXILIARY INTERFACE AND CONTROL		
32	AUX LATCH	Synchronization input for the auxiliary DACs' shift register and AUX OUT.
31	AUX CLK	Clock input for the auxiliary DACs' 16-bit shift register. AUX DATA is latched on the falling edge of AUX CLK while AUX LATCH is low.
30	AUX DATA	Data input for the AUX DACs and the AUX FLAG serial interface.
33	AUX FLAG	Digital output flag, this can be used as a digital control output and is controlled from the auxiliary serial interface.
TEST		
8, 26	Test 1, Test 2	Test pins for factory use only. These pins should be left unconnected and not used as routes for other circuit signals.
14, 43	Test 3, Test 4	Test pins. These must be tied to ground for normal device operation.

PRELIMINARY TECHNICAL DATA

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ANALOG DEVICES

LC²MOS Baseband I/O Converter

AD7005

FEATURES

Single +5 V Supply
2-Channel Sigma-Delta ADC
2.33 MHz Sampling Rate
Simultaneous Sampling
Digital Filter (22 kHz Bandwidth)
2-Channel 10-Bit D/A Converters
194.4 kHz Update Rate
Simultaneous Update
4th Order Bessel Low-Pass Filters
3 Auxiliary D/A Converters
Fast Interface Port
Power Down Modes
On-Chip Voltage Reference
44-Pin PQFP

APPLICATIONS

TIA Digital Cellular Telephony
Private Mobile Telephony
Signal Generation/Acquisition
FSK, PSK Demodulation

GENERAL DESCRIPTION

The AD7005 is a complete low power, two-channel, input/output port with signal conditioning. The device is utilized as a baseband digitization subsystem performing signal conversion between the DSP and the IF/RF sections in the American digital cellular telephone system.

The transmit path contains two high accuracy, fast DACs with output reconstruction filters. The receive path is composed of two high performance sigma-delta ADCs with digital filtering. A common bandgap reference feeds the ADCs and signal DACs.

Three control DACs (AUX DAC1 to AUX DAC3) are included for such functions as AFC, AGC and transmit power control.

As it is a necessity for all mobile systems to use the lowest power possible, the device has power down or sleep options. Each of the three digital channels has an independent power down control.

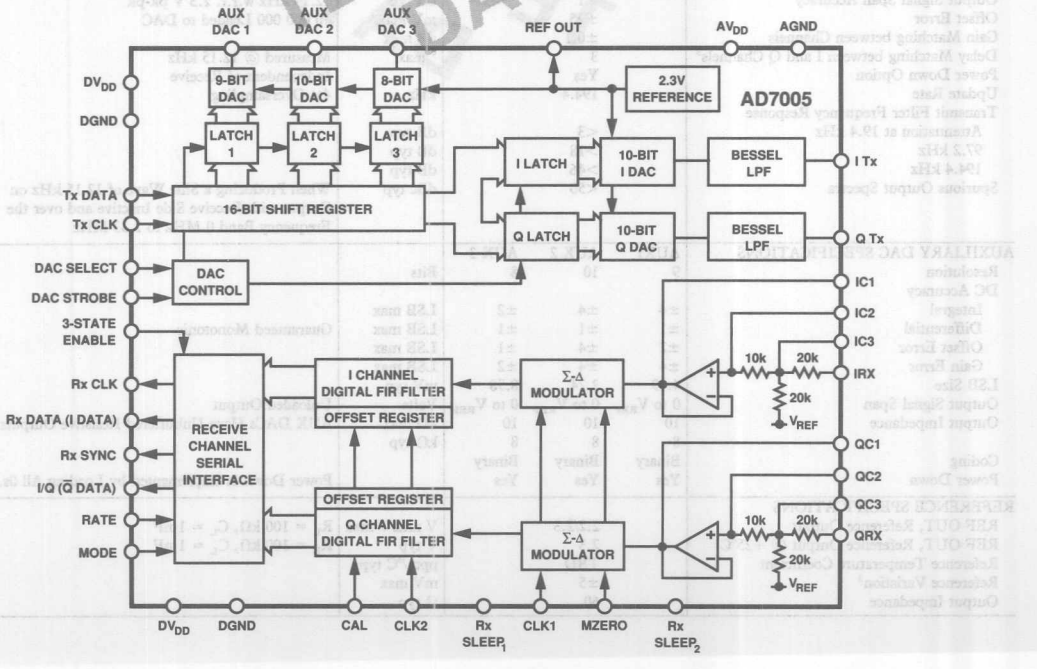
All the device control logic is contained on-chip.

The AD7005 is housed in 44-pin PQFP.

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PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Signal Input Span		±1.15		Volts	Biased on V_{REF} (2.3 V)
Sampling Rate		2.33		MHz	
Output Rate		48.6		kHz	RATE 0
		97.2		kHz	RATE 1
Accuracy					
Integral		1		LSB	
Differential[2]		0			
Bias Offset Error @ +25°C		±10		LSB	After Calibration
T_{MIN} to T_{MAX}		±12		LSB	After Calibration
Input Resistance (dc)		40		kΩ typ	
		38/42		kΩ min/max	
Input Capacitance		20		pF max	
Dynamic Specifications					
Dynamic Range		64		dB min	
Signal to (Noise + Distortion)		62		dB min	
Gain Match Between Channels		±0.1		dB max	Input Frequency = 12.15 kHz
Frequency Response					
0–17 kHz		±0.1		dB max	
19 kHz		−0.8		dB max	
21 kHz		−2.5		dB max	
35 kHz		−66		dB max	
>97.6 kHz		−72		dB max	
Group Delay Between Channels (0–21 kHz)		50		ns typ	
Coding		Twos Complement			
Absolute Group Delay Linearity (0–21 kHz)		126		µs typ	
Power Down Option		Yes			Independent of Transmit
TRANSMIT DAC SPECIFICATIONS					
Resolution		10		Bits	
Number of Channels		2			
DC Accuracy					
Integral		±2		LSB typ	
Differential		±2		LSB typ	Guaranteed Monotonic
Output Signal Span		±1.15		Volts typ	Centered on 2.3 V Nominal (10 kΩ/20 pF Load)
Output Signal Span Accuracy		±1		dB typ	12.15 kHz w.r.t. 2.3 V pk-pk
Offset Error		±25		mV max	10 000 000 Loaded to DAC
Gain Matching between Channels		±0.1		dB max	
Delay Matching between I and Q Channels[3]		3		° max	Measured @ 12.15 kHz
Power Down Option		Yes			Independent of Receive
Update Rate		194.4		kHz	4× Oversampling
Transmit Filter Frequency Response					
Attenuation at 19.4 kHz		<3		dB typ	
97.2 kHz		>18		dB typ	
194.4 kHz		>46		dB typ	
Spurious Output Spectra		<50		dBc typ	When Producing a Sine Wave of 12.15 kHz on Output with Receive Side Inactive and over the Frequency Band 0 MHz to 2.33 MHz
AUXILIARY DAC SPECIFICATIONS	AUX1	AUX 2	AUX 3		
Resolution	9	10	8	Bits	
DC Accuracy					
Integral	±4	±4	±2	LSB max	
Differential	±1	±1	±1	LSB max	Guaranteed Monotonic
Offset Error	±2	±4	±1	LSB max	
Gain Error	±4	±4	±2	LSB max	
LSB Size	4.49	2.24	8.98	mV typ	
Output Signal Span	0 to V_{REF}	0 to V_{REF}	0 to V_{REF}	Volts	Unloaded Output
Output Impedance	10	10	10	kΩ max	AUX DACs Have Unbuffered Resistive Outputs.
	8	8	8	kΩ typ	
Coding	Binary	Binary	Binary		
Power Down	Yes	Yes	Yes		Power Down Is Implemented by Loading All 0s.
REFERENCE SPECIFICATIONS					
REF OUT, Reference Output		2.2/2.3		V min/V max	R_L = 100 kΩ, C_L = 1 nF
REF OUT, Reference Output @ +25°C		2.3		V typ	R_L = 100 kΩ, C_L = 1 nF
Reference Temperature Coefficient		TBD		ppm/°C typ	
Reference Variation[3]		±5		mV max	
Output Impedance		60		Ω typ	

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	AD7005A	Units	Test Conditions/Comments
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD} – 0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	4.0	V min	$\|I_{OUT}\| \leq 200$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
I_{DD}			
All Sections Active	25	mA max	
ADC and Auxiliary Paths Active	13	mA max	Tx SLEEP = "1"
Transmit DAC and Aux Paths Active	12	mA max	Rx $SLEEP_1$ = Rx $SLEEP_2$ = V_{DD}
Auxiliary Path Only Active	2	mA max	Tx SLEEP = "1"; Rx $SLEEP_1$ = Rx $SLEEP_2$ = V_{DD}

NOTES
[1]Operating temperature ranges as follows: A Version: −40°C to +85°C.
[2]Unmeasurable: sigma-delta conversion is inherently free of differential nonlinearities.
[3]Defined as the delay between V_{REF} transition on the I and Q output as each DAC is stepped from 1/3 to 2/3 full scale.
Specifications subject to change without notice.

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PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . −0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND . . . −0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latchup.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



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INPUT CLOCK TIMING SPECIFICATIONS[1] (AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	300	300	ns min	CLK1, CLK2 Cycle Time
t_2	100	100	ns min	CLK1, CLK2 High Time
t_3	100	100	ns min	CLK1, CLK2 Low Time

AUX/SIGNAL DAC TIMING (V_{DD} Tx = V_{DD} Rx = +5 V ± 10%; Test = AGND = DGND Tx = DGND Rx = 0 V, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_4	100	100	ns min	Tx CLOCK Cycle Time
t_5	40/60	40/60	% max	Tx CLOCK Duty Cycle
	60/40	60/40	% max	
t_6	40	40	ns min	Tx DATA to Tx CLOCK Setup Time
t_7	50	50	ns min	Tx DATA to Tx CLOCK Hold Time
t_8	50	50	ns min	STROBE to Tx CLOCK Setup Time
t_9	40	40	ns min	STROBE to Tx CLOCK Hold Time
t_{10}	16 (t_4 + t_5)	16 (t_4 + t_5)	ns min	STROBE Duration
t_{11}	20	20	ns min	DAC SELECT to DAC STROBE Setup Time
t_{12}	20	20	ns min	DAC SELECT to DAC STROBE Hold Time

NOTES
[1]All input signal rise and fall times measured from 10% to 90% of +5 V. tr = tf = 20 ns.

PRELIMINARY TECHNICAL DATA

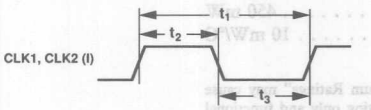


Figure 1. Clock Timing

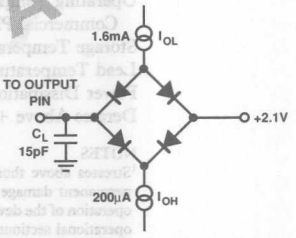


Figure 2. Load Timing Circuit

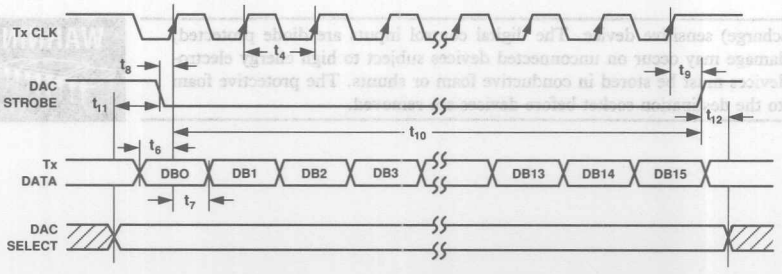


Figure 3. Aux/Signal DAC Timing Diagram

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RECEIVE SECTION TIMING

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = DGND = 0 V, $f_{CLK1} = f_{CLK2}$ = 2.33 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_{14}	0	0	ns min	Rx SLEEP Hold Time After CLK1, CLK2 High
t_{15}	25	25	ns min	Rx SLEEP Setup Time Before CLK1, CLK2 High
t_{16}	0	0	ns min	Rx SYNC to Rx SLEEP asserted, See Note[4]
	$15t_1$	$15t_1$	ns max	RATE 0
	$39t_1$	$39t_1$	ns max	RATE 1
t_{17}				Rx CLK Active after CLK1 Rising Edge Following Falling Edge of SLEEP
	56	56	ns	RATE 0
	32	32	ns	RATE 1
t_{18}				Rx CLK Cycle Time
	t_1	t_1	ns	MODE 0
	$2t_1$	$2t_1$	ns	MODE 1
t_{19}				Rx CLK High Pulse Width
	30	30	ns min	MODE 0
	90	90	ns min	MODE 1
t_{20}				Rx CLK Low Pulse Width
	30	30	ns min	MODE 0
	30	30	ns min	MODE 1
t_{21}	25	25	ns max	Propagation Delay from CLK1, CLK2 High to Rx CLK High
t_{22}	20	20	ns max	Rx SYNC Valid Prior to Rx CLK Falling.
t_{23}				Rx SYNC High Pulse Width
	t_1	t_1	ns	MODE 0
	$2t_1$	$2t_1$	ns	MODE 1
t_{24}				Rx SYNC Cycle Time
	$24t_1$	$24t_1$	ns	MODE 0 RATE 0
	$12t_1$	$12t_1$	ns	MODE 0 RATE 1
	$48t_1$	$48t_1$	ns	MODE 1 RATE 0
	$24t_1$	$24t_1$	ns	MODE 1 RATE 1
t_{25}	15	15	ns min	Rx DATA Valid After Rx CLK Rising Edge
t_{26}	15	15	ns max	Propagation Delay from Rx CLK Rising Edge to I/Q
t_{27}	10	10	ns max	Digital Output Rise Time[2]
t_{28}	10	10	ns max	Digital Output Fall Time[2]

CALIBRATION AND CONTROL TIMING

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND Tx = AGND Rx = DGND = 0 V, f_{CLK1}, f_{CLK2} = 2.33 MHz, V_{REF} = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_{29}	25	25	ns min	Rx SLEEP to CAL Setup Time
t_{30}	$608t_1$	$608t_1$	ns min	CAL Pulse Width
t_{31}	25	25	ns min	RATE, MODE or 3-STATE ENABLE Setup Time

NOTES
[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Digital output rise and fall times specify the time required for the output to go between 10% and 90% of 5 V.
[3]See Figure 2 for Test Circuit.
[4]t_{16} specifies a window, after Rx SYNC which marks the beginning of I data, where Rx SLEEP should be asserted for the current IQ data pair to be last prior to entering SLEEP mode.

PRELIMINARY TECHNICAL DATA

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PQFP Pin Number	Mnemonic	Function
POWER SUPPLY		
28	AV_{DD}	Positive power supply for analog section. This is +5 V ± 5%.
37	AGND	Analog ground.
4, 15	DV_{DD}	Positive power supply for digital section. This is +5 V ± 5%, both DV_{DD} pins must be tied together.
7, 16	DGND	Digital ground; both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
5	I Tx	Analog output for the I (In-phase) channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
3	Q Tx	Analog output for the Q (Quadrature) channel. This output comes from a 10-bit DAC and is filtered by a 4th order Bessel low-pass filter.
39	IRX	Analog input for the I receive channel.
42, 40	IC1, IC3	An external capacitor can be connected between these two pins, in order to configure the I channel input conditioning circuit as a Sallen & Key second order low-pass filter. Otherwise these pins should be left open circuit.
41	IC2	An external capacitor can be connected to this pin and AGND, in order to configure the I channel input conditioning circuit as a Sallen & Key second order low-pass filter. Otherwise these pins should be left open circuit.
2	QRX	Analog input for the Q receive channel.
43, 1	QC1, QC3	An external capacitor can be connected between these two pins, in order to configure the Q channel input conditioning circuit as a Sallen & Key second order low-pass filter. Otherwise these pins should be left open circuit.
44	QC2	An external capacitor can be connected to this pin and AGND, in order to configure the Q channel input conditioning circuit as a Sallen & Key second order low-pass filter. Otherwise these pins should be left open circuit.
34	AUX DAC1	Analog output voltage from the 9-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
36	AUX DAC2	Analog output voltage from the 10-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
35	AUX DAC3	Analog output voltage from the 8-bit auxiliary DAC. This is a voltage mode DAC with a high output impedance and hence should be buffered if used to drive moderate impedance loads.
38	REF OUT	Reference output, this is 2.5 volts nominal.
TRANSMIT AND AUXILIARY INTERFACE AND CONTROL		
8, 11	CLK1, CLK2	Master clock inputs for both the transmit and receive sections. CLK1 and CLK2 must be externally hardwired together and driven from a 2.33 MHz TTL compatible crystal.
31	DAC STROBE	DAC latch strobe, digital input. When DAC STROBE is brought low, it enables the 16-bit shift register to be loaded. On the rising edge of DAC STROBE, the contains of the shift register is transferred to either the I and Q-latches or to the auxiliary DAC latches, depending on DAC SELECT.
32	DAC SELECT	DAC SELECT, digital input. DAC SELECT determines whether the transmit DACs or the auxiliary DACs are being updated when loading the 16-bit shift register.
30	Tx CLK	Transmit clock, digital input. Serial data bits are loaded into the 16-bit shift register on the rising edge of Tx CLK while DAC STROBE is low.
33	Tx DATA	Transmit data, digital input. This input is used in conjunction with Tx CLK and DAC STROBE to load the 16-bit shift register.

PRELIMINARY TECHNICAL DATA

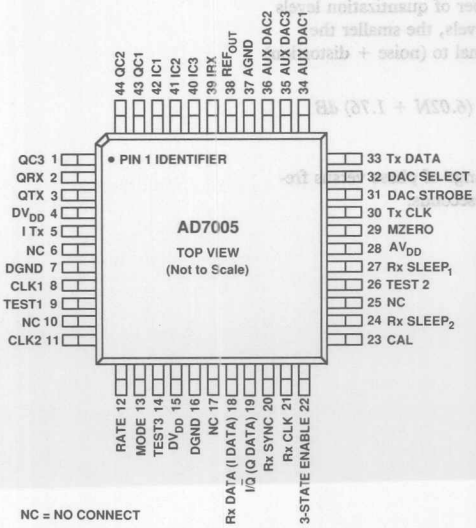
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PQFP Pin Number	Mnemonic	Function
RECEIVE INTERFACE AND CONTROL		
13	MODE	Digital control input. When high (MODE 1), the I and Q outputs are on separate pins (Q DATA and I DATA). When low (MODE 0), I and Q are on the same pin (Rx DATA).
12	RATE	Digital control input. This determines whether the receive section interface operates at a word rate of 97.2 kHz or at a word rate of 48.6 kHz. When high (RATE 1), the output word rate is 97.2 kHz. When low (RATE 0), the output word rate is 48.6 kHz.
18	Rx DATA (I DATA)	This is a dual-function digital output. When the device is operating in MODE 0, the Rx DATA (both I and Q) is available at this pin. When the device is operating in MODE 1, only I DATA is available at this pin.
19	I/Q (Q DATA)	This is a dual-function digital output. When the device is operating in MODE 0, it indicates whether I DATA or Q DATA is present on Rx DATA pin. In MODE 1, Q DATA is available at this pin.
20	Rx SYNC	Synchronization output for framing I and Q data at the receive interface.
21	Rx CLK	Output clock for the receive section interface.
22	3-STATE CONTROL	This digital input controls the output 3-state drivers on the receive section interface. When it is high, the outputs are enabled. When low, they are in high impedance.
23	CAL	Calibration control pin for digital filter section. When brought high, for a minimum of 608 master clock cycles, the receive section enters a calibration cycle. Where I and Q offset registers are updated, when the CAL pin is brought low again, with offset values which are subtracted out from subsequent ADC conversions. CAL should remain low during normal operation.
29	MZERO	Digital control input. When high the analog modulator input is internally grounded (i.e. tied to V_{REF}). MZERO, in conjunction with CAL, allows on-chip offsets to be calibrated out. Low for normal operation.
27, 24	Rx $SLEEP_1$, Rx $SLEEP_2$	Power down control inputs for receive section. When high, the receive section goes into stand-by mode and draws minimal current. Rx $SLEEP_1$ and Rx $SLEEP_2$ must be externally hardwired together for normal device operation.
TEST		
8, 26	Test 1, Test 2	Test pins for factory use only. These pins should be left unconnected and not used as routes for other circuit signals.
14	Test 3	Test pin. These must be tied to ground for normal device operation.

PRELIMINARY TECHNICAL DATA

4

PIN CONFIGURATION



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TERMINOLOGY

Signal Input Span
The input signal range for the I and Q channels is biased about V_{REF}. It can go ±1.25 volts about this point.

Sampling Rate
This is the rate at which the sigma-delta modulators on the receive channels sample the analog input.

Output Rate
This is the rate at which data words are made available at the Rx DATA pin (Mode 0) or the I DATA and Q DATA pins (Mode 1). There are two rates: RATE 0 and RATE 1. When operating in RATE 1 the output word rate is equal to 97.2 kHz, and is equal to 48.6 kHz for RATE 0.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the DAC or ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the DAC or ADC.

Bias Offset Error
This is the offset error (in LSBs) in the ADC section.

Dynamic Range
Dynamic Range is the ratio of the maximum output signal to the smallest output signal the converter can produce (1 LSB), expressed logarithmically, in decibels ($dB = 20\log_{10}$ (ratio)). For an N-bit converter, the ratio is theoretically very nearly equal to 2N (in dB, $20N\log_{10}(2) = 6.02N$). However, this theoretical value is degraded by converter noise and inaccuracies in the LSB weight.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency (fs/2), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for a sine wave is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Absolute Group Delay
Absolute group delay is the rate of change of phase versus frequency, d0/df. It is expressed in microseconds.

Group Delay Linearity
The group delay linearity or differential group delay is the group over the full band relative to the group delay at one particular frequency. The reference frequency for the AD7005 is 1 kHz.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Settling Time
This is the digital filter settling time in the AD7005 sigma-delta modulator section. On initial power up or after returning from the Sleep mode, it is necessary to wait this amount of time to get useful data.

Output Signal Span
This is the output signal range for the transmit channel section and the auxiliary DAC section. For the transmit channel, the span is ±1.25 volts centered on 2.5 volts and for the auxiliary DAC section it is 0 to $+V_{REF}$.

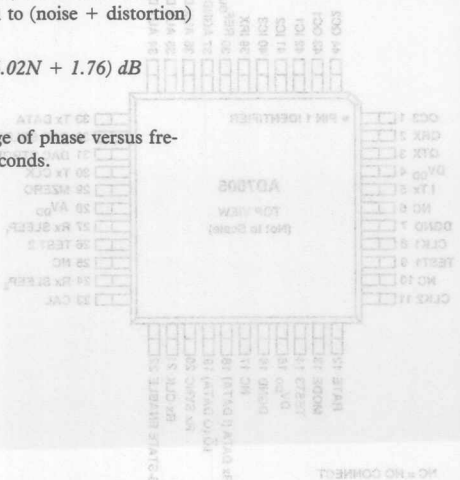
Output Signal Full-Scale Accuracy
This is the accuracy of the full-scale output (all 1s loaded to the DACs) on the transmit channel and is expressed in dBs.

Offset Error
This is the amount of offset in the transmit DACs and the auxiliary DACs and is expressed in mVs for the transmit section and in LSBs for the auxiliary section.

Gain Error
This is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out and is expressed in LSBs. In the AD7005, gain error is specified for the auxiliary section.

Output Impedance
This is a measure of the drive capability of the auxiliary DAC outputs and is expressed in kΩs.

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CIRCUIT DESCRIPTION

TRANSMIT SECTION

The transmit section of the AD7005 performs the baseband conversion of I and Q (In phase and Quadrature) waveforms for the TIA Digital cellular communications system. The transmit channel consists of two 10-bit DACs, followed by 4th order Bessel reconstruction filters.

Transmit DACs

The 10-bit DACs can be used to perform the conversion of I and Q waveforms when implementing $\pi/4$ DQPSK modulation in accordance with the TIA digital telephony standard. When Tx SLEEP is set (DB13 = "1"), the transmit section powers down, with the I Tx and Q Tx outputs connected to V_{REF} through a nominal impedance of 80 kΩ.

Reconstruction Filters

The reconstruction filters smooth the DAC output signals, providing continuous time I and Q waveforms at the output pins. These are 4th order Bessel low-pass filters with a cut-off frequency of approximately 19.4 kHz. Figure 5 shows a typical transmit filter frequency response, while Figure 6 shows a typical plot of group delay versus frequency. The filters are designed to have a linear phase response in the passband and due to the reconstruction filters' being on-chip, the phase mismatch between the I and Q transmit channels is kept to a minimum.

Digital Interface

Mode 0 Interfacing, DAC SELECT = "0"

In Mode 0 interfacing, both the transmit DACs and auxiliary DACs can be updated using a three-pin serial interface. The 16-bit serial register is organized into a data field (DB0–DB9) and a control field (DB10–DB15). Data is clocked into a 16-bit shift register on the rising edge of each Tx CLK, MSB first, and is framed by the DAC STROBE signal. On loading the 16-bit serial register, the DAC STROBE signal is brought high, preventing any further clocking of the serial register and updates the selected latch. Control bits DB13–DB15 relate to the transmit I and Q transmit DACs, and DB13 determines whether the transmit section is active (DB13 = 0) or in sleep mode (DB13 = 1), while control bits DB14 & DB15 relate to the individual loading of the I and Q 10-bit latches.

In order to simultaneously update the I and Q latches, a buffer latch is provided to temporarily store the contains for the Q latch. When DB14 = 1 and DB15 = 0, the contains of the data field (DB0–DB9) is transferred to a Q-buffer latch. When DB14 = 1 and DB15 = 1, the contains of the data field is transferred to the I latch and, simultaneously, the contains of the Q-buffer latch is transferred to the Q latch on the rising edge of DAC STROBE. Hence, to obtain simultaneous loading of the I and Q DACs, one must first load the Q buffer, then load the I latch.

PRELIMINARY TECHNICAL DATA

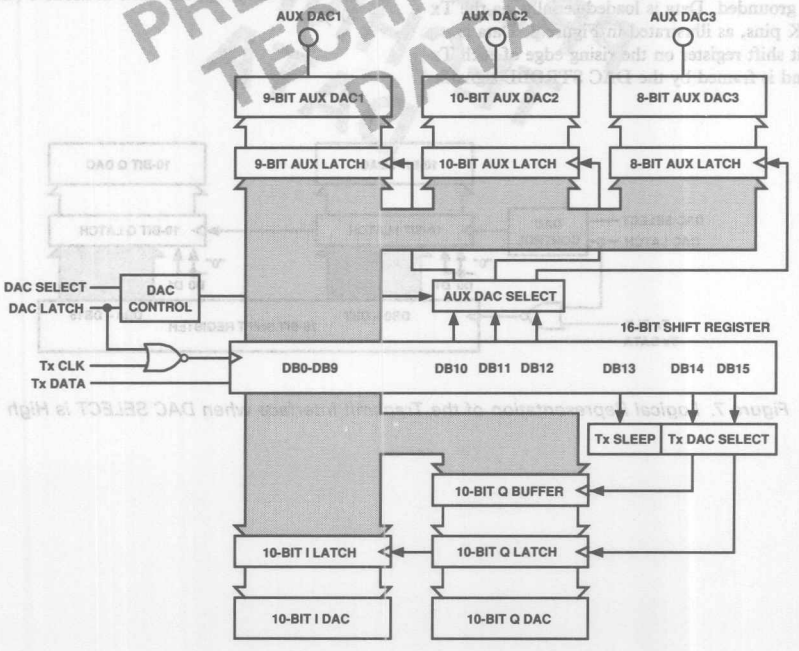


Figure 4. Logical Representation of the Transmit/Auxiliary Interface when DAC SELECT is Low

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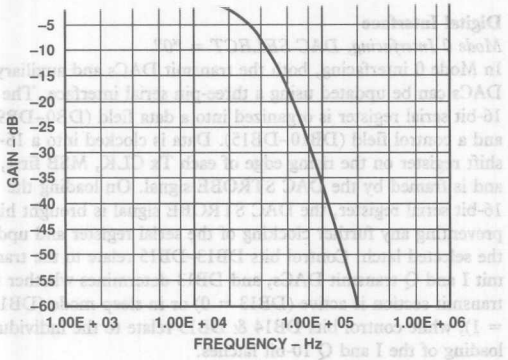


Figure 5. Transmit Filter Frequency Response

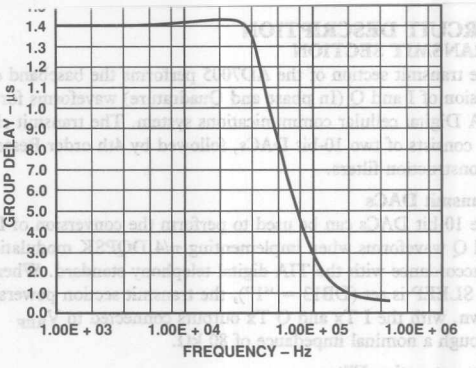


Figure 6. Transmit Filter Group Delay

Mode 1 Interfacing, DAC SELECT = "1"

Mode 1 interfacing provided direct access to the transmit DACs but only 8 of the 10 bits are available. If the DAC SELECT pin is high prior to DAC STROBE falling then the 16-bit serial register is organized as two 8-bit words. The lower 8 bits (DB0–DB7) are mapped to the I DAC and the higher 8 bits (DB8–DB15) are mapped to the Q DAC. The 2 LSBs of each DAC are internally grounded. Data is loaded serially via the Tx DATA and Tx CLK pins, as illustrated in Figure 3. Data is clocked into a 16-bit shift register on the rising edge of each Tx CLK, MSB first, and is framed by the DAC STROBE signal.

Once the 16 bits have been loaded, the rising edge of DAC STROBE updates both I and Q transmit DACs.

Figure 7 logically represents the serial interface when DAC SELECT is high. As with Mode 0 interfacing, the transmit DACs are put into sleep mode by setting a control bit (DB13) in the 16-bit shift register when in Mode 0 (DAC SELECT = "0").

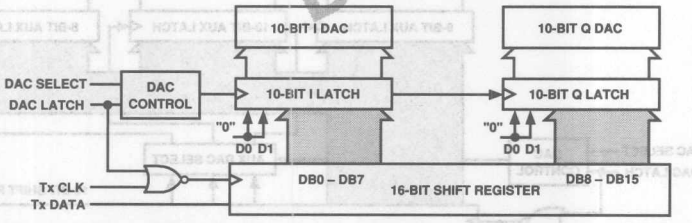


Figure 7. Logical Representation of the Transmit Interface when DAC SELECT is High

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INPUT CONDITIONING CIRCUIT

An input conditioning circuit, one for each channel, is provided so that antialiasing filters can be implemented on-chip, if required, and they can also be used to provide additional attenuation near the passband of the digital filter. The input conditioning circuits can be configured as a second order low-pass Sallen and Key active filter with the addition of only two external capacitors. They can also be configured as noninverting buffers by simply not connecting any external components. Figure 8 shows typical capacitor values, while Figures 9 and 10 show the frequency response and group delay for these capacitor values.

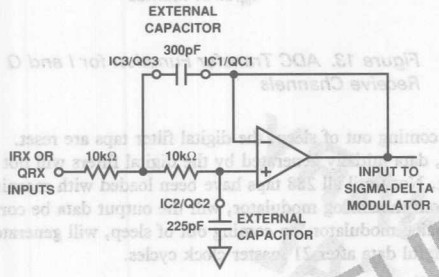


Figure 8. Equivalent Circuit for the IRX and QRX Inputs

SIGMA-DELTA ADC

The AD7005 receive channels employ a sigma-delta conversion technique that provides a high resolution 12-bit output for both I and Q channels with system filtering being implemented on-chip.

The output of the switched capacitor filter is continuously sampled at 1.165 MHz (master clock/2), by a charge-balanced modulator, and is converted into a digital pulse train whose duty cycle contains the digital information. Due to the high oversampling rate, which spreads the quantization noise from 0 to 582.5 kHz ($F_S/2$), the noise energy contained in the band of interest is reduced (Figure 11a). To reduce the quantization still further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 11b).

The digital filter that follows the modulator removes the large out-of-band quantization noise (Figure 11c), while converting the digital pulse train into parallel 12-bit-wide binary data. The 12-bit I and Q data are made available, via a serial interface, in a variety of formats.

Digital Filter

The digital filters used in the AD7005 receive section carry out two important functions. First, they remove the out-of-band quantization noise which is shaped by the analog modulator. Second, they are also designed to perform system level filtering, providing excellent rejection of the neighboring channels.

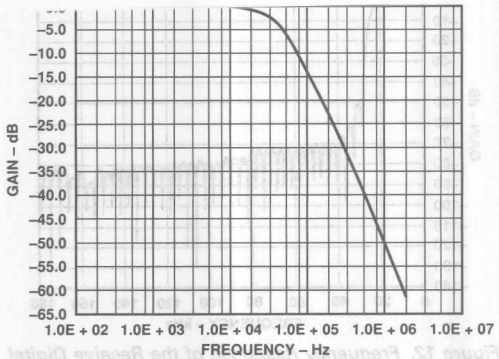


Figure 9. Frequency Response for Capacitors Values Shown

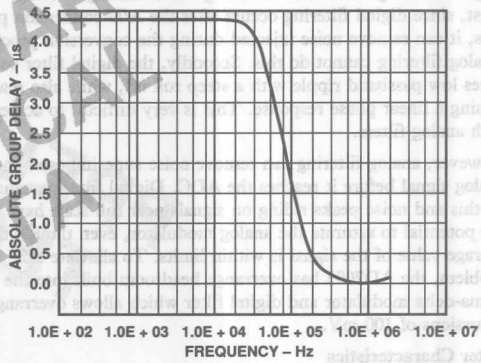


Figure 10. Absolute Group Delay for Capacitors Values Shown

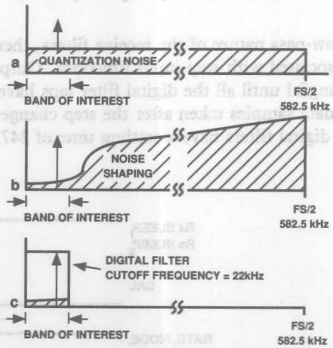


Figure 11. a) Effect of High Oversampling Ratio.
b) Use of Noise Shaping to Further Improve SNR.
c) Use of Digital Filtering to Remove the Out of Band Quantization Noise.

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4

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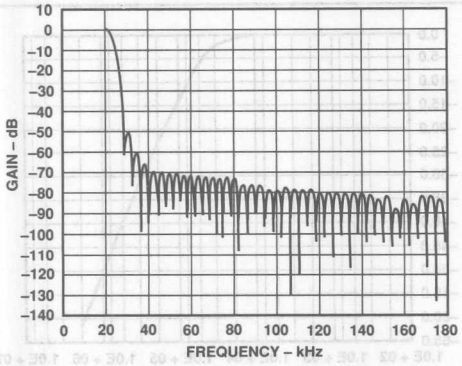


Figure 12. Frequency Response of the Receive Digital Filter

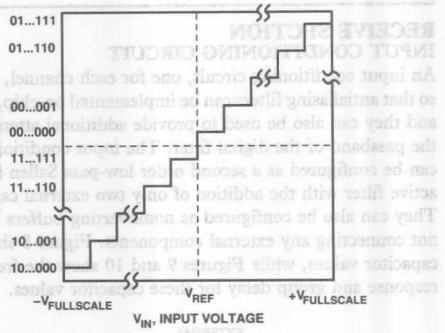


Figure 13. ADC Transfer Function for I and Q Receive Channels

Digital filtering has certain advantages over analog filtering. First, since digital filtering occurs after the A/D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Secondly, the digital filter combines low passband ripple with a steep roll off, while also maintaining a linear phase response. This is very difficult to achieve with analog filters.

However, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full-scale have the potential to saturate the analog modulator, even though the average value of the signal is within limits. To alleviate this problem, the AD7005 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV.

Filter Characteristics

The digital filter is a 288-tap FIR filter, clocked at half the master clock frequency. The frequency response is shown in Figure 12. The 3 dB point is at 22 kHz. The digital filter has a linear phase response with an absolute group delay of 123.6 μs ($144 \times 2t_1$).

Due to the low-pass nature of the receive filters, there is a settling time associated with step input functions. Output data will not be meaningful until all the digital filter taps have been loaded with data samples taken after the step change. Hence, the AD7005 digital filters have a settling time of 247.2 μs ($288 \times 2t_1$).

When coming out of sleep, the digital filter taps are reset. Hence, data initially generated by the digital filters will not be correct. Not until all 288 taps have been loaded with meaningful data from the analog modulator, will the output data be correct. The analog modulator, on coming out of sleep, will generate meaningful data after 21 master clock cycles.

Calibration

Included in the digital filter is a means by which receive signal offsets may be calibrated out. Calibration can be effected through the use of the CAL and MZERO pins.

Each channel of the digital low-pass filter section has an offset register. The offset register can be made to contain a value representing the dc offset of the preceding analog circuitry. In normal operation, the value stored in the offset register is subtracted from the filter output data before the data appears on the serial output pin. By so doing, the dc offset gets cancelled.

In each channel the offset register is cleared (twos complement zero) when CAL is high and becomes loaded with the first digital filter result after CAL falls. This result will be a measure of the channel dc offset if the analog channel is switched to zero prior to CAL falling. Time must be provided for the analog circuitry and the digital filter to settle after the analog circuitry is switched to zero and before CAL falls. The offset register will then be loaded with the proper representation of the dc offset.

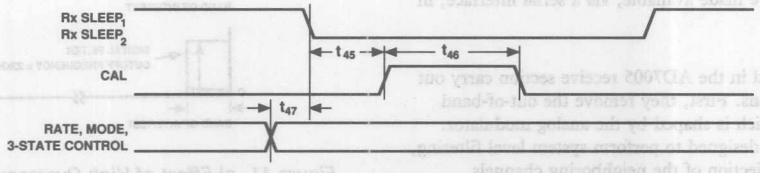


Figure 14. Calibration and Control Timing

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CAL must be high for more than 608 master clock cycles (CLK1, CLK2). If the analog channels are switched to zero coincident with CAL rising, this time is also sufficient to satisfy the settling time of the analog sigma-delta modulators and the digital filters. CAL may be held high for an unlimited time if convenient or necessary. Only the digital result following the fall of CAL will be loaded into each offset register. After CAL falls, normal operation resumes immediately.

The offset registers are static and retain their contents even during sleep mode (Rx $SLEEP_1$ and Rx $SLEEP_2$ high). They need only be updated if drifts in the analog dc offsets are experienced or expected. However, on initial application of power to the digital supply pins the offset registers may contain grossly incorrect values, and therefore calibration must be activated at least once after power is applied even if the facility of calibration is not regularly used.

The MZERO pin can be used to zero the sigma-delta modulators if calibration of preceding analog circuitry is not required. Each analog modulator has an internal analog multiplexer which is controlled by MZERO. With MZERO low, the modulator inputs are connected to the IRx and QRx pins for normal operation. With MZERO high, both modulators inputs are connected to the REF OUT pin, which is analog ground for the modulators. Typically, the CAL and MZERO pins would be tied together and driven by the same digital signal. If calibration of external analog circuitry is desired, MZERO should be kept low during the calibration cycle.

The offset registers have enough resolution to hold the value of any dc offset between ±5 V. However, the performance of the sigma-delta modulators will degrade if full-scale signals with more that 100 mV of offset are experienced. If large offsets are present, these can be calibrated out, but signal excursions from the offsets should be limited such that the I Rx and Q Rx voltages remain within ±1.35 V of V_{REF}.

Digital Interface

A flexible serial interface is provided for the AD7005 receive section. Four basic operating modes are available. Table I shows the truth table for the different serial modes that are available. The MODE pin determines whether the I and Q serial data is made available on two separate pins (MODE 1) or, combined on to a single output pin (MODE 0). The RATE pin determines whether I and Q receive data is provided at 97.2 kHz (RATE 1) or at 48.6 kHz (RATE 0).

When the receive section is put back into sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ high, the receive interface will complete the current IQ cycle before entering into a low-power sleep mode.

MODE 0 RATE 1 Interface

The timing diagram for the MODE 0 RATE 1 receive interface is shown in Figure 15. It can be use to interface to DSP processors requiring the use of only one serial port.

When using MODE 0, the serial data is made available on the Rx DATA pin, with the I/Q pin indicating whether the 12-bit word being clocked out is an I sample or a Q sample. Although the I data is clocked out before the Q data, internally both samples are processed together. RATE 1 selects an output word rate of 97.2 kHz, which is equal to the master clock (CLK1, CLK2) divided by 24.

When the receive section is brought out of sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ low, (after 32 master clock cycles) the Rx CLK output will continuously shift out I and Q data, always beginning with I data. Rx SYNC provides a framing signal that indicates the beginning of an I or Q, 12-bit data word that is valid on the next falling edge of Rx CLK. On coming out of sleep, Rx SYNC goes high one clock cycle before the beginning of I data, and subsequently goes high in the same clock cycle as the last bit of each 12-bit word (both I and Q). Rx DATA is valid on the falling edge of Rx CLK and is clocked out MSB first, with the I/Q pin indicating whether Rx DATA is I data or Q data.

MODE 0 RATE 0 Interface

Figure 16 shows the receive timing diagram when MODE 0, RATE 0 is selected. Again, I and Q data are shifted out on the Rx DATA pin, but here the output word rate is reduced to 48.6 kHz, this being equal to the master clock (CLK1, CLK2) divided by 48.

Once the receive section is brought out of sleep mode, (after 56 master clock cycles) the Rx CLK output becomes active and generates an Rx SYNC framing pulse on the first Rx CLK. This is followed by 12 continuous clock cycles during which the I data is shifted out on the Rx DATA pin. Following, the Rx CLK remains high for 11 master clock cycles before clocking out the Q data in exactly the same manner.

Rx DATA is valid on the falling edge of Rx CLK with the I/Q pin indicating whether Rx DATA is I data or Q data.

MODE 1 RATE 1 Interface

Figure 17 shows the timing for MODE 1 RATE 1 receive digital interface. MODE 1 RATE 1 gives an output word rate of 97.2 kHz, but I and Q data are transferred on separate pins. I data is shifted out on Rx DATA (I DATA) pin and Q data is shifted out on the I/Q (Q DATA) pin. RATE 1 selects an output word rate of 97.2 kHz (this is equal to the master clock divided by 24).

When the receive section is brought out of sleep mode, by bringing Rx $SLEEP_1$ and Rx $SLEEP_2$ low, (after 32 master clock cycles) the Rx CLK output will continuously shift out I and Q data, on separate pins. Rx SYNC provides a framing signal that is used to indicate the beginning of both the I and Q, 12-bit data word that is valid on the next falling edge of Rx CLK. On coming out of sleep, Rx SYNC goes high one clock cycle before the beginning of I data, and subsequently goes high in the same clock cycle as the I and Q LSBs. It takes 24 Rx CLKs (excluding the first framing pulse) to complete a single I/Q cycle. I DATA and Q DATA is valid on the falling edge of Rx CLK and is clocked out MSB first.

MODE 1 RATE 0 Interface

Figure 18 shows the receive timing diagram when MODE 1 RATE 1 is selected. MODE 1 RATE 1, again I and Q data are transferred on separate pins. I data is shifted out on Rx DATA (I DATA) pin and Q data is shifted out on the I/Q (Q DATA) pin. The output word rate is reduced to 48.6 kHz, which is equal to the master clock (CLK1, CLK2) divided by 48.

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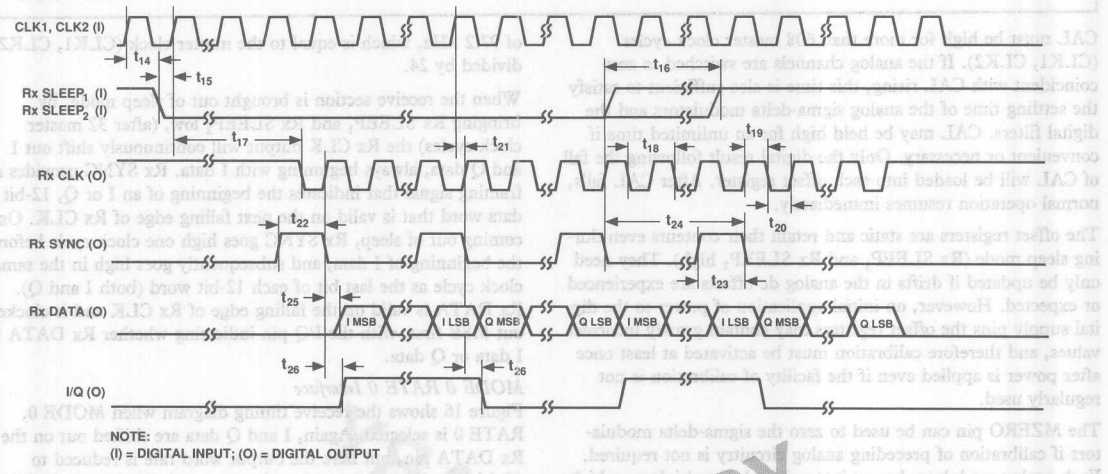


Figure 15. Mode 0, Rate 1 Receive Timing

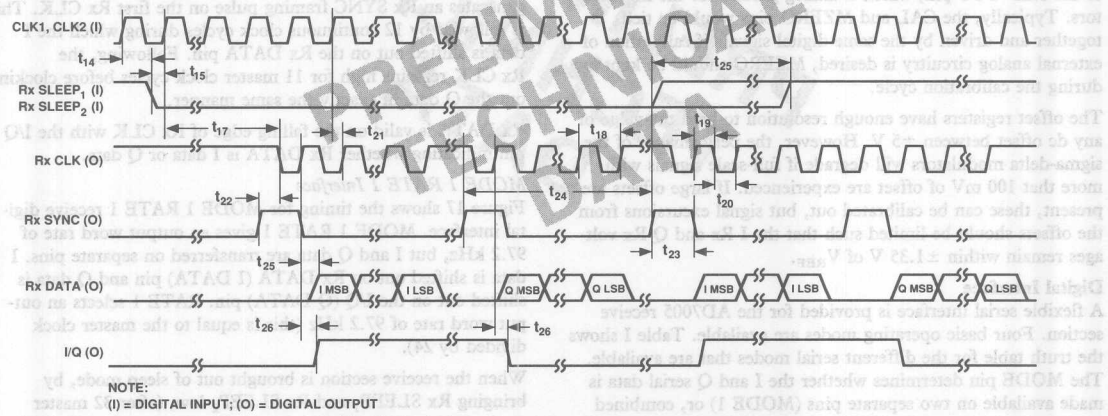
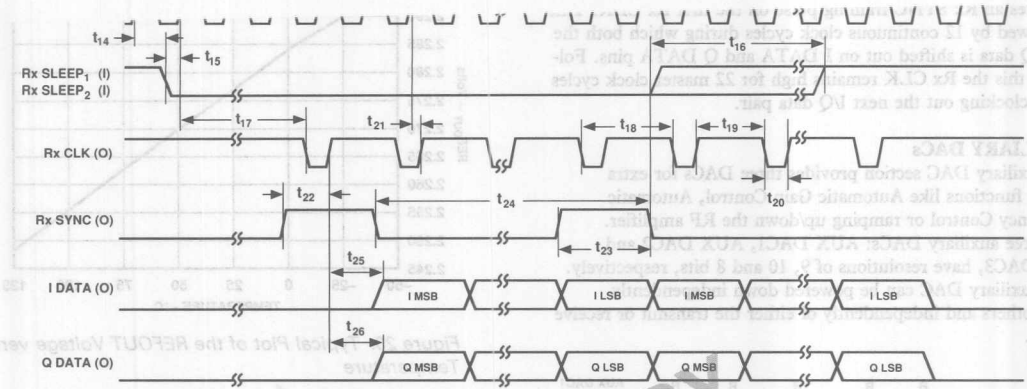


Figure 16. Mode 0, Rate 0 Receive Timing

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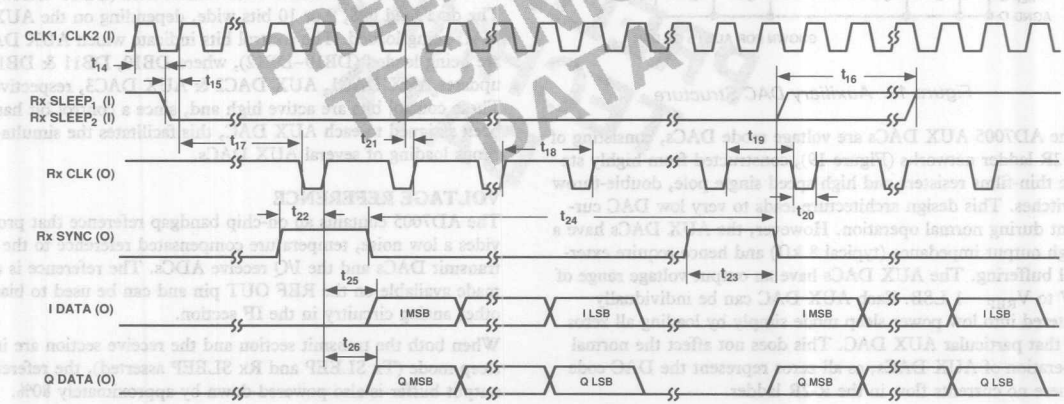
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NOTE:
(I) = DIGITAL INPUT; (O) = DIGITAL OUTPUT

Figure 17. Mode 1, Rate 1 Receive Timing

PRELIMINARY TECHNICAL DATA



NOTE:
(I) = DIGITAL INPUT; (O) = DIGITAL OUTPUT

Figure 18. Mode 1, Rate 0 Receive Timing

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56 master clock cycles, the Rx CLK output becomes active and generates an Rx SYNC framing pulse on the first Rx CLK. This is followed by 12 continuous clock cycles during which both the I and Q data is shifted out on I DATA and Q DATA pins. Following this the Rx CLK remains high for 22 master clock cycles before clocking out the next I/Q data pair.

AUXILIARY DACs

The auxiliary DAC section provides three DACs for extra control functions like Automatic Gain Control, Automatic Frequency Control or ramping up/down the RF amplifier. The three auxiliary DACs: AUX DAC1, AUX DAC2 and AUX DAC3, have resolutions of 9, 10 and 8 bits, respectively. Each auxiliary DAC can be powered down independently of the others and independently of either the transmit or receive section.

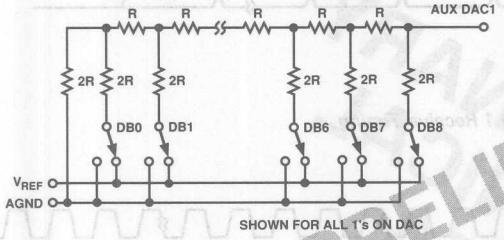


Figure 19. Auxiliary DAC Structure

The AD7005 AUX DACs are voltage mode DACs, consisting of R-2R ladder networks (Figure 19), constructed from highly stable thin-films resisters and high speed single pole, double-throw switches. This design architecture leads to very low DAC current during normal operation. However, the AUX DACs have a high output impedance (typical 8 kΩ) and hence require external buffering. The AUX DACs have an output voltage range of 0V to V_{REF} −1 LSB. Each AUX DAC can be individually entered into low power sleep mode simply by loading all zeros to that particular AUX DAC. This does not affect the normal operation of AUX DACs, as all zeros represent the DAC code where no currents flow in the R-2R ladder.

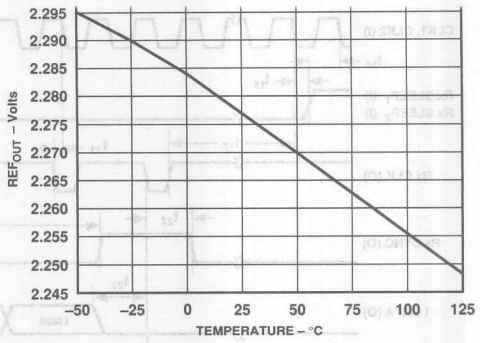


Figure 20. Typical Plot of the REFOUT Voltage versus Temperature

Digital Interface

AUX DAC loading is accomplished via the same 16-bit shift register used for loading the transmit DACs. When loading any of the auxiliary DACs, the DAC SELECT signal must be low. Figure 4 logically represents the serial interface when DAC SELECT is low. The 16-bit serial word is organized as a data field (DB0–DB9) combined with control field (DB10–DB13). The data field is 8, 9 or 10 bits wide, depending on the AUX DAC being loaded. The control bits indicate which AUX DACs are being loaded (DB10–DB12), where DB10, DB11 & DB12 updates AUX DAC1, AUX DAC2 & AUX DAC3, respectively. These control bits are active high and, since a control bit has been assigned to each AUX DAC, this facilitates the simultaneous loading of several AUX DACs.

VOLTAGE REFERENCE

The AD7005 contains an on-chip bandgap reference that provides a low noise, temperature compensated reference to the I/Q transmit DACs and the I/Q receive ADCs. The reference is also made available on the REF OUT pin and can be used to bias other analog circuitry in the IF section.

When both the transmit section and the receive section are in sleep mode (Tx SLEEP and Rx SLEEP asserted), the reference output buffer is also powered down by approximately 80%.

Table I. Truth Table for the Mode and Rate Pins

Mode	Rate	Data Format		Output Word Rate
0	0	IQ Data	$I/\overline{Q}$	48.6 kHz
0	1	IQ Data	$I/\overline{Q}$	97.2 kHz
1	0	I Data	Q Data	48.6 kHz
1	1	I Data	Q Data	97.2 kHz

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

CMOS DDS IF Modulator

AD7008

FEATURES
32-Bit Phase Accumulator
10-Bit Analog DAC Output
50 MHz Clock
20 MHz Output Capability
Frequency, Phase and Amplitude Modulation
Full AM Quadrature Modulator for SSB
Unused Section Power Down
Bit Serial or Parallel Control Interface
Single +5 V Supply
Low Power
TTL/5 V CMOS Compatible Logic Inputs
8-/16-Bit Microprocessor Interface
44-Pin PQFP

GENERAL DESCRIPTION

The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for SSB generation.

Clock rates up to 50 MHz are supported, yielding usable analog outputs up to about 20 MHz. Frequency accuracy can be controlled to one part in 4 billion. Modulation is controlled by loading registers either through the parallel microprocessor interface or the serial interface. A frequency select pin permits selection between two frequencies on a per cycle basis.

An amplitude modulator contains two multipliers fed with sine and cosine values from a ROM lookup table, and with amplitude values loaded from either the parallel or serial ports. When loaded with quadrature data, the sum of the two multipliers provides a SSB RF signal.

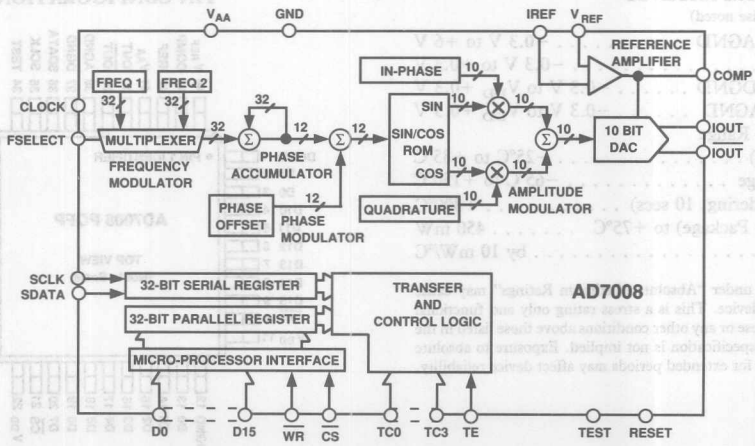
The serial and parallel interfaces may be operated independently and asynchronously from the DDS clock; the transfer control signals are internally synchronized to prevent metastability problems. The synchronizer can be bypassed to reduce the transfer latency in the event that the microprocessor clock is synchronous with the DDS clock.

A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface). The DAC may be adjusted for speed and power through a single external resistor.

4

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7008—SPECIFICATIONS[1] (V_{DD} +5 V ± 5%; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

Parameter	AD7008A	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Number of Channels	1		
Update Rate	50	MSPS	
DC Accuracy			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	
Dynamic Specifications			
Signal-to-Noise Ratio	TBD	dB min	
Total Harmonic Distortion	TBD	dB min	
Peak Spurious Noise	TBD	dB min	
Coding	Binary		
Power-Down Option	Yes		
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD} −0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	4.0	V min	$\|I_{OUT}\| \leq 40$ µA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			
Normal Operation	TBD	mA max	SLEEP = 0 V
Low Power Sleep Mode	TBD	mA max	SLEEP = V_{DD}

NOTE
[1]Operating temperature ranges as follows: A Version; −40°C to +85°C.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

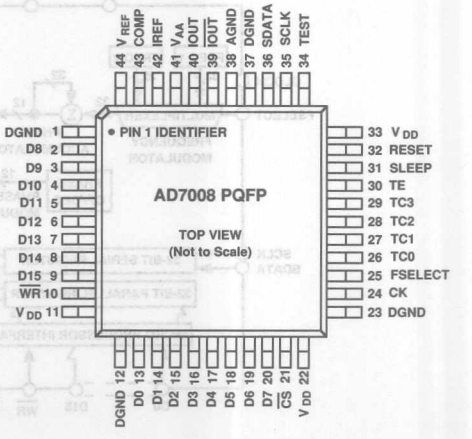
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} TX, V_{DD}, RX to AGND . . . . . −0.3 V to +6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digitial I/O Voltage to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Analog I/O Voltage to AGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . −25°C to +85°C
Storage Temperate Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C . . . . . by 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



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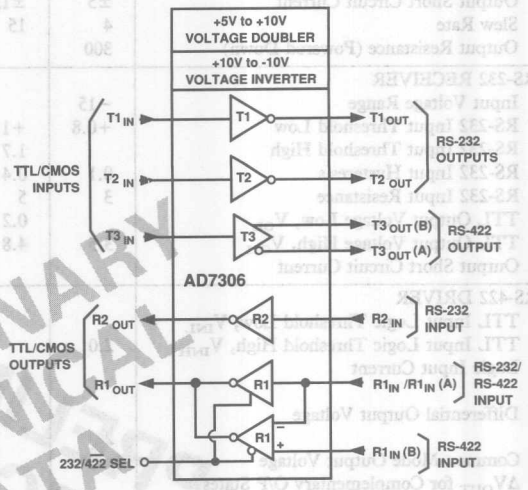
+5 V Powered RS-232, RS-422 Transceiver

AD7306

FEATURES
RS-232 and RS-422 on One Chip
Single +5 V Supply
0.1 μF Capacitors
Short Circuit Protection
Excellent Noise Immunity
Low Power BiCMOS Technology
High Speed, Low Skew RS-422 Operation

APPLICATIONS
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7306 line driver/receiver is a 5 V monolithic product which provides an interface between TTL signal levels and dual standard EIA RS-232/RS-422 signal levels. The part contains two RS-232 drivers, one RS-422 driver, one RS-232 receiver, and one receiver which can be configured either as RS-232 or as RS-422.

An internal charge pump voltage converter facilitates operation from a single +5 V power supply. The internal charge pump generates ±10 V levels allowing RS-232 output levels to be developed without the need for external bipolar power supplies.

A highly efficient charge pump design allows operation using non polarized, miniature 0.1 μF capacitors. This gives a considerable saving in printed circuit board space over conventional products which use up to 10 μF capacitors. The charge pump output voltages may also be used to power external circuitry which requires dual supplies.

The RS-232 channels are suitable for communications rates up to 60 kHz and the RS-422 channels are suitable for high speed communications up to 500 kHz. The RS-422 transmitter complementary outputs are closely matched and feature low timing skew between the complementary outputs. This is often an essential requirement to meet tight system timing specifications.

All inputs feature ESD protection, all driver outputs feature high source and sink current capability and are internally protected against short circuits on the outputs. An epitaxial layer is used to guard against latch-up.

The part is available in 24-pin DIP and SOIC packages.

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RS-232 DRIVER					
TTL Input Logic Threshold Low, V_{INL}		1.4	0.8	V	
TTL Input Logic Threshold High, V_{INH}	2.0	1.4		V	
Input Logic Current		5	20	µA	
RS-232 High Level Output Voltage	5.0	7.3		V	R_L = 3 kΩ
RS-232 Low Level Output Voltage	−5.0	−6.5		V	R_L = 3 kΩ
Output Short Circuit Current	±5	±12		mA	V_{OUT} = 0 V
Slew Rate	4	15	30	V/µs	C_L = 2500 pF, R_L = 3 kΩ
Output Resistance (Powered Down)	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±3 V
RS-232 RECEIVER					
Input Voltage Range	−15		+15	V	
RS-232 Input Threshold Low	+0.8	+1.3		V	
RS-232 Input Threshold High		1.7	+2.4	V	
RS-232 Input Hysteresis	0.1	0.4	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}		0.2	0.4	V	V_{CC} = +5 V, I_{OUT} = +4 mA
TTL Output Voltage High, V_{OH}	3.5	4.8		V	V_{CC} = +5 V, I_{OUT} = −4 mA
Output Short Circuit Current			±85	mA	0 V ≤ V_{OUT} ≤ V_{CC}
RS-422 DRIVER					
TTL Input Logic Threshold Low, V_{INL}			0.8	V	
TTL Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current			+2	µA	V_{IN} = 5 V
			−2	µA	V_{IN} = 1 V
Differential Output Voltage			5.0	V	V_{CC} = 5 V, R_L = ∞
	2			V	V_{CC} = 5 V, R_L = 100 Ω
Common-Mode Output Voltage			3	V	
ΔV_{OUT} for Complementary O/P States			0.2	V	R_L = 100 Ω
Output Short Circuit Current	35		150	mA	−1 V ≤ V_{CMR} ≤ +7 V
RS-422 RECEIVER					
Common-Mode Voltage Range			±7	V	Typical RS-422 Input Voltage <5 V
Differential Input Threshold Voltage	−0.2		+0.2	V	
Input Voltage Hysteresis		70		mV	V_{CM} = 0 V
Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA, V_{CC} = 5 V
TTL Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −4.0 mA, V_{CC} = 5 V
Short Circuit Output Current	±7		±85	mA	V_{OUT} = GND or V_{CC}
POWER SUPPLY CURRENT					
I_{CC}		18	30	mA	Outputs Unloaded
CHARGE PUMP VOLTAGE GENERATOR					
V+ Output Voltage	7.8	8.8		V	I_{OUT} = 0 mA
	7.3	8.2		V	I_{OUT} = 5 mA
	6.8	7.4		V	I_{OUT} = 10 mA
	5.8	6.6		V	I_{OUT} = 15 mA
V− Output Voltage	−7.3	−8.6		V	I_{OUT} = 0 mA
	−6.3	−7.3		V	I_{OUT} = −5 mA
Generator Rise Time		200		µs	

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%, C1 = C2= C3 = C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units
Switching Characteristics				
Propagation Delay RS-422				
TTL/CMOS to RS-422 t_{PLH}		35	100	ns
TTL/CMOS to RS-422 t_{PHL}		35	100	ns
RS-422 O/P to O/P t_{SKEW}		5	10	ns
Driver Rise/Fall Time t_R, t_F		15	40	ns
RS-422 Receiver				
Input to Output t_{PLH}, t_{PHL}		110	200	ns
RS-232 Disable to RS-422 Enable t_{EN1}		25	100	ns
RS-422 Disable to RS-232 Enable t_{EN2}		25	100	ns
Baud Rate				
RS-232	57.6			kHz
RS-422	500			kHz

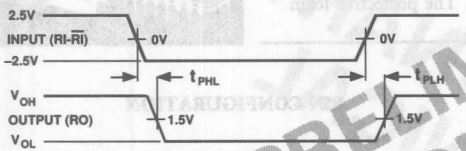


Figure 1. RS-422 Receiver Timing

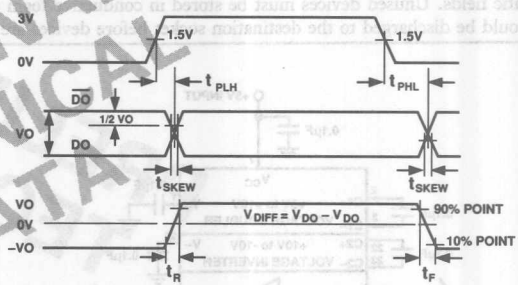


Figure 2. RS-422 Transmitter Timing

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . +7 V
V+ . . . . . (V_{CC} −0.3 V) to +13.2 V
V− . . . . . +0.3 V to −13.2 V
Inputs
$T1_{IN}$, $T2_{IN}$ . . . . . V− to V+
$T3_{IN}$ . . . . . −0.3 V to V_{CC} + 0.3 V
$R1_{IN}$ A/B, $R2_{IN}$ . . . . . −25 V to +25 V
SEL . . . . . −0.3 V to V_{CC} +0.3 V
Outputs
$T1_{OUT}$,$T2_{OUT}$ . . . . . (V+, +0.3 V) to (V−, +0.3 V)
$T3_{OUT}$(A), (B) . . . . . −15 V to +15 V
$R1_{OUT}$, $R2_{OUT}$ . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
T_{OUT} . . . . . Continuous

Power Dissipation
Plastic DIP (Derate 7 mW/°C above +70°C) . . . . . 675 mW
Small Outline (Derate 7 mW/°C above +70°C) . . . . 375 mW
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PRELIMINARY TECHNICAL DATA

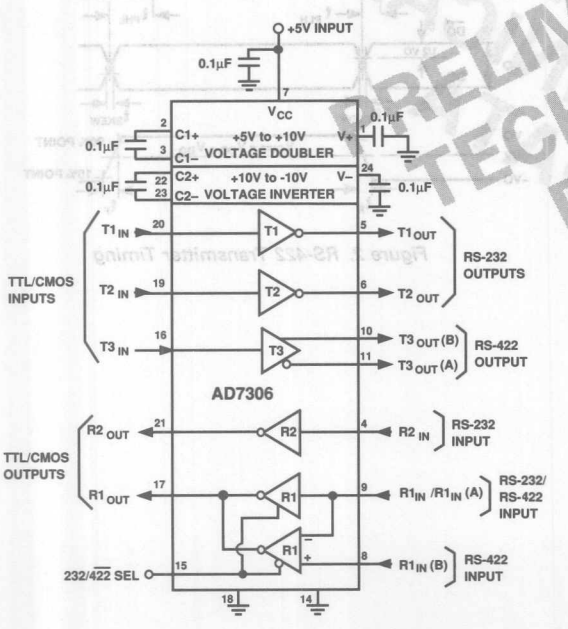
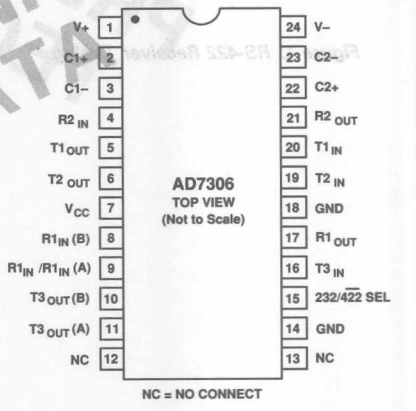


Figure 3. Application Circuit

PIN CONFIGURATION



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

GENERAL DESCRIPTION

The AD7306 drivers/receivers provide an interface which is compatible with RS-232/RS-422 standard interfaces. As both standards are widely accepted it is often necessary to provide an interface which is compatible with both. The AD7306 is ideally suited to this type of application as both standards may be met using only one package.

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated below. First the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

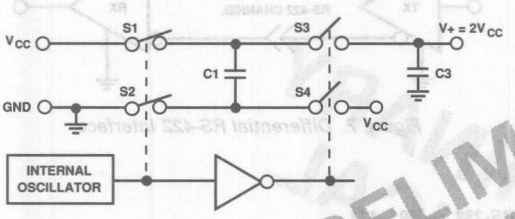


Figure 4. Voltage Doubler

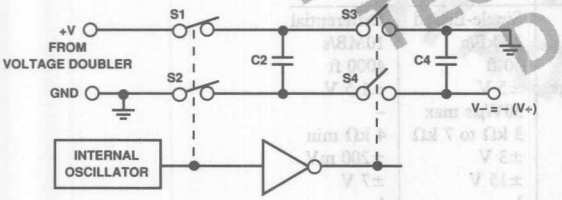


Figure 5. Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable.

The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

The generator rise time after power up is 200 µs typical. This time is necessary to completely charge the storage capacitors in the charge pump. Therefore, RS-232 data transmission should not be initiated until this time has elapsed after switch on. This will ensure that valid data is transmitted.

RS-232 Drivers

The RS-232 drivers in the/AD7306 meet the EIA RS-232 specifications. The drivers are inverting level shifters which convert TTL/CMOS levels into RS-232-C output levels. The input switching threshold is typically 1.3 V. With a typical RS-232 load, the output levels are ±8 V. Under worst case load conditions, the drivers are guaranteed to provide ±5 V which meets the minimum RS-232 requirement. The output slew rate is internally limited to <30 V/µs without the need for an external slew-limiting capacitor. Short circuit protection is also provided which prevents damage in the event of output fault conditions. Active current limiting is provided which limits the output short circuit current but which does not degrade the output voltage swing with maximum load as conventional passive limiting would.

RS-232 Receivers

The receivers are inverting level shifters which accept RS-232-C input levels (±3 V to ±15 V) and translates them into 5 V TTL/CMOS levels. The input switching thresholds are 0.75 V minimum and 2.5 V maximum which are well within the RS-232-C requirement of ±3 V. Internal pull-down resistors to GND are provided on the receiver inputs. This ensures that an unconnected input will be interpreted as a low level giving a logic "1" on the TTL/CMOS output. Excellent noise immunity is achieved by the use of hysteresis and internal filtering circuitry. The filter rejects noise glitches of up to 0.5 µs in duration.

RS-422 Drivers

The RS-422 drivers on the AD7306 accept TTL/CMOS inputs and translate them into differential RS-422 level signals. The input switching threshold is typically 1.3 V. The unloaded output differential voltage is typically ±4.5 V (see Typical Performance Characteristics). Short circuit protection is provided on the output which limits the current to less than 100 mA. Only one output should be shorted at any time to avoid exceeding the total power dissipation for the package.

RS-422 Receivers

The RS-422 receivers on the AD7306 accept differential input signals and translates them into TTL/CMOS output levels. Excellent noise immunity is achieved using the differential configuration.

PRELIMINARY TECHNICAL DATA

4

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Single-ended interfaces are used for low speed, short distance communications such as from a computer terminal to a printer. A single line is used to carry the signal. Various standards have been developed to standardize the communication link, the most popular of these being the RS-232. The RS-232 standard was introduced in 1962 by the EIA and has been widely used throughout the industry. It was developed for single-ended data transmission at relatively slow data rates over short distances. A typical RS-232 interface is shown in Figure 6.

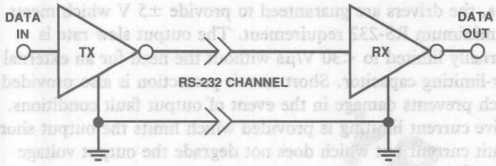


Figure 6. Single-Ended RS-232 Interface

When transmitting at high data rates, over long distances and through noisy environments, single-ended data transmission is often inadequate. In this type of application, differential data transmission offers superior performance. Differential transmission uses two signal lines to transmit data. It rejects ground shifts and is insensitive to noise signals which appear as common mode voltages on the transmission lines. To accommodate faster data communication, the differential RS-422 standard was developed. Therefore, it can be used to reliably transmit data at higher speeds and over longer distances than single-ended transmission. A typical RS-422 interface is shown in Figure 7.

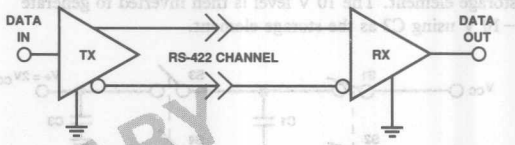


Figure 7. Differential RS-422 Interface

Table I. Comparison of RS-232 and RS-422 Interface Standards

Specification	RS-232-C	RS-422
Transmission Type	Single-Ended	Differential
Maximum Data Rate	20 kB/s	10MB/s
Maximum Cable Length	50 ft	4000 ft
Minimum Driver Output Voltage	±5 V	±1.5 V
Slew Rate	30V/μs max	–
Receiver Input Resistance	3 kΩ to 7 kΩ	4 kΩ min
Receiver Input Sensitivity	±3 V	±200 mV
Receiver Input Voltage Range	±15 V	±7 V
No. of Drivers per Line	1	1
No. of Receivers per Line	1	10

PRELIMINARY TECHNICAL DATA

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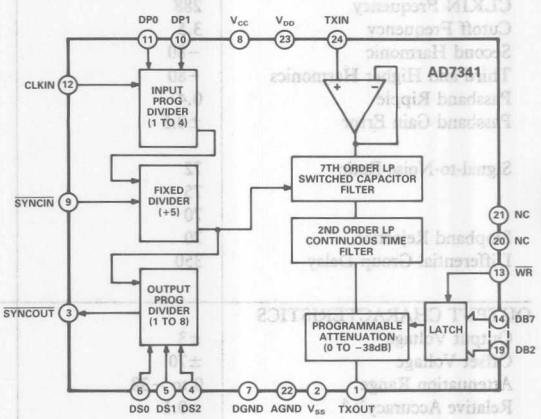
LC²MOS Voiceband Reconstruction and Antialiasing Filter Set

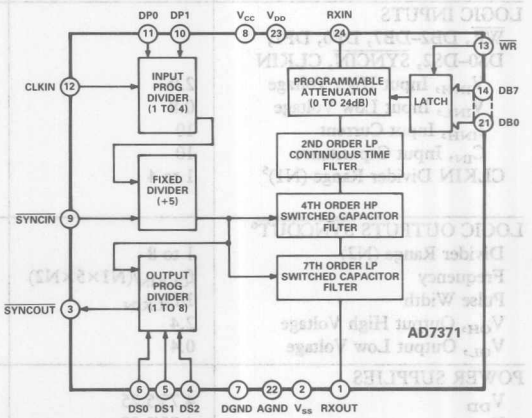
AD7341/AD7371

FEATURES

- **AD7341 – Transmit (Reconstruction) Filter for 14-Bit DAC (AD7840)**
  Programmable Attenuation (0dB to −38dB)
- **AD7371 – Receive Filter for 14-Bit ADC (AD7871)**
  Programmable Gain (0dB to 24dB)
- **70dB Stopband Attenuation**
- **75dB In-Band Signal-to-Noise Ratio**
- **Better Than −75dB Total Harmonic Distortion**
- **CCITT V.32 and V.33 Compatible**
- **Small, 0.3″, 24-Pin Plastic Package and 28-Pin PLCC**

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7341 and AD7371 are reconstruction and antialiasing filters designed for use in high speed voiceband modems with speeds up to 14.4 kbits/sec, in accordance with CCITT V.32 and V.33 recommendations. These filters, along with the AD7840 DAC, the AD7871 ADC and a digital signal processor (DSP) can be used to implement a complete modem.

The AD7341 is the transmit or reconstruction filter. It implements the filter function using a seventh order low pass switched capacitor filter and a second order low pass continuous time filter. The cutoff frequency is 3.5kHz.

The AD7371 is the receive filter. It is a high order bandpass filter with a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz. The filter function is implemented using a second order low pass continuous time filter, a fourth order high pass switched capacitor filter and a seventh order low pass switched capacitor filter.

AD7341/AD7371—SPECIFICATIONS

TRANSMIT FILTER[1] (V_{DD} = V_{CC} = 5V ± 5%; V_{SS} = −5V ± 5%; AGND = DGND = 0V; CLKIN = 288kHz (M/S Ratio = 40/60 to 60/40. T_A = +25°C. Attenuator set at 0dB, unless otherwise stated.)

Parameter	AD7341JN AD7341JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	100	MΩ typ	
FILTER CHARACTERISTICS[2, 3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	0≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on Programmable Attenuator
Signal-to-Noise Ratio	72	dB min	0≤f≤3.5kHz
	75	dB typ	SNR Includes Noise and Harmonics
	70	dB typ	Attenuator Set at −30dB, 0≤f≤3.5kHz
Stopband Rejection	70	dB min	f≥6.1kHz
Differential Group Delay	350	μs typ	0≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	R_L = 3kΩ, C_L = 100pF
Offset Voltage	±70	mV max	
Attenuation Range	0 to −38	dB	Determined by DB2–DB7, See Table III
Relative Accuracy[3, 4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS $\overline{WR}$, DB2–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1\times5\times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	μs	
V_{OH}, Output High Voltage	2.4	V min	I_{SOURCE} = 400μA
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6mA
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
I_{DD} + I_{CC}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES

[1]Operating temperature ranges as follows: J versions: 0 to +70°C.

[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.

[3]Measured using a ±3V, 1kHz sine wave.

[4]Measured over the full attenuation range.

[5]Required to derive internal frequency of 288kHz from CLKIN.

[6]Determined by data transmission rate.

Specifications subject to change without notice.

RECEIVE FILTER[1] (V_{DD} = V_{CC} = 5V ± 5%; V_{SS} = −5V ± 5%; AGND = DGND = 0V; CLKIN = 288kHz M/S Ratio = 40/60 to 60/40. T_A = +25°C. PGA set at 0dB, unless otherwise stated.)

Parameter	AD7371JN AD7371JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	10	kΩ typ	
FILTER CHARACTERISTICS[2, 3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Lower Cutoff Frequency	180	Hz	0.1dB Down from the Lowest Point in the Passband
Upper Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	200Hz≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on PGA
Signal-to-Noise Ratio	72	dB min	180Hz≤f≤3.5kHz
	75	dB typ	
	60	dB typ	Input Signal Level of −24dB; PGA Gain Set at +24dB
Stopband Rejection	66	dB min	f≥6.1kHz
	40	dB typ	f≥60kHz
Differential Group Delay	300	µs typ	500Hz≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	R_L = 3kΩ, C_L = 100pF
Offset Voltage	±70	mV max	
Gain Range	0 to +24	dB	Determined by DB0–DB7, see Table VI
Relative Accuracy[3, 4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS			
$\overline{WR}$, DB0–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1\times5\times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	µs	
V_{OH}, Output High Voltage	2.4	V min	I_{SOURCE} = 400µA
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6mA
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
I_{DD} + I_{CC}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES
[1]Operating temperature ranges as follows: J versions: 0 to +70°C.
[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.
[3]Measured using a ±3V, 1kHz sine wave.
[4]Measured over the full attenuation range.
[5]Required to derive a switched capacitor filter frequency of 288kHz from CLKIN.
[6]Determined by data transmission rate.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

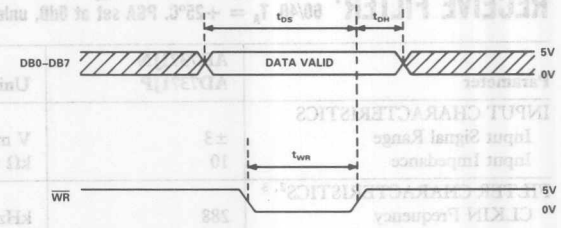
($V_{DD} = V_{CC} = +5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$)

Parameter	Limit at T_A = +25°C	Units	Comments
t_{WR}	80	ns min	Write Pulse Width
t_{DS}	60	ns min	Data Setup Time
t_{DH}	20	ns min	Data Hold Time
t_{SYNCIN}	80	ns min	SYNCIN Pulse Width

NOTE

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of +5V. tr = tf = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$.

Figure 1. AD7341/AD7371 Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND ..... −0.3V to +7V
V_{CC} to DGND ..... −0.3V to +7V
V_{DD} to V_{CC} ..... −0.6V to +0.6V
V_{SS} to DGND ..... +0.3V to −7V
AGND to DGND ..... −0.3V to V_{CC}
RXIN, TXIN to AGND ..... V_{SS} −0.3V to V_{DD} + 0.3V
RXOUT, TXOUT to AGND[1] ... V_{SS} −0.3V to V_{DD} + 0.3V
Digital Input Voltage to DGND ..... −0.3V to V_{CC} + 0.3V
Power Dissipation (Any Package) to +75°C 1000mW
Operating Temperature Range
J Versions ..... 0 to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10secs) ..... +300°C

NOTE

[1]RXOUT, TXOUT may be shorted to AGND, DGND, V_{DD}, V_{CC}, V_{SS} provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one absolute maximum rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

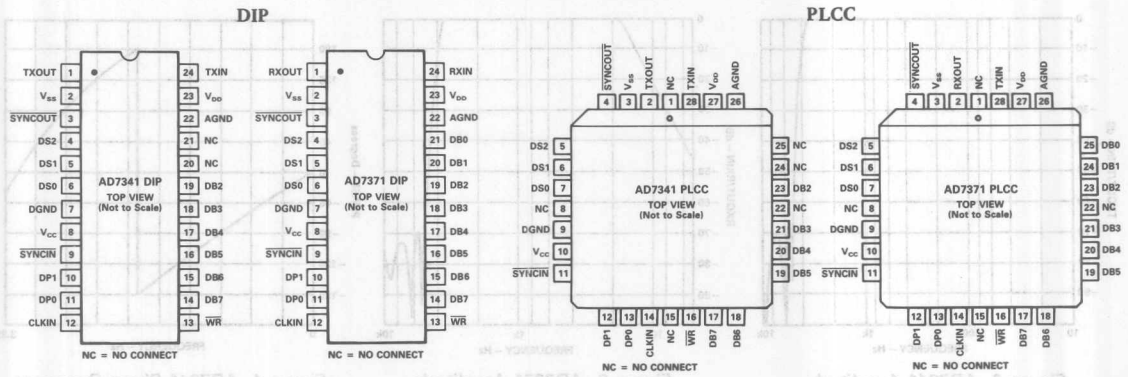


ORDERING GUIDE

Model	Function	Temperature Range	Package Option*
AD7341JN	Transmit Filter	0°C to +70°C	N-24
AD7341JP	Transmit Filter	0°C to +70°C	P-28A
AD7371JN	Receive Filter	0°C to +70°C	N-24
AD7371JP	Receive Filter	0°C to +70°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN CONFIGURATIONS



4

TERMINOLOGY

Cutoff Frequency

The filter cutoff frequency is the point in the response where the amplitude begins to fall off. For the AD7341 and AD7371 it is defined as 0.1dB down from the lowest point in the passband. The AD7341 low pass filter has one cut off frequency at 3.5kHz while the AD7371 band pass filter has a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the filter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (including harmonics) up to 3.5kHz.

Second Harmonic

Second harmonic is the ratio of the second harmonic amplitude to the fundamental amplitude, expressed in dBs.

Third and Higher Harmonics

This is the amplitude ratio of the rms sum of the third and higher harmonics to the fundamental, expressed in dBs. Total harmonic distortion (THD) is the rms sum of the second harmonic and the third and higher harmonics.

Passband Ripple

This is the ripple in the passband section of the frequency response and is expressed in dBs. For the AD7341, it is measured in the band 0 to 3.3kHz, and for the AD7371 it is measured in the band 200Hz to 3.3kHz.

Passband Gain Error

Passband gain error is the deviation of the actual passband level from the ideal passband level. For the AD7341, it is measured with the attenuation set to 0dB (DB2–DB7 = 1); for the AD7371, it is measured with the gain set to 0dB (DB0–DB7 = 1).

Stopband Rejection

This is the magnitude of the stopband response relative to the passband magnitude. The stopband is specified for frequencies greater than 6.1kHz.

Differential Group Delay

Absolute group delay is the rate of change of phase versus frequency, d0/df. For the AD7341 and AD7371, differential group delay is the absolute group delay in a specified band relative to the absolute group delay at 1kHz. The specified band for the AD7341 is 0 to 3.3kHz and for the AD7371 it is 500Hz to 3.3kHz.

Offset Voltage

This is the amount of offset introduced into the input signal by the filter. For the AD7341 it is measured with the attenuation set at 0dB, and for the AD7371 it is measured with the gain set at 0dB.

Attenuation Range

For the AD7341, this is the amount by which the output can be attenuated, using the digital inputs DB7–DB2. Table I gives a selection of attenuations for various values of digital input.

Gain Range

For the AD7371, this is the amount by which the input can be amplified, using the digital inputs DB7–DB0. Table VI gives gain versus digital input code.

Relative Accuracy

This is a measure of the accuracy with which either the AD7341 attenuation or the AD7371 gain can be programmed, having allowed for the passband gain error. It is expressed in dBs relative to attenuation or gain setting with a digital input code of all 1s.

TYPICAL PERFORMANCE CURVES ($V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $f_{CLKIN} = 288kHz$, $T_A = +25°C$ unless otherwise stated)

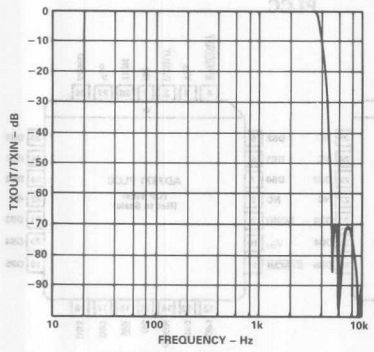


Figure 2. AD7341 Amplitude Response

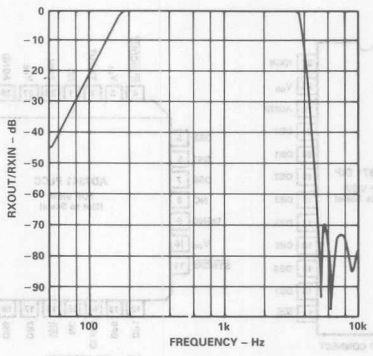


Figure 3. AD7371 Amplitude Response

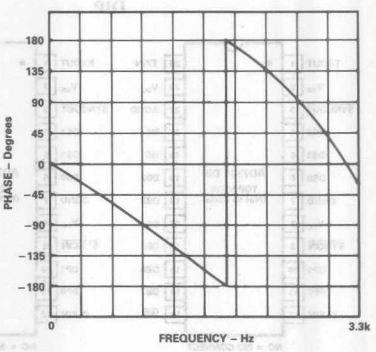


Figure 4. AD7341 Phase Response

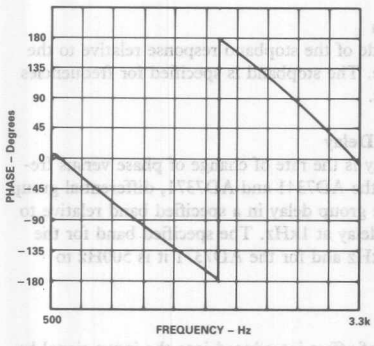


Figure 5. AD7371 Phase Response

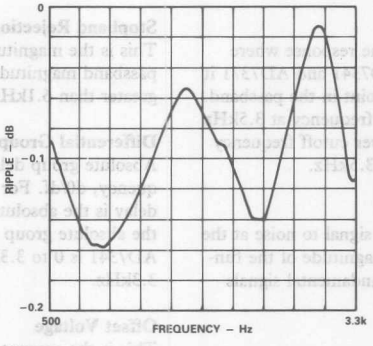


Figure 6. Passband Ripple in the AD7341/AD7371

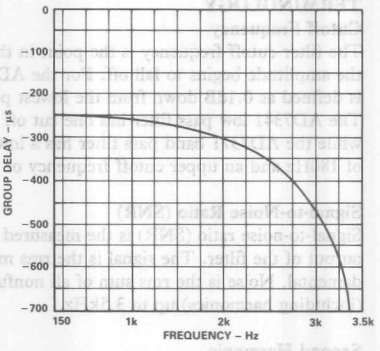


Figure 7. AD7341 Group Delay

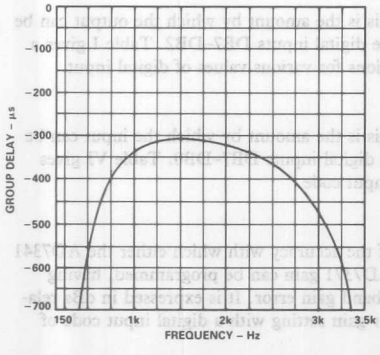


Figure 8. AD7371 Group Delay

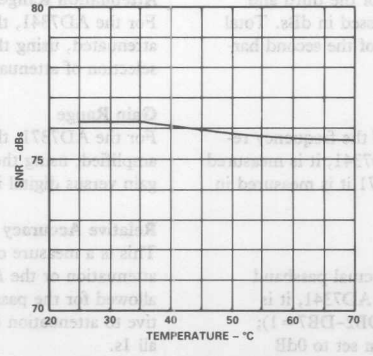


Figure 9. AD7341 SNR vs. Temperature

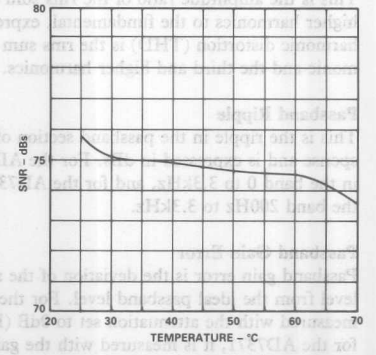


Figure 10. AD7371 SNR vs. Temperature

AD7341 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	TXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{SYNCOUT}$	This output pulse is derived from the SCF (Switched Capacitor Filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table II). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table I shows the typical $\overline{SYNCOUT}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.
4	DS2	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
5	DS1	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
6	DS0	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{SYNCIN}$	This asynchronous digital input resets the internal clock circuitry from which $\overline{SYNCOUT}$ is derived. This allows $\overline{SYNCOUT}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{WR}$	Active low digital input. Data for the on chip programmable attenuation is loaded to the input latch when this signal goes low and is latched when it goes high.
14–19	DB7–DB2	Six-bit data bus which sets the attenuation level on the output. See Table III.
20	NC	No connect.
21	NC	No connect.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	TXIN	Filter input.

Table I. Setting $\overline{SYNCOUT}$ Frequency Using DS2, DS1, DS0

DS2	DS1	DS0	$\overline{SYNCOUT}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table II. Setting CLKIN Divide Ratio Using DP1, DP0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table III. Output Attenuation vs. Digital Input Code

DB7	DB6	DB5	DB4	DB3	DB2	Attenuation dB
1	1	1	1	1	1	0
0	1	1	1	1	1	−6
0	0	1	1	1	1	−12
0	0	0	1	1	1	−18
0	0	0	0	1	1	−24
0	0	0	0	0	1	−30
0	0	0	0	0	0	−38

AD7371 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	RXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{\text{SYNCOUT}}$	This output pulse is derived from the SCF (switched capacitor filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table V). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table IV shows the typical $\overline{\text{SYNCOUT}}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.
4	DS2	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
5	DS1	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
6	DS0	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{\text{SYNCIN}}$	This digital input resets the internal clock circuitry from which $\overline{\text{SYNCOUT}}$ is derived. This allows $\overline{\text{SYNCOUT}}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{\text{WR}}$	Active low digital input. Data for the on chip programmable gain is loaded to the input latch when this signal goes low and is latched when it goes high.
14–21	DB7–DB0	Eight-bit data bus which sets the gain level on the input. See Table VI.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	RXIN	Filter input.

Table IV. Setting $\overline{\text{SYNCOUT}}$ Frequency Using DS2, DS1, DS0

DS2	DS1	DS0	$\overline{\text{SYNCOUT}}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table V. Setting CLKIN Divide Ratio Using DP1, DP0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table VI. Input Gain vs. Digital Input Code

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Gain dB
0	0	0	0	0	0	0	0	24
0	0	0	0	0	1	1	1	21
0	0	0	1	0	0	0	1	18
0	0	0	1	1	1	1	1	15
0	0	1	1	0	0	1	1	12
0	1	0	1	0	0	0	0	9
0	1	1	1	1	0	0	0	6
1	0	1	1	0	0	0	0	3
1	1	1	1	1	1	1	1	0

AD7341 Filter

The AD7341 transmit filter performs the reconstruction or smoothing function for the transmit channel D/A converter. Figure 11 is the block diagram for the filter and programmable attenuation section.

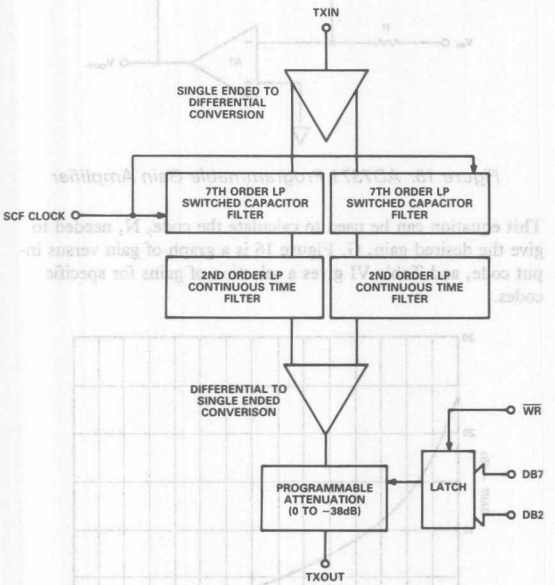


Figure 11. AD7341 Filter Section

The transmit channel signal is applied at TXIN and is converted to a differential signal. It then goes to the fully differential switched capacitor low pass section. This is a seventh order elliptical filter which gives a 3.5kHz cut off frequency and stopband attenuation of greater than 70dB at frequencies above 6.1kHz. The use of the differential filter structure ensures an excellent harmonic distortion figure and also gives improved rejection of common mode noise such as clock feedthrough in the switched capacitor switching transistors. The filter cut off frequency depends directly on the clock driving the switched capacitor section and upon the capacitor matching. Capacitor matching is typically better than 2% and this means that if the clock is constant, cut off frequency variation from device to device will be less than 2%. Since the switched capacitor filters are sampled data systems (analog data) with a sampling frequency of 57.6kHz, they must be followed by a smoothing filter to remove aliased components due to this clock. This smoothing filter is a second order low pass continuous time section. The differential single ended signal. The level of SCF clock feedthrough at the output is typically −65dB. This can be further reduced by using a simple RC combination at the output (39kΩ and 1000pF reduce the feedthrough to −80dB). The second order filter shown in Figure 22 reduces it to below −90dB. After recombination of the differential signals, a programmable attenuation stage follows. The attenuator circuit diagram is shown in Figure 12. It consists of an 8-bit multiplying DAC with the two LSBs (DB1, DB0) tied high. The transfer function is given by:

$$A = 20 \log \frac{256}{4N+3}$$

where A is the attenuation in dBs and N is the 6-bit binary code loaded to the device. Expressing N in terms of A gives:

$$N = \frac{1}{4}\left[\frac{256}{10^{A/20}} - 3\right]$$

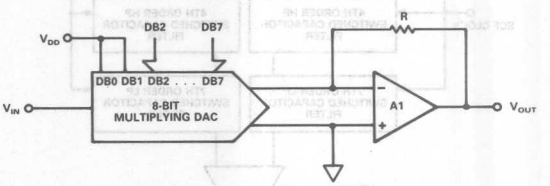


Figure 12. AD7341 Output Attenuator

This allows the calculation of the device input code for a given output attenuation. The attenuation range is 0 to 38dB and allows the user to adapt the output signal for different line specifications. Figure 13 shows how attenuation varies with input code, and Table III gives a selection of attenuations for specific codes.

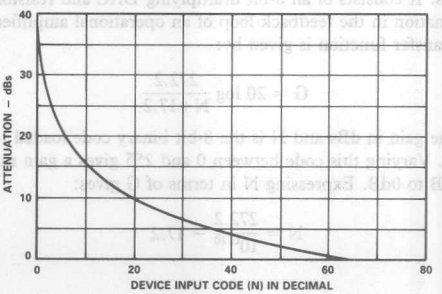


Figure 13. Programmable Attenuation vs. Input Code for the AD7341

AD7371 Filter

The receive filter performs the antialiasing function for the receive channel A/D converter. It provides rejection of high frequency out-of-band signals, attenuation of low frequency noise at both 50Hz and 60Hz line frequencies and programmable gain for the input signal. Figure 14 is the block diagram for the filter and programmable gain section.

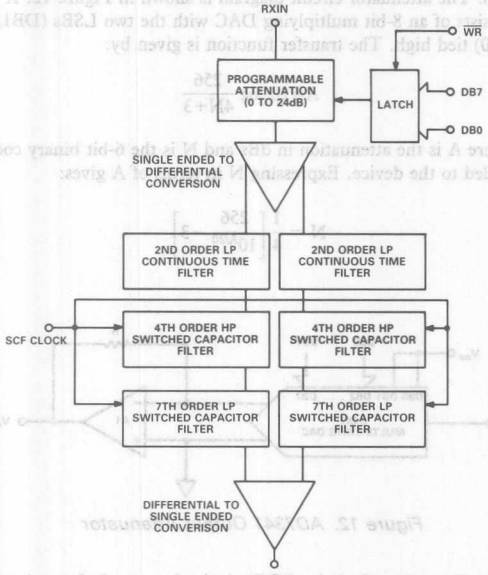


Figure 14. AD7371 Filter Section

The input signal is applied at RXIN and passes through the programmable gain stage. Figure 15 shows the circuit diagram for this. It consists of an 8-bit multiplying DAC and resistor combination in the feedback loop of an operational amplifier. The transfer function is given by:

$$G = 20 \log \frac{272.2}{N+17.2}$$

G is the gain in dBs and N is the 8-bit binary code loaded to the device. Varying this code between 0 and 255 gives a gain range of 24dB to 0dB. Expressing N in terms of G gives:

$$N = \frac{272.2}{10^{G/20}} - 17.2$$

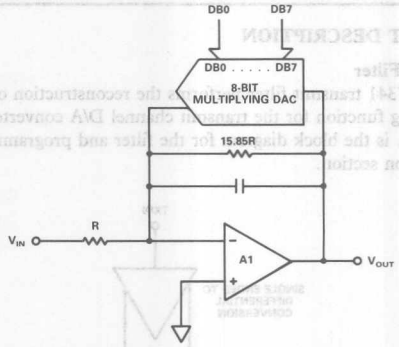


Figure 15. AD7371 Programmable Gain Amplifier

This equation can be used to calculate the code, N, needed to give the desired gain, G. Figure 16 is a graph of gain versus input code, and Table VI gives a selection of gains for specific codes.

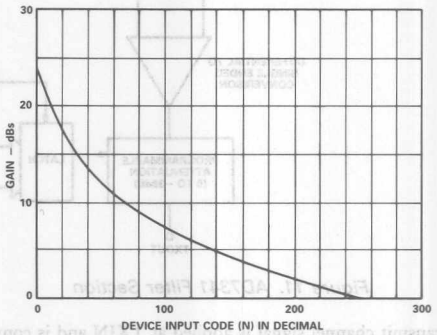


Figure 16. Programmable Gain vs. Input Code for the AD7371

After the PGA stage, the receive signal is converted to a fully differential signal before going to the differential filters. The first differential filter is a second order continuous time section. This is necessary to provide antialiasing for the sampling switched capacitor filter. The continuous time filter eliminates any high frequency components from the input signal which would be aliased back into the passband of the switched capacitor filter and appear as noise. Following the continuous time filter, the fourth order elliptical high pass switched capacitor section has a cutoff frequency of 180Hz, and the seventh order elliptical low pass switched capacitor section has a cutoff frequency of 3.5kHz. As in the reconstruction filter, the cutoff frequency variation from device to device for fixed CLKIN is typically less than 2%. On recombination of the differential signals, the output goes to RXOUT.

SCF Clock and System Synchronization

The clock generation circuitry for both the AD7341 and the AD7371 is identical and is shown in Figure 17. For the specified filter response, the switched capacitor clock must be 57.6kHz. This means that CLKX in Figure 17 must always be 288kHz (57.6kHz×5). The input programmable divider allows the user the option of four CLKIN frequencies (288kHz, 576kHz, 864kHz or 1152kHz). The input divider can then be programmed to ensure that CLKX is 288kHz.

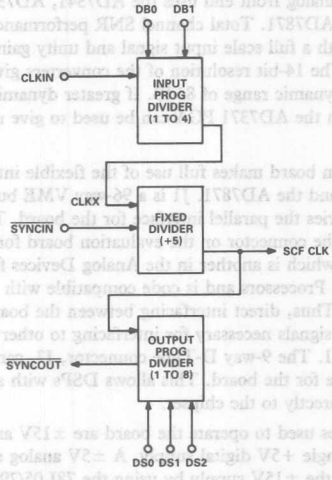


Figure 17. AD7341/AD7371 Clock Generation Circuitry

The AD7341 and the AD7371 are always used with a DAC and ADC respectively. The DAC and ADC update and sample at a certain rate (9.6kHz or 7.2kHz, for example). The filters sample at 57.6kHz. In order to ensure that there is no low frequency aliasing, the DAC/ADC rate must be synchronized with the SCF clock. This means the SCF rate must be an integral multiple of the DAC/ADC rate. The AD7341/AD7371 actually generates this required synchronized clock on chip. The output programmable divider allows division of the SCF clock by 1 to 8. The divide ratio is determined by inputs DS0–DS2. The output of the programmable divider goes to $\overline{\text{SYNCOUT}}$ which is then used to drive either the $\overline{\text{CONVST}}$ input of an ADC or the $\overline{\text{LDAC}}$ input of a DAC. The output programmable divider also has a reset input ($\overline{\text{SYNCIN}}$). This is normally tied high. When it is brought low, the counter is reset. On returning high, the counter is reactivated. By using this $\overline{\text{SYNCIN}}$ facility, it is possible to adjust the point in time at which sampling occurs while maintaining the same rate. This is useful in modem applications and is known as cycle slipping. Figure 18 shows the complete timing waveforms for the AD7341/AD7371.

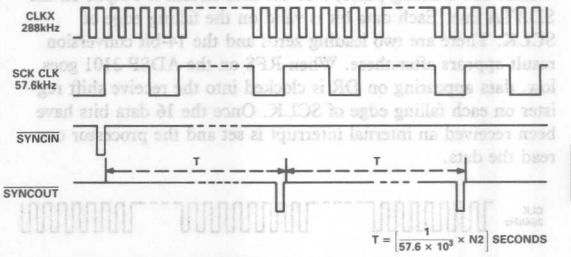


Figure 18. AD7341/AD7371 Timing Waveforms

APPLYING THE AD7341/7371

The prime application for the AD7341/7371 is in the analog front end for echo-cancelling modems. Here, the filters are combined with a high resolution DAC and ADC to provide the interface between the analog and the digital domain. The excellent noise performance of the AD7371 and the high resolution of the AD7871 (14-bit ADC) combine to allow the modem echo-cancelling loop to be implemented totally in the digital domain. This overcomes the disadvantage with lower resolution systems which need to do a digital approximation of the echo and reconstruct in analog form for an analog echo-cancelling loop.

Conversely, in the modem transmitter, the combination of AD7341 and high resolution DAC (14-bit AD7840) allows transmission of the signal with minimum impairments to the line.

Figure 19 shows a typical hardware interface between the analog front end chipset and the ADSP-2101 in an echo-cancelling modem. The ADSP-2101 is the new DSP microcomputer from Analog Devices. It has program memory and data memory on chip

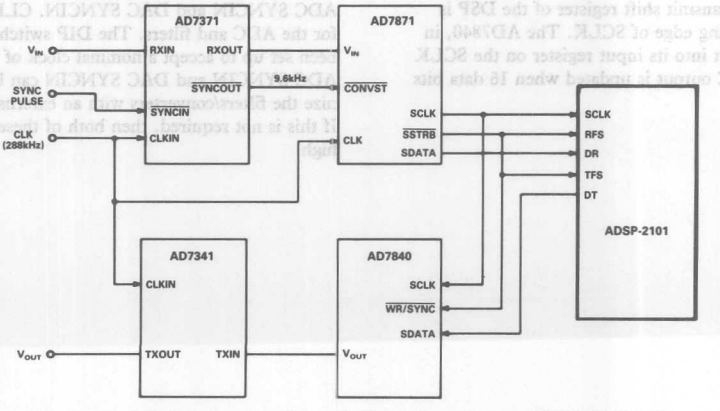


Figure 19. Modem Analog Front End and Interface to ADSP-2101 DSP

and is code compatible with the ADSP-2100. It also has two serial ports. The particular configuration, shown in Figure 19, uses the serial interface on both the AD7840 and AD7871 to talk to one of the ADSP-2101 serial ports. The system timing diagram is shown on Figure 20. The 288kHz clock drives the two filters and the ADC. The $\overline{\text{SYNCIN}}$ pulse may be used to set the absolute sampling instant. DS0, DS1 and DS2 on the AD7371 are programmed to give a 9.6kHz $\overline{\text{SYNCOUT}}$ signal. This drives the AD7871 $\overline{\text{CONVST}}$ input and is thus the sampling rate. SCLK on the AD7871 clocks out serial data on its rising edge. $\overline{\text{SSTRB}}$ is the framing pulse for the serial data. Within this framing pulse, a 16-bit data stream is output on the SDATA line. Each data bit is valid on the falling edge of SCLK. There are two leading zeros and the 14-bit conversion result appears after these. When RFS on the ADSP-2101 goes low, data appearing on DR is clocked into the receive shift register on each falling edge of SCLK. Once the 16 data bits have been received an internal interrupt is set and the processor can read the data.

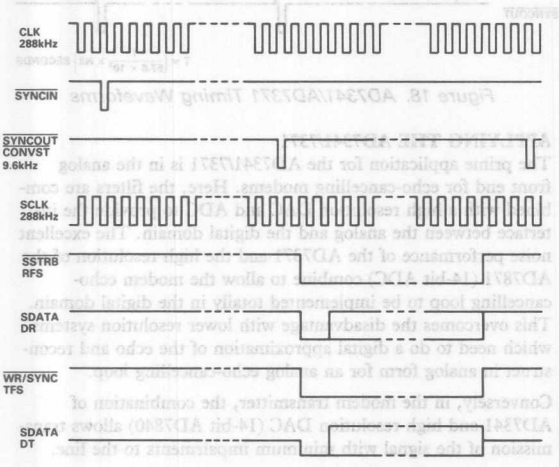


Figure 20. System Timing for Figure 19

The circuit of Figure 19 also uses the $\overline{\text{SSTRB}}$ signal to frame the transmit data from the DSP . Thus, when $\overline{\text{SSTRB}}$ goes low, data contained in the transmit shift register of the DSP is clocked out on each rising edge of SCLK. The AD7840, in turn, loads each data bit into its input register on the SCLK falling edges. The DAC output is updated when 16 data bits have been received.

Using the ADSP-2101 and the chipset, the modem hardware is simplified. The number of lines required to connect the chips is much less than a parallel interface structure would need and no external glue logic is required.

CHIPSET LAYOUT

Figure 23 is the circuit diagram for a modem analog front end based on the Analog Devices chip set. The component overlay is given in Figure 21, while the PCB layout is given in Figures 24 and 25.

The modem analog front end uses the AD7341, AD7371, AD7840 and AD7871. Total channel SNR performance is better than 72dB with a full scale input signal and unity gain on the filter chips. The 14-bit resolution of the converters gives an instantaneous dynamic range of 84dB. If greater dynamic range is required, then the AD7371 PGA can be used to give up to 24dB extra.

The evaluation board makes full use of the flexible interfaces on the AD7840 and the AD7871. J1 is a 96-way VME bus connector which carries the parallel interface for the board. This plugs directly into the connector on the evaluation board for the ADSP-2100, which is another in the Analog Devices family of Digital Signal Processors and is code compatible with the ADSP-2101. Thus, direct interfacing between the boards is possible. All the signals necessary for interfacing to other DSPs are available on J1. The 9-way D-Type connector, J2, carries the serial interface for the board. This allows DSPs with serial ports to interface directly to the chipset.

Power supplies used to operate the board are ±15V analog supplies and a single +5V digital supply. A ±5V analog supply is derived from the ±15V supply by using the 78L05/79L05 regulators. This supply is used for the AD7341, AD7371, AD7840 and AD7871. The supply grounds are tied together on the board so that there is no need to have them connected back at the supply source.

The analog input and output ranges are both ±10V. The analog input is attenuated by IC1 and associated circuitry to give the required ±3V input range for the filter and ADC. Likewise, the analog output from the reconstruction filter (±3V) is gained up by the output amplifier (IC6) to give a ±10V output. This output amplifier also contains a simple second order filter to further attenuate the switched capacitor clock noise at the output.

There are three digital inputs to the board. These are CLKIN, ADC SYNCIN and DAC SYNCIN. CLKIN provides the clock for the ADC and filters. The DIP switches on the board have been set up to accept a nominal clock of 288kHz for the filters. ADC SYNCIN and DAC SYNCIN can be used to resynchronize the filters/converters with an external synchronizing signal. If this is not required, then both of these inputs should be tied high.

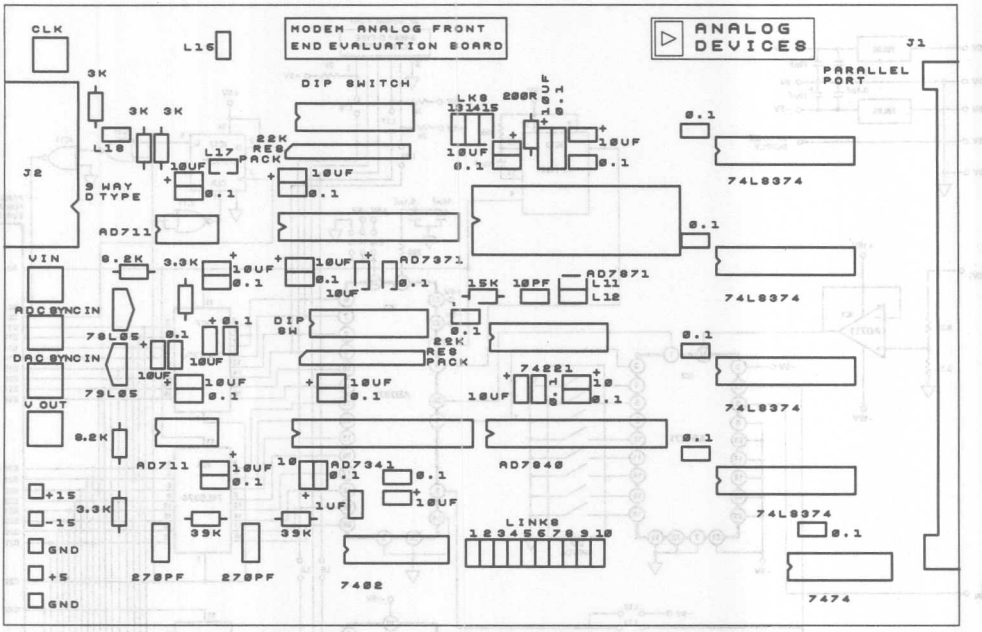


Figure 21. Component Overlay for Circuit of Figure 23

Parallel Interface

If the parallel interface is required, then the four latch chips (IC7 to IC10) should be inserted into the sockets provided. Links L16, L17, L18, L5 and L6 should be omitted. This isolates the serial port from bus activity. Link L15 should be inserted to choose 14-bit parallel operation for the ADC. Omit links L14 and L13. Internal or external clock operation for the ADC may be chosen by L11 and L12. L11 gives external clock operation, while L12 gives internal clock operation. AD7871 conversion is started by $\overline{\text{CONVST}}$ (pin 1) going low. When conversion is complete, $\overline{\text{INT/BUSY}}$ (pin 4) goes low. IC13 extends this pulse. This is then used to read the ADC result into the latches and to interrupt the processor. The processor interrupt service routine then reads the latch contents. Note that the data format is 14 bits with sign extension to 16 bits.

On the AD7840 insert L2 to tie the chip select low and omit L1. Insert L3 to use $\overline{\text{SYNCOUT}}$ of filter to write to the DAC and omit L4. Thus, the processor writes data to the latches and the DAC gets updated on every rising edge of $\overline{\text{WR/SYNC}}$. The data format is 14-bit right justified.

Serial Interface

If the serial interface is required, then omit the four latches (74LS374) and use the serial connector (J2). Links L5, L6, L16, L17 and L18 must be inserted. Omit L15 and insert L14. This places the AD7871 in serial mode of operation with continuously running SCLK. As in the parallel mode, conversion is started by $\overline{\text{CONVST}}$ going low. Serial data appears on Pin 9 (SDATA) as conversion is taking place, and it is latched into the processor shift register on each falling edge of SCLK. The frame synchronization pulse for the data is on Pin 7 ($\overline{\text{SSTRB}}$). The data format is 16-bit with the MSB first. The 16 bits of data are made up of two leading zeros and the 14-bit conversion result. For the DAC in the serial mode omit L3 and insert L4. This provides the necessary inversion of the $\overline{\text{SYNCOUT}}$ pulse from the filter so that it can be used as the frame synchronization for the DAC and the processor. When this goes low data in the processor shift register is clocked out on each rising edge of SCLK and latched into the DAC shift register on each falling edge of SCLK. Since $\overline{\text{LDAC}}$ (Pin 24) is tied permanently low, the DAC register is updated automatically when the 16-bit data stream has been received. The format of this data stream is set up by links L7 to L10. Consult Table I on the AD7840 data sheet for the appropriate settings. Figure 22, below, shows the pin designations for J2.

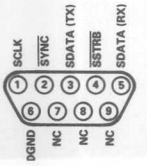
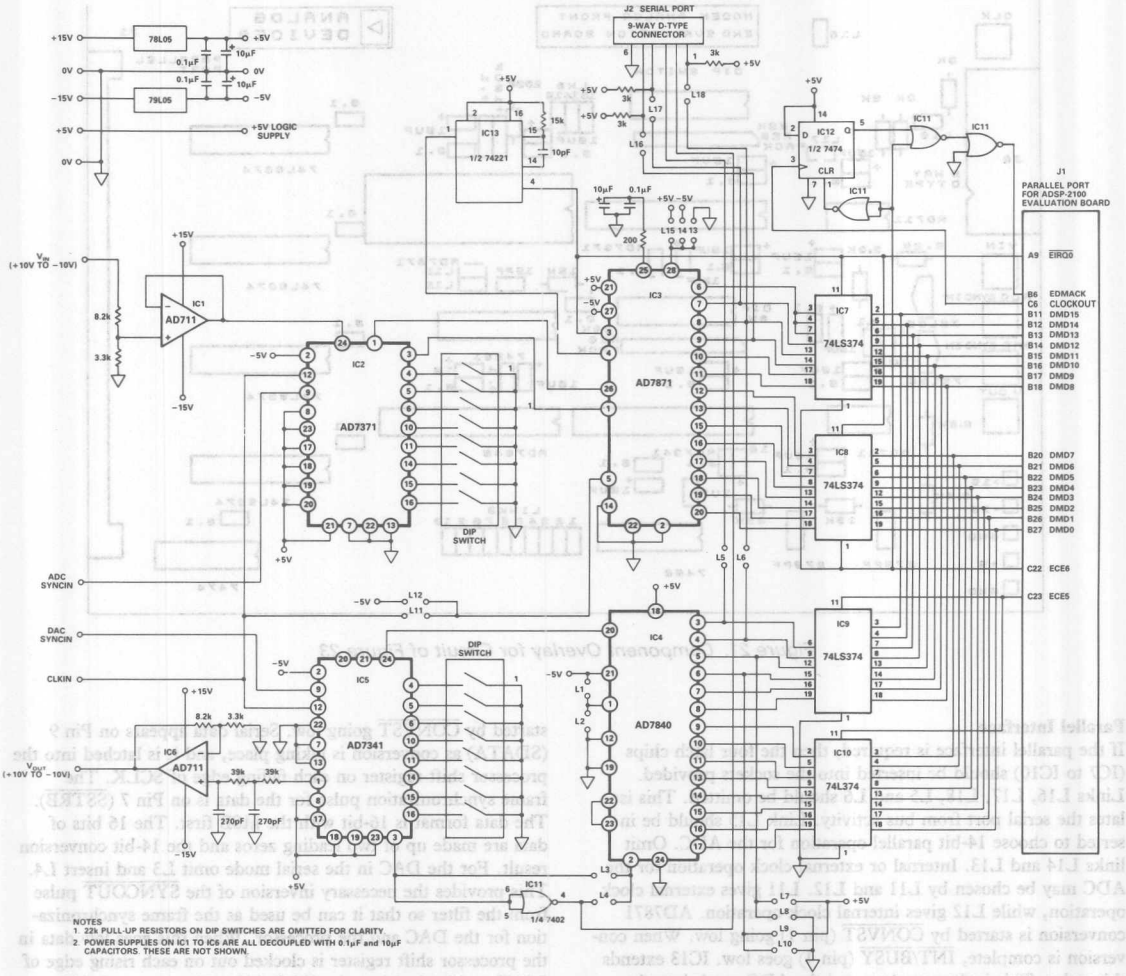


Figure 22. Pin Configuration for J2 (Front View)



NOTES
1. 22k PULL-UP RESISTORS ON DIP SWITCHES ARE OMITTED FOR CLARITY.
2. POWER SUPPLIES ON IC1 TO IC6 ARE ALL DECOUPLED WITH 0.1μF and 10μF CAPACITORS. THESE ARE NOT SHOWN.

Figure 23. Circuit Diagram for Modem Analog Front End

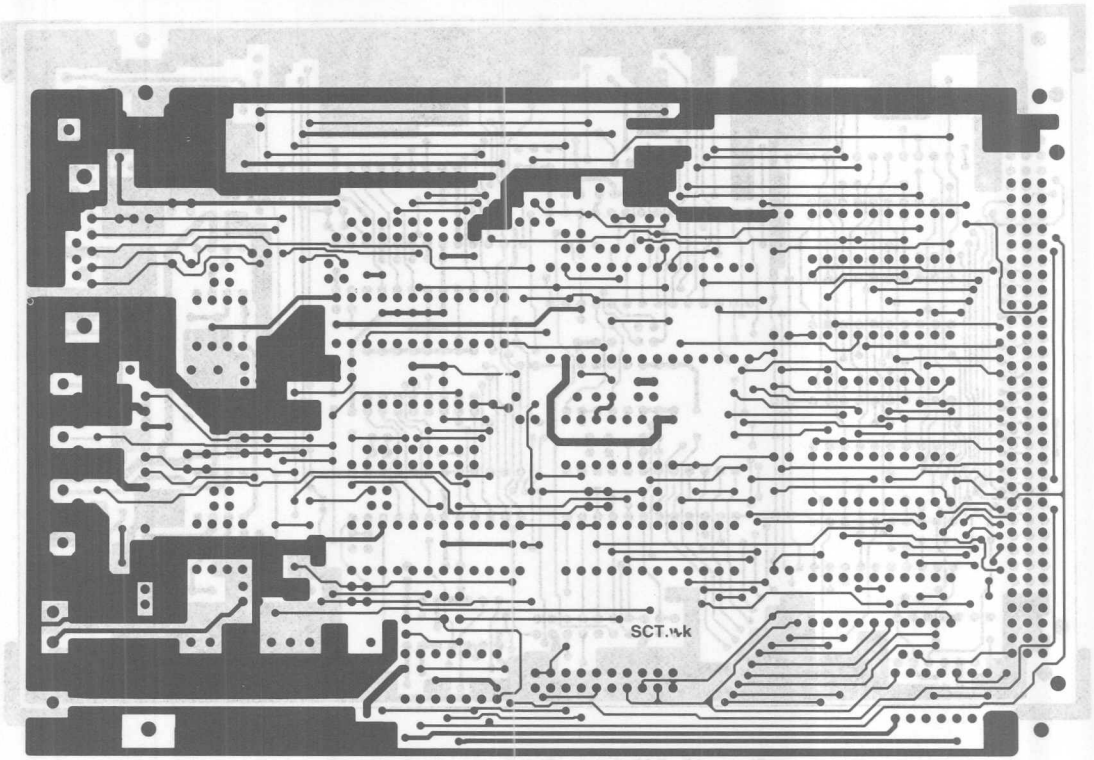


Figure 24. PCB Component Side Layout for Figure 23

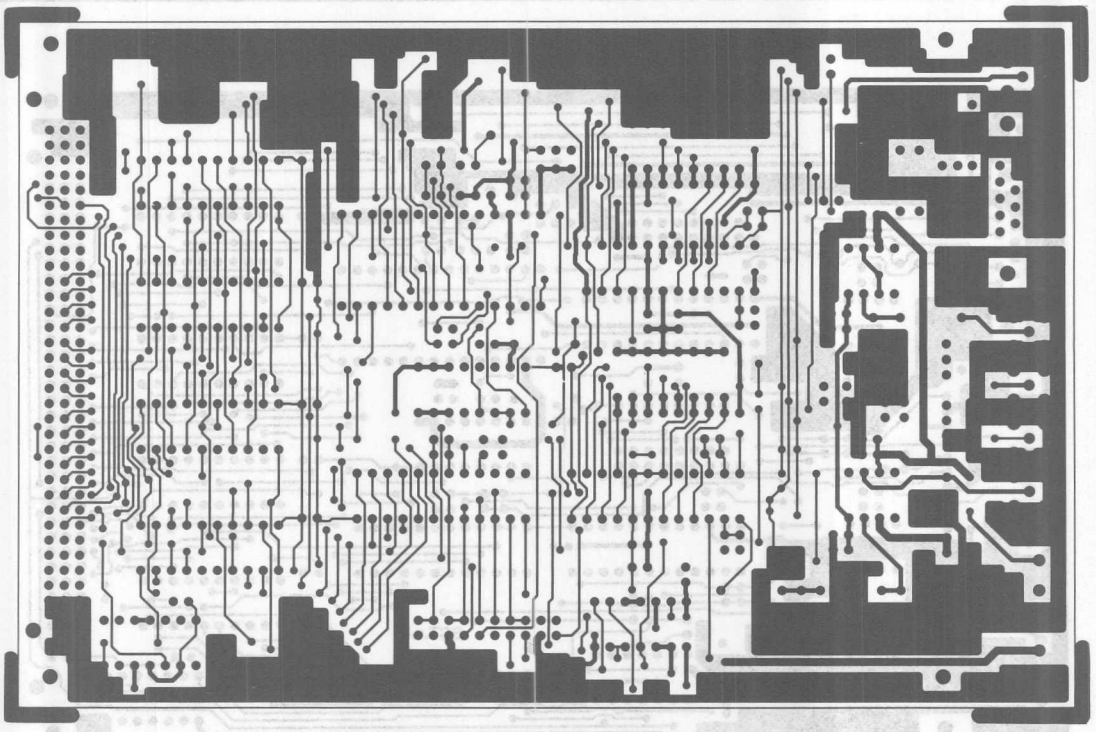


Figure 25. PCB Solder Side Layout for Figure 23

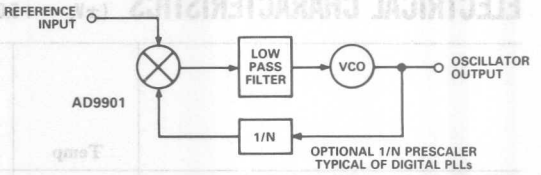
Ultrahigh Speed Phase/Frequency Discriminator

AD9901

FEATURES
- Phase and Frequency Detection
- ECL/TTL/CMOS Compatible
- Linear Transfer Function
- No "Dead Zone"
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- Low Phase Noise Reference Loops
- Fast-Tuning "Agile" IF Loops
- Secure "Hopping" Communications
- Coherent Radar Transmitter/Receiver Chains

PHASE-LOCKED LOOP



4

GENERAL DESCRIPTION

The AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminate phase detection zones common to other digital designs.

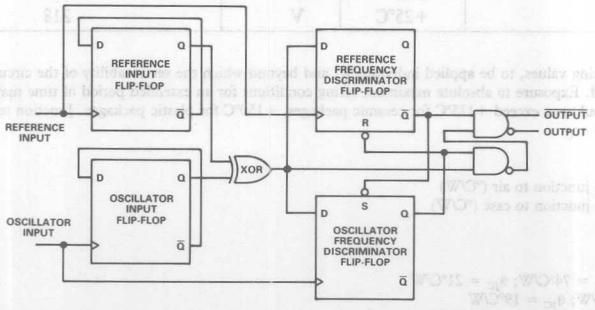
With a single +5V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a −5.2V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase-/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0°C to +70°C, and as a military temperature device, −55°C to +125°C. The commercial versions are packaged in a 14-pin ceramic DIP and a 20-pin PLCC.

The AD9901 Phase/Frequency Discriminator is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9901/883B data sheet for specifications.

FUNCTIONAL BLOCK DIAGRAM



Positive Supply Voltage (+V_S for TTL Operation)	+7V
Negative Supply Voltage (−V_S for ECL Operation)	−7V
Input Voltage Range (TTL Operation)	0V to +5.5V
Differential Input Voltage (ECL Operation)	4.0V
I_{SET} Current	12mA
Output Current	30mA
Operating Temperature Range	
AD9901KQ/KP	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature[2]	
Plastic	+150°C
Ceramic	+175°C
Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = +5.0V [for TTL] or −5.2V [for ECL], unless otherwise noted)

	Temp	Test Level	Commercial Temperature 0°C to +70°C AD9901KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
TTL Input Logic "1" Voltage	Full	VI	2.0			V
TTL Input Logic "0" Voltage	Full	VI			0.8	V
TTL Input Logic "1" Current[3]	Full	VI			0.6	mA
TTL Input Logic "0" Current[3]	Full	VI			1.6	mA
ECL Differential Switching Volt.	Full	VI	300			mV
ECL Input Current	Full	VI			20	μA
OUTPUT CHARACTERISTICS						
Peak-to-Peak Output Voltage Swing[4]	Full	VI	1.6	1.8	2.0	V
TTL Output Compliance Range	Full	V		3–7		V
ECL Output Compliance Range	Full	V		±2		V
I_{OUT} Range	Full	V		0.9–11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	V
AC CHARACTERISTICS						
Linear Phase Detection Range[4]						
40kHz	+25°C	V		360		Degrees
30MHz	+25°C	V		320		Degrees
70MHz	+25°C	V		270		Degrees
Functionality @ 70MHz	+25°C	I		Pass/Fail		
POWER SUPPLY CHARACTERISTICS						
TTL Supply Current (+5.0V)[5, 6]	+25°C	I		43.5	54.0	mA
	Full	I		43.5	54.0	mA
ECL Supply Current (−5.2V)[5, 6]	+25°C	I		42.5	52.5	mA
	Full	I		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		218		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Maximum junction temperature should not exceed +175°C for ceramic packages, +150°C for plastic packages. Junction temperature can be calculated by:

$t_J = PD\ (\theta_{JA}) + t_A = PD\ (\theta_{JC}) + t_C$

where:

PD = power dissipation

θ_{JA} = thermal impedance from junction to air (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W

AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W

AD9901 PLCC = θ_{JA} = 88.2°C/W; θ_{JC} = 45.2°C/W

[3]V_L = +0.4V; V_H = +2.4V.

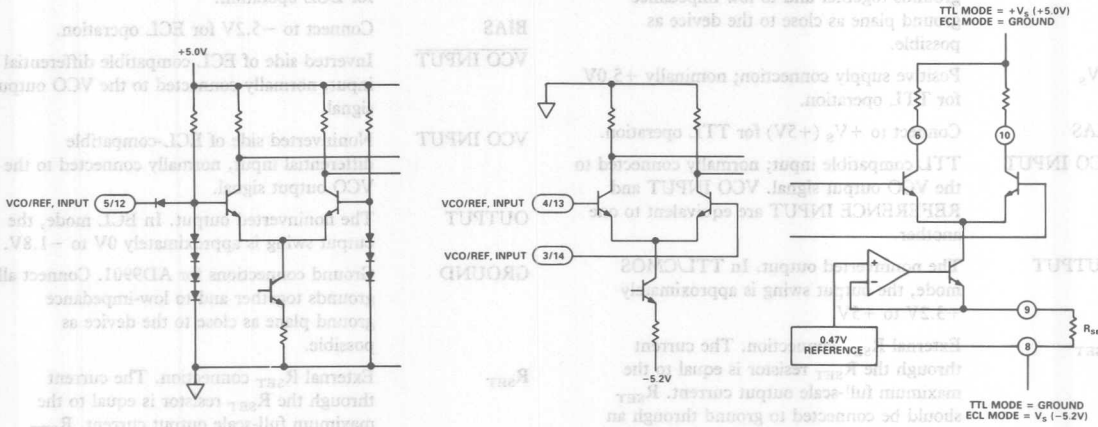
[4]R_{SET} = 47.5Ω; R_L = 182Ω.

[5]Includes load current of 10mA (load resistors = 182Ω).

[6]Supply should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

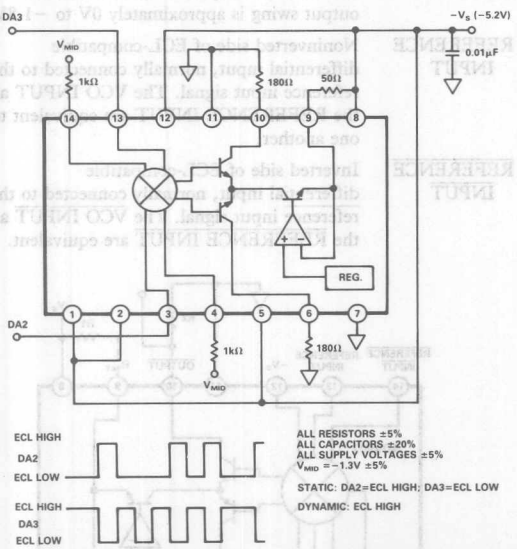
(Based on DIP Pinouts)



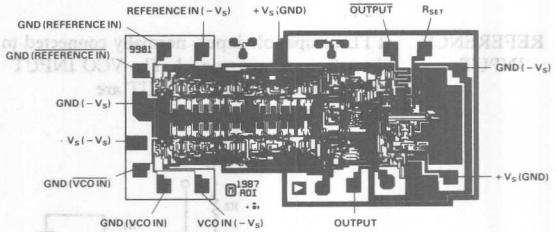
TTL Input *ECL Input* *Output*

AD9901 BURN-IN CIRCUIT

(Based on DIP ECL Pinouts)



DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	63 × 118 × 16(±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding

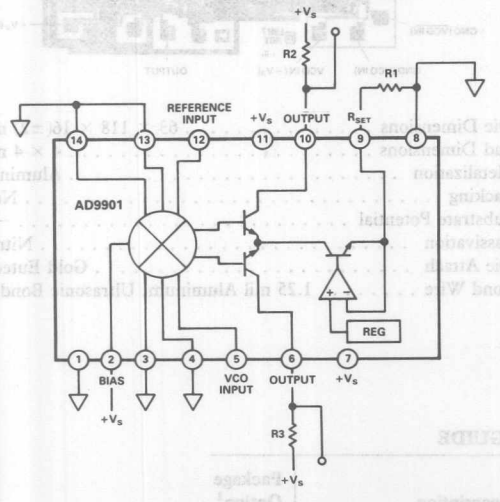
ORDERING GUIDE

Model	Temperature	Description	Package Option[1]
AD9901KQ	0°C to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0°C to +70°C	20-Pin PLCC	P-20A
AD9901TQ/883[2]	−55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD9901TE/883[2]	−55°C to +125°C	20-Contact Ceramic LCC	E-20A

NOTES
[1]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip.
For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

TTL/CMOS MODE FUNCTIONAL PIN DESCRIPTIONS

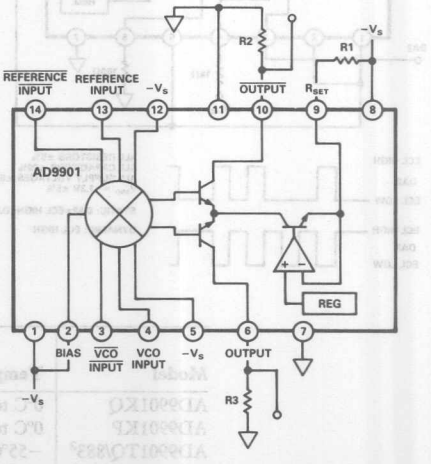
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
$+V_S$	Positive supply connection; nominally +5.0V for TTL operation.
BIAS	Connect to $+V_S$ (+5V) for TTL operation.
VCO INPUT	TTL compatible input; normally connected to the VCO output signal. VCO INPUT and REFERENCE INPUT are equivalent to one another.
OUTPUT	The noninverted output. In TTL/CMOS mode, the output swing is approximately +3.2V to +5V.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to ground through an external resistor in TTL mode. $I_{SET} = 0.47V/R_{SET} = I_{LOAD}$ (max.)
$\overline{\text{OUTPUT}}$	The inverted output. In TTL/CMOS mode, the output swing is approximately +3.2V to +5V.
REFERENCE INPUT	TTL compatible input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent.



TTL Mode
(Based on DIP Pinouts)

ECL MODE FUNCTIONAL PIN DESCRIPTIONS

$-V_S$	Negative supply connection, nominally −5.2V for ECL operation.
BIAS	Connect to −5.2V for ECL operation.
$\overline{\text{VCO INPUT}}$	Inverted side of ECL compatible differential input, normally connected to the VCO output signal.
VCO INPUT	Noninverted side of ECL-compatible differential input, normally connected to the VCO output signal.
OUTPUT	The noninverted output. In ECL mode, the output swing is approximately 0V to −1.8V.
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to $-V_S$ through an external resistor in ECL mode. $I_{SET} = 0.47V/R_{SET} = I_{LOAD}$ (max).
$\overline{\text{OUTPUT}}$	The inverted output. In ECL mode, the output swing is approximately 0V to −1.8V.
REFERENCE INPUT	Noninverted side of ECL-compatible differential input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent to one another.
$\overline{\text{REFERENCE INPUT}}$	Inverted side of ECL-compatible differential input, normally connected to the reference input signal. The $\overline{\text{VCO INPUT}}$ and the $\overline{\text{REFERENCE INPUT}}$ are equivalent.



ECL Mode
(Based on DIP Pinouts)

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

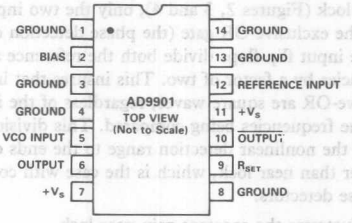
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

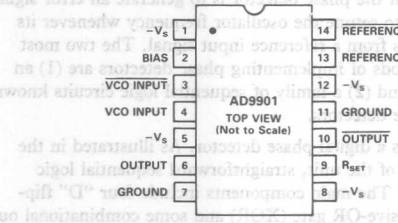
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN CONFIGURATIONS

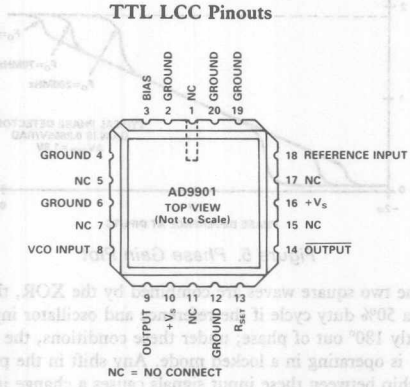
TTL DIP Pinouts



ECL DIP Pinouts

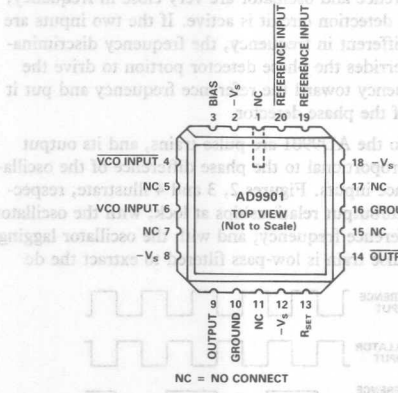


TTL LCC Pinouts



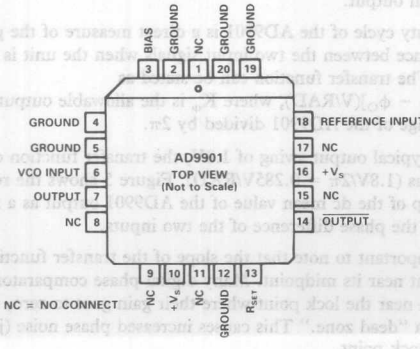
NC = NO CONNECT

ECL LCC Pinouts



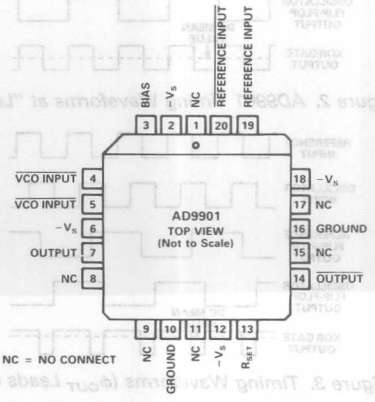
NC = NO CONNECT

TTL PLCC Pinouts



NC = NO CONNECT

ECL PLCC Pinouts



NC = NO CONNECT

THEORY OF OPERATION

A phase detector is one of three basic components of a phase-locked loop (PLL); the other two are a filter and a tunable oscillator. A basic PLL control system is shown in Figure 1.

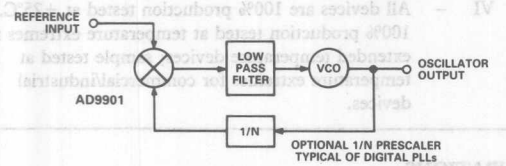


Figure 1. Phase-Locked Loop Control System

The function of the phase detector is to generate an error signal which is used to retune the oscillator frequency whenever its output deviates from a reference input signal. The two most common methods of implementing phase detectors are (1) an analog mixer and (2) a family of sequential logic circuits known as digital phase detectors.

The AD9901 is a digital phase detector. As illustrated in the block diagram of the unit, straightforward sequential logic design is used. The main components include four "D" flip-flops, an exclusive-OR gate (XOR) and some combinational output logic. The circuit operates in two distinct modes: as a linear phase detector and as a frequency discriminator.

When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency and put it within range of the phase detector.

Input signals to the AD9901 are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 2, 3 and 4 illustrate, respectively, the input/output relationships at lock; with the oscillator leading the reference frequency; and with the oscillator lagging. This output pulse train is low-pass filtered to extract the dc

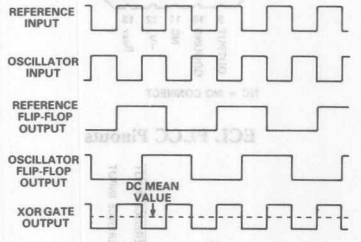


Figure 2. AD9901 Timing Waveforms at "Lock"

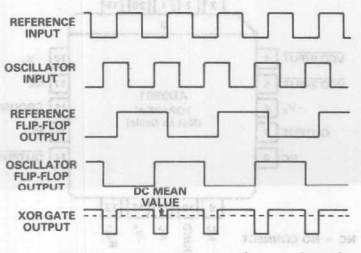


Figure 3. Timing Waveforms (ϕ_{OUT} Leads ϕ_{IN})

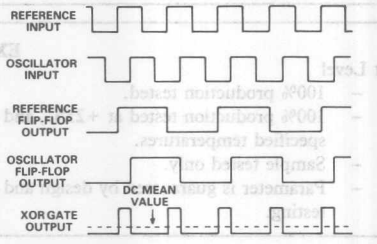


Figure 4. Timing Waveforms (ϕ_{OUT} Lags ϕ_{IN})

mean value $[K_\phi (\phi_I - \phi_O)]$ where K_ϕ is a proportionality constant (phase gain).

At or near lock (Figures 2, 3 and 4), only the two input flip-flops and the exclusive-OR gate (the phase detection circuit) are active. The input flip-flops divide both the reference and oscillator frequencies by a factor of two. This insures that inputs to the exclusive-OR are square waves, regardless of the input duty cycles of the frequencies being compared. This division-by-two also moves the nonlinear detection range to the ends of the range rather than near lock, which is the case with conventional digital phase detectors.

Figure 5 illustrates the constant gain near lock.

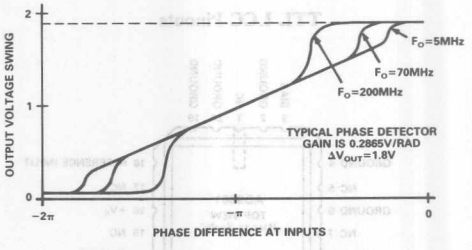


Figure 5. Phase Gain Plot

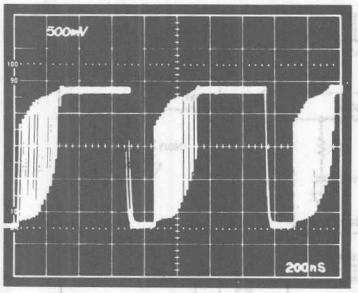
When the two square waves are combined by the XOR, the output has a 50% duty cycle if the reference and oscillator inputs are exactly 180° out of phase; under these conditions, the AD9901 is operating in a locked mode. Any shift in the phase relationship between these input signals causes a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

The duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals when the unit is near lock. The transfer function can be stated as $[K_\phi(\phi_I - \phi_O]$(V/RAD), where K_ϕ is the allowable output voltage range of the AD9901 divided by 2π.

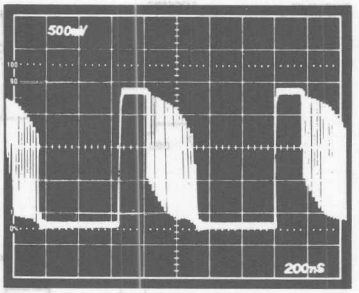
For a typical output swing of 1.8V, the transfer function can be stated as ($1.8V/2\pi = 0.285V/RAD$). Figure 5 shows the relationship of the dc mean value of the AD9901 output as a function of the phase difference of the two inputs.

It is important to note that the slope of the transfer function is constant near its midpoint. Many digital phase comparators have an area near the lock point where their gain goes to zero, resulting in a "dead zone." This causes increased phase noise (jitter) at the lock point.

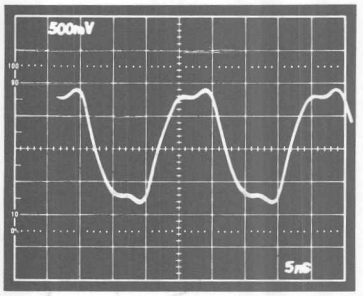
The AD9901 avoids this dead zone by shifting it to the endpoints of the transfer curve, as indicated in Figure 5. The



Photograph 1. AD9901 Output Waveform($F_O << F_1$)



Photograph 2. AD9901 Output Waveform ($F_O >> F_1$)



Photograph 3. AD9901 Output Waveform ($F_O=F_I$= 50MHz)

increased gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise, which is far more dependent upon lock region characteristics.

It should be noted, however, that as frequency increases, the linear range is decreased. At the ends of the detection range, the reference and oscillator inputs approach phase alignment. At this point, slew rate limiting in the detector effectively increases phase gain. This decreases the linear detection by nominally 3.6ns. Therefore, the typical detection range can be found by calculating $[(1/F - 3.6ns)/(1/F)] \times 360°$. As an example, at 200MHz the linear phase detection range is ±50°.

Away from lock, the AD9901 becomes a frequency discriminator. Any time either the reference or oscillator input occurs twice before the other, the Frequency High or Frequency Low flip-flop is clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Combining the frequency discriminator with the phase detector eliminates locking to a harmonic of the reference.

Photograph 1 shows the effect of the "Frequency Low" flip-flop when the oscillator frequency is much lower than the reference input. The narrow pulses, which result from cycles when two positive reference-input transitions occur before a positive VCO edge, increase the dc mean value. Photograph 2 illustrates the inverse effect when the "Frequency High" flip-flop reacts to a much higher VCO frequency.

Photograph 3 shows the output waveform at lock for 50MHz operation. This output results when the phase difference between reference and oscillator is approximately $-\pi$Rad.

4

AD9901 APPLICATIONS

The figure below illustrates a phase-locked loop (PLL) system utilizing the AD9901. The first step in designing this type of circuit is to characterize the VCO's output frequency as a function of tuning voltage. The transfer function of the oscillator in the diagram is shown in Figure 6.

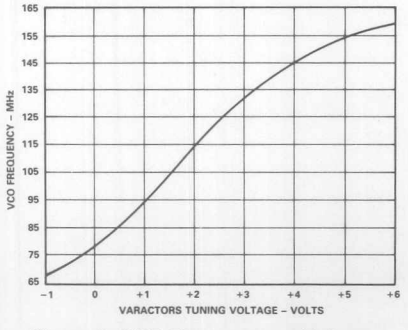


Figure 6. VCO Frequency vs. Voltage

Next, the range of frequencies over which the VCO is to operate is examined to assure that it lies on a linear portion of the transfer curve. In this case, frequencies from 100MHz to 120MHz result from tuning voltages of approximately +1.5V to +2.5V. Because the nominal output swing of the AD9901 is 0 to −1.8V, an inverting amplifier with a gain of 2 follows the loop filter.

As shown in the illustration, a simple passive RC low-pass filter made up of two resistors and a tantalum capacitor eliminates the need for an expensive high speed op amp active-filter design. In this passive-filter second-order-loop system, where n=2, the damping factor is equal to:

$$\delta = 0.5\,[K_O K_d/n(\tau_1 + \tau_2)]^{1/2}\,[\tau_2 + (n/K_O K_d)]$$

and the values for τ_1 and τ_2 are the low-pass filter's time constants R_1C and R_2C. The gain of 2 of the inverting stage, when combined with the phase detector's gain, gives:

$$K_d = 0.572V/RAD$$

With K_O = 115.2 MRAD/s/V, τ_1 equals 1.715s, and τ_2 equals 3.11×10^{-4}s for the required damping factor of 0.7. The illustrated values of 30Ω (R_1), 160Ω (R_2), and 10μF (C) in the diagram approximate these time constants.

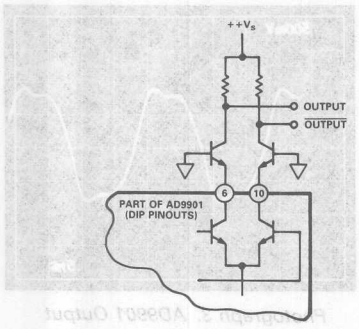
The gain of the RC filter is:

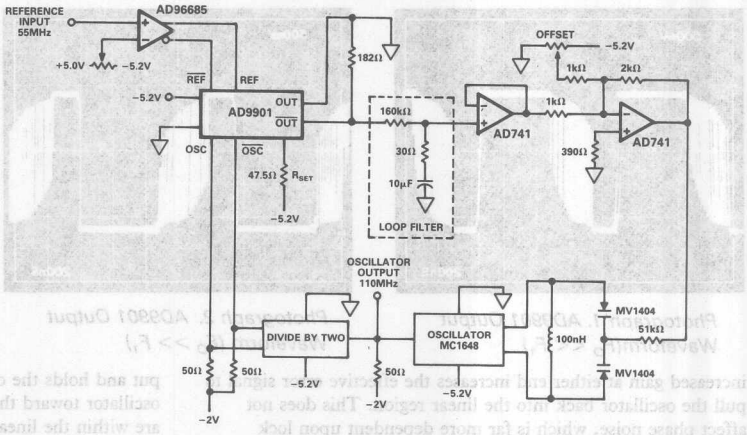
$$V_O/V_I = (1 + sR_2C)/[1 + s(R_1 + R_2)C].$$

Where $K_O K_d >> \omega_n$, the system's natural frequency:

$$\omega_n = [K_O K_d/n(\tau_1 + \tau_2)]^{1/2} = 4.5kHz.$$

For general information about phase-locked loop design, the user is advised to consult the following references: Gardner, *Phase-Lock Techniques* (Wiley); or Best, *Phase Locked Loops* (McGraw-Hill).





Phased Locked Loop Using AD9901

32-Bit, 300 MSPS Phase Accumulator for DDS

AD9950

FEATURES
- 300 MSPS Clock Rate
- 32-Bit Frequency Resolution
- Low Power: 1.5 W
- On-Board Quad Logic
- 16- or 32-Bit Bus Compatible

APPLICATIONS
- Frequency Synthesizers
- Waveform Generators
- Frequency Hopping Systems
- Communications and Radar Receivers

GENERAL DESCRIPTION

The AD9950 is a 32-bit, 300 MSPS phase accumulator for direct digital synthesis (DDS) applications. The twelve most significant bits (MSBs) of the accumulator are provided to address an external phase-to-amplitude conversion table for waveform synthesis.

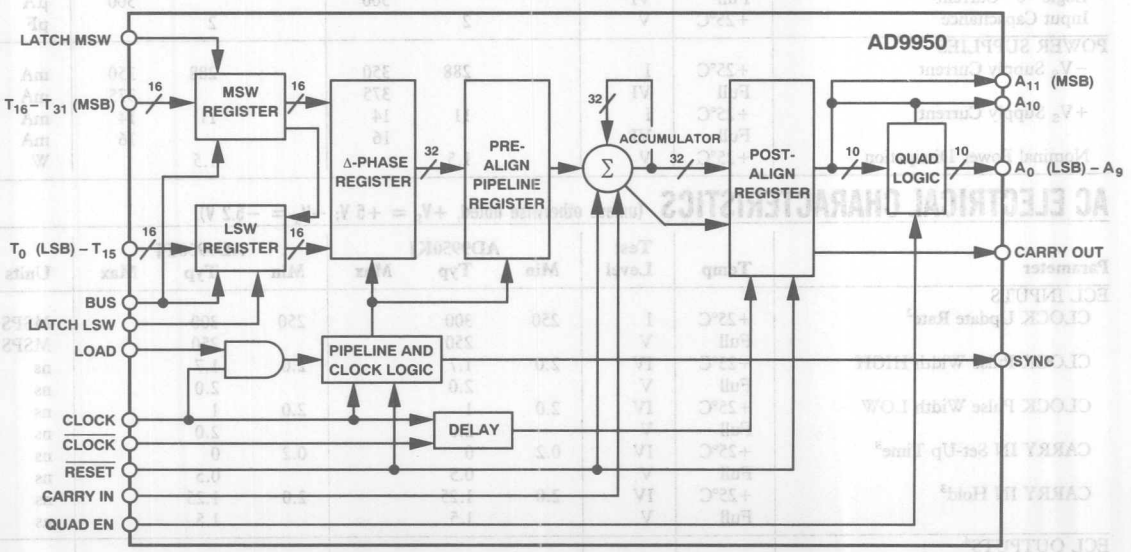
Frequency control signals are TTL compatible, and the internal accumulator can operate at rates up to 300 MSPS because of the high speed bipolar process used in fabricating the device. Output phase data is ECL compatible and can be interfaced with either ROM or RAM. An external look-up table can contain data to generate standard functions such as sines, cosines, etc.

On-board quadrature logic reduces the amount of external memory required to implement the phase-to-amplitude conversions in applications which generate periodic waveforms symmetrical about their 90° phase points.

The AD9950KJ is packaged in a 68-pin J-leaded ceramic chip carrier for a commercial temperature range of 0°C to +70°C; the model AD9950TJ is available for military applications with a temperature range of −55°C to +125°C in the same package. Contact the factory for information on devices meeting the requirements of MIL-STD-883.

4

AD9950 DDS PHASE ACCUMULATOR BLOCK DIAGRAM



Supply Voltage ($\pm V_S$) . . . . . ±7 V
TTL Inputs . . . . . $+V_S$ to −0.5 V
ECL Inputs . . . . . 0 V to $-V_S$
Operating Temperature Range
AD9950KJ . . . . . 0°C to +70°C
AD9950TJ . . . . . −55°C to +125°C
AD9950KJ . . . . . −65°C to +150°C
AD9950TJ . . . . . −65°C to +150°C
Junction Temperature[1]
AD9950KJ . . . . . +175°C
AD9950TJ . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V)

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
ECL INPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
Logic "1" Current	Full	VI			200			200	μA
Logic "0" Current	Full	VI			200			200	μA
Input Capacitance	+25°C	V		2			2		pF
ECL OUTPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
TTL INPUTS									
Logic "1" Voltage	Full	VI	+2			+2			V
Logic "0" Voltage	Full	VI			+0.8			+0.8	V
Logic "1" Current	Full	VI			300			300	μA
Logic "0" Current	Full	VI			500			500	μA
Input Capacitance	+25°C	V		2			2		pF
POWER SUPPLIES									
$-V_S$ Supply Current	+25°C	I		288	350		288	350	mA
	Full	VI			375			375	mA
$+V_S$ Supply Current	+25°C	I		11	14		11	14	mA
	Full	VI			16			16	mA
Nominal Power Dissipation	+25°C	V		1.5			1.5		W

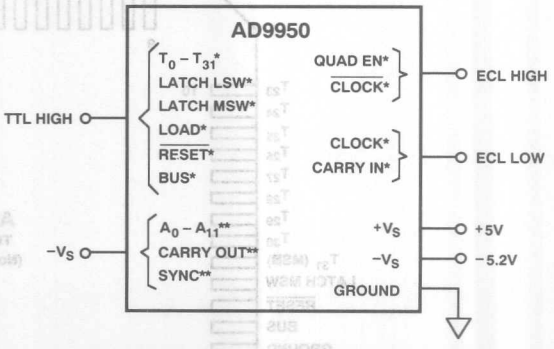
AC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V)

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
ECL INPUTS									
CLOCK Update Rate[2]	+25°C	I	250	300		250	300		MSPS
	Full	V		250			250		MSPS
CLOCK Pulse Width HIGH	+25°C	IV	2.0	1.7		2.0	1.7		ns
	Full	V		2.0			2.0		ns
CLOCK Pulse Width LOW	+25°C	IV	2.0	1		2.0	1		ns
	Full	V		2.0			2.0		ns
CARRY IN Set-Up Time[3]	+25°C	IV	0.2	0		0.2	0		ns
	Full	V		0.5			0.5		ns
CARRY IN Hold[3]	+25°C	IV	2.0	1.25		2.0	1.25		ns
	Full	V		1.5			1.5		ns
ECL OUTPUTS[4]									
Rise Time[5]	+25°C	IV		1	1.6		1	1.6	ns
	Full	V		1.2			1.2		ns
Fall Time	+25°C	IV		1	1.6		1	1.6	ns
	Full	V		1.2			1.2		ns
Data Skew[6]	+25°C	V		0.4			0.4		ns
Output Capacitance	+25°C	V		2			2		pF
A_0–A_{11} Delay[3]	+25°C	IV	3.7	4.5	5.3	3.7	4.5	5.3	ns
	Full	V		5.0			5.0		ns
SYNC Propagation Delay[3]	+25°C	IV	3.5	4.2	5.0	3.5	4.2	5.0	ns
	Full	V		4.6			4.6		ns
CARRY OUT Propagation Delay[3]	+25°C	IV	3.6	4.4	5.2	3.6	4.4	5.2	ns

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
TTL INPUTS—Bus Mode									
T_{16}–T_{31} Set-Up Time[7]	+25°C	IV	5.0	3.8		5.0	3.8		ns
(t_{TSU})	Full	V		4.3			4.3		ns
T_{16}–T_{31} Hold Time[7]	+25°C	IV	0.5	−0.5		0.5	−0.5		ns
(t_{TH})	Full	V		0.5			0.5		ns
LOAD Set-Up Time[3]	+25°C	IV	0.75	0.2		0.75	0.2		ns
(t_{LSU})	Full	V		0.5			0.5		ns
LOAD Hold Time[3]	+25°C	IV	0.2	0		0.2	0		ns
(t_{LH})	Full	V		0.2			0.2		ns
TTL INPUTS—Parallel Mode									
T_1–T_{31} Set-Up Time[3]	+25°C	IV	3.0	1.5		3.0	1.5		ns
(t_{TSU})	Full	V		2.5			2.5		ns
T_1–T_{31} Hold Time[3]	+25°C	IV	0.5	−0.5		0.5	−0.5		ns
(t_{TH})	Full	V		1.0			1.0		ns
LOAD Set-Up Time[3]	+25°C	IV	0.75	0.2		0.75	0.2		ns
(t_{LSU})	Full	V		0.5			0.5		ns
LOAD Hold Time[3]	+25°C	IV	0.2	0		0.2	0		ns
(t_{LH})	Full	V		0.2			0.2		ns
RESET									
Minimum Pulse Width	+25°C	IV	2.5	1.6		2.5	1.6		ns
(Low)	Full	V		2			2		ns

NOTES
[1]Typical thermal impedances (part in socket): θ_{JA} = 42°C/W; θ_{JC} = 11°C/W.
[2]Minimum specification with 50% duty cycle on clock. Typical can be achieved with duty cycle adjustment to 70% HIGH.
[3]Referenced to CLOCK/$\overline{\text{CLOCK}}$ differential signal crossing point (CLOCK rising; $\overline{\text{CLOCK}}$ falling).
[4]ECL outputs terminated to −2 V through 100 Ω.
[5]Measured as the 10% to 90% transition time.
[6]Measured as the worst case difference between the 50% points of both falling and rising edges.
[7]Referenced to the 50% point of the rising edge of LATCH MSW or LATCH LSW.
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS
Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



*INDICATES EACH PIN IS CONNECTED THROUGH 100Ω
**INDICATES EACH PIN IS CONNECTED THROUGH 10kΩ

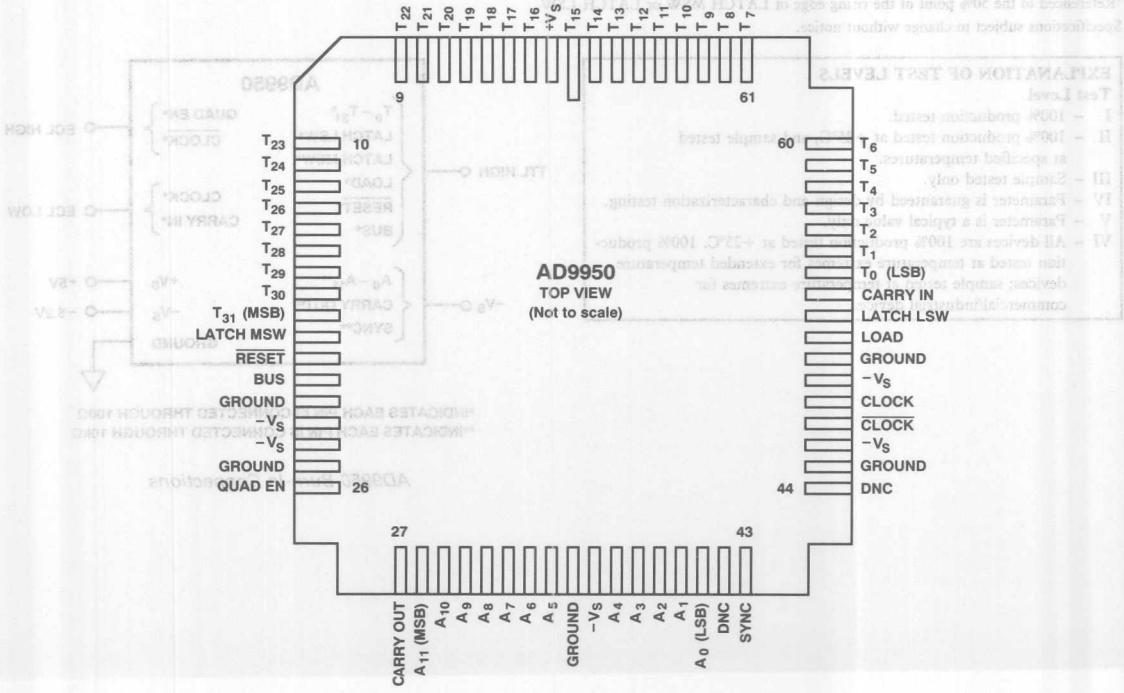
AD9950 Burn-In Connections

AD9950 TRUTH TABLE
BUS MODE
(Data Inputs = T_{16}–T_{31})

BUS	$\overline{\text{RESET}}$	LATCH MSW	LATCH LSW	LOAD	OPERATION
1	1	0	1	0	Transfers Most Significant 16-Bit Tuning Word into MSW Register
1	1	1	0	0	Transfers Least Significant 16-Bit Tuning Word into LSW Register
1	1	1	1	1	Load MSW and LSW Registers (32 Bits) Into Δ-Phase Register on Next CLOCK Cycle
X	0	X	X	X	Asynchronous Reset

PARALLEL MODE
(Data Inputs = T_0–T_{31})

BUS	$\overline{\text{RESET}}$	LATCH MSW	LATCH LSW	LOAD	OPERATION
0	1	X	X	1	Load 32-Bit Tuning Word into Δ-Phase Register on Next CLOCK Cycle
X	0	X	X	X	Asynchronous Reset



AD9950 Pin Designations

AD9950 PIN DESCRIPTIONS

Pin	Name	Function
1, 3–18 and 54–68	T_0–T_{31}	TTL-compatible word that determines the phase step of the accumulator. The tuning word can be loaded in parallel (32 bits) or bus (16 bits) mode. In bus mode, the two 16-bit words are loaded into the MSW and LSW registers through T_{16}–T_{31}.
2	$+V_S$	Positive power supply, nominally +5 V.
19	LATCH MSW	TTL-compatible latch command for the 16 most significant bits (MSBs) of the tuning word. In parallel mode, the MSW register is always transparent. In bus mode, the MSW register is transparent when LATCH MSW is LOW.
20	$\overline{\text{RESET}}$	TTL-compatible asynchronous reset command. See text.
21	BUS	TTL-compatible control pin. Logic HIGH enables the MSW and LSW registers, and multiplexes the data from T_{16}–T_{31} into both registers. Logic LOW enables the parallel load mode; the MSW and LSW registers are transparent, and T_0–T_{31} are latched directly into the delta-phase register by the LOAD signal.
22, 25, 35, 45, 50	GROUND	Ground return for the device. Ground for the ECL output stages is Pin 35.
23, 24, 36, 46, 49	$-V_S$	Negative power supply, nominally −5.2 V. Power for the ECL output stages is from Pin 36.
26	QUAD EN	ECL-compatible control pin. Logic HIGH enables the quadrature logic, which reduces the amount of memory required to implement the external phase-to-amplitude look-up table. The quadrature logic is used when generating waveforms symmetrical about the 90° and 180° phase points (i.e., a sine wave). See text.
27	CARRY OUT	ECL-compatible overflow flag. Logic HIGH at this pin indicates an overflow condition exists for the output data during that clock cycle. For applications in which two AD9950 units are cascaded to obtain 64 bits of phase resolution, CARRY OUT of the lower-order accumulator should be connected to CARRY IN of the higher-order accumulator.
47	$\overline{\text{CLOCK}}$	ECL-compatible input; should be driven differentially with CLOCK.
48	CLOCK	ECL-compatible input; should be driven differentially with $\overline{\text{CLOCK}}$. The contents of the delta-phase register are added to the output register after each rising edge of the CLOCK input.
28–34 and 37–41	A_0–A_{11}	Twelve bits of ECL-compatible output data from the phase accumulator output register.
42, 44	DNC	Internal test points. Do not connect; let pins float.
43	SYNC	ECL-compatible output signal. SYNC will go HIGH for one clock cycle following the prealignment of new tuning data. SYNC serves as a flag to indicate the completion of the minimum period for loading new data. See Theory Section.
51	LOAD	TTL-compatible latch control for the delta-phase register. Data is transferred into the delta-phase register on the first rising edge of CLOCK after LOAD has gone HIGH.
52	LATCH LSW	TTL-compatible latch command for the 16 least significant (LSBs) of the tuning word. In parallel mode, the LSW register is always transparent. In bus mode, the LSW register is transparent when LATCH LSW is LOW.
53	CARRY IN	ECL-compatible input. The effective value of the tuning word is increased by one LSB when CARRY IN is HIGH. For applications in which two AD9950 units are cascaded to obtain 64 bits of phase resolution, CARRY OUT of the lower-order accumulator should be connected to CARRY IN of the higher-order accumulator.

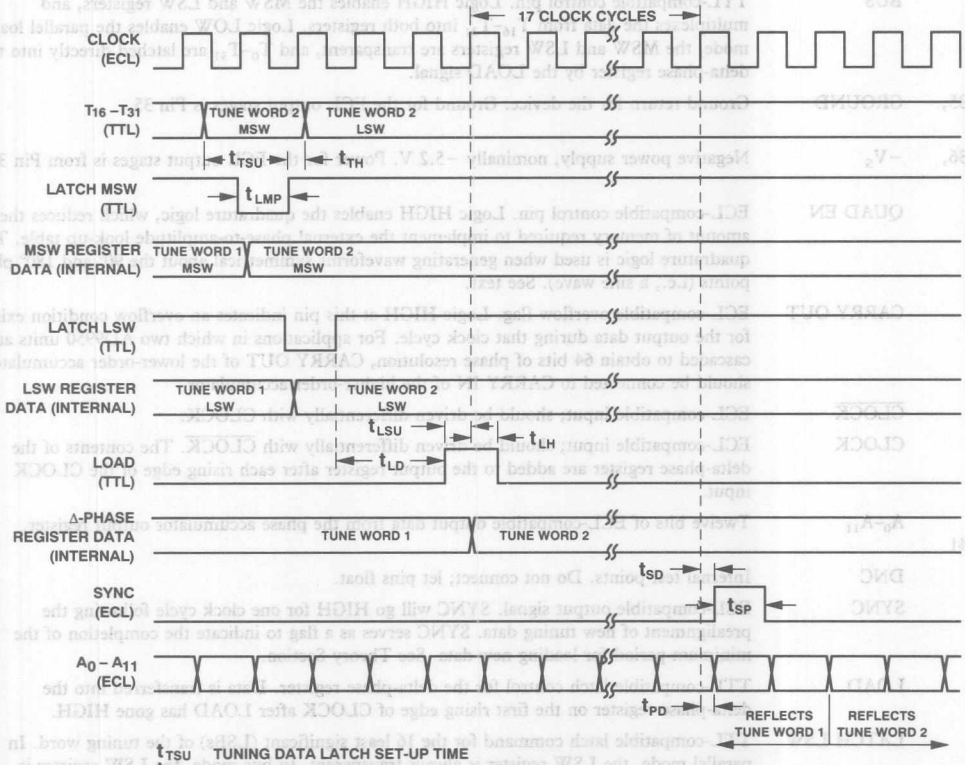
AD9950 THEORY OF OPERATION

Refer to the block diagram of the AD9950 on the first page of this data sheet.

The heart of the AD9950 is a 32-bit carry-save adder accumulator, implemented with 2-bit ripple-carry adder cores. The 32-bit input for this adder is stored in the Δ-phase registers.

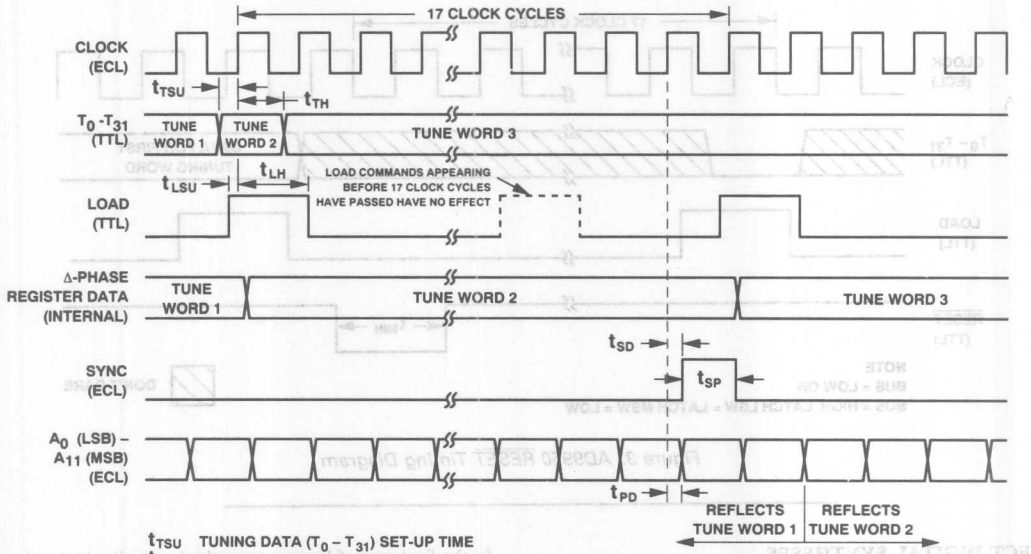
Registers for the most significant word (MSW) and least significant word (LSW) are controlled by the BUS command. In the parallel mode (BUS @ logic LOW), these registers are transparent, and serve only to buffer the tuning data. In the bus mode (BUS @ logic HIGH), they operate as level-triggered latches; and data is strobed into the registers on the leading edge of LATCH MSW or LATCH LSW. In the bus mode, data for both registers is multiplexed through T_{16}–T_{31}.

In either mode, new data is strobed into the Δ-Phase register by the rising edge of the first clock cycle after the LOAD command goes high. These and other timing relationships are illustrated in the timing diagrams.



t_{TSU}	TUNING DATA LATCH SET-UP TIME
t_{TH}	TUNING DATA HOLD TIME
t_{LMP}	MSW/LSW LATCH MINIMUM PULSE WIDTH LOW = 2ns
t_{LSU}	LOAD COMMAND SET-UP TIME
t_{LH}	LOAD COMMAND HOLD TIME
t_{LD}	MINIMUM LOAD COMMAND DELAY, MEASURED FROM MOST RECENT MSW/LSW REGISTER UPDATE
t_{SD}	SYNC PROPAGATION DELAY (DOES NOT INCLUDE 17 CLOCK CYCLE PIPELINE DELAY)
t_{SP}	SYNC PULSE WIDTH
t_{PD}	OUTPUT DATA (A_0 – A_{11}) PROP DELAY

Figure 1. AD9950 Bus Mode Timing Diagram



t_{TSU} TUNING DATA ($T_0 - T_{31}$) SET-UP TIME
t_{TH} TUNING DATA HOLD TIME
t_{LSU} LOAD COMMAND SET-UP TIME
t_{LH} LOAD COMMAND HOLD TIME
t_{SD} SYNC PROPAGATION DELAY (DOES NOT INCLUDE 17 CLOCK CYCLE PIPELINE DELAY)
t_{SP} SYNC PULSE WIDTH
t_{PD} OUTPUT DATA ($A_0 - A_{11}$) PROP DELAY

Figure 2. AD9950 Parallel Mode Timing Diagram

When new data is presented to the Δ-Phase register, the carry-save architecture requires that the data for the 2-bit cores be staggered in time, and this delay is provided by the block labeled Pre-Align Pipeline Register. The scheme used to prealign the data requires the Δ-Phase Register to remain constant for 16 clock cycles after each update.

Timing circuits in the AD9950 latch the contents of the Δ-phase register for 16 clock cycles after the LOAD command goes HIGH, preventing corruption of the data during the prealignment process. After the 16-clock-cycle delay, the SYNC output will go high for one clock cycle to indicate that new data has completed the prealignment, and a new tuning word can be loaded into the Δ-phase register. It should be noted that the tuning speed (frequency update rate) of the DDS is limited by this architecture to one-seventeenth of the clock rate.

The data from the 2-bit cores must also be realigned to provide the 12-bit output of the AD9950, and this delay is provided by the block labeled Post-Align Register. When the quad logic is enabled (QUAD EN @ logic HIGH), the 10 LSBs (A_0–A_9) are inverted when A_{10} is HIGH. This logic is used with similar external logic to reduce the size of a sine look-up table.

Pre- and post-alignment delays combine to form a 17-clock-cycle delay of the output data. In addition to this delay, the loading of the Δ-phase register and the adder accumulator each add an additional clock cycle delay, bringing the total delay through the AD9950 to 19 clock cycles.

The $\overline{\text{RESET}}$ (active LOW) command is asynchronous, and will reset the adder accumulator and the post-align logic. The Δ-phase register and the pre-align logic are not affected by the $\overline{\text{RESET}}$ command, even though the timing (SYNC) circuits are reset. A complete reset of the AD9950 should be executed whenever power is applied. This resetting consists of loading the Δ-phase register with all zeros; allowing the data to propagate through the prealign registers (16 clock cycles, as described above); and then taking the $\overline{\text{RESET}}$ pin LOW.

Timing for the reset circuits is shown in Figure 3.

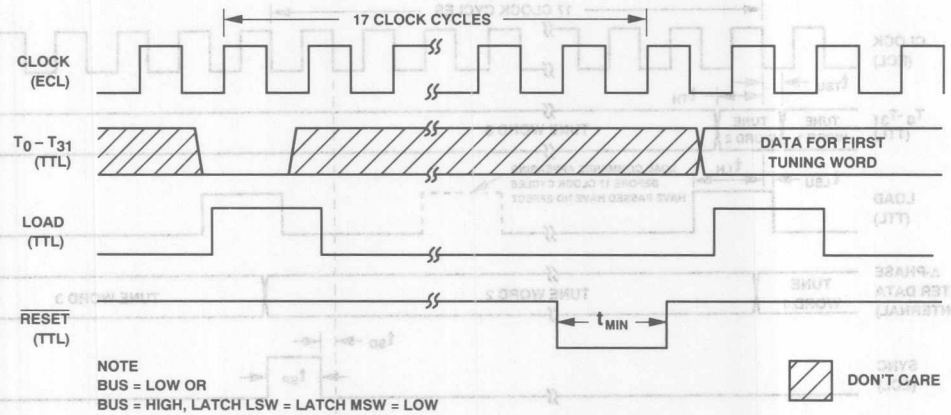


Figure 3. AD9950 $\overline{\text{RESET}}$ Timing Diagram

DIRECT DIGITAL SYNTHESES

Direct digital synthesis (DDS) is a method of deriving a wide-band, digitally controlled frequency (sine wave) synthesizer from a single reference frequency (system clock).

The circuit has three major components:

1. Phase Accumulator
2. Phase-to-Amplitude Converter
3. Digital-to-Analog Converter

These major stages and their relationships to one another are illustrated in the block diagram shown below.

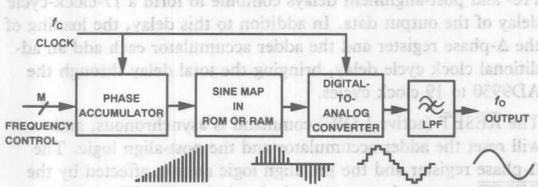


Figure 4. Block Diagram of DDS Generator

The phase accumulator is a digital device which generates the phase increment of the output waveform. Its input is a digital word which (with the reference oscillator) determines the frequency of the output waveform. The output of the phase accumulator stage represents the current phase of the generated waveform. In effect, the accumulator serves as a variable-frequency oscillator generating a digital signal.

Translating phase information from the phase accumulator into amplitude data takes place in the phase-to-amplitude converter; this is most commonly accomplished by means of a look-up table (LUT) stored in memory.

In the final step of frequency synthesis, amplitude data is converted into an analog signal. This is done by a digital-to-analog (D/A) converter which must have good linearity; low glitch impulse; and fast, symmetrical rise and fall times. When it does, the frequency synthesizer is able to produce a spectrally pure waveform.

The AD9950 is a digital phase accumulator intended for use in DDS applications. A simplified block diagram of an accumulator is shown below.

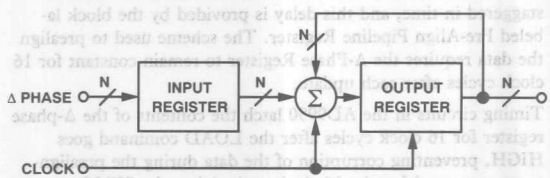


Figure 5. Accumulator Simplified Block Diagram

Operation of the device is straightforward: the contents of the input register are added to the output register on each clock cycle.

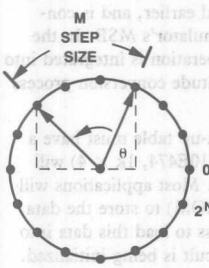
Input data represents a phase step, and is referred to as Δ-phase. The output data is a digital ramp whose frequency is a fraction of the clock frequency:

$$f_{OUT} = \frac{Phase\ Step}{2\pi} f_{CLOCK} = \frac{\Delta\ Phase}{2^N} f_{CLOCK},$$

$$\Delta\ Phase \leq 2^N - 1$$

where N is the resolution (number of bits) of the accumulator. (N determines the resolution to which the output frequency can be adjusted: $f_{CLOCK}/2^N$.)

The output data of the phase accumulator can be considered a phase vector moving around a circle, as shown graphically in Figure 6.



ACCUMULATOR RESOLUTION

BITS	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

Figure 6. Vector Representation of Phase Accumulator State

In this analogy, the vector will move around the circle in fixed steps, called Δ-Phase, in response to each clock cycle. The number of phase points which is available is determined by N, the resolution of the accumulator. The frequency of the output waveform is determined by the number of clock cycles required to move the phase vector around the circle one time.

Phase data at the output of the accumulator is converted to amplitude data by means of a look-up table (LUT); that data, in turn, is converted to an analog signal by a digital-to-analog converter (DAC).

To avoid aliasing, the output frequency should be limited to less than one-half the clock frequency. This translates to limiting Δ-Phase $\leq 2^{(N-1)}$. The majority of DDS systems limit output frequency to less than 40% of the clock rate to make design of the low-pass filter (LPF) easier. Practical DDS designs often limit the output frequency to less than 25% to minimize the effects of ac limitations in the DAC.

The DAC is the only analog component in the circuit, and its resolution determines the amplitude quantization of the generated waveform. This amplitude quantization places a theoretical limit on the signal-to-noise ratio (SNR) of the DDS system. In addition to quantization effects, the DAC has static and dynamic nonlinearities which corrupt the converter's ideal transfer function. DC nonlinearity, slew rate, glitch impulse, settling time, and digital feedthrough are all DAC characteristics which can reduce the dynamic range of the overall DDS system.

Implementing the Look-Up Table

Using the full resolution of the phase accumulator in the phase-to-amplitude conversion is both impractical and unnecessary. As an example, using the full resolution of the AD9950 would require a look-up table >4G × 12.

It is preferable to have the LUT only large enough to insure that the dc error of the output waveform is dominated by the quantization error of the DAC. In most DDS applications, the conversion is to a sine (or cosine) wave. This requires the look-up table to have two more bits of resolution than the DAC. In the AD9950, phase output data is truncated to 12 bits, supporting a 10-bit DAC for sine wave applications (4k × 10 LUT).

Using the Quad Logic

In sine wave applications, the amount of memory needed to implement the LUT can be reduced by taking advantage of the known characteristics of a sine wave. The AD9950 incorporates on-board "quad logic" to simplify using this technique. This logic is enabled by taking the QUAD EN (Pin 26) input high.

First, the look-up table does not need to store the most significant bit (MSB) of the amplitude data because it is the same as the MSB of the phase accumulator data; this reduces the amount of memory which is required to 4k × 9.

The symmetrical properties of sine waves allow further reduction. Only the first quadrant (90°) of the sine wave is required, as shown. This reduces the memory of the LUT addressed by the 10 LSBs of the AD9950 to 1k × 9.

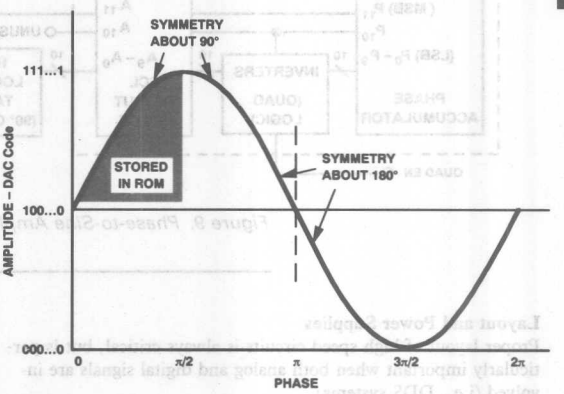


Figure 7. AD9950 Sinewave Phase-Amp Converter

Because the second quadrant of the sine wave is the mirror image of the first, it can be addressed by inverting the 10 least significant bits (LSBs) of the AD9950. This address inversion is performed on board the AD9950 by the quadrature logic, a set of inverters which are transparent when data is in the first quadrant, but functional when data is in the second quadrant. The second-most significant bit (A_{10}) of the accumulator determines in which quadrant the data is located and controls the inverters.

Each inverter is actually a two-input exclusive-or (XOR) gate driven by one of the LSBs (A_0–A_9) and A_{10}. Its operation is illustrated in Figure 8.

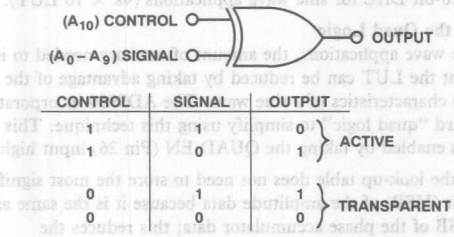


Figure 8. XOR as Controlled Inverter

Quadrants three and four of the sine wave are the inverse of quadrants one and two. Amplitude data for the LSBs in these quadrants is obtained by inverting the data from the LUT. This step is similar to the inversion described earlier, and is controlled by the complement of the accumulator's MSB. In the Analog Devices model AD9720, this operation is integrated into the DAC. The complete phase-to-amplitude conversion process using quad logic is illustrated below.

The memory used to construct the look-up table must have a fast read access time; 3 ns ECL RAM (10E474, 1k × 4) will support the update rate of the AD9950. Most applications will require a separate read-only memory (ROM) to store the data permanently and an initialization process to load this data into the RAM during the time the DDS circuit is being initialized.

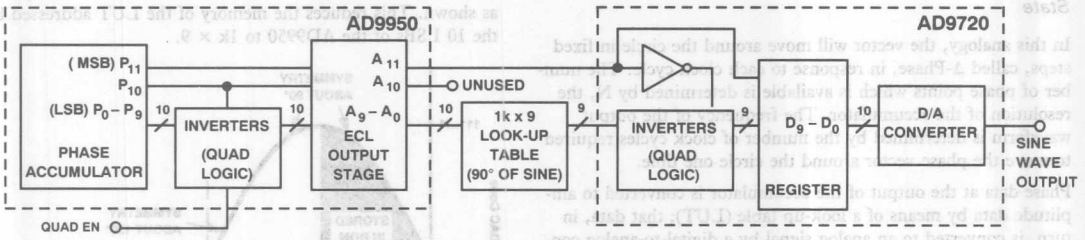


Figure 9. Phase-to-Sine Amplitude Conversion, Using Quad Logic

Layout and Power Supplies

Proper layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved (i.e., DDS systems).

Analog signal paths should be kept as short as possible, and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. Terminations for ECL signals should be as close as possible to the receiving gate.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance power planes.

AD9950 APPLICATION

The diagram shown below illustrates implementation of a 300 MSPS direct digital synthesizer using the AD9950 32-bit phase accumulator and the AD9720 10-bit 300 MSPS digital-to-analog converter (DAC). The AD9950 is controlled by a 16-bit microprocessor, which provides tuning data for the system.

Phase-to-amplitude conversion uses a 1k × 9 LUT and is stored in very fast (3 ns access time) ECL RAM. Data for the ECL RAM is stored permanently in a CMOS ROM and is transferred into the RAM as part of the initilization process discussed earlier.

Sine data for the LUT is based on the 12-bit phase data from the AD9950 and is calculated as:

$$ROUND\left[511.5 \times sin\left(\frac{A_0\text{–}A_9}{4096} \times 2\pi\right)\right]$$

This provides data for the AD9720 DAC that has a spectral purity of ≤ 76 dBFS.

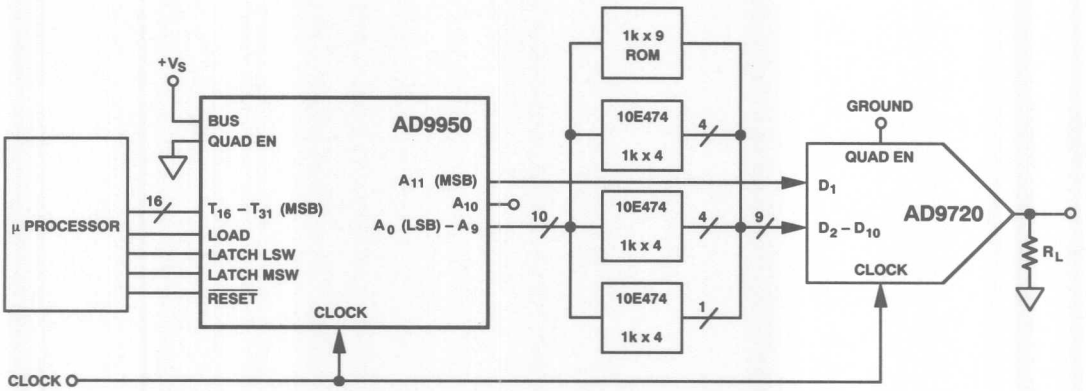
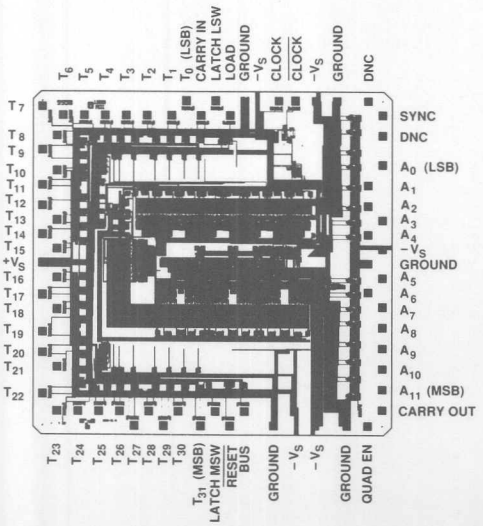


Figure 10. AD9950 10-Bit DDS Application

DIE LAYOUT AND MECHANICAL INFORMATION

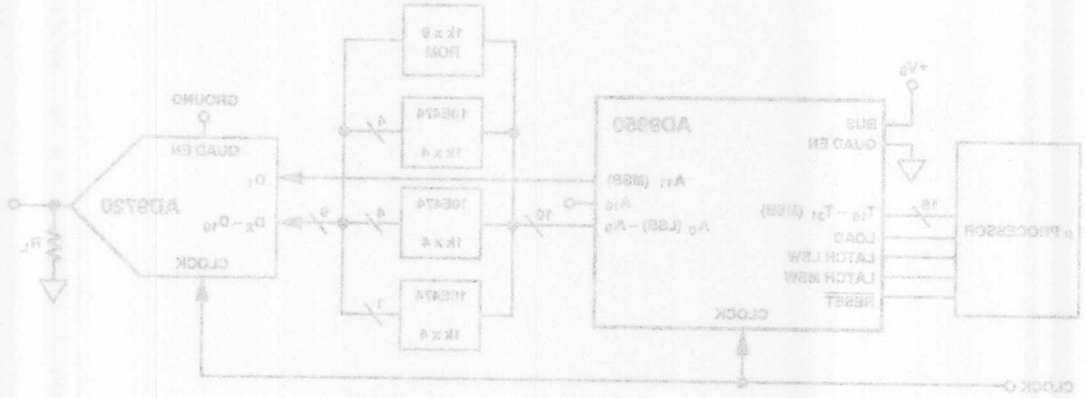


Die Dimensions	175 × 172 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic)
Bond Wire	1–1.3 mil, Gold; Gold Ball Bonding

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9950KJ	0°C to +70°C	68-Pin J-Leaded Ceramic	J-68
AD9950TJ	−55°C to +125°C	68-Pin J-Leaded Ceramic	J-68

*J = J-leaded ceramic package; hermetically sealed ceramic package, similar to PLCC. For outline information see Package Information section.


ADSP-2100
ADSP-2101
ADSP-2102
ADSP-2103
ADSP-2104
ADSP-2105
ADSP-2111
ADSP-2115
ADSP-2116
ADSP-2117
ADSP-2118
ADSP-2119
ADSP-2120
ADSP-2121
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ADSP-2147
ADSP-2148
ADSP-2149
ADSP-2150
ADSP-2151
ADSP-2152
ADSP-2153
ADSP-2154

LIU-01

FEATURES

- Recovers Data From Lines Varying From 0 ft. to Over 6000 ft.
- Wide Data Range, Under 300bps to Over 6Mbps
- Accepts RZ and NRZ Data Formats
- Accepts Unipolar and Bipolar Transmission Formats
- Single +5Volt Operation
- Automatic Gain/ Equalization Control; Dynamic Range>60dB
- TTL/CMOS Compatible Clock and Data Outputs
- Provides LOSS-OF-CARRIER Output
- Suitable for T1, E1, T1C, T2, DDS, and LAN Applications
- Meets CCITT and ATT Specifications for ISDN Compatibility

APPLICATIONS

- PBXs and LANs Using Twisted-Pair, Coax, or Fiber Optic Cable
- ISDN Compatible Equipment: Computers, FAX Machines, Test Equipment
- Industrial Communications/Process Control
- Digital Multiplexers, CSUs, and Switching Equipment

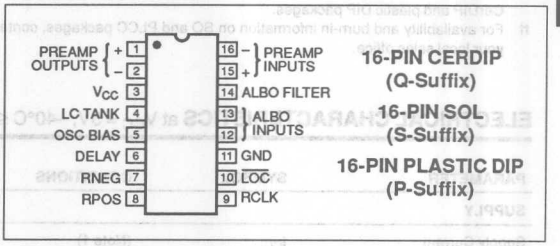
GENERAL DESCRIPTION

The LIU-01 is a versatile monolithics receiver for use in serial data transmission networks. It allows the recovery of data transmitted in both RZ and NRZ formats over lines from 0 ft. to over 6000 ft. The LIU-01 separates the clock from data and presents both clock and data as TTL/CMOS compatible outputs. A LOSS-OF-CARRIER output is also provided to indicate that the incoming signal has fallen below a usable level. The LIU-01 incorporates a high gain preamplifier and dual ALBO ports enabling it to automatically

Continued

4

PIN CONNECTIONS

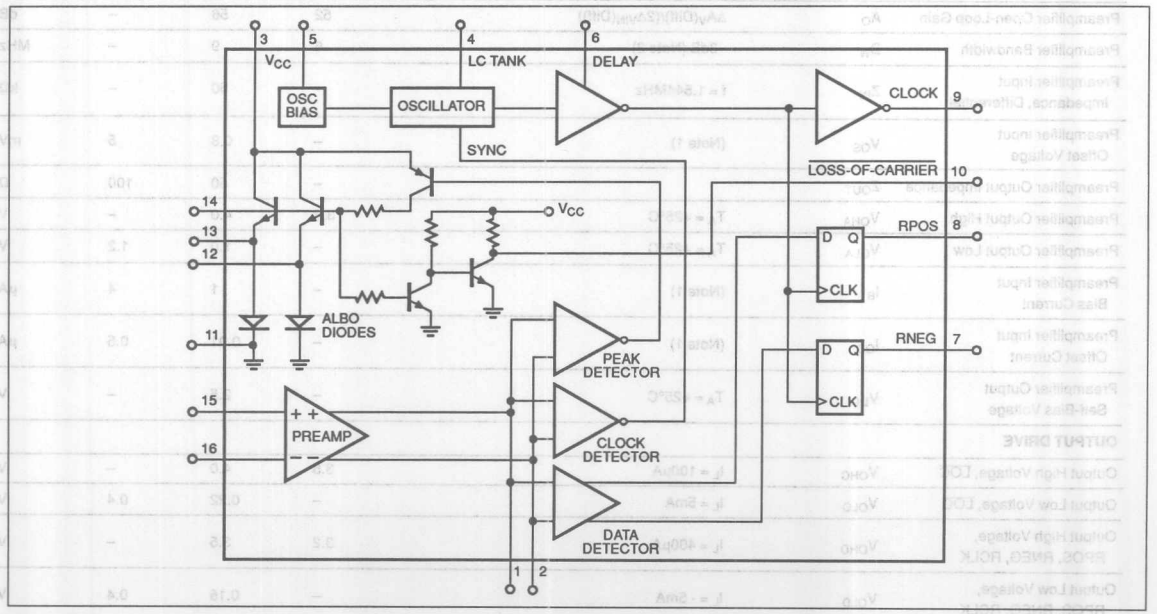


16-PIN CERDIP (Q-Suffix)

16-PIN SOL (S-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION *Continued*

adjust for the signal attenuation and frequency distortion encountered at varying lengths of twisted-pair, coax, or fiber optic transmission lines. It will tolerate an input signal range of over 60dB and can handle data rates ranging from less than 300bps to greater than 6Mbps.

The LIU-01 meets all CCITT and ATT specifications for an ISDN compatible receiver interface. Additionally, it is directly compatible with the R8070 and, with one additional inverter gate, the DS2180 digital T1 transeivers.

ORDERING INFORMATION †

PACKAGE		
CERDIP 16-PIN	PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
LIU01FQ	LIU01FP	XIND
—	LIU-1FS††	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltage, Pin 3 to Pin 11 ..... 6.5V, –0.5V
Maximum Voltage, Any Pin Except 12 and 13 ..... V_{CC}
Maximum Sinking Current, Any Pin 20mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature ..... +300°C
Junction Temperature ..... +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{CC} = 5V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

			LIU-01F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC}	(Note 1)	–	20	28	mA
Supply Voltage	V_{CC}		4.75	5.0	5.5	V
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A_O	$\Delta A_V(Diff)/(2\Delta_{VIN}(Diff))$	52	56	–	dB
Preamplifier Bandwidth	B_W	–3dB (Note 2)	6	9	–	MHz
Preamplifier Input Impedance, Differential	Z_{IN}	f = 1.544MHz	–	50	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	(Note 1)	–	0.8	5	mV
Preamplifier Output Impedance	Z_{OUT}		–	50	100	Ω
Preamplifier Output High	V_{OHA}	T_A = +25°C	3.8	4.0	–	V
Preamplifier Output Low	V_{OLA}	T_A = +25°C	–	1.0	1.2	V
Preamplifier Input Bias Current	I_B	(Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	(Note 1)	–	0.01	0.5	µA
Preamplifier Output Self-Bias Voltage	V_{DC}	T_A = +25°C	–	2.5	–	V
OUTPUT DRIVE						
Output High Voltage, $\overline{LOC}$	V_{OHC}	I_L = 100µA	3.5	4.0	–	V
Output Low Voltage, $\overline{LOC}$	V_{OLC}	I_L = 5mA	–	0.22	0.4	V
Output High Voltage, RPOS, RNEG, RCLK	V_{OHD}	I_L = 400µA	3.2	3.5	–	V
Output Low Voltage, RPOS, RNEG, RCLK	V_{OLD}	I_L = - 5mA	–	0.15	0.4	V

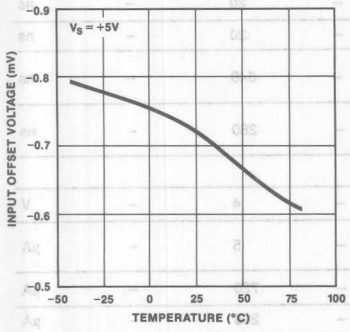
ELECTRICAL CHARACTERISTICS at V_{CC} = 5V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	LIU-01F MIN	TYP	MAX	UNITS
Output Pulse Rise-Time	T_{OR}		–	20	–	ns
Output Pulse Fall-Time	T_{OF}		–	20	–	ns
Output Pulse-Width, RPOS, RNEG	P_{WD}	f = 1.544MHz	–	648	–	ns
Output Pulse-Width, RCLK	P_{WC}	f = 1.544MHz	–	280	–	ns
CLOCK CIRCUIT						
Oscillator Bias Voltage	V_{BIAS}	$V_{PIN\,5}$	–	4	–	V
Tank Emitter-Follower Base Current	I_{TB}	(Note 1)	–	5	–	µA
Oscillator Bias Current	I_{OSC}		–	720	–	µA
Oscillator Injection Current	I_{INH}		–	200	–	µA
Data Sampling Interval	T_{DS}		–	20	–	ns
Delay Circuit Resistor	R_d	Measured from Pin 6 to Pin 3 T_A = +25°C	700	1000	1300	Ω
ALBO						
ALBO Threshold	V_{TA}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	1.35	1.5	1.65	V
ALBO Threshold ±Differential	V_{TAD}		–	–	75	mV
ALBO ON Voltage	V_{O14}	Measured at Pin 14, $[V_{PIN\,1} - V_{PIN\,2}]$ = ALBO Threshold + 20mV	1.0	1.7	4.0	V
ALBO OFF Voltage V_{F14}		Measured at Pins 12, 13, 14 (Note 1)	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN		–	6	15	Ω
Maximum ALBO Diode Impedance	R_D MAX	f = 1.544MHz (Note 2)	20	30	–	kΩ
ALBO Diode Impedance Matching		R_D = 100Ω	–	10	–	%
DATA/CLOCK THRESHOLDS						
Clock Threshold	V_{TC}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	0.92	1.05	11.22	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$		68	71	74	%
Data Threshold	V_{TD}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	0.62	0.75	0.90	V
Data Threshold as % of ALBO Voltage	$T_{CD\%}$		46	50	54	%

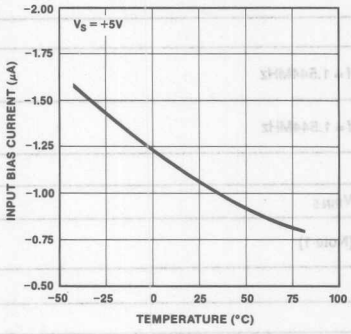
NOTES:
1. Preamplifier self-biased $V_{PIN\,1} \approx V_{PIN\,2} \approx V_{PIN\,15} \approx V_{PIN\,16}$.
2. Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS

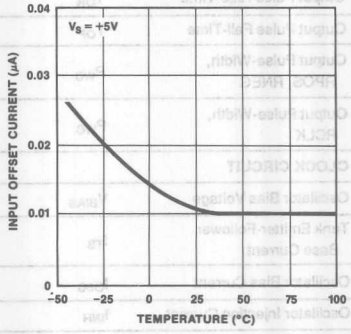
INPUT OFFSET VOLTAGE vs TEMPERATURE



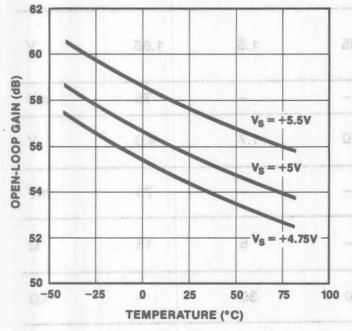
INPUT BIAS CURRENT vs TEMPERATURE



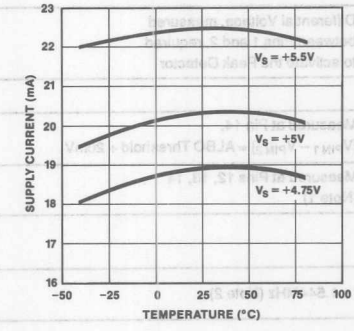
INPUT OFFSET CURRENT vs TEMPERATURE



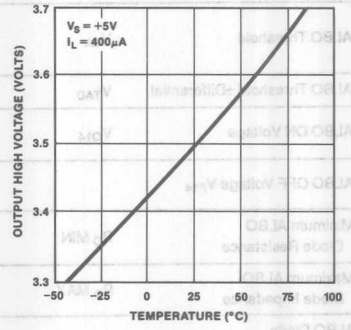
OPEN-LOOP GAIN vs TEMPERATURE



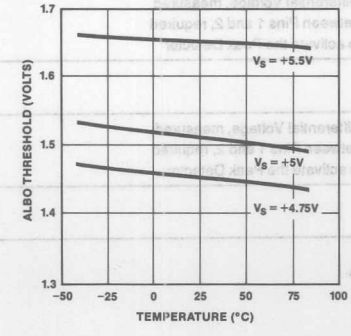
SUPPLY CURRENT vs TEMPERATURE



OUTPUT HIGH VOLTAGE (V_{OHD}) vs TEMPERATURE



ALBO THRESHOLD vs TEMPERATURE



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The Preamplifier: The LIU-01 contains a differential-input, differential-output preamplifier with a gain-bandwidth product of over 5GHz. Internally, the preamp outputs drive a differential signal into a set of threshold comparators. The external inverting preamp output is normally used only for biasing. The differential inputs and the external noninverting output behave as a conventional op amp. Thus, the preamplifier open-loop gain, A_{VOL}, is specified as $\Delta V_O(+)/\Delta V_{IN}(Diff)$. Preamplifier bandwidth, typically 9MHz, is the frequency at which A_{VOL} has fallen 3dB from its DC value. Unlike a 741-type op amp whose single-pole open-loop gain response provides unity gain stability, the LIU-01's preamplifier has been optimized for maximum gain-bandwidth product and exhibits a multiple-pole gain roll-off beyond 10MHz. The preamp's open-loop gain and phase vs. frequency characteristics are shown in Figure 1. Specific points on these characteristic curves are listed in Table 1. The curves imply that the LIU-01 requires a minimum closed-loop gain of 200 for stability. By providing 46dB of feedback loop attenuation at 20MHz, the preamp will be stable with about 35° of phase margin. To aid in modeling the frequency response of the LIU-01 preamp, Table 2 lists the approximate locations of the first 6 open-loop poles.

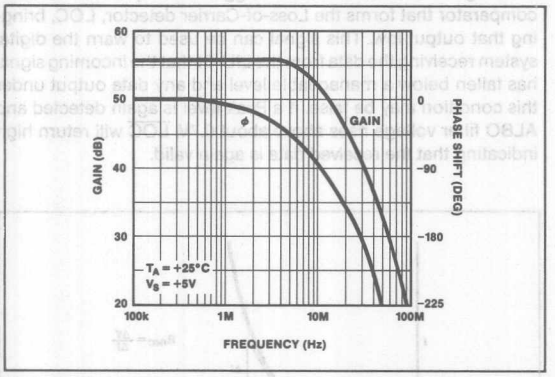


FIGURE 1: *LIU-01 preamplifier gain/phase vs frequency.*

TABLE 1: Typical Preamp Gain/Phase Response

FREQUENCY (MHz)	A_{VOL} (dB)	PHASE (DEG)
1.0	55.7	−8.7
1.544	55.7	−14.0
9.0	52.7	−82.7
20.0	45.8	−145.7
30.0	40.8	−180.8

TABLE 2: LIU-01 Preamp Model

A_{VOL}	R_O	OPEN-LOOP POLES
56dB	50Ω	12MHz 20MHz 4 × 135MHz

The LIU-01's preamp is designed to operate around a balanced DC common-mode bias level equal to roughly 50% of the supply voltage on both its inputs and outputs. This allows the outputs to achieve maximum swing when amplifying an AC coupled, bipolar signal. It also produces zero differential preamp output voltage for zero input signal. Operating from a +5V supply, the preamp outputs will balance at approximately +2.5V allowing an output voltage swing of ±1.5V around this bias level as illustrated in Figure 2.

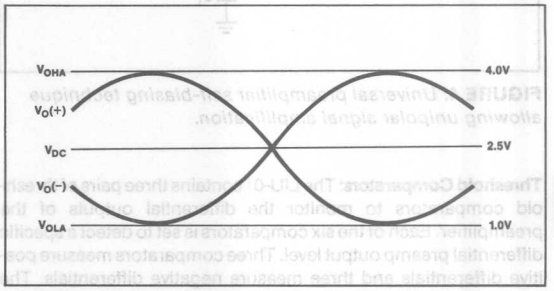


FIGURE 2: *The differential outputs of the LIU-01's preamplifier swing symmetrically around a DC bias point of about 2.5V. $V_O(-)$ is inverted with respect to $V_O(+)$ about this point.*

Figures 3 and 4 show two methods of configuring the preamp to automatically self-bias both the inputs and outputs to an optimum level. The single resistor and capacitor used in Figure 3 extracts the DC average of the inverting output and feeds it back to the noninverting input to establish the input common-mode level. This negative feedback will force the outputs to center their swing around the DC level at which $V_O(Diff) = 0V$. This type of self-biasing is practical only when the preamp is passing a balanced, AC coupled, bipolar signal. If the preamp must preserve the DC level of an unbalanced, unipolar signal, then a self-biasing scheme as is shown in Figure 4 is required. This network sets the input common-mode level by establishing the DC average of both differential outputs. In this way, the input common-mode level will always be that voltage at which $V_O(Diff) = 0V$ regardless of the input signal.

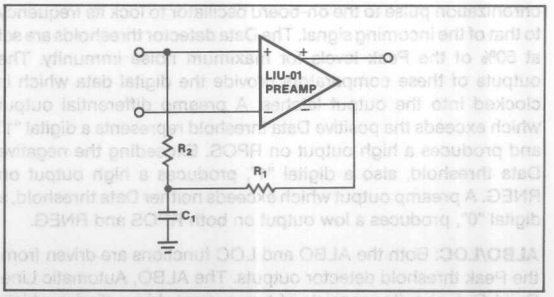


FIGURE 3: *Preamp self-biasing for use with AC coupled, balanced bipolar signals.*

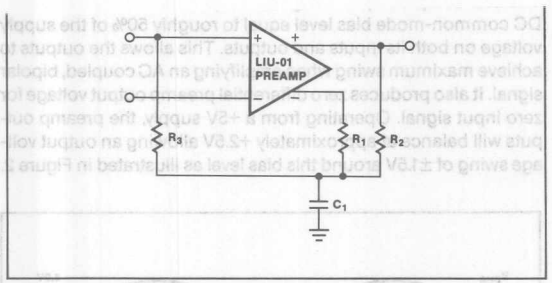


FIGURE 4: *Universal preamplifier self-biasing technique allowing unipolar signal amplification.*

Threshold Comparators: The LIU-01 contains three pairs of threshold comparators to monitor the differential outputs of the preamplifier. Each of the six comparators is set to detect a specific differential preamp output level. Three comparators measure positive differentials and three measure negative differentials. The individual thresholds are labeled as positive and negative Peak, Clock and Data as shown in Figure 5.

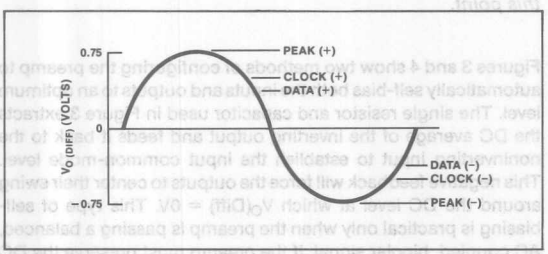


FIGURE 5: *Six threshold comparators detect positive and negative differential preamp output levels.*

The Peak detector outputs are used to perform an AGC-type function (ALBO) to maintain a constant preamp output level. The Clock detector thresholds are set at 71% of the Peak levels. When the Clock thresholds are reached, the comparators send a synchronization pulse to the on-board oscillator to lock its frequency to that of the incoming signal. The Data detector thresholds are set at 50% of the Peak levels for maximum noise immunity. The outputs of these comparators provide the digital data which is clocked into the output latches. A preamp differential output which exceeds the positive Data threshold represents a digital "1" and produces a high output on RPOS. Exceeding the negative Data threshold, also a digital "1", produces a high output on RNEG. A preamp output which exceeds neither Data threshold, a digital "0", produces a low output on both RPOS and RNEG.

ALBO/LOC: Both the ALBO and LOC functions are driven from the Peak threshold detector outputs. The ALBO, Automatic Line Build-Out, circuitry consists of two current driven diodes which act as variable impedance elements enabling the LIU-01 to close a current pulse is sourced into the ALBO diodes. These pulses are averaged to a DC current by an external ALBO filter capacitor. As the current flowing through the diodes increases, their incremental impedance is lowered as described by the exponential I-V curve for a diode-connected NPN transistor shown in Figure 6. The impedance of the NPN transistor emitters which source the current to the ALBO diodes follows an identical curve. Because the bases of these transistors look like an AC short to ground by virtue of the external ALBO filter capacitor, the total AC impedance of each ALBO port looks like the parallel combination of two diodes:

Equation 1 $$R_D \cong \frac{0.026V}{2I_D} + R_{STRAY}$$

where I_D equals the DC current flowing through the diodes and R_{STRAY} represents the stray resistance inherent in the LIU-01, about 3Ω. The longer a Peak level is detected, the greater I_D becomes, lowering R_D. When no Peak levels are detected, the voltage on the ALBO filter capacitor becomes zero, shutting off current to the diodes. Under this condition, the stray pin capacitance of about 3pF will limit maximum ALBO impedance. A 1.544MHz signal will see an effective port ALBO impedance of about 30kΩ. In addition to shutting off the ALBO diodes, the loss of voltage on the ALBO filter will trigger the simple two-transistor comparator that forms the Loss-of-Carrier detector, $\overline{LOC}$, bringing that output low. This signal can be used to warn the digital system receiving the data from the LIU-01 that the incoming signal has fallen below a manageable level and any data output under this condition may be false. If a Peak level is again detected and ALBO filter voltage rises above about 0.7V, $\overline{LOC}$ will return high indicating that the received data is again valid.

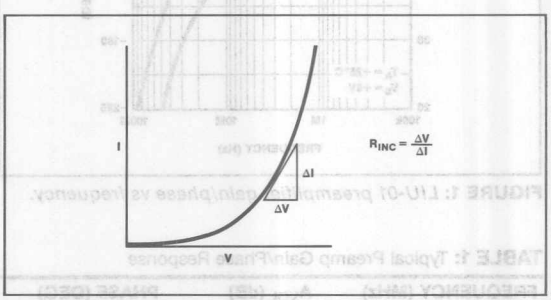


FIGURE 6: *The incremental impedance of the diode-connected NPN transistor used as the ALBO diode is dependent on the DC bias current flowing through it.*

The Oscillator: The LIU-01's on-board oscillator is designed to be free-running at a frequency, f_o, set by an external inductor and capacitor, where $f_o \cong 1/(2\pi\sqrt{LC})$. The phase and exact frequency of the oscillator are synchronized to the incoming data signal by the Clock threshold comparators. Each time the preamplifier's differential output exceeds the Clock thresholds, the comparator's outputs inject a current pulse into the LC tank oscillator aligning its oscillation with the incoming signal. During periods

where no Clock levels are detected by the comparators, the LC tank's oscillation will relax back to its own resonant frequency. An internal comparator is used to square the LC tank's sinusoidal oscillation into a digital level clock. This comparator incorporates a delay function to allow the user to control when the clock edge will reach the output latches. The clock signal then passes through an inverter buffer and is presented as a TTL/CMOS compatible output, RCLK.

The Output Latches: Two edge-triggered, D-type latches provide the TTL/CMOS compatible digital data outputs, RPOS and RNEG, of the LIU-01. The digital information at the outputs of the Data threshold comparators is clocked into these latches on the rising edge of the internal clock. This corresponds to RPOS and RNEG both being updated on the falling edge of the output clock. The latched data outputs will remain stable until they are updated again by the next clock cycle, therefore, the rising edge of the RCLK can be used directly to shift RPOS and RNEG into a shift register or onto a microprocessor bus. The timing of the LIU-01 digital outputs is illustrated in Figure 7. The output architecture of the LIU-01 is directly compatible with the R8070 digital transceiver. Unlike the R8070, the DS2180 digital transceiver clocks data in on the falling edge of the input clock. Using an inverting gate to invert RCLK enables the LIU-01 to shift data into the DS2180.

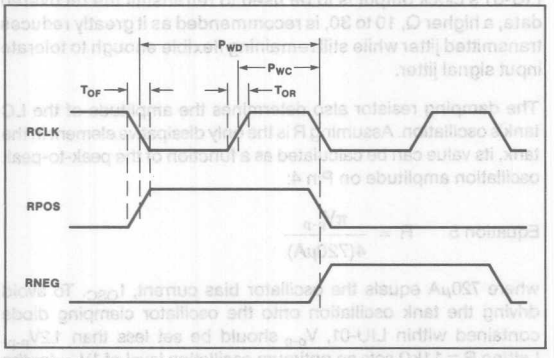


FIGURE 7: *The LIU-01's output timing insures that the data outputs are stable on the rising edge of RCLK. Skew between outputs is typically 10ns.*

DESIGNING WITH THE LIU-01

DESIGNING A WIDEBAND AMPLIFIER

Figure 8 shows a typical configuration using the LIU-01's preamplifier to create a high gain, wideband amplifier. The capacitor C_1 determines the amplifier's low frequency gain roll-off while resistors R_1 and R_2 set the AC closed-loop gain. At DC, the amplifier is in unity gain. A zero at $\omega_1 = 1/(R_2C_1)$ causes the AC gain to rise until a pole is reached at $\omega_2 = 1/(R_1C_1)$. The final value of closed-loop signal gain is equal to:

Equation 2 $$A_{VCL} = \frac{A_{VOL}}{1+\left(\frac{A_{VOL}R_1}{R_2}\right)}$$

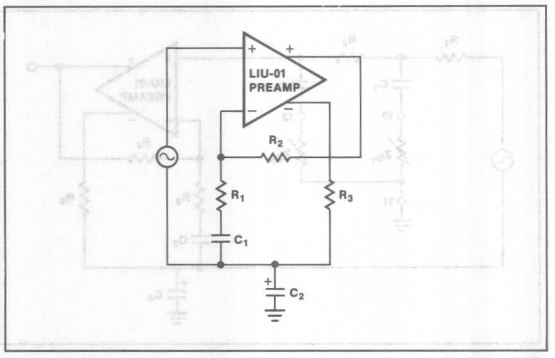


FIGURE 8: *Typical noninverting preamplifier gain configuration with self-biasing.*

To ensure preamp stability, the ratio R_2/R_1 must be a minimum of 200 to a bandwidth of at least 20MHz. Low value resistors should be used for R_2 and R_1 to minimize the effects of stray capacitance in the feedback loop. Since PC board applications exhibit at least 2pF of stray feedback capacitance (equal to about 4kΩ impedance at 20MHz), R_1 should be less than 20Ω.

Because the preamp's differential output voltage is monitored by the internal threshold comparators, any output offset will degrade the symmetry of positive and negative threshold levels. Operating the preamplifier in DC unity gain is instrumental in minimizing the output offset voltage. Offset can be further reduced by balancing the preamp's DC input source impedance. Preamp output loading in the form of feedback and biasing networks should also be balanced to ensure uniform inverting action between the two preamp outputs.

AGC USING THE ALBO DIODES

The variable impedance action of the LIU-01's internal ALBO diodes can be used to create a wide dynamic range AGC loop with the preamplifier as shown in Figure 9. While the preamp operates at a fixed AC gain, the input signal is variably attenuated by the impedance-divider networks of R_1/Z_{D_1} and R_2/Z_{D_2}. As the input signal magnitude increases and the preamp's outputs cross the Peak thresholds, ALBO diode impedance decreases providing more signal attenuation prior to the preamplifier input. If input signal magnitude decreases, diode impedance will increase, reducing signal attenuation. The result is a constant preamp input level creating a constant preamp output amplitude.

The DC blocking capacitors C_1 and C_2 are required to remove from the signal path the DC bias voltage, 0V to 0.8V, of the ALBO diodes. These capacitors also create a frequency dependency by adding a pole/zero pair in the attenuation characteristics of each ALBO diode stage. Figure 10 illustrates the gain vs. frequency response of the first ALBO stage assuming that $R_1 \ll R_2$ and $Z_{D_1} \ll R_1$. As Z_{D_1} changes depending on input signal amplitude, ω_z also changes. At $Z_{D_1} = R_D MAX$, $\omega_z = \omega_p$, and the stage gain equals unity with flat frequency response. At $Z_{D_1} = R_D MIN$, there is maximum separation between ω_z and ω_p and a maximum attenuation equal to approximately Z_{D_1}/R_1. Combining the effects of two ALBO stages allows the programming of two variable-duration poles and a gain ranging from unity to $(Z_{D_1}Z_{D_2})/(R_1R_2)$.

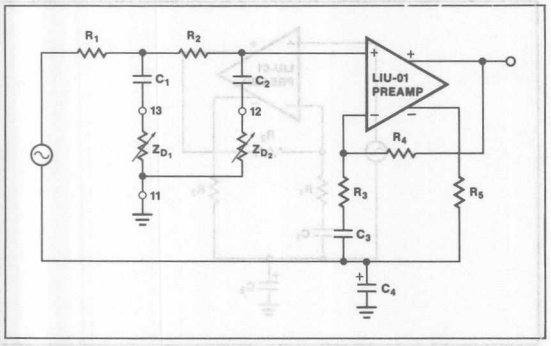


FIGURE 9: *By attenuating the input signal through impedance dividers, the ALBO network simulates the attenuation and frequency characteristics of maximum line length.*

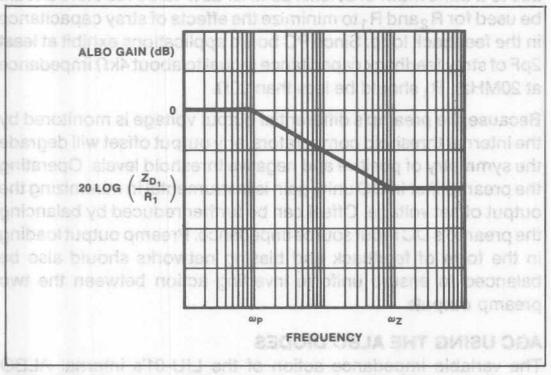


FIGURE 10: *The ALBO impedance creates frequency dependent attenuation.*

DESIGNING THE LC TANK OSCILLATOR

The oscillator on-board the LIU-01 is based on a pulsed LC resonant tank and produces a continuous "square-wave" clock output even in the absence of an incoming data signal. Connected as shown in Figure 11, the oscillator input, Pin 4, oscillates sinusoidally about the 4V oscillator bias, Pin 5. The nominal oscillation frequency, f_o, is given by the formula:

Equation 3 $$f_O = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

which takes into account the effect of the damping resistor, R. The damping resistor is used to reduce the Q of the LC tank where:

Equation 4 $$Q = R\sqrt{\frac{C}{L}}$$

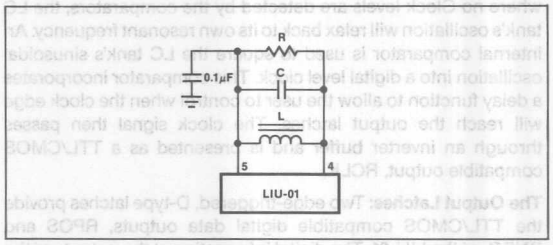


FIGURE 11: *A simple LRC resonant tank oscillator is used by the LIU-01 to recover the encoded clock from an incoming data signal.*

As the Q of the tank is reduced, the oscillation frequency becomes more easily pulled away from f_o by the synchronizing pulses of the Clock threshold comparators. A low Q, 2 to 10, is desirable for the receiver's oscillator because often the incoming data bit stream is timed at a clock rate slightly different from f_o. The bit stream may also contain timing jitter where each data bit or packet of bits arrives with a slightly different clock timing. To ensure that no data bits are missed under these conditions, the LIU-01's oscillator must be flexible enough to track the clock frequency carried within the incoming bit stream. However, if the LIU-01's clock output is to be used to retransmit the recovered data, a higher Q, 10 to 30, is recommended as it greatly reduces transmitted jitter while still remaining flexible enough to tolerate input signal jitter.

The damping resistor also determines the amplitude of the LC tank's oscillation. Assuming R is the only dissipative element in the tank, its value can be calculated as a function of the peak-to-peak oscillation amplitude on Pin 4:

Equation 5 $$R = \frac{\pi V_{p\text{-}p}}{4(720\mu A)}$$

where 720μA equals the oscillator bias current, I_{OSC}. To avoid driving the tank oscillation onto the oscillator clamping diode contained within LIU-01, $V_{p\text{-}p}$ should be set less than $1.2V_{p\text{-}p}$. Letting R = 1.1kΩ sets an optimum oscillation level of $1V_{p\text{-}p}$ for the LIU-01.

The values for L and C can be calculated by choosing the desired Q and f_o and then substituting Equation 4 into Equation 3. The generalized formulas for L and C become:

Equation 6 $$C = \frac{\sqrt{4Q^2 - 1}}{4\pi f_O R}$$

Equation 7 $$L = \frac{CR^2}{Q^2}$$

Note that to maintain a sustained oscillation during the absence of an incoming data bit stream, the Q of the LC tank must be greater than 1.

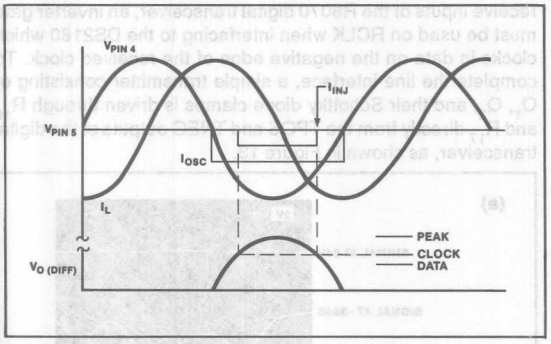


FIGURE 12: *The LC tank is synchronized to the incoming data when the clock detector injection current, I_{INJ}, is centered inside the oscillator's bias current pulse.*

When an incoming data bit stream is of sufficient amplitude to cross the Clock detectors' thresholds, a pulse of current is injected into the tank to synchronize the oscillator frequency to that of the incoming encoded clock. When synchronization is achieved, the various voltage and current waveforms are aligned as shown in Figure 12.

For maximum noise and jitter immunity, the clock edge which latches data into the D-type output latches should appear centered in the period where valid data is present. This active clock edge, generated by the negative-going "zero crossing" of the oscillation voltage on Pin 4, which leads by 90° in phase the center of the synchronized data bit. To accommodate this phenomena, a capacitor is used on Pin 6 to delay the clock edge as it passes to the D-latches. For the LIU-01, the value of this capacitor is calculated as:

Equation 8 $$C_{DELAY} = \frac{1}{5R_D f_O} - \frac{16ns}{R_D}$$

taking into account the value of the internal delay resistor, R_D = 1kΩ nominal, and a small propagation delay associated with the logic gates inside the LIU-01.

4

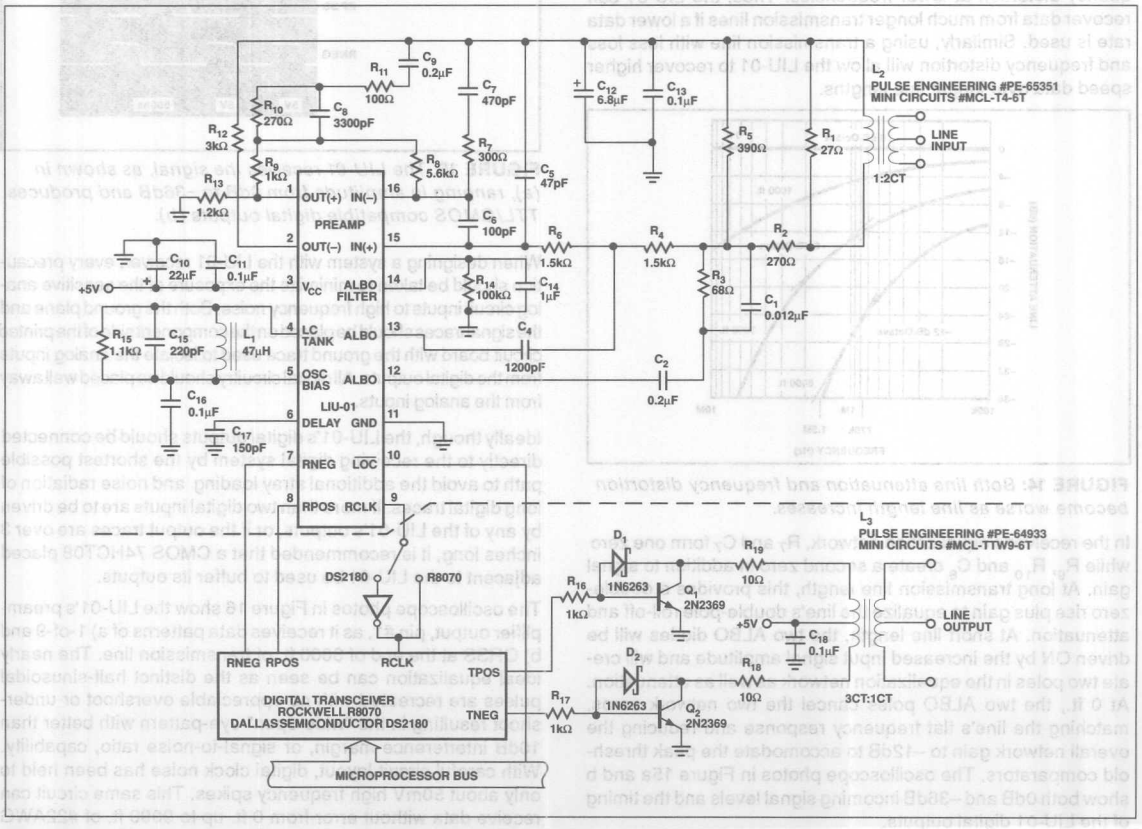


FIGURE 13: *The LIU-01 enables this 4-wire transceiver to recover T1 data at 1.544Mbits/s with an input signal level varying from 0dB to less than –38dB. The ALBO/equalization network is compatible with unshielded #22AWG twisted-pair wire measuring 16pf/ft.*

a 1.544MHz clock with a Q of about 2.4 for excellent jitter tolerance. The line input network, including the preamplifier feedback loop and ALBO diodes, is designed to compensate for the losses and distortion of the #22AWG unshielded twisted-pair wire transmission line whose characteristics of loss vs. frequency vs. length are shown in Figure 14. The goal of the receiver's equalization network is to allow the recovery of 1.544Mb/s T1 format with an input level that varies from 0dB ($6V_{p-p}$) to –38dB ($75mV_{p-p}$) measured at a frequency 1/2 the data rate, 772kHz. At 0 ft. of transmission line, the receiver's incoming signal is at 0dB level with no frequency distortion. By 3000 feet, the signal is at –12dB level and falling at –6dB/octave, single-pole roll-off, between 770kHz and 1.544MHz. At 6000 feet of transmission line, the signal falls to –24dB with a –12dB/octave, double-pole frequency roll-off.

Data rate and transmission line characteristics play an important role in determining the maximum line length from which the LIU-01 can recover data. From Figure 14 it can be seen that #22AWG twisted-pair wire exhibits much less loss and frequency distortion at lower frequencies. Thus, the LIU-01 can recover data from much longer transmission lines if a lower data rate is used. Similarly, using a transmission line with less loss and frequency distortion will allow the LIU-01 to recover higher speed data over longer line lengths.

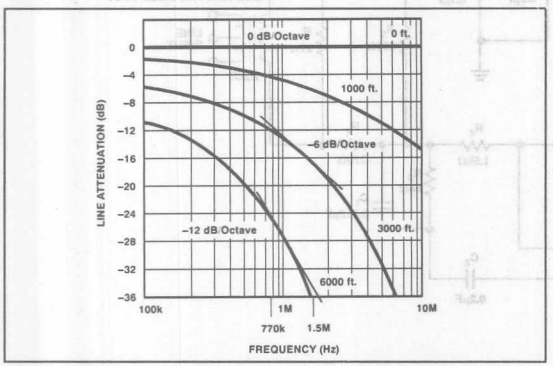


FIGURE 14: *Both line attenuation and frequency distortion become worse as line length increases.*

In the receiver's equalization network, R_7 and C_7 form one zero while R_9, R_{10} and C_8 create a second zero in addition to signal gain. At long transmission line length, this provides a double-zero rise plus gain to equalize the line's double-pole roll-off and attenuation. At short line length, the two ALBO diodes will be driven ON by the increased input signal amplitude and will create two poles in the equalization network as well as attenuation. At 0 ft., the two ALBO poles cancel the two network zeros, matching the line's flat frequency response and reducing the overall network gain to –12dB to accomodate the peak threshold comparators. The oscilloscope photos in Figure 15a and b show both 0dB and –36dB incoming signal levels and the timing of the LIU-01 digital outputs.

clocks in data on the negative edge of the received clock. To complete the line interface, a simple transmitter consisting of Q_1, Q_2, and their Schottky diode clamps is driven through R_{16} and R_{17} directly from the TPOS and TNEG outputs of the digital transceiver, as shown in Figure 13.

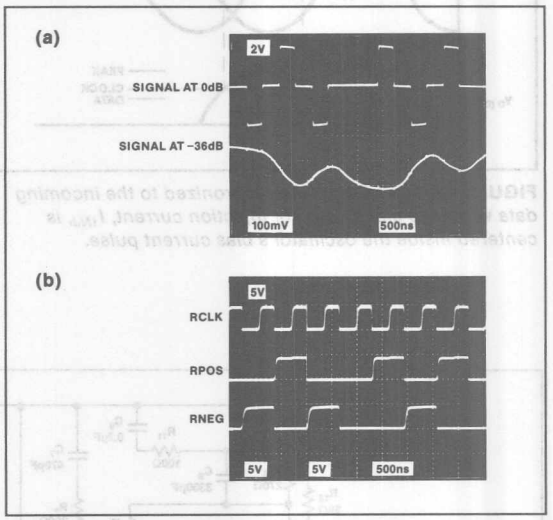


FIGURE 15: *The LIU-01 receives the signal, as shown in (a), ranging in amplitude from 0dB to –36dB and produces TTL/CMOS compatible digital outputs (b).*

When designing a system with the LIU-01 receiver, every precaution should be taken to minimize the exposure of the sensitive analog circuit inputs to high frequency noise. Both the ground plane and the signal traces should be placed on the component side of the printed circuit board with the ground trace used to isolate the analog inputs from the digital outputs. All digital circuitry should be placed well away from the analog inputs.

Ideally though, the LIU-01's digital outputs should be connected directly to the receiving digital system by the shortest possible path to avoid the additional stray loading and noise radiation of long digital traces. If more than two digital inputs are to be driven by any of the LIU-01's outputs, or if the output traces are over 3 inches long, it is recommended that a CMOS 74HCT08 placed adjacent to the LIU-01 be used to buffer its outputs.

The oscilloscope photos in Figure 16 show the LIU-01's preamplifier output, pin #1, as it receives data patterns of a) 1-of-9 and b) QRSS at the end of 6000 ft. of transmission line. The nearly ideal equalization can be seen as the distinct half-sinusoidal pulses are recreated with no appreciable overshoot or undershoot resulting in the "wide-open" eye-pattern with better than 10dB interference margin, or signal-to-noise ratio, capability. With careful circuit layout, digital clock noise has been held to only about 50mV high frequency spikes. This same circuit can receive data without error from 0 ft. up to 9000 ft. of #22AWG transmission line.

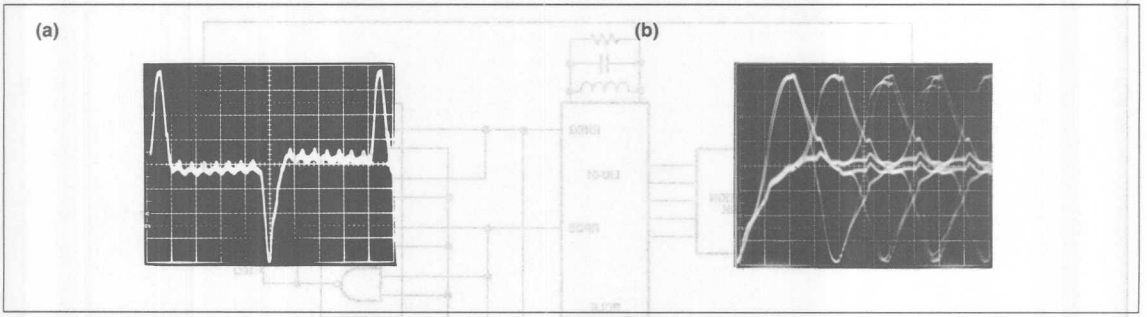


FIGURE 16: *The LIU-01's preamplifier output, pin #1, should produce half-sinusoidal pulses of recovered data signal when properly equalized for the transmission line. The circuit of Figure 13 has excellent response as shown here receiving at 6000 ft. a 1-of-9 pattern, a, and a QRSS pattern, b.*

In some applications, such as passive transmission line monitoring, the receiver must not terminate the line, but instead appears as a very high impedence load. To accomodate this need and still provide a low source impedence to the LIU-01, a buffer amplifier can be used as shown in Figure 17. The JFET input of BUF-03 presents a very high impedence to the transmission line while driving the equalization network with less than 10Ω output impedence at 1.544MHz. This buffering technique works well when analog supply voltages of at least ±8 volts are available to power the buffer. Figure 18 shows another technique for buffering the LIU-01 from the transmission line using only a single +5 volt supply. The emitter-follower transistor, Q1, appears to the line to be about a 50kΩ impedence at 1.544MHz.

With a nominal collector current of 4mA set by the 500Ω emitter resistor, Q1 drives the LIU-01's network with about 8Ω output impedence. The AC coupling capacitor, C_C, is required to remove the DC level shift of Q1's base-emitter voltage drop.

In Figure 19, the LIU-01 is used as an in-line monitor allowing data and clock to be read from the transmission line while simultaneously retransmitting a regenerated 0dB T1 signal. The data outputs RPOS and RNEG are logically recombined with RCLK by the 74HC00 which also acts directly as output line driver. The Schottky diode, D_1, along with R_1 and C_1 stretch the duty cycle of RCLK from a nominal 43% to 50% as required for T1 transmission.

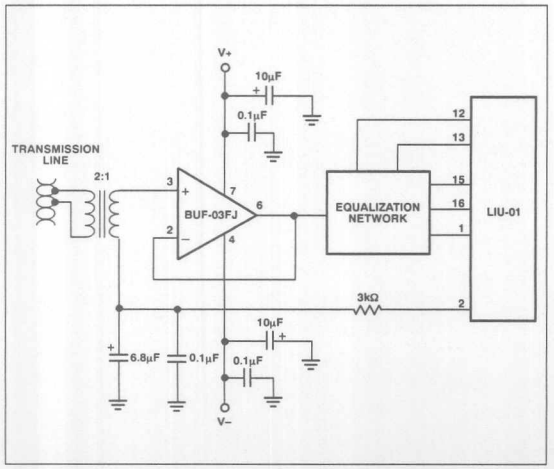


FIGURE 17: *The OP-42 provides high impedance input to the equalization network without raising the source impedance to the LIU-01 preamplifier.*

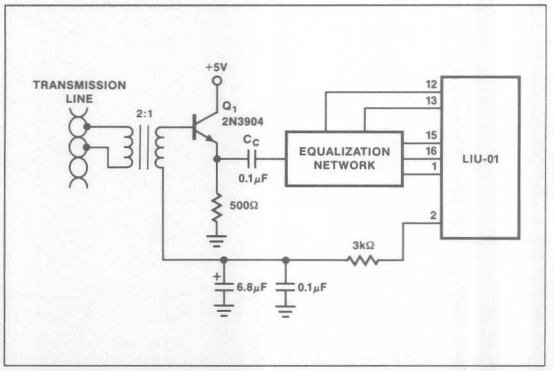


FIGURE 18: *Emitter-follower Q_1 acts as buffer between the equalization network and the transmission line while operating from only a +5V supply.*

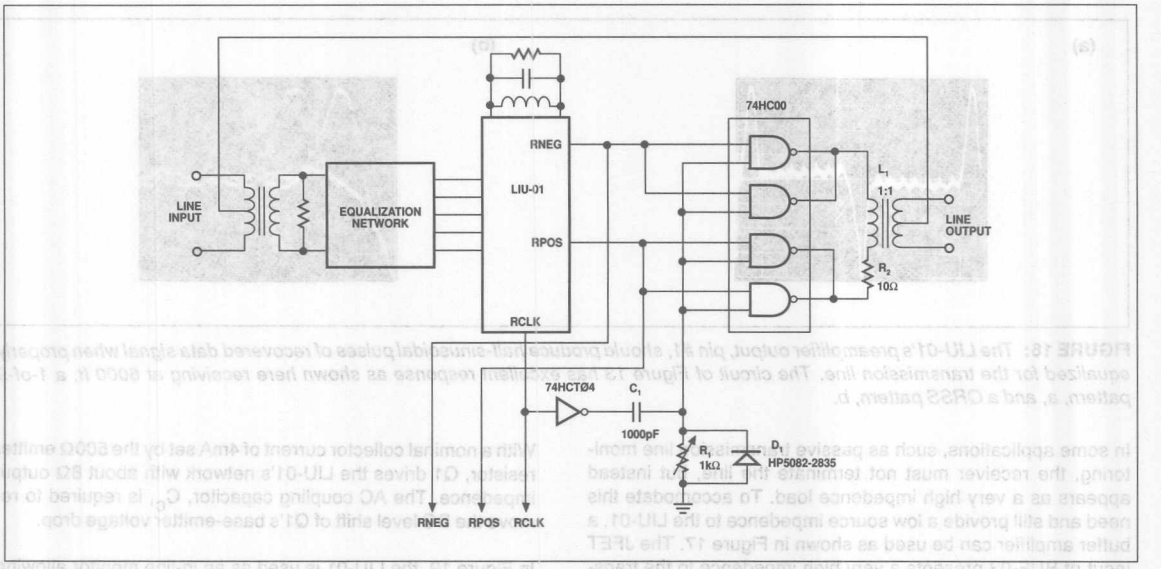


FIGURE 19: *The LIU-01 acts an in-line monitor/repeater using 74HC00 as an output driver. D_1, R_1, and C_1 stretch the duty cycle of RCLK to 50%. The value of R_1 depends on the operating data rate.*

RPT-82/RPT-83

FEATURES

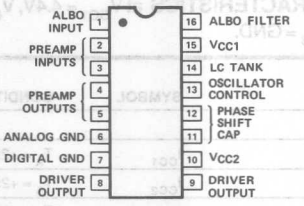
- **Automatic ALBO Function**
- **Clock-Shutdown Circuit (RPT-83)**
- **Low-Power Operation (100mW)**
- **Pin Compatible with XR-C277**

GENERAL DESCRIPTION

The RPT-82/83 are integrated circuits that perform the active functions required for regenerative PCM repeaters. They can operate from less than 100kHz to greater than 3MHz. In PCM systems, information is transmitted by the presence or absence of bipolar pulses in specified time slots. The RPT-82/83 repeaters automatically adjust gain to optimize signal levels, determine if a pulse is present or not, and retransmit the reconstructed pulses.

The difference between the RPT-82 and the RPT-83 is that the RPT-83 contains a **clock-shutdown circuit**. This shutdown circuit senses the incoming signal level and disables the clock drive if the incoming signal is below the level where accurate reconstruction is possible. This prevents noise or cross-talk from appearing as a valid signal that would be retransmitted.

PIN CONNECTIONS & ORDERING INFORMATION

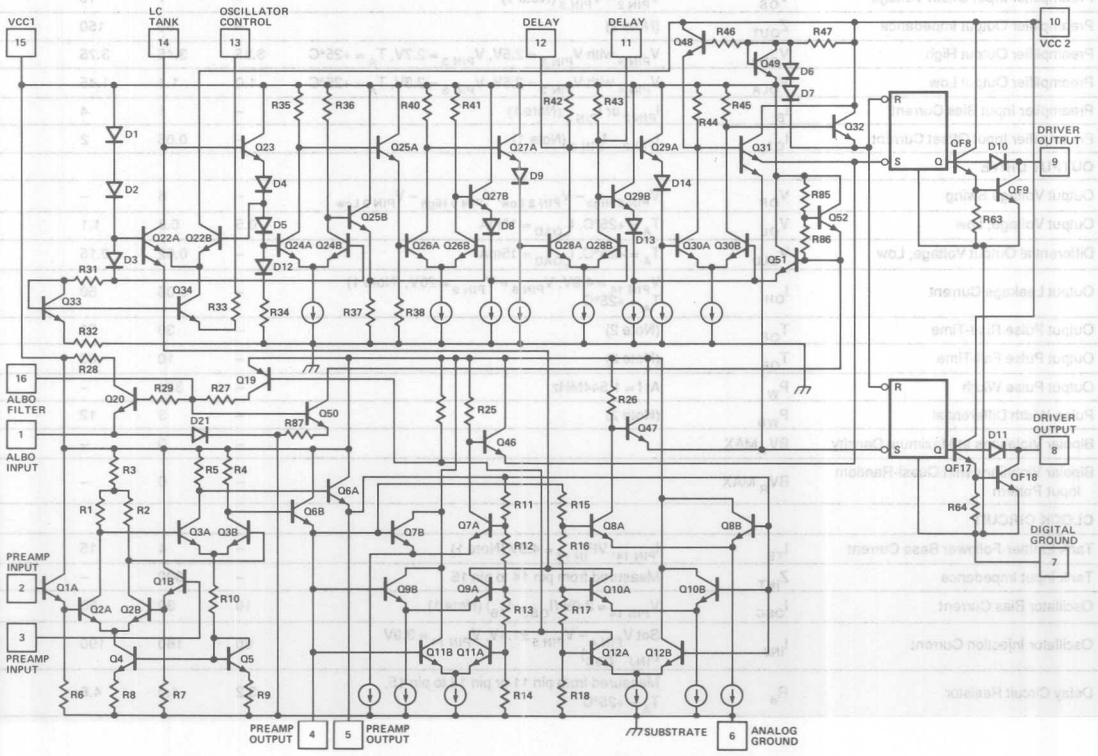


16-PIN HERMETIC DIP (Q-Suffix)

16-PIN SO (S-Suffix)

HERMETIC DIP	SO
RPT82FQ	RPT82FS
RPT83FQ	RPT83FS

RPT-83 SIMPLIFIED SCHEMATIC



Pin 10 to Pin 7 or 6 ..... ±16.0V, –0.2V
Pin 15 to Pin 7 or 6 ..... 8.0V, –0.2V
Maximum Voltage at Pins 8 or 9 ..... 30V, –0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14 ..... V_{CC2}
Maximum Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Solding Temperature ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.
$V_{PIN\ 6} = V_{PIN\ 7} = V_{PIN\ 13} = GND$.

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83 MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC1}	$T_A = +25°C$ (Note 1)	5.0	8.5	9.5	mA
Supply Current	I_{CC2}	$T_A = +25°C$ (Note 1)	1.0	2.5	3.5	mA
Total Supply Current	$I_{CC1} + I_{CC2}$	$T_A = +25°C$ (Note 1)	6	11	13	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain $\frac{\Delta V_{PIN\ 5}}{\Delta V_{PIN\ 2}}$	A_0	Measure $\Delta V_{Pin\ 2}$ necessary to change pins from 1.9V to 3.2V	44	48	51	dB
Preamplifier Bandwidth	B_W	3dB Points (Note 2)	3	5	–	MHz
Preamplifier Input Impedance	Z_{IN}		–	600	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	$V_{PIN\ 2} - V_{PIN\ 3}$ (Note 1)	–	1	15	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	–	80	150	Ω
Preamplifier Output High	V_{OHA}	$V_{PIN\ 4}$ with $V_{PIN\ 2} = 2.5V$, $V_{PIN\ 3} = 2.7V$, $T_A = +25°C$	3.35	3.45	3.75	V
Preamplifier Output Low	V_{OLA}	$V_{PIN\ 4}$ with $V_{PIN\ 2} = 2.5V$, $V_{PIN\ 3} = 2.3V$, $T_A = +25°C$	1.0	1.4	1.45	V
Preamplier Input Bias Current	I_B	$I_{PIN\ 2}$ or $I_{PIN\ 3}$ (Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	$I_{PIN\ 2} - I_{PIN\ 3}$ (Note 1)	–	0.05	2	µA
OUTPUT DRIVE						
Output Voltage Swing	V_{OP}	$V_{PIN\ 8\ High} - V_{PIN\ 8\ Low}$; $V_{PIN\ 9\ High} - V_{PIN\ 9\ Low}$	–	6	–	V
Output Voltage, Low	V_{OL}	$T_A = +25°C$. $I_{LOAD} = 15mA$	0.5	0.8	1.1	V
Differential Output Voltage, Low	V_{OLD}	$T_A = +25°C$. $I_{LOAD} = 15mA$	–	0.02	0.15	V
Output Leakage Current	I_{OH}	$V_{PIN\ 14} = 4.9V$, $V_{PIN\ 8} = V_{PIN\ 9} = 20V$, (Note 1) $T_A = +25°C$	–	0.05	50	µA
Output Pulse Rise-Time	T_{OS}	(Note 2)	–	30	50	ns
Output Pulse Fall-Time	T_{OF}	(Note 2)	–	10	60	ns
Output Pulse Width	P_W	At f = 1.544MHz	–	324	–	ns
Pulse-Width Differential	P_{WD}	(Note 2)	–	3	12	ns
Bipolar Violations at Maximum Density	BV_1 MAX		–	0	–	–
Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX		–	0	–	–
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{PIN\ 14}$, $VP_{IN\ 14} = 4.9V$ (Note 1)	–	4	15	µA
Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	–	300	–	kΩ
Oscillator Bias Current	I_{OSC}	$V_{PIN\ 14} = 3.9V$ ($I_{OSC} - I_{TB}$) (Note 1)	10	30	50	µA
Oscillator Injection Current	I_{INJ}	Set $V_{PIN\ 4} - V_{PIN\ 5} \pm 1.4V$, $V_{PIN\ 14} = 3.9V$ ($I_{INJ} - I_{OSC}$)	60	160	190	µA
Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, $T_A = +25°C$	3.2	4.0	4.8	kΩ

$V_{PIN\ 6} = V_{PIN\ 7} = V_{PIN\ 13}$ = GND. *Continued*

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83 MIN	TYP	MAX	UNITS
MISCELLANEOUS						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to activate the Peak Detector. T_A = +25°C	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector T_A = +25°C	0.85	1.0	1.2	V
Data Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector T_A = +25°C	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$	T_A = +25°C	67	73	78	%
Data Threshold as % of ALBO Voltage	$V_{TL\%}$	T_A = +25°C	46	54	58	%
ALBO ON Voltage	V_{O16}	Measured at pin 16, $[V_{p4} - V_{p5}]$ = ALBO Threshold	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 T_A = +25°C	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN		–	8	–	Ω
Maximum ALBO Diode Impedance	R_D MAX	f = 1.544MHz	–	30	–	kΩ
ALBO Gain Range	A_m	(Note 3)	36	48	–	dB

NOTES:
1. $V_{PIN}2 = 2.5V$; adjust $V_{PIN\ 3}$ until $V_{PIN\ 4} = V_{PIN\ 5}$.
2. Sample tested.
3. Guaranteed by design.

FUNCTIONAL DESCRIPTION

Bipolar-pulse transmission, the transmission of alternately positive and negative pulses, is used on repeater lines to remove the DC component present in unipolar PCM pulse trains. This also places the principal energy components in the 0–1.544MHz band, as opposed to the 0–3.088MHz band for unipolar pulse trains. The absence of a DC component in bipolar pulse trains permits the repeater to be transformer-coupled to the repeater line and helps prevent time-shifting of the regenerator firing levels with variations in input pulse density (see Figure 1).

ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS

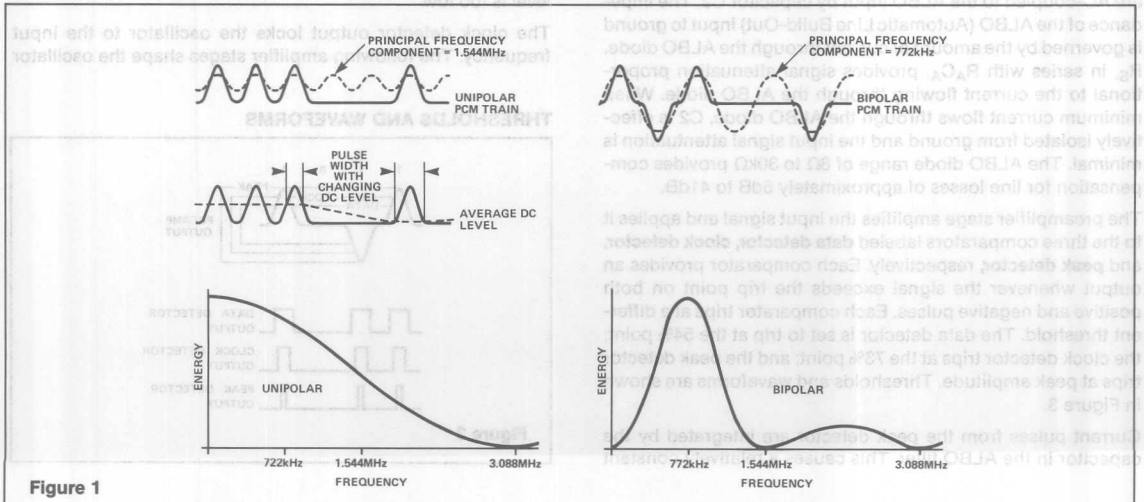


Figure 1

FUNCTIONAL BLOCK DIAGRAM

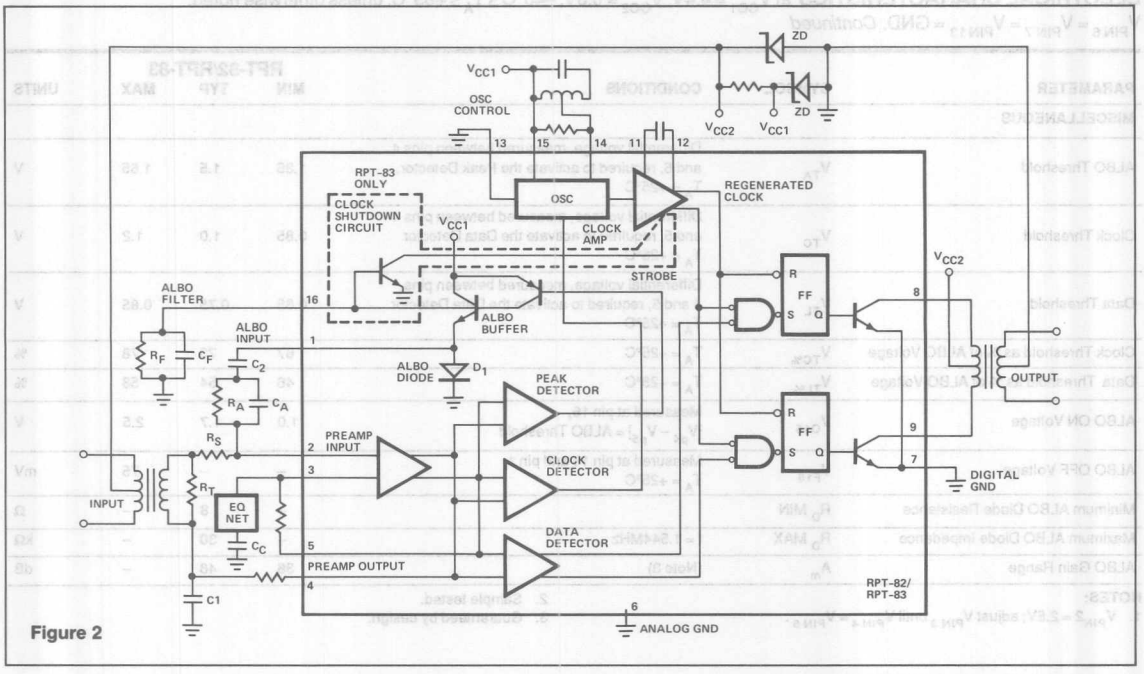


Figure 2

The bipolar-PCM pulse train is transformer-coupled into the preamplifier as shown in the functional block diagram (Figure 2). The secondary of the input transformer is loaded with the proper terminating resistor, R_T, to match the line impedance. One side of the transformer secondary is AC-coupled to ground by capacitor C1; the other side of the secondary winding is in series with resistance R_S. Resistor R_S and the RC network R_AC_A are AC-coupled to the ALBO input by capacitor C2. The impedance of the ALBO (Automatic Line Build-Out) input to ground is governed by the amount of current through the ALBO diode. R_S, in series with R_AC_A, provides signal attenuation proportional to the current flowing through the ALBO diode. When minimum current flows through the ALBO diode, C2 is effectively isolated from ground and the input signal attentuation is minimal. The ALBO diode range of 8Ω to 30kΩ provides compensation for line losses of approximately 5dB to 41dB.

The preamplifier stage amplifies the input signal and applies it to the three comparators labeled **data detector, clock detector,** and **peak detector,** respectively. Each comparator provides an output whenever the signal exceeds the trip point on both positive and negative pulses. Each comparator trips at a different threshold. The data detector is set to trip at the 54% point; the clock detector trips at the 73% point; and the peak detector trips at peak amplitude. Thresholds and waveforms are shown in Figure 3.

Current pulses from the peak detector are integrated by the capacitor in the ALBO filter. This causes a relatively constant current to flow through the emitter follower and D1. In the RPT-83, a low voltage at the ALBO filter enables the clock-shutdown circuit when there is no input signal. The clock-shutdown circuit turns off the clock amplifier so that neither the regenerated clock, nor the strobe outputs, are sent to the flip-flops. This prevents the RPT-83 from sending noise or cross-talk out as valid-appearing data pulses when the incoming data level is too low.

The clock detector output locks the oscillator to the input frequency. The following amplifier stages shape the oscillator

THRESHOLDS AND WAVEFORMS

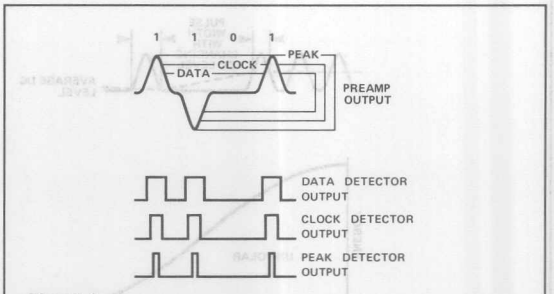


Figure 3

output and shift it in time. The phase-shift capacitor is selected to provide additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses. This provides optimum timing for determining if a "1" or a "0" is present. A 0-to-30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

The delayed regenerated clock and the data-detector outputs drive the input flip-flops and output transistors. The output transistors are coupled to the transmission line through an output transformer.

DETAILED DESCRIPTION

PREAMPLIFIER

The preamplifier performs two basic functions. The first is to raise the level of the incoming signal to the correct level to trip the comparators. The second is to provide frequency/gain compensation to enhance the signal-to-noise ratio of the incoming signal. The preamp is designed to be operated in a near open-loop condition. A limited amount of feedback is used to control the frequency response. The gain-phase relationship of the preamp (see Figures 4 and 5) implies that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

ALBO

To enable the preamp to operate open-loop with a wide range of signal levels, the ALBO diode is connected between the preamp input and ground. Since the ALBO-diode conductance is directly proportional to the ALBO-diode current, and the ALBO diode is driven by the peak detector, any signal in excess of that required to trip the peak detector will be shunted to ground through the ALBO diode. This automatic-gain-control function maintains the signal at the optimum level to operate the clock and data detectors.

The combination of R_S and R_A, in parallel with both C_A and the series impedance of the ALBO diode, perform the following two functions: 1) the automatic-gain-control function previously described, and 2) the frequency/phase compensation for transmission-line losses.

FREQUENCY/PHASE COMPENSATION

Frequency/phase compensation is desirable for three reasons:

1. If the bandwidth is wider than necessary, noise and crosstalk outside of the signal-frequency band will appear at the threshold detectors. Out-of-band signals increase the probability that an incorrect logic decision will be made. These incorrect logic decisions will increase the bit error rate.
2. Nonlinear phase-shifts in the transmission line may cause the signal to be distorted to the extent that bit errors occur. Phase compensation in the repeater can partly correct for this problem.
3. Large phase-shifts in the preamplifier at high frequencies can cause instability if not compensated for by the feedback network. (See Figures 4 and 5).

CLOCK DETECTOR

The clock detector drives the clock-tank circuit with a pulse each time that the incoming signal is greater than 73% of the average peak signal.

PEAK DETECTOR

The peak detector drives the ALBO buffer and ALBO diode at the peak of the amplified "1" bits. Whenever the preamp AC-signal-output exceeds about 1.5V peak-to-peak, the ALBO buffer becomes forward biased and drives current into both the ALBO diode and the ALBO filter. This closed-loop AGC action maintains the preamp input signal at about 5mVp-p.

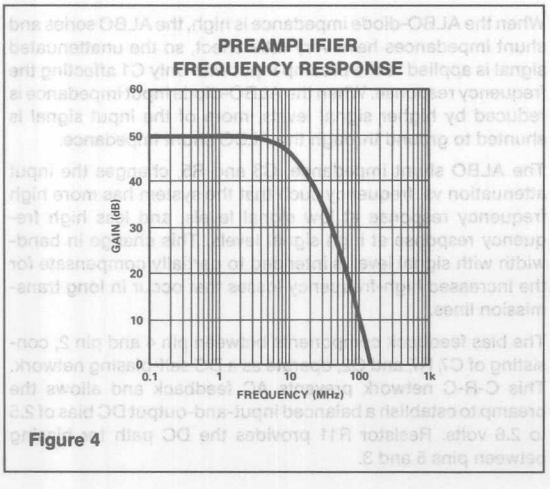


Figure 4

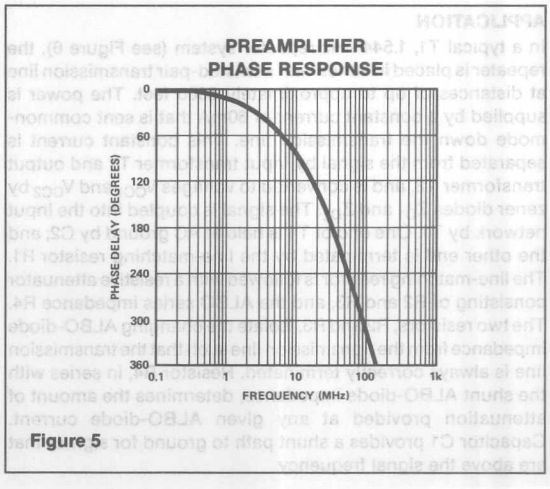


Figure 5

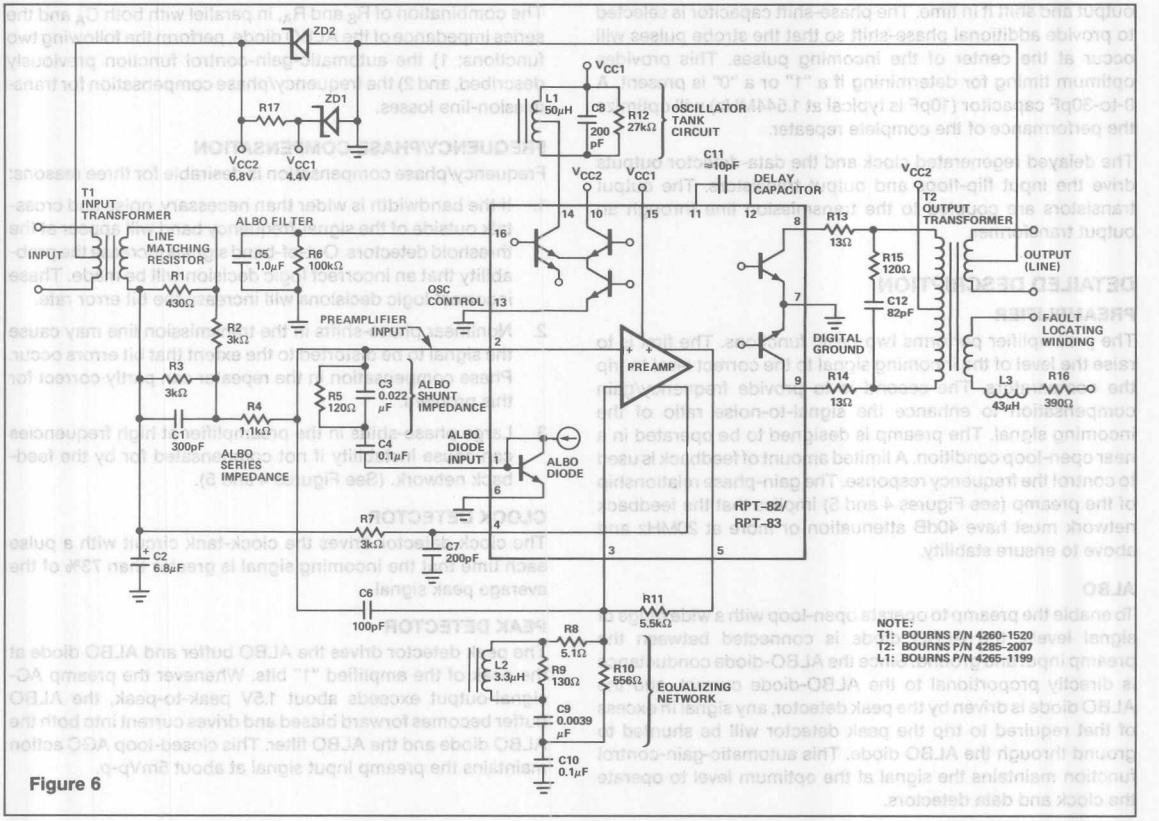


Figure 6

APPLICATION

In a typical T1, 1.544MHz repeater system (see Figure 6), the repeater is placed in series with a twisted-pair transmission line at distances of up to approximately 6000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T1 and output transformer T2, and is converted to voltages V_{CC1} and V_{CC2} by zener diodes Z_{D1} and Z_{D2}. The signal is coupled into the input network by T1. One end of T1 is held at AC ground by C2; and the other end is terminated by the line-matching resistor R1. The line-matching resistor is followed with a resistive attenuator consisting of R2 and R3, and the ALBO series impedance R4. The two resistors, R2 and R3, isolate the changing ALBO-diode impedance from the transmission line such that the transmission line is always correctly terminated. Resistor R4, in series with the shunt ALBO-diode impedance, determines the amount of attenuation provided at any given ALBO-diode current. Capacitor C1 provides a shunt path to ground for signals that are above the signal frequency.

When the ALBO-diode impedance is high, the ALBO series and shunt impedances have very little effect, so the unattenuated signal is applied to the preamp input with only C1 affecting the frequency response. When the ALBO-diode input impedance is reduced by higher signal levels, more of the input signal is shunted to ground through the ALBO shunt impedance.

The ALBO shunt impedance, C3 and R5, changes the input attenuation vs. frequency such that the system has more high frequency response at low signal levels, and less high frequency response at high signal levels. This change in bandwidth with signal level is intended to partially compensate for the increased high-frequency losses that occur in long transmission lines.

The bias feedback components between pin 4 and pin 2, consisting of C7, R7, and C2, operate as a DC self-biasing network. This C-R-C network prevents AC feedback and allows the preamp to establish a balanced input-and-output DC bias of 2.5 to 2.6 volts. Resistor R11 provides the DC path for biasing between pins 5 and 3.

Resistor R11 and capacitor C6 provide an AC feedback path. Resistors R10 and R11 act as an AC voltage divider that is shunted by the variable impedance of the resonant circuit comprised of L2 and C9. This frequency-selective feedback path, between pin 5 and pin 3, increases preamp gain at approximately 900kHz which further improves the system signal-to-noise ratio. The beneficial effect of the frequency-selective network is shown in Figure 7. The lower trace is a typical input signal (all 1's in this example) and the upper trace is the preamp output.

Figures 8 and 9 show the appearance of different preamp inputs measured at pin 5. Figure 8 is typical of an all 1's signal pattern with very little cross-talk or noise. Figure 9 shows a normal pattern of random 1's and 0's.

Due to the automatic-gain-control action of the ALBO circuitry, the peak amplitude is held constant for line losses of approximately 5dB to greater than 36dB. These signals are superimposed on a DC level of approximately 2.5V.

The preamp output drives the clock detector (reference Figures 2 and 6) which drives the clock-tank circuitry (L1, C8, and R12). The signal at pin 14, a sine wave of 0.2 to 1.0Vp-p (depending upon the percentage of 1-bits), drives the clock amplifier. The phase-shift capacitor, C11, provides the additional phase shift so that this integrated and phase-shifted signal (Figure 10) will strobe the output flip-flops at the optimum time to determine if a 1-bit is present. If a 1-bit is present, outputs from the data detector and the strobe cause the flip-flops to drive alternate output transistors. This signal is coupled through the output transformer into the next section of transmission line (see Figure 11, all 1's; and Figure 12, a random 1-0 pattern).

Figure 13 is a scope photograph of the signals as observed at several locations in the system. All traces are DC coupled and referenced to zero volts at the bottom graticule line. All signals, except the output, are displayed at 1-volt-per-division. The output is shown at 2-volts-per-division. The signal is all 1's. The phase relationships are typical for this type of repeater.

The signals shown are:

1. The preamp output at pin 5.
2. The clock-tank at pin 14.
3. The phase-shifted clock at pin 11.
4. The output signal at pin 8.

R13, 14, 15, and C12 control ringing and overshoot in the output waveform.

The fault-locating winding with L3 and R16 is used in long-line systems to determine which repeater, in a large series of repeaters, has become defective.

The RPT-82 and RPT-83 can be used in a variety of systems over a wide range of frequencies. The low-frequency response is limited by the difficulty in maintaining useable Q in the clock-tank circuit and by transformer-coupling losses. At high frequencies, the major limitation is the output-pulse rise-and-fall time.

The preamp is a high-gain, wide-bandwidth linear amplifier. Analog circuits do not have the noise rejection that is common with most digital circuits. To obtain best performance, certain precautions should be observed.

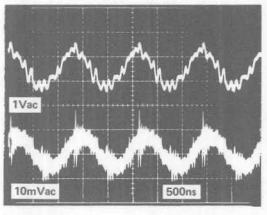


Figure 7

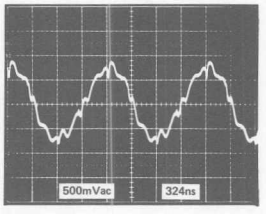


Figure 8

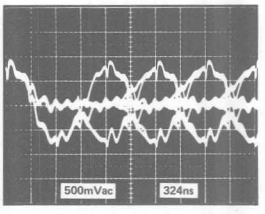


Figure 9

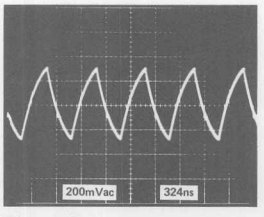


Figure 10

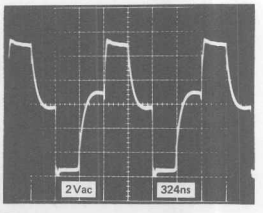


Figure 11

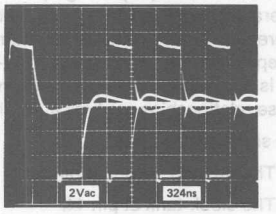


Figure 12

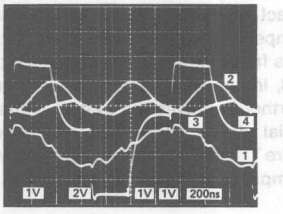


Figure 13

Circuit layout techniques used for R.F. amplifiers should be followed. Use of double-sided boards with all unused circuit-board area made into a ground plane is highly recommended. Keep input and output leads as far apart as possible, and signal runs as short as possible. Locate the attenuator network and the ALBO series impedance R4 as close to pin 2 as possible.

Power supply voltages V_{CC1} and V_{CC2} should be bypassed near pins 10 and 15. A bypass capacitor between the V_{CC2} connection on T_2 and pin 7 is also recommended.

PCM Repeater

RPT-85

FEATURES

- **Automatic ALBO Function**
- **Low-Power Operation (100mW)**
- **Wide Data Rate Range <100 kbit/s to >3 Mbit/s**
- **Compatible with T1, CEPT/E1, and T1C Systems**
- **Pin Compatible with XR-T445**

ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP	SO	
RPT-85FQ†	RPT-85FS††	XIND

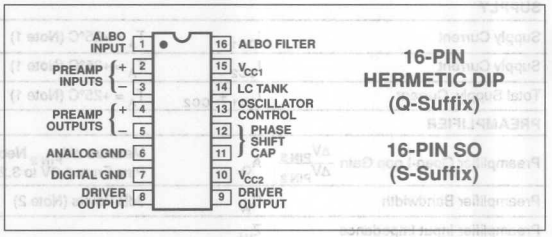
† Burn-in is available on extended industrial temperature range parts in CerDIP.
†† For availability and burn-in information on SO packages, contact your local sales office.

GENERAL DESCRIPTION

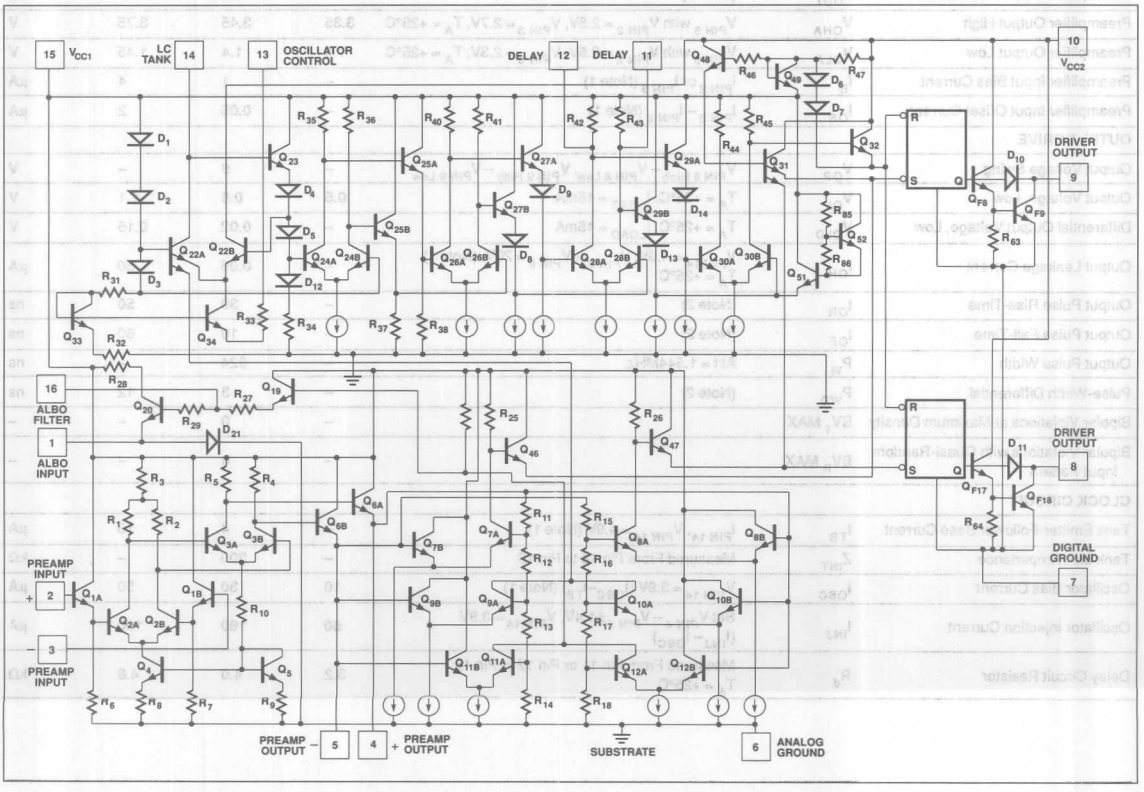
The RPT-85 is an integrated circuit that performs the active functions required for regenerative PCM repeaters. It can operate from less than 100kHz to greater than 3MHz. In PCM systems, information is transmitted by the presence or absence of bipolar pulses in specified time slots. The RPT-85 repeater automatically adjusts gain to optimize signal levels, determines if a pulse is present or not, and retransmits the reconstructed pulses.

For higher dynamic range performance and single supply designs, see RPT-86 and RPT-87.

PIN CONNECTIONS



RPT-85 SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Pin 10 to Pin 7 or 6 ..... 16.0V, –0.2V
Pin 15 to Pin 7 or 6 ..... 8.0V, –0.2V
Maximum Voltage at Pins 8 or 9 ..... 30V, –0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14 ..... V_{CC2}
Maximum Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature ..... 300°C
Junction Temperature ..... 150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin SO (S)	111	35	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{CC1} = 4.4V, V_{CC2} = 6.8V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

$V_{PIN\ 6} = V_{PIN\ 7} = V_{PIN\ 13}$ = GND.

PARAMETER	SYMBOL	CONDITIONS	RPT-85 MIN	RPT-85 TYP	RPT-85 MAX	UNITS
SUPPLY						
Supply Current	I_{CC1}	T_A = +25°C (Note 1)	5.0	8.5	9.5	mA
Supply Current	I_{CC2}	T_A = +25°C (Note 1)	1.0	2.5	3.5	mA
Total Supply Current	$I_{CC1} + I_{CC2}$	T_A = +25°C (Note 1)	6	11	13	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain $\frac{\Delta V_{PIN\ 5}}{\Delta V_{PIN\ 2}}$	A_O	Measure $\Delta V_{PIN\ 2}$ Necessary to Change Pins From 1.9V to 3.2V	44	48	53	dB
Preamplifier Bandwidth	B_W	3dB Points (Note 2)	3	5	–	MHz
Preamplifier Input Impedance	Z_{IN}		–	600	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	$V_{PIN\ 2} - V_{PIN\ 3}$ (Note 1)	–	1	15	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	–	80	150	Ω
Preamplifier Output High	V_{OHA}	$V_{PIN\ 5}$ with $V_{PIN\ 2}$ = 2.5V, $V_{PIN\ 3}$ = 2.7V, T_A = +25°C	3.35	3.45	3.75	V
Preamplifier Output Low	V_{OLA}	$V_{PIN\ 5}$ with $V_{PIN\ 2}$ = 2.5V, $V_{PIN\ 3}$ = 2.3V, T_A = +25°C	1.0	1.4	1.45	V
Preamplifier Input Bias Current	I_B	$I_{PIN\ 2}$ or $I_{PIN\ 3}$ (Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	$I_{PIN\ 2} - I_{PIN\ 3}$ (Note 1)	–	0.05	2	µA
OUTPUT DRIVE						
Output Voltage Swing	V_{OP}	$V_{PIN\ 8\ High} - V_{PIN\ 8\ Low}$, $V_{PIN\ 9\ High} - V_{PIN\ 9\ Low}$	–	6	–	V
Output Voltage, Low	V_{OL}	T_A = +25°C, I_{LOAD} = 15mA	0.5	0.8	1.1	V
Differential Output Voltage, Low	V_{OLD}	T_A = +25°C, I_{LOAD} = 15mA	–	0.02	0.15	V
Output Leakage Current	I_{OH}	$V_{PIN\ 14}$ = 4.9V, $V_{PIN\ 8} = V_{PIN\ 9}$ = 20V, (Note 1) T_A = +25°C	–	0.05	50	µA
Output Pulse Rise-Time	t_{OR}	(Note 2)	–	30	50	ns
Output Pulse Fall-Time	t_{OF}	(Note 2)	–	10	60	ns
Output Pulse Width	P_W	At f = 1.544MHz	–	324	–	ns
Pulse-Width Differential	P_{WD}	(Note 2)	–	3	12	ns
Bipolar Violations at Maximum Density	BV_1 MAX		–	0	–	–
Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX		–	0	–	–
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{PIN\ 14}$, $V_{PIN\ 14}$ = 4.9V (Note 1)	–	4	15	µA
Tank Input Impedance	Z_{INT}	Measured From Pin 14 to Pin 15	–	300	–	kΩ
Oscillator Bias Current	I_{OSC}	$V_{PIN\ 14}$ = 3.9V (I_{OSC}–I_{TB}) (Note 1)	10	30	50	µA
Oscillator Injection Current	I_{INJ}	Set $V_{PIN\ 4} - V_{PIN\ 5}$ ±1.4V, $V_{PIN\ 14}$ = 3.9V ($I_{INJ} - I_{OSC}$)	60	160	190	µA
Delay Circuit Resistor	R_d	Measured From Pin 11 or Pin 12 to Pin 15, T_A = +25°C	3.2	4.0	4.8	kΩ

ELECTRICAL CHARACTERISTICS at V_{CC1} = 4.4V, V_{CC2} = 6.8V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. $V_{PIN\ 6} = V_{PIN\ 7} = V_{PIN\ 13}$ = GND. *Continued*

PARAMETER	SYMBOL	CONDITIONS	RPT-85 MIN	RPT-85 TYP	RPT-85 MAX	UNITS
MISCELLANEOUS						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to activate the Peak Detector. T_A = +25°C	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector. T_A = +25°C	0.85	1.0	1.2	V
Data Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector. T_A = +25°C	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$	T_A = +25°C	67	73	78	%
Data Threshold as % of ALBO Voltage	$V_{TL\%}$	T_A = +25°C	46	54	58	%
ALBO ON Voltage	V_{O16}	Measured at Pin 16, [$V_{PIN\ 4} – V_{PIN\ 5}$] = ALBO Threshold	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at Pin 16 and Pin 1 T_A = +25°C (Note 1)	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN		–	8	–	Ω
Maximum ALBO Diode Impedance	R_D MAX	f = 1.544MHz	–	30	–	kΩ
ALBO Gain Range	A_m	(Note 3)	36	48	–	dB

NOTES:
1. $V_{PIN\ 2}$ = 2.5V; adjust $V_{PIN\ 3}$ until $V_{PIN\ 4} = V_{PIN\ 5}$.
2. Sample tested.
3. Guaranteed by design.

FUNCTIONAL DESCRIPTION

Bipolar-pulse transmission, the transmission of alternately positive and negative pulses, is used on repeater lines to remove the DC component present in unipolar PCM pulse trains. This also places the principal energy components in the 0–1.544MHz band, as opposed to the 0–3.088MHz band for unipolar pulse trains. The absence of a DC component in bipolar pulse trains permits the repeater to be transformer-coupled to the repeater line and helps prevent time-shifting of the regenerator firing levels with variations in input pulse density (see Figure 1).

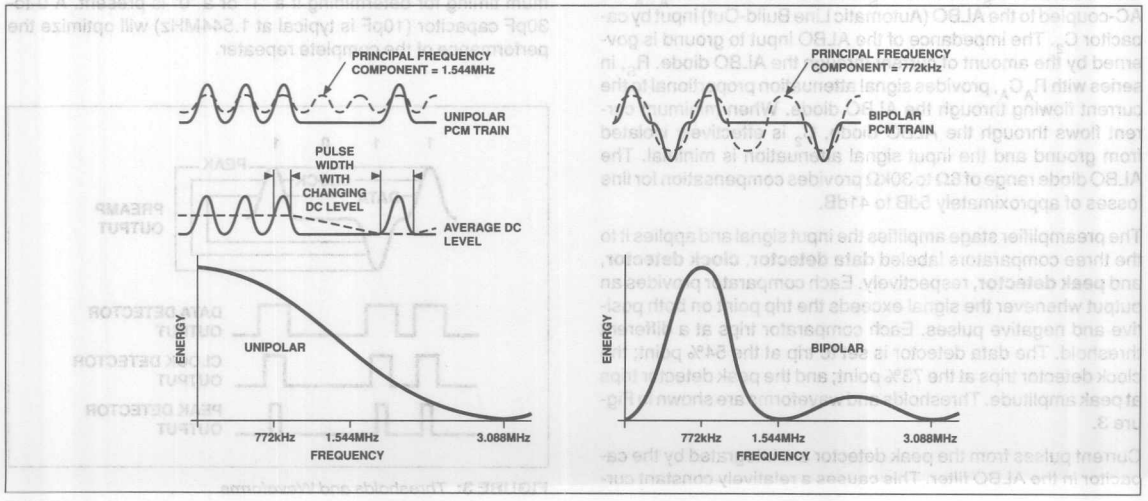


FIGURE 1: *Energy Spectra of Bipolar and Unipolar Pulse Trains*

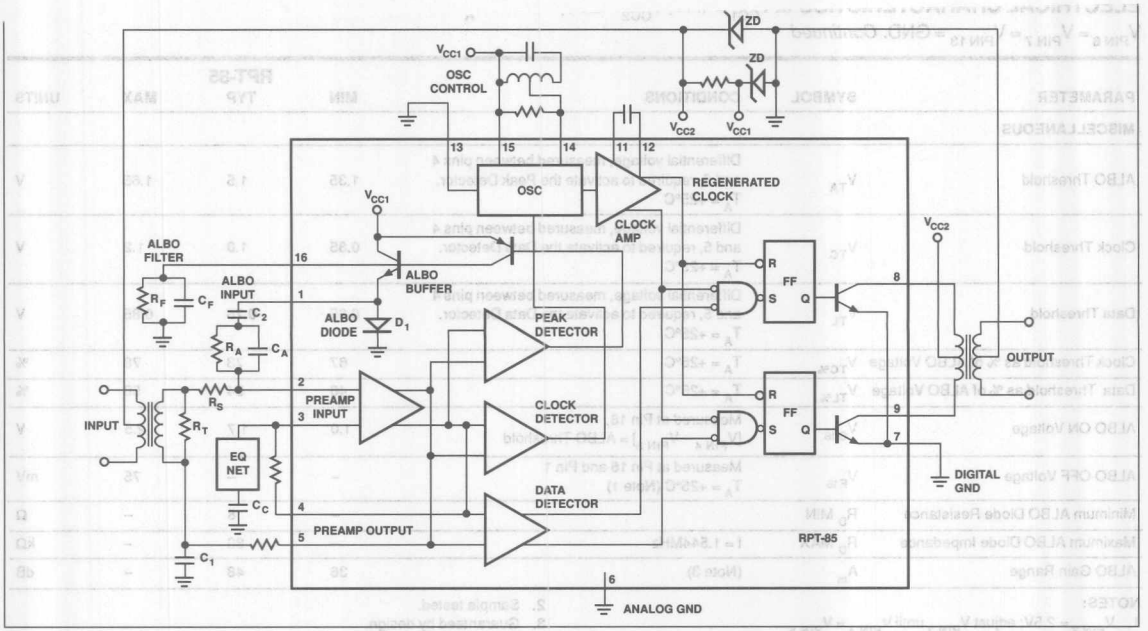


FIGURE 2: *Functional Block Diagram*

The bipolar-PCM pulse train is transformer-coupled into the preamplifier as shown in the functional block diagram (Figure 2). The secondary of the input transformer is loaded with the proper terminating resistor, R_T, to match the line impedance. One side of the transformer secondary is AC-coupled to ground by capacitor C_1; the other side of the secondary winding is in series with resistance R_S. Resistor R_S and the RC network R_AC_A are AC-coupled to the ALBO (Automatic Line Build-Out) input by capacitor C_2. The impedance of the ALBO input to ground is governed by the amount of current through the ALBO diode. R_S, in series with R_AC_A, provides signal attenuation proportional to the current flowing through the ALBO diode. When minimum current flows through the ALBO diode, C_2 is effectively isolated from ground and the input signal attenuation is minimal. The ALBO diode range of 8Ω to 30kΩ provides compensation for line losses of approximately 5dB to 41dB.

The preamplifier stage amplifies the input signal and applies it to the three comparators labeled **data detector**, **clock detector**, and **peak detector**, respectively. Each comparator provides an output whenever the signal exceeds the trip point on both positive and negative pulses. Each comparator trips at a different threshold. The data detector is set to trip at the 54% point; the clock detector trips at the 73% point; and the peak detector trips at peak amplitude. Thresholds and waveforms are shown in Figure 3.

Current pulses from the peak detector are integrated by the capacitor in the ALBO filter. This causes a relatively constant current to flow through the emitter follower and D_1.

The clock detector output locks the oscillator to the input frequency. The following amplifier stages shape the oscillator output and shift it in time. The phase-shift capacitor is selected to provide additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses. This provides optimum timing for determining if a "1" or a "0" is present. A 0-to-30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

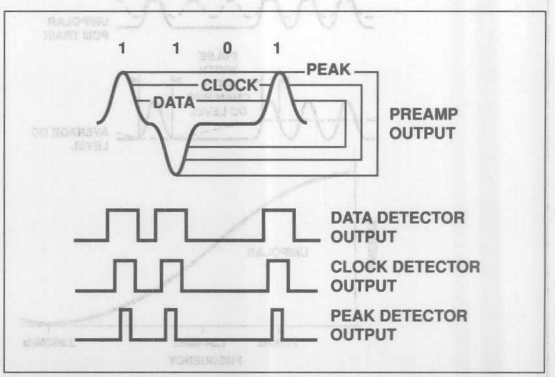


FIGURE 3: *Thresholds and Waveforms*

The delayed regenerated clock and the data-detector outputs drive the input flip-flops and output transistors. The output transistors are coupled to the transmission line through an output transformer.

DETAILED DESCRIPTION

PREAMPLIFIER

The preamplifier performs two basic functions. The first is to raise the level of the incoming signal to the correct level to trip the comparators. The second is to provide frequency/gain compensation to enhance the signal-to-noise ratio of the incoming signal. The preamp is designed to be operated in a near open-loop condition. A limited amount of feedback is used to control the frequency response. The gain-phase relationship of the preamp (see Figures 4 and 5) implies that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

ALBO

To enable the preamp to operate open-loop with a wide range of signal levels, the ALBO diode is connected between the preamp input and ground. Since the ALBO-diode conductance is directly proportional to the ALBO-diode current, and the ALBO diode is driven by the peak detector, any signal in excess of that required to trip the peak detector will be shunted to ground through the ALBO diode. This automatic-gain-control function maintains the signal at the optimum level to operate the clock and data detectors.

The combination of R_S and R_A, in parallel with both C_A and the series impedance of the ALBO diode, perform the following two functions: 1) the automatic-gain-control function previously described, and 2) the frequency/phase compensation for transmission line losses.

FREQUENCY/PHASE COMPENSATION

Frequency/phase compensation is desirable for three reasons:

1. If the bandwidth is wider than necessary, noise and crosstalk outside of the signal-frequency band will appear at the threshold detectors. Out-of-band signals increase the probability that an incorrect logic decision will be made. These incorrect logic decisions will increase the bit error rate.
2. Nonlinear phase-shifts in the transmission line may cause the signal to be distorted to the extent that bit errors occur. Phase compensation in the repeater can partly correct for this problem.
3. Large phase-shifts in the preamplifier at high frequencies can cause instability if not compensated for by the feedback network (see Figures 4 and 5).

CLOCK DETECTOR

The clock detector drives the clock-tank circuit with a pulse each time that the incoming signal is greater than 73% of the average peak signal.

PEAK DETECTOR

The peak detector drives the ALBO buffer and ALBO diode at the peak of the amplified "1" bits. Whenever the preamp AC-sigal-output exceeds about 1.5V peak-to-peak, the ALBO buffer becomes forward biased and drives current into both the ALBO diode and the ALBO filter. This closed-loop AGC action maintains the preamp input signal at about $5mV_{p-p}$.

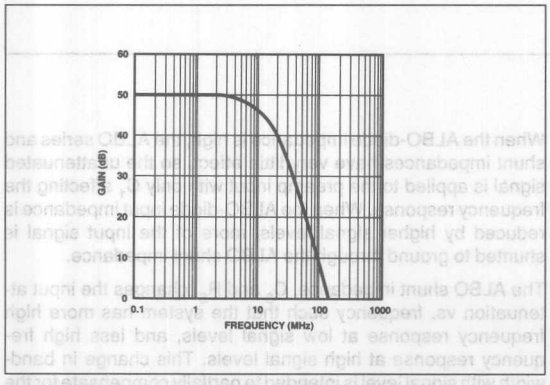


FIGURE 4: *Preamplifier Frequency Response*

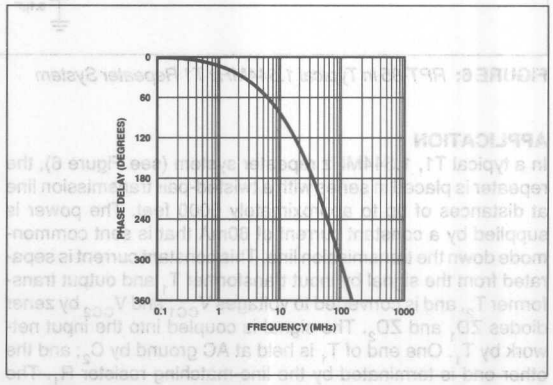


FIGURE 5: *Preamplifier Phase Response*

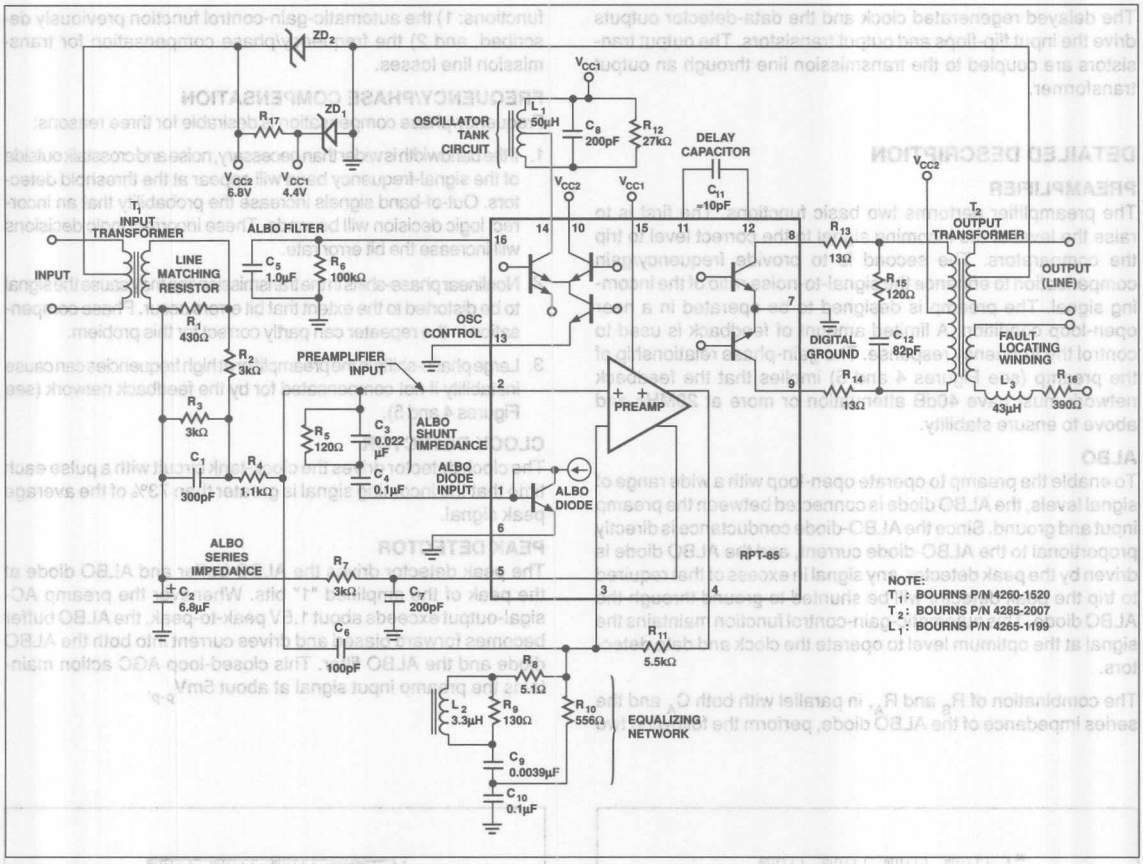


FIGURE 6: *RPT-85 in Typical 1.544MHz T1 Repeater System*

APPLICATION

In a typical T1, 1.544MHz repeater system (see Figure 6), the repeater is placed in series with a twisted-pair transmission line at distances of up to approximately 6000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T_1 and output transformer T_2, and is converted to voltages V_{CC1} and V_{CC2} by zener diodes ZD_1 and ZD_2. The signal is coupled into the input network by T_1. One end of T_1 is held at AC ground by C_2; and the other end is terminated by the line-matching resistor R_1. The line-matching resistor is followed with a resistive attenuator consisting of R_2 and R_3, and the ALBO series impedance R_4. The two resistors, R_2 and R_3, isolate the changing ALBO-diode impedance from the transmission line such that the transmission line is always correctly terminated. Resistor R_4, in series with the shunt ALBO-diode impedance, determines the amount of attenuation provided at any given ALBO-diode current. Capacitor C_1 provides a shunt path to ground for signals that are above the signal frequency.

When the ALBO-diode impedance is high, the ALBO series and shunt impedances have very little effect, so the unattenuated signal is applied to the preamp input with only C_1 affecting the frequency response. When the ALBO-diode input impedance is reduced by higher signal levels, more of the input signal is shunted to ground through the ALBO shunt impedance.

The ALBO shunt impedance, C_3 and R_5, changes the input attenuation vs. frequency such that the system has more high frequency response at low signal levels, and less high frequency response at high signal levels. This change in bandwidth with signal level is intended to partially compensate for the increased high-frequency losses that occur in long transmission lines.

The bias feedback components between pin 5 and pin 2, consisting of C_7, R_7, and C_2, operate as a DC self-biasing network. This C-R-C network prevents AC feedback and allows the preamp to establish a balanced input-and-output DC bias of 2.5 to 2.6 volts. Resistor R_{11} provides the DC path for biasing between pins 4 and 3.

Resistor R_{11} and capacitor C_6 provide an AC feedback path. Resistors R_{10} and R_{11} act as an AC voltage divider that is shunted by the variable impedance of the resonant circuit comprising L_2 and C_9. This frequency-selective feedback path, between pin 4 and pin 3, increases preamp gain at approximately 900kHz which further improves the system signal-to-noise ratio. The beneficial effect of the frequency-selective network is shown in Figure 7. The lower trace is a typical input signal (all 1's in this example) and the upper trace is the preamp output.

Figures 8 and 9 show the appearance of different preamp inputs measured at pin 4. Figure 8 is typical of an all 1's signal pattern with very little crosstalk or noise. Figure 9 shows a normal pattern of random 1's and 0's.

Due to the automatic-gain-control action of the ALBO circuitry, the peak amplitude is held constant for line losses of approximately 5dB to greater than 36dB. These signals are superimposed on a DC level of approximately 2.5V.

The preamp output drives the clock detector (reference Figures 2 and 6) which drives the clock-tank circuitry (L_1, C_8, and R_{12}). The signal at pin 14, a sine wave of 0.2 to 1.0V_{p-p} (depending upon the percentage of 1-bits), drives the clock amplifier. The phase-shift capacitor, C_{11}, provides the additional phase shift so that this integrated and phase-shifted signal (Figure 10) will strobe the output flip-flops at the optimum time to determine if a 1-bit is present. If a 1-bit is present, outputs from the data detector and the strobe cause the flip-flops to drive alternate output transistors. This signal is coupled through the output transformer into the next section of transmission line (see Figure 11, all 1's; and Figure 12, a random 1-0 pattern).

Figure 13 is a scope photograph of the signals as observed at several locations in the system. All traces are DC coupled and referenced to zero volts at the bottom graticule line. All signals, except the output, are displayed at 1-volt-per-division. The output is shown at 2-volts-per-division. The signal is all 1's. The phase relationships are typical for this type of repeater.

The signals shown are:

1. The preamp output at pin 4.
2. The clock-tank at pin 14.
3. The phase-shifted clock at pin 11.
4. The output signal at pin 8.

R_{13}, R_{14}, R_{15} and C_{12} control ringing and overshoot in the output waveform.

The fault-locating winding with L_3 and R_{16} is used in long-line systems to determine which repeater, in a large series of repeaters, has become defective.

The RPT-85 can be used in a variety of systems over a wide range of frequencies. The low-frequency response is limited by the difficulty in maintaining useable Q in the clock-tank circuit and by transformer-coupling losses. At high frequencies, the major limitation is the output-pulse rise-and-fall time.

The preamp is a high-gain, wide-bandwidth linear amplifier. Analog circuits do not have the noise rejection that is common with most digital circuits. To obtain best performance, certain precautions should be observed.

Circuit layout techniques used for R.F. amplifiers should be followed. Use of double-sided boards with all unused circuitboard area made into a ground plane is highly recommended. Keep input and output leads as far apart as possible, and signal runs as short as possible. Locate the attenuator network and the ALBO series impedance R_4 as close to pin 2 as possible.

Power supply voltages V_{CC1} and V_{CC2} should be bypassed near pins 10 and 15. A bypass capacitor between the V_{CC2} connection on T_2 and pin 7 is also recommended.

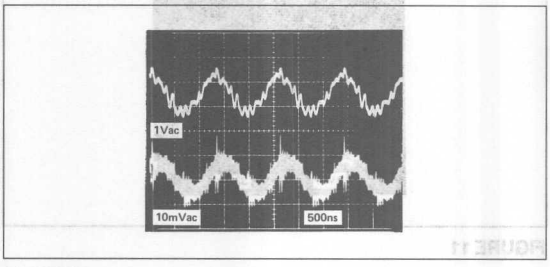


FIGURE 7

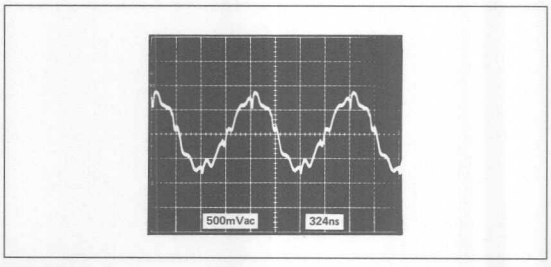


FIGURE 8

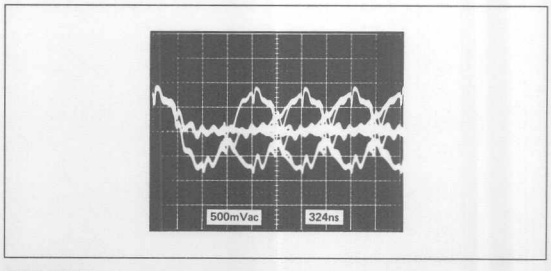


FIGURE 9

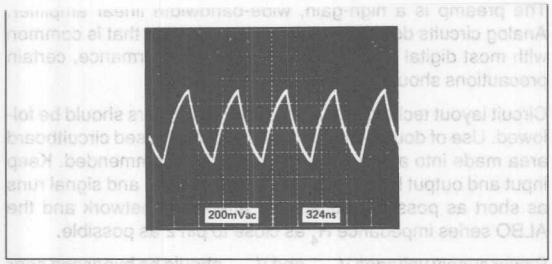


FIGURE 10

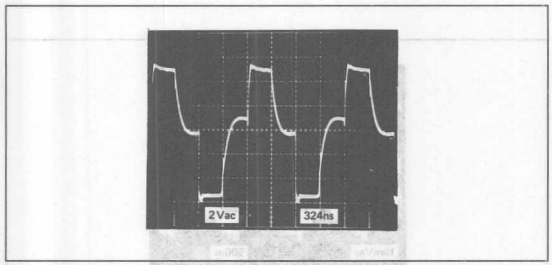


FIGURE 11

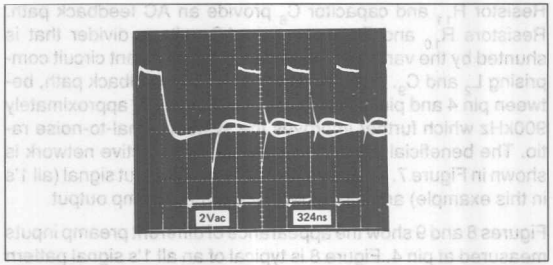


FIGURE 12

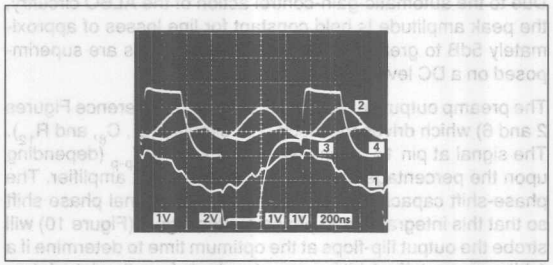


FIGURE 13

FEATURES

- **Low Power Consumption (56mW)**
- **Single-Supply Operation**
- **Wide Data Rate Range <100kbit/s to >3Mbit/s**
- **Dual ALBO Diodes; Dynamic Range >50dB**
- **Clock-Shutdown Circuit (RPT-87)**

ORDERING INFORMATION†

PACKAGE			OPERATING TEMPERATURE
CERDIP	PLASTIC	SO	RANGE
RPT86FQ	RPT86FP	RPT86FS††	XIND
RPT87FQ	RPT87FP	RPT87FS††	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

GENERAL DESCRIPTION

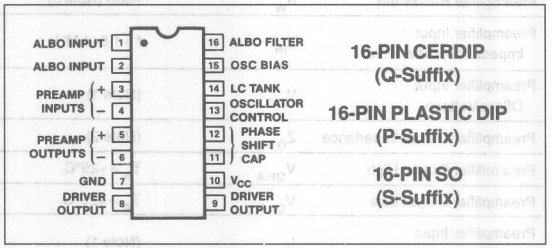
The RPT-86 and RPT-87 are monolithic repeater circuits containing all the active functions required in regenerative PCM repeaters. These devices automatically adjust gain to optimize signal levels, determine if a pulse is present, and re-transmit the reconstructed pulses. The RPT-86 and RPT-87 operate at data rates from under 100kbit/s to over 3Mbit/s and are compatible with T1 (1.544Mbit/s), CEPT/E1 (2.048Mbit/s), and T1C (3.152Mbit/s) systems.

A key feature of the RPT-86/RPT-87 repeaters is the ability to operate on a single supply of 5.6V with a typical quiescent supply current of only 10mA. In addition, the RPT-86 and RPT-87 have two Automatic Line Build-Out (ALBO) diodes coupled with a high-gain preamplifier that allows for a dynamic input signal range exceeding 50dB.

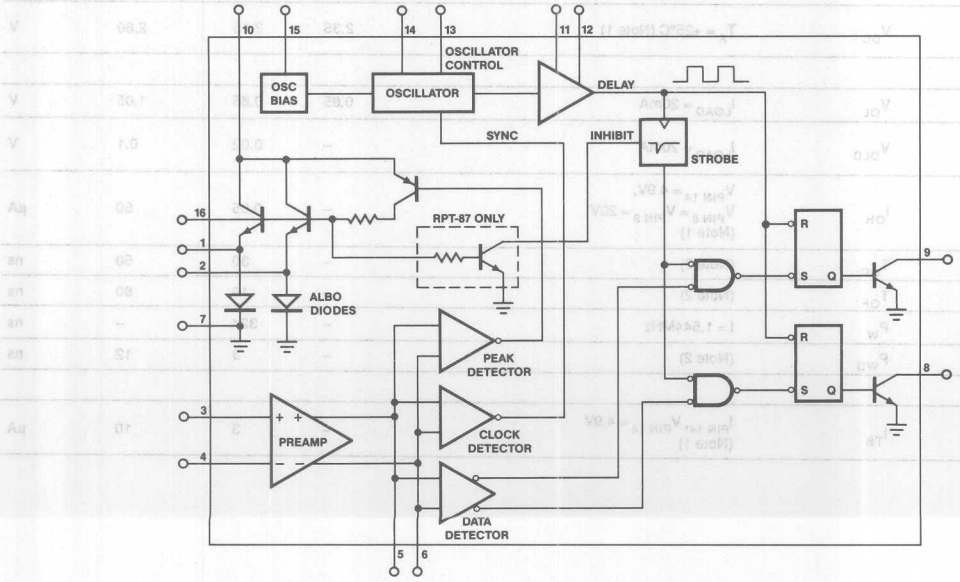
The RPT-87 also contains a clock-shutdown circuit. This shutdown circuit senses the incoming signal level and disables the clock drive to the output latches if the incoming signal is below the level where accurate pulse reconstruction is possible. This prevents noise or crosstalk from being mistaken as valid data and retransmitted.

4

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Pin 10 to Pin 7, 20ms Pulse, Duty Cycle ≤0.05 ..... 35V, –1.0V
Voltage Pin 10 to Pin 7, Continuous 50Hz Half-Wave Sinusoid ..... 25V, –1.0V
Pin 10 to Pin 7, Continuously ..... 13.5V, –0.7V
Voltage Pins 8 or 9 to Pin 7, Continuously ..... 35V, –1.0V
Voltage Pins 3,4,5,6,11,12,14 to Pin 7 ..... V_{CC}
Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature ..... 300°C
Junction Temperature ..... 150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
16-Pin SO (S)	111	35	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{CC} = 5.6V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. $V_{PIN\ 7}$ = $V_{PIN\ 13}$ = GND.

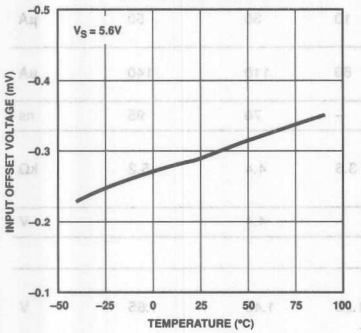
PARAMETER	SYMBOL	CONDITIONS	RPT-86F/RPT-87F MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC}	(Note 1)	5	9.8	10.5	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A_O		46	49	54	dB
Preamplifier Bandwidth	B_W	–3dB (Note 3)	3	5	–	MHz
Preamplifier Input Impedance, Differential	Z_{IN}	f = 1.544 MHz	–	50	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	(Note 1)	–	0.5	2.5	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	–	200	300	Ω
Preamplifier Output High	V_{OHA}	T_A = +25°C	3.30	3.50	–	V
Preamplifier Output Low	V_{OLA}	T_A = +25°C	–	1.20	1.45	V
Preamplifier Input Bias Current	I_B	(Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	(Note 1)	–	0.01	0.1	µA
Preamplifier Output Self-Bias Voltage	V_{DC}	T_A = +25°C (Note 1)	2.35	2.45	2.60	V
OUTPUT DRIVE						
Output Voltage Low	V_{OL}	I_{LOAD} = 20mA	0.65	0.85	1.05	V
Differential Output Voltage, Low	V_{OLD}	I_{LOAD} = 20mA	–	0.02	0.1	V
Output Leakage Current	I_{OH}	$V_{PIN\ 14}$ = 4.9V, $V_{PIN\ 8}$ = $V_{PIN\ 9}$ = 20V (Note 1)	–	0.05	50	µA
Output Pulse Rise-Time	T_{OR}	(Note 2)	–	30	50	ns
Output Pulse Fall-Time	T_{OF}	(Note 2)	–	10	60	ns
Output Pulse Width	P_W	f = 1.544MHz	–	324	–	ns
Pulse-Width Differential	P_{WD}	(Note 2)	–	3	12	ns
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{PIN\ 14}$, $V_{PIN\ 14}$ = 4.9V (Note 1)	–	3	10	µA

ELECTRICAL CHARACTERISTICS at V_{CC} = 5.6V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. $V_{PIN\ 7} = V_{PIN\ 13}$ = GND. *Continued*

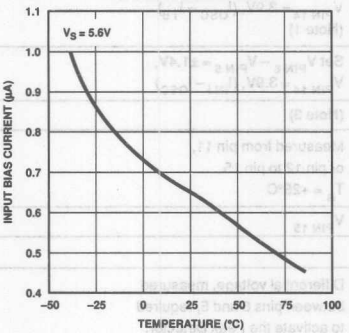
PARAMETER	SYMBOL	CONDITIONS	RPT-86F/RPT-87F MIN	TYP	MAX	UNITS
Oscillator Bias Current	I_{OSC}	$V_{PIN\ 14}$ = 3.9V, ($I_{OSC} - I_{TB}$) (Note 1)	10	30	50	µA
Oscillator Injection Current	I_{INJ}	Set $V_{PIN\ 6} - V_{PIN\ 5} = \pm 1.4V$, $V_{PIN\ 14}$ = 3.9V, ($I_{INJ} - I_{OSC}$)	80	110	140	µA
Data Sampling Interval	T_{DS}	(Note 3)	–	70	95	ns
Delay Circuit Resistor	R_d	Measured from pin 11, or pin 12 to pin 15 T_A = +25°C	3.6	4.4	5.2	kΩ
Oscillator Bias Voltage	V_{BIAS}	$V_{PIN\ 15}$	–	4.4	–	V
ALBO						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 6 and 5, required to activate the Peak Detector.	1.25	1.45	1.65	V
ALBO Threshold ± Differential	V_{TAD}		–	–	100	mV
ALBO ON Voltage	V_{O16}	Measured at pin 16, [$V_{PIN\ 6} - V_{PIN\ 5}$] = ALBO Threshold + 20mV	1.0	1.6	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16, pin 1, and pin 2 (Note 1)	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN	Forced ΔI of 6 mA to 7 mA, measure voltage at pins 1 and 7, Calculate R_D by 1/2.	–	6	10	Ω
Maximum ALBO Diode Resistance	R_D MAX	f = 1.544MHz (Note 4)	20	30	–	kΩ
ALBO Diode Impedance Matching		$R_{DMIN} \leq R_D \leq R_{DMAX}$	–	10	–	%
DATA / CLOCK THRESHOLDS						
Clock Threshold	V_{TC}	Differential voltage, measured between pins 6 and 5, required to activate the Clock Detector.	0.85	1.0	1.15	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$		63	69	75	%
Data Threshold	V_{TL}	Differential voltage, measured between pins 6 and 5, required to activate the Data Detector.	0.65	0.75	0.85	V
Data Threshold as % of ALBO Voltage	$V_{TL\%}$		46	51	56	%

NOTES:
1. Preamplifier self-biased. $V_{PIN\ 3} \cong V_{PIN\ 4} \cong V_{PIN\ 5} \cong V_{PIN\ 6}$.
2. Sample tested.
3. Guaranteed by correlation to other tested parameters.
4. Guaranteed by design.

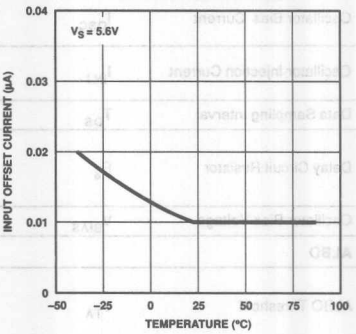
INPUT OFFSET VOLTAGE vs TEMPERATURE



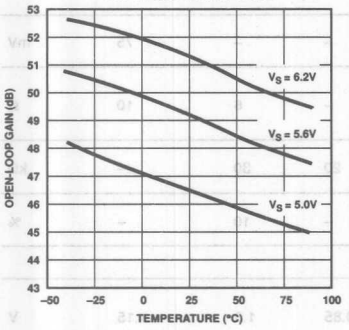
INPUT BIAS CURRENT vs TEMPERATURE



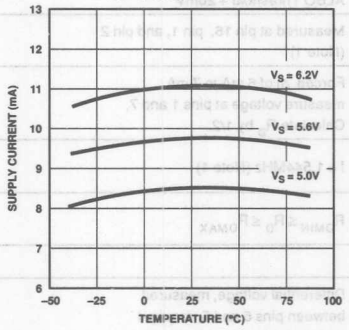
INPUT OFFSET CURRENT vs TEMPERATURE



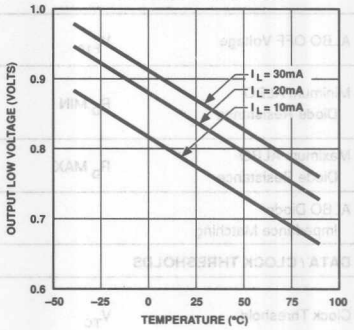
OPEN-LOOP GAIN vs TEMPERATURE



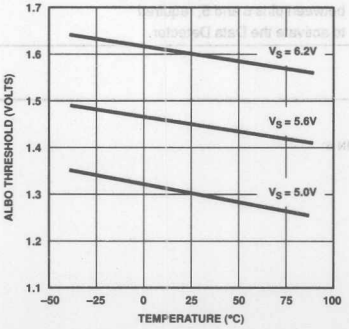
SUPPLY CURRENT vs TEMPERATURE



OUTPUT LOW VOLTAGE (V_{OL}) vs TEMPERATURE



ALBO THRESHOLD vs TEMPERATURE



FUNCTIONAL DESCRIPTION

The Preamplifier: The RPT-86 and RPT-87 repeater ICs contain a differential input, differential output preamplifier. From the differential input to the noninverting output, it behaves as a conventional op amp. The preamplifier has typically 5MHz, –3dB bandwidth. Its open-loop gain-phase frequency response is shown in Figure 1. In order to operate the preamplifier under a stable condition, some amount of external feedback is necessary to control the frequency response. The open-loop frequency response suggests that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

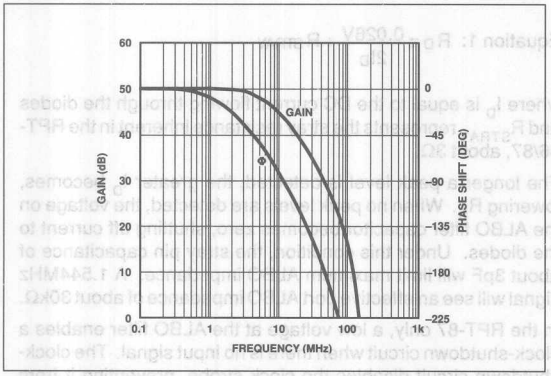


FIGURE 1: *Gain-Phase Frequency Response of the Preamplifier*

TABLE 1: Typical Preamp Gain/Phase Response

FREQUENCY (MHz)	AVOL(dB)	PHASE(DEG)
1.0	50	–12
1.544	50	–20
6.2	47	–60
20	39	–119
25.3	36.3	–135
45	29.5	–180

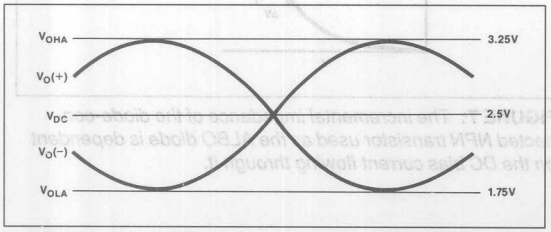


FIGURE 2: *The differential outputs of the RPT-86/87 preamplifier swing symmetrically around a DC bias point of about 2.5V. $V_O^{(-)}$ is inverted with respect to $V_O^{(+)}$ about this point.*

both its inputs and outputs. This allows the outputs to achieve maximum swing when amplifying an AC-coupled, bipolar signal. It also produces zero differential preamp output voltage for zero input signal. Operating from a +5.6V supply, the preamp outputs will balance at approximately +2.5V allowing an output voltage swing of ±0.75V around its bias level as illustrated in Figure 2.

Figures 3 and 4 show two methods of configuring the preamp to automatically self-bias both the inputs and outputs to an optimum level. The single resistor and capacitor used in Figure 3 extracts the DC average of the inverting output and feeds it back to the noninverting input to establish the input common-mode level. This negative feedback will force the outputs to center their swing around the DC level at which V_O(Diff) = 0V. This type of self-biasing is practical only when the preamp is passing a balanced, AC coupled, bipolar signal. If the preamp must preserve the DC level of an unbalanced, unipolar signal, then a self-biasing scheme as is shown in Figure 4 is required. This network sets the input common-mode level by establishing the DC average of both differential outputs. In this way, the input common-mode level will always be that voltage at which V_O(Diff) = 0V regardless of the input signal.

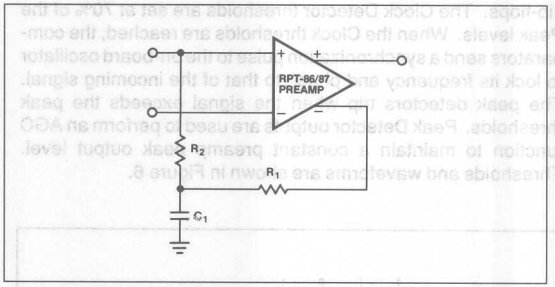


FIGURE 3: *Preamp self-biasing for use with AC coupled, balanced bipolar signals.*

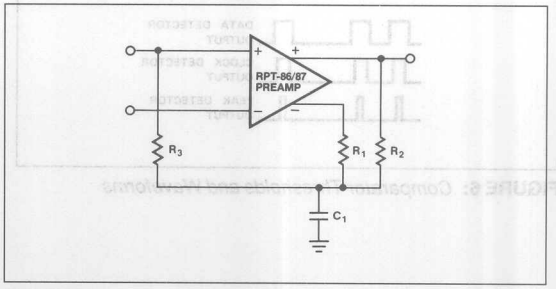


FIGURE 4: *Universal preamplifier self-biasing technique allowing unipolar signal amplification.*

Threshold Comparators: The RPT-86/87 contains three pairs of threshold comparators to monitor the differential outputs of the preamplifier. Each of the six comparators is set to detect a specific differential preamp output level. Three comparators measure positive differentials and three measure negative differentials. The individual threshold comparators are labeled as positive and negative Peak, Clock, and Data detector, as shown in Figure 5.

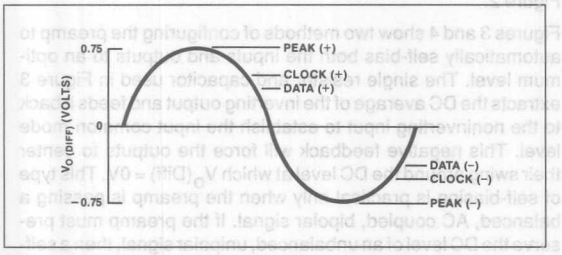


FIGURE 5: *Six threshold comparators detect positive and negative differential preamp output levels.*

The data Detector thresholds are set at 50% of the Peak levels for maximum noise immunity. The outputs of these comparators contain the digital data and are presented to the output R-S flip-flops. The Clock Detector thresholds are set at 70% of the Peak levels. When the Clock thresholds are reached, the comparators send a synchronization pulse to the on-board oscillator to lock its frequency and phase to that of the incoming signal. The peak detectors trip when the signal exceeds the peak thresholds. Peak Detector outputs are used to perform an AGC function to maintain a constant preamp peak output level. Thresholds and waveforms are shown in Figure 6.

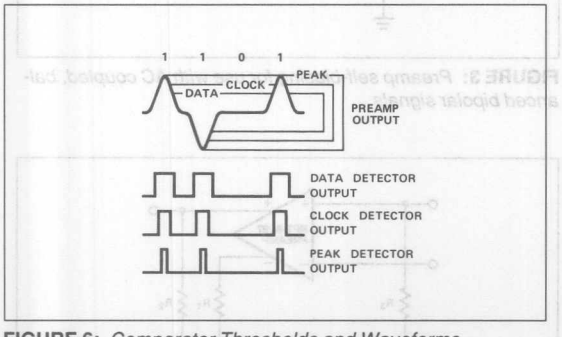


FIGURE 6: *Comparator Thresholds and Waveforms*

ALBO: The ALBO function is driven from the Peak threshold detector outputs. The ALBO (Automatic Line Build-Out) circuitry consists of two current-driven diodes which act as variable impedance elements enabling the RPT-86/87 to close an AGC loop around the preamplifier. As a peak level is detected, a current pulse is sourced into the ALBO diodes. These pulses are averaged to a DC current by an external ALBO filter capacitor. As the current flowing through the diodes increases, their incremental impedance is lowered as described by the exponential I-V curve for a diode-connected NPN transistor shown in Figure 7. The impedance of the NPN transistor emitters which source the current to the ALBO diodes follows an identical curve. Because the bases of these transistors look like an AC short to ground by virtue of the external ALBO filter capacitor, the total AC impedance of each ALBO port looks like the parallel combination of two diodes.

Equation 1: $$R_D \cong \frac{0.026V}{2I_D} + R_{STRAY}$$

where I_D is equal to the DC current flowing through the diodes and R_{STRAY} represents the stray resistance inherent in the RPT-86/87, about 3Ω.

The longer a peak level is detected, the greater I_D becomes, lowering R_D. When no peak levels are detected, the voltage on the ALBO filter capacitor becomes zero, shutting off current to the diodes. Under this condition, the stray pin capacitance of about 3pF will limit maximum ALBO impedance. A 1.544MHz signal will see an effective port ALBO impedance of about 30kΩ.

In the RPT-87 only, a low voltage at the ALBO filter enables a clock-shutdown circuit when there is no input signal. The clock-shutdown circuit disables the clock strobe, preventing it from latching the output flip-flops. This prevents the RPT-87 from sending false data that is triggered by noise or crosstalk when the incoming signal level is too low.

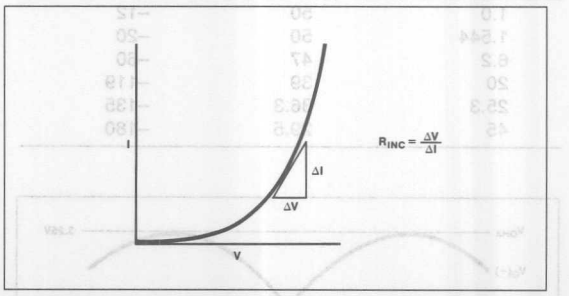


FIGURE 7: *The incremental impedance of the diode-connected NPN transistor used as the ALBO diode is dependent on the DC bias current flowing through it.*

The Oscillator: The RPT-86/87's on-board oscillator is designed to be free-running at a frequency, f_o, set by an external inductor and capacitor across pins 14 and 15, where $f_o = 1/(2\pi\sqrt{LC})$. The phase and exact frequency of the oscillator are synchronized to the incoming data signal by the Clock threshold comparators. Each time the preamplifier's differential output exceeds the Clock thresholds, the comparator's outputs inject a current pulse into the LC tank oscillator aligning its oscillation with the incoming signal. During periods where no Clock levels are detected by the comparators, the LC tank's oscillation will relax back to its own resonant frequency. An internal comparator is used to square the LC tank's sinusoidal oscillation into digital level clock. This comparator incorporates a delay function (a capacitor across pins 11 and 12) that provides additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses, thus allowing the user to control when the clock strobe will reach the output latches.This provides optimum timing for determining if a "1" or a "0" is present. A 0 to 30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

Data Output: When the incoming signal is detected as valid data, it is strobed into the two output R-S flip-flops. Their respective outputs are open-collector drivers that allows driving directly into a center-tapped isolation transformer. This recreates a full amplitude bipolar, AMI signal and transmits it down the next length of transmission line.

DESIGNING WITH THE RPT-86 AND RPT-87

DESIGNING A WIDEBAND AMPLIFIER

Figure 8 shows a typical configuration using the RPT-86/87's preamplifier to create a high-gain, wideband amplifier. The capacitor C_1 determines the amplifier's low frequency gain roll-off while resistors R_1 and R_2 set the AC closed-loop gain. At DC, the amplifier is in unity gain. A zero at $\omega_1 = 1/(R_2C_1)$ causes the AC gain to rise until a pole is reached at $\omega_2 = 1/(R_1C_2)$. The final value of closed-loop signal gain is equal to:

Equation 2: $$A_{VCL} = \frac{A_{VOL}}{1 + \left(\frac{A_{VOL}\,R_1}{R_2}\right)}$$

To ensure preamp stability, the ratio R_2/R_1 must be a minimum of 100 to a bandwidth of at least 20MHz. Low value resistors should be used for R_2 and R_1 to minimize the effects of stray capacitance in the feedback loop. Since PC board applications exhibit at least 2pF of stray feedback capacitance (equal to about 4kΩ impedance at 20MHz), R_1 should be less than 40Ω.

Because the preamp's differential output voltage is monitored by the internal threshold comparators, any output offset will degrade the symmetry of positive and negative threshold levels. Operating the preamplifier in DC unity gain is instrumental in minimizing the output offset voltage. Offset can be further reduced by balancing the preamp's DC input source impedance.

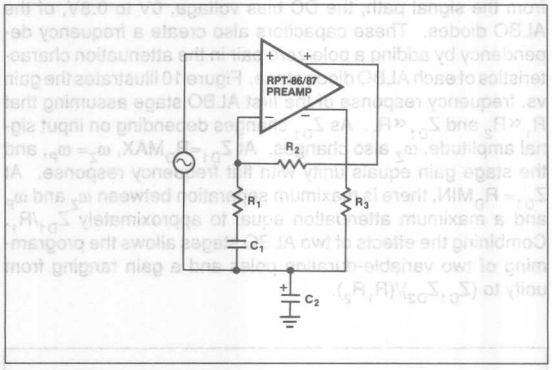


FIGURE 8: *Typical noninverting preamplifier gain configuration with self-biasing.*

Preamp output loading in the form of feedback and biasing networks should also be balanced to ensure uniform inverting action between the two preamp outputs.

AGC USING THE ALBO DIODES

The variable impedance action of the RPT-86/87's internal ALBO diodes can be used to create a wide dynamic range AGC loop with the preamplifiers as shown in Figure 9. While the preamp operates at a fixed AC gain, the input signal is variably attenuated by the impedance-divider networks of R_1/Z_{D1} and R_2/Z_{D2}. As the input signal magnitude increases and the preamp's outputs cross the Peak thresholds, ALBO diode impedance decreases providing more signal attenuation prior to the preamplifier input. If input signal magnitude decreases, diode impedance will increase, reducing signal attenuation. The result is a constant preamp input level creating a constant preamp output amplitude.

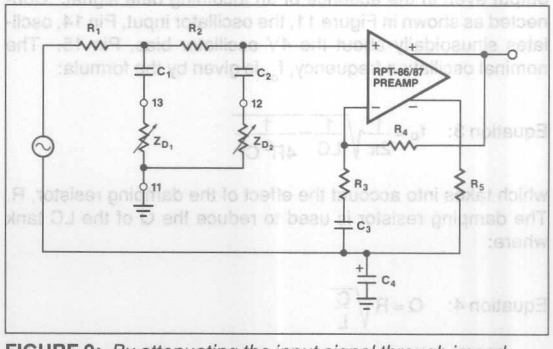


FIGURE 9: *By attenuating the input signal through impedance dividers, the ALBO network simulates the attenuation and frequency characteristics of maximum line length.*

ALBO diodes. These capacitors also create a frequency dependency by adding a pole/zero pair in the attenuation characteristics of each ALBO diode stage. Figure 10 illustrates the gain vs. frequency response of the first ALBO stage assuming that $R_1 \ll R_2$ and $Z_{D1} \ll R_1$. As Z_{D1} changes depending on input signal amplitude, ω_Z also changes. At $Z_{D1}=R_D MAX$, $\omega_Z = \omega_P$, and the stage gain equals unity with flat frequency response. At $Z_{D1} = R_D MIN$, there is maximum separation between ω_Z and ω_P and a maximum attenuation equal to approximately Z_{D1}/R_1. Combining the effects of two ALBO stages allows the programming of two variable-duration poles and a gain ranging from unity to $(Z_{D1}Z_{D2})/(R_1R_2)$.

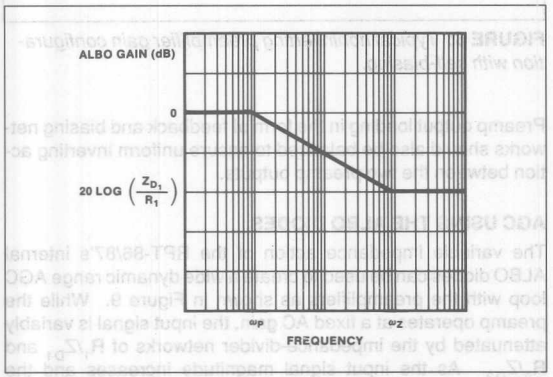


FIGURE 10: *The ALBO impedance creates frequency dependent attenuation.*

DESIGNING THE LC TANK OSCILLATOR

The oscillator on board the RPT-86/87 is based on a pulsed LC resonant tank and produces a continuous "square-wave" clock output even in the absence of an incoming data signal. Connected as shown in Figure 11, the oscillator input, Pin 14, oscillates sinusoidally about the 4V oscillator bias, Pin 15. The nominal oscillation frequency, f_o, is given by the formula:

Equation 3: $$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

which takes into account the effect of the damping resistor, R. The damping resistor is used to reduce the Q of the LC tank where:

Equation 4: $$Q = R\sqrt{\frac{C}{L}}$$

As the Q of the tank is reduced, the oscillation frequency becomes more easily pulled away from f_o by the synchronizing pulses of the Clock threshold comparators. A low Q is desirable for the repeater's

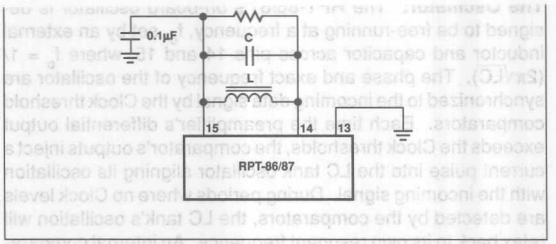


FIGURE 11: *A simple LRC resonant tank oscillator is used by the RPT-86/87 to recover the encoded clock from an incoming data signal.*

oscillator because often the incoming data bit stream is timed at a clock rate slightly different from f_o. The bit stream may also contain timing jitter where each data bit or packet of bits arrives with a slightly different clock timing. To ensure that no data bits are missed under these conditions, the RPT-86/87's oscillator must be flexible enough to track the clock frequency carried within the incoming bit stream.

The damping resistor also determines the amplitude of the LC tank's oscillation. Assuming R is the only dissipative element in the tank, its value can be calculated as a function of the peak-to-peak oscillation amplitude on Pin 14:

Equation 5: $$R = \frac{\pi V_{p\text{-}p}}{4(30\mu A)}$$

where 30µA equals the oscillator bias current, I_{OSC}. To avoid driving the tank oscillation onto the oscillator clamping diode contained within the RPT-86/87, V_{p-p} should be set less than $1.2V_{p\text{-}p}$. Letting R = 24kΩ sets an optimum oscillation level of $1V_{p-p}$ for the RPT-86/87.

The values for L and C can be calculated by choosing the desired Q and f_o and then substituting Equation 4 into Equation 3. The generalized formulas for L and C become:

Equation 6: $$C = \frac{\sqrt{4Q^2 - 1}}{4\pi f_o R}$$

Equation 7: $$L = \frac{CR^2}{Q^2}$$

Note that to maintain a sustained oscillation during the absence of an incoming data bit stream, the Q of the LC tank must be greater than 1.

When an incoming data bit stream is of sufficient amplitude to cross the Clock Detector's thresholds, a pulse of current is injected into the tank to synchronize the oscillator frequency to that of the incoming encoded clock. When synchronization is achieved, the various voltage and current waveforms are aligned as shown in Figure 12.

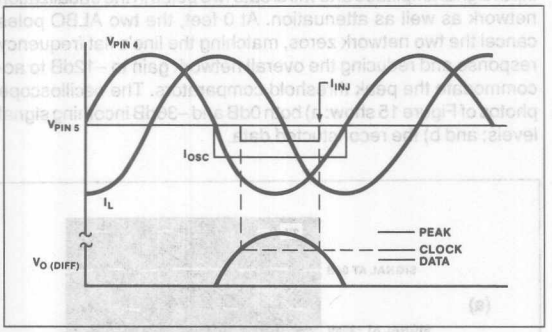


FIGURE 12: *The LC tank is synchronized to the incoming data when the clock detector injection current, I_{INJ}, is entered inside the oscillator's bias current pulse.*

TYPICAL APPLICATIONS

The circuit shown in Figure 13 is a typical T1, 1.544Mbit/s repeater system. The repeater is placed in series with a #22AWG unshielded, twisted-pair transmission line at distances of up to every 9,000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T_1 and output transformer T_2, and is converted to a 5.6V supply voltage that powers the RPT-86/87 by the Zener diodes Z_D. The incoming signal is coupled into the input network by the transformer T_1. One end of T_1's secondary winding is held at AC ground by capacitors C_9 and C_{10}; and the other end is terminated by the line-matching resistor R_1. The line-matching resistor is followed by a line equalization network, which includes the preamplifier feedback circuit and ALBO diodes. This network is designed to compensate for the losses and distortion of the #22AWG twisted-

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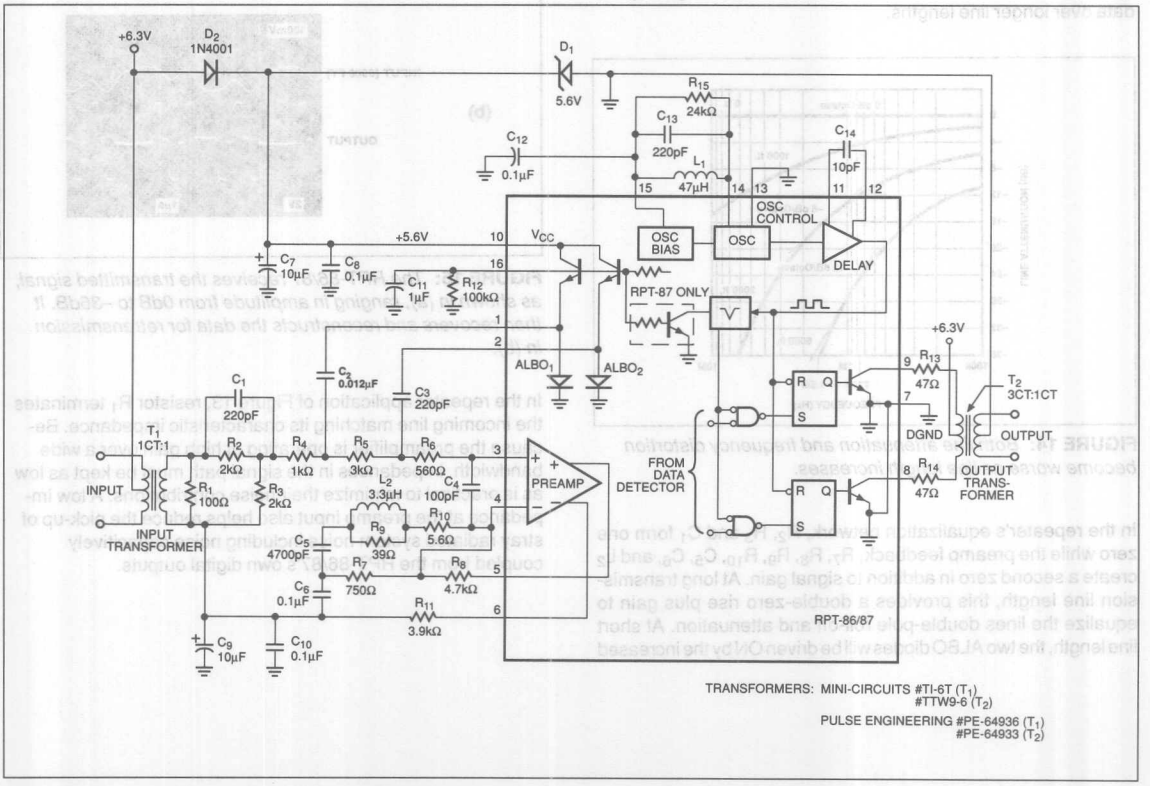


FIGURE 13: *A complete 1.544Mbit/s T1 Repeater Design. For additional details, see application note AN-140. (Note: for 2.048 Mbit/s E1 application, this same circuit works well to –44dB. The only changes necessary are R_1 = 120Ω, C_{13} = 150pF, and L_1 = 39µH. See application note AN-118).*

pair wire transmission line whose characteristics of loss vs. frequency vs. length are shown in Figure 14. The goal of the repeater's equalization network is to allow the recovery of the 1.544 Mbit/s T1 format data with an input level that varies from 0dB ($6V_{p-p}$) to –36dB ($95mV_{p-p}$) measured at a frequency 1/2 the data rate, or 772kHz. As evidenced in Figure 14, at 0 feet of transmission line, the receiver's incoming signal has 0dB attenuation with no frequency distortion. By 3000 feet, the signal amplitude reduces to –12dB level and falling at –6dB/octave, single-pole roll-off, between 770kHz and 1.544MHz. At 6000 feet of transmission line, the signal falls to –26dB with –12dB/octave, double-pole frequency roll-off.

Data rate and transmission line characteristics play an important role in determining the maximum line length from which the RPT-86/87 can recover data. From figure 14 it can be seen that #22AWG twisted-pair wire exhibits much less loss and frequency distortion at lower frequencies. Thus, the RPT-86/87 can recover data from much longer transmission lines if a lower data rate is used. Similarly, using a transmission line with less loss and frequency distortion will allow the RPT-86/87 to recover higher speed data over longer line lengths.

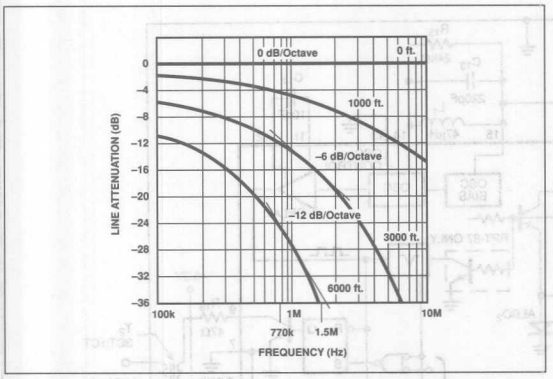


FIGURE 14: *Both line attenuation and frequency distortion become worse as line length increases.*

In the repeater's equalization network, R_2, R_3 and C_1 form one zero while the preamp feedback, R_7, R_8, R_9, R_{10}, C_5, C_6, and L_2 create a second zero in addition to signal gain. At long transmission line length, this provides a double-zero rise plus gain to equalize the lines double-pole roll-off and attenuation. At short line length, the two ALBO diodes will be driven ON by the increased input signal amplitude and will create two poles in the equalization network as well as attenuation. At 0 feet, the two ALBO poles cancel the two network zeros, matching the line's flat frequency response and reducing the overall network gain to –12dB to accommodate the peak threshold comparators. The oscilloscope photos of Figure 15 show: a) both 0dB and –36dB incoming signal levels; and b) the reconstucted data.

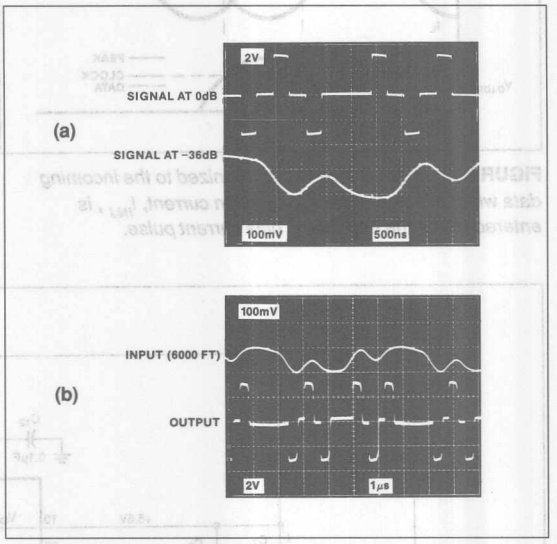


FIGURE 15: *The RPT-86/87 receives the transmitted signal, as shown in (a), ranging in amplitude from 0dB to –36dB. It then recovers and reconstructs the data for retransmission in (b).*

In the repeater application of Figure 13, resistor R_1 terminates the incoming line matching its characteristic impedance. Because the preamplifier is operating at high gain over a wide bandwidth, impedances in the signal path must be kept as low as is practical to minimize their noise contributions. A low impedance at the preamp input also helps reduce the pick-up of stray radiated system noise including noise capacitively coupled from the RPT-86/87's own digital outputs.

Digital Panel Meters
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Selection Guide
Digital Panel Meters

Model	Digits	FS Range	Data Output	Display Type	Page	Comments
AD2026	3	−99 mV to +999 mV	N/A	LED	C I 5–11	+5 V Power
AD2010	3 1/2	±199.9 mV	BCD	LED	C I 5–7	+5 V Power
AD2021	3 1/2	±199.9 mV, ±1.999 V, ±19.99 V	Serial	LED	C I 5–9	+5 V Power

Orientation
Digital Panel Meters

A digital panel instrument is a self-contained instrument designed for panel mounting. It contains circuitry for measuring analog quantities, converting them to digital and providing a numeric readout. In addition, it usually provides data outputs for interfacing with a printer and/or a computer system. A *digital panel meter* measures voltage, generally with fractional-millivolt resolution.

A useful publication from Analog Devices may be helpful in understanding the issues involved in data conversion: *Analog-Digital Conversion Handbook*, third edition (1986, $32.95). It is available from the Analog Devices Literature Center at P.O. Box 796, Norwood MA 02062.

A DPM samples the input voltage periodically, converts that voltage to digital, and displays the corresponding reading visually. A digital panel meter, then, consists of four basic functional sections: the input section, including signal conditioning and analog to digital conversion circuitry; the display; the data outputs and the power supply.

Processing the Input Signal

The primary function of the input section is to convert an analog input voltage into a digital signal for display. Besides this basic function, the input section also buffers the input to provide a high input impedance, prevent circuit damage in overvoltage conditions, reject both normal-mode and common-mode noise on the input signal, compensate for large variations in operating temperature and sometimes even measure the ratio of two separate input voltages.

The analog to digital conversion scheme used on most DPMs is the dual-slope type due to its inherent stability and normal-mode noise rejection. The dual-slope converter can also be used to measure the ratio of two input voltages in some DPM designs. Lower-resolution DPMs sometimes use staircase or single slope converters which require RC filtering of the input signal for a normal-mode-noise rejection.

The input of the DPM may be single-ended, differential or floating. Single-ended inputs measure the input voltage with respect to input common and may require some care in application to avoid ground loop problems. To prevent ground loops, some of Analog Devices' DPMs use a "limited differential input," where a resistor separates analog and digital grounds allowing up to 200mV of common-mode voltage and providing up to 60dB of common-mode rejection.

Displaying the Data – Digital Outputs

Once the input signal is digitized, it is decoded and displayed on a digital readout. Analog Devices DPMs use large seven-segment light-emitting diode (LED) displays.

DPM full-scale range, including *overrange*, is defined by the number of digits and polarity. In mixed-fraction designations (e.g., 3 1/2 digits), a full digit is one capable of displaying any numeral from 0 through 9. The fraction generally means the ratio of the display's maximum leading digit to the power of two that corresponds to the number of overrange bits; for example, a 3 1/2-digit meter's maximum reading is 1999, a 4 3/4-digit meter's maximum reading is 39999.

Since the visual display of a DPM must be in a decimal format, counter chips used in DPM conversion circuitry are generally binary-coded decimal (BCD) types. The data output format depends on the circuit design of the meter; for example, the AD2010 has parallel BCD data outputs with all BCD bits available simultaneously, while the AD2021 has character-serial outputs – each BCD digit is gated onto a single set of parallel output lines in sequence. The latter technique requires fewer connections and simplifies data interfacing.

Digital data outputs from DPMs are generally compatible with DTL or TTL logic systems; many DPMs are also compatible with CMOS logic.

Control

The kinds and number of control inputs and outputs – and their interpretation – may differ from one model to another, but they are well defined on the data sheets. Examples of typical control functions that may be found in DPMs include triggering of conversions, external *hold*, decimal points (jumper or logic-programmable), display blanking and *status* output.

Understanding Performance Specifications

Resolution, Accuracy and Stability – these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.

Besides temperature variations, there are three components of DPM inaccuracy: *zero offset error*, *gain error* and *quantization error*. In any device using a counter and clock to determine a digital output, there is always a potential ±1 count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed ±1 digit inaccuracy.

Zero-level offsets in the analog circuitry cause errors specified as a percentage of full-scale reading. These errors can be corrected by a zero-calibration potentiometer requiring periodic resetting.

Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range potentiometer is used for periodic adjustment of the gain.

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

To illustrate these specifications, consider a 3 1/2 digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or 0.05% of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of ±0.05% ±1 digit.

Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only 50ppm/°C (0.005%/°C) will produce an additional error of ±0.05% over a range of only ±10°C.

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable.

DEFINITIONS – DPM TERMS & SPECIFICATIONS

Accuracy (Absolute): DPMs are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.

Accuracy (Relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: *Linearity*.

Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPMs using transistor input circuitry are biased current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to 8, 4, 2 and 1 and 10 permissible levels with weights 0-9. BCD is normally used where a decimal display is needed.

Bipolar: A bipolar DPM measures inputs which may be of either positive or negative polarity and automatically displays the polarity as well as the magnitude of the input voltage on the readout.

Character Serial BCD: Multiplexed BCD data outputs, where each digit is gated sequentially onto four common output lines.

Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common-mode voltage range. Common-mode rejection is expressed as a ratio and usually given in dB. (CMR = 20 log CMRR 120dB of common-mode rejection.) (CMRR = 10^6) means that a 10V common-mode voltage is processed as though it were an additive differential input signal of 10μV magnitude.

Common-Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.

Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externally-triggered rates.

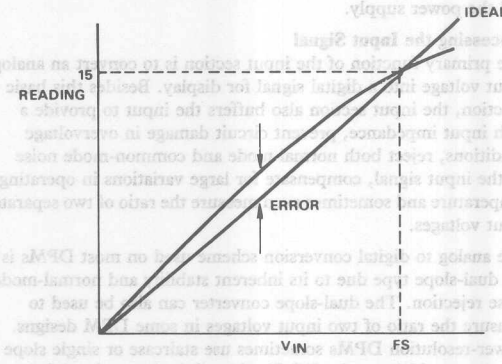
Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full-scale reading.

Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time.

Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.

Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For dc measuring DPMs, the input is measured at dc. For ac measuring DPMs, it is expressed as a dc resistance shunted by a specified capacitance.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices defines nonlinearity as the deviation from a straight line drawn between the zero and full-scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.



Linearity

Normal-Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the analog *high* input. Normal-mode rejection is expressed as the ratio of the actual value of the undesired signal to its measured value over a specified frequency range. (NMR (dB) = 20 log NMRR, e.g., NMR = 40dB means an attenuation of 100:1.)

Overload: An input voltage exceeding the full-scale range of the DPM produces an overload condition. An overload condition is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a 3 1/2 digit DPM with a range of 199.9mV, a ≥200mV, signal will produce an overload condition.

Overrange: An input signal that exceeds all nines on a DPM, but is less than an overload. On a 3 1/2 digit DPM with a full-scale range of 199.9mV, the all-nines range is 0-99.9mV, and signals from 100-199.9mV are said to fall in the 100% overrange region. Some DPMs have higher overrange capability. A 3 3/4 digit DPM has a full-scale range of 3.999 or 300% overrange.

Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained dc voltages that can be tolerated.

Parallel BCD: A data output format where all digital outputs are available simultaneously.

Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications.

Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A 3 1/2 digit DPM's full-scale range consists of three digits (all-nines range) and 100 percent overrange capability.

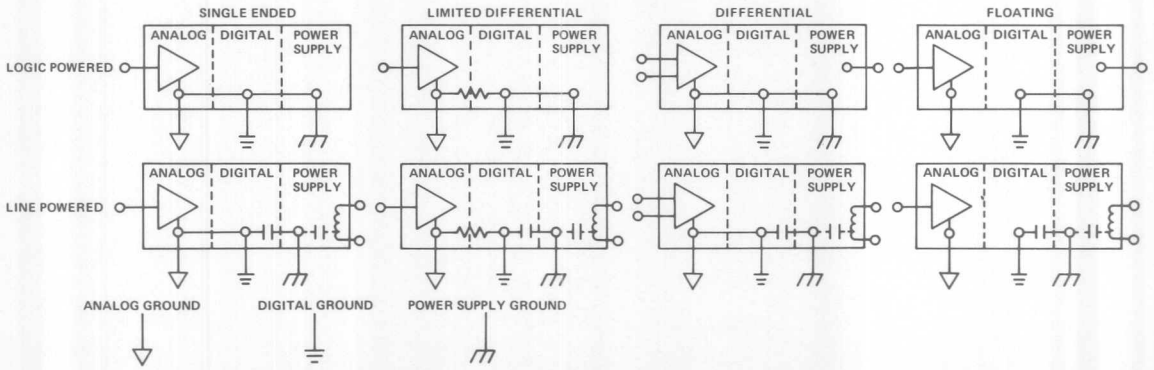
Ratiometric: Dual Slope DPMs compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPMs provide inputs for external reference voltages for ratiometric measurements.

Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full-scale range and number of digits of a DPM. For example, if a 3 1/2 digit DPM has a resolution of 1 part in 2000 (0.05%) over a full-scale range of 199.9mV, the DPM can resolve 0.1mV.

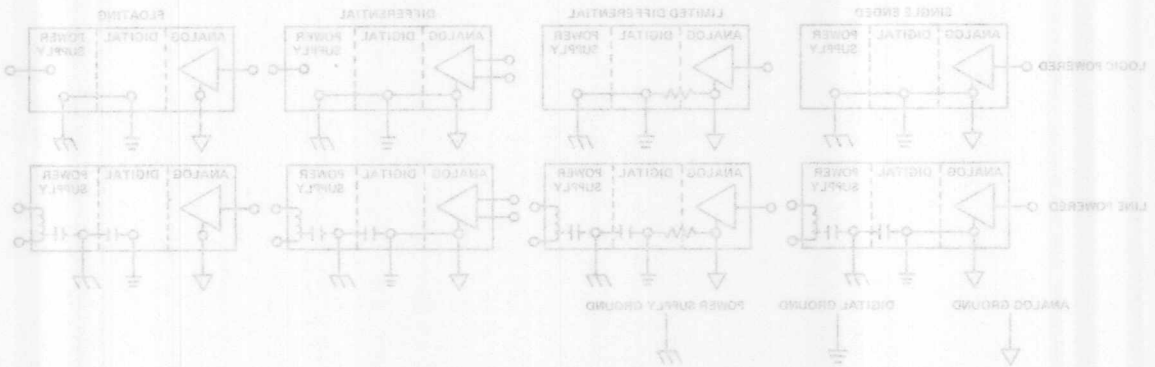
Digits	Counts (F.S.)	Resolution (% F.S.)
2 1/2	199	0.5%
3	999	0.1%
3 1/2	1999	0.05%
3 3/4	3999	0.025%
4	9999	0.01%
4 1/2	19999	0.005%
4 3/4	39999	0.0025%

Temperature Coefficient: The additive error term (ppm/°C or % Reading/°C) caused by effects of variations in operating temperature on the electronic characteristics of the DPM.

Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.



Grounding Configurations of DPMs

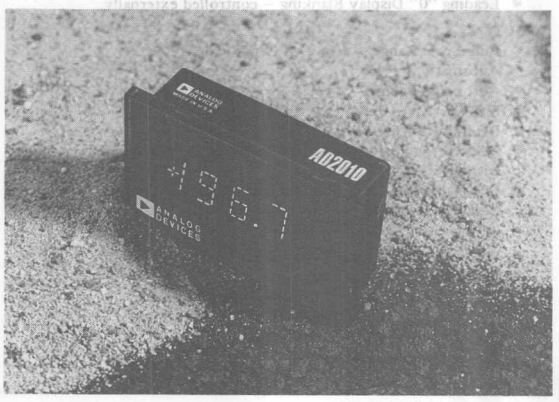

ANALOG
DIGITAL
POWER SUPPLY
ANALOG GROUND
DIGITAL GROUND
POWER SUPPLY GROUND

Low Cost, 3 1/2 Digit DPM for OEM Applications

AD2010

FEATURES
LED Display with Latched Digital Outputs
Small Size, Lightweight
Automatic Zero Correction; Max Error: 0.05% ±1 Digit
High Normal Mode Rejection: 40dB @ 50 or 60Hz
Optional Ratiometric Operation
Leading "0" Display Blanking
5VDC Powered

APPLICATIONS
Medical/Scientific/Analytic Instruments
Data Acquisition Systems
Industrial Weighing Systems
Readouts in Engineering Units
Digital Thermometers



5

GENERAL DESCRIPTION

Analog Devices' model AD2010 represents an advance in price/performance capabilities of 3½ digit digital panel meters. The AD2010 offers 0.05% ±1 digit maximum error with bipolar, single ended input, resolution of 100μV, and a common mode rejection ratio of 60dB (CMRR) at ±200mV (CMV).

The AD2010 features a light-emitting-diode (LED) display with a full scale range of 0 to ±199.9 millivolts, latched digital data outputs and control interface signals, and leading zero display blanking. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors, thereby providing virtually no error. Another useful feature of the AD2010 is its 5V dc operation. The AD2010 can operate from the users' 5V dc system supply, thereby eliminating the shielding and decoupling needed for line powered units when the ac line must be routed near signal leads.

To satisfy most application requirements, the conversion rate of the AD2010 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 24 readings per second dow.. .o an indefinite hold time. The AD2010 can also be connected for automatic conversion at its maximum conversion rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

A simplified block diagram of the AD2010, illustrating the features described above is shown in Figure 1.

For detailed information, contact factory.

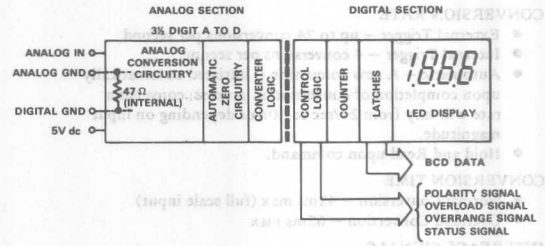


Figure 1. Simplified Functional Block Diagram

IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY

Dual-slope integration, as used in the AD2010 and as described in the theory of operation section, offers several design benefits.

- Conversion accuracy, for example, is independent of both the timing capacitor value and the clock frequency, since they affect both the up ramp and down ramp integration in the same ratio.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.

AD2010—SPECIFICATIONS (typical at +25°C and +5V dc unless otherwise noted)

DISPLAY OUTPUT
- Display consists of four LED's (0.27″ (6.9mm) high). for data digits plus 100% overrange and polarity indication.
- Overload – three data digits display zeros and flashes.
- Decimal Points – selectable at input connector.
- Leading "0" Display Blanking – controlled externally.

INPUT
- Full Scale Range – 0 to ±199.9 millivolts
- Automatic Zero
- Automatic Polarity
- Bias Current – 3nA
- DC Impedance – 100MΩ
- Overvoltage Protection – 20V sustained, 50V momentary without damage.
- Decimal Points (3) – illuminate with logic "1", extinguish with logic "0".

ACCURACY
- Maximum Error – 0.05% of reading ±1 digit
- Resolution – 0.1 millivolt
- Temperature Range – 0 to +50°C operating
  -30°C to +85°C storage
- Temperature Coefficient – ±50ppm/°C

NORMAL MODE REJECTION
- 40dB @ 60Hz

COMMON MODE REJECTION
- 60dB @ ±200mV

CONVERSION RATE
- External Trigger – up to 24 conversions per second
- Internal Trigger – 4 conversions per second
- Automatic – A new conversion is initiated automatically upon completion of conversion in process; conversion rate will vary from 24/sec to 40/sec depending on input magnitude.
- Hold and Read upon command.

CONVERSION TIME
- Normal Conversion – 42ms max (full scale input)
- Overload Conversion – 62ms max

INTERFACE SIGNALS
- DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

- Inputs

External Trigger – Operation in the "External Trigger" mode requires that the "External Hold" input be a logic "0" or ground.

Negative Trigger Pulses – Applying a logical "low" to the "HOLD" input disables the internal trigger. A negative trigger pulse (logic "1" to logic "0") of 1.0μs minimum applied to the "EXT TRIGGER" input will initiate conversion in the same manner as the internal oscillator. The external trigger should not be repeated, however, until the "status" indicates completion of the conversion in process.

Positive Trigger Pulses – The "HOLD" input can be used to trigger the AD2010 from a "normally low" signal with the "EXT TRIGGER" input open or logic "1". Following a "hold" a new reading will be initiated on the leading edge of the "hold" signal. Thus, a momentary positive pulse on the "HOLD" input can be used to trigger the AD2010. The drift correct interval, however, begins on the trailing edge of the positive pulse, so if the pulse width exceeds 1ms, the conversion will actually be initiated by the internal trigger.

Maximum Conversion Rate - Automatic – The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output back into the "hold" input. In this manner the status signal going high at the end of one conversion immediately initiates a new conversion. The pulses appearing on the status line can be used to step a multiplexer directly, since the built-in drift-correct delay of 8.33ms will allow settling of the input prior to conversion. A logic "0" applied to the "EXT TRIGGER" will inhibit the automatic trigger mode.

External Hold – Logic "0" or ground applied to this input disables the internal trigger and the last conversion is held and displayed. For a new conversion under internal control the input must be opened or at logic "1". For a new conversion under external control, a positive pulse of less than 1.0ms can be applied (as previously explained).

OUTPUTS
- 3 BCD Digits (8421 Positive True) - latched - 3TTL loads
- Overrange - logic "1" - latched - 6TTL loads, indicates overrange.
- Overload - logic "0" indicates overload (>199.9mV) logic "1" - latched - 6TTL loads, indicates data valid.
- Polarity - logic "1" - latched - 6TTL loads, indicates positive polarity input.
- Status - logic "0" - conversion in process logic "1" - latched - 6TTL loads, indicates conversion complete.

POWER
- +5V dc ±5%, 500mA

WARM UP
- Essentially none to specified accuracy

ADJUSTMENTS
- Range potentiometer for full scale calibration. Calibration recommended every six months.

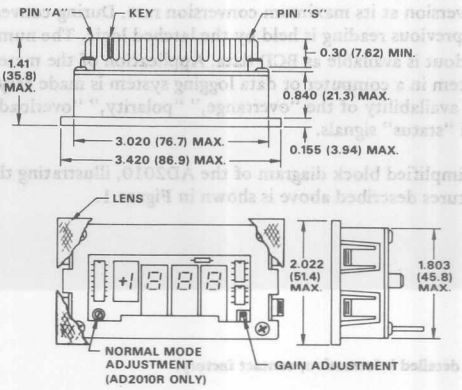
SIZE
- 3″W x 1.8″H x 0.84″D (76.2 x 45.7 x 21.3mm) (overall depth for case and printed circuit board extension is 1.40″ (35.6mm)).

ORDERING GUIDE
- AD2010 - Standard AD2010 as described above - tuned for peak normal mode rejection at 60Hz and its harmonics.

WEIGHT
- 4 oz. (113.5gm)

OVERALL DIMENSIONS

All dimensions are given in inches and (mm).



Specifications subject to change without notice.

Low Cost, 3 1/2 Digit Logic Powered DPM with LED Displays

AD2021

FEATURES

- "Second Generation" MOS-LSI Design
- Large 0.5" (13mm) LED Displays
- +5VDC Logic Powered
- ±1.999V, ±199.9mV or ±19.99V Full Scale Ranges
- Limited Differential Input
- Low Power Consumption: 2.0 Watts
- Small Size, Industry Standard Case Design

APPLICATIONS

- General Purpose Logic Powered DPM Applications
- Portable Applications Requiring Low Power Consumption

GENERAL DESCRIPTION

The AD2021 is a low cost, 3½ digit, +5V dc logic powered digital panel meter with large LED displays. While designed for general purpose DPM applications, the small size, light weight and low power consumption of the AD2021 make it an ideal digital readout for modern, compact instrument designs.

THE BENEFITS OF "SECOND GENERATION" DESIGN

The AD2021 is designed around MOS-LSI (Metal-Oxide-Semiconductor, Large Scale Integration) integrated circuits, which greatly reduce the number of components, and thereby the size, and reduce power consumption to 2.0 watts. Both the lower power consumption and fewer interconnections between components promise greatly increased reliability, and the circuit design maintains the performance and features of earlier DPMs. Large 0.5 inch (13mm) LED displays offer the visual appeal of gas discharge displays with the ruggedness and lifetime of all solid state devices.

EXCELLENT PERFORMANCE AND EASY APPLICATION

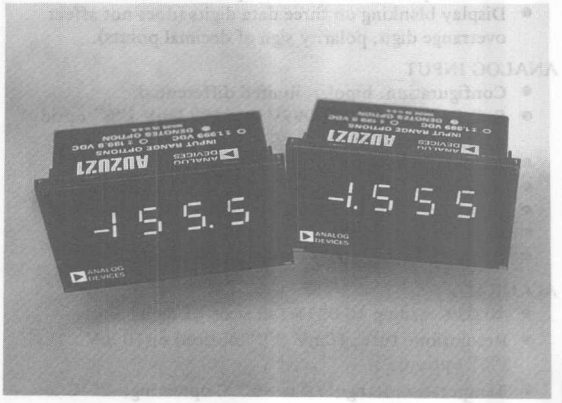
The AD2021 measures input voltage over a full scale range of ±1.999V dc or ±199.9mV dc ("S" option) with an accuracy of ±0.05% reading ±0.025% full scale ±1 digit. Using the "limited differential" input first used on Analog Devices' AD2010, the AD2021 prevents ground loop problems and provides 35 to 50dB of common mode rejection at common mode voltages up to ±200mV. Normal mode rejection is 40dB at 50Hz to 60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible to CMOS logic systems. For those applications requiring parallel BCD data, schemes for making the serial to parallel conversion are available. Controls to hold readings, select decimal points and blank the display are provided.

DESIGNED AND BUILT FOR RELIABILITY

The AD2021 is packaged in Analog Devices' logic powered DPM case size, only 1.25 inches (32mm) deep. The small size of this DPM makes it easy to accommodate in any instrument design, and since several other manufacturers now use the same panel cutout for logic powered DPMs, this industry standardization allows mechanical second sourcing. In addition, the

For detailed information, contact factory.



AD2021 uses the same pin connections as the AD2010 (except in BCD outputs, of course) as a convenience to allow updating designs to take advantage of the second generation design and larger display of the AD2021. Each AD2021 receives a full one week failure free burn-in before shipment.

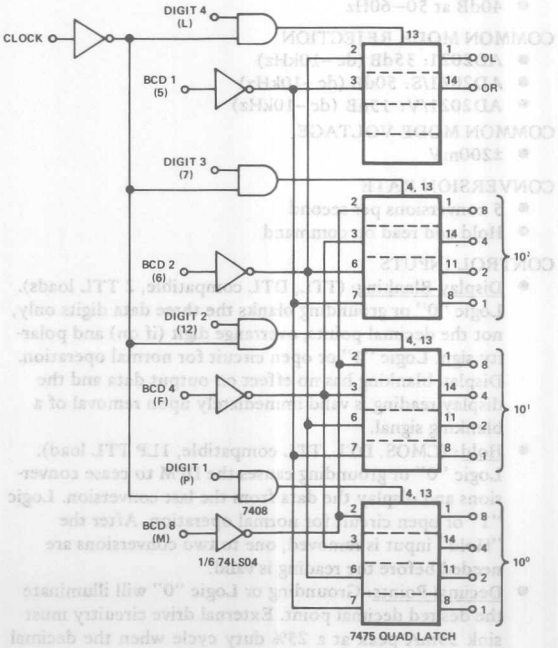


Figure 1. AD2021 Bit Parallel Character Serial to Full Parallel Data Conversion. AD2021 Pin Connections Are Shown in Parentheses.

AD2021 — SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.5″ (13mm) high for three data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points selectable at input connector.
- Display blanking on three data digits (does not affect overrange digit, polarity sign of decimal points).

ANALOG INPUT
- Configuration: bipolar, limited differential
- Full Scale Range: ±1.999V or ±199.9mV ("S" option) ±19.99V ("V" option)
- Automatic Polarity
- Auto Zero
- Input Impedance: 100MΩ (1MΩ – "V" option)
- Bias Current: 50pA
- Overvoltage Protection: ±50V dc, sustained

ACCURACY
- ±0.05% reading ±0.025% full scale ±1 digit[1]
- Resolution: 1mV, 10mV ("V" option) or 100μV ("S" option)
- Temperature Range[2]: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: auto zero
- Warm-Up Time to Rated Accuracy: less than one minute
- Settling Time to Rated Accuracy: 0.4 second

NORMAL MODE REJECTION
- 40dB at 50–60Hz

COMMON MODE REJECTION
- AD2021: 35dB (dc –10kHz)
- AD2021/S: 50dB (dc –10kHz)
- AD2021/V: 15dB (dc –10kHz)

COMMON MODE VOLTAGE
- ±200mV

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS
- Display Blanking: (TTL, DTL compatible, 2 TTL loads). Logic "0" or grounding blanks the three data digits only, not the decimal points, overrange digit (if on) and polarity sign. Logic "1" or open circuit for normal operation. Display blanking has no effect on output data and the display reading is valid immediately upon removal of a blanking signal.
- Hold: (CMOS, DTL, TTL compatible, 1LP TTL load). Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After the "Hold" input is removed, one to two conversions are needed before the reading is valid.
- Decimal Points: Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle when the decimal points are illuminated.

DATA OUTPUTS (See Application Section for details on data outputs)
- BCD Data Outputs: (CMOS, LP TTL or LP Schottky compatible), bit parallel, character serial format.
- Digit Strobe Outputs: (CMOS, DTL, TTL compatible, one TTL load). Logic "1" on any of these lines indicates the output data is valid for that digit.
- Polarity Output: (CMOS, TTL, DTL compatible, one TTL load). Logic "1" indicates positive polarity input, logic "0" indicates negative polarity.
- Status: (CMOS or LP TTL compatible). When this signal is at Logic "1", the output data is valid.
- Clock: (CMOS, DTL, TTL compatible, one TTL load). The clock signal is brought out to facilitate conversion from character serial to parallel data.
- INTERFACING DATA OUTPUTS. The BCD data outputs are in a bit parallel, character serial format. There are four BCD bit outputs (1, 2, 4, 8) and four digit outputs (10^0, 10^1, 10^2, 10^3). The BCD digits are gated onto the output lines sequentially, and the BCD bits are valid for the digit whose digit line is high. The data is valid except when being updated which occurs within 2 milliseconds after the status line goes low.

REFERENCE OUTPUT
- A 6.4V ±5% analog reference output is made available. This reference should be buffered and filtered if use in external circuitry is desired.

POWER INPUT
- +5V dc ±5%, 1.45 watts

CALIBRATION ADJUSTMENTS (See Application Section for calibration instructions)
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE
- 3″W x 1.8″H x 1.33″D (76 x 46 x 34mm)
- 1.90″ (48mm) overall depth to rear of card edge connector.
- Panel cutout required: 3.175″ x 1.810″ (80.65 x 45.97mm).

WEIGHT
- 4 ounces, (115 grams)

OPTIONS – ORDERING GUIDE
- Input Voltage Range: AD2021 – 1.999V dc Full Scale
  AD2021/S – 199.9mV dc Full Scale
  AD2021/V – 19.99V dc Full Scale

CONNECTOR
- 30 pin, 0.156″ spacing card edge connector. Viking 2VK15D/1-2 or equivalent.
- Optional: Order AC1501

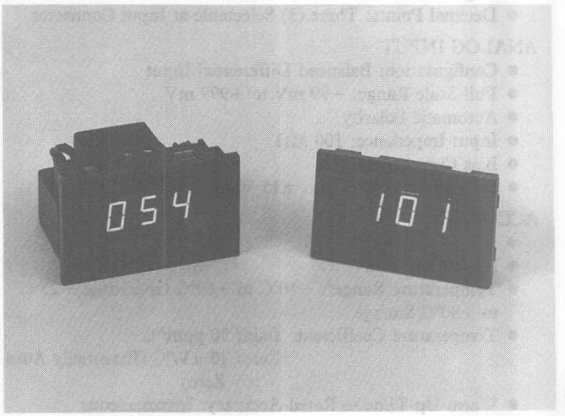
NOTES
[1] Guaranteed at 25°C and nominal supply voltage
[2] Guaranteed

Specifications subject to change without notice.

Low Cost, 3 Digit Logic Powered DPM

AD2026*

FEATURES
Third Generation I^2L LSI Design
Logic Powered (+5 V DC)
Large 0.56″ Red Orange LEDs
Balanced Differential Input/Floating 1000 V, CMV
Terminal Block Interface (AC Version)
High Reliability: >250,000 Hour MTBF
Small Size and Weight
Low Cost



5

GENERAL DESCRIPTION

The AD2026 is specifically designed to provide a digital alternative to analog panel meters. The AD2026 is logic powered (+5 V dc). Most of the analog digital circuitry is implemented on a single I^2L LSI chip, the AD2020. Only 13 additional components are required to complete the AD2026. The entire assembly is mounted on a single 3″ × 1 5/8″ PCB.

The AD2026 offers as a standard feature, 0.56″ high LED Displays. Brightness is enhanced due to the Red Orange lens. In addition to the Red Orange lens, the AD2026 is also available with a dark red lens for applications where maximum brightness is not required and minimum backlighting is desired.

A unique patented case design utilizes molded-in fingers, both to capture the PCB in the case and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The AD2026 occupies less than 1″ of space behind the panel.

EXCELLENT PERFORMANCE

The AD2026 offers the instrument designer digital accuracy, resolution and use of readout while occupying less space than its analog counterpart. Other features of analog meters such as reliability and instantaneous response are retained in the AD2026.

The AD2026 measures and displays inputs from −99 mV to +999 mV, with an accuracy of 0.1% of reading ±1 digit. Zero shift is less than one bit over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input of the AD2026 rejects common-mode voltages up to 200 mV, enough to eliminate most ground loop problems.

WIRING CONNECTIONS

For Balanced Differential operation with the AD2026, connect input as shown in Figure 1. The common-mode loop must provide a return path for the bias currents internal to the AD2026. The resistance of this path must be less than 100 kΩ and total common-mode voltages must not exceed 200 mV.

For applications where attenuation is required scaling resistors can be connected between Pins 6 and 7 and between Pins F and H. Pin 5 must be used as the High Analog Input when scaling resistors are used and Pin 4 when they are not. Pin E is the Analog Low Input.

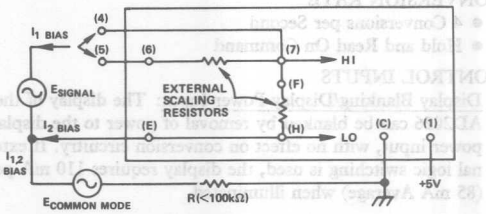


Figure 1.

PIN CONNECTIONS

DC VERSION

Pin	Function	Pin	Function
1	+5 V Power	A	Decimal Point XX.X
2	+5 V Display Power	B	Decimal Point XXX.
3	Decimal Point XXX	C	Power Ground
4	Input (When Scaling Resistors Not Used)	D	Hold
		E	Analog Ground
5*	Input (When Scaling Resistors Are Used)	F*	Shunt Arm of Scaling Resistor Divider
6*	Series Arm of Scaling Resistor Divider	H*	Shunt Arm of Scaling Resistor Divider
7*	Series Arm of Scaling Resistor Divider		

*Not normally used. Allows convenient mounting of scaling resistors.

***Covered by Patent Numbers: 4,092,698, 29,992; 3,872,466; and 3,887,863.**

AD2026—SPECIFICATIONS (typical at +25°C and nominal supply voltage unless otherwise noted)

DISPLAY OUTPUT
- Light Emitting Diode, Planar Seven Segment Display Readouts, 0.56″ (14.6 mm) High (Orange)
- Overload Indication: EEE
- Negative Indication: −XX
- Negative Overload Indication: − − −
- Decimal Points: Three (3) Selectable at Input Connector

ANALOG INPUT
- Configuration: Balanced Differential Input
- Full-Scale Range: −99 mV to +999 mV
- Automatic Polarity
- Input Impedance: 100 MΩ
- Bias Current: 100 nA
- Overvoltage Protection: ±15 V dc, Sustained

ACCURACY
- ±0.1% ±1 Digit[1]
- Resolution: 1 mV
- Temperature Range[2]: −10°C to +60°C Operating: −25°C to +80°C Storage
- Temperature Coefficient: Gain: 50 ppm/°C
  Zero: 10 μV/°C (Essentially Auto Zero)
- Warm-Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 sec for Full Input Voltage Swing

COMMON-MODE REJECTION
(1 kΩ Source Imbalance, DC to 1 kHz)
- 50 dB, ±200 mV Common-Mode Voltage

CONVERSION RATE
- 4 Conversions per Second
- Hold and Read On Command

CONTROL INPUTS

Display Blanking/Display Power Input: The display of the AD2026 can be blanked by removal of power to the display power input, with no effect on conversion circuitry. If external logic switching is used, the display requires 110 mA peak (85 mA Average) when illuminated.

Hold: When the Hold input is at Logic "0," grounded or open circuit, the AD2026 will convert at 4 conversions per second. If a voltage of 0.6 V to 2.4 V is applied to this input, the DPM will stop converting and hold the last reading. A 12 kΩ resistor in series with this input to +5 V will provide the proper voltage input.

DECIMAL POINT
- To Illuminate Decimal Points Ground Appropriate Pin (A, B or 3)

POWER INPUT[3]
- Converter: +5 V ±5%, 0.2 Watts Typ; 0.33 Watts Max
- Display: +5 V ±40%, 0.45 Watts Typ; 0.75 Watts Max

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended Recalibration Interval: Six Months

SIZE
- 3.43″ W × 2.0″ H × 0.85″ D (87 × 52 × 22 mm)
- 0.88″ (22 mm) Overall Depth to Rear of Connector
- Panel Cutout Required: 3.175 ±0.015″ × 1.810 ±0.015″ (80.65 ±0.38 × 45.97 ±0.38 mm)

WEIGHT
- 1.8 Ounces (53 Grams)

CONNECTIONS

A 10-Pin T&B/Ansley 609-1000M with Two Feet of 10 Conductor Ribbon Cable Is Available. Order AC2618.

Conductor to Pin A Is Color Coded. Sequence of Ribbon Connections Is A, 1, B, 2, C, 3, etc.

ORDERING GUIDE

AD2026-11

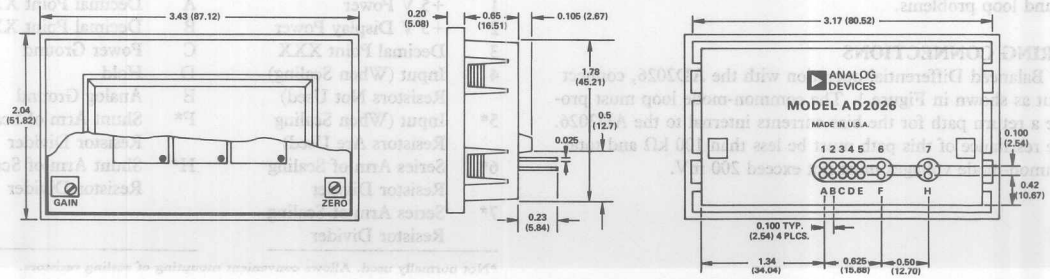
Lens[4]		
Red Lens	1	ENTER
Red Orange Lens	2	

NOTES
[1]Guaranteed at +25°C and nominal supply voltage.
[2]Guaranteed.
[3]When the same power supply is used to power both display and converter, +5 V, ±5%, 0.65 watts typical, 0.9 watts max is required.
[4]No Charge Options.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
1. ALL DIMENSIONS ARE IN INCHES AND (MM).
2. PANEL THICKNESS 0.0625 TO 0.125 (1.6) TO (3.2).

For more than twenty-five years, Analog Devices has provided high-performance solutions to signal processing problems. This extensive interaction with designers of leading-edge signal processing systems forms the basis for continued development of new signal processing products. Today, Analog Devices offers a wide range of programmable DSP processors based on an architecture that is optimized for signal processing. Processors range from a very low cost fixed-point microcomputer, to the highest performance IEEE-compatible floating-point microprocessor.

Together with our signal processing customers, Analog Devices has created the industry's first family of Mixed-Signal Processors (MSProcessors™) and Mixed-Signal Peripherals (MSPeripherals™). Mixed-Signal Processors combine a programmable DSP architecture for signal processing with Analog Devices' precision signal acquisition circuitry to provide compact, low cost, high performance, single-chip solutions. Analog Devices is committed to the continuing integration of high-performance signal acquisition systems with optimized DSP processors.

Future MSProcessors will extend the performance of both the signal acquisition system and the DSP engine to address emerging applications requirements. What applications can you imagine with MSProcessors?

OPTIMIZED DSP ARCHITECTURE

Architectures optimized for DSP must meet the five following requirements:

Fast, Flexible Arithmetic
- Arithmetic units arranged in parallel for Fixed- and Floating-Point families
- Single-cycle register context switch for Fixed- and Floating-Point families
- Separate input and output registers for Fixed-Point family
- General purpose register file for Floating-Point family

Extended Dynamic Range of Multiply/Accumulate
- 40-Bit accumulator for Fixed-Point family
- 80-Bit accumulator for Floating-Point family

Single-Cycle Access of Dual Operands
- Provides single-cycle, 3-bus performance:
  — next instruction fetch
  —2 data operands

Hardware Circular Buffer
- Maintains 8 simultaneous circular buffers for Fixed-Point family
- Maintains 16 simultaneous circular buffers for Floating-Point family

Zero-Overhead Looping and Single-Cycle Conditional Branching
- Single-cycle conditional arithmetic instruction for Fixed- and Floating-Point families
- Stack supports 4 levels of nested loops for Fixed-Point family
- Stack supports 16 levels of nested loops for Floating-Point family

Analog Devices extends the optimized DSP architecture to include features such as:
- Auto data buffering
- Auto boot from external byte-wide EPROM
- Auto companding of data through serial port

DSP DEVELOPMENT SUPPORT

All processors are supported with a comprehensive set of development tools including:

- ANSI C-Compiler
- Linker
- System Builder
- Low Cost EZ-TOOLS
- Assembler
- Simulator
- Demonstration Board
- In-Circuit Emulators

Applications assistance is provided by:

- Expert DSP Staff
- Applications Handbooks
- Applications Assistance Line
- Computer Bulletin Board
- *DSPatch* Applications Newsletter
- Applications Library
- 3-Day Programming Workshop

For more information on our DSP products, contact your local Analog Devices sales office or authorized distributor. For marketing information, contact DSP marketing (617) 461-3881. For applications assistance, contact DSP applications (617) 461-3672.

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Selection Guide

DSP Processor Key Feature Summary

Model	Inst Cycle Time ns	Off-Chip Harvard Arch	Internal Program Memory RAM	Internal Data Memory RAM	Internal Program Cache Word	Program Memory Boot	Serial Ports	8/16-Bit Host Interface Port	Program Timer	On-Chip A/D and D/A	Ext Interrupts	Low Power Modes	Pin Count	Package Options[1]
16-Bit Fixed-Point														
ADSP-2100A	80	√	—	—	16 × 24	—	—	—	—	—	4	—	100	PGA, PQFP, CQFP
ADSP-2101	60	—	2K × 24	1K × 16	—	√	2	—	√	—	3	1	68	PGA, PLCC
ADSP-2102	60	—	2K × 24[2]	1K × 16	—	√	2	—	√	—	3	1	68	PGA, PLCC
ADSP-2105	100	—	1K × 24	0.5K × 16	—	√	1	—	√	—	3	1	68	PLCC
ADSP-2106	100	—	1K × 24[2]	0.5K × 16	—	√	1	—	√	—	3	1	68	PLCC
ADSP-2111	60	—	2K × 24	1K × 16	—	√	2	√	√	—	3	1	100	PGA, PQFP
ADSP-2112	60	—	2K × 24[2]	1K × 16	—	√	2	√	√	—	3	1	100	PGA, PQFP
ADSP-21msp50	77	—	2K × 24	1K × 16	—	√	2	√	√	√	3	2	132/144	PQFP/PGA
ADSP-21msp51	77	—	2K × 24[2] & 2K × 24 ROM	1K × 16	—	√	2	√	√	√	3	2	132/144	PQFP/PGA
32/40-Bit Floating-Point														
ADSP-21020	40	√	—	—	32 × 48	—	—	—	√	—	4	1	223	PGA, PPGA

NOTES
[1]Package Options: CQFP = Ceramic Quad Flat Pack; PGA = Ceramic Pin Grid Array; PLCC = Plastic Leaded Chip Carrier; PQFP = Plastic Quad Flat Pack; PPGA = Plastic Pin Grid Array.
[2]RAM/ROM.

Bus Interface & Serial I/O Products

THE μMAC® SERIES

The μMAC product line consists of data acquisition and control front ends designed for use in industrial applications. The systems provide signal conditioning, A/D and D/A conversion and control capabilities in front of a supervisory computer or in a stand-alone configuration. Two general groups of systems are available: intelligent, fixed function systems and programmable stand-alone systems.

Fixed-Function Front Ends

The fixed function systems are the μMAC-4000 and the μMAC-1050. The μMAC-4000 system provides isolation and conditioning of signals, A/D and D/A conversion, and storage of data (in engineering units) that is transferred to any host computer upon command (via RS-232 link). The μMAC-1050 offers additional levels of functionality such as minimum/maximum recording, local alarming, CAM sequence emulation, configuration storage in EEPROM, ramping of analog outputs, and other features that minimize host computer interaction. The unit also supports an RS-422/485 port for multidrop configurations.

Software driver options are available for both the μMAC-4000 and μMAC-1050 to provide a high level language interface to the units as well as support from Industry Standard software packages such as FIX DMACS, Control EG, LABTECH NOTEBOOK and LABTECH CONTROL. Refer to the chart for more detailed information.

Programmable Units

The programmable μMAC units are the μMAC-1060, μMAC-5000, μMAC-6000, and the μDCS-6000. The μMAC-5000 and μMAC-6000 are fully programmable in μMACBASIC® or C (μMAC-6000 only) and support battery-backed data and program storage, hardware watchdog timers, and serial communications for stand alone operation or custom host interface.

The μMAC-1060 is a single board controller that offers unprecedented price/performance levels. The unit is programmable in a fast, space efficient version of C, and also provides a watchdog timer, battery-backed memory, and up to three serial ports.

The μDCS-6000 provides a complete solution for distributed process monitoring and control applications. Based on the μMAC-6000 hardware, the system becomes a powerful controller with embedded FIX DMACS* software from Intellution for a truly "No Programming Required" distributed control solution.

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***ASYST is a trademark of ASYST Software Technologies, Inc.**
Control EG is a trademark of Quinn-Curtis
PS/2, Micro Channel, PC DOS, IBM PC, PC/XT and PC AT are trademarks of International Business Machines Corporation
LABTECH NOTEBOOK and LABTECH CONTROL are registered trademarks of Laboratory Technologies Corporation
MS-DOS, QuickBASIC and Microsoft are registered trademarks of Microsoft Corporation
MULTIBUS is a trademark of Intel Corporation
SNAPSHOT STORAGE SCOPE is a trademark of HEM Data Corporation
THE FIX and FIX DMACS are trademarks of Intellution, Inc.
TURBO Pascal and TURBO C are trademarks of Borland International Corporation
Unkelscope is a trademark of the Massachusetts Institute of Technology

THE RTI® SERIES

The RTI Series consists of analog and digital input/output boards that are compatible with popular microcomputer bus standards including:

- RTI-800 Series, IBM PC/XT/AT*
- RTI-200 Series, IBM PS/2,* Micro Channel* Architecture
- RTI-1200 Series, STD
- RTI-600 Series, VMEbus
- RTI-700 Series, MULTIBUS*

The RTI Series are families of boards that provide a wide range of functionality. Each board can operate independently or can be used with other RTI Series boards to solve an application. Different analog-to-digital conversion speeds, resolutions, input and output channel capacities and configurations are available, allowing customization of the systems. The RTI Series is typically used in applications where the computer is close to the sensors being measured.

RTI Software

The RTI-200 Series, RTI-800 Series and some of the RTI-1200 Series boards are supported by MS-DOS* driver software that provides easy-to-use, high-level routines for user written software programs. The routines can be called from popular languages like Microsoft* BASIC (Interpreted and Compiled), C, QuickBASIC,* Borland International TURBO Pascal* and TURBO C.*

Industry standard data acquisition and control software products like LABTECH NOTEBOOK,* LABTECH CONTROL,* ASYST*, SNAPSHOT STORAGE SCOPE,* Control EG,* THE FIX,* UnkelScope* and others support many of the RTI Series boards.

Signal Conditioners

The μMAC and RTI products can be used with signal conditioners in applications that require conditioning for isolated or nonisolated signals. The 3B and 5B Series of signal conditioning modules and the STB family of analog signal conditioning panels can be used with most RTI and μMAC products.

Selection Guide
Bus Interface & Serial I/O Products

IBM PC/XT/AT I/O Boards

		Analog Input				Analog Output		Digital I/O		
				Max Throughput						
Model	Function	Analog Input Channels	Resolution	XT	AT	Analog Output Channels	Resolution	Channels	Time-Related	Other Features
RTI-800 RTI-800-A RTI-800-F	Analog Input and Digital I/O	16 SE/8 DI 16 SE/8 DI 16 SE/8 DI	12-Bit 12-Bit 12-Bit	31 kHz 58 kHz 91 kHz	27 kHz 58 kHz 58 kHz			8 In/8 Out 8 In/8 Out 8 In/8 Out	3 Counter/Timers 3 Counter/Timers 3 Counter/Timers	Analog Input Expandable to 32 SE/16 DI PGA External Digital Trigger
RTI-802-4 RTI-802-8	Analog Output					4 8	12-Bit 12-Bit			Remote Sensing
RTI-815 RTI-815-A RTI-815-F	Multifunction Analog and Digital I/O	16 SE/8 DI 16 SE/8 DI 16 SE/8 DI	12-Bit 12-Bit 12-Bit	31 kHz 58 kHz 91 kHz	27 kHz 58 kHz 58 kHz	2 2 2	12-Bit 12-Bit 12-Bit	8 In/8 Out 8 In/8 Out 8 In/8 Out	3 Counter/Timers 3 Counter/Timers 3 Counter/Timers	Analog Input Expandable to 32 SE/16 DI PGA External Digital Trigger
RTI-817	Digital I/O							Three 8-Bit Ports		External Strobing Interrupts on Change of State
RTI-820	Modular Analog and Digital I/O	Up to 64	12-Bit	19 kHz	19 kHz	Up to 16	12-Bit	Three 8-Bit Ports		Interfaces Directly to Analog Signal Conditioning Panels; Slave Microprocessor Controls Analog Outputs
RTI-827	Frequency Input, Event Counting, Pulse Output							Three Outputs One 4-Bit Port	5 Counter/Timers	Debounce Circuitry on on Inputs External Interrupts
RTI-850-F	High Resolution Analog Input	8 DI	16-Bit 15-Bit 14-Bit	N/A N/A N/A	71 kHz 76 kHz 76 kHz					On-Board Memory Extensive Analog and Digital Triggering
RTI-860	High Speed Simultaneous Analog Input	16 SE	12-Bit 8-Bit	N/A N/A	250 kHz 330 kHz					On Board Memory Extensive Analog and Digital Triggering
RTI-870	Ultrahigh Resolution	4 DI	22-Bit	20 Hz				Two 4-Bit Ports		

STD BUS Compatible I/O Boards

	Analog Devices Part Number	STD BUS (NMOS) RTI-1226	RTI-1225	RTI-1260	RTI-1262	RTI-1265	RTI-1266	RTI-1267	STD BUS (CMOS) RTI-1280	RTI-1281	RTI-1282
Board Type	Input	•		•		•			•		
	Input/Output		•				•	•		•	
	Output				•						•
Channel Capacity	Input (Single Ended/ Differential)	16/8	16/8	32/16		64	64	24 Digital I/O	16/8	16/8	
	Output		2		4		16			2	4 or 8
Input Resolution	10 Bits	•	•								
	12 Bits			•		•	•		•	•	
Output Resolution	8 Bits		•								
	12 Bits				•		•			•	•
Additional Features											
Programmable Gain Amplification				•					•	•	
Single +5 V Operation		•	•	•	•	•	•	•	•	•	•
4–20 mA Output					•						•
Direct Sensor Interface Thermocouples, RTDs						•	•				
IBM PC Software Compatible						•	•	•			

Selection Guide
Bus Interface & Serial I/O Products

IBM PS/2 Micro Channel I/O Boards

		Analog Input			Analog Output		Digital I/O		Other
Model	Function	Analog Input Channels	Resolution	Max Throughput	Analog Output Channels	Resolution	Channels	Time Related	Other Features
RTI-204	Low Cost Analog Input and Digital I/O	8 SE	12-Bit	19 kHz	0	N/A	8 Bits	2 Counter/Timers	Digital Pattern Recogni
RTI-205	Low Cost Multifunction Analog and Digital I/O	8 SE	12-Bit	19 kHz	2	12-Bit	8 Bits	2 Counter/Timers	Digital Pattern Recogni
RTI-217	Digital I/O	0	N/A	N/A	0	N/A	Four 8-Bit Ports	0	Interrupt on Change of External Strobing and Interrupt Support
RTI-220	Analog I/O	Up to 64	12-Bit	21 kHz	Up to 16	12-Bit	0	0	Interfaces Directly to Analog Signal Conditioning Panels; Slave Microprocessor Controls Analog Outputs
RTI-222	Analog Output	0	N/A	N/A	Up to 16	12-Bit	0	0	Interfaces Directly to An Signal Conditioning Pan Slave Microprocessor Co Analog Outputs

VMEbus Compatible I/O Boards

	Analog Devices Part Number	VMEbus RTI-600	VMEbus RTI-602
Board Type	Input	•	
	Input/Output		
	Output		•
Channel Capacity	Input (Single Ended/ Differential)	32/16	
	Output		4
Input Resolution	10 Bits		
	12 Bits	•	
Output Resolution	8 Bits		
	12 Bits		•
Additional Features			
Programmable Gain Amplification		•	
Single +5 V Operation		•	•
4–20 mA Output			•
Direct Sensor Interface Thermocouples, RTDs			

Multibus Compatible I/O Boards

	Analog Devices Part Number	Multibus RTI-711	Multibus RTI-724	Multibus RTI-732
Board Type	Input	•		
	Input/Output			•
	Output		•	
Channel Capacity	Input (Single Ended/ Differential)	32/16		32/16
	Output		4	2
Input Resolution	10 Bits			
	12 Bits	•		•
Output Resolution	8 Bits			
	12 Bits		•	•
Additional Features				
Programmable Gain Amplification		•		•
Single +5 V Operation		•	•	•
4–20 mA Output				•
Direct Sensor Interface Thermocouples, RTDs				

Selection Guide
Bus Interface & Serial I/O Products

µMAC Series

	µMAC-1050	µMAC-4000	µMAC-5000	µMAC-6000	µMAC-1060	µDCS-6000
Programming	**Fixed Function (PC Programming in C, Basic Pascal, 3rd Party Packages)**	**Fixed Function**	**µMACBASIC**	**µMACBASIC, C**	**C**	**FIX DMACS**
Max RAM	N/A	N/A	128K	256K	512K	256K
# Comm Ports						
Serial	1	1	2	3	3 max	3
IEEE-488	None	None	None	1	None	For Expansion Only
Max I/O Points						
AIO	48 AIN, 10 AOT	48 AIN, 32 AOT	100+*	350+*	64 AIN, 32 AOT	1000+
DIO	64	272	304	1024	128	4000+
Resolution (Bits)	18 Bits	13 Bits	11/14 Bits	12/14 Bits	13–18 Bits	12/14 Bits
Data Acquisition Rate per Channel	20	15	50/25	2800/1400 (C)	400–40	10

*Input/Output capability depends on configuration.

Mixed-Signal Application Specific Integrated Circuits

Analog Devices offers a full spectrum of signal conditioning and conversion capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 10- to 14-bit accuracy and 12- to 20-bit resolution that formerly required board-level solutions. Combined with our general purpose DSPs from the ADSP-2100 and ADSP-21000 families, our ASICs can provide custom two-chip solutions to meet complex system requirements.

Analog Devices can incorporate most of the functions of its standard monolithic linear and converter parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, England and Ireland.

Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in our MIL-38510 certified facilities.

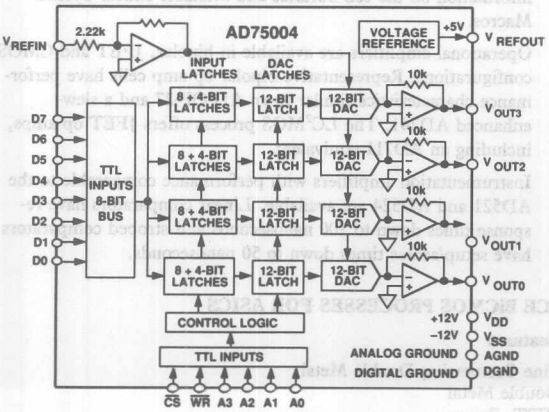
DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are three Linear System Macros, a custom chipset and a semicustom chip.

AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously. Outputs swing ±5 V, drive ±5 mA, and settle within 4 µs.

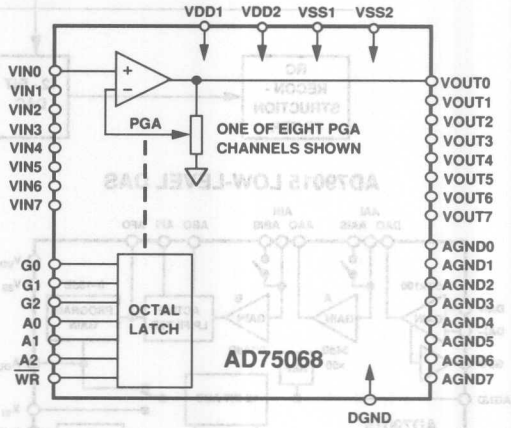
AD75004 QUAD DAC



AD75068 Octal Programmable Gain Amplifier

The AD75068 contains eight programmable gain amplifiers (PGAs). Each is complete, including switch/resistor network and gain programming latch, and requires no external components. Each channel may be independently programmed for gains from 1 to 128. A unique circuit design maintains constant 2 MHz bandwidth at all gains and offers very low phase shift; the PGAs also feature low input bias current (<4 pA).

AD75068 OCTAL PROGRAMMABLE GAIN AMPLIFIER



Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. For example, the AD75004 quad DAC could be expanded to 6 channels, each of which may have separate reference inputs. The AD75068 could be configured to include filtering. These modifications, when based on standard library cells, can provide the fastest, most cost effective semicustom solution.

Modem Chipset

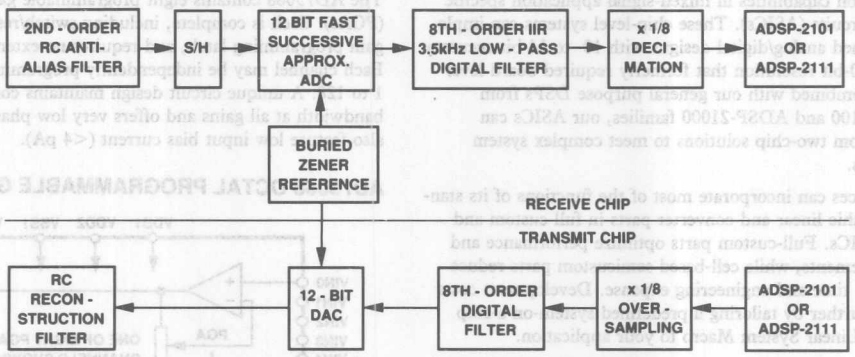
Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface an Analog Devices digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is 8 × oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.

AD79015 Low Level DAS

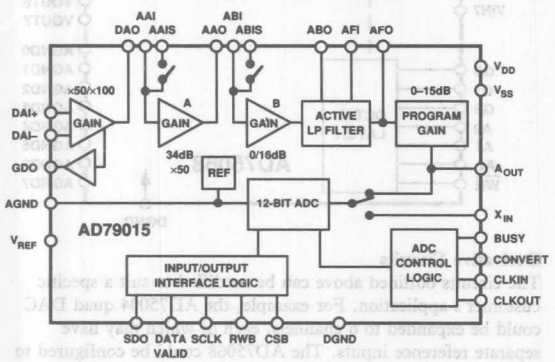
This circuit is a complete data acquisition system for low level signals (e.g., ECG and EEG) with a throughput of 10,000 samples per second. It provides high accuracy, high stability and functional completeness in a small 28-pin PLCC package. It includes a high performance instrumentation amp, low-pass and band-pass filters, and a 12-bit ADC with on-chip reference. It also includes a fast 8/12-bit serial port to interface to most microprocessor systems.

8

HIGH SPEED MODEM CHIPSET



AD79015 LOW-LEVEL DAS



HIGH PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard-product ICs. These mixed bipolar-CMOS processes include thin-film resistors which may be laser trimmed for precise matching and provide stable performance over a wide temperature range.

The ABCMOS, BiMOS II, and Linear Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 40,000 devices can be placed on a single chip. Bipolar transistors provide low noise, low offset input stages and moderate power output stages. The CMOS devices offer high input impedance, and make dense logic and analog switches for data converters, multiplexers and switched-capacitor filters. LC^2MOS also provides a JFET for very low noise amplifiers, and a low-noise buried-Zener reference. ABCMOS represents the next generation in a combined bipolar/CMOS process for mixed-signal applications.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 V to split ±15V, with signal levels ranging from single-ended +3 V to ±10 V. These processes are ideally suited for applications in avionics, instrumentation, industrial automation, computers and peripherals, and telecommunications.

The following table summarizes the processes available for designing ASICs. Other processes in development will offer even higher speed, denser logic and higher integration of analog and digital functions.

CELL LIBRARIES

Cell libraries for the bipolar/CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC^2MOS process offers JFET op amps, including an AD711 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

ANALOG DEVICES HIGH PERFORMANCE BiCMOS PROCESSES FOR ASICS

Process	Power	Signal	Features
ABCMOS	+5 V to ±5 V	+3 V to ±3 V	Fine Geometries; Double Metal
BiMOS II	±5 V to ±12 V	±3 V to ±10 V	Double Metal
LC^2MOS	+5 V to ±15 V	+3 V to ±10 V	JFET, Zener
LC^2MOS 2	+5 V to ±5 V	+3 V to ±3 V	Fine Geometries; Poly-Poly Capacitors, JFET, Zener

Digital-to-analog converters range in resolution from 8 to 16 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 16 bits in resolution, and include cells equivalent to the AD7871 and AD674.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584, and low-noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types

Frequency Range: 200 Hz to 20 kHz (switched-cap) or 100 Hz to 1 MHz (RC)

Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)

Signal/Noise and THD: >75 dB, compatible with 12-bit data acquisition.

Logic cells include gates, counters, registers, microsequencer, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTs.

COMPUTER-AIDED DESIGN TOOLS

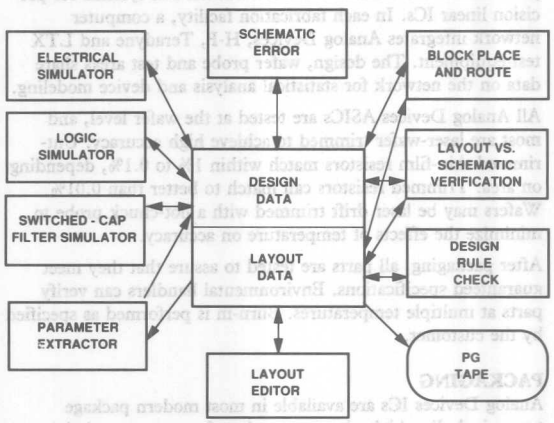
Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before signoff for final layout and fabrication.

The overall work flow through the CAD environment follows. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS™, to address these issues and to implement turn-key designs.

The JANUS schematic editor offers numerous time-saving techniques and provides for specification of such data as wire widths, routing layers and routing priorities. It automatically generates a net list used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

COMPUTER-AIDED DESIGN FLOW



Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines while autorouting noncritical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

JANUS is a trademark of Analog Devices, Inc.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, H-P, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

Available Packages

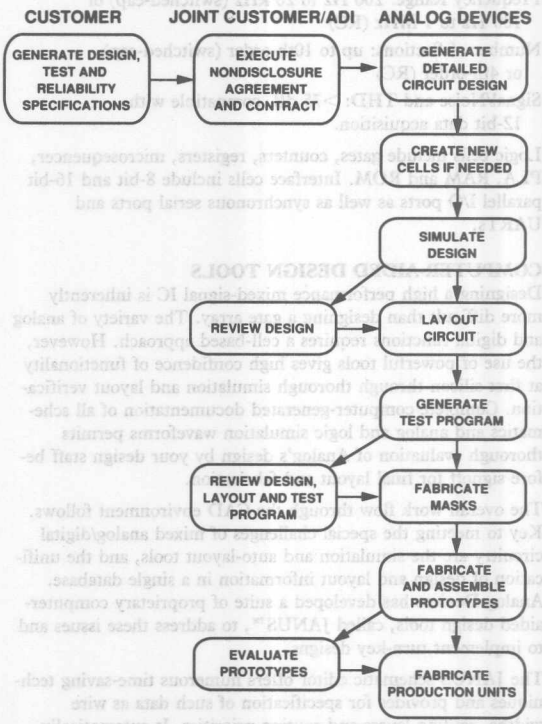
Pin Grid Array (PGA): 68 to 144 pins
Leaded Ceramic Chip Carrier (LDCC): 44 pins
Plastic Quad Flat Pack (PQFP): 44 to 132 pins
Plastic Leaded Chip Carrier (PLCC): 20 to 68 pins
Plastic Dual Inline Package (DIP): 14 to 64 pins
Side-Brazed DIP: 14 to 64 pins
Frit-Seal DIP (Cerdip): 14 to 40 pins
Small Outline (SO): 14 to 28 pins
Ceramic Quad Flat Pack (CQFP): 80 to 104 leads

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

PROGRAM RESPONSIBILITIES AND INTERFACES



Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements
- Input Voltage Range: 105 V ac to 125 V ac
- Frequency: 50 Hz to 250 Hz

Electrical Specifications
- Temperature Coefficient: 0.02%/°C
- Output Voltage Accuracy: ±2%, max
  See Specifications Table
- Breakdown Voltage: 500 V rms, min
- Isolation Resistance: 50 MΩ
- Short Circuit Protection: All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements
- Operating Temperature Range: −25°C to +71°C
- Storage Temperature Range: −25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.45
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling

No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p (with 15 µF tantalum capacitor across each output) 2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7 A	±0.5%	±0.01%	62%	3.5×2.5×0.88

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Supplies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

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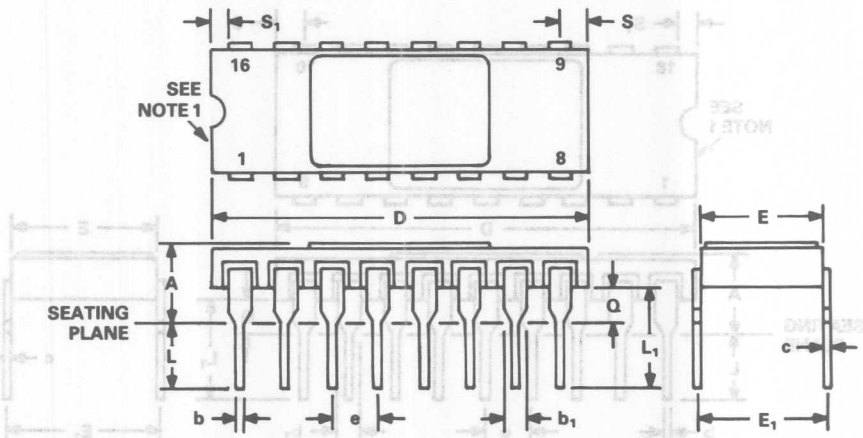
ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
Side Brazed DIP (Ceramic)				
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D-18	XB*	18-Lead	D6-3	10-4
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	F*	16-Lead		10-27
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*Special Order Only

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ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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N-24	P	24-Lead (Narrow Body)		10-34
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D-16
16-Lead Side Brazed Ceramic DIP

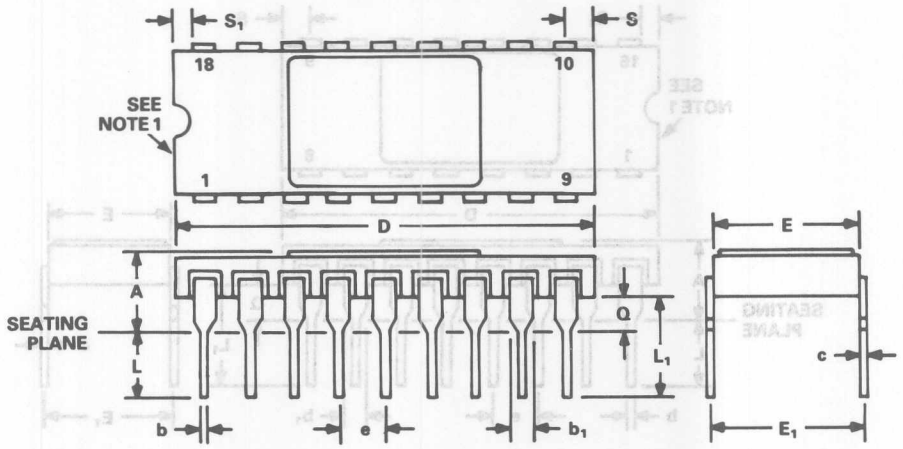


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

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D-18
18-Lead Side Brazed Ceramic DIP

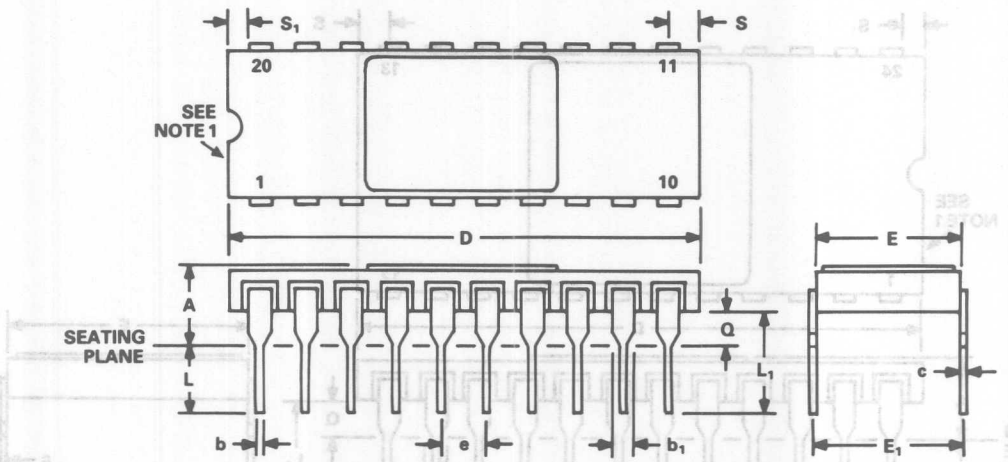


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

D-20
20-Lead Side Brazed Ceramic DIP

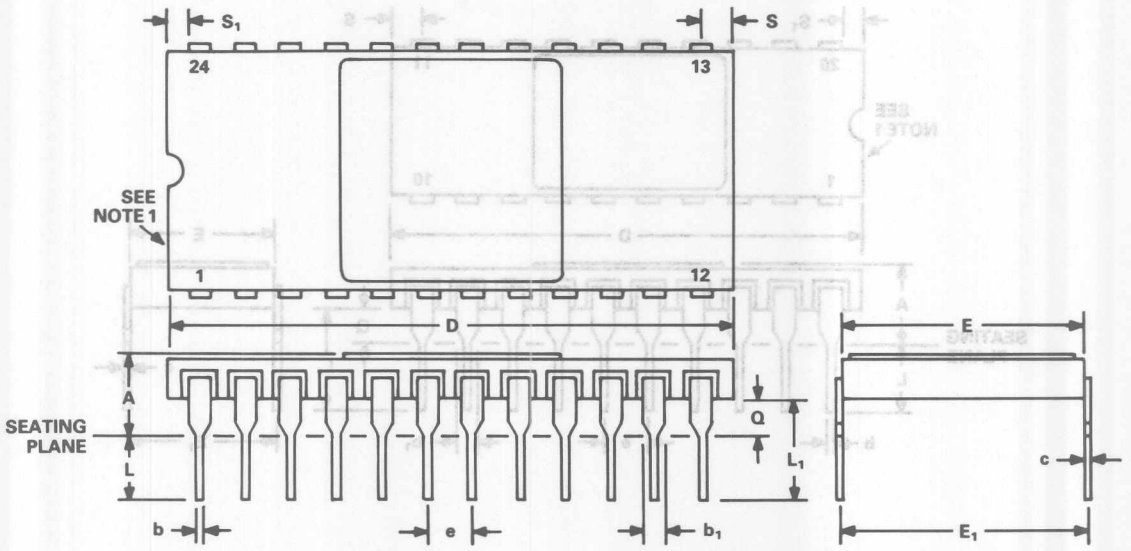


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

D-24
24-Lead Side Brazed Ceramic DIP

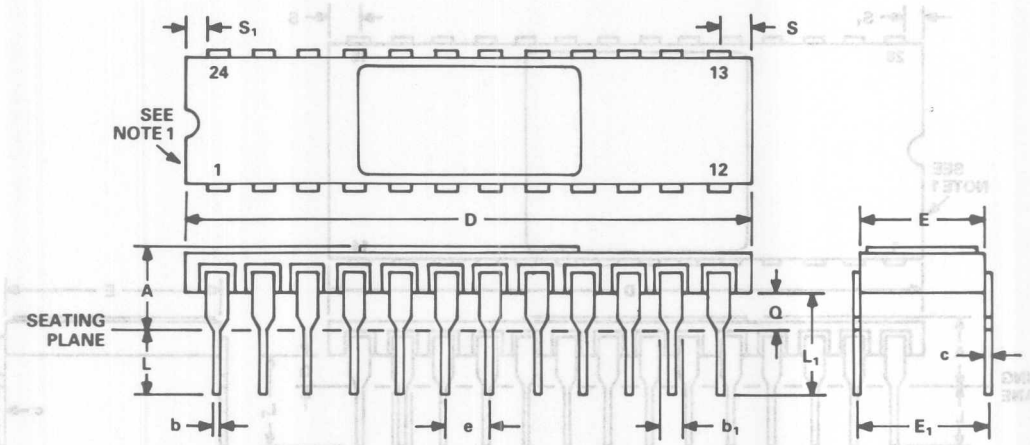


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.120	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

D-24A

24-Lead Side Brazed Ceramic DIP (Single Width)

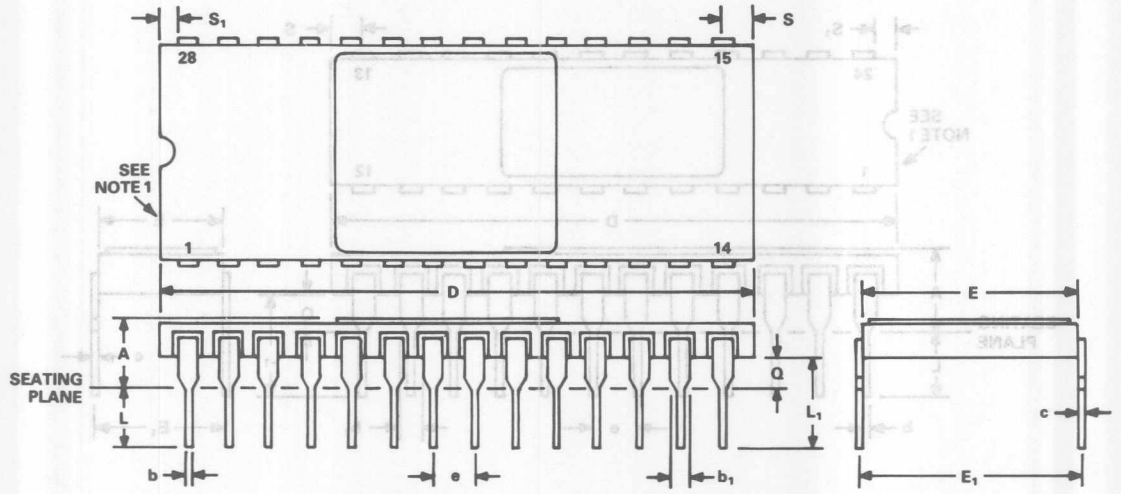


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

D-28
28-Lead Side Brazed Ceramic DIP

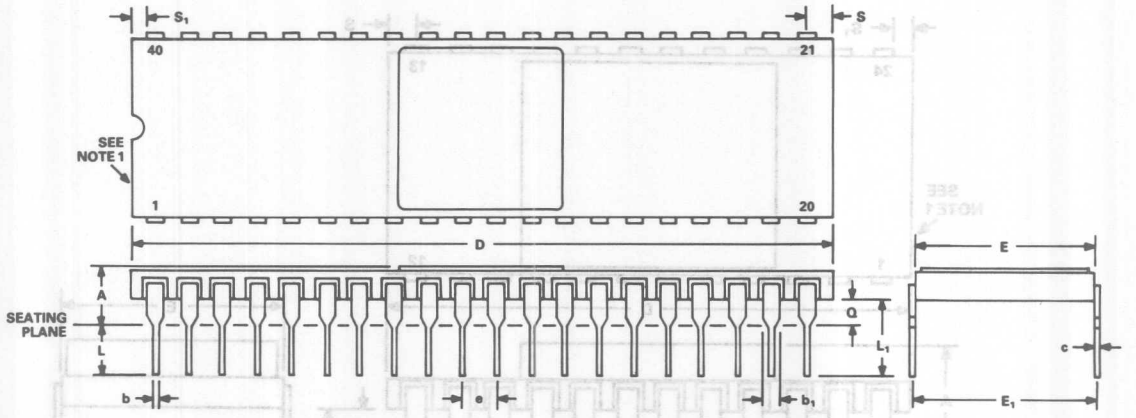


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.018	0.20	0.46	6
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.100		2.54	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

D-40

40-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.096		53.24	4
E	0.590	0.620	12.95	15.75	4
E_1	0.520	0.630	13.21	16.00	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

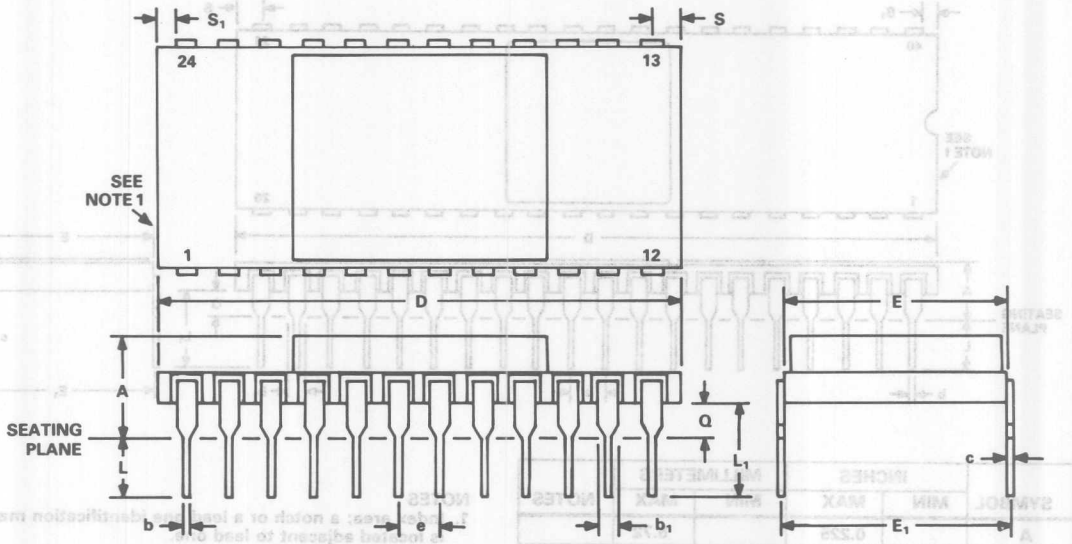
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Thirty-eight spaces.

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DH-24A

24-Lead Side Brazed Ceramic DIP for Hybrid



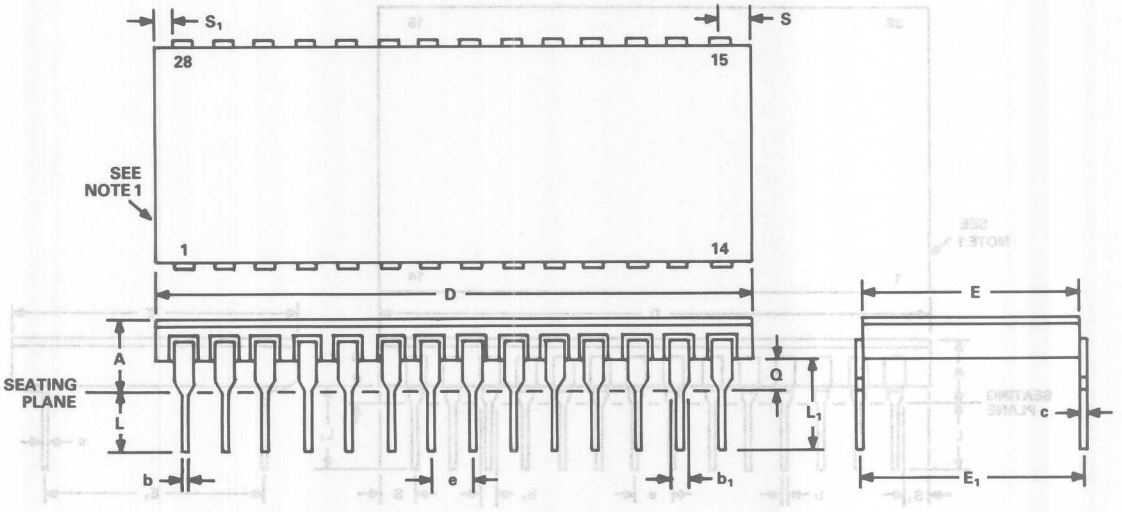
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.212		30.79	
E	0.580	0.605	14.73	15.37	
E_1	0.590	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

DH-28

28-Lead Side Brazed Ceramic DIP for Hybrid (Large Cavity)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.414		35.92	
E	0.580	0.610	14.73	15.49	
E_1	0.590	0.610	14.99	15.49	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.01	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

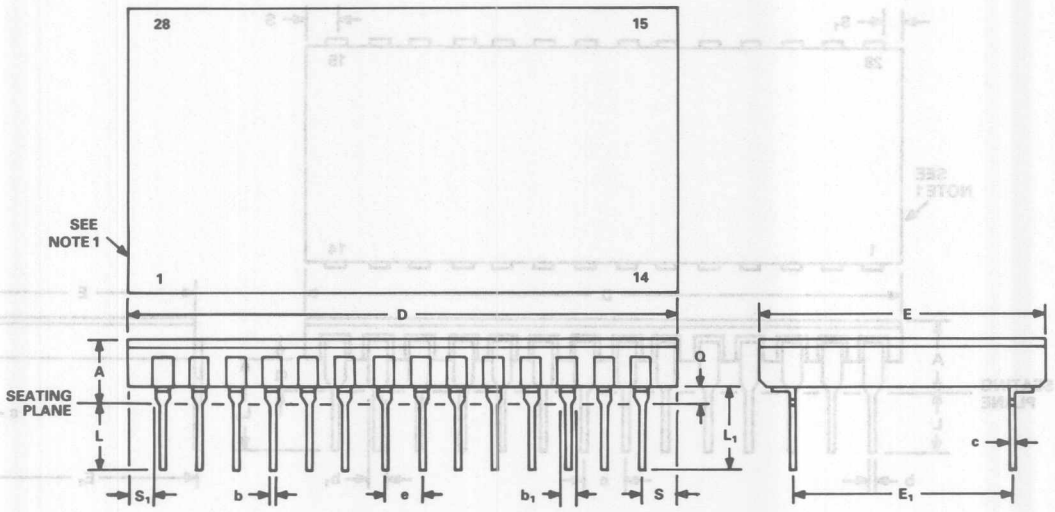
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-six spaces.

10

DH-28A

28-Lead Bottom Brazed Ceramic DIP for Hybrid

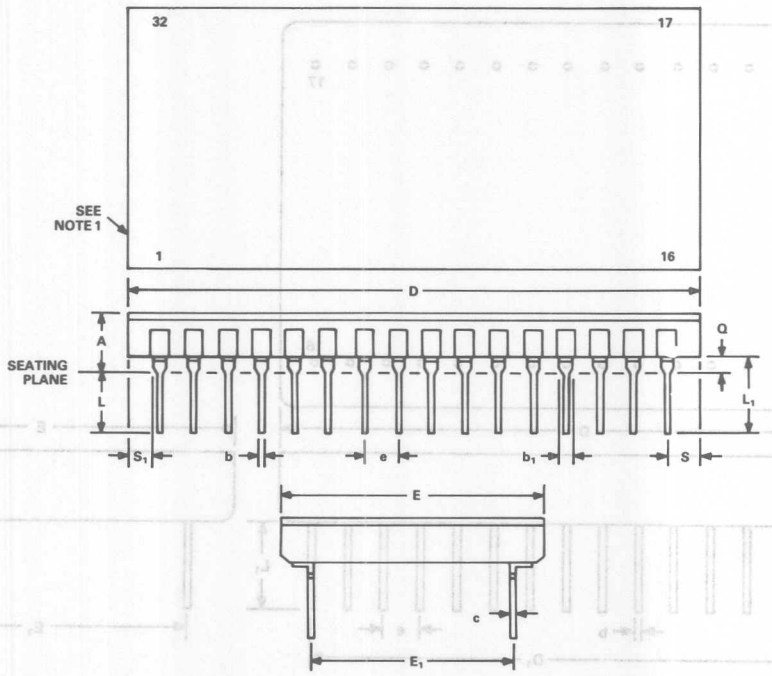


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.575		40.01	
E	0.770	0.810	19.56	20.57	
E_1	0.550	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.137		3.48	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-six spaces.

DH-32E
32-Lead Bottom Brazed Ceramic DIP

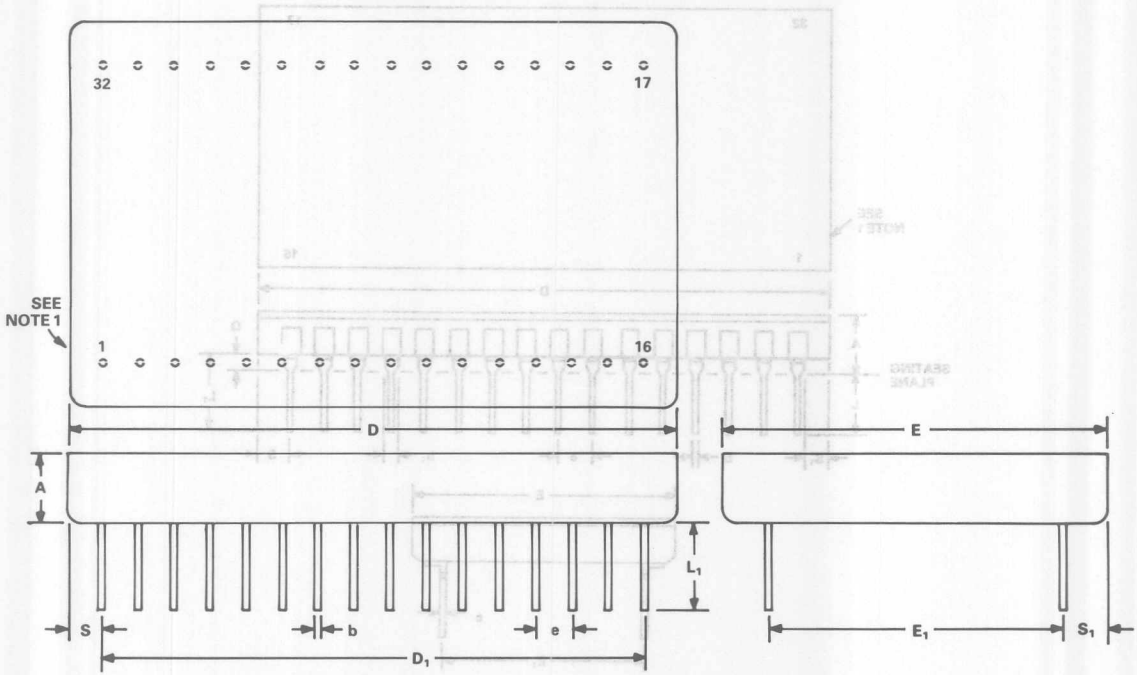


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.750		44.45	
E	1.075	1.105	27.31	28.07	
E_1	0.890	0.910	22.61	23.11	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.120		3.05	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

M-32
32-Lead Metal Platform DIP

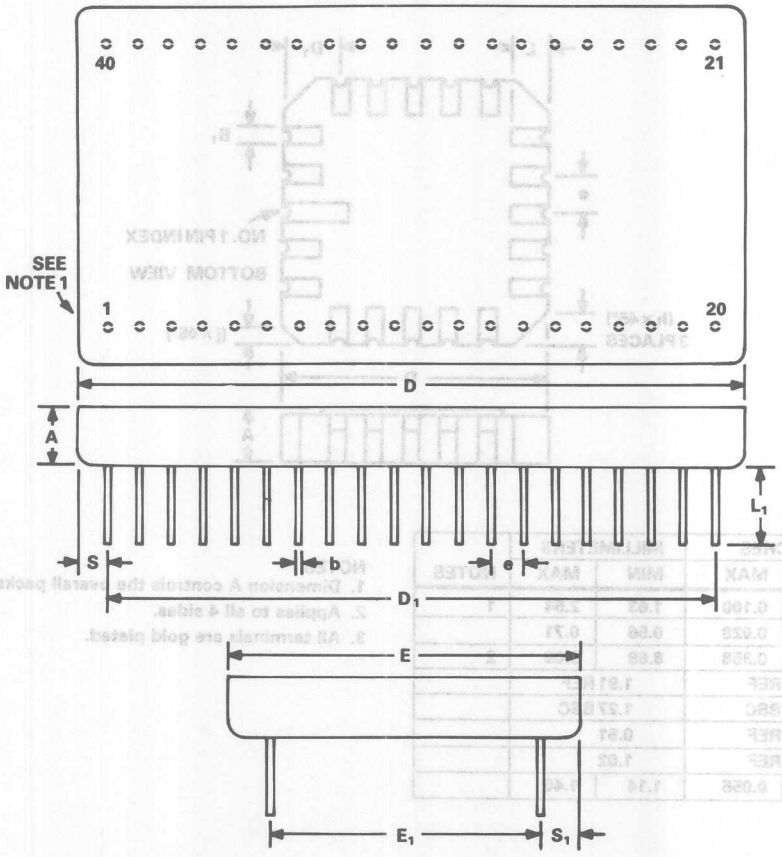


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b		0.020		0.51	
D		1.745		44.323	
D_1	1.494	1.506	37.948	38.252	
E		1.145		29.083	
E_1	0.880	0.920	22.352	23.368	3
e	0.098	0.102	2.49	2.59	4
L_1	0.240		6.09		
S	0.115	0.135	2.92	3.43	2
S_1	0.115	0.135	2.92	3.43	2

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Thirty spaces.

M-40
40-Lead Metal Platform DIP

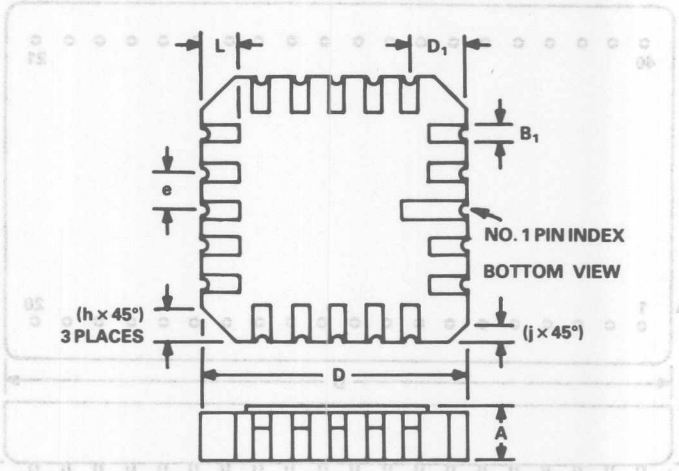


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.19		4.83	
b		0.020		0.51	
D		2.145		54.483	
D_1	1.894	1.906	48.108	48.412	
E		1.145		29.083	
E_1	0.880	0.920	22.352	23.368	3
e	0.098	0.102	2.49	2.59	4
L_1	0.240		6.09		
S	0.115	0.135	2.92	3.43	2
S_1	0.115	0.135	2.92	3.43	2

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Thirty-eight spaces.

10

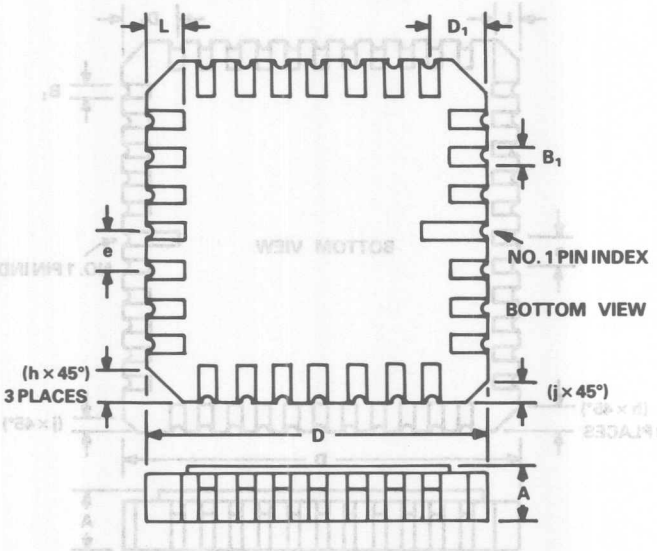
E-20A
20-Terminal Leadless Ceramic Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

E-28A
28-Terminal Leadless Ceramic Chip Carrier

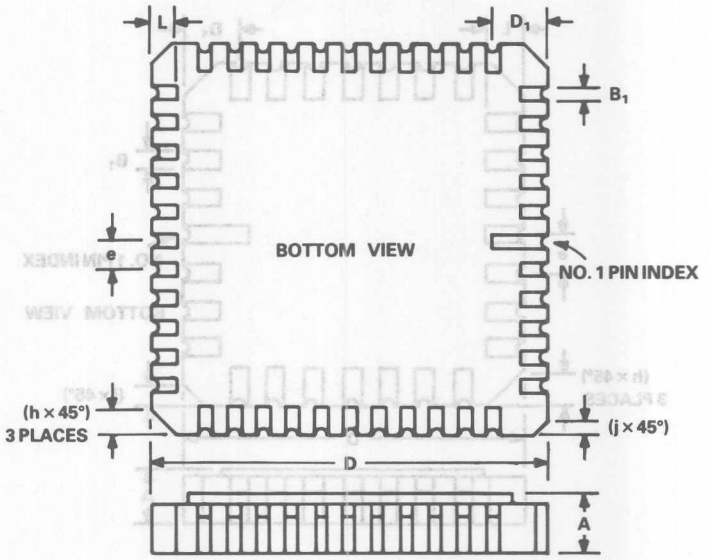


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.442	0.458	11.23	11.63	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

10

E-44A
44-Terminal Leadless Ceramic Chip Carrier

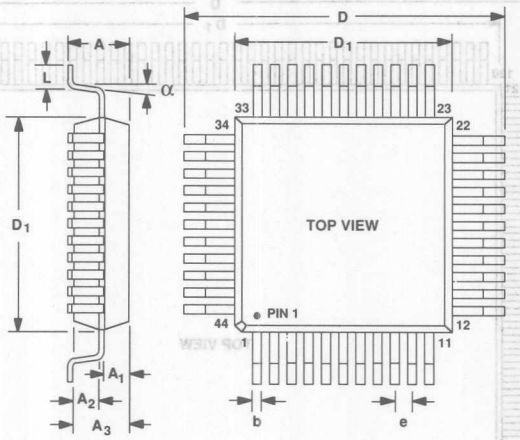


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.640	0.662	16.27	16.82	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

S-44

44-Lead Plastic Quad Flatpack (PQFP)

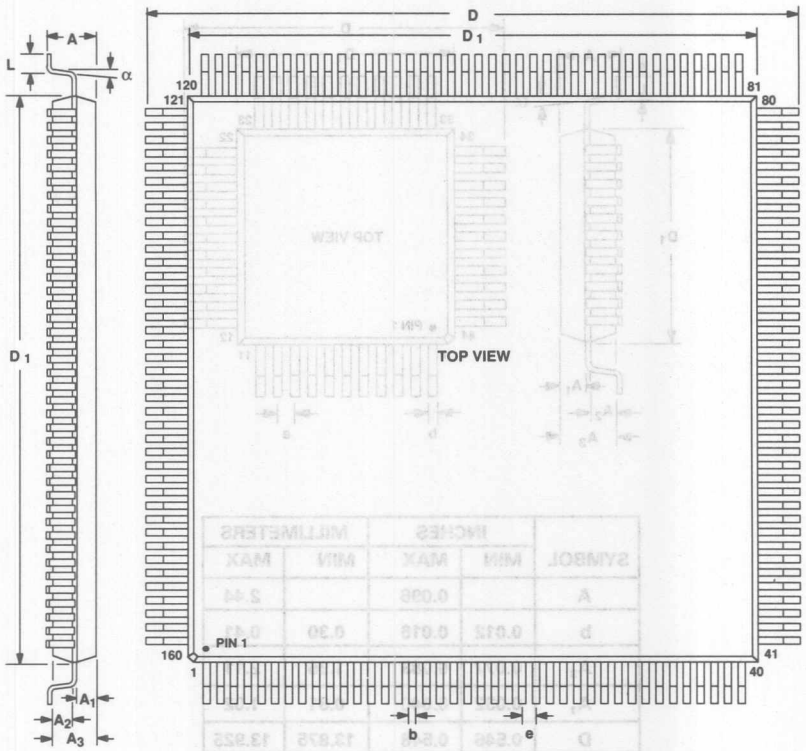


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.096		2.44
b	0.012	0.016	0.30	0.41
A_3	0.077	0.083	1.96	2.11
A_1	0.032	0.040	0.81	1.02
D	0.546	0.548	13.875	13.925
A_2	0.032	0.040	0.81	1.02
D_1	0.390	0.398	9.91	10.11
e	0.029	0.033	0.74	0.84
L	0.025	0.037	0.64	0.94
α	0.8	8.0°		

10

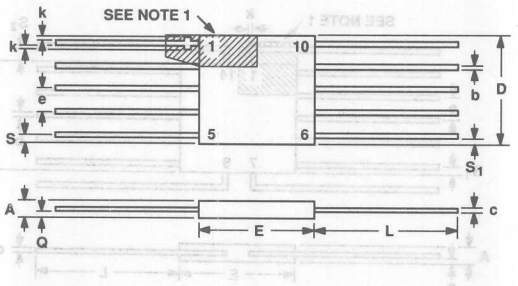
S-160

160-Lead Plastic Quad Flatpack (PQFP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.160		4.07
A_1	0.062	0.070	1.57	1.77
A_2	0.062	0.070	1.57	1.77
A_3	0.125	0.145	3.17	3.67
D	1.246	1.266	31.65	32.15
E	1.098	1.106	27.90	28.10
D_1	1.098	1.106	27.90	28.10
e	0.029	0.033	0.75	0.85
L	0.025	0.037	0.65	0.95
b	0.012	0.016	0.30	0.14
E_1	1.098	1.106	27.90	28.10
α	0.0°	8.0°		

10-Lead Cerpack/Flatpack
(L-Suffix)

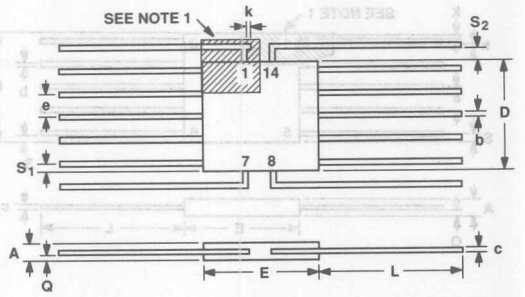


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	
b	0.010	0.019	0.25	0.48	
c	0.003	0.006	0.08	0.15	
D		0.290		7.37	3
E	0.240	0.260	6.10	6.60	
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S		0.045		1.14	5
S_1	0.005		0.13		5, 6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050″ (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000″ (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

14-Lead Cerpack/Flatpack
(M-Suffix)

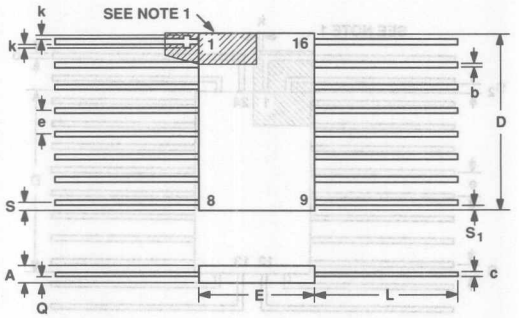


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.030	0.085	0.76	2.16	
b	0.010	0.019	0.25	0.48	
c	0.003	0.006	0.08	0.15	
D		0.280		7.11	3
E	0.240	0.260	6.10	6.60	
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S_1	0.005		0.13		5, 6
S_2	0.004		0.10		

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050" (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000" (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

16-Lead Cerpack/Flatpack
(F-Suffix)

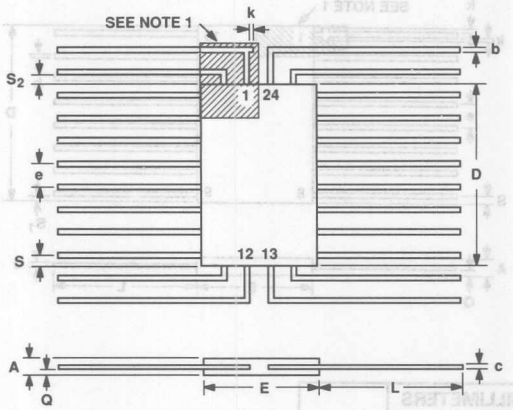


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.085	1.14	2.16	
b	0.015	0.019	0.38	0.48	
c	0.003	0.006	0.08	0.15	
D		0.440		11.18	3
E	0.245	0.285	6.22	7.24	
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.23	1.02	2
S		0.045		1.14	5
S_1	0.005		0.13		5, 6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050" (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000" (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

24-Lead Cerpack/Flatpack
(N-Suffix)

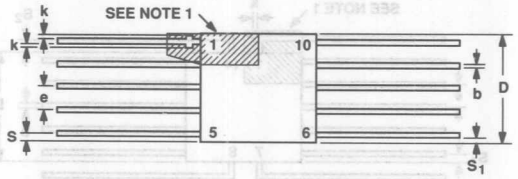


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.090	1.14	2.29	
b	0.015	0.019	0.38	0.48	
c	0.003	0.006	0.08	0.15	
D		0.430		10.92	3
E	0.245	0.285	6.22	7.24	
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S	0.005		0.13		5, 6
S_2	0.004		0.10		

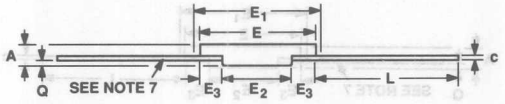
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050″ (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000″ (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

10-Lead Flatpack
(L-Suffix)



Bottom-Brazed (LB-Suffix)

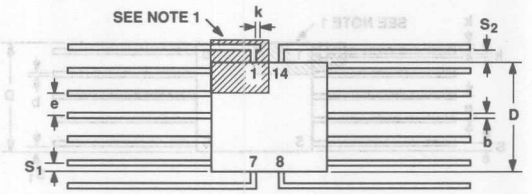


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	
b	0.010	0.019	0.25	0.48	
c	0.003	0.006	0.08	0.15	
D		0.290		7.37	3
E	0.240	0.260	6.10	6.60	
E_1		0.280		7.11	3
E_2	0.125		3.18		
E_3	0.030		0.76		
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S		0.045		1.14	5
S_1	0.005		0.13		5, 6

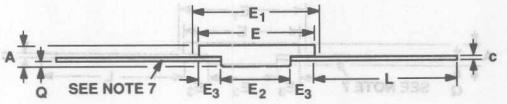
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050" (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000" (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

14-Lead Flatpack
(M-Suffix)



Bottom-Brazed (MB-Suffix)

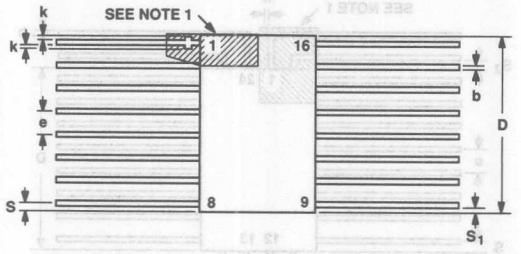


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	
b	0.010	0.019	0.25	0.48	
c	0.003	0.006	0.08	0.15	
D		0.280		7.11	3
E	0.240	0.260	6.10	6.60	
E_1		0.280		7.11	3
E_2	0.125		3.18		
E_3	0.030		0.76		
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S_1	0.005		0.13		5, 6
S_2	0.004		0.10		

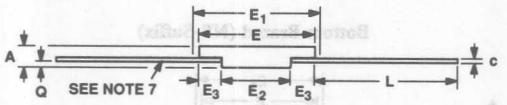
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050″ (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000″ (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

16-Lead Flatpack
(F-Suffix)



Bottom-Brazed (FB-Suffix)

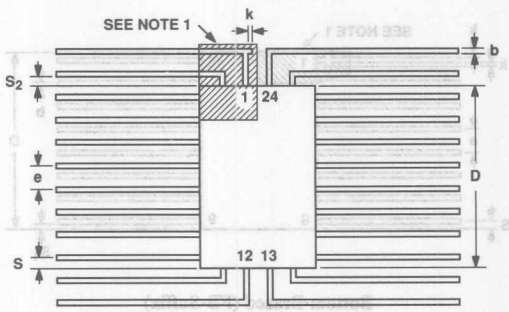


	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.045	0.085	1.14	2.16	
b	0.015	0.019	0.38	0.48	
c	0.003	0.006	0.08	0.15	
D		0.440		11.18	3
E	0.245	0.285	6.22	7.24	
E_1		0.305		7.75	3
E_2	0.130		3.30		
E_3	0.030		0.76		
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.23	1.02	2
S		0.045		1.14	5
S_1	0.005		0.13		5, 6

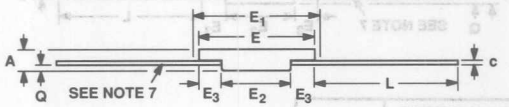
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050" (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000" (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

24-Lead Flatpack
(N-Suffix)



Bottom-Brazed (NB-Suffix)

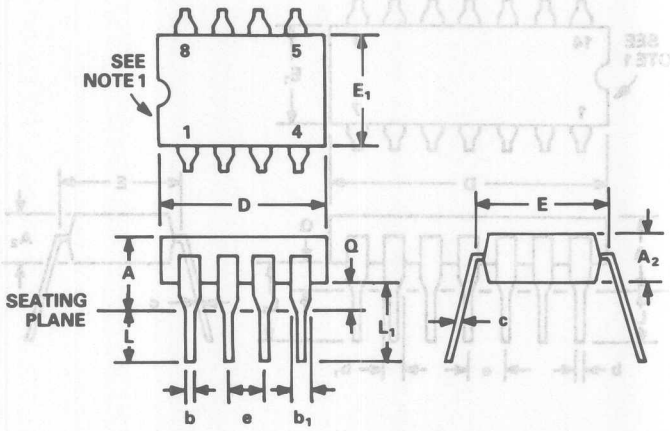


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.045	0.090	1.14	2.29	
b	0.015	0.019	0.38	0.48	
c	0.003	0.006	0.08	0.15	
D		0.430		10.92	3
E	0.245	0.285	6.22	7.24	
E_1		0.305		7.75	3
E_2	0.125		3.18		
E_3	0.030		0.76		
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	
Q	0.010	0.040	0.25	1.02	2
S	0.005		0.13		5, 6
S_2	0.004		0.10		

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050″ (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 may be 0.000″ (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see Note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

N-8
8-Lead Plastic DIP

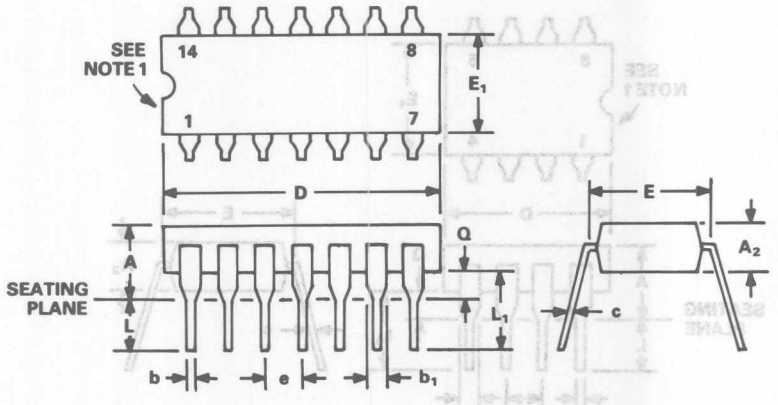


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

10

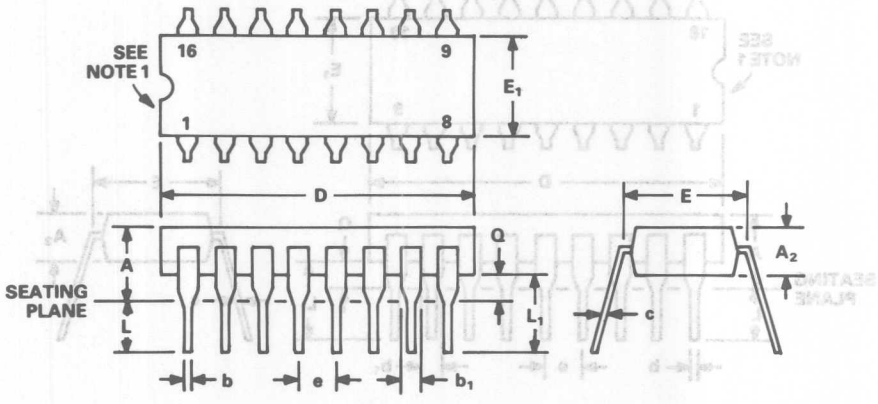
N-14
14-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-16
16-Lead Plastic DIP



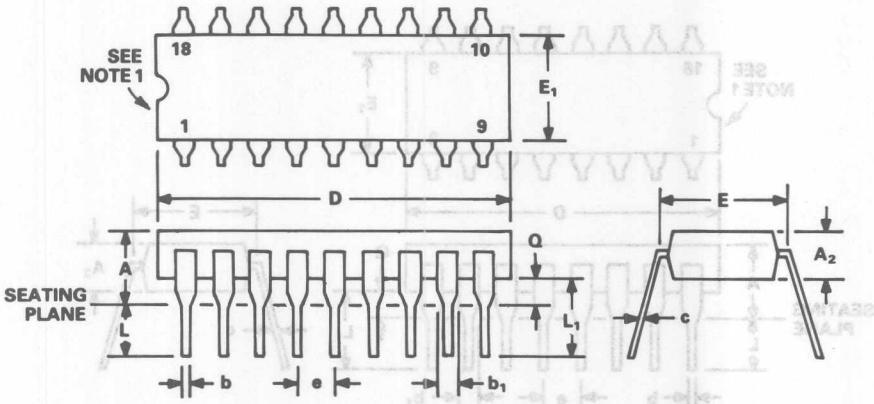
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

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N-18
18-Lead Plastic DIP

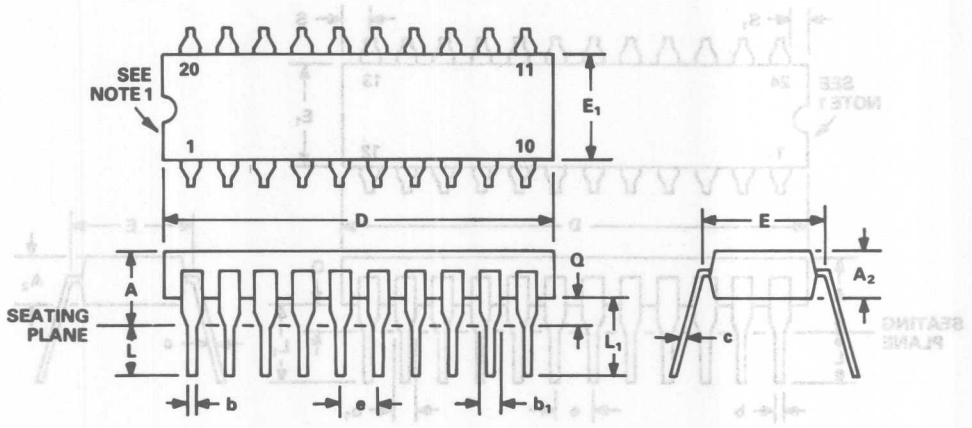


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-20
20-Lead Plastic DIP



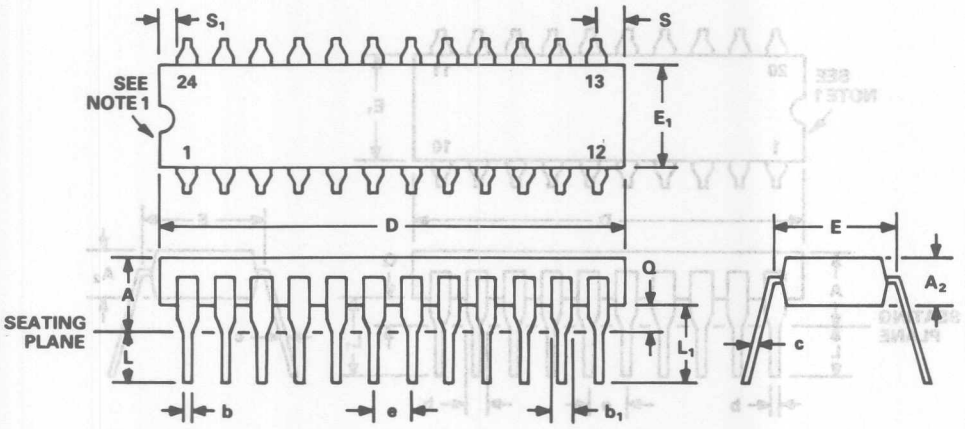
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

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N-24
24-Lead Plastic DIP

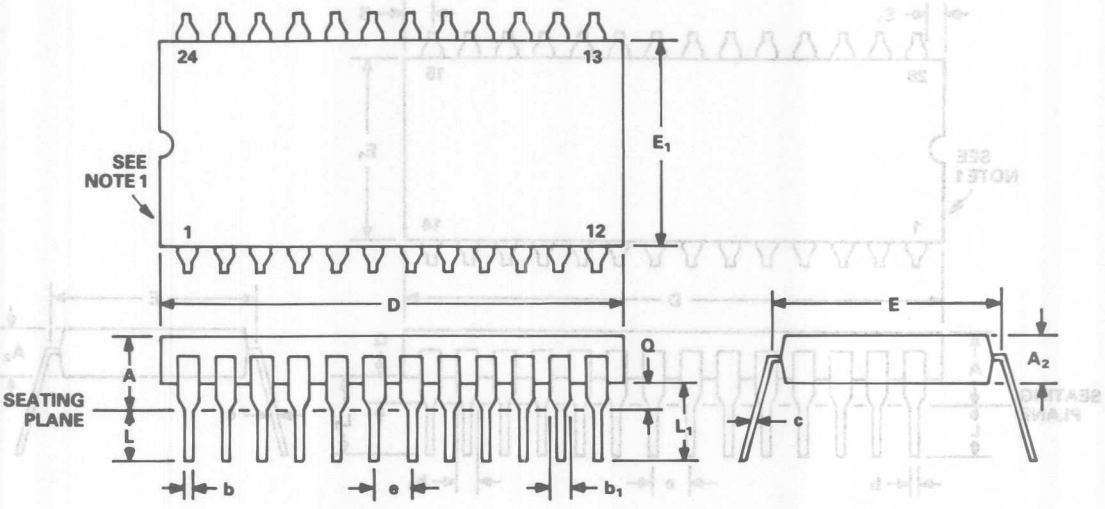


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.60	32.30	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

N-24A
24-Lead Plastic DIP (Double Width)



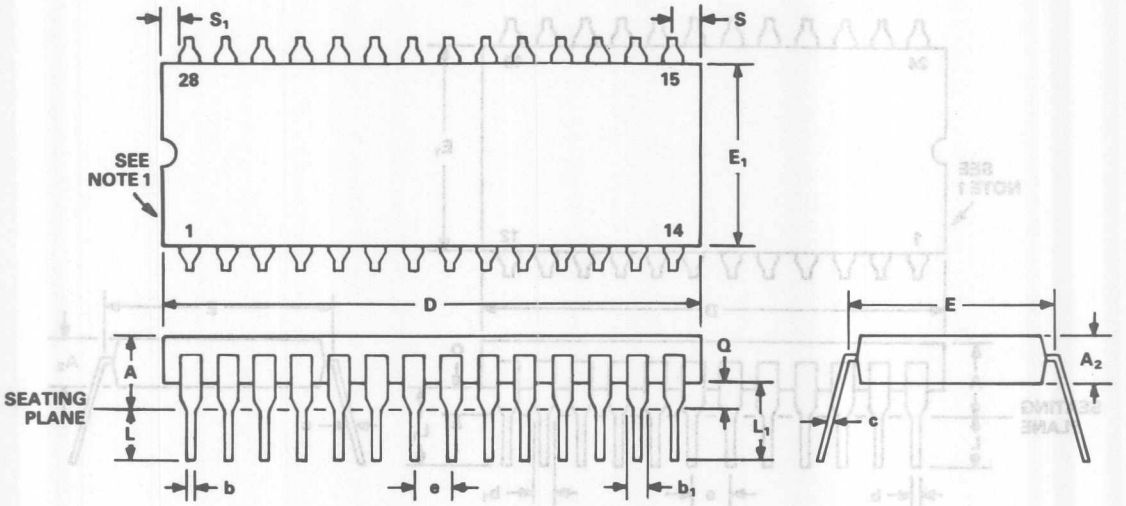
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.030	0.070	0.77	1.77	
c	0.008	0.015	0.204	0.381	
D	1.150	1.290	29.30	32.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

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N-28
28-Lead Plastic DIP

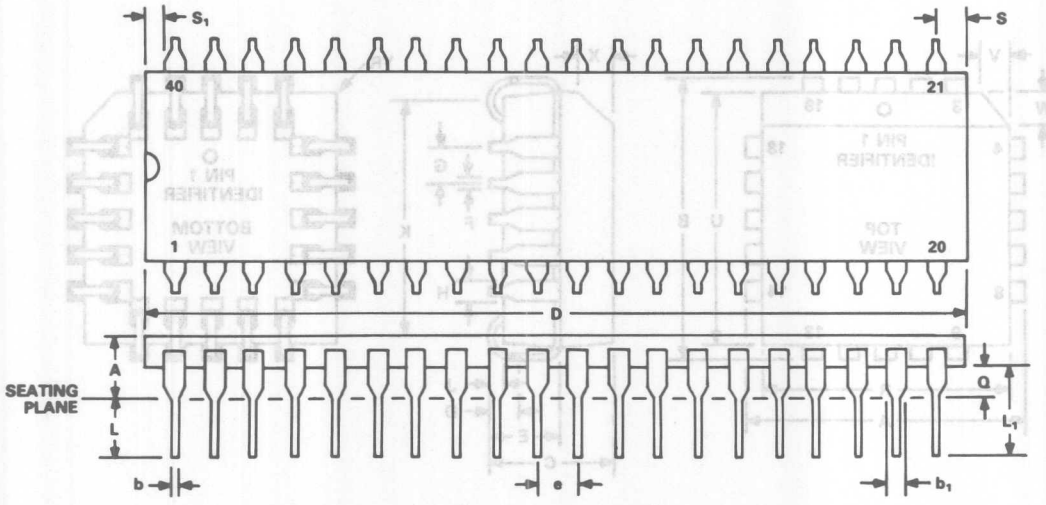


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1		0.070		1.77	
c	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.10	39.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

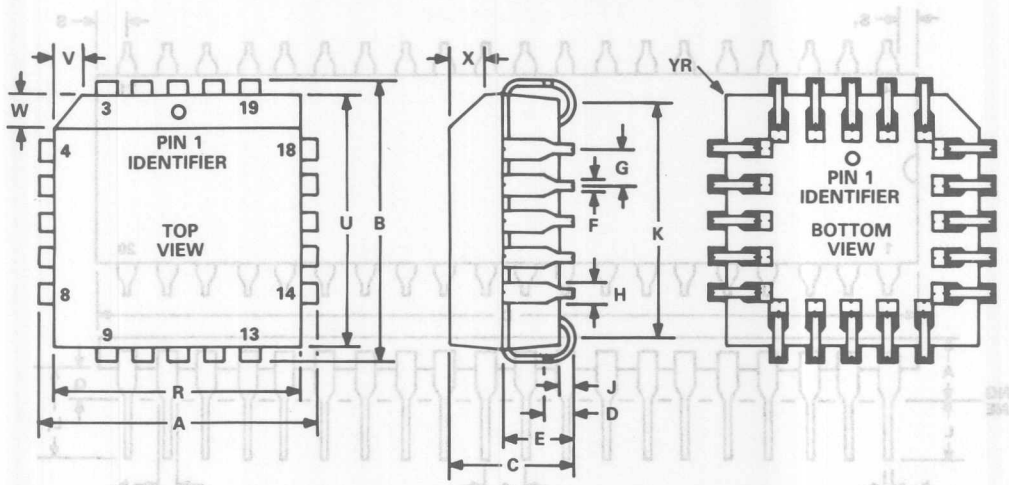
N-40A
40-Pin Plastic DIP



NOTE:
LEADS ARE SOLDER-PLATED KOVAR OR ALLOY 42

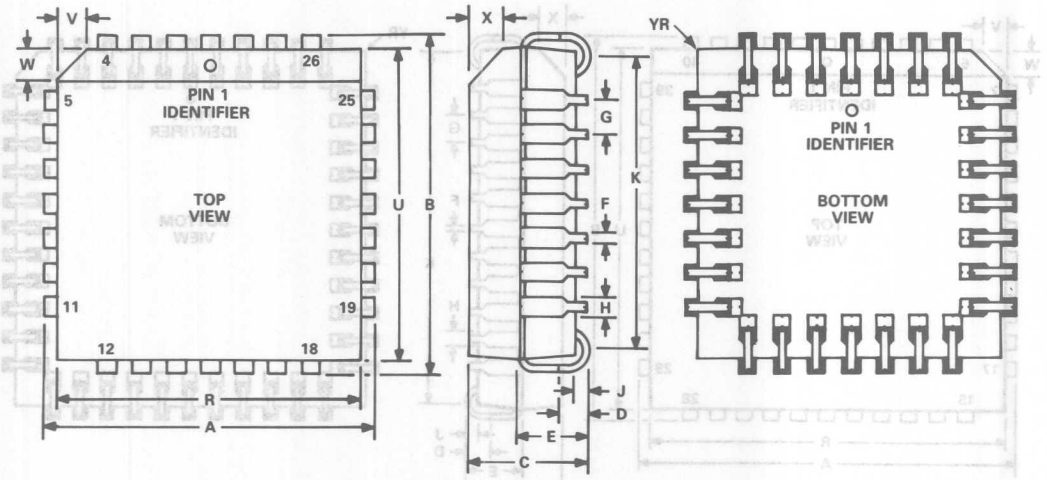
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
b	0.015	0.025	0.38	0.64
b_1	0.040	0.060	1.02	1.52
c	0.008	0.015	0.20	0.38
D	–	2.08	–	52.83
E	0.550	0.550	13.46	13.97
E_1	0.580	0.620	14.73	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.175	3.05	4.45
L_1	0.140	–	3.56	–
Q	0.015	0.060	0.38	1.52
S	–	0.110	–	2.79
S_1	0.005	–	0.13	–
α	0°	15°	0°	15°

P-20A
20-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

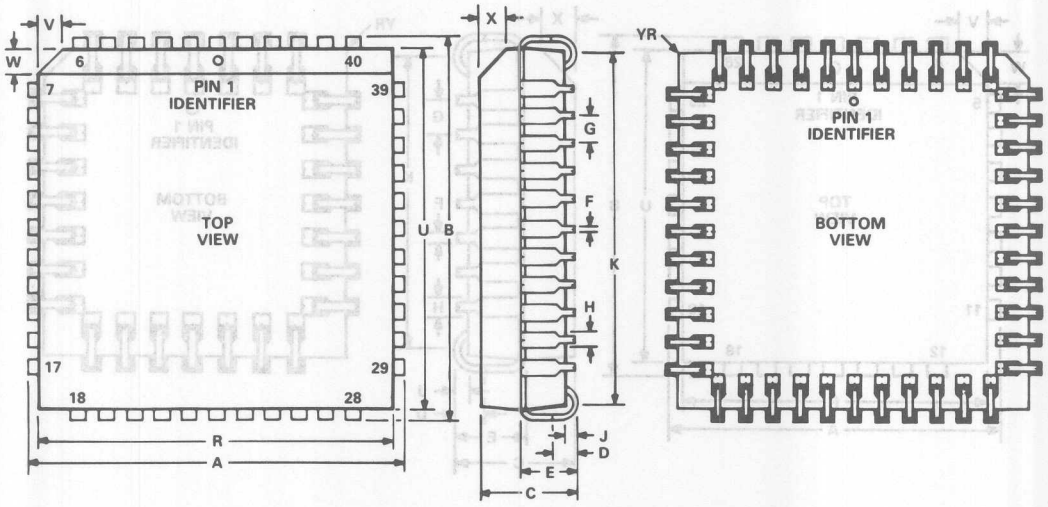
P-28A
28-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-44A

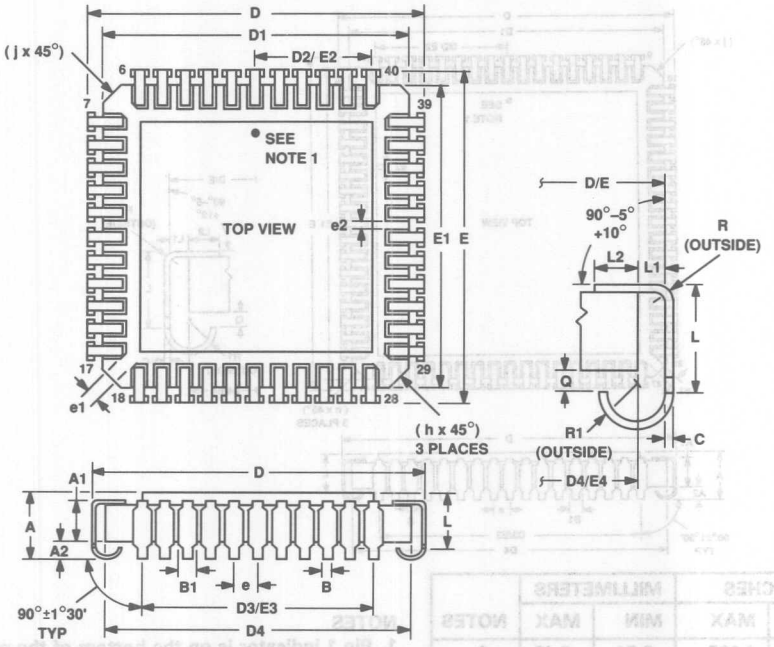
44-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.650	0.656	16.51	16.66
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

J-44

44-Lead J-Leaded Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.100	0.135	2.54	3.43	2
A1	0.054	0.078	1.37	1.98	
A2	0.025		0.64		
B	0.013	0.023	0.33	0.58	3
B1	0.020	0.032	0.51	0.81	3
C	0.006	0.013	0.15	0.33	3
D/E	0.680	0.700	17.27	17.78	
D1/E1	0.628	0.662	15.95	16.82	
D2/E2	0.250 BSC		6.35 BSC		
D3/E3	0.500 BSC		12.70 BSC		
D4/E4	0.610	0.650	15.49	16.51	
e	0.050 BSC		1.27 BSC		
e1/e2	0.012		0.30		
L	0.030		0.76		
L1	0.005		0.12		
L2	0.025		0.76		
Q	0.003		0.08		
R	0.015		0.38		
R1	0.025	0.040	0.76	1.02	
h	0.040 REF		1.02 REF		
j	0.020 REF		0.52 REF		

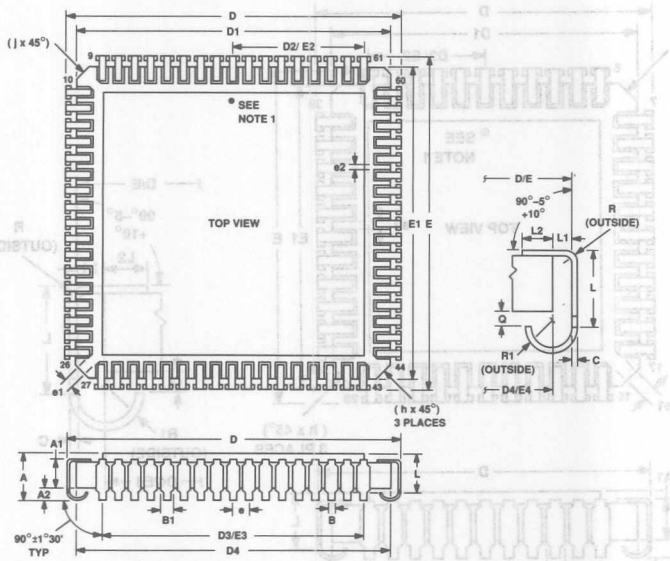
NOTES

1. Pin 1 indicator is on the bottom of the package.
2. Dimension A controls the overall package thickness.
3. All leads—increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.

10

J-68

68-Lead J-Leaded Chip Carrier

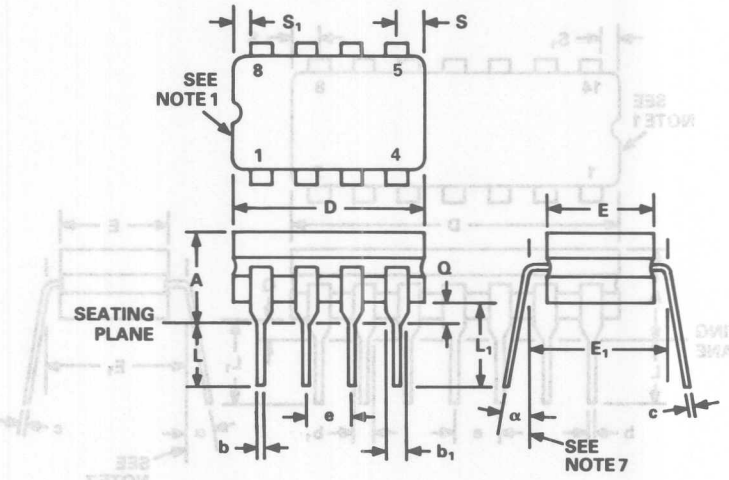


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.100	0.135	2.54	3.43	2
A_1	0.069	0.091	1.75	2.31	
A_2	0.025		0.64		
B	0.013	0.023	0.33	0.58	3
B_1	0.020	0.032	0.51	0.81	3
C	0.006	0.013	0.15	0.33	3
D/E	0.980	1.000	24.89	25.4	
D1/E1	0.920	0.960	23.37	24.38	
D2/E2	0.400 BSC		10.16 BSC		
D3/E3	0.800 BSC		20.32 BSC		
D4/E4	0.910	0.950	23.11	24.13	
e	0.050 BSC		1.27 BSC		
e1/e2	0.012		0.30		
L	0.030		0.76		
L1	0.005		0.12		
L2	0.025		0.76		
Q	0.003		0.08		
R	0.015		0.38		
R1	0.025	0.040	0.76	1.02	
h	0.040 REF		1.02 REF		
j	0.020 REF		0.52 REF		

NOTES

1. **Pin 1 indicator is on the bottom of the package.**
2. **Dimension A controls the overall package thickness.**
3. **All leads—increase maximum limit by 0.0003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.**

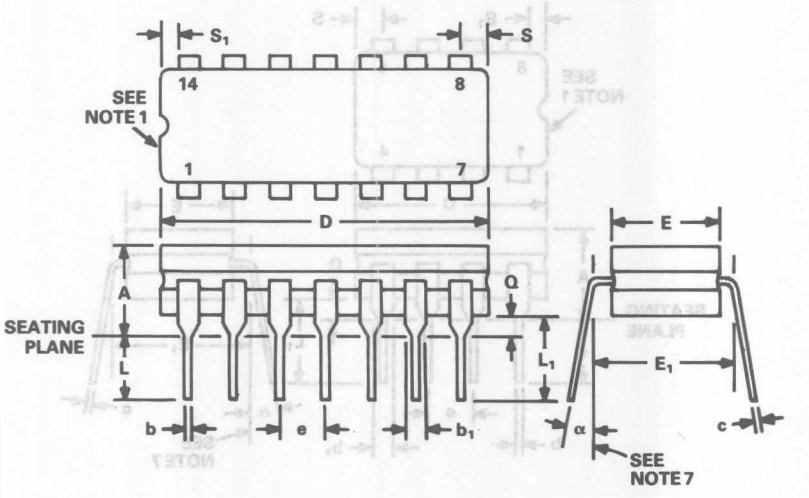
Q-8
8-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

Q-14
14-Lead Cerdip

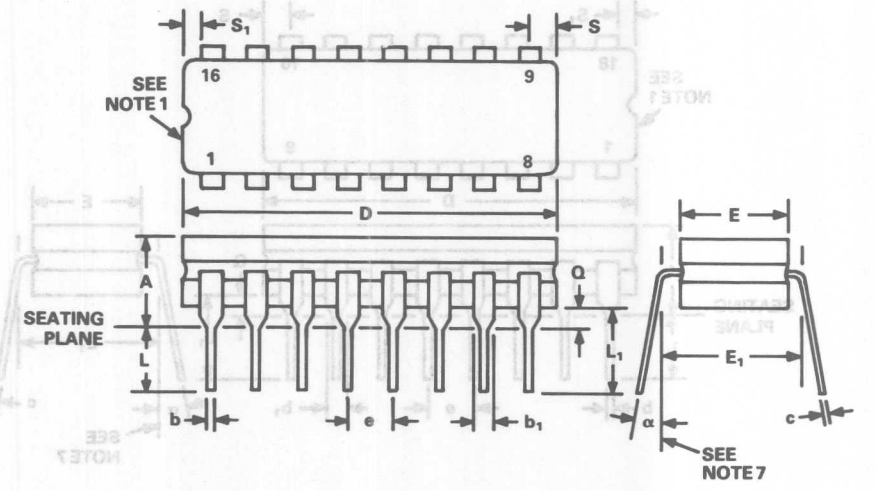


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

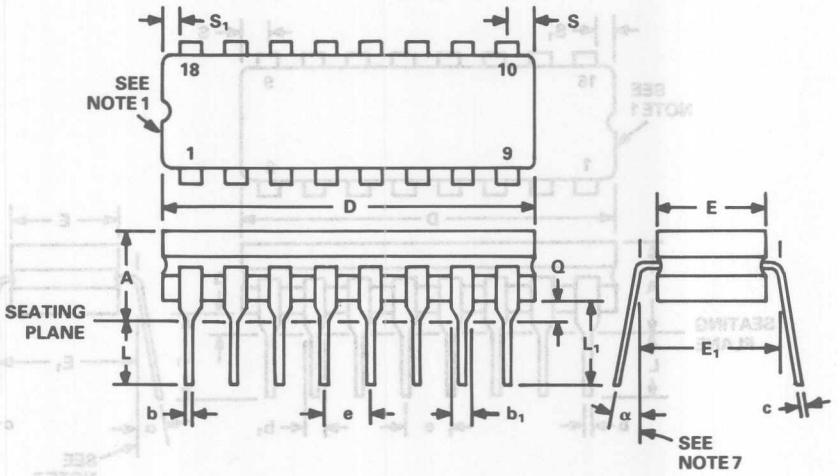
Q-16
16-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

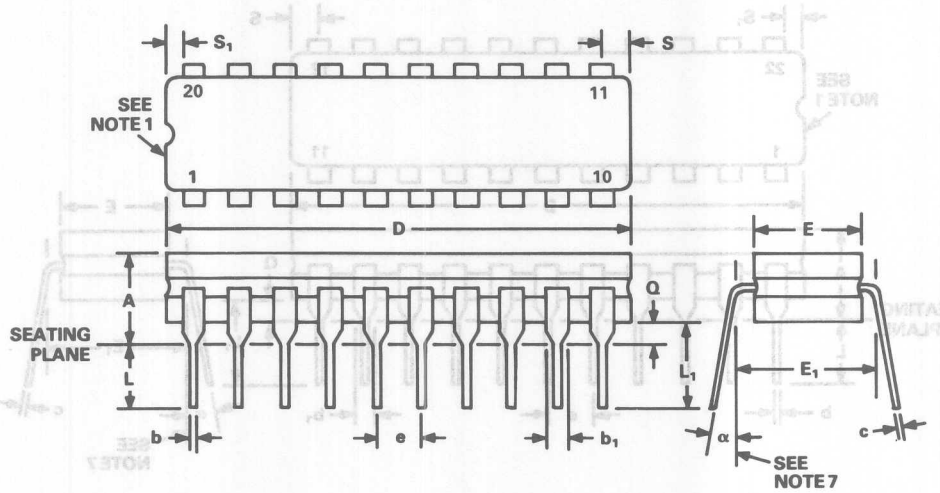
Q-18
18-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

Q-20
20-Lead Cerdip

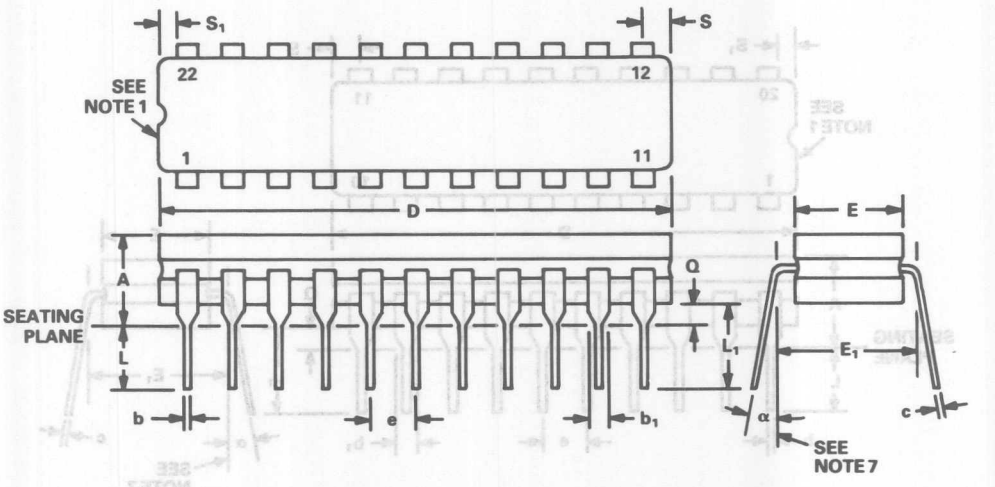


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

10

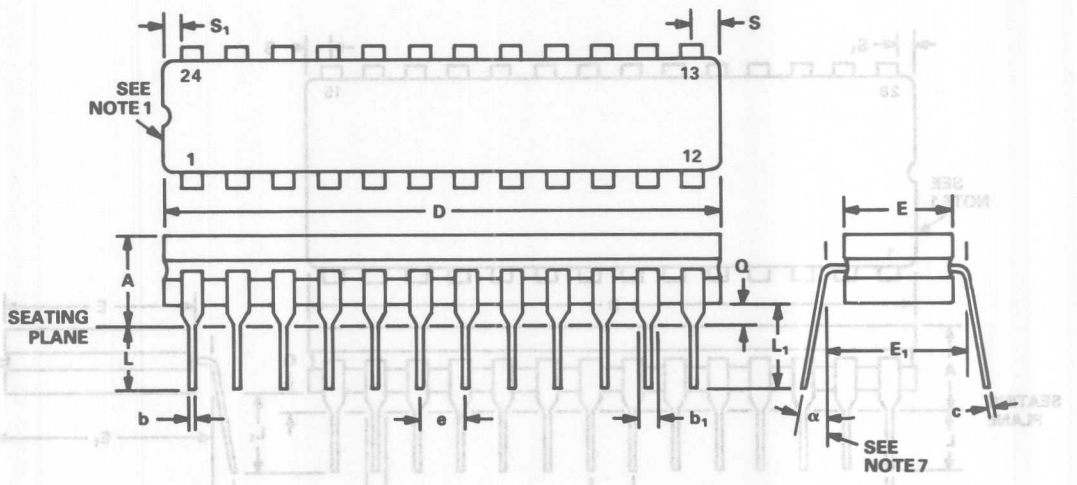
Q-22
22-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.175		29.85	4
E	0.320	0.410	8.13	10.41	4
E_1	0.390	0.420	9.09	10.67	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1		0.150		3.81	
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty spaces.

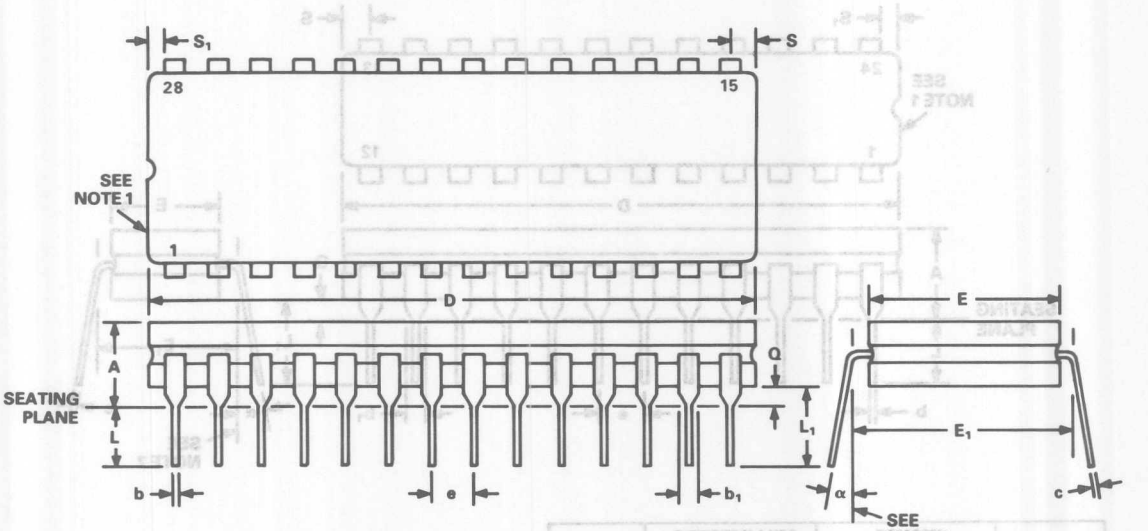
Q-24
24-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

Q-28
28-Lead Cerdip

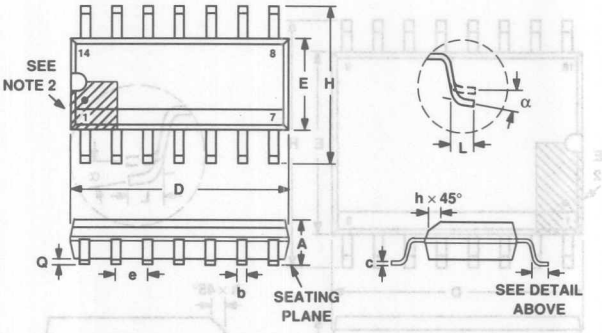


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-six spaces.

SO-14

14-Lead Narrow-Body SO
(S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

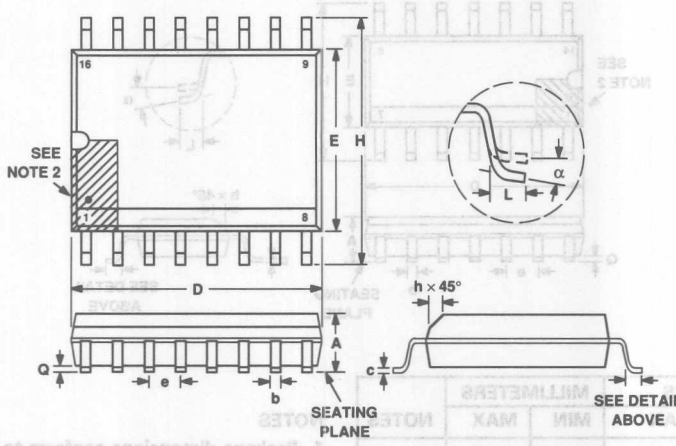
NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

10

R-16 (S-Suffix)

16-Lead Wide-Body SO
(SOL-16)



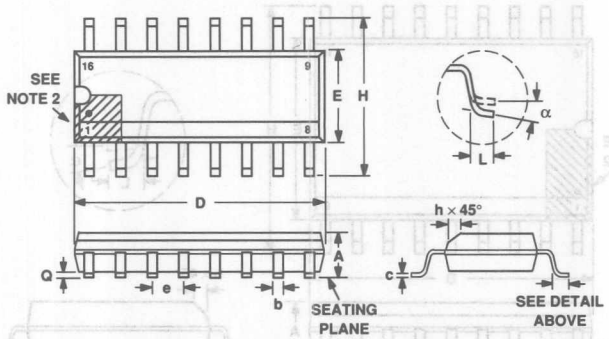
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-16A (S-Suffix)

16-Lead Narrow Body SO
(SO-16)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

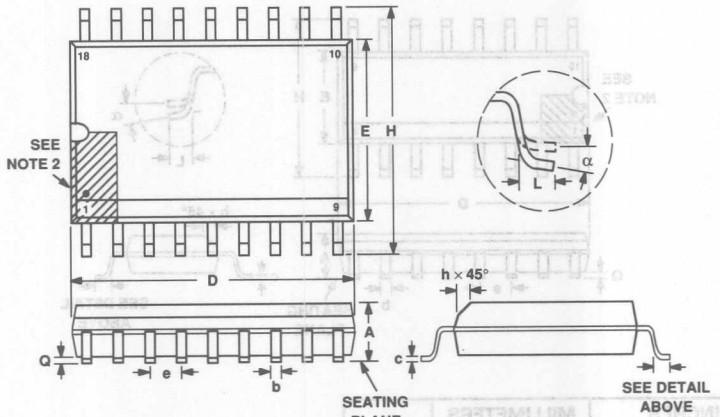
NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

10

R-18 (S-Suffix)

18-Lead Wide-Body SO
(SOL-18)



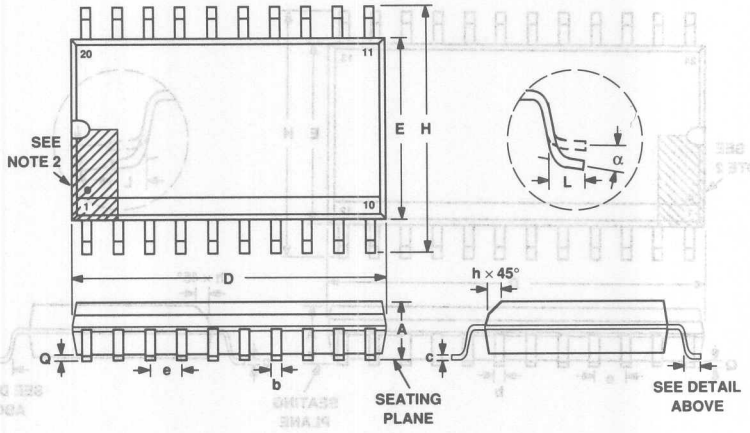
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4469	0.4625	11.35	11.75	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AB (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-20 (S-Suffix)

20-Lead Wide-Body SO
(SOL-20)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

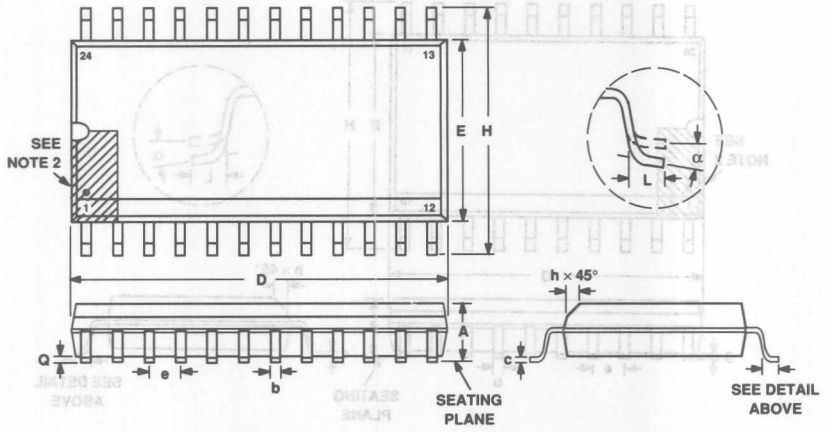
NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

10

R-24 (S-Suffix)

24-Lead Wide-Body SO
(SOL-24)



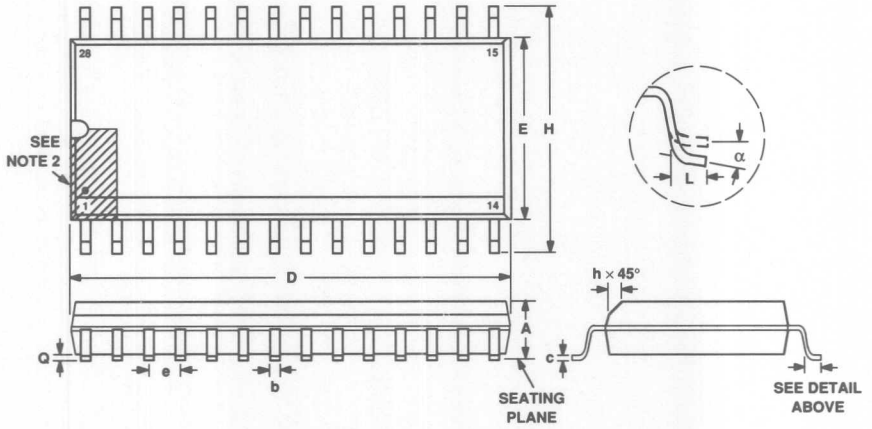
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AD (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-28 (S-Suffix)

28-Lead Wide-Body SO
(SOL-28)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

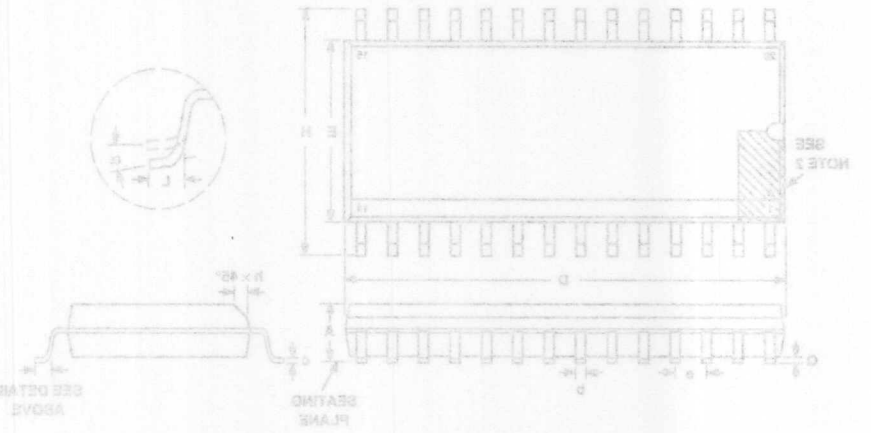
NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AE (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

10

R-28 (S-Suffix)

28-Lead Wide-Body SO
(SOL-28)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0128	0.0192	0.33	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AE (Issue A, June 1995).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

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Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multioption subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number*, an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

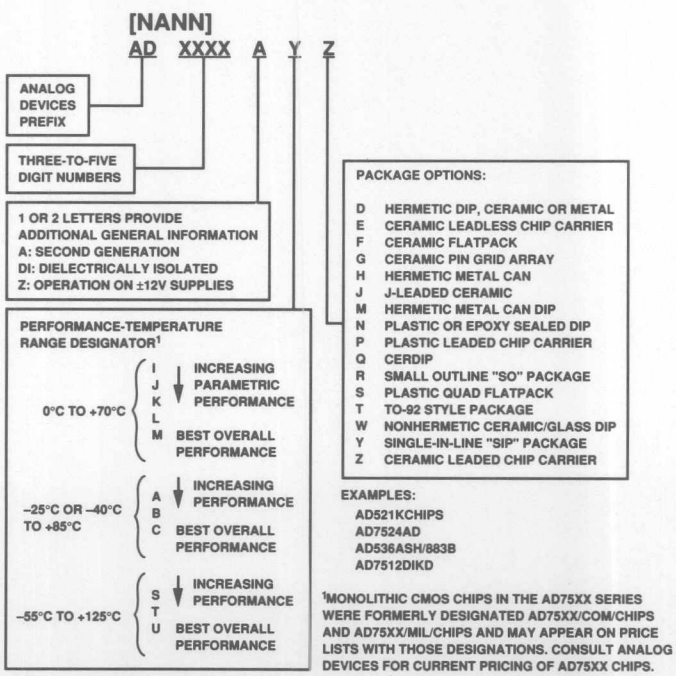


Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter][two or three digits] is used instead of ADXXXX, e.g., 2S80.**

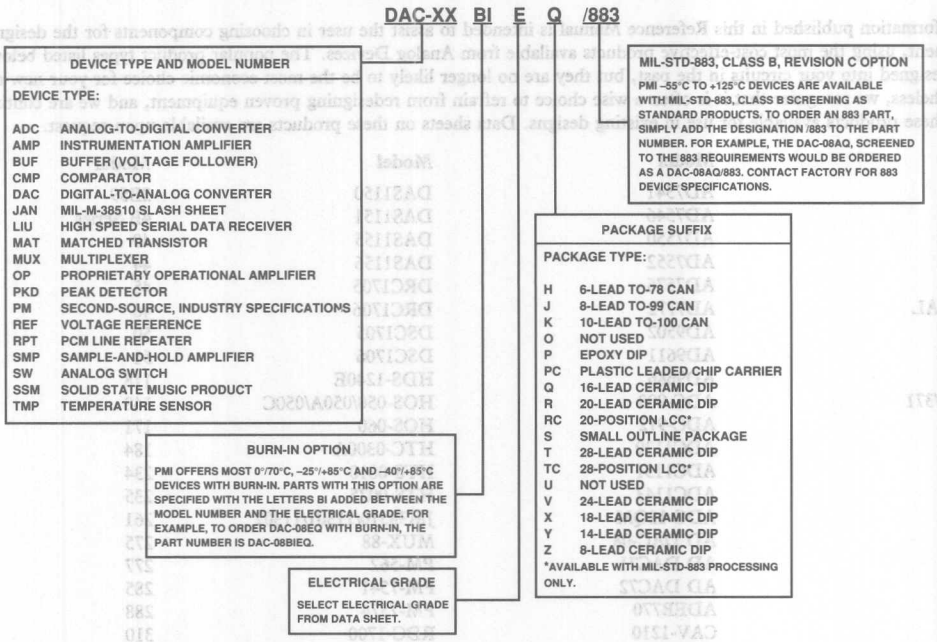


Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via FAX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. Analog Devices' minimum order value is two hundred fifty dollars ($250.00).

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

You may also order Analog Devices parts through distributors. For information on distributors, please see pages 11–12 and 11–13 at the back of this volume.

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WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and µMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Reference Manual (But Still Available)

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model
AD101	AD7541	DAS1150	2B59
AD201	AD7546	DAS1151	4B Series
AD293	AD7550	DAS1155	40
AD294	AD7552	DAS1156	44
AD301	AD7576	DRC1705	45
AD301AL	AD7772	DRC1706	46
AD367	AD9502	DSC1705	50
AD368	AD9611	DSC1706	51
AD369	AD9686	HDS-1240E	118
AD370/371	ADC-908	HOS-050/050A/050C	148
AD392	ADC-912	HOS-060	171
AD503	ADC1130	HTC-0300A	184
AD504	ADC1131	HTS-0010	234
AD506	ADC1143	HTS-0025	235
AD510	ADC-12QM	JM38510/11301/11302	261
AD515	AD DAC-08	MUX-88	275
AD518	AD DAC71	PM-562	277
AD533	AD DAC72	PM-7541	285
AD535	ADEB770	PM-7574	288
AD545	CAV-1210	RDC-1700	310
AD567	DAC-QS	RDC-1702	429
AD611	DAC-QZ	RDC-1704	433
AD651	DAC-01	RDC-1725	434
AD1147	DAC-02/03	RDC-1726	435
AD1148	DAC-05/06	RDC-1768	436
AD1403	DAC-10Z	RTM Series	440
AD2004	DAC-12M	SDC1700	442
AD2006	DAC-12QS	SDC1702	450
AD2008	DAC-12QZ	SDC1704	451
AD2009	DAC-20	SDC1725	452
AD2016	DAC71/72	SDC1726	453
AD2020	DAC-86	SDC1768	458
AD2033	DAC-88	SHA-5	460
AD2040	DAC-89	SHA-1134	603
AD3554	DAC-210	SHA-1144	751
AD3860	DAC-888	SMP-81	756
AD5200 Series	DAC1108	STM Series	903
AD5210 Series	DAC1136	SW-01/02	906
AD7110	DAC1138	SW-7510/7511 2B24	915
AD7240	DAC1146	2B34	926
AD7520	DAC-1408A	2B35	947
AD7521	DAC1420	2B50	959
AD7522	DAC1422	2B52	968
AD7523	DAC1423	2B53	972
AD7525	DAC1508A	2B56	
AD7530	DAC-8212	2B57	
AD7531	DAS1128	2B58	

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent
AD108/208/308	AD705
AD108A/208A/308A	AD705
AD111/211/311	AD790
AD345	AD1321/1322
AD351	AD790
AD362	AD1362
AD376	AD1376
AD501	AD711
AD502	AD711
AD505	AD509
AD508	AD517
AD511	AD711
AD512	AD711
AD513	AD711
AD514	AD711
AD516	AD711
AD520	AD524
AD523	AD549
AD528	AD711/744
AD530	AD533
AD531	AD532
AD540	AD544
AD559	AD557/AD558
AD565	AD565A
AD566	AD566A
AD612	AD524
AD614	AD524
AD689	AD586
AD801	AD711
AD810-813	None
AD814-816	None
AD818	None
AD820-822	None
AD830-833	None
AD835-839	None
AD1145	AD7846
AD1408	AD558
AD1508	AD558
AD1678	AD678
AD1679	AD679
AD1779	AD779
AD2003	AD2021
AD2022	None
AD2023	None
AD2024	None
AD2025	None
AD2027	None
AD2028	None
AD2036	None
AD2037	None
AD2038	None
AD5010/6020	AD9000
AD6012	AD565A
AD7115	AD7111
AD7513	ADG201A
AD7516	AD7510DI
AD7519	None
AD7527	AD7548
AD7544	AD7548
AD7555	AD1175K
AD7560	None
AD7570	AD7579/AD7580
AD7571	AD7579/AD7580
AD7583	AD7880+MUX
AD9011	AD9002
AD9521	AD640
AD9615	AD9611/AD9617
AD9685	AD96685
AD9687	AD96686
AD9688	AD9002/AD9028
AD ADC-816	AD7820/AD7821
ADC-8S	AD673
ADC-10Z	AD574A
ADC-12QL	AD7578
ADC-12QZ	AD574A/AD674A
ADC-14I/17I	AD1170
ADC-1100	AD7550/AD7552
ADC1102	AD7870
ADC1103	AD7572A
ADC1105	AD7550/AD7552
ADC1109	AD7572A
ADC1111	AD574A
ADC1121	AD7880
ADC1123	AD7880
ADC1133	AD574A
ADC-QM	AD574A/AD674A
ADC-QU	AD574A/AD674A
AD DAC100	AD561
ADG200	None
ADG201	ADG201A
ADLH0032G/CG	AD843
ADLH0033G/CG	AD9620/AD9630
ADM501	None
ADP501	None
ADREF01	REF-01
ADREF02	REF-02
ADSHC-85	AD585
ADSHM-5	HTC-0300A
AMP-01BX	AMP-01AX
AMP-01BX/883C	AMP-01AX/883C
AMP-05BX	AMP-05AX
AMP-05BX/883C	AMP-05Z/883C
API1620/1718	Consult ADI
BDM 1615/16/17	None
BUF-03BJ/883C	BUF-03AJ/883C
CAV-0920/1020	AD9020/9060
CAV-1202	AD9005
CAV-1205	AD9005
CMP-01Z	CMP-01J
CMP-05BJ	CMP-05CJ
CMP-05BZ	CMP-05CZ
CMP-05GJ	CMP-05CJ
CMP-404BY	CMP-404AY
CMP-404BY/883C	CMP-404AY/883C
DAC-02ACX1	DAC-02CCX1
DAC-05AX1	DAC-02CCX1
DAC-05EX1	DAC-02CCX1
DAC-10BX	DAC-10FX
DAC-10CX	DAC-10GX
DAC-10DF	AD568
DAC-10H	DAC-10Z
DAC-14QM	DAC1136
DAC-16QM	DAC1136
DAC-100AAQ7	DAC-100ACQ7
DAC-100AAQ8	DAC-100ACQ8
DAC-100ABQ7	DAC-100ACQ7
DAC-100ABQ8	DAC-100ACQ8
DAC-100BBQ5/883C	DAC-100ACQ5/883C
DAC-100BCQ7	DAC-100BBQ7
DAC-100DDQ7	DAC-100CCQ7
DAC-312BR	DAC-312ER
DAC-888AX	DAC-888EX
DAC-888BX	DAC-888EX
DAC1009	AD767
DAC1106	AD568
DAC1112	DAC12QS
DAC1118	AD767
DAC1122	AD7541A
DAC1125	AD7533
DAC1132	AD667
DAC-1408-6P	DAC-1408-8P
DAC-1408-7P	DAC-1408-8P
DAC-1408-7Q	DAC-1408-8Q
DAC-1408-GQ	DAC-1408-8Q
DAC-1508A-8Q	DAC-1408-8Q
DRC1605/06	DRC1705/06; SDC1740

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
DRC1765/66	AD2S65/66	OP-02EZ	OP-177GZ	PM-157J	PM-175J/883C
DSC1605/06	DSC1705/06; SDC1740	OP-02J	OP-02AJ	PM-157J/883C	PM-157AJ/883C
DSC1765/66	AD2S65/66	OP-02/883C	OP-02AZ/883C	PM-208AJ	PM-108AJ/883C
DTM1716/17	AD2S65/66	OP-04DY	OP-04CY	PM-208AZ	PM-108AZ
HAS-0802	HAS1202A	OP-04GBC	OP-04NBC	PM-308AZ	PM-1008GZ
HAS-1002	HAS1202A	OP-04Y/883C	OP-04AY/883C	PM-308J	PM-1008G
HAS-1202	HAS1202A	OP-05Z	OP-05AZ	PM-4136RC	OP-11ARC/883C
HDD-1015	AD9712A	OP-05/883C	OP-05AZ/883C	PM-562AV	PM-562HV
HDD-1409	None	OP-06BJ/883C	OP-06AJ/883C	PM-562BV	PM-562HV
HDG-0805	AD9701	OP-06EZ	OP-06GZ	PM-562FV	PM-562HV
HDH-0802	AD9713A	OP-06FZ	OP-06GZ	PM-562GV	PM-562HV
HDH-1003	AD9713A	OP-08AJ	PM-1008AJ	PM-741J	OP-02AJ
HDH-1205	AD9713A	OP-08AJ/883C	PM-1008AJ/883C	RAC1763	None
HDL-3805	ADV453/ADV478	OP-08AZ/883C	PM-1008AZ/883C	RDC1602/03	RDC1702/03
HDL-3806	ADV453/ADV478	OP-08CZ/883C	PM-1008AZ/883C	RDC1711	None
HDM-1210	AD668/AD9713A	OP-08EJ	PM-1008EJ	RDC1721	AD2S46
HDS-0810E	AD9712A	OP-08EZ	PM-1008EZ	RDC1767	RDC1768
HDS-0820	AD9713A	OP-09ARC/883C	OP-11ARC/883C	RSCT1621	AD2S80A/82A
HDS-1015E	AD9712A	OP-09FY	OP-09EY	RTI-1200	RTI-711 Series
HDS-1025	AD9713A	OP-12BZ	OP-12AZ	RTI-1201	RTI-711 Series
HDS-1250	AD668/AD9713A	OP-12CZ	OP-12AZ	RTI-1202	RTI-711 Series
HOS-100AH/SH	None	OP-12GZ	OP-12FZ	RTM1630-34	RTM1680/83
HOS-200	AD9620/30	OP-14DZ	OP-14CZ	RTM1636	Consult ADI
HTC-0300	HTC-0300A	OP-14GRBC	OP-14GBC	RTM1660/63/71/72	Consult ADI
HTC-0500	HTC-0300A	OP-14J/883C	OP-14AJ/883C	RTM1679	None
IPA-1751	IPA-1764	OP-15BJ	OP-15AJ	RTM1681/86/87/89	Consult ADI
IRDC1730-33	AD2S80A/82A	OP-15BZ	OP-15AZ	RTM1690/96	Consult ADI
MAH-0801	AD9005	OP-16BJ	OP-16AJ	RTM1697	None
MAH-1001	AD9005	OP-17BZ/883C	OP-17AZ/883C	RTM1736/37	RDC1740 + CCT
MAS-0801	AD9005	OP-17CJ	OP-17AJ	SAC1763	None
MAS-1001	AD9005	OP-17FJ	OP-17EJ	SBCD1752/53/56/57	None
MAS-1202	AD9005	OP-17FZ	OP-17EZ	SCDX1623	None
MAT-01/883C	MAT-01AH/883C	OP-20CJ	OP-20BJ	SCM1677	None
MAT-02BH	MAT-02AH	OP-21GRBC	OP-21GBC	SDC1602/3/4	SDC1702/03/04/40
MAT-02BH/883C	MAT-02AH/883C	OP-215BJ	OP-215AJ	SDC1711	None
MATV-0811	AD9012/48	OP-215BJ/883C	OP-215AJ/883C	SDC1721	AD2S46
MATV-0816	AD9012/48	OP-215BZ	OP-215AZ	SDC1767	SDC1768
MATV-0820	AD9012/48	OP-215CZ/883C	OP-215BZ/883	SERDEX	µMAC-5000
MCI-1794	AD2S80A/82A	OP-21BJ	OP-21AJ	SHA-1A	AD585
MDA Family	AD9712A/13A	OP-21BZ	OP-21AZ	SHA-2A	AD781
MDH Family	AD9712A/13A	OP-21EJ	OP-21AJ	SHA-3	AD585
MDMS Family	AD9712A/13A	OP-220BJ	OP-220AJ	SHA-4	AD585
MDS Family	AD9712A/13A	OP-22AJ	OP-22AJ/883C	SHA-6	AD1154
MDSL Family	AD9712A/13A	OP-22EJ	OP-22AJ/883C	SHA1114	AD585
MOD-1005/20	AD9020/60	OP-32BZ	OP-32AZ	SMP-10BY	SMP-10AY
MUX-08AQ	MUX-08BQ	OP-32BZ/883C	OP-32AZ/883C	SMP-10BY/883C	SMP-10AY/883C
MUX-24AQ	MUX-24EQ	OP-32FZ	OP-32EZ	SPA-1695	None
MUX-24BQ	MUX-24FQ	OP-50BY	OP-50AY	SSCT1621	AD2S80A/82A
MUX-16AT	MUX-16ET	OP-50BY/883C	OP-50AY/883C	SSCT1622/23	None
MUX-16BT	MUX-16FT	OSC-1754	OSC-1758	STM1630-34	STM1680/83
OP-01HJ	OP-01J	PKD-01BY	PKD-01AY	STM1636	Consult ADI
OP-01HZ	OP-01HP	PKD-01BY/883C	PKD-01AY/883C	STM1660/63/71/72	Consult ADI
OP-02BJ	OP-02AJ	PM-111Y	PM-111J	STM1679	None
OP-02BJ/883C	OP-02AJ/883C	PM-11Y/883C	PM-111J/883C	STM1681/86/87/89	Consult ADI
OP-02EJ	OP-07DJ	PM-139AY	PM-139AY/883C	STM1690/96	Consult ADI
OP-02EP	OP-177GP	PM-156AZ	PM-156AZ/883C	STM1697	None

Model	Closest Recommended Equivalent
STM1736/37	SDC1740 + CCT
SW-01BQ	SW-01FQ
SW-7510AQ	SW-7510EQ
SW-7510BQ	SW-7510FQ
SW-7511AQ	SW-1577BQ
THC-Family	HTC-0300A
THS-Family	HTC-0300A
TSL1612	Consult ADI
1S10/20	1S40; AD2S80A/82A
1S14/24/44/64	1S74
1S61	1S60; AD2S80A/82A
2S20	AD2S80A/82A
5S70/5S72	AD2S75
9S70/71/72	None
9S75/76/79	None
41	AD515A
42	AD549
43	AD549
47	AD845
48	AD845
52	AD707
102	AD845
106	118
107	118
108	AD845
110	AD845
120	50
141	40
142	AD845
143	AD845
146	AD382
149	50
153	AD517
161	None
163	None
165	None
170	None
180	AD OP-07
183	184
220	234
230	235
231	233
232	235
233	None
260	AD707
272	None
273	None
276	None
274J	284J
279	286J
280	281
282J	292A
283J	292A
287	None
301	310 (Module)
302	310 (Module)
311	AD549
350	None
424	435/AD534
426	AD534
427	None
428	AD538
432	None
454	AD537
456	AD537
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
605	AD524
606	AD625
610	AD625
752	759
901	904
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AD580	C II 6–5
AD581	C II 6–9
AD582	C II 4–29
AD583	C II 4–33
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AD586	C II 6–23
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AD592	L
AD594/595	L
AD596/597	L
AD598	L
AD611	L
AD624	L
AD625	L
AD630	L
AD632	L
AD633	L
AD636	L
AD637	L
AD639	L
AD640	L
AD642	L
AD644	L
AD645	L
AD647	L
AD648	L
AD650	C II 3–15
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AD654	C II 3–43
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AD668	C I 2–123
•AD669	C I 2–139
AD670	C II 2–69
AD671	C II 2–81
AD673	C II 2–97
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•AD674B	C II 2–109
•AD675	C II 2–121
•AD676	C II 2–123
AD678	C II 2–137
AD679	C II 2–149
•AD680	C II 6–55
•AD682	C II 4–41
AD684	C II 4–49
•AD688	C II 6–63
AD693	L
AD694	L
AD704	L
AD705	L
AD706	L
AD707	L
AD708	L
AD711	L
AD712	L
AD713	L
AD734	L
AD736	L
AD737	L
AD741	L
AD743	L
AD744	L
AD746	L
•AD766	C I 2–151
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AD790	L
AD827	L
AD829	L
AD834	L
AD840	L
AD841	L
AD842	L
AD843	L
AD844	L
AD845	L
AD846	L
AD847	L
AD848	L
AD849	L
AD880	L
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AD892	L
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AD1362	C II 7–41
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AD1377	C II 2–215
•AD1378	C II 2–223
AD1380	C II 2–231
•AD1382	C II 2–239
•AD1385	C II 2–255
AD1403/1403A	C II 6–71
•AD1671	C II 2–259
•AD1674	C II 2–269
•AD1851	C I 2–173
AD1856	C I 2–183
AD1860	C I 2–191
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AD2006	D
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AD2020	D
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AD2026	C I 5–11
AD2033	D
AD2040	D
AD2700	C II 6–75
AD2701	C II 6–75
AD2702	C II 6–75
AD2710	C II 6–79
AD2712	C II 6–79
AD3554	L
AD3860	D
AD5200 Series	D
AD5210 Series	D
AD5240	C II 2–809
AD5539	L
•AD7001	C I 4–47
•AD7002	C I 4–59
•AD7005	C I 4–75
•AD7008	C I 4–91
AD7110	D
AD7111	C I 2–247
AD7118	C I 2–253
AD7224	C I 2–259
AD7225	C I 2–279
AD7226	C I 2–291
AD7228	C I 2–323
•AD7228A	C I 2–331
•AD7233	C I 2–339
AD7237	C I 2–347
AD7240	D
•AD7242	C I 2–359
•AD7243	C I 2–371
•AD7244	C I 2–359
AD7245	C I 2–383
•AD7245A	C I 2–385
AD7247	C I 2–347
AD7248	C I 2–383
•AD7248A	C I 2–385
•AD7306	C I 4–93
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AD7521	D
AD7522	D
AD7523	D
AD7524	C I 2–399
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AD7531	D
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AD7547	C I 2–593
AD7548	C I 2–601
AD7549	C I 2–629
AD7550	D
AD7552	D
•AD7564	C I 2–637
•AD7568	C I 2–645
AD7569	C II 8–7
AD7572	C II 2–299
•AD7572A	C II 2–303
AD7574	C II 2–315
AD7575	C II 2–323
AD7576	D
AD7578	C II 2–335
AD7579	C II 2–347
AD7580	C II 2–347
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•AD7701	C II 2–403
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•AD7778	C II 2–509
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AD7824	C II 2–533
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•AD7837	C I 2–681
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AD7848	C I 2–735
•AD7868	C II 8–79
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AD7870	C II 2–545
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•AD7875	C II 2–545
•AD7876	C II 2–545
AD7878	C II 2–595
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•AD9032	C II 2–765
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AD9501	L
AD9502	D
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•AD9713A	C I 2–761
•AD9720	C I 2–765
•AD9721	C I 2–765
AD9768	C I 2–769
AD9901	C I 4–115
•AD9950	C I 4–123
•AD22001	L
•AD22050	L
•AD22100	L
•AD22150	L
•AD22180	L
•AD22181	L
AD75004	C I 2–773, C I 8–1, C II 9–1
•AD75019	C II 5–39
AD75068	C I 8–1, C II 9–1
•AD75069	C I 2–777
•AD75089	C I 2–777
•AD75090	C I 2–777
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AD96687	L
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AD ADC80	C II 2–803
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•ADC-170	C II 2–817
ADC-908	D
ADC-910	C II 2–819
ADC-912	D
•ADC-912A	C II 2–831
ADC1130/1131	D
ADC1140	C II 2–843
ADC1143	D
AD DAC-08	D
AD DAC71	D
AD DAC72	D
AD DAC80	C I 2–783
AD DAC85	C I 2–783
AD DAC87	C I 2–783
•ADDS-21XX-SW	D
•ADDS-2100A-ICE	D
ADDS-2101-ICE	D
•ADDS-2101-EZ	D
•ADDS-2111-EZ	D
ADG201A	C II 5–43
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ADG202A	C II 5–43
ADG211A	C II 5–57

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AD OP-27	L
AD OP-37	L
ADSP-824ROM	D
ADSP-1008A	D
ADSP-1009A	D
ADSP-1010A	D
ADSP-1010B	D
ADSP-1012A	D
ADSP-1016A	D
ADSP-1024A	D
ADSP-1080A	D
ADSP-1081A	D
ADSP-1101	D
ADSP-1110A	D
ADSP-1401	D
ADSP-1402	D
ADSP-1410	D
ADSP-2100	D
ADSP-2100A	C I 6–2
ADSP-2101	C I 6–2
ADSP-2102	C I 6–2
•ADSP-2105	C I 6–2
•ADSP-2106	C I 6–2
•ADSP-2111	C I 6–2
•ADSP-2112	C I 6–2
•ADSP-21msp50	C I 6–2
•ADSP-21msp51	C I 6–2
ADSP-3128A	D
ADSP-3201	D
ADSP-3202	D
ADSP-3210	D
ADSP-3211	D
ADSP-3212	D

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ADSP-3221	D
ADSP-3222	D
•ADSP-21000-SW	D
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ADV453	C I 2–799
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•ADV473	C I 2–805
•ADV475	C I 2–827
ADV476	C I 2–817
•ADV477	C I 2–827
ADV478	C I 2–839
•ADV7120	C I 2–851
•ADV7121	C I 2–857
•ADV7122	C I 2–857
•ADV7141	C I 2–869
•ADV7146	C I 2–869
•ADV7148	C I 2–869
•ADV7150	C I 2–889
•ADV7151	C I 2–907
•ADV7152	C I 2–889
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AMP-02	P
AMP-03	P
AMP-05	P
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BUF-03	P
CAV-1210	D
CMP-01	P
CMP-02	P
CMP-04	P
CMP-05	P
CMP-08	P
CMP-404	P
DAC-QS	D
DAC-QZ	D
DAC-01	D
DAC-02/03	D
DAC-05	C I 11–4, C II 12–4
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DAC-08	C I 2–923
DAC-10	C I 2–935
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DAC-12M	D
DAC-12QS	D
DAC-12QZ	D
•DAC-16	C I 2–943
DAC-20	D
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DAC-89	D
DAC-100	C I 2–945
DAC-210	D
DAC-312	C I 2–953
DAC-888	D
DAC1108	D
DAC1136	D
DAC1138	D
DAC1146	D
DAC-1408A	D
DAC1420	D
DAC1422	D
DAC1423	D
DAC-1508A	D
DAC-8012	C I 2–967
DAC-8043	C I 2–977
DAC-8143	C I 2–987
DAC-8212	D
DAC-8221	C I 2–1001
DAC-8222	C I 2–1015
DAC-8228	C I 2–1029
DAC-8229	C I 2–1041
DAC-8248	C I 2–1053
DAC-8408	C I 2–1069
DAC-8412	C I 2–1083
•DAC-8413	C I 2–1083
DAC-8426	C I 2–1095
DAC-8800	C I 2–1107
DAC-8840	C I 2–1121
•DAC-8841	C I 2–1131
DAS1128	D
DAS1150	D
DAS1151	D
DAS1152	C II 7–65
DAS1153	C II 7–65
DAS1155	D
DAS1156	D
DAS1157	C II 7–69
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DRC1706	D
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HDS-1240E	D
HOS-050A	L
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HTC-0300A	D
HTS-0010	D
HTS-0025	D
•IPA1764	C I 3–115
LIU-01	C I 4–135
LTS-0614	L
LTS-0655	L
LTS-0680	L
LTS-2020	L
LTS-2101	L
LTS-2200	L
LTS-2302	L
LTS-2510	L
LTS-2600	L
LTS-2700	L
LTS-2800	L
MAT-01	P
MAT-02	P
MAT-03	P
MAT-04	P
MUX-08	C II 5–111
MUX-16	C II 5–123
MUX-24	C II 5–111
MUX-28	C II 5–123
MUX-88	D
OP-01	P
OP-02	P
OP-04	P
OP-05	P
OP-06	P
OP-07	P
OP-09	P
OP-10	P
OP-11	P
OP-12	P
OP-14	P
OP-15	P
OP-16	P
OP-17	P
OP-20	P
OP-21	P
OP-22	P
OP-27	P
OP-32	P
OP-37	P
OP-41	P
OP-42	P
OP-43	P
OP-44	P
OP-50	P
OP-61	P
OP-64	P

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OP-80	P
OP-90	P
OP-97	P
OP-160	P
OP-177	P
OP-200	P
OP-207	P
OP-215	P
OP-220	P
OP-221	P
OP-227	P
OP-249	P
OP-260	P
OP-270	P
OP-271	P
•OP-282	P
OP-290	P
OP-297	P
OP-400	P
OP-420	P
OP-421	P
OP-470	P
OP-471	P
•OP-482	P
OP-490	P
•OSC1758	C I 3–117
PKD-01	P
PM-108	P
PM-111	P
PM-119	P
PM-139	P
PM-148/248	P
PM-155	P
PM-155A	P
PM-156	P
PM-156A	P
PM-157	P
PM-157A	P
PM-1008	P
PM-1012	P
PM-2108	P
•PM-6012	C I 2–1141
PM-7224	C I 2–267
PM-7226	C I 2–303
PM-7226A	C I 2–303
PM-7524	C I 2–405
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PM-7628	C I 2–665
PM-7645	C I 2–573
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REF-02	C II 6–91
REF-03	C II 6–99
REF-05	C II 6–107
REF-08	C II 6–113
REF-10	C II 6–121
REF-43	C II 6–127
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RPT-83	C I 4–147
RPT-85	C I 4–155
RPT-86	C I 4–163
RPT-87	C I 4–163
RTM Series	D
SDC1700/RDC1700	D
SDC1702/RDC1702	D
SDC1704/RDC1704	D
SDC1725/RDC1725	D
SDC1726/RDC1726	D
SDC1740/RDC1740	C I 3–119
SDC1741/RDC1741	C I 3–119
SDC1742/RDC1742	C I 3–119
SDC1768/RDC1768	D
SHA-5	D
SHA-1134	D
SHA-1144	D
SMP-04	C II 4–87
SMP-08	C II 4–101
SMP-10	C II 4–109
SMP-11	C II 4–109
●SMP-18	C II 4–119
SMP-81	D
SSM-2013	P
SSM-2014	P
SSM-2015	P
SSM-2016	P
SSM-2017	P
SSM-2018	P
SSM-2024	P
SSM-2100	P
SSM-2110	P
SSM-2120	P
SSM-2122	P
SSM-2131	P
SSM-2132	P
SSM-2134	P
SSM-2139	P

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SSM-2141	P
SSM-2142	P
SSM-2210	P
SSM-2220	P
SSM-2300	P
SSM-2402	C II 5–133
●SSM-2404	C II 5–147
SSM-2412	C II 5–133
STM Series	D
SW-01	D
SW-02	D
SW-06	C II 5–149
SW-201	C II 5–161
SW-202	C II 5–161
SW-7510	D
SW-7511	D
1B21	L
1B22	L
1B31	L
1B32	L
1B41	L
1B51	L
●1S74	C 3–127
2B20	L
2B22	L
2B23	L
2B24	L
2B30	L
2B31	L
2B34	L
2B35	L
2B50	L
2B52	L
2B53	L
2B54/2B55	L
2B56	L
2B57	L
2B58	L
2B59	L
2S50	C I 3–135
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4B Series	L
5B Series	L
6B Series	L
●7B Series	L
40	L

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44	L
45	L
46	L
50	L
51	L
118	L
148	L
171	L
184	L
234	L
235	L
261	L
275	L
277	L
281	L
284J	L
285	L
286J	L
288	L
289	L
290A	L
292A	L
310	L
429	L
433	L
434	L
435	L
436	L
440	L
442	L
450	D
451	D
452	D
453	D
458	D
460	D
741A/PM741	P
751	D
755	L
756	L
757	L
759	L
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906	D
915	D
920	C I 9–1, C II 10–1
921	C I 9–1, C II 10–1
922	C I 9–1, C II 10–1
923	C I 9–1, C II 10–1

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926	D
927	C I 9–1, C II 10–1
928	C I 9–1, C II 10–1
940	C I 9–2, C II 10–2
941	C I 9–2, C II 10–2
943	C I 9–2, C II 10–2
945	C I 9–2, C II 10–2
947	D
949	C I 9–2, C II 10–2
951	C I 9–2, C II 10–2
952	C I 9–1, C II 10–1
953	C I 9–2, C II 10–2
955	C I 9–1, C II 10–1
958	C I 9–2, C II 10–2
959	D
960	C I 9–2, C II 10–2
962	C I 9–2, C II 10–2
964	C I 9–2, C II 10–2
965	C I 9–2, C II 10–2
966	C I 9–2, C II 10–2
967	C I 9–2, C II 10–2
968	D
970	C I 9–1, C II 10–1
972	D
973	C I 9–1, C II 10–1
974	C I 9–1, C II 10–1
975	C I 9–1, C II 10–1
976	C I 9–1, C II 10–1
977	C I 9–1, C II 10–1

●New product since publication of the most recent Databooks.

*C I = *Data Converter Reference Manual, Volume I;* C II = *Data Converter Reference Manual, Volume II*; D = Data sheet available, consult factory; L = *Linear Products Databook*; P = *Precision Monolithics Division Databook.*

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44	L
45	L
46	L
50	L
51	L
118	L
148	L
171	L
184	L
234	L
235	L
261	L
275	L
277	L
281	L
284[1]	L
285	L
286[1]	L
288	L
289	L
290A	L
292A	L
310	L
429	L
433	L
434	L
435	L
436	L
440	L
442	L
450	D
451	D
452	D
453	D
458	D
460	D
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751	D
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905	C I 9-1, C II 10-1
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920	C I 9-1, C II 10-1
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922	C I 9-1, C II 10-1
923	C I 9-1, C II 10-1

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927	C I 9-1, C II 10-1
928	C I 9-1, C II 10-1
940	C I 9-2, C II 10-2
941	C I 9-2, C II 10-2
943	C I 9-2, C II 10-2
945	C I 9-2, C II 10-2
947	D
949	C I 9-2, C II 10-2
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952	C I 9-1, C II 10-1
953	C I 9-2, C II 10-2
955	C I 9-1, C II 10-1
958	C I 9-2, C II 10-2
959	D
960	C I 9-2, C II 10-2
962	C I 9-2, C II 10-2
964	C I 9-2, C II 10-2
965	C I 9-2, C II 10-2
966	C I 9-2, C II 10-2
967	C I 9-2, C II 10-2
968	D
970	C I 9-1, C II 10-1
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973	C I 9-1, C II 10-1
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977	C I 9-1, C II 10-1

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